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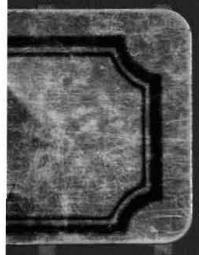
Linear Applications Handbook



Linear Applications Numerical List (Continued)

Application Notes		Date	Revision Date	Page
AN-225	IC Temperature Sensor Provides Thermocouple Cold-Junction Compensation	4/79	—	443
AN-227	Applications of Wideband Buffers	10/79	3/91	449
AN-233	The A/D Easily Allows Many Unusual Applications	1/80	—	465
AN-236	An Introduction to Sampling Theorem	1/80	6/86	469
AN-237	Convolution: Digital Signal Processing	1/80	6/86	481
AN-240	Wide-Range Current-to-Frequency Converters	5/80	8/90	489
AN-241	Working with High Impedance Op Amps	2/80	3/91	495
AN-242	Applying a New Precision Op Amp	4/80	10/90	501
AN-245	Application of the ADC-1210 CMOS A/D Converter	—	6/86	523
AN-247	Using the ADC0808/ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Analog Multiplexer	9/80	6/86	531
AN-253	LH0024 and LH0032 High Speed Op Amp Applications	/80	—	547
AN-255	Power Spectrum Estimation	11/80	—	558
AN-256	Circuitry for Inexpensive Relative Humidity Measurement	8/81	—	586
AN-258	Data Acquisition Using the ADC0816 and ADC0817 8-Bit A/D Converter with On-Chip 16 Channel Multiplexer	1/81	6/86	590
AN-260	A 20-Bit (1 ppm) Linear Slope-Integrating A/D Converter	1/81	—	612
AN-261	Low Distortion Wideband Power Op Amp	7/81	8/90	618
AN-262	Applying Dual and Quad FET Op Amps	5/81	6/86	627
AN-263	Sine Wave Generation Techniques	3/81	3/91	634
AN-265	An Electronic Watt-Watt Hour Meter	2/84	6/86	646
AN-266	Circuit Applications of Sample-Hold Amplifiers	1/81	6/86	651
AN-269	Circuit Applications of Multiplying CMOS A/D Converters	9/81	6/86	659
AN-271	Applying the New CMOS MICRO-DAC	9/81	6/86	664
AN-272	Op Amp Booster Designs	9/81	6/86	674
AN-274	CMOS A/D Converter Interfaces Easily with Many Microprocessors	7/81	6/86	681
AN-275	CMOS D/A Converters Match Most Microprocessors	7/81	—	685
AN-276	A New Low-Cost Sampled Data 10-Bit CMOS A/D Converter	7/81	—	690
AN-277	The New MICRO-DAC Product Line for Microprocessor Systems	7/81	6/86	695
AN-278	Designing with a New Super Fast Dual Norton Amplifier	9/81	6/86	701
AN-280	A/D Converters Easily Interface with 70 Series Microprocessors	11/81	—	709
AN-281	Data Acquisition Using INS8048	11/81	6/86	715
AN-284	Single-Supply Applications of CMOS MICRO-DACs	9/81	3/91	720
AN-285	An Acoustic Transformer Powered Super-High Isolation Amplifier	10/81	6/86	724
AN-286	Applications of the LM392 Comparator Op Amp IC	9/81	6/86	728
AN-288	System-Oriented DC-DC Conversion Techniques	4/82	6/86	734
AN-292	Applications of the LM3524 Pulse-Width Modulator	8/82	6/86	739
AN-293	Control Applications of CMOS DACs	3/82	6/86	744
AN-294	Special Sample and Hold Techniques	4/82	6/86	750
AN-295	A High Performance Industrial Weighing System	3/82	6/86	754
AN-298	Isolation Techniques for Signal Conditioning	5/82	6/86	758
AN-299	Audio Applications of Linear Integrated Circuits	4/82	8/90	765
AN-300	Simple Circuit Detects Loss of 4 mA–20 mA Signal	5/82	—	770
AN-301	Signal Conditioning for Sophisticated Transducers	1/82	—	774
AN-307	Introducing the MF 10: A Versatile Monolithic Active Filter Building Block	8/82	8/90	786
AN-311	Theory and Applications of Logarithmic Amplifiers	7/82	4/91	797
AN-336	Understanding Integrated Circuit Package Power Capabilities	3/83	—	802
AN-343	LH1605 Switching Regulator	9/83	6/86	807
AN-344	LF13006/LF13007 Precision Digital Gain Set Applications	3/84	6/86	817
AN-346	High-Performance Audio Applications of the LM833	8/85	8/90	822
AN-384	Audio Noise Reduction and Masking	3/85	—	831
AN-386	A Non-Complementary Audio Noise Reduction System	3/85	—	837
AN-390	DNR® Applications of the LM1894	3/85	—	847
AN-391	The LM1823: A High Quality TV Video I.F. Amplifier and Synchronous Detector for Cable Receivers	3/85	—	856

National Semiconductor

Linear Applications Numerical List

Application Notes		Date	Revision Date	Page
AN-3	Drift Compensation Techniques for Integrated DC Amplifiers	11/67	6/86	1
AN-4	Monolithic Op-Amp—The Universal Linear Component	4/68	6/86	6
AN-13	Application of the LH0002 Current Amplifier	9/68	6/86	16
AN-20	An Application Guide for Op Amps	8/80	8/90	19
AN-23	The LM105—An Improved Positive Regulator	1/69	—	31
AN-24	A Simplified Test Set for Op Amp Characterization	1/86	6/86	39
AN-29	IC Op Amp Beats FETs on Input Current	12/69	3/91	49
AN-30	Log Converters	11/69	3/91	66
AN-31	Op Amp Circuit Collection	2/78	3/91	70
AN-32	FET Circuit Applications	2/70	6/86	94
AN-41	Precision IC Comparator Runs from +5V Logic Supply	10/70	8/90	107
AN-42	IC Provides On-Card Regulation for Logic Circuits	2/71	—	113
AN-46	The Phase Locked Loop IC as a Communications System Building Block	6/71	8/90	119
AN-48	Applications for a New Ultra-High Speed Buffer	8/71	—	133
AN-49	Pin Diode Drivers	/75	—	140
AN-56	1.2V Reference	12/71	—	146
AN-69	LM380 Power Audio Amplifier	12/72	—	150
AN-71	Micropower Circuits Using the LM4250 Programmable Op Amp	7/72	—	157
AN-72	The LM3900—A New Current-Differencing Quad + Input Amplifiers	9/72	6/86	166
AN-74	LM139/LM239/LM339—A Quad of Independently Functioning Comparators	1/73	—	211
AN-79	IC Pre-Amp Challenges Choppers on Drift	2/73	—	227
AN-82	LM125/LM126 Precision Dual-Tracking Regulators	8/80	6/86	235
AN-87	Comparing the High Speed Comparators	6/73	8/90	251
AN-88	CMOS Linear Applications	7/73	6/86	257
AN-97	Versatile Timer Operates from Microseconds to Hours	12/73	10/90	260
AN-103	LM340 Series Three Terminal Positive Regulators	8/80	—	272
AN-104	Noise Specs Confusing?	5/74	8/90	284
AN-110	Fast IC Power Transistor with Thermal Protection	5/74	—	291
AN-116	Use the LM158/258/358 Dual, Single Supply Op Amp	8/80	3/91	298
AN-127	LM143 Monolithic High Voltage Operation Amplifier Applications	4/76	—	302
AN-146	FM Remote Speaker System	6/75	8/90	314
AN-154	1.3V IC Flasher, Oscillator, Trigger or Alarm	12/75	3/91	318
AN-156	Specifying A/D and D/A Converters	2/76	6/86	333
AN-161	IC Voltage Reference Has 1 ppm per Degree Drift	6/76	—	339
AN-162	LM2907 Tachometer/Speed Switch Building Block Applications	6/76	8/90	345
AN-173	IC Zener Eases Reference Design	11/76	—	362
AN-178	Applications for an Adjustable IC Power Regulator	1/77	—	365
AN-181	3-Terminal Regulator is Adjustable	3/77	—	369
AN-182	Improving Power Supply Reliability with IC Power Regulators	4/77	—	375
AN-184	References for A/D Converters	7/77	—	378
AN-193	Single Chip Data Acquisition System Simplifies Analog to Digital Conversion	7/77	—	382
AN-200	CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor System	3/78	—	385
AN-202	A Digital Multimeter Using ADD3501	7/80	6/86	395
AN-210	New Phase-Locked Loops Have Advantage as Frequency to Voltage Converters (and more)	4/79	8/90	399
AN-211	New Op Amps Ideas	12/78	3/91	407
AN-222	Super Matched Bipolar Transistor Pair Sets New Standard for Drift and Noise	7/79	8/90	433

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LINEAR APPLICATIONS HANDBOOK

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

Many of the application schematics call out the generic family, identified by either the military temperature range version or commercial temperature range version of the device. Generally, any device in the generic family will work in the circuit. For example, an amplifier indicated as an LM108 refers to the generic "108" family, and does not imply that only military-grade devices will work in the application. Military (or industrial) and prime electrical ("A") grade devices need only be considered when their tighter electrical limits or wider temperature range warrants their use.

The temperature range of linear devices is indicated by either the first digit in the part number, or a letter following the base part number.

Grade	Specified Temperature Range	Part Number
Military	$-55°C \leq T_A \leq +125°C$	LM1XX or LMXXXM
Extended*	$-40°C \leq T_A \leq +125°C$	LMXXXE
Industrial*	$-25°C \leq T_A \leq +85°C$	LM2XX or LMXXXI
Commercial	$0°C \leq T_A \leq +70°C$	LM3XX or LMXXXC

**Some industrial temperature range devices may be rated for the extended (also known as automotive) temperature range. Other extended temperature range devices may not include a temperature range designation in their part number. Check the device datasheet for the specified temperature range(s).*

Because commercial parts are less expensive than military or industrial, these points should be kept in mind when trying to determine the most cost-effective approach to a given design.

Linear Applications Numerical List (Continued)

Application Notes		Date	Revision Date	Page
AN-402	LM2889 R.F. Modulator	6/85	6/86	872
AN-435	LMC835 Digital Controlled Graphic Equalizer	3/86	—	883
AN-446	A 150W IC Op Amp Simplifies Design of Power Circuits	4/86	—	891
AN-447	Protection Schemes for BIFET Amplifiers and Switches	4/86	8/90	905
AN-460	LM34/LM35 Precision Monolithic Temperature Sensors	6/86	11/90	908
AN-656	Understanding the Operation of CRT Monitor	11/89	—	917
AN-693	LM628 Programming Guide	4/90	4/91	923
AN-694	A DMOS 3A, 55V H-Bridge: The LMD18200	6/90	—	943
AN-706	LM628/LM629 User Guide	8/90	—	952
AN-711	LM78S40 Switching Voltage Regulator Applications	11/90	—	974
AN-715	LM385 Feedback Provides Regulator Isolation	11/90	—	989
AN-769	Dynamic Specifications for Sampling A/D Converters	5/91	—	990
AN-775	Specifications and Architectures of Sample-and-Hold Amplifiers	7/92	9/93	996
AN-776	20W Simple Switcher Forward Converter	6/91	—	1002
AN-777	LM2577 Three Output, Isolated Flyback Regulator	6/91	—	1006
AN-779	A Basic Introduction to Filters—Active, Passive, and Switched-Capacitor	4/91	—	1008
AN-813	Topics on Using the LM6181—A New Current Feedback Amplifier	3/92	—	1030
AN-828	Increasing the High Speed Torque of Bipolar Stepper Motors	5/93	—	1040
AN-840	Development of an Extensive SPICE Macromodel for "Current Feedback" Amplifiers	11/93	—	1049
AN-856	A SPICE Compatible Macromodel for CMOS Operational Amplifiers	11/93	—	1063
AN-861	Guide to CRT Design	1/93	—	1067
AN-867	Designing the Video Section of 1600 x 1280-Pixel CRTs	12/93	—	1082
AN-898	Audio Amplifiers Utilizing: SPIKE™ Protection	10/93	—	1093
AN-906	Interfacing the LM12454/8 Data Acquisition System Chips to Microprocessors and Microcontrollers	10/93	—	1102
AB-7	Multivibrator Timer CAD	3/86	8/90	1132
AB-10	Fluid Level Control System	11/83	—	1134
AB-11	High-Efficiency Regulator Has Low Drop-Out Voltage	9/83	6/86	1136
AB-12	Wide Adjustable Range PNP Voltage Regulator	2/84	—	1137
AB-24	Bench Testing LM3900 and LM359 Input Parameters	12/85	8/90	1138
AB-25	Dithering Display Expands Bar Graph's Resolution	8/81	—	1140
AB-30	RS-232 Line Driver Power Supply	6/86	8/90	1142
LB-1	Instrumentation Amplifier	3/69	—	1144
LB-2	Feedforward Compensation Speeds Op Amps	3/69	—	1146
LB-4	Fast Compensation Extends Power Bandwidth	4/69	—	1148
LB-5	High Q Notch Filter	3/69	—	1149
LB-6	Fast Voltage Comparators with Low Input Current	5/69	—	1150
LB-8	Precision AC/DC Converters	8/69	—	1153
LB-9	Universal Balancing Techniques	8/69	—	1155
LB-11	The LM110—An Improved IC Voltage Follower	3/70	—	1157
LB-12	An IC Voltage Comparator for High Impedance Circuitry	1/70	—	1160
LB-14	Speed Up the LM108 with Feedforward Compensation	11/70	—	1162
LB-15	High Stability Regulators	1/71	—	1164
LB-16	Easily Tuned Sine Wave Oscillators	3/71	—	1166
LB-17	LM118 Op Amp Slews 70V/μs	9/71	—	1168
LB-18	+5V to −15V Converter	7/72	—	1170
LB-19	Predicting Op Amp Slew Rate Limited Response	8/72	—	1172
LB-20	A Fully Differential Input Voltage Amplifier	12/72	—	1174
LB-21	Instrumentational Amplifier	6/73	8/90	1176
LB-22	Low Drift Amplifier	3/86	—	1178
LB-23	Precise Tri-Wave Generation	6/73	—	1179
LB-24	Versatile IC Pre-Amp Makes Thermocouple Amplifier with Cold Junction Compensation	6/73	—	1180
LB-25	True rms Detector	6/73	—	1182
LB-26	Specifying Selected Op Amps and Comparators	10/73	—	1184
LB-27	Micropower Thermometer	1/74	—	1186

Linear Applications Numerical List (Continued)

Application Notes		Date	Revision Date	Page
LB-28	General Purpose Power Supply	6/74	—	1188
LB-32	Microvolt Comparator	6/76	—	1190
LB-34	A Micropower Voltage Reference	6/76	—	1192
LB-35	Adjustable 3-Terminal Regulator for Low-Cost Battery Charging Systems	8/76	—	1193
LB-38	Wide Range Timer	2/77	—	1195
LB-39	Circuit Techniques for Avoiding Oscillations in Comparator Applications	1/78	—	1196
LB-41	Precision Reference Uses Only Ten Microamperes	6/78	—	1198
LB-42	Get Fast Stable Response from Improved Unity-Gain Followers	8/78	—	1200
LB-44	Get More Power Out of Dual or Quad Op Amps	4/79	—	1202
LB-45	Frequency-to-Voltage Converter Uses Sample-and-Hold to Improve Response and Ripple	4/79	—	1204
LB-46	A New Production Technique for Trimming Voltage Regulators	7/79	6/86	1206
LB-47	High Voltage Adjustable Power Supplies	3/80	—	1208
LB-48	Simple Voltmeter Monitors TTL Supplies	2/80	—	1210
LB-49	Programmable Power Regulators Help Check Out Computer System Operating Margins	1/85	—	1212
LB-51	Add Kelvin Sensing and Parallel Capability to 3-Terminal Regulators	3/81	—	1214
LB-52	A Low Noise Precision Op Amp	12/80	—	1216
LB-53	μP Interface for a Free Running A/D Allows Asynchronous Reads	7/81	6/86	1218
Appendix A	The Monolithic Operational Amplifier: A Tutorial Study	12/84	6/86	1220
Appendix C	V/F Converter IC's Handle Frequency-to-Voltage Needs	8/80	6/86	1241
Appendix D	Versatile Monolithic V/F's Can Compute as well as Convert with High Accuracy	8/80	6/86	1247
Appendix H	Standard Resistance Values	6/86	—	1254

National Semiconductor

Device/Application Literature Cross-Reference

Device Number	Application Literature
ADCXXXX	AN-156
ADC80	AN-360
ADC0801	AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53
ADC0802	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0803	AN-233, AN-274, AN-280, AN-281, LB-53
ADC08031	AN-460
ADC0804	AN-233, AN-274, AN-276, AN-280, AN-281, AN-301, AN-460, LB-53
ADC0805	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0808	AN-247, AN-280, AN-281
ADC0809	AN-247, AN-280
ADC0816	AN-193, AN-247, AN-258, AN-280
ADC0817	AN-247, AN-258, AN-280
ADC0820	AN-237
ADC0831	AN-280, AN-281
ADC0832	AN-280, AN-281
ADC0833	AN-280, AN-281
ADC0834	AN-280, AN-281
ADC0838	AN-280, AN-281
ADC1001	AN-276, AN-280, AN-281
ADC1005	AN-280
ADC10461	AN-769
ADC10462	AN-769
ADC10464	AN-769
ADC10662	AN-769
ADC10664	AN-769
ADC1210	AN-245
ADC12441	AN-769
ADC12451	AN-769
ADC3501	AN-200, AN-202
ADC3511	AN-200
ADC3701	AN-200
ADC3711	AN-200
CD4016	AB-10
DACXXXX	AN-156
DAC0800	AN-693
DAC0830	AN-284
DAC0831	AN-271, AN-284
DAC0832	AN-271, AN-284
DAC1000	AN-271, AN-275, AN-277, AN-284
DAC1001	AN-271, AN-275, AN-277, AN-284
DAC1002	AN-271, AN-275, AN-277, AN-284
DAC1006	AN-271, AN-275, AN-277, AN-284
DAC1007	AN-271, AN-275, AN-277, AN-284

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
DAC1008	AN-271, AN-275, AN-277, AN-284
DAC1020	AN-263, AN-269, AN-2293, AN-294, AN-299
DAC1021	AN-269
DAC1022	AN-269
DAC1208	AN-271, AN-284
DAC1209	AN-271, AN-284
DAC1210	AN-271, AN-284
DAC1218	AN-293
DAC1219	AN-693
DAC1220	AN-253, AN-269
DAC1221	AN-269
DAC1222	AN-269
DAC1230	AN-284
DAC1231	AN-271, AN-284
DAC1232	AN-271, AN-284
DAC1280	AN-261, AN-263
DH0034	AN-253
DH0035	AN-49
INS8070	AN-260
LF111	LB-39
LF155	AN-263, AN-447
LF198	AN-245, AN-294
LF311	AN-301
LF347	AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447, LB-44
LF351	AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C
LF351A	AN-240
LF351B	Appendix D
LF353	AN-256, AN-258, AN-262, AN-263, AN-266, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D
LF356	AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447, AN-693
LF357	AN-263, AN-447, LB-42
LF398	AN-247, AN-258, AN-266, AN-294, AN-298, LB-45
LF411	AN-294, AN-301, AN-344, AN-447
LF412	AN-272, AN-299, AN-301, AN-344, AN-447
LF441	AN-301, AN-447
LF13006	AN-344
LF13007	AN-344
LF13331	AN-294, AN-447
LH0002	AN-13, AN-227, AN-263, AN-272, AN-301
LH0024	AN-253
LH0032	AN-242, AN-253
LH0033	AN-48, AN-227, AN-253
LH0063	AN-227
LH0070	AN-301
LH0071	AN-245
LH0094	AN-301
LH0101	AN-261
LH1605	AN-343
LH2424	AN-867
LM10	AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300, AN-460, AN-693
LM11	AN-241, AN-242, AN-260, AN-266, AN-271

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM12	AN-446, AN-693, AN-706
LM101	AN-4, AN-13, AN-20, AN-24, LB-42, Appendix A
LM101A	AN-29, AN-30, AN-31, AN-79, AN-241 AN-711, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28
LM102	AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11
LM103	AN-110, LB-41
LM105	AN-23, AN-110, LB-3
LM106	AN-41, LB-6, LB-12
LM107	AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A
LM108	AN-29, AN-30, AN-31, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21
LM108A	AN-260, LB-15, LB-19
LM109	AN-42, LB-15
LM109A	LB-15
LM110	LB-11, LB-42
LM111	AN-41, AN-103, LB-12, LB-16, LB-32, LB-39
LM112	LB-19
LM113	AN-56, AN-110, LB-21, LB-24, LB-28, LB-37
LM117	AN-178, AN-181, AN-182, LB-46, LB-47
LM117HV	LB-46, LB-47
LM118	LB-17, LB-19, LB-21, LB-23, Appendix A
LM119	LB-23
LM120	AN-182
LM121	AN-79, AN-104, AN-184, AN-260, LB-22
LM121A	LB-32
LM122	AN-97, LB-38
LM125	AN-82
LM126	AN-82
LM129	AN-173, AN-178, AN-262, AN-266
LM131	AN-210, AN-460, Appendix D
LM131A	AN-210
LM134	LB-41, AN-460
LM135	AN-225, AN-262, AN-292, AN-298, AN-460
LM137	LB-46
LM137HV	LB-46
LM138	LB-46
LM139	AN-74
LM143	AN-127, AN-271
LM148	AN-260
LM150	LB-46
LM158	AN-116
LM160	AN-87
LM161	AN-87, AN-266
LM163	AN-295
LM194	AN-222, LB-21
LM195	AN-110
LM199	AN-161, AN-260
LM199A	AN-161
LM211	LB-39
LM231	AN-210
LM231A	AN-210
LM235	AN-225
LM239	AN-74

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM258	AN-116
LM260	AN-87
LM261	AN-87
LM34	AN-460
LM35	AN-460
LM301A	AN-178, AN-181, AN-222
LM308	AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D
LM308A	AN-225, LB-24
LM309	AN-178, AN-182
LM311	AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39
LM313	AN-263
LM316	AN-258
LM317	AN-178, LB-35, LB-46
LM317H	LB-47
LM318	AN-299, LB-21
LM319	AN-828, AN-271, AN-293
LM320	AN-288
LM321	LB-24
LM324	AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C
LM329	AN-256, AN-263, AN-284, AN-295, AN-301
LM329B	AN-225
LM330	AN-301
LM331	AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix C, Appendix D
LM331A	AN-210, Appendix C
LM334	AN-242, AN-256, AN-284
LM335	AN-225, AN-263, AN-295
LM336	AN-202, AN-247, AN-258
LM337	LB-46
LM338	LB-49, LB-51
LM339	AN-74, AN-245, AN-274
LM340	AN-103, AN-182
LM340L	AN-256
LM342	AN-288
LM346	AN-202, LB-54
LM348	AN-202, LB-42
LM349	LB-42
LM358	AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C
LM358A	Appendix D
LM359	AN-278, AB-24
LM360	AN-87
LM361	AN-87, AN-294
LM363	AN-271
LM380	AN-69, AN-146
LM382	AN-147
LM385	AN-242, AN-256, AN-301, AN-344, AN-460, AN-693, AN-777
LM386	LB-54
LM391	AN-272
LM392	AN-274, AN-286
LM393	AN-271, AN-274, AN-293, AN-694
LM394	AN-262, AN-263, AN-271, AN-293, AN-299, AN-311, LB-52
LM395	AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, AN-460, LB-28

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM399	AN-184
LM555	AN-694, AB-7
LM556	AB-7
LM565	AN-46, AN-146
LM566	AN-146
LM604	AN-460
LM628	AN-693, AN-706
LM629	AN-693, AN-694, AN-706
LM709	AN-24, AN-30
LM710	AN-41, LB-12
LM725	LB-22
LM741	AN-79, LB-19, LB-22
LM832	AN-386, AN-390
LM833	AN-346
LM1036	AN-390
LM1202	AN-867
LM1203	AN-861
LM1458	AN-116
LM1524	AN-272, AN-288, AN-292, AN-293
LM1558	AN-116
LM1578A	AB-30
LM1823	AN-391
LM1830	AB-10
LM1865	AN-390
LM1886	AN-402
LM1889	AN-402
LM1894	AN-384, AN-386, AN-390
LM2419	AN-861
LM2577	AN-776, AN-777
LM2889	AN-391, AN-402
LM2907	AN-162
LM2917	AN-162
LM2931	AB-12
LM2931CT	AB-11
LM3045	AN-286
LM3046	AN-146, AN-299
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3525A	AN-694
LM3578A	AB-30
LM3876	AN-898
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3911	LB-27, AN-460
LM3914	AN-460, LB-48, AB-25
LM3915	AN-386
LM3999	AN-161
LM4250	AN-88, LB-34
LM6181	AN-813, AN-840
LM7800	AN-178
LM12454/8	AN-906
LM18293	AN-706

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM78L12	AN-146
LM78S40	AN-711
LMC555	AN-460, AN-828
LMC660	AN-856
LMC835	AN-435
LMC6044	AN-856
LMC6062	AN-856
LMC6082	AN-856
LMC6484	AN-856
LMD18200	AN-694, AN-828
LMF40	AN-779
LMF60	AN-779
LMF90	AN-779
LMF100	AN-779
LMF120	AN-779
LMF380	AN-779
LMF390	AN-779
LP324	AN-284
LP395	AN-460
LPC660	AN-856
MF4	AN-779
MF5	AN-779
MF6	AN-779
MF8	AN-779
MF10	AN-307, AN-779
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74HC86	AN-861, AN-867
MM74LS138	LB-54
MM53200	AN-290
2N4339	AN-32

National Semiconductor

Subject Index

A/D (See Analog-to-Digital)
ABSOLUTE VALUE AMPLIFIER: AN-31
AC AMPLIFIER: AN-31, AN-48, AN-72
AC TO DC CONVERTER: AN-31, LB-8
ACTIVE FILTER (See Filter)
AGC
DC: AN-72
Methods: AN-72
Television Signal: AN-391
ALARM
Inexpensive IC: AN-154
AM-FM:
Demodulators and Detectors: AN-46
AMMETER
AN-71, AN-242
AMPLIFIERS:
150 Watt Op Amp, LM12: AN-446
AC: AN-31, AN-48, AN-72
Absolute Value: AN-31
AGC: AN-391
Anti-Log Generator: AN-30, AN-31
Audio: AN-32, AN-69, AN-72, AN-898
Battery Powered: AN-71, AN-211
Bias Current: AN-242
Bridge: AN-29, AN-31
Bridged: AN-69
Buffered: AN-253
Buffered High Current Output: AN-4, AN-13, AN-29, AN-31, AN-48, AN-253, AN-261, AN-272
Cascode, FET: AN-32
Cascode, RF: AN-32
Circuit Description LH0002: AN-4, AN-13, AN-227
Circuit Description LH0024: AN-253
Circuit Description LH0032: AN-253
Circuit Description LH0033: AN-48, AN-227
Circuit Description LH0063: AN-227
Circuit Description LM108/LM208/LM308: AN-29
Circuit Description LM118/LM218/LM318: LB-17
Circuit Description LM3900: AN-72
Circuit Description LM4250 Micropower Programmable Amp: AN-71
Clamping: AN-31, LB-8
CMOS as Linear Amp: AN-88
Compensation: AN-242, AN-253, AN-813, AN-861
CRT (Cathode Ray Tube): AN-861
Current Amplifier: AN-4, AN-13, AN-227
Current Feedback Amplifier: AN-813, AN-840
Difference: AN-20, AN-29, AN-31, AN-72
Differential Input: LB-20
Differentiator: AN-20, AN-31, AN-72
Digitally Controlled: AN-269
Drift Testing: AN-79
Dual Op Amp with Single Supply: AN-116
FET Input: AN-4, AN-29, AN-32, AN-227, AN-253, AN-447
Fiber Optic Link: AN-253
Follower (See Voltage Follower)
Frequency Compensation: AN-79
High Current Buffer: AN-4, AN-13, AN-29, AN-31, AN-48, AN-227
High Input Impedance: AN-29, AN-31, AN-32, AN-48, AN-72, AN-227, AN-241, AN-253, LB-1
High Resolution (Video): AN-867, AN-813, AN-861
High Speed: AN-227, AN-253, LB-42, AN-813, AN-840, AN-861, AN-867
High Speed Peak Detector: AN-227
High Speed Sample and Hold: AN-253
High Voltage: AN-72, AN-127
Improved DC Characteristics: AN-79
Input Guarding: AN-29, AN-447
Instrumentation: AN-29, AN-31, AN-71, AN-79, AN-127, AN-222, AN-242, LB-1, LB-21
Instrumentation Shield/Line Driver: AN-48
Integrator: AN-20, AN-29, AN-31, AN-72, AN-88
Integrator, JFET AC Coupled: AN-32
Inverting: AN-20, AN-31, AN-71, AN-72, LB-17
Level Shifting: AN-4, AN-13, AN-32, AN-41, AN-48
Line Receiver: AN-72
Logarithmic Converter: AN-29, AN-30, AN-31
Low Drift: AN-79, AN-222, LB-22, LB-24
Low Frequency: AN-74
Low Noise: AN-222, AN-346
Low Offset: AN-242
Meter: AN-71
Micropower: AN-71
Microphone: AN-346
Nano-Watt: AN-71
Noise: AN-241

Subject Index (Continued)

Noise Specifications: AN-104, LB-26
Non-Inverting Amplifier: AN-20, AN-31, AN-72
Non-Linear: AN-4, AN-31
Norton: AN-72, AN-278
Operational: AN-4, AN-20, AN-29, AN-31, AN-63, AN-211, AN-241, AN-446, Appendix A
Output Resistance: AN-29
Paralleling: LB-44
Photocell: AN-20
Photodiode: AN-20, AN-29, AN-31, LB-12
Photoresistor Bridge: AN-29
Piezoelectric Transducer: AN-29, AN-31
Power: AN-69, AN-72, AN-110, AN-125, AN-127, AN-446, AN-898, LB-44 (See also Buffer, High Current)
Preamp: AN-79, AN-346, LB-24
Pulse: AN-13
Rejection, Power Supply: AN-29
Reset Stabilized: AN-20
RF (See RF Amplifier)
RGB: AN-861
Sample and Hold: AN-4, AN-29, AN-31, AN-32, AN-48, AN-72, AN-245, LB-11
Single Supply: AN-72, AN-211
Solar Cell: AN-4
Specifying Selected Parameters: LB-26
Squaring: AN-72
Strain Gauge: AN-222
Summing: AN-20, AN-31
Temperature Probe: AN-31, AN-56
Transmission Line Driver: AN-4, AN-13
Tutorial Study of Op Amps: Appendix A
Variable Gain: AN-31, AN-32, AN-299, AN-346, LB-1 (See also AGC)
Very High Current Booster with High Compliance: AN-127
Video: AN-813, AN-861
Wide Band Buffer: AN-227
1A Class AB Current Booster: AN-127
100 mA Current Booster: AN-127
90 Watt Audio: AN-127

ANALOG COMMUTATOR (See Analog Switch)
ANALOG DIVIDER: AN-4, AN-30, AN-31
ANALOG MULTIPLIER: AN-4, AN-20, AN-30, AN-31
ANALOG SWITCH: AN-32
ANALOG-TO-DIGITAL: AN-156, AN-245, AN-360
Absolute Conversion: AN-247
Accuracy: AN-156, AN-276
Analog Input Consideration: AN-247
Auto Gain Ranging Converter: AN-245
Binary Codes: AN-156
Converters: AN-87, AN-156, AN-162, AN-193, AN-233, AN-245, AN-247, AN-258, AN-260, AN-274, AN-276, AN-281, LB-6, Appendix C, Appendix D
Current Source: AN-202
Dielectric Absorption: AN-260
Differential Analog Input: AN-233
Dual Slope Converter: AN-260
Errors: AN-156
FET Switched Multiplexer: AN-260
Free-Running Interface: LB-53
Grounding Considerations: AN-274
Integrating Converters: AN-260
Integrating 10-Bit: AN-262
Integrator Comparator: AN-260
Linearity Error Specifications: AN-156
Logarithmic: AN-274
Microprocessor Compatible: AN-284
Microprocessor Controlled Offset Adjust: AN-274
Microprocessor Interfacing: AN-274
Offset Adjust: AN-274
Ramp Generator: AN-260
Ratiometric Conversion: AN-247
References: AN-184
Resolution: AN-156, AN-276
Sampled Data Comparator: AN-276
Sampled Data Comparator Input: AN-274
Single Slope Converter: AN-260
Single Supply: AN-245, AN-284
Span Adjustment: AN-233, AN-274
Specifications: AN-156, AN-769
Successive Approximation Register: AN-193
Testing: AN-179, AN-233
Voltage Comparator: AN-276
Voltage Mode: AN-284
Z-80 Interface: AN-247
10-Bit Data Formats: AN-277
12-Bit Serial Output: AN-245
15-Bit Single Slope Integrating Converter: AN-295
6800 μP Interface: AN-247
8080 μP Interface: AN-247

ANALOG-TO-DIGITAL CONVERTER
As a Divider: AN-233
As a Voltage Comparator: AN-233
High Speed: AN-237

AND GATE: AN-72, AN-74
ANTI-LOG GENERATOR: AN-30, AN-31
ARC PROTECTION (CRT): AN-861
ATTENUATION
Digital: AN-284 (See also AGC)
AUDIO AMPLIFIERS: AN-32, AN-69, AN-72, AN-346, AN-898
Bridge Amplifier: AN-69
Intercom: AN-69
Phono: AN-346
Power Amplifier: AN-69

Subject Index (Continued)

RIAA: AN-346
Tone Control: AN-69
Voltage-Controlled: AN-299
1A Class AB Current Booster: AN-127
100 mA Current Booster: AN-127
(See also FM Stereo, Amplifiers)

AUDIO PREAMPLIFIER
Flat: AN-346
Phono: AN-346

AUDIO MIXER: AN-72

AUTO ERROR CORRECTION: AN-360

AUTO GAIN RANGING: AN-360

AUTOMATIC GAIN CONTROL (See AGC)

AUTOMOTIVE
Anti-Skid Circuit: AN-162
Tachometer: AN-162

BANDPASS FILTER: AN-72, AN-307, AN-346, AN-779, LB-11

BANDWIDTH, EXTENDED: AN-29, LB-2, LB-4, LB-14, LB-19, AN-813

BANDWIDTH, FULL POWER: LB-19, AN-769

BATTERY
Charger: LB-35

BATTERY POWERED AMPLIFIERS: AN-71

BESSEL FILTER: AN-779

BI-QUAD FILTER: AN-72

BIAS CURRENT (See Drift Compensation)
Compensation: AN-3
Drift Compensation: AN-3

BIAS CURRENT TEST SET: AN-24

BLINKER
Lamp: AN-110
Low Voltage IC: AN-154
Two Wire: AN-154

BOARD LAYOUT: AN-29, AN-813, AN-861

BOLOMETER (COMPARATOR): LB-32

BOOTSTRAPPED SHUNT FREQUENCY COMPENSATION: AN-29

BREAKER POINT DWELL METER: AN-162

BRIDGE AMPLIFIER: AN-29, AN-31

BUFFERS: AN-49, AN-227
High Current: AN-4, AN-13, AN-29, AN-31, AN-48, AN-272, LB-44
Using CMOS Amplifiers: AN-88
(See also Voltage Followers)

BUTTERWORTH FILTER: AN-779

BYPASSING, SUPPLY TERMINAL: AN-4, AN-227, AN-253, LB-2, LB-15

CABLE DRIVER: AN-813

CAD SYSTEM: AB-7

CALIBRATOR
Oscilloscope Square Wave: AN-154

CAPACITANCE MULTIPLIER: AN-29, AN-31
Digitally Controlled: AN-271
Programmable: AN-344

CAPACITIVE TRANSDUCER: AN-162

CAPACITORS
Bypass: AN-4, AN-428, LB-2, LB-15
Compensation: AN-29
(See also Frequency Compensation)
Dielectric Polarization: AN-29
Electrolytic as Timing Capacitor: AN-97
Filter, Power Supply: AN-23
Multiplier, Capacitance: AN-29, AN-31
Tantalum Bypass: LB-15

CARRIER CURRENT TRANSCEIVER: AN-146

CASCODE AMPLIFIER: AN-32

CHARGER: LB-35

CHEBYSHEV FILTER: AN-779

CHOPPER AMPLIFIERS, ALTERNATIVES: AN-79

CHOPPER DRIVES: AN-828

CHOPPER STABILIZED AMPLIFIER: AN-49

CIRCUIT DESCRIPTIONS: AN-49
LH0002 Current Amplifier: AN-13
LH0033 Buffer Amplifier: AN-48
LM34/LM35 Temperature Sensor: AN-460
LM105/LM205/LM305 Positive Voltage Regulator: AN-23
LM108/LM208/LM308 Operational Amplifier: AN-29
LM109/LM209/LM309 Three Terminal Regulator: AN-42
LM110/LM210/LM310 Voltage Follower: LB-11
LM111/LM211/LM311 Voltage Comparator: AN-41, LB-12
LM113 1.2 Volt Reference Diode: AN-56
LM118/LM218/LM318 High Slew Rate Op Amp: LB-17
LM565 Phase Locked Loop: AN-46
LM1894 DNR™: AN-386
LM3900 Quad Amplifier: AN-72
LM4250 Micropower Programmable Op Amp: AN-71

CLAMP
Back Porch: AN-861
Grid (CRT): AN-867
Precision: AN-31, LB-8

CLASS A AUDIO AMPLIFIER: AN-72

CMOS LINEAR AMPLIFIERS (See Amplifiers, CMOS)

CMOS LOGIC VOLTAGE REGULATOR: AN-71

COAXIAL CABLE DRIVE: AN-227

COLD JUNCTION COMPENSATION: AN-222, AN-225

COMMUTATION: AN-49

COMPARATORS (See Voltage Comparators)

COMPENSATION, DRIFT (See Drift Compensation)

COMPENSATION, FREQUENCY (See Frequency Compensation)

COMPENSATION, TEMPERATURE (See Drift Compensation)

Subject Index (Continued)

COMPONENT NOISE (See Noise, Component)
CONTINUITY CHECKER, AUDIBLE: AN-154
CONTROL SYSTEM, ENVIRONMENTAL: AN-193
CONVERTER
- 100 MHz: AN-32
- AC to DC: AN-31, LB-8
- Analog-to-Digital: (See Analog-to-Digital)
- Cable: AN-391
- Current-to-Voltage: AN-20, AN-31
- DC-to-DC: LB-18 (See also Switching Regulator)
- Digitally Programmable Band Pass Filter: AN-299
- Digitally Programmable Panner Attenuator: AN-299
- Frequency to Voltage: AN-97, AN-210, LB-45, Appendix C, Appendix D
- Logarithmic: AN-29, AN-30, AN-31
- Phono Preamp: AN-299
- Voltage Controlled Amplifier: AN-299
- Voltage-to-Frequency: AN-286, AN-299, Appendix D

COUNTER, PULSE: AN-72
CRT DEFLECTION CIRCUITRY: AN-656
CRT MONITOR: AN-656
CROSSOVERS
- Active: AN-346

CRYSTAL OSCILLATOR: AN-32, AN-41, AN-74, AN-402
CUBE GENERATOR: AN-30, AN-31
CURRENT AMPLIFIER
- High Output: AN-227, AN-262

CURRENT BOOSTER: AN-127, AN-227
CURRENT LIMITING
- Adjustable: AN-21
- External: AN-21, AN-29, AN-227
- External Circuit: AN-82, AN-227
- Foldback: AN-82 (See Foldback Current Limiting)
- Output Short Circuit: AN-72, AN-227
- Sense Voltage Reduction: AN-21, AN-31, AN-32
- Switchback (See Foldback Current Limiting)
- Switching Regulator: AN-21
- Two Terminal Current Limiter: AN-110
- 1A, 65V Power Supply with Variable Current Limit: AN-127

CURRENT LOOP: AN-300
CURRENT MEASUREMENT: AN-300
CURRENT MIRROR: AN-72
CURRENT MOTOR: AN-31, AN-32, AN-300 (See also Current-to-Voltage Converter)
CURRENT NOISE (See Noise, Current)
CURRENT SINK
- Digitally Controlled: AN-271
- Fixed: AN-72
- Precision: AN-20, AN-31, AN-32

CURRENT SOURCE
- Bilateral: AN-29, AN-31
- High Compliance: AN-127
- High Current: AN-42
- Multiple: AN-72
- Precision: AN-20, AN-31, AN-32
- Programmable: AN-344
- Two Terminal: AN-110
- 200 mA: AN-103

CURRENT-TO-FREQUENCY CONVERTER: AN-240
CURRENT-TO-VOLTAGE CONVERTER: AN-20, AN-31
DATA ACQUISITION SYSTEM: AN-906
D-TO-A CONVERTER: (See Digital-to-Analog)
DC SERVO-MOTOR CONTROLLERS: AN-460
DC-TO-AC CONVERTER: LB-18
DELAY SWITCH: AN-110
- Two Terminal: AN-97 (See also Timers)

DEMODULATORS: AN-49
- AM-FM: AN-46
- Frequency Shift Keying: AN-46
- IRIG Channel: AN-46
- Weather Satellite Picture: AN-46

DETECTORS: AN-391
- Peak: AN-87, AN-386
- Pulse Width: (See Pulse Width Detectors)
- Synchronous: AN-391
- True RMS: LB-25
- Zero Cross: AN-74 (See also Demodulators)

DIELECTRIC ABSORPTION: AN-260
DIELECTRIC POLARIZATION CAPACITOR: AN-29
DIFFERENCE AMPLIFIER: AN-20, AN-29, AN-31, AN-72
DIFFERENCE INTEGRATOR: AN-72
DIFFERENTIAL SIGNAL COMMUTATOR: AN-49
DIFFERENTIATOR: AN-20, AN-31, AN-72
DIGITAL DIVIDER
- Variable Ratio: AN-286

DIGITAL GAINSET: AN-344
DIGITAL INSTRUMENTATION AMPLIFIER: AN-344
DIGITAL MULTIMETER: AN-202
DIGITAL SWITCHING CIRCUITS: AN-72
DIGITAL-TO-ANALOG CONVERTER: AN-48
- Amplifier Gain Control: AN-271, AN-284
- Composite Low Offset Fast Amplifier: AN-271
- Digitally Controlled AC Attenuator: AN-284
- Digitally Controlled Capacitance Amplifier: AN-271
- Digitally Controlled Current Sink: AN-271
- Digitally Controlled Function Generator: AN-271
- High Voltage Output: AN-271, AN-293
- Output Range Level Shifting: AN-271
- Plate Driving Deflection Amplifier: AN-293
- Processor Controlled Shaker Table Driver: AN-293
- Scanner Control: AN-293

Subject Index (Continued)

Single Supply Voltage Mode: AN-271
Temperature Limit Controller: AN-293
Used as a Digitally Programmable Potentiometer: AN-271
Vernier Adjustment: AN-271
4-Quadrant Multiplexing: AN-271
4 to 20 mA Current Loop: AN-271

DIODE
Catch: AN-22
Clamps: AN-861
Precision: AN-31, AN-173, LB-8
Protective: AN-21, AN-861
Reference: AN-56, AN-110
Zener: AN-56
Zenered Transistor Base-Emitter Junction: AN-71

DISCRETE TIME SYSTEM: AN-236

DISCRIMINATOR, MULTIPLE APERTURE WINDOW: AN-31

DIVIDER, ANALOG: AN-4, AN-30, AN-31, AN-222

DNR™
Applications: AN-390
Calibration: AN-390
Cascading: AN-390
Circuit Design: AN-386
Operating Principles: AN-384

DOUBLE ENDED LIMIT DETECTOR: AN-31

DOUBLE SIDEBAND MODULATOR: AN-38, AN-49

DOUBLER, FREQUENCY: AN-41

DRIFT
Minimizing in Amplifiers: LB-22, LB-32, AN-242

DRIFT COMPENSATION: AN-79, AN-242
Bias Current: AN-3, AN-20, AN-29, AN-31
Board Layout: AN-29
Gain, Transistor: AN-56
Guarding Inputs: AN-29
Integrator, Low Drift: AN-31
Non-Linear Amplifiers: AN-4, AN-31
Offset Voltage: AN-3, AN-20, AN-31, AN-242
Reset Stabilized Amplifier: AN-20
Sample and Hold: AN-4, AN-29
Transistor Gain: AN-56
Voltage Regulator: AN-21, AN-23, AN-42, LB-15

DRIFT, VOLTAGE AND CURRENT: AN-29 (See also Drift Compensation)

DRIVERS
Cable: AN-813
Chopper: AN-828
L/R: AN-828
MOS Clock Driver: AN-74
Zero Crossing Detector and Line Driver: AN-162 (See also Voltage Followers, Buffers, Amplifiers)

DUAL TRACKING REGULATORS (See Regulators, Dual Tracking)

DIGITAL VOLT METER (DVM): AN-200

DWELL METER: AN-162

DYNAMIC SPECIFICATIONS: AN-769

ECL (See Emitter Coupled Logic)

ELECTRONIC SHUTDOWN: AN-82, AN-103

ELLIPTIC FILTER: AN-779

EMI (Electromagnetic Interference): AN-861

EMITTER COUPLED LOGIC, DIRECT INTERFACING: AN-87

EQUALIZER, GRAPHIC: AN-435

ERRORS
Low Error Amplifiers: LB-21
Reducing Comparator Errors for 1 μV Sensitivity: LB-32

FEEDFORWARD COMPENSATION: LB-2, LB-14, LB-17

FERRITE BEAD: AN-23

FET
Amplifier: AN-32
Operational Amplifier Input: AN-4, AN-29, AN-32, AN-447
Switches: AN-32, AN-447
Volt Meter, FET VM: AN-32

FILTER: AN-307
Adjustable Q: AN-31, LB-5
Bandpass: AN-72, AN-712, AN-779, LB-11 (See also Filter, Notch)
Bessel: AN-779
Bi-Quad: AN-72
Butterworth: AN-779
Chebeyshev: AN-779
Digitally Programmable Gain: AN-269
Elliptic: AN-779
Full Wave Rectifying and Averaging: AN-20, AN-31
High Pass Active Filter: AN-31, AN-72, AN-227, AN-346, LB-11, AN-779
Infrasound: AN-346
Low Pass Active Filter: AN-20, AN-31, AN-72, AN-286, AN-346, AN-779
Low Distortion: AN-346, AN-386
Low Pass Adjustable: AN-384, AN-386
Notch: AN-31, AN-48, AN-227, AN-712, AN-779, LB-5, LB-11
Notch, Adjustable Q: AN-31, AN-779, LB-5
PID: AN-693, AN-706
Power Supply: AN-23, LB-10
Programmable: AN-344
Sallen Key: AN-779
Sensitivity Functions: AN-72
Surface Acoustic Wave: AN-391
Switched Capacitor: AN-779
Tone Control: AN-32
Ultrasound: AN-346
Vestigial Side Band: AN-402

Subject Index (Continued)

FLASHER
- Inexpensive IC: AN-154
- Lamp: AN-110
- Two Wire: AN-154

FLIP-FLOP, TRIGGER: AN-72

FLUID LEVEL CONTROL: AB-10

FLYBACK POWER SUPPLY: AN-656

FM
- Blend: AN-390
- Calibration Modulation Level: AN-402

FM STEREO
- Remote Speaker: AN-146

FOLDBACK CURRENT LIMITING
- Negative Voltage Regulator: AN-21, LB-3
- Positive Voltage Regulator: AN-23, LB-3
- Power Dissipation Curve: AN-23
- Temperature Sensitivity: AN-23
  (See also Current Limiting, Foldback)

FOLLOWERS, VOLTAGE (See Voltage Followers)

FREQUENCY COMPENSATION: AN-79
- Bandwidth, Extended: AN-29, LB-2, LB-4, LB-14, LB-19, LB-42
- Bootstrapped Shunt: AN-29
- Capacitance, Stray: AN-4, AN-31, AN-428
- Capacitive Loads: AN-4, AN-447, LB-14, LB-42
- Differentiator: AN-20
- Feedforward: LB-2, LB-14, LB-17
- Ferrite Bead: AN-23
- Hints: AN-4, AN-20, AN-23, AN-41, AN-447, LB-2, LB-4, LB-42
- Multiplier: AN-210
- Multivibrator: AN-4
- Oscillation, Involuntary: AN-4, AN-20, AN-29

FREQUENCY DOUBLER: AN-41

FREQUENCY RESPONSE: LB-19
(See also Frequency Compensation)

FREQUENCY SHIFT KEYING DEMODULATOR: AN-46

FREQUENCY-TO-CURRENT CONVERTER: AN-162

FREQUENCY-TO-VOLTAGE CONVERTER: AN-97, AN-162, AN-210

FULL POWER BANDWIDTH: LB-19, AN-769

FUNCTION GENERATOR (See Generator)

GAIN CONTROL
- Digital: AN-269
- Voltage Controlled: AN-299 (See also AGC)

GAIN TEST SET: AN-24

GATES, OR AND AND: AN-72

GENERATOR
- Digitally Controlled: AN-435
- Multiple Function: AN-115, LB-23
- One Shot: AN-88
- Programmable: AN-344
- Pulse Generator: AN-74
- Sine Wave: AN-115
- Square Wave: AN-74, AN-88, AN-154, LB-23
- Staircase: AN-88, AN-162
- Time Delay: AN-14
- Triangle Wave: LB-23 (See also Oscillator)

GRAPHIC EQUALIZER
- Digitally Controlled: AN-435

GUARD DRIVER: AN-48, AN-227

GUARDING AMPLIFIER INPUTS: AN-29

GYRATOR (See Inductor, Simulated)

H-BRIDGE: AN-693, AN-694

HALL EFFECT SENSOR (COMPARATOR): LB-32

HARMONIC DISTORTION: AN-769

HIGH FREQUENCY: AN-227, AN-253, AN-391

HIGH PASS ACTIVE FILTER: AN-31, AN-72, AN-307, AN-346, AN-779, LB-11

HIGH PASS FILTER: AN-227, AN-307, AN-346

HIGH SPEED DUAL COMPARATOR: AN-115

HIGH SPEED OP AMP: AN-278, AN-428, AN-813, LB-42

HIGH SPEED PEAK DETECTOR: AN-227

HIGH SPEED SHIELD/LINE DRIVER: AN-227

HIGH VOLTAGE
- Driver: AN-49
- Flasher: AN-154
- Op Amp: AN-127
- Regulator: AN-103

HUMIDITY MEASUREMENT: AN-256

INDICATOR
- Applications: AN-154

INDUCTANCE-RESISTANCE (L/R) DRIVERS: AN-828

INDUCTOR
- Core, Switching Regulator: AN-21
- Ferrite Bead: AN-23
- Simulated: AN-31, AN-435, AN-712
- Voltage-Controlled: AN-712

INSTRUMENTATION AMPLIFIER (See Amplifiers, Instrumentation)

INPUT GUARDING: AN-29, AN-48

INTEGRATOR: AN-20, AN-29, AN-31, AN-32, AN-72

INTERMODULATION DISTORTION: AN-769

INTERNAL TIMER: AN-31

INTRUSION ALARM
- Fiber Optic: AN-266

INVERTING AMPLIFIER: AN-20, AN-31, AN-71, AN-72, LB-17

ISOLATED INPUT SIGNAL CONDITIONING AMPLIFIER: AN-266

ISOLATION AMPLIFIER: AN-266, AN-285

ISOLATION, DIGITAL: AN-41

Subject Index (Continued)

ISOLATION TECHNIQUES
- Thermocouple: AN-298
- Transformer: AN-266, AN-285

JFETs: AN-32

JUNCTION TEMPERATURE, MAX ALLOWABLE: AN-336

LAMP DRIVER
- Ground Referenced: AN-72
- Voltage Comparator: AN-4, AN-72, LB-12

LARGE SIGNAL RESPONSE: LB-19

LED (See Light Emitting Diode)

LEVEL DETECTOR WITH HYSTERESIS: AN-87

LEVEL SHIFTING AMPLIFIER: AN-4, AN-13, AN-32, AN-41, AN-48

LIGHT ACTIVATED SWITCH: AN-10

LIGHT EMITTING DIODE
- 1.5V LED Flasher: AN-154

LIMIT DETECTOR: AN-31

LIMITER (See Clamp)

LINE DRIVER: AN-13, AN-48

LINE RECEIVER AMPLIFIER: AN-72

LINE RECEIVERS, COMPARATORS SUITABLE FOR: AN-87

LIQUID DETECTOR: AB-10, AN-154

LM12 150-WATT OP AMP: AN-446

LOGARITHMIC AMPLIFIER: AN-29, AN-30, AN-31, AN-211
- DAC Controlled Scale Factor: AN-269
- Digitally Programmable: AN-269

LOGARITHMIC CONVERTER: AN-311

LOW PASS ACTIVE FILTER: AN-20, AN-31, AN-72, AN-307, AN-346, AN-779

LOW DRIFT AMPLIFIERS (See Amplifiers, Low Drift)

LVDT
- Position Sensor: AN-301

MACROMODELS (See Models, Spice)

MAGNETIC
- Variable Reluctance Pickup Buffer: AN-162

MAGNETIC FIELD SENSOR: AN-301

MAGNETIC TAPE: AN-390

MAGNETIC TRANSDUCER AMPLIFIER: AN-74

METER AMPLIFIER: AN-71, AN-222, AN-265

MICROPHONE PREAMPLIFIER: AN-299, AN-346

MICROPOWER
- Amplifier: AN-71, AN-211
- Circuit Description LM4250 Programmable Op Amp: AN-71
- Voltage Comparator: AN-71

MIXER
- Audio: AN-72
- Low Frequency: AN-72

MODELS
- Spice: AN-813, AN-840, AN-856

MODEM FILTER: AN-307

MODULATION AND DEMODULATION: AN-38, AN-49, AN-402

MODULATOR
- FM Audio: AN-402
- Pulse Width: AN-31

MOISTURE DETECTOR: AB-10, AN-154

MONOSTABLE MULTIVIBRATORS (See Multivibrator)

MOS ANALOG SWITCH: AN-49

MOS DIFFERENTIAL SWITCH: AN-49

MOTION CONTROL: AN-693, AN-706

MOTION DETECTOR (See Sensor, Air; Sensor, Liquid)

MOTOR CONTROL: AN-693, AN-694

MOTOR SPEED CONTROLLER: AN-292

MOTOR, STEPPER: AN-828

MOTOR TORQUE CONTROLLER: AN-693, AN-828

MULTIPLEXER (See Analog Switch)

MULTIPLIER
- Analog: AN-4, AN-20, AN-30, AN-31, AN-222
- Capacitance: AN-29, AN-31
- Cube Generator: AN-30, AN-31
- Resistance: AN-29

MULTIVIBRATOR: AN-4, AN-24, AN-31, AN-41, AN-71, AN-72, AN-74

NEGATIVE AND POSITIVE VOLTAGE REGULATORS (See Symmetrical Voltage Regulators)

NEGATIVE REGULATOR (See Negative Voltage Regulators)

NEGATIVE VOLTAGE REFERENCE: AN-20, AN-31

NEGATIVE VOLTAGE REGULATOR
- Circuit Description LM104/LM204/LM304: AN-21
- Drift Compensation (See Drift Compensation, Voltage Regulator)
- Foldback Current Limiting: AN-21, LB-3
- High Current: AN-21
- High Voltage: AN-21
- Hints: LB-15
- Line Regulation Improvement: AN-21
- Low Dropout Voltage: AN-211
- Overvoltage Protection: AN-21
- Power Dissipation: AN-21
- Precision, Stable: LB-15
- Programmable: AN-20, AN-31
- Protective Diodes: AN-21
- Remote Sensing: AN-21
- Ripple: AN-21
- Switching: AN-21
- Three Terminal: AN-182
- Transient Response: AN-21

NIXIE DRIVER: AN-32

Subject Index (Continued)

NOISE:
- Component: AN-104
- Figure: AN-104, AN-222, AN-391
- Filtering in Microvolt Comparators: LB-32
- Generator, "Buzz Box": AN-154
- I/F: AN-104
- Measurement: AN-180
- Television Receiver: AN-391
- Thermal: AN-104
- Theory: AN-222
- Voltage: AN-104
- Weighting: AN-384

NOISE REDUCTION
- Audio: AN-384, AN-386
- Comparison of Types: AN-384
- Complementary: AN-384
- FM: AN-390
- Masking: AN-384, AN-386
- Single-Ended: AN-384, AN-386, AN-390
- Tape: AN-390
- Television Audio: AN-390
- VTR: AN-390

NON-INVERTING AMPLIFIER: AN-20, AN-31, AN-72

NON-LINEAR AMPLIFIER: AN-4, AN-31

NORTON AMPLIFIER: AN-72, AN-278

NOTCH FILTER: AN-31, AN-48, AN-307, AN-779, LB-5, LB-11

OFFSET
- Ajusting Offset and Drift to Almost Zero: AN-79, LB-32, AN-242
- Drift Compensation: AN-3
- Voltage Compensation: AN-3

OFFSET CURRENT TEST SET: AN-24

OFFSET VOLTAGE ADJUSTMENT: LB-9

OFFSET VOLTAGE COMPENSATION (See Drift Compensation)

OFFSET VOLTAGE TEST SET: AN-24

ONE SHOT: AN-72, AN-88

OPERATIONAL AMPLIFIERS: (See Amplifiers, Operational)

OPERATIONAL AMPLIFIER TESTING: AB-12

OPERATIONAL AMPLIFIER TEST SET: AN-24

OPERATIONAL AMPLIFIER VOLTAGE REFERENCE: AN-288

OPTICALLY ISOLATED SWITCHES (See Switches, Optically Isolated)

OR GATE: AN-72, AN-74
- Regulator: AN-103

OSCILLATION, INVOLUNTARY (See Frequency Compensation)

OSCILLATOR
- Crystal: AN-41, AN-74, AN-402
- Crystal JFET: AN-32
- Fiber Optic: AN-266
- Inexpensive IC: AN-154
- L/C: AN-402
- Morse Code: AN-154
- Multivibrator: AN-4, AN-24, AN-31, AN-41, AN-71, AN-72
- One Shot: AN-88
- Piezoelectric Driver: AN-72
- Programmable "Unijunction": AN-72
- Pulse: AN-97
- Pulse Output: AN-71, AN-72
- Quadrature Output: AN-31, LB-16
- RF: AN-402
- RF JFET: AN-32
- Sawtooth: AN-72
- Sine Wave: AN-20, AN-29, AN-31, AN-32, AN-72, AN-115, AN-264, AN-712, LB-16
- Square Wave: AN-88
- Staircase: AN-72
- Television: AN-402
- Triangle Wave: AN-20, AN-24, AN-31, AN-72
- Tunable Frequency: LB-16
- Vestigial Side Band: AN-402
- Video: AN-402
- Voltage-Controlled: AN-24, AN-72, AN-81, AN-146, AN-162, AN-391, Appendix C
- Wien Bridge: AN-20, AN-31, AN-32

OVERSPEED LATCHES/INDICATORS (See Frequency-to-Voltage)

PACKAGE POWER CAPABILITIES: AN-336

PARALLELING OP AMP: LB-44

PEAK DETECTOR: AN-4, AN-31, AN-72, AN-74, AN-87, AN-227, AN-386

PHASE
- Phase Shift Oscillator: AN-88
- PLL Range Extender: AN-162
- Wide Range Phase Shifter: AN-391

PHASE COMPARATOR: AN-72

PHASE LOCKED LOOP: AN-146, AN-391, AN-81
- Advantages as Voltage-to-Frequency Converter: AN-210
- Circuit Description LM565: AN-46
- Damping: AN-46
- FM Audio Modulation: AN-402
- Locking: AN-46
- Loop Filter: AN-46
- Multiamplifier: AN-72
- Noise Performance: AN-46
- Phase Comparator: AN-72
- Theory: AN-46
- VCO: AN-72

PHASE SHIFT OSCILLATOR: AN-88

PHASE SHIFTER: AN-32

PHONO PREAMPLIFIER: AN-32, AN-222, AN-346

PHOTOCELL AMPLIFIER: AN-20

Subject Index (Continued)

PHOTODIODE
Amplifier: AN-20, AN-29, AN-31, AN-244, LB-12
Level Detector: AN-41, AN-244
PHOTORESISTOR AMPLIFIER: AN-29
PID CONTROLLER: AN-693, AN-706
PIN DIODE DRIVER: AN-49
PIN DIODE SWITCHING: AN-49
POLARITY SWITCHER: AN-344
POLARIZATION, DIELECTRIC: AN-29
POSITION SENSOR: AN-162
LVDT: AN-301
POSITIVE AND NEGATIVE VOLTAGE REGULATORS (See Symmetrical Voltage Regulators)
POSITIVE REGULATOR (See Regulator, Positive)
POSITIVE VOLTAGE REFERENCE: AN-20, AN-31, AN-56
POSITIVE VOLTAGE REGULATOR
Adjustable Output: AN-42, AN-178, AN-181, AN-182, LB-35
Bootstrapped Regulator: AN-211
Circuit Description LM105/LM205/LM305: AN-23, AN-211
Circuit Description LM109/LM209/LM309: AN-42
CMOS Compatible: AN-71
Current Limit: AN-72, AN-211
Drift Compensation (See Drift Compensation, Voltage Regulator)
Failure Mechanisms: AN-23
Filtering, Power Supply: AN-23
Fixed Output: AN-42
Foldback Current Limiting: AN-23
Heat Dissipation: AN-23
High-Current: AN-23, AN-72
High Voltage: AN-72, AN-211, LB-47
Hints: AN-23, LB-15
Low Voltage: AN-56, AN-211
Micropower Quiescent Power Drain: AN-71, AN-211
NPN Pass Transistors: AN-72
Power Limitations: AN-23
Precision: AN-42, LB-15
Programmable Low Power: AN-20, AN-31
Protection: AN-23, AN-72
Ripple Induced Failures: AN-23
Switching Regulator (See Switching Regulator)
Temperature Compensation: AN-42, LB-15
Three Terminal: AN-103, AN-178, AN-182, LB-35
Trimming Output Voltage: LB-46 (See also Voltage Regulators)
POWER AMPLIFIER (See Buffer, High Current)
POWER CAPABILITIES, IC PACKAGE: AN-336
POWER DISSIPATION
Regulator: AN-82, AN-103
H-Bridge: AN-694
POWER LINE CARRIER: AN-146
POWER SUPPLY: AN-56
General Purpose: LB-28
Monitor: LB-48
Programmable: LB-49 (See also Regulators)
Split: AN-69, AN-71
PREAMPLIFIER
CRT: AN-861
Phono: AN-32, AN-222, AN-346
Servo: AN-4, AN-31
Stereo: AN-346
Video: AN-861 (See also Amplifiers, Preamp)
PRECISION REFERENCE: AN-161, AN-173
PROGRAMMABLE GAIN: AN-289
PROGRAMMABLE OP AMP: AN-71
PROGRAMMABLE "UNIJUNCTION" OSCILLATOR: AN-72
PROGRAMMABLE VOLTAGE REGULATOR: AN-20, AN-31
PULSE AMPLIFIER: AN-13, AN-813
PULSE COUNTER: AN-72
PULSE GENERATOR: AN-71, AN-72, AN-74
PULSE STRETCHER:
Proportional: AN-266
PULSE WIDTH DETECTOR: AN-97
PULSE WIDTH MODULATOR: AN-21, AN-31, AN-74, LB-18
PULSE WIDTH MULTIVIBRATOR: AN-292
PYROELECTRIC
Accelerometer: AN-301
Detector Amplifier: AN-301
Resonator Temperature Sensor: AN-301
QUAD AMPLIFIER: AN-71, AN-72
QUAD COMPARATOR: AN-74
QUADRATURE OSCILLATOR: AN-31, AN-307, LB-16
RATE GYRO: AN-301
RECEIVER
FM Remote Speaker: AN-146
Infared: AN-290
Television: AN-391
VHF: AN-290
Ultrasonic: AN-290
RECTIFIER, FAST HALF-WAVE: AN-31, LB-8
RECTIFIER, FULL-WAVE: AN-20, LB-8
REFERENCE
Low Drift Precision 6.9V: AN-161, AN-173, AN-184
Micropower: AN-222, LB-34, LB-41
Precision: AN-79, AN-161, LB-41
REFERENCE DIODE: AN-110
REFERENCE VOLTAGE: AN-211
REFERENCE VOLTAGE DETECTOR: AN-300
REFERENCE VOLTAGE REGULATOR: AN-20, AN-31
REGULATORS (See Voltage Regulators)

Subject Index (Continued)

RELAY DRIVER: AN-72
REMOTE LINKS
Infared: AN-290
VHF: AN-290
Ultrasonic: AN-290
REMOTE SENSING
High Current Negative Regulator: AN-21
High Negative Voltage: AN-21
REMOTE SPEAKER SYSTEM: AN-146
REMOTE TEMP SENSOR/ALARM: AN-74
RESET STABILIZED AMPLIFIER: AN-20
RESISTANCE
Choice of Resistors for Op Amps: AN-79
Tester for Low Values of Resistance: LB-32
RESISTANCE MULTIPLICATION: AN-29
RESISTOR VALUES, STANDARD: Appendix E
RF: AN-391
RF AMPLIFIER
Cascode: AN-32, AN-813
RF OSCILLATOR (See Oscillator, RF)
RIAA PHONO PREAMPLIFIER: AN-222, AN-299, AN-346
RIPPLE, POWER SUPPLY: AN-21, AN-23, LB-10
RISE TIME, AMPLIFIER: LB-19
RMS
True RMS Detector: LB-25
ROOT EXTRACTOR: AN-4, AN-31, AN-222
RTD CONTROLLER: AN-292
SAFE AREA PROTECTION: AN-103
SALLEN-KEY FILTER: AN-779
SAMPLE AND HOLD: AN-4, AN-29, AN-31, AN-32, AN-72, AN-266, AN-294, LB-11, LB-45
Circuit: AN-286
Extended HOLD Time: AN-245, AN-294
High Speed: AN-253, AN-294
HOLD Step: AN-294
Infinite: AN-245
Infinite HOLD Time: AN-245, AN-294
Reduction of HOLD Step: AN-245, AN-294
Terms: AN-266
SAMPLING THEOREM: AN-236
SAWTOOTH GENERATOR: AN-72
SCHMITT TRIGGER: AN-32, AN-72
SENSE VOLTAGE (See Current Limiting)
SENSITIVITY FUNCTIONS: AN-72
SENSOR
Mass Velocity: AN-162
Rotational Velocity: AN-162
SERVO PREAMPLIFIER: AN-4, AN-31
SETTLING TIME: LB-17
SHORT CIRCUIT PROTECTION (See Current Limiting)
SIGNAL-TO-NOISE RATIO: AN-104, AN-769
SINE SHAPER: AN-263
SINE WAVE GENERATOR: AN-115, AN-263, AN-269, AN-307
SINE WAVE OSCILLATOR: AN-20, AN-29, AN-31, AN-32, AN-72, AN-263, LB-16
Crystal: AN-263
Digital: AN-263
High Voltage: AN-263
Phase Shift: AN-263
Sine Wave Voltage Reference: AN-262
Tuning Fork: AN-263
Voltage-Controlled: AN-262
Wien Bridge: AN-263
SINE WAVE RESPONSE: LB-19
SINGLE SUPPLY AMPLIFIER: AN-72
SINGLE SUPPLY OPERATION: AN-31, AN-48
SIREN OSCILLATOR: AN-154
SLEW RATE: LB-17, LB-19, LB-42
(See also Frequency Compensation, Feedforward)
SLEW RATE LIMITING: LB-19
SMALL SIGNAL RESPONSE: LB-19
S/N RATIO (See Signal-to-Noise Ratio)
SOLAR CELL AMPLIFIER: AN-4
SOUND
Peak: AN-384
Pressure: AN-384
Sound Effects Oscillator: AN-154
SPEED SENSOR (See Sensor, Speed)
SPEED SWITCH (See Frequency-to-Voltage Converter)
SPICE (See Models)
SQUARE ROOT CIRCUIT: AN-4, AN-31, AN-222
SQUARE WAVE GENERATOR: AN-74, AN-88, AN-115, AN-154, AN-222, LB-23
SQUARING AMPLIFIER: AN-72, AN-222
SQUARING CIRCUITS: AN-222
STAIRCASE GENERATOR: AN-72, AN-88
(See also Generator, Staircase)
STANDARD VALUES RESISTOR: Appendix E
STEP RESPONSE: LB-19
STEPPER MOTOR: AN-828
STEREO (See FM Stereo)
STEREO PREAMPLIFIER: AN-346
STRAIN GAUGE CONVERTER: AN-301
SUBTRACTOR (See Difference Amplifier)
SUMMING AMPLIFIER: AN-20, AN-31
SUPPLY VOLTAGE SPLITTING: AN-31
SWITCHED CAPACITOR FILTER: AN-307, AN-779
SWITCHES
Optically Isolated: AN-110
Two Terminal Time Delay: AN-97
SWITCH, ANALOG: AN-32
SWITCHBACK CURRENT LIMITING
(See Foldback Current Limiting)

SWITCHING REGULATOR: AN-343, AN-97, AN-110, AB-30, AN-711

Buck Converter: AN-343, AN-711
Boost (Step-Up) Converters: AN-711
Circuit Description LH1605: AN-343
Circuit Description LM78S40: AN-711
Current Limiting: AN-2, AN-21
DC Motor Speed Regulation: AN-343
Dissipation: AN-21
Driver: AN-2, AN-21
Dual-Output: AB-30
Efficiency: AN-21
Forward Converter: AN-776
High Negative Current: AN-21
Hint: AN-21
Inductor Core Selection: AN-21, AN-711
Inverting (DC Plus to DC Minus) Converter: AN-711, LB-18
Isolated Flyback: AN-777
Line Regulation: AN-21
Negative: AN-21
Overload Shutdown: AN-21
Polarity Conversion: LB-18
Theory: AN-711, LB-18

SYMMETRICAL VOLTAGE REGULATOR
Tracking Regulator: AN-20

SYNCHRONOUS
Video Detector: AN-391

TACHOMETER: AN-72, AN-97

TAPE READER
Magnetic: AN-74

TAPE COMPENSATION
Weighing System: AN-271

TELEVISION: AN-402

TEMPERATURE: AN-292
Centigrade Sensors: AN-460
Controller: AN-293
Farenheit Sensors: AN-460
Oven Controller: AN-262
Platinum RTD High Temperature: AN-262
Timer Used as Controller: AN-97
Transducer: AN-225, AN-460
Transducer, Micropower: LB-27

TEMPERATURE COMPENSATED ZENER DIODE: AN-56

TEMPERATURE COMPENSATION (See Drift Compensation)

TEMPERATURE CONTROLLER: AN-286, AN-292, AN-293

TEMPERATURE CONTROL: AN-262, AN-293
Precision: AN-266
High Efficiency: AN-266

TEMPERATURE PROBE AMPLIFIER: AN-31, AN-56

TEMPERATURE PROBE COMPARATOR: AN-72

TEST SET, OPERATIONAL AMPLIFIER: AN-24

THERMAL CAPABILITIES, DEVICE: AN-336

THERMAL FEEDBACK REDUCTION IN MICROVOLT COMPARATORS: LB-32

THERMAL NOISE (See Noise, Thermal)

THERMAL SHUTDOWN: AN-82, AN-103

THERMOCOUPLE: AN-225
Amplifier with Cold Junction Compensation: AN-211, AN-222, AN-225, LB-24
Comparator: LB-32
Effects on IC's: AN-79, LB-22, LB-32

THERMOMETER: AN-262
Electronic: AN-225, AN-233
Micropower: LB-27, AN-211
Temperature Controller: AN-97
Thermocouple: LB-24
Using Platinum Sensor: AN-286

THERMOMETER, ELECTRONIC: AN-31, AN-56

THRESHOLD DETECTOR: AN-20, AN-31

TIME DELAY GENERATOR: AN-74

TIME, INTERVAL: AN-31

TIMER CIRCUITS: AB-7, AN-97, AN-110

TIMERS
Chain of Timer: AN-97
Cycle Interrupt: AN-97
Dual Supply Operation: AN-97
Electrolytic Timing Capacitors: AN-97
Eliminating Timing Cycle upon Initial Application of Power: AN-97
Linearizing Charging Sweep: AN-97
Negative Pulse Triggering: AN-97
Noise Immunity: AN-97
One Hour: AN-97
Time Delay Circuit: AN-110
Time Out, Power Up: AN-97
Wide Range Timer: LB-38
Zero Power Dissipation between Timing Intervals: AN-97
5V Logic Supply Driving 28V Relay: AN-97
30V Supply Interfacing with 5V Logic: AN-97

TIMING ERROR: AN-97

TONE CONTROL: AN-32, AN-435
Stereo: AN-435

TOTAL HARMONIC DISTORTION: AN-180

TRANSCONDUCTANCE AMPLIFIER: AN-386

TRANSDUCER
Amplifier: LB-24
Signal Conditioners: AN-301
Temperature: LB-27

TRANSFER FUNCTION TEST SET: AN-24

Subject Index (Continued)

TRANSISTOR
- Low Noise: AN-222
- Optically Isolated: AN-110
- Power, Protected: AN-110

TRANSMITTER
- FM Remote Speaker: AN-146
- Infared: AN-290
- Two Wire: AN-211
- VHF: AN-290
- Ultrasonic: AN-290

TRIAC TRIGGER: AN-154

TRIANGLE WAVE OSCILLATOR: AN-20, AN-24, AN-31, AN-72

TRIGGER APPLICATIONS: AN-154

TRIGGER, FLIP-FLOP: AN-72

TRIGGER, SCHMITT: AN-32, AN-72

TUNED RF CIRCUITS (See Amplifiers)

TV (See Television)

UNITY-GAIN BUFFER: AN-20

VCO (See Voltage-Controlled Oscillator)

VELOCITY SENSOR (See Sensor, Velocity)

VIDEO: AN-391, AN-656

VOLTAGE COMPARATOR: AN-41, AN-74, AN-103, AN-288, LB-39
- A-to-D Converter Circuit: LB-6
- AC Coupled: LB-6
- Avoiding Oscillations: LB-39
- Buffered Output: AN-29
- Circuit Description LM111/LM211/LM311: AN-41, LB-12
- Comparison: AN-87, LB-12
- DTL Driver: AN-4, AN-29, AN-31, LB-12
- Dual Limit, High Speed: AN-48
- Fast: LB-6
- High Current: AN-71
- High Speed Differential: AN-87
- Hints: AN-41
- Inverting and Non-Inverting with Hysteresis: AN-74
- Lamp Driver: AN-4, AN-72, LB-12
- Micropower: AN-71
- Microvolt: LB-32
- MOS Driver: AN-41, LB-12
- Op Amp Voltage Comparator: AN-4, AN-71, AN-72
- Preamplifier: LB-32
- Quad Array: AN-74
- Specifying Selected Parameters: LB-26
- Timers Used as: AN-97
- TTL Driver: AN-4, AN-29, AN-31, AN-41, LB-12
- Zero Crossing: AN-31, AN-41, LB-6, LB-12

VOLTAGE CONTROLLED AMPLIFIER: AN-299

VOLTAGE CONTROLLED OSCILLATOR: AN-72, AN-74, AN-81, AN-146, AN-162, AN-391 (See also Voltage-to-Frequency Converter)

VOLTAGE FOLLOWER: AN-63
- Bias Current: AN-20
- Circuit Description LH0033: AN-48
- Circuit Description LM110/LM210/LM310: LB-11
- Comparison: LB-11
- Frequency Compensation: LB-42
- Hints, Operating: AN-20
- Offset Adjustment: AN-31, LB-9
- Single Supply: AN-72
- Voltage Reference: AN-20, AN-31, AN-56
- 1 Amp: AN-110

VOLTAGE NOISE (See Noise, Voltage)

VOLTAGE REFERENCES (See Reference)

VOLTAGE REGULATORS: AN-178 (See also Regulators, Voltage; Positive, Negative, or Switching Voltage Regulator)
- Adjustables: AN-178, AN-181, AN-211, AB-11, AB-12, LB-46
- Automotive: AB-12
- Battery Charging: AB-11, AB-12
- Current: AN-103, AN-110, AN-127
- Dual Tracking: AN-82, AN-103
- High Current: AN-103, AN-110
- High Current Dual Tracking: AN-82
- High Current Regulators: AB-11
- High Input Voltage: AN-103, AN-211
- Improving Reliability: AN-182
- Low Dropout: AB-11, AB-12
- PNP: AB-11, AB-12
- Trimming: LB-46
- 1A, 65V with Variable Current Limit: AN-127
- ±32.5V Dual Tracking: AN-127

VOLTAGE-TO-FREQUENCY CONVERTER: AN-210, AN-240, LB-45, Appendix C, Appendix D (See also Analog-to-Digital Converters and Voltage-Controlled Oscillators)

VOLT METER: AN-32, AN-71, LB-45

WEIGHING SYSTEM
- Precision: AN-295

WIEN BRIDGE OSCILLATOR: AN-20, AN-31, AN-32, AN-263

WINDOW DISCRIMINATOR, MULTIPLE APERATURE: AN-31

ZENER DIODE
- IC: AN-56
- Transistor Base-Emitter Junction: AN-71

ZENERS (See Reference)

ZERO CROSSING DETECTOR: AN-[illegible], AN-74, LB-6, LB-12
- Comparators Suitable for "Two Shot": AN-87, AN-162

8080 MICROPROCESSOR: AN-200

Drift Compensation Techniques for Integrated DC Amplifiers

National Semiconductor
Application Note 3

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introduction

With DC amplifiers, it is usually possible to substantially improve drift performance by using additional circuitry along with some form of adjustment. In fact, one of the reasons that discrete-component operational amplifiers have better input current specifications than monolithic amplifiers is that current compensation is used. Monolithic circuits cannot incorporate these techniques because it is not possible to select components or make adjustments. These adjustments can, however, be made external to the amplifier. This article will discuss a number of compensation methods which can substantially reduce the input currents of monolithic amplifiers, especially in limited-temperature-range applications.

Bias current compensation reduces offset and drift when the amplifier is operated from high source resistances. With low source resistances, such as a thermocouple, the drift contribution due to bias current can be made quite small. In this case, the offset voltage drift becomes important.

A technique is presented here by which offset voltage drifts better than 0.5 μV/°C can be realized. The compensation technique involves only a single room-temperature balance adjustment. Therefore, chopper-stabilized performance can be realized, with low source resistances, in a fairly-simple amplifier without tedious cut-and-try compensation methods.

bias current compensation

The simplest and most effective way of compensating for bias currents is shown in *Figure 1*. Here, the offset produced by the bias current on the inverting input is cancelled by the offset voltage produced across the variable resistor, R_3. The main advantage of this scheme, besides its simplicity, is that the bias currents of the two input transistors tend to track well over temperature so that low drift is also achieved. The disadvantage of the method is that a given compensation setting works only with fixed feedback resistors, and the compensation must be readjusted if the equivalent parallel resistance of R_1 and R_2 is changed.

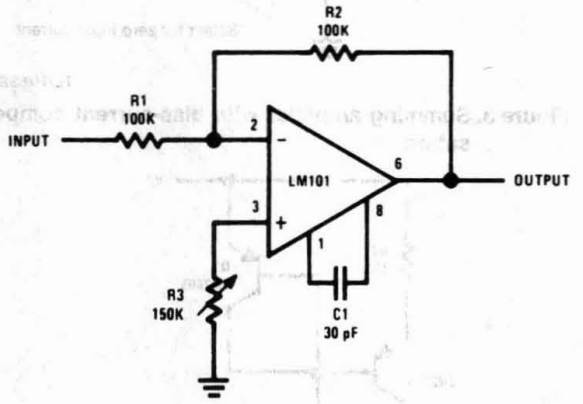

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Figure 1. Summing amplifier with bias-current compensation for fixed source resistances

Figure 2 shows a similar circuit for a non-inverting amplifier. The offset voltage produced across the DC resistance of the source due to the input current is cancelled by the drop across R_3. For proper adjustment range, R_3 should have a maximum value about three times the source resistance and the equivalent parallel resistance of R_1 and R_2 should be less than one-third the input source resistance.

This circuit has the same advantages as that in *Figure 1*, however, it can only be used when the input source has a fixed DC resistance. In many applications, such as long-interval integrators, sample-and-hold circuits, switched-gain amplifiers or voltage followers operating from unknown source, the source impedance is not defined. In these cases other compensation schemes must be used.

Figure 3 gives a compensation technique which does not depend upon having a fixed source resistance. A current is injected into the input terminal from the base of a PNP transistor. Since NPN input transistors are used on the integrated amplifier,* the base current of the PNP balances out the

*This is true for all monolithic operational amplifiers presently available.

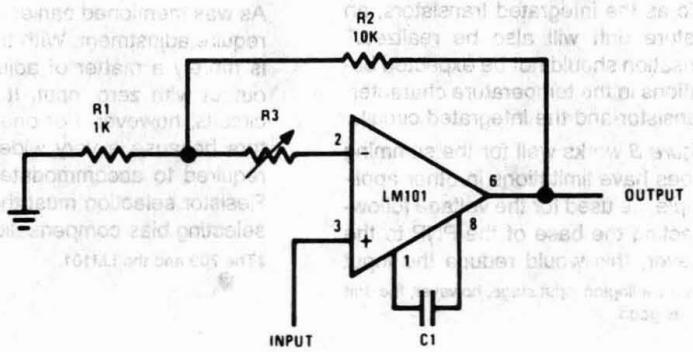

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Figure 2. Non-inverting amplifier with bias-current compensation for fixed source resistances

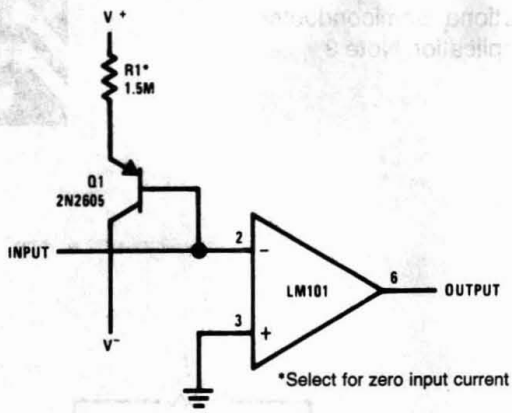

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Figure 3. Summing amplifier with bias-current compensation

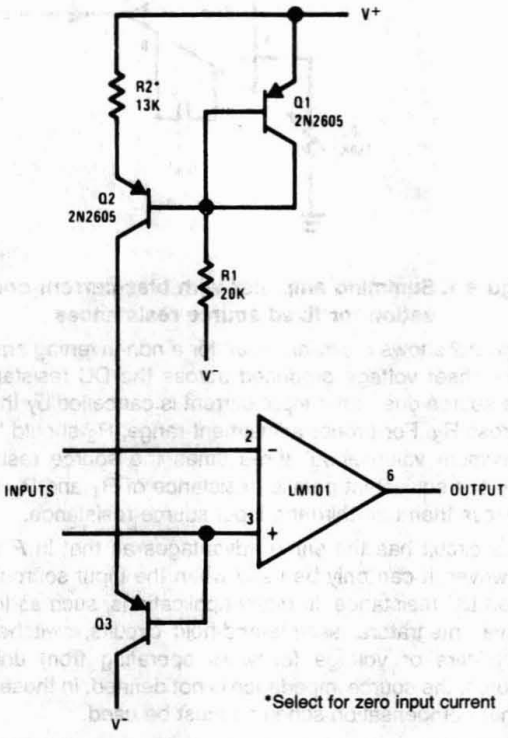

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Figure 4. Bias-current compensation for non-inverting amplifier operated over large common mode range

base current of the NPN. Further, since a silicon-planar PNP transistor has approximately the same current-gain versus temperature characteristic as the integrated transistors, an improvement in temperature drift will also be realized.† However, perfect compensation should not be expected because of unit-to-unit variations in the temperature characteristics of both the PNP transistor and the integrated circuit.

Although the circuit in *Figure 3* works well for the summing amplifier connection, it does have limitations in other applications. It could, for example, be used for the voltage follower configuration by connecting the base of the PNP to the non-inverting input. However, this would reduce the input impedance (to about 150 MΩ) because the current supplied by the PNP will vary with the input voltage level.

If this characteristic is objectionable, the more-complicated circuit shown in *Figure 4* can be used.

The emitter of the PNP transistor is fed from a current source so that the compensating current does not vary with input-voltage level. The design of the current source is such as to give it about the same characteristics as those on the input stage of the better monolithic amplifiers‡ to give closer compensation with changes in temperature and supply voltage. The circuit makes use of the emitter base voltage differential between two transistors operated at different collector currents.[1,2] Although it is recommended in the references that these transistors be well matched, it is not really necessary since the devices are operated at much different collector currents.

Figure 5 shows another compensation scheme for the voltage follower connection. This circuit is much simpler than that shown in *Figure 4*, but the temperature compensation is not quite as good. The compensating current is obtained through a resistor connected across a diode which is bootstrapped to the output. The diode acts as a regulator so that the compensating current does not change appreciably with signal level, giving input impedances about 1000 MΩ. The negative temperature coefficient of the diode voltage also provides some temperature compensation.

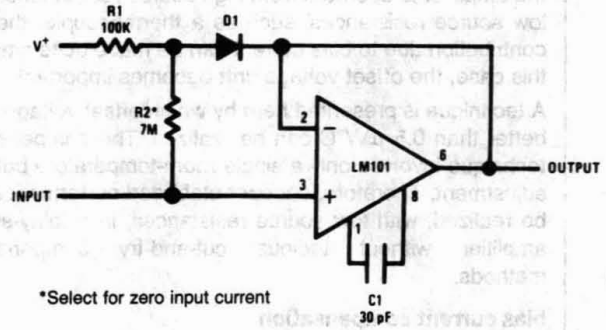

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Figure 5. Voltage follower with bias-current compensation

All the circuits discussed thus far have been tailored for particular applications. *Figure 6* shows a completely-general scheme wherein both inputs are current compensated over the full common mode range as well as against power supply and temperature variations. This circuit is suitable for use either as a summing amplifier or as a non-inverting amplifier. It is not required that the DC impedance seen by both inputs be equal, although lower drift can be expected if they are.

As was mentioned earlier, all the bias compensation circuits require adjustment. With the circuits in *Figures 1* and *2*, this is merely a matter of adjusting the potentiometer for zero output with zero input. It is not so simple with the other circuits, however. For one, it is difficult to use potentiometers because a very wide range of resistance values are required to accommodate expected unit-to-unit variations. Resistor selection must therefore be used. Test circuits for selecting bias compensation resistors are given in *Figure 7*.

‡The 709 and the LM101.

†If the operational amplifier uses a Darlington input stage, however, the drift compensation will not be nearly as good.

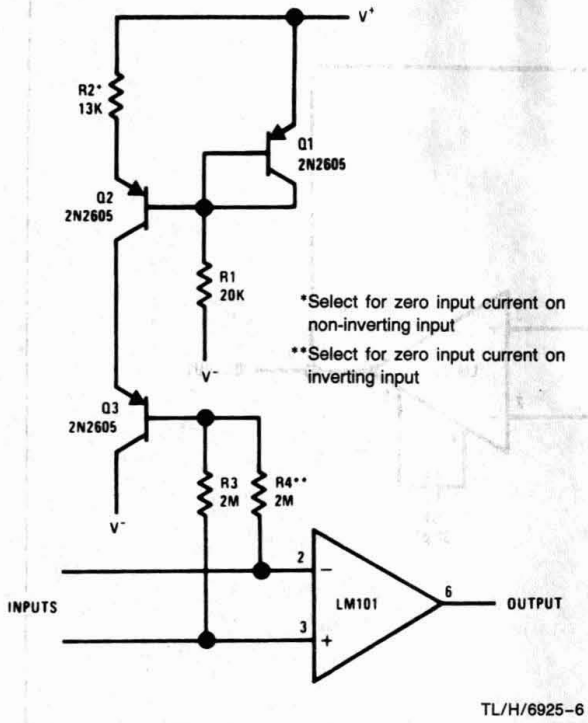

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Figure 6. Bias-current compensation for differential inputs

offset voltage compensation

The highly predictable behavior of the emitter-base voltage of transistors has suggested a unique drift compensation method; it is shown in Reference 3 that the offset voltage drift of a differential transistor pair can be reduced by about an order of magnitude by unbalancing the collector currents such that the initial offset voltage is zero. The basis for this comes from the equation for the emitter-base voltage differential of two transistors operating at the same temperature:

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{S2}}{I_{S1}} - \frac{kT}{q} \log_e \frac{I_{C2}}{I_{C1}} \qquad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, q is the charge of an electron, I_S is a constant which depends only on how the transistor is made and I_C is the collector current. This equation is derived in Reference 2.

It is worthwhile noting here that these expressions make no assumptions about the current gain of the transistors. It is shown in References 5 and 6 that the emitter-base voltage is a function of collector current, not emitter current. Therefore, the balance will not be upset by base current (except for interaction with the DC source resistance).

The first term in Equation (1) is the offset voltage of the two transistors for equal collector currents. It can be seen that this offset voltage is directly proportional to the absolute temperature–a fact which is substantiated by experiment.[4] The second term is the change of offset voltage which arises from operating the transistors at unequal collector currents. For a fixed ratio of collector currents, this is also proportional to absolute temperature. Hence, if the collector currents are unbalanced in a fixed ratio to give a zero emitter-base voltage differential, the temperature drift will also be zero.

Experiment indicates that this is indeed true. Thermal drifts less than 100 μV over the −55°C to +125°C temperature range have been realized consistently. In order to obtain these low drifts, however, it is almost necessary to use a monolithic transistor pair, since a 0.05°C temperature differential will give a 100 μV drift. With a monolithic pair, the physical proximity of the devices as well as the high thermal conductivity of silicon holds this differential to an absolute minimum.

For low drift, the transistors must operate from a low enough source resistance that the voltage drop across the source due to base current (or base current differential if both bases see the same resistance) is insignificant. Furthermore, the transistors must be operated at a low enough collector current that the emitter-contact and base-spreading resistances are negligible, since Equation (1) assumes that they are zero.

A complete amplifier using this principle is shown in *Figure 8*. A monolithic transistor pair is used as a preamplifier for a conventional operational amplifier. A null potentiometer, which is set for zero output for zero input, unbalances the collector load resistors of the transistor pair such that the collector currents are unbalanced for zero offset. This gives minimum drift. An interesting feature of the circuit is that the performance is relatively unaffected by supply voltage variations: a 1V change in either supply causes an offset voltage change of about 10 μV. This happens because neither term in Equation (1) is affected by the magnitude of the collector currents.

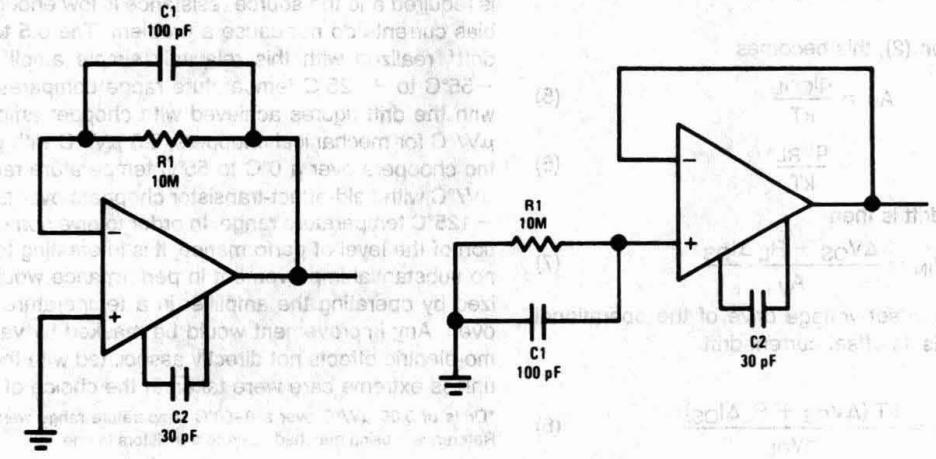

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Figure 7. Test circuits for selecting bias-compensation resistors

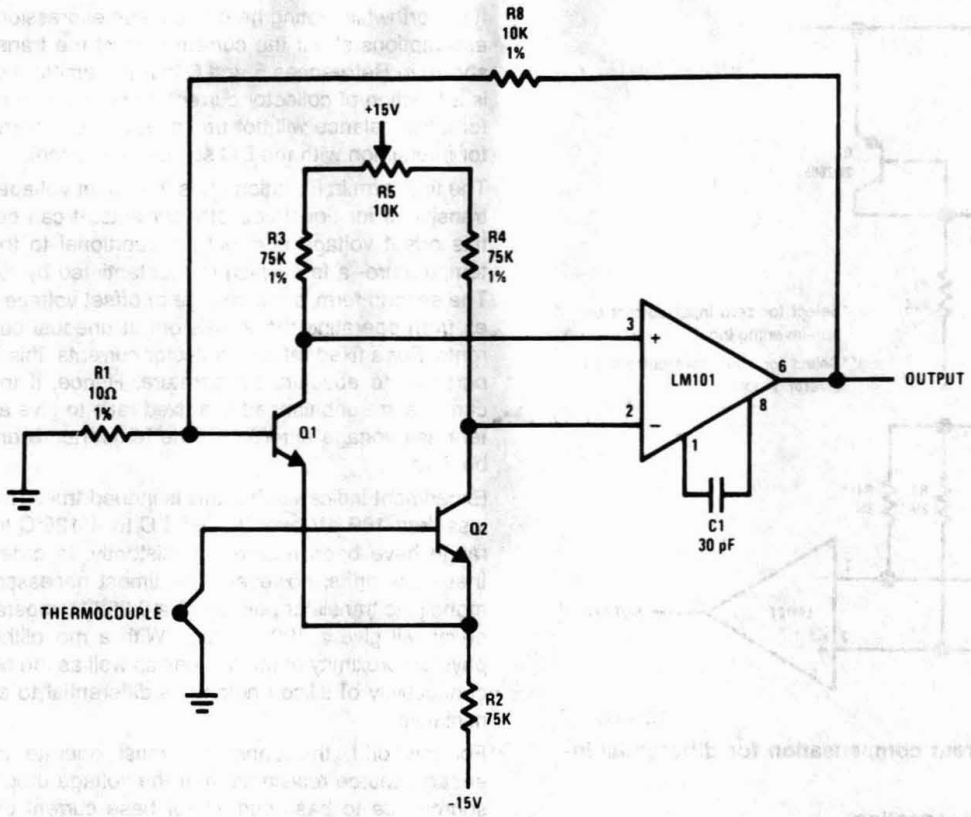

Figure 8. Example of a DC amplifier using the drift-compensation technique

In order to get low drift, it is necessary that the gain of the preamplifier be high enough so that the drift of the operational amplifier does not degrade performance. The gain can be determined from the expression for the transconductance of the input transistors:

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{kT} \quad (2)$$

The voltage gain is

$$A_V = \frac{\partial V_{OUT}}{\partial V_{IN}} \quad (3)$$

$$= \frac{\partial I_C}{\partial V_{BE}} R_L \quad (4)$$

where R_L is the average value of the two collector load resistors on the input stage and I_C is the average of the two collector currents.

Substituting Equation (2), this becomes

$$A_V = \frac{qI_C R_L}{kT} \quad (5)$$

$$= \frac{qV_{RL}}{kT} \quad (6)$$

The input referred drift is then

$$\Delta V_{IN} = \frac{\Delta V_{OS} + R_L \Delta I_{OS}}{A_V} \quad (7)$$

where ΔV_{OS} is the offset voltage drive of the operational amplifier and ΔI_{OS} is its offset current drift.

Using Equation (7),

$$\Delta V_{IN} = \frac{kT\,(\Delta V_{OS} + R_L \Delta I_{OS})}{qV_{RL}} \quad (8)$$

With the circuit shown in *Figure 8*, Equation (8) gives a 25 μV input-referred drift for every 10 mV of offset voltage drift or for every 100 nA of offset current drift. It is obvious from this that the offset current drift is most important if an operational amplifier with bipolar input transistors is used.

Another important consideration is the matching of the collector load resistors on the preamplifier stage. A 0.1-percent imbalance in the load resistors due to thermal mismatches or any other cause will produce a 25 μV shift in offset. This includes the balancing potentiometer which can introduce an error that will depend on how far it is set off midpoint if it has a different temperature coefficient than the resistors.

The most obvious use of this type of low drift amplifier is with thermocouples, magnetometers, current shunts, wire strain gauges or similar signal sources where very low drift is required and the source resistance is low enough that the bias currents do not cause a problem. The 0.5 to 1 μV/°C drift* realized with this relatively simple amplifier over a −55°C to +125°C temperature range compares favorably with the drift figures achieved with chopper amplifiers: 0.4 μV/°C for mechanical choppers, 0.5 μV/°C with photoelectric choppers over a 0°C to 55°C temperature range and 2 μV/°C with field-effect-transistor choppers over a −55°C to +125°C temperature range. In order to give some appreciation of the level of performance, it is interesting to note that no substantial improvement in performance would be realized by operating the amplifier in a temperature-controlled oven. Any improvement would be masked by various thermo-electric effects not directly associated with the amplifier unless extreme care were taken in the choice of input lead

*Drifts of 0.05 μV/°C over a 0–50°C temperature range were reported in Reference 3 using matched discrete transistors in one can.

material, the method of making connections and the balancing of thermal paths. These factors are, in fact, important when making oven tests to verify the drift of the amplifier since thermoelectric effects can easily produce drift voltages larger than those of the amplifier if they are not properly handled.

summary

A number of compensation circuits designed to increase the DC resolution of monolithic operational amplifiers have been presented. Both current compensation techniques for high impedance levels as well as methods of achieving chopper-stabilized drift performance at low impedance levels have been covered.

Fairly-simple current compensation which requires that the impedance levels be fixed have been described along with compensation which is effective in cases where the source impedance is not well defined. This latter category includes long-interval integrators, sample-and-hold circuits, switched-gain amplifiers or voltage followers which operate from an unknown source. The application of these schemes is generally limited to integrated amplifiers since modular amplifiers almost always incorporate current compensation.

The drift-reduction techniques provide stabilities better than 0.5 μV/°C for low impedance sources, such as thermocouples, current shunts or strain gauges. With a properly designed circuit, compensation depends only on a single room temperature adjustment, so excellent performance can be obtained from a fairly-simple amplifier.

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Monolithic Op Amp—The Universal Linear Component

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Application Note 4

introduction

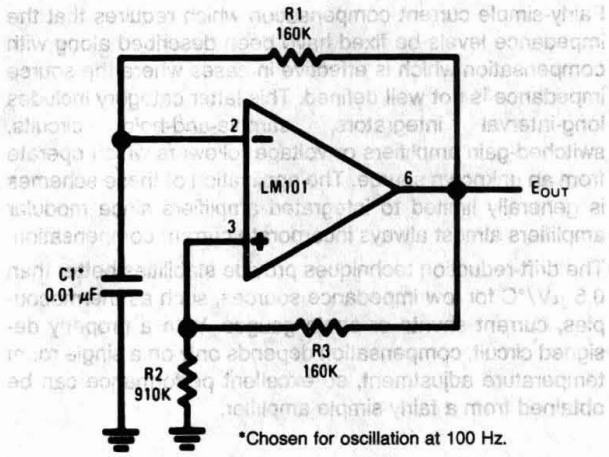
Operational amplifiers are undoubtedly the easiest and best way of performing a wide range of linear functions from simple amplification to complex analog computation. The cost of monolithic amplifiers is now less than $2.00, in large quantities, which makes it attractive to design them into circuits where they would not otherwise be considered. Yet low cost is not the only attraction of monolithic amplifiers. Since all components are simultaneously fabricated on one chip, much higher circuit complexities than can be used with discrete amplifiers are economical. This can be used to give improved performance. Further, there are no insurmountable technical difficulties to temperature stabilizing the amplifier chip, giving chopper-stabilized performance with little added cost.

Operational amplifiers are designed for high gain, low offset voltage and low input current. As a result, dc biasing is considerably simplified in most applications; and they can be used with fairly simple design rules because many potential error terms can be neglected. This article will give examples demonstrating the range of usefulness of operational amplifiers in linear circuit design. The examples are certainly not all-inclusive, and it is hoped that they will stimulate even more ideas from others. A few practical hints on preventing oscillations in operational amplifiers will also be given since this is probably the largest single problem that many engineers have with these devices.

Although the designs presented use the LM101 operational amplifier and the LM102 voltage follower produced by National Semiconductor, most are generally applicable to all monolithic devices if the manufacturer's recommended frequency compensation is used and differences in maximum ratings are taken into account. A complete description of the LM101 is given elsewhere;[1] but, briefly, it differs from most other monolithic amplifiers, such as the LM709,[2] in that it has a ±30V differential input voltage range, a +15V, −12V common mode range with ±15V supplies and it can be compensated with a single 30 pF capacitor. The LM102,[3] which is also used here, is designed specifically as a voltage follower and features a maximum input current of 10 nA and a 10 V/μs slew rate.

operational-amplifier oscillator

The free-running multivibrator shown in *Figure 1* is an excellent example of an application where one does not normally consider using an operational amplifier. However, this circuit operates at low frequencies with relatively small capacitors because it can use a longer portion of the capacitor time constant since the threshold point of the operational amplifier is well determined. In addition, it has a completely-symmetrical output waveform along with a buffered output, although the symmetry can be varied by returning R2 to some voltage other than ground.



TL/H/7357–1

Figure 1. Free-running multivibrator

Another advantage of the circuit is that it will always self start and cannot hang up since there is more dc negative feedback than positive feedback. This can be a problem with many "textbook" multivibrators.

Since the operational amplifier is used open loop, the usual frequency compensation components are not required since they will only slow it down. But even without the 30 pF capacitor, the LM101 does have speed limitations which restrict the use of this circuit to frequencies below about 2 kHz.

The large input voltage range of the LM101 (both differential and single ended) permits large voltage swings on the input so that several time constants of the timing capacitor, C1, can be used. With most other amplifiers, R2 must be reduced to keep from exceeding these ratings, which requires that C1 be increased. Nonetheless, even when large values are needed for C1, smaller polarized capacitors may be used by returning them to the positive supply voltage instead of ground.

level shifting amplifier

Frequently, in the design of linear equipment, it is necessary to take a voltage which is referred to some dc level and produce an amplified output which is referred to ground. The most straight-forward way of doing this is to use a differential amplifier similar to that shown in *Figure 2a*. This circuit, however, has the disadvantages that the signal source is loaded by current from the input divider, R3 and R4, and that the feedback resistors must be very well matched to prevent erroneous outputs from the common mode input signal.

A circuit which does not have these problems is shown in *Figure 2b*. Here, an FET transistor on the output of the operational amplifier produces a voltage drop across the feedback resistor, R1, which is equal to the input voltage. The voltage across R2 will then be equal to the input voltage multiplied by the ratio, R2/R1; and the common mode rejection will be as good as the basic rejection of the amplifier, independent of the resistor tolerances. This voltage is buffered by an LM102 voltage follower to give a low impedance output.

An advantage of the LM101 in this circuit is that it will work with input voltages up to its positive supply voltages as long as the supplies are less than ±15V.

voltage comparators

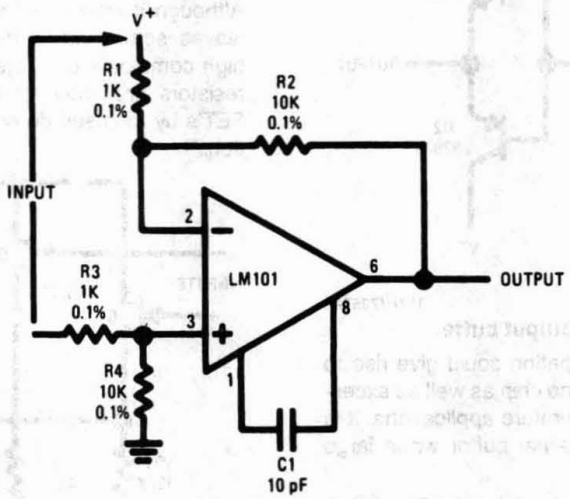
The LM101 is well suited to comparator applications for two reasons: first, it has a large differential input voltage range and, second, the output is easily clamped to make it compatible with various driver and logic circuits. It is true that it doesn't have the speed of the LM710[4] (10 μs versus 40 ns, under equivalent conditions); however, in many linear applications speed is not a problem and the lower input currents along with higher voltage capability of the LM101 is a tremendous benefit.

Two comparator circuits using the LM101 are shown in *Figure 3*. The one in *Figure 3a* shows a clamping scheme which makes the output signal directly compatible with DTL or TTL integrated circuits. An LM103 breakdown diode clamps the output at 0V or 4V in the low or high states, respectively. This particular diode was chosen because it has a sharp breakdown and low equivalent capacitance. When working as a comparator, the amplifier operates open loop so normally no frequency compensation is needed. Nonetheless, the stray capacitance between Pins 5 and 6 of the amplifier should be minimized to prevent low level oscillations when the comparator is in the active region. If this becomes a problem a 3 pF capacitor on the normal compensation terminals will eliminate it.

Figure 3b shows the connection of the LM101 as a comparator and lamp driver. Q1 switches the lamp, with R2 limiting the current surge resulting from turning on a cold lamp. R1 determines the base drive to Q1 while D1 keeps the amplifier from putting excessive reverse bias on the emitter-base junction of Q1 when it turns off.

more output current swing

Because almost all monolithic amplifiers use class-B output stages, they have good loaded output voltage swings, delivering ±10V at 5 mA with ±15V supplies. Demanding much more current from the integrated circuit would require, for one, that the output transistors be made considerably larg-



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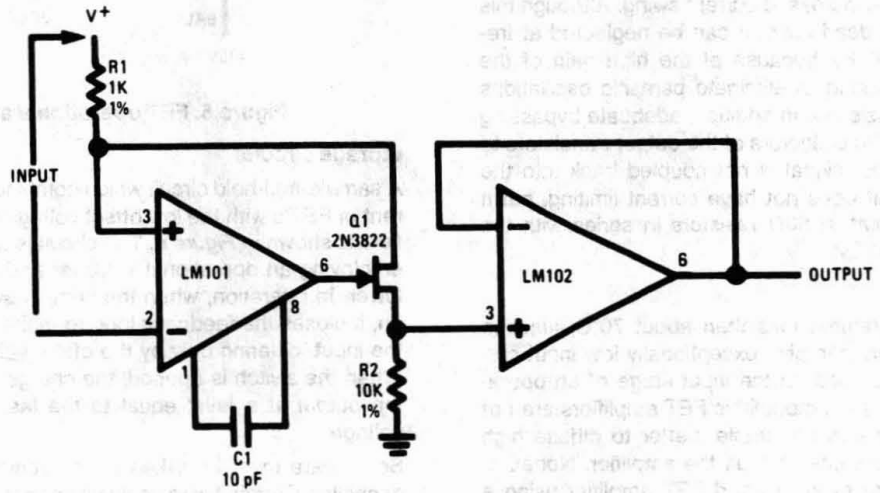
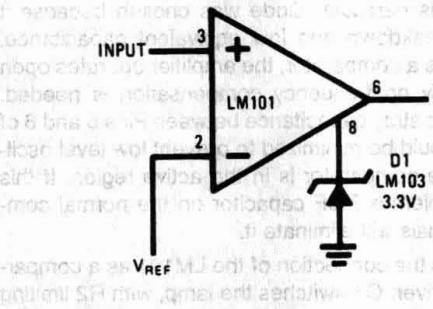
a. standard differential amplifier



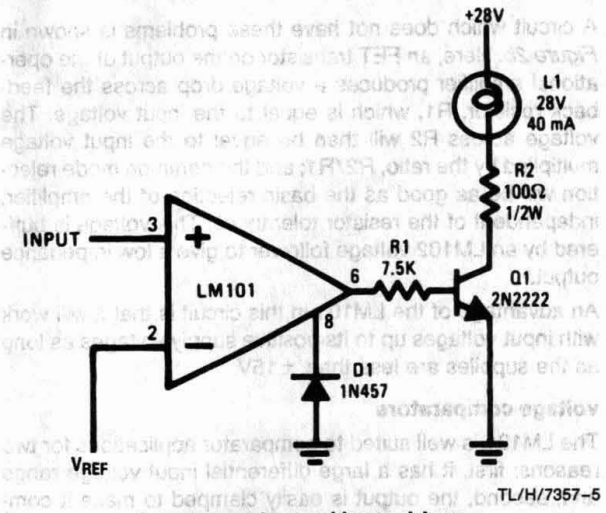
TL/H/7357–3

b. level-isolation amplifier

Figure 2. Level-shifting amplifiers



a. comparator for driving DTL and TTL integrated circuits



b. comparator and lamp driver

Figure 3. Voltage comparator circuits

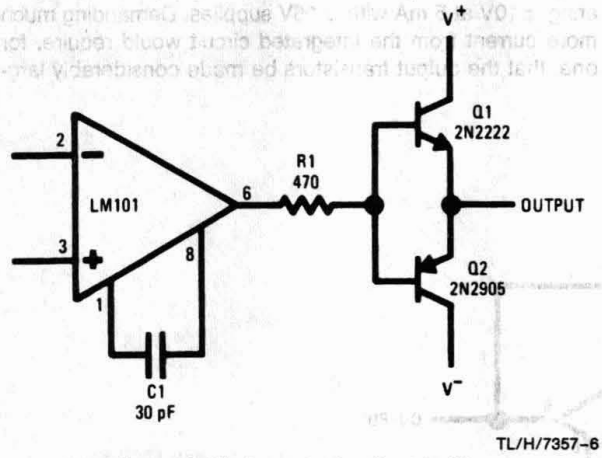


Figure 4. High current output buffer

er. In addition, the increased dissipation could give rise to troublesome thermal gradients on the chip as well as excessive package heating in high-temperature applications. It is therefore advisable to use an external buffer when large output currents are needed.

A simple way of accomplishing this is shown in *Figure 4*. A pair of complementary transistors are used on the output of the LM101 to get the increased current swing. Although this circuit does have a dead zone, it can be neglected at frequencies below 100 Hz because of the high gain of the amplifier. R1 is included to eliminate parasitic oscillations from the output transistors. In addition, adequate bypassing should be used on the collectors of the output transistors to insure that the output signal is not coupled back into the amplifier. This circuit does not have current limiting, but it can be added by putting 50Ω resistors in series with the collectors of Q1 and Q2.

an fet amplifier

For ambient temperatures less than about 70°C, junction field effect transistors can give exceptionally low input currents when they are used on the input stage of an operational amplifier. However, monolithic FET amplifiers are not now available since it is no simple matter to diffuse high quality FET's on the same chip as the amplifier. Nonetheless, it is possible to make a good FET amplifier using a discrete FET pair in conjunction with a monolithic circuit.

Such a circuit is illustrated in *Figure 5*. A matched FET pair, connected as source followers, is put in front of an integrated operational amplifier. The composite circuit has roughly the same gain as the integrated circuit by itself and is compensated for unity gain with a 30 pF capacitor as shown. Although it works well as a summing amplifier, the circuit leaves something to be desired in applications requiring high common mode rejection. This happens both because resistors are used for current sources and because the FET's by themself do not have good common mode rejection.

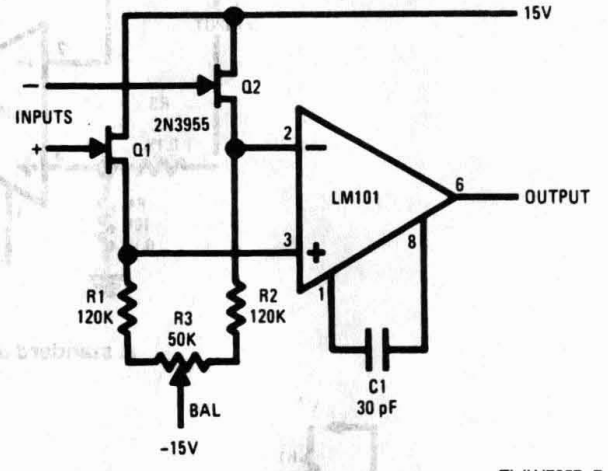


Figure 5. FET operational amplifier

storage circuits

A sample-and-hold circuit which combines the low input current of FET's with the low offset voltage of monolithic amplifiers is shown in *Figure 6*. The circuit is a unity gain amplifier employing an operational amplifier and an FET source follower. In operation, when the sample switch, Q2, is turned on, it closes the feedback loop to make the output equal to the input, differing only by the offset voltage of the LM101. When the switch is opened, the charge stored on C2 holds the output at a level equal to the last value of the input voltage.

Some care must be taken in the selection of the holding capacitor. Certain types, including paper and mylar, exhibit a polarization phenomenon which causes the sampled volt-

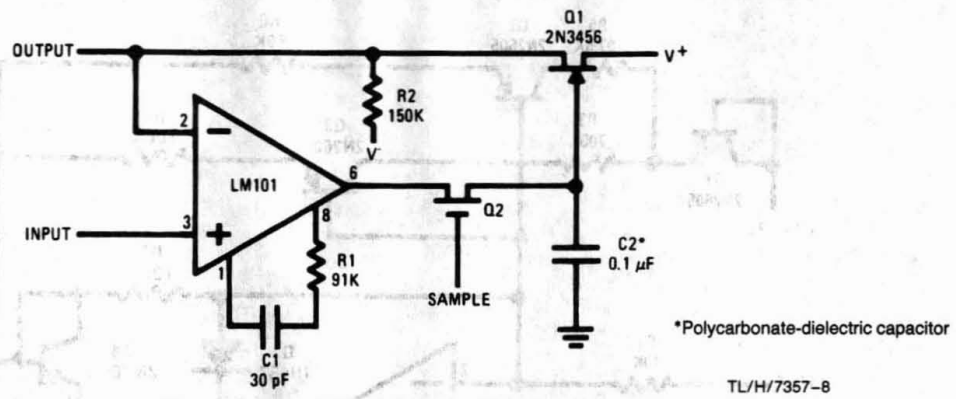


Figure 6. Low drift sample and hold

age to drop off by about 50 mV, and then stabilize, when the capacitor is exercised over a 5V range during the sample interval. This drop off has a time constant in the order of seconds. The effect, however, can be minimized by using capacitors with teflon, polyethylene, glass or polycarbonate dielectrics.

Although this circuit does not have a particularly low output resistance, fixed loads do not upset the accuracy since the loading is automatically compensated for during the sample interval. However, if the load is expected to change after sampling, a buffer such as the LM102 must be added between the FET and the output.

A second pole is introduced into the loop response of the amplifier by the switch resistance and the holding capacitor, C2. This can cause problems with overshoot or oscillation if it is not compensated for by adding a resistor, R1, in series with the LM101 compensation capacitor such that the breakpoint of the R1C1 combination is roughly equal to that of the switch and the holding capacitor.

It is possible to use an MOS transistor for Q1 without worrying about the threshold stability. The threshold voltage is balanced out during every sample interval so only the short-term threshold stability is important. When MOS transistors are used along with mechanical switches, drift rates less than 10 mV/min can be realized.

Additional features of the circuit are that the amplifier acts as a buffer so that the circuit does not load the input signal.

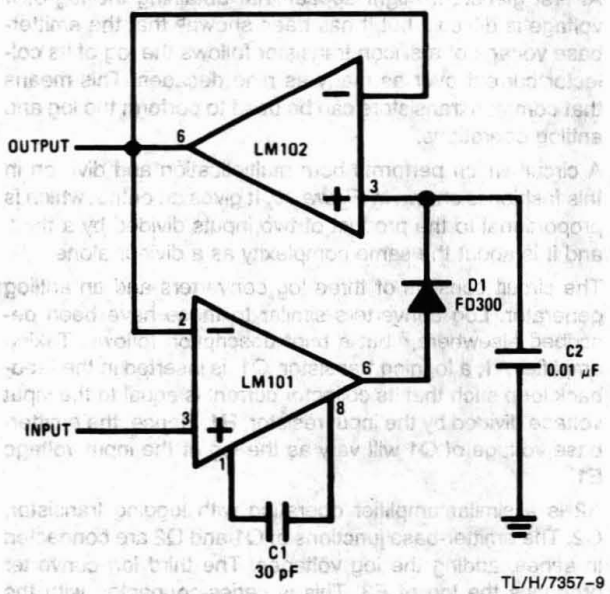


Figure 7. Positive peak detector with buffered output

Further, gain can also be provided by feeding back to the inverting input of the LM101 through a resistive divider instead of directly.

The peak detector in *Figure 7* is similar in many respects to the sample-and-hold circuit. A diode is used in place of the sampling switch. Connected as shown, it will conduct whenever the input is greater than the output, so the output will be equal to the peak value of the input voltage. In this case, an LM102 is used as a buffer for the storage capacitor, giving low drift along with a low output resistance.

As with the sample and hold, the differential input voltage range of the LM101 permits differences between the input and output voltages when the circuit is holding.

non-linear amplifiers

When a non-linear transfer function is needed from an operational amplifier, many methods of obtaining it present themself. However, they usually require diodes and are therefore difficult to temperature compensate for accurate breakpoints. One way of getting around this is to make the output swing so large that the diode threshold is negligible by comparison, but this is not always practical.

A method of producing very sharp, temperature-stable breakpoints in the transfer function of an operational amplifier is shown in *Figure 8*. For small input signals, the gain is determined by R1 and R2. Both Q2 and Q3 are conducting to some degree, but they do not affect the gain because their current gain is high and they do not feed any appreciable current back into the summing mode. When the output voltage rises to 2V (determined by R3, R4 and V^-), Q3 draws enough current to saturate, connecting R4 in parallel with R2. This cuts the gain in half. Similarly, when the output voltage rises to 4V, Q2 will saturate, again halving the gain.

Temperature compensation is achieved in this circuit by including Q1 and Q4. Q4 compensates the emitter-base voltage of Q2 and Q3 to keep the voltage across the feedback resistors, R4 and R6, very nearly equal to the output voltage while Q1 compensates for the emitter base voltage of these transistors as they go into saturation, making the voltage across R3 and R5 equal to the negative supply voltage. A detrimental effect of Q4 is that it causes the output resistance of the amplifier to increase at high output levels. It may therefore be necessary to use an output buffer if the circuit must drive an appreciable load.

servo preamplifier

In certain servo systems, it is desirable to get the rate signal required for loop stability from some sort of electrical, lead network. This can, for example, be accomplished with reactive elements in the feedback network of the servo preamplifier.

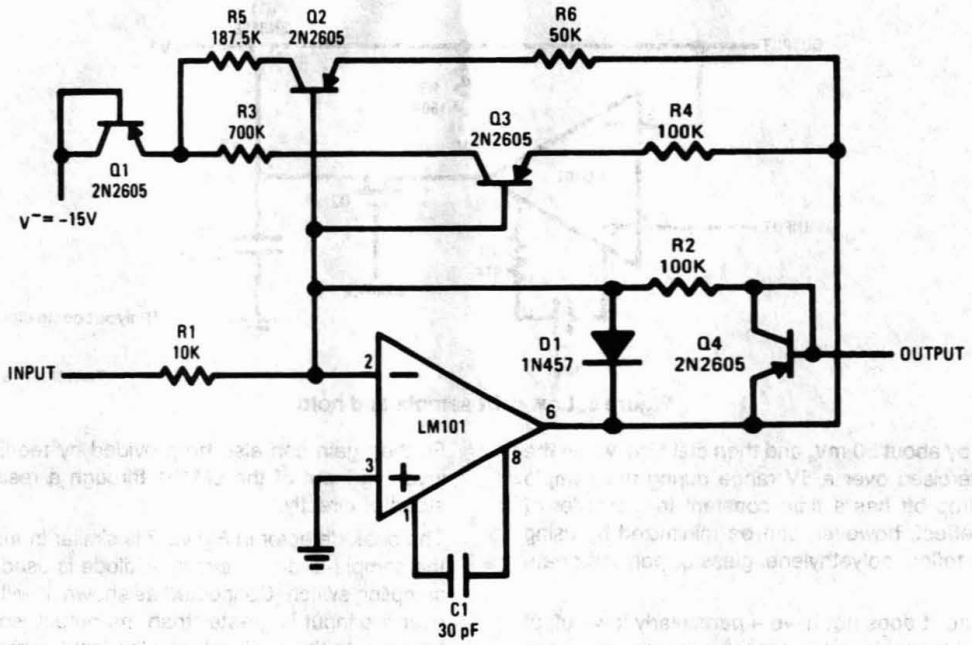


Figure 8. Nonlinear operational amplifier with temperature-compensated breakpoints

Many saturating servo amplifiers operate over an extremely wide dynamic range. For example, the maximum error signal could easily be 1000 times the signal required to saturate the system. Cases like this create problems with electrical rate networks because they cannot be placed in any part of the system which saturates. If the signal into the rate network saturates, a rate signal will only be developed over a narrow range of system operation; and instability will result when the error becomes large. Attempts to place the rate networks in front of the error amplifier or make the error amplifier linear over the entire range of error signals frequently gives rise to excessive dc error from signal attenuation.

These problems can be largely overcome using the kind of circuit shown in *Figure 9*. This amplifier operates in the linear mode until the output voltage reaches approximately 3V with 30 μA output current from the solar cell sensors. At this point the breakdown diodes in the feedback loop begin to conduct, drastically reducing the gain. However, a rate signal will still be developed because current is being fed back into the rate network (R1, R2 and C1) just as it would if the amplifier had remained in the linear operating region. In fact, the amplifier will not actually saturate until the error current reaches 6 mA, which would be the same as having a linear amplifier with a $\pm$600V output swing.

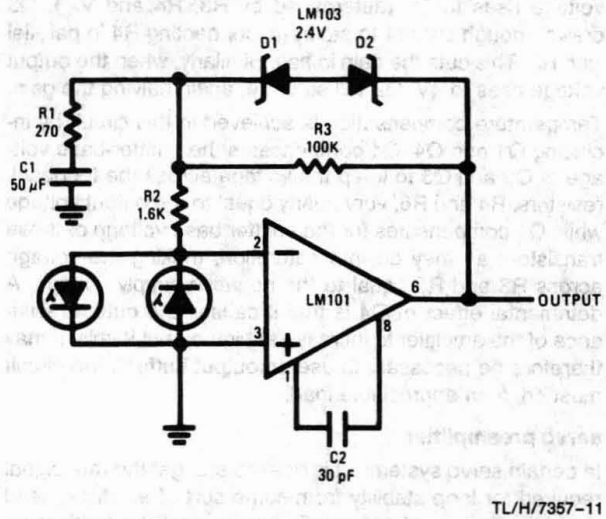


Figure 9. Saturating servo preamplifier with rate feedback

computing circuits

In analog computation it is a relatively simple matter to perform such operations as addition, subtraction, integration and differentiation by incorporating the proper resistors and capacitors in the feedback circuit of an amplifier. Many of these circuits are described in reference 5. Multiplication and division, however, are a bit more difficult. These operations are usually performed by taking the logarithms of the quantities, adding or subtracting as required and then taking the antilog.

At first glance, it might appear that obtaining the log of a voltage is difficult; but it has been shown[6] that the emitter-base voltage of a silicon transistor follows the log of its collector current over as many as nine decades. This means that common transistors can be used to perform the log and antilog operations.

A circuit which performs both multiplication and division in this fashion is shown in *Figure 10*. It gives an output which is proportional to the product of two inputs divided by a third, and it is about the same complexity as a divider alone.

The circuit consists of three log converters and an antilog generator. Log converters similar to these have been described elsewhere,[7] but a brief description follows. Taking amplifier A1, a logging transistor, Q1, is inserted in the feedback loop such that its collector current is equal to the input voltage divided by the input resistor, R1. Hence, the emitter-base voltage of Q1 will vary as the log of the input voltage E1.

A2 is a similar amplifier operating with logging transistor, Q2. The emitter-base junctions of Q1 and Q2 are connected in series, adding the log voltages. The third log converter produces the log of E3. This is series-connected with the antilog transistor, Q4; and the combination is hooked in par-

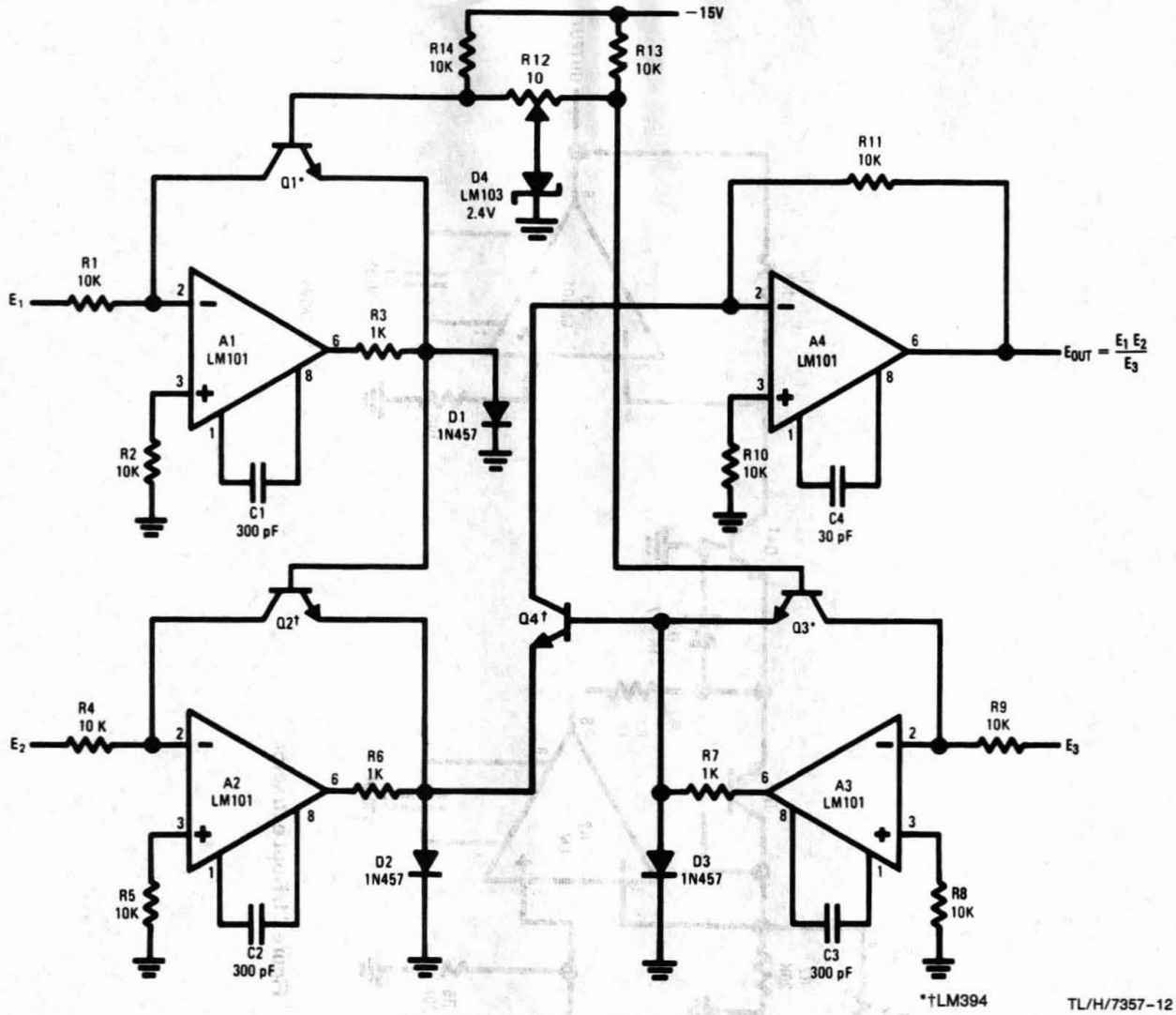


Figure 10. Analog multiplier/divider

allel with the output of the other two log convertors. Therefore, the emitter-base of Q4 will see the log of E3 subtracted from the sum of the logs of E1 and E2. Since the collector current of a transistor varies as the exponent of the emitter-base voltage, the collector current of Q4 will be proportional to the product of E1 and E2 divided by E3. This current is fed to the summing amplifier, A4, giving the desired output.

This circuit can give 1-percent accuracy for input voltages from 500 mV to 50V. To get this precision at lower input voltages, the offset of the amplifiers handling them must be individually balanced out. The zener diode, D4, increases the the collector-base voltage across the logging transistors to improve high current operation. It is not needed, and is in fact undesirable, when these transistors are running at currents less than 0.3 mA. At currents above 0.3 mA, the lead resistances of the transistors can become important (0.25Ω is 1-percent at 1 mA) so the transistors should be installed with short leads and no sockets.

An important feature of this circuit is that its operation is independent of temperature because the scale factor change in the log converter with temperature is compensated by an equal change in the scale factor of the antilog generator. It is only required that Q1, Q2, Q3 and Q4 be at the same temperature. Dual transistors should be used and arranged as shown in the figure so that thermal mismatches between cans appear as inaccuracies in scale factor (0.3-percent/°C) rather than a balance error (8-percent/°C). R12 is a balance potentiometer which nulls out the offset voltages of all the logging transistors. It is adjusted by setting all input voltages equal to 2V and adjusting for a 2V output voltage.

The logging transistors provide a gain which is dependent on their operating level, which complicates frequency compensation. Resistors (R3, R6 and R7) are put in the amplifier output to limit the maximum loop gain, and the compensation capacitor is chosen to correspond with this gain. As a result, the amplifiers are not especially designed for speed, but techniques for optimizing this parameter are given in reference 6.

Finally, clamp diodes D1 through D3, prevent exceeding the maximum reverse emitter-base voltage of the logging transistors with negative inputs.

root extractor*

Taking the root of a number using log converters is a fairly simple matter. All that is needed is to take the log of a voltage, divide it by, say ½ for the square root, and then

*The "extraction" used here doubtless has origin in the dental operation most of us would fear less than having to find even a square root without tables or other aids.

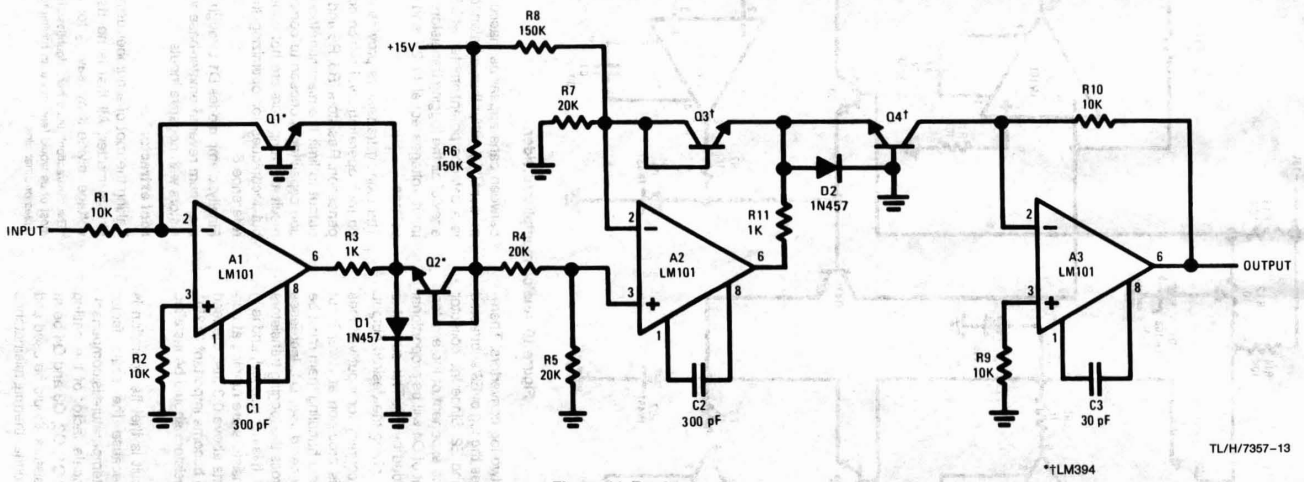
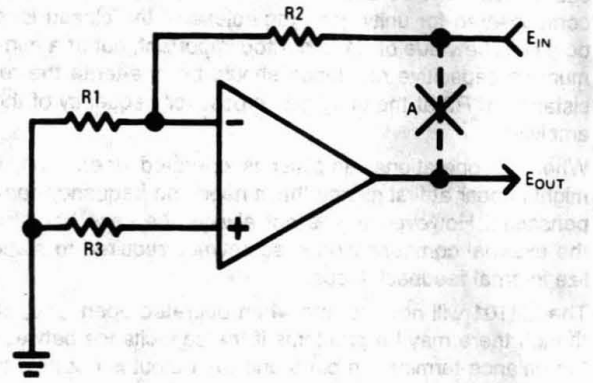
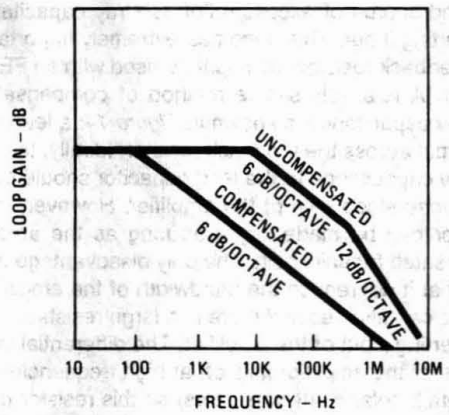


Figure 11. Root extractor



TL/H/7357–14

a. measuring loop gain



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b. typical response

Figure 12. Illustrating loop gain

take the antilog. A circuit which accomplishes this is shown in *Figure 11*. A1 and Q1 form the log converter for the input signal. This feeds Q2 which produces a level shift to give zero voltage into the R4, R5 divider for a 1V input. This divider reduces the log voltage by the ratio for the root desired and drives the buffer amplifier, A2. A2 has a second level shifting diode, Q3, its feedback network which gives the output voltage needed to get a 1V output from the antilog generator, consisting of A3 and Q4, with a unity input. The offset voltages of the transistors are nulled out by imbalancing R6 and R8 to give 1V output for 1V input, since any root of one is one.

Q2 and Q3 are connected as diodes in order to simplify the circuitry. This doesn't introduce problems because both operate over a very limited current range, and it is really only required that they match. R7 is a gain-compensating resistor which keeps the currents in Q2 and Q3 equal with changes in signal level.

As with the multiplier/divider, the circuit is insensitive to temperature as long as all the transistors are at the same temperature. Using transistor pairs and matching them as shown minimizes the effects of gradients.

The circuit has 1-percent accuracy for input voltages between 0.5 and 50V. For lower input voltages, A1 and A3 must have their offsets balanced out individually.

frequency compensation hints

The ease of designing with operational amplifiers sometimes obscures some of the rules which must be followed with any feedback amplifier to keep it from oscillating. In general, these problems stem from stray capacitance, excessive capacitive loading, inadequate supply bypassing or improper frequency compensation.

In frequency compensating an operational amplifier, it is best to follow the manufacturer's recommendations. However, if operating speed and frequency response is not a consideration, a greater stability margin can usually be obtained by increasing the size of the compensation capacitors. For example, replacing the 30 pF compensation capacitor on the LM101 with a 300 pF capacitor will make it ten times less susceptible to oscillation problems in the unity-gain connection. Similarly, on the LM709, using 0.05 μF, 1.5 kΩ, 2000 pF and 51Ω components instead of 5000 pF, 1.5 kΩ, 200 pF and 51Ω will give 20 dB more stability margin. Capacitor values less than those specified by the manufacturer for a particular gain connection should not be used since they will make the amplifier more sensitive to strays and capacitive loading, or the circuit can even oscillate with worst-case units.

The basic requirement for frequency compensating a feedback amplifier is to keep the frequency roll-off of the loop gain from exceeding 12 dB/octave when it goes through unity gain. *Figure 12a* shows what is meant by loop gain. The feedback loop is broken at the output, and the input sources are replaced by their equivalent impedance. Then the response is measured such that the feedback network is included.

Figure 12b gives typical responses for both uncompensated and compensated amplifiers. An uncompensated amplifier generally rolls off at 6 dB/octave, then 12 dB/octave and even 18 dB/octave as various frequency-limiting effects within the amplifier come into play. If a loop with this kind of response were closed, it would oscillate. Frequency compensation causes the gain to roll off at a uniform 6 dB/octave right down through unity gain. This allows some margin for excess rolloff in the external circuitry.

Some of the external influences which can affect the stability of an operational amplifier are shown in *Figure 13*. One is the load capacitance which can come from wiring, cables or an actual capacitor on the output. This capacitance works against the output impedance of the amplifier to attenuate high frequencies. If this added rolloff occurs before the loop gain goes through zero, it can cause instability. It should be remembered that this single rolloff point can give more than 6 dB/octave rolloff since the output impedance of the amplifier can be increasing with frequency.

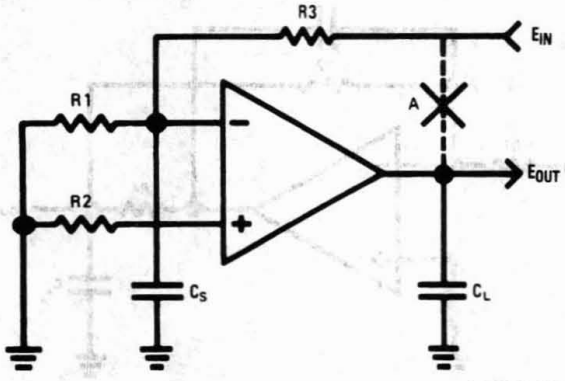

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Figure 13. External capacitances that affect stability

A second source of excess rolloff is stray capacitance on the inverting input. This becomes extremely important with large feedback resistors as might be used with an FET-input amplifier. A relatively simple method of compensating for this stray capacitance is shown in *Figure 14*: a lead capacitor, C1, put across the feedback resistor. Ideally, the ratio of the stray capacitance to the lead capacitor should be equal to the closed-loop gain of the amplifier. However, the lead capacitor can be made larger as long as the amplifier is compensated for unity gain. The only disadvantage of doing this is that it will reduce the bandwidth of the amplifier. Oscillations can also result if there is a large resistance on the non-inverting input of the amplifier. The differential input impedance of the amplifier falls off at high frequencies (especially with bipolar input transistors) so this resistor can produce troublesome rolloff if it is much greater than 10K, with most amplifiers. This is easily corrected by bypassing the resistor to ground.

When the capacitive load on an integrated amplifier is much greater than 100 pF, some consideration must be given to its effect on stability. Even though the amplifier does not oscillate readily, there may be a worst-case set of conditions under which it will. However, the amplifier can be stabilized for any value of capacitive loading using the circuit

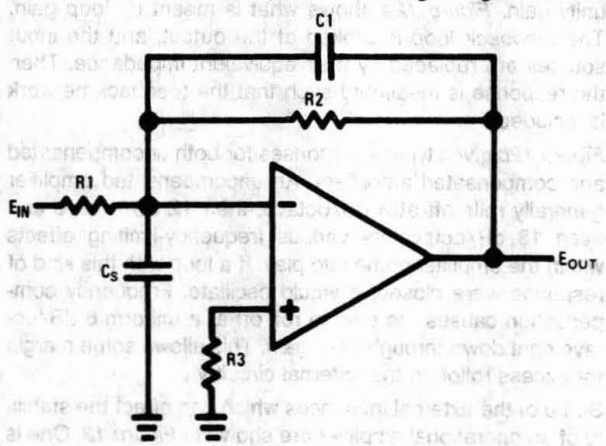

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Figure 14. Compensating stray input capacitance

shown in *Figure 15*. The capacitive load is isolated from the output of the amplifier with R4 which has a value of 50Ω to 100Ω for both the LM101 and the LM709. At high frequencies, the feedback path is through the lead capacitor, C1, so that the lag produced by the load capacitance does not cause instability. To use this circuit, the amplifier must be compensated for unity gain, regardless of the closed loop dc gain. The value of C1 is not too important, but at a minimum its capacitive reactance should be one-tenth the resistance of R2 at the unity-gain crossover frequency of the amplifier.

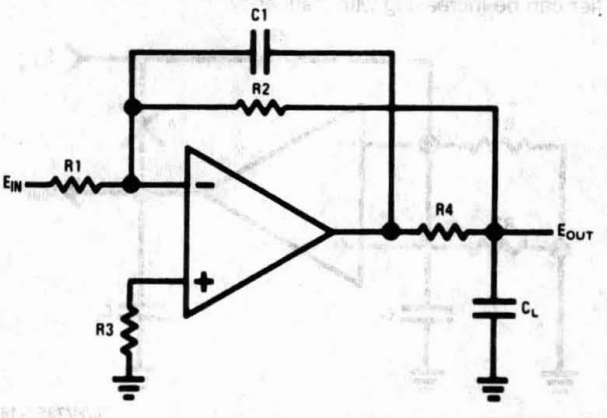

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Figure 15. Compensating for very large capacitive loads

When an operational amplifier is operated open loop, it might appear at first glance that it needs no frequency compensation. However, this is not always the case because the external compensation is sometimes required to stabilize internal feedback loops.

The LM101 will not oscillate when operated open loop, although there may be problems if the capacitance between the balance terminal on pin 5 and the output is not held to an absolute minimum. Feedback between these two points is regenerative if it is not balanced out with a larger feedback capacitance across the compensation terminals. Usually a 3 pF compensation capacitor will completely eliminate the problem. The LM709 will oscillate when operated open loop unless a 10 pF capacitor is connected across the input compensation terminals and a 3 pF capacitor is connected on the output compensation terminals.

Problems encountered with supply bypassing are insidious in that they will hardly ever show up in a Nyquist plot. This problem has not really been thoroughly investigated, probably because one sure cure is known: bypass the positive and negative supply terminals of each amplifier to ground with at least a 0.01 μF capacitor.

For example, a LM101 can take over 1 mH inductance in either supply lead without oscillation. This should not suggest that they should be run without bypass capacitors. It has been established that 100 LM101's on a single printed circuit board with common supply busses will oscillate if the supplies are not bypassed about every fifth device. This happens even though the inputs and outputs are completely isolated.

The LM709, on the other hand, will oscillate under many load conditions with as little as 18 inches of wire between the negative supply lead and a bypass capacitor. Therefore, it is almost essential to have a set of bypass capacitors for every device.

Operational amplifiers are specified for power supply rejection at frequencies less than the first break frequency of the open loop gain. At higher frequencies, the rejection can be reduced depending on how the amplifier is frequency compensated. For both the LM101 and LM709, the rejection of high frequency signals on the positive supply is excellent. However, the situation is different for the negative supplies. These two amplifiers have compensation capacitors from the output down to a signal point which is referred to the negative supply, causing the high frequency rejection for the negative supply to be much reduced. It is therefore important to have sufficient bypassing on the negative supply to remove transients if they can cause trouble appearing on the output. One fairly large (22 μF) tantalum capacitor on the negative power lead for each printed-circuit card is usually enough to solve potential problems.

When high-current buffers are used in conjunction with operational amplifiers, supply bypassing and decoupling are even more important since they can feed a considerable amount of signal back into the supply lines. For reference, bypass capacitors of at least 0.1 μF are required for a 50 mA buffer.

When emitter followers are used to drive long cables, additional precautions are required. An emitter follower by it-

self—which is not contained in a feedback loop—will frequently oscillate when connected to a long length of cable. When an emitter follower is connected to the output of an operational amplifier, it can produce oscillations that will persist no matter how the loop gain is compensated. An analysis of why this happens is not very enlightening, so suffice it to say that these oscillations can usually be eliminated by putting a ferrite bead[8] between the emitter follower and the cable.

Considering the loop gain of an amplifier is a valuable tool in understanding the influence of various factors on the stability of feedback amplifiers. But it is not too helpful in determining if the amplifier is indeed stable. The reason is that most problems in a well-designed system are caused by secondary effects—which occur only under certain conditions of output voltage, load current, capacitive loading, temperature, etc. Making frequency-phase plots under all these conditions would require unreasonable amounts of time, so it is invariably not done.

A better check on stability is the small-signal transient response. It can be shown mathematically that the transient response of a network has a one-for-one correspondence with the frequency domain response.† The advantage of transient response tests is that they are displayed instantaneously on an oscilloscope, so it is reasonable to test a circuit under a wide range of conditions.

Exact methods of analysis using transient response will not be presented here. This is not because these methods are difficult, although they are. Instead, it is because it is very easy to determine which conditions are unfavorable from the overshoot and ringing on the step response. The stability margin can be determined much more easily by how much greater the aggravating conditions can be made before the circuit oscillates than by analysis of the response under given conditions. A little practice with this technique can quickly yield much better results than classical methods even for the inexperienced engineer.

summary

A number of circuits using operational amplifiers have been proposed to show their versatility in circuit design. These have ranged from low frequency oscillators through circuits for complex analog computation. Because of the low cost of monolithic amplifiers, it is almost foolish to design dc amplifiers without integrated circuits. Moreover, the price makes it practical to take advantage of operational-amplifier performance in a variety of circuits where they are not normally used.

Many of the potential oscillation problems that can be encountered in both discrete and integrated operational amplifiers were described, and some conservative solutions to these problems were presented. The areas discussed included stray capacitance, capacitive loading and supply bypassing. Finally, a simplified method of quickly testing the stability of amplifier circuits over a wide range of operating conditions was suggested.

†The frequency-domain characteristics can be determined from the impulse response of a network and this is directly relatable to the step response through the convolution integral.

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Application of the LH0002 Current Amplifier

National Semiconductor
Application Note 13

INTRODUCTION

The LH0002 Current Amplifier integrated building block provides a wide band unity gain amplifier capable of providing peak currents of up to ±200 mA into a 50Ω load.

The circuit uses thick film technology to integrate 2 NPN and 2 PNP complementary matched silicon transistors with 4 cermet resistors on a single alumina ceramic substrate. A circuit schematic is shown in *Figure 1*. The negative thermal feedback provided by the close proximity of the components on a single substrate eliminates any thermal runaway problem that could occur if this circuit were constructed using discrete components.

A typical circuit features a dynamic input impedance of 200 kΩ, an output impedance of 6Ω, DC to 50 MHz bandwidth, and an output voltage swing that approaches supply voltage. A complete list of the guaranteed and typical values for the electrical characteristics under the stated conditions is given in Table I. These features make the LH0002 ideal for integration with an operational amplifier inside a closed loop configuration to increase its current output. The symmetrical class AB output portion of the circuit also provides a constant low output impedance for both the positive and negative slopes of output pulses.

CIRCUIT OPERATION

The majority of circuit applications will use symmetrical power supplies, with equal positive voltage being applied to pins 1 and 2, and equal negative voltage applied to pins 6 and 7.

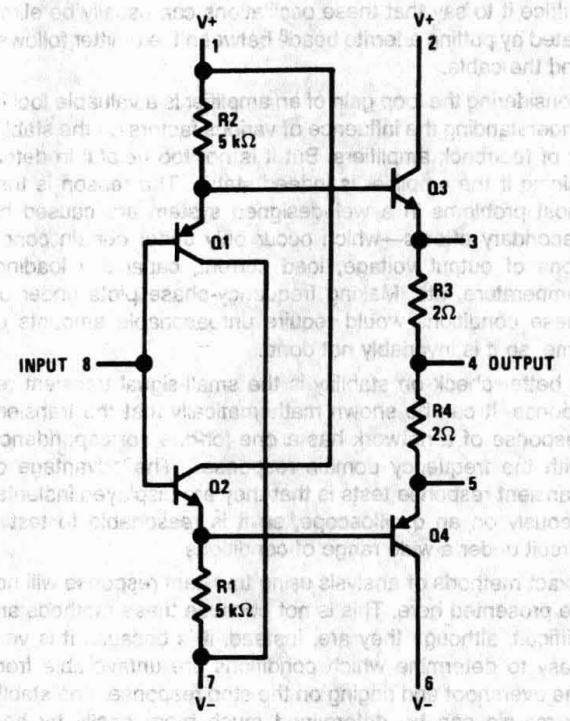

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FIGURE 1. Circuit Schematic

TABLE I. Electrical characteristics, specification applies for T_A = 25°C with +12.0V on pins 1 and 2; −12.0V on pins 6 and 7.

Parameters	Conditions	Min	Typ	Max	Units
Voltage Gain	R_S = 10 kΩ, R_L = 1.0 kΩ V_{IN} = 3.0 V_{pp}, f = 1.0 kHz T_A = 55°C to 125°C	0.95	0.97		
Input Impedance	R_S = 200 kΩ, V_{IN} = 1.0 V_{rms}, f = 1.0 kHz, R_L = 1.0 kΩ	180	200	—	kΩ
Output Impedance	V_{IN} = 1.0 V_{rms}, f = 1.0 kHz R_L = 50Ω, R_S = 10 kΩ	—	6	10	Ω
Output Voltage Swing	R_L = 1.0 kΩ, f = 1.0 kHz	±10	±11	—	V
DC Input Offset Voltage	R_S = 10 kΩ, R_L = 1.0 kΩ T_A = −55°C to 125°C	—	±40	±100	mV
DC Input Offset Current	R_S = 10 kΩ, R_L = 1.0 kΩ T_A = −55°C to 125°C	—	±6.0	±10	μA
Harmonic Distortion	V_{IN} = 5.0 V_{rms}, f = 1.0 kHz	—	0.1	—	%
Bandwidth	V_{IN} = 1.0 V_{rms}, R_L = 50Ω R_S = 100Ω	30	50	—	MHz
Positive Supply Current	R_S = 10 kΩ, R_L = 1 kΩ	—	+6.0	+10.0	mA
Negative Supply Current	R_S = 10 kΩ, R_L = 1 kΩ	—	−6.0	−10.0	mA

The reason that pin 2 and pin 6 are not connected internally to pin 1 and pin 7, respectively, is to increase the versatility of circuit operation by allowing a decreased voltage to be applied to pins 2 and 6 to minimize the power dissipation in Q3 and Q4. The larger voltage applied to the input stage also provides increased current drive as required to the output stage.

The operation of the circuit can be understood by considering that the input pin 8 is at V_{IN}. The emitter of Q1 will be approximately 0.6V more positive than V_{IN} at 25°C, and the converse is true for Q2. This 0.6V will provide a forward bias on Q3 to cancel out the Q1 base to emitter drop which in turn would provide V_{IN} at the output if all junctions, resistors, power supplies, etc., were electrically identical. The greatest error is introduced because the forward drops in the base-emitter junctions for the NPN and PNP devices are slightly different. For example, the V_{BE} of the NPN will be typically 0.6V and the V_{BE} of the PNP will be typically 0.64V under the same conditions of I_C = 2.4 mA at V_{CE} = 12.0V at 25°C. These are the approximate input stage circuit conditions for Q1 and Q2 for plus and minus 12V supplies. Fortunately, this error in both input and output offset voltage is almost always negligible when it is used inside the closed loop of a high gain operational amplifier.

A plot of input impedance vs frequency is shown in *Figure 2*. Inspection of this plot shows that the input impedance can be closely approximated to that of a simple first order linear network with a 45° phase lag at 0.6 MHz and a 90° phase lag at approximately one decade higher in frequency. This information is very useful for designers who have to integrate circuits which have large source impedances over a wide frequency range. The output impedance of the amplifier is very low, 6Ω typically, and in conjunction with a voltage bandwidth of approximately 50 MHz can be considered to be insignificant for most applications for this type of device.

A plot of the voltage bandwidth is shown in *Figure 3*. Inspection of this plot shows that phase information as well as gain information was included to assist users of this device. For example, at 10 MHz, less than an 8° phase lag would be subtracted from the phase margin of an operational amplifier when it is integrated with this device. The open loop gain of the operational amplifier would be decreased by less than 10% at 10 MHz and therefore can be considered to be insignificant for most applications.

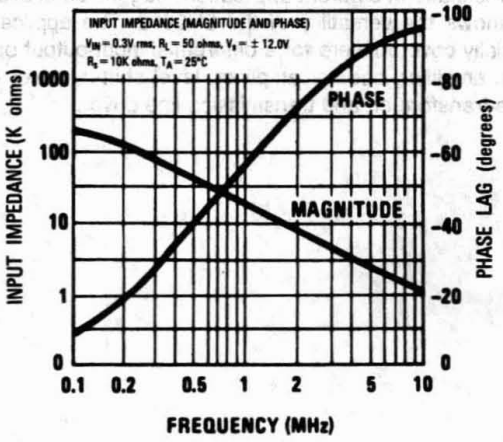

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FIGURE 2. Input Impedance vs Frequency

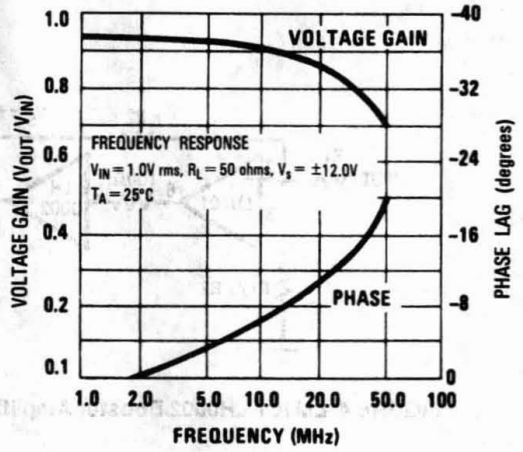

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FIGURE 3. Frequency Response

APPLICATIONS

Figure 4 shows the LH0002 integrated with the LM101 in a booster follower configuration. The configuration is stable without the requirement for any external compensation; however, it would behoove the designer to be conservative and bypass both the negative and positive power supplies with at least a 0.01 μf capacitor to cancel out any power supply lead inductance. A 100Ω damping resistor, located right at the input of the LH0002, might also be required between the operational amplifier and the booster amplifier. The physical layout will determine the requirement for this type of oscillation suppression. Current limiting can be added by incorporating series resistors from pins 2 and 6 to their respective power supplies. The exact value would be a function of power supply voltage and required operating temperature.

A breadboard of this configuration was assembled to empirically check the increase in offset voltage due to the addition of the LH0002. The offset voltage was measured with and without an LH0002 inside the loop with a voltage gain of 100, at −55°C, 25°C and 125°C. The additional offset voltage was less than 0.3% for all three temperature conditions even though the offset voltage of the LH0002 is much higher than that of the LM101. The high open loop gain of the LM101 divides out this source of circuit error. The integration of this device also allows higher closed loop circuit gain without excessive cross-over distortion than would be obtainable with the simple booster amplifier shown in *Figure 5*.

Figure 6 shows the LH0002 being used as a level shifter with a high pass filter on the input in order to reference the output to zero quiescent volts. The purpose of the 10 kΩ resistor is to provide current bias to the circuit's input transistors to reduce the output offset voltage. *Figure 3*, Input Impedance vs Frequency, provides a useful design aid in order to determine the value of the capacitor for the particular application. The 10 kΩ resistor, of course, has to be considered as being in parallel with the circuit's input impedance.

For a pulse input signal, the output impedance of the circuit remains low for both the positive and negative portions of the output pulse. This circuit provides both fast rise and fall times for pulse signals, even with capacitive loading. The LH0002 data sheet shows typical rise and fall times for both positive and negative pulses into a 50Ω load.

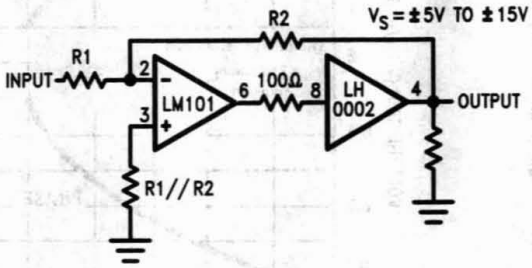

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FIGURE 4. LM101-LH0002 Booster Amplifier Integration

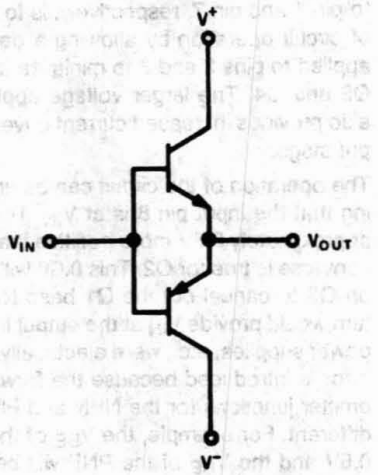

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FIGURE 5. Simple Booster Amplifier

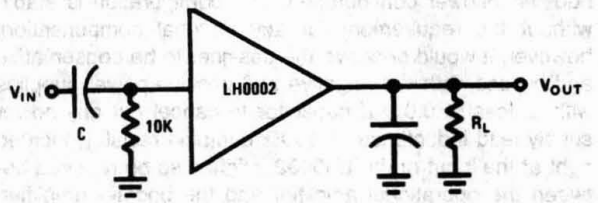

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FIGURE 6. Level Shifter

Figure 7 shows the LH0002 being used to drive a pulse-transformer. The low output offset voltage allows the pulse transformer to be directly coupled to the amplifier without using a coupling capacitor to prevent saturation. The pulse transformer can be used to change the amplitude and impedance level of the pulse, the polarity of the pulses, or, with the aid of a center-tapped winding, positive and negative pulses simultaneously.

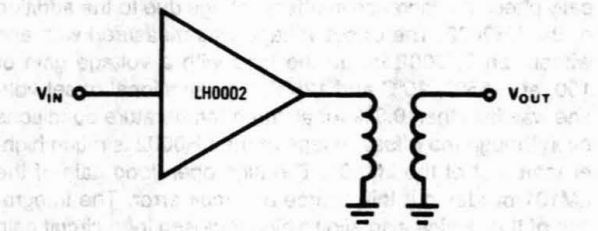

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FIGURE 7. Driver for a Pulse-Transformer

The LH0002 can also be used to drive long transmission lines. *Figure 8* shows a circuit configuration to match the output impedance of the amplifier to the load and coaxial cable for proper line termination to minimize reflections. A capacitor can be added to empirically adjust the time response of the waveform.

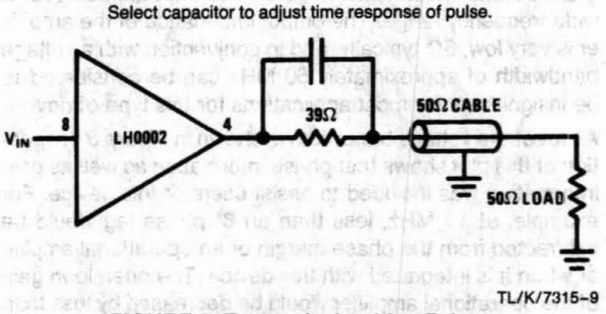

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FIGURE 8. Transmission Line Driver

SUMMARY

The multitude of different applications suggested in this article shows the versatility of the LH0002. The applications specially covered were for a differential input-output operational amplifier, booster amplifier, level shifter, driver for a pulse-transformer, and transmission line driver.

An Applications Guide for Op Amps

National Semiconductor
Application Note 20

INTRODUCTION

The general utility of the operational amplifier is derived from the fact that it is intended for use in a feedback loop whose feedback properties determine the feed-forward characteristics of the amplifier and loop combination. To suit it for this usage, the ideal operational amplifier would have infinite input impedance, zero output impedance, infinite gain and an open-loop 3 dB point at infinite frequency rolling off at 6 dB per octave. Unfortunately, the unit cost–in quantity–would also be infinite.

Intensive development of the operational amplifier, particularly in integrated form, has yielded circuits which are quite good engineering approximations of the ideal for finite cost. Quantity prices for the best contemporary integrated amplifiers are low compared with transistor prices of five years ago. The low cost and high quality of these amplifiers allows the implementation of equipment and systems functions impractical with discrete components. An example is the low frequency function generator which may use 15 to 20 operational amplifiers in generation, wave shaping, triggering and phase-locking.

The availability of the low-cost integrated amplifier makes it mandatory that systems and equipments engineers be familiar with operational amplifier applications. This paper will present amplifier usages ranging from the simple unity-gain buffer to relatively complex generator and wave shaping circuits. The general theory of operational amplifiers is not within the scope of this paper and many excellent references are available in the literature.[1,2,3,4] The approach will be shaded toward the practical, amplifier parameters will be discussed as they affect circuit performance, and application restrictions will be outlined.

The applications discussed will be arranged in order of increasing complexity in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies. The integrated amplifiers shown in the figures are for the most part internally compensated so frequency stabilization components are not shown; however, other amplifiers may be used to achieve greater operating speed in many circuits as will be shown in the text. Amplifier parameter definitions are contained in Appendix I.

THE INVERTING AMPLIFIER

The basic operational amplifier circuit is shown in *Figure 1*. This circuit gives closed-loop gain of R2/R1 when this ratio is small compared with the amplifier open-loop gain and, as the name implies, is an inverting circuit. The input impedance is equal to R1. The closed-loop bandwidth is equal to the unity-gain frequency divided by one plus the closed-loop gain.

The only cautions to be observed are that R3 should be chosen to be equal to the parallel combination of R1 and R2 to minimize the offset voltage error due to bias current and that there will be an offset voltage at the amplifier output equal to closed-loop gain times the offset voltage at the amplifier input.

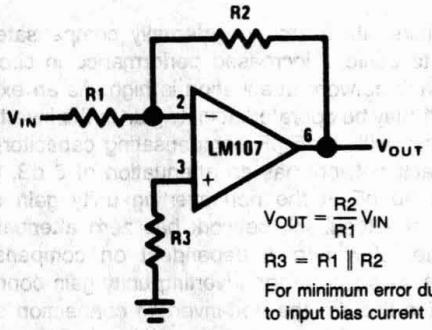

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FIGURE 1. Inverting Amplifier

Offset voltage at the input of an operational amplifier is comprised of two components, these components are identified in specifying the amplifier as input offset voltage and input bias current. The input offset voltage is fixed for a particular amplifier, however the contribution due to input

bias current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment the source resistance for both inputs should be equal. In this case the maximum offset voltage would be the algebraic sum of amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low source resistances and offset current causes the main error for high source resistances.

In high source resistance applications, offset voltage at the amplifier output may be adjusted by adjusting the value of R3 and using the variation in voltage drop across it as an input offset voltage trim.

Offset voltage at the amplifier output is not as important in AC coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak to peak linear output swing of the amplifier.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where feedback network attenuation is high. As an example, the LM101 may be operated at unity gain in the inverting amplifier circuit with a 15 pF compensating capacitor, since the feedback network has an attenuation of 6 dB, while it requires 30 pF in the non-inverting unity gain connection where the feedback network has zero attenuation. Since amplifier slew rate is dependent on compensation, the LM101 slew rate in the inverting unity gain connection will be twice that for the non-inverting connection and the inverting gain of ten connection will yield eleven times the slew rate of the non-inverting unity gain connection. The compensation trade-off for a particular connection is stability versus bandwidth, larger values of compensation capacitor yield greater stability and lower bandwidth and vice versa.

The preceding discussion of offset voltage, bias current and stability is applicable to most amplifier applications and will be referenced in later sections. A more complete treatment is contained in Reference 4.

THE NON-INVERTING AMPLIFIER

Figure 2 shows a high input impedance non-inverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3 dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain.

The primary differences between this connection and the inverting circuit are that the output is not inverted and that the input impedance is very high and is equal to the differential input impedance multiplied by loop gain. (Open loop gain/Closed loop gain.) In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance.

Applications cautions are the same for this amplifier as for the inverting amplifier with one exception. The amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.

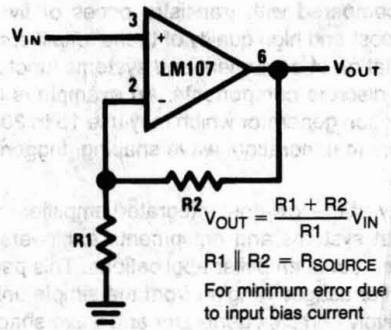


FIGURE 2. Non-Inverting Amplifier

THE UNITY-GAIN BUFFER

The unity-gain buffer is shown in *Figure 3*. The circuit gives the highest input impedance of any operational amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open-loop gain or to the common mode rejection, whichever is less.

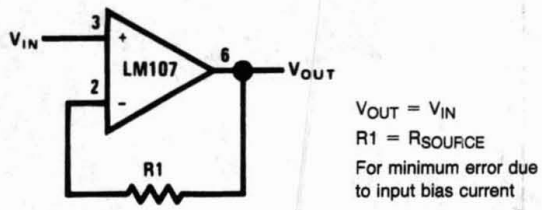


FIGURE 3. Unity Gain Buffer

Input impedance is a misleading concept in a DC coupled unity-gain buffer. Bias current for the amplifier will be supplied by the source resistance and will cause an error at the amplifier input due to its voltage drop across the source resistance. Since this is the case, a low bias current amplifier such as the LH102[6] should be chosen as a unity-gain buffer when working from high source resistances. Bias current compensation techniques are discussed in Reference 5.

The cautions to be observed in applying this circuit are three: the amplifier must be compensated for unity gain operation, the output swing of the amplifier may be limited by the amplifier common mode range, and some amplifiers exhibit a latch-up mode when the amplifier common mode range is exceeded. The LM107 may be used in this circuit with none of these problems; or, for faster operation, the LM102 may be chosen.

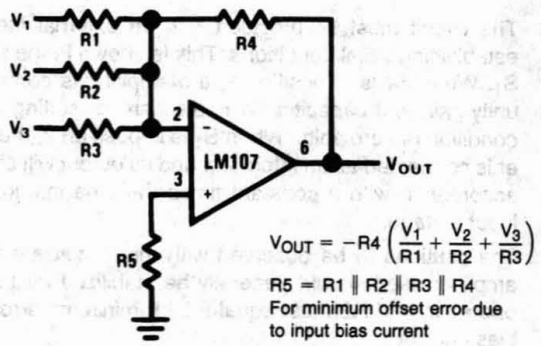


FIGURE 4. Summing Amplifier

SUMMING AMPLIFIER

The summing amplifier, a special case of the inverting amplifier, is shown in *Figure 4*. The circuit gives an inverted output which is equal to the weighted algebraic sum of all three inputs. The gain of any input of this circuit is equal to the ratio of the appropriate input resistor to the feedback resistor, R4. Amplifier bandwidth may be calculated as in the inverting amplifier shown in *Figure 1* by assuming the input resistor to be the parallel combination of R1, R2, and R3. Application cautions are the same as for the inverting amplifier. If an uncompensated amplifier is used, compensation is calculated on the basis of this bandwidth as is discussed in the section describing the simple inverting amplifier.

The advantage of this circuit is that there is no interaction between inputs and operations such as summing and weighted averaging are implemented very easily.

THE DIFFERENCE AMPLIFIER

The difference amplifier is the complement of the summing amplifier and allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to the two inputs. This circuit is shown in *Figure 5* and is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.

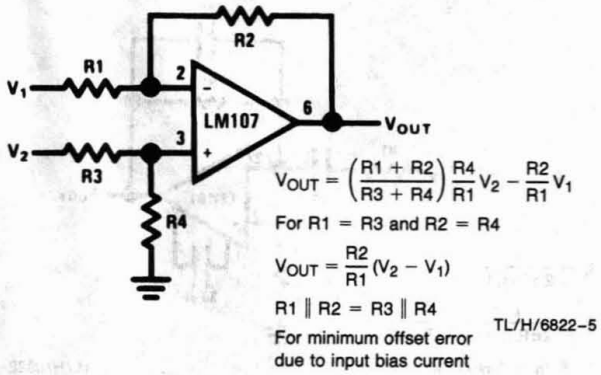


FIGURE 5. Difference Amplifier

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal; inverting input impedance is the same as for the inverting amplifier of *Figure 1* and the non-inverting input impedance is the sum of R3 and R4. Gain for either input is the ratio of R1 to R2 for the special case of a differential input single-ended output where R1 = R3 and R2 = R4. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

DIFFERENTIATOR

The differentiator is shown in *Figure 6* and, as the name implies, is used to perform the mathematical operation of differentiation. The form shown is not the practical form, it is a true differentiator and is extremely susceptible to high frequency noise since AC gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator, R1C1, is an RC low pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity gain.

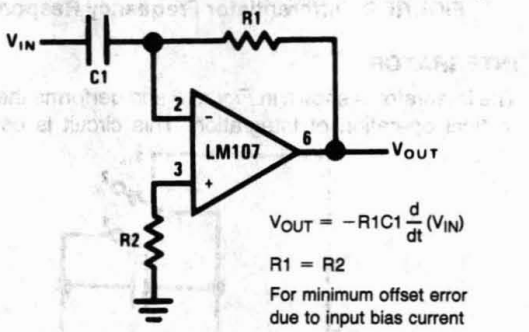
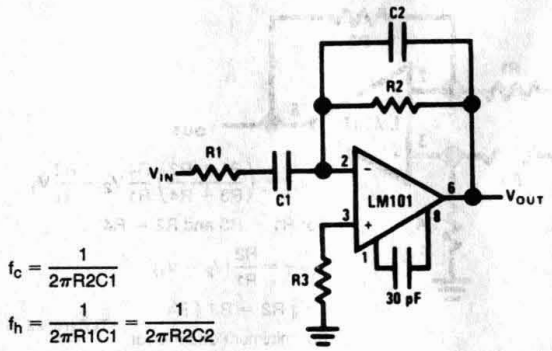


FIGURE 6. Differentiator



$$f_c = \frac{1}{2\pi R2C1}$$

$$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

$f_c < f_h < f_{unity\ gain}$

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FIGURE 7. Practical Differentiator

A practical differentiator is shown in *Figure 7*. Here both the stability and noise problems are corrected by addition of two additional components, R1 and C2. R2 and C2 form a 6 dB per octave high frequency roll-off in the feedback network and R1C1 form a 6 dB per octave roll-off network in the input network for a total high frequency roll-off of 12 dB per octave to reduce the effect of high frequency input and amplifier noise. In addition R1C1 and R2C2 form lead networks in the feedback loop which, if placed below the amplifier unity gain frequency, provide 90° phase lead to compensate the 90° phase lag of R2C1 and prevent loop instability. A gain frequency plot is shown in *Figure 8* for clarity.

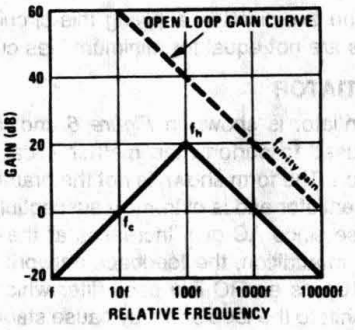

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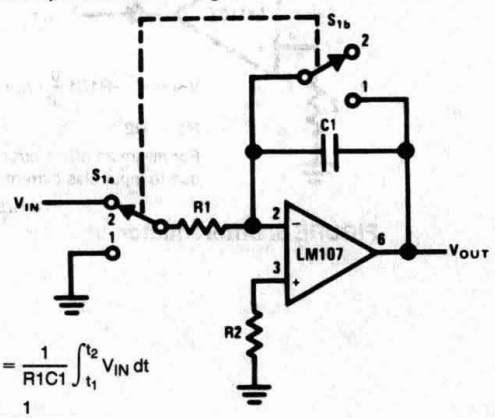
FIGURE 8. Differentiator Frequency Response

INTEGRATOR

The integrator is shown in *Figure 9* and performs the mathematical operation of integration. This circuit is essentially



$$V_{OUT} = \frac{1}{R1C1}\int_{t_1}^{t_2} V_{IN}\,dt$$

$$f_c = \frac{1}{2\pi R1C1}$$

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R1 = R2

For minimum offset error due to input bias current

FIGURE 9. Integrator

a low-pass filter with a frequency response decreasing at 6 dB per octave. An amplitude-frequency plot is shown in *Figure 10*.

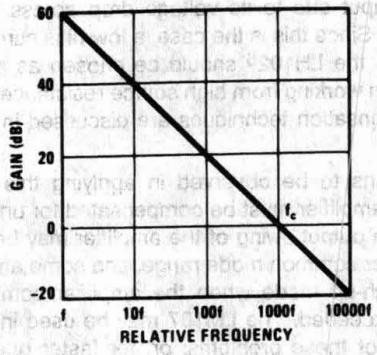

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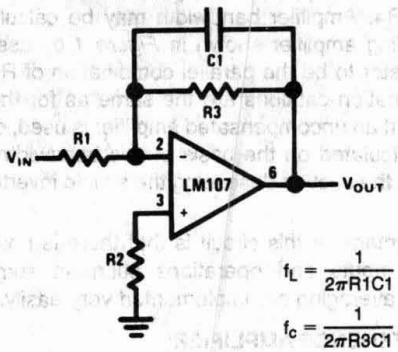
FIGURE 10. Integrator Frequency Response

The circuit must be provided with an external method of establishing initial conditions. This is shown in the figure as S_1. When S_1 is in position 1, the amplifier is connected in unity-gain and capacitor C1 is discharged, setting an initial condition of zero volts. When S_1 is in position 2, the amplifier is connected as an integrator and its output will change in accordance with a constant times the time integral of the input voltage.

The cautions to be observed with this circuit are two: the amplifier used should generally be stabilized for unity-gain operation and R2 must equal R1 for minimum error due to bias current.

SIMPLE LOW-PASS FILTER

The simple low-pass filter is shown in *Figure 11*. This circuit has a 6 dB per octave roll-off after a closed-loop 3 dB point defined by f_c. Gain below this corner frequency is defined by the ratio of R3 to R1. The circuit may be considered as an AC integrator at frequencies well above f_c; however, the time domain response is that of a single RC rather than an integral.



$$f_L = \frac{1}{2\pi R1C1}$$

$$f_c = \frac{1}{2\pi R3C1}$$

$$A_L = \frac{R3}{R1}$$

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FIGURE 11. Simple Low Pass Filter

R2 should be chosen equal to the parallel combination of R1 and R3 to minimize errors due to bias current. The amplifier should be compensated for unity-gain or an internally compensated amplifier can be used.

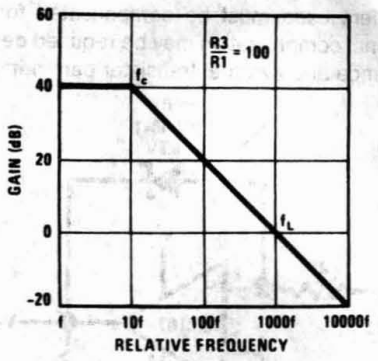

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FIGURE 12. Low Pass Filter Response

A gain frequency plot of circuit response is shown in *Figure 12* to illustrate the difference between this circuit and the true integrator.

THE CURRENT-TO-VOLTAGE CONVERTER

Current may be measured in two ways with an operational amplifier. The current may be converted into a voltage with a resistor and then amplified or the current may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage transducer avoids both of these problems.

The current-to-voltage transducer is shown in *Figure 13*. The input current is fed directly into the summing node and the amplifier output voltage changes to extract the same current from the summing node through R1. The scale factor of this circuit is R1 volts per amp. The only conversion error in this circuit is I_{bias} which is summed algebraically with I_{IN}.

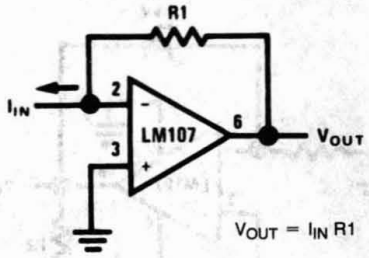

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FIGURE 13. Current to Voltage Converter

This basic circuit is useful for many applications other than current measurement. It is shown as a photocell amplifier in the following section.

The only design constraints are that scale factors must be chosen to minimize errors due to bias current and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity-gain operation. Valuable techniques for bias current compensation are contained in Reference 5.

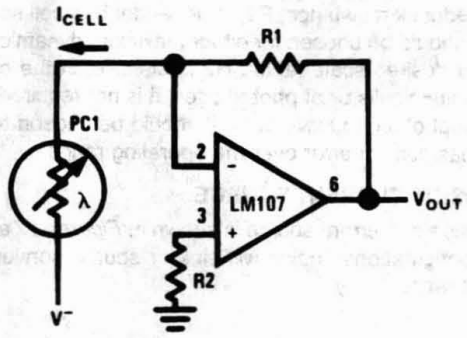

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FIGURE 14. Amplifier for Photoconductive Cell

PHOTOCELL AMPLIFIERS

Amplifiers for photoconductive, photodiode and photovoltaic cells are shown in *Figures 14, 15* and *16* respectively.

All photogenerators display some voltage dependence of both speed and linearity. It is obvious that the current rhough a photoconductive cell will not display strict proportionality to incident light if the cell terminal voltage is allowed to vary with cell conductance. Somewhat less obvious is the fact that photodiode leakage and photovoltaic cell internal losses are also functions of terminal voltage. The current-to-voltage converter neatly sidesteps gross linearity problems by fixing a constant terminal voltage, zero in the case of photovoltaic cells and a fixed bias voltage in the case of photoconductors or photodiodes.

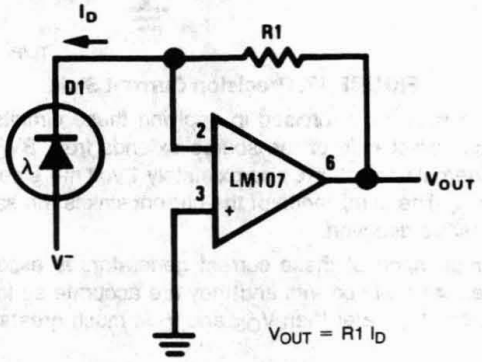

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FIGURE 15. Photodiode Amplifier

Photodetector speed is optimized by operating into a fixed low load impedance. Currently available photovoltaic detectors show response times in the microsecond range at zero load impedance and photoconductors, even though slow, are materially faster at low load resistances.

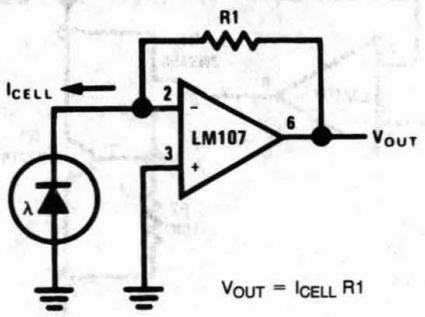

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FIGURE 16. Photovoltaic Cell Amplifier

The feedback resistance, R1, is dependent on cell sensitivity and should be chosen for either maximum dynamic range or for a desired scale factor. R2 is elective: in the case of photovoltaic cells or of photodiodes, it is not required in the case of photoconductive cells, it should be chosen to minimize bias current error over the operating range.

PRECISION CURRENT SOURCE

The precision current source is shown in *Figures 17* and *18*. The configurations shown will sink or source conventional current respectively.

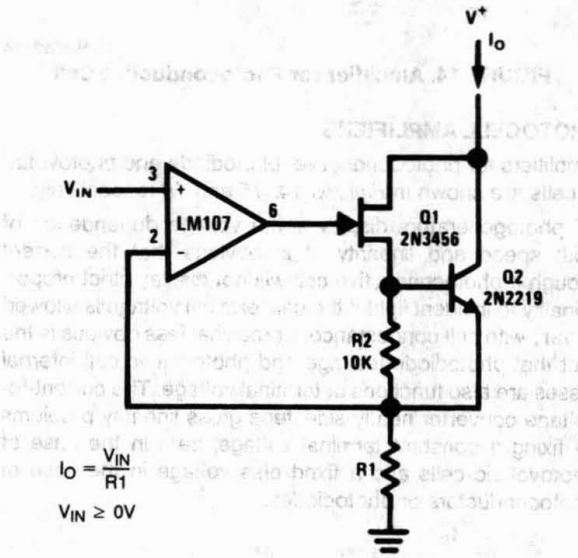

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FIGURE 17. Precision Current Sink

Caution must be exercised in applying these circuits. The voltage compliance of the source extends from BV_{CER} of the external transistor to approximately 1 volt more negative than V_{IN}. The compliance of the current sink is the same in the positive direction.

The impedance of these current generators is essentially infinite for small currents and they are accurate so long as V_{IN} is much greater than V_{OS} and I_O is much greater than I_{bias}.

The source and sink illustrated in *Figures 17* and *18* use an FET to drive a bipolar output transistor. It is possible to use a Darlington connection in place of the FET-bipolar combination in cases where the output current is high and the base current of the Darlington input would not cause a significant error.

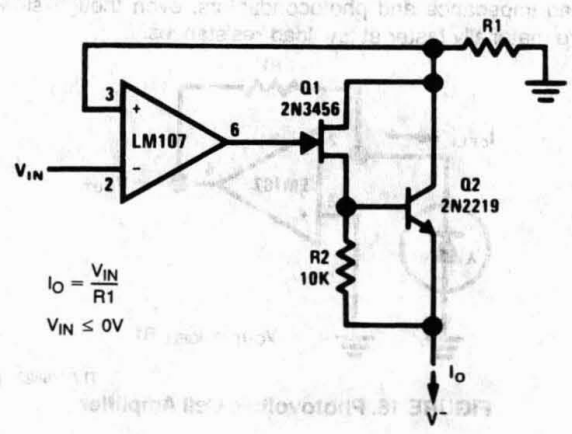

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FIGURE 18. Precision Current Source

The amplifiers used must be compensated for unity-gain and additional compensation may be required depending on load reactance and external transistor parameters.

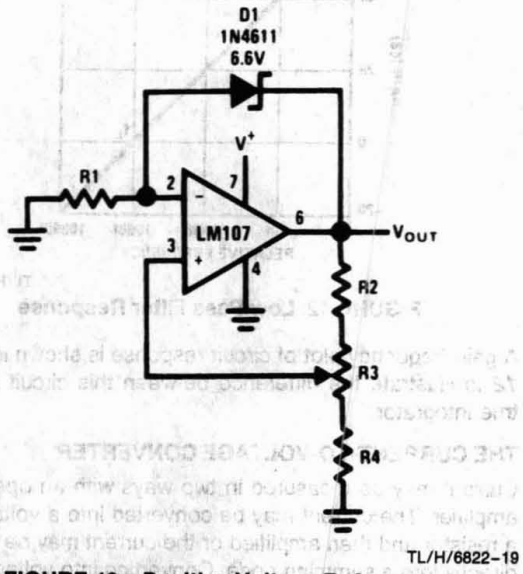

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FIGURE 19a. Positive Voltage Reference

ADJUSTABLE VOLTAGE REFERENCES

Adjustable voltage reference circuits are shown in *Figures 19* and *20*. The two circuits shown have different areas of applicability. The basic difference between the two is that *Figure 19* illustrates a voltage source which provides a voltage greater than the reference diode while *Figure 20* illustrates a voltage source which provides a voltage lower than the reference diode. The figures show both positive and negative voltage sources.

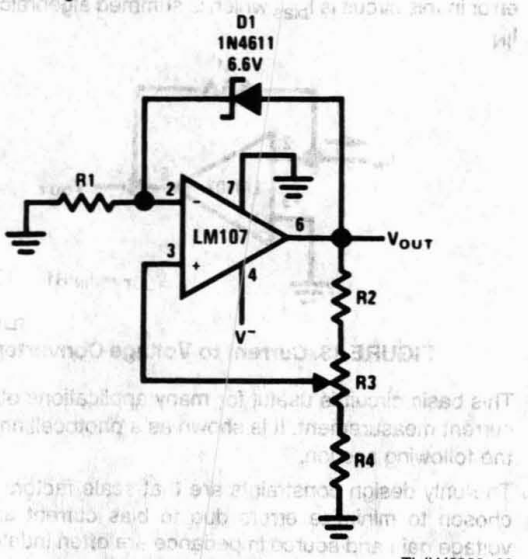

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FIGURE 19b. Negative Voltage Reference

High precision extended temperature applications of the circuit of *Figure 19* require that the range of adjustment of V_{OUT} be restricted. When this is done, R1 may be chosen to provide optimum zener current for minimum zener T.C. Since I_Z is not a function of V^+, reference T.C. will be independent of V^+.

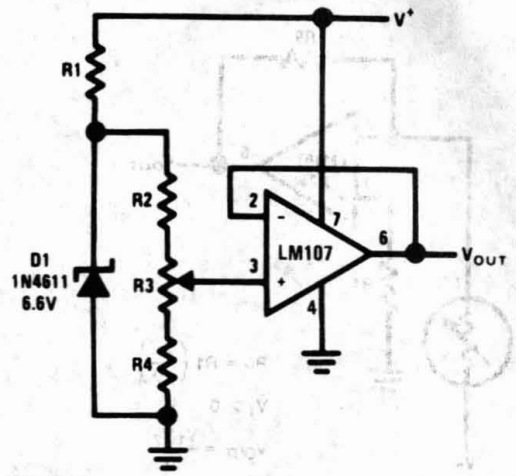

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FIGURE 20a. Positive Voltage Reference

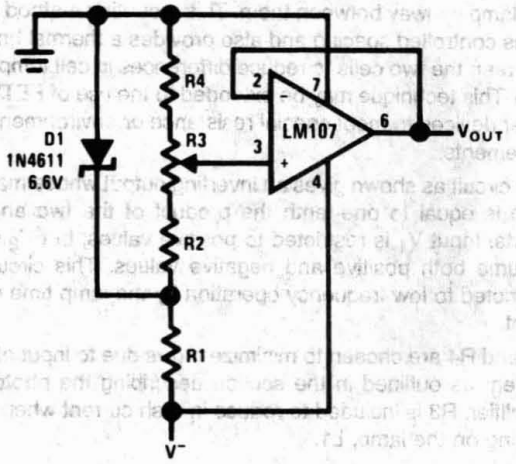

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FIGURE 20b. Negative Voltage Reference

The circuit of *Figure 20* is suited for high precision extended temperature service if V^+ is reasonably constant since I_Z is dependent on V^+. R1, R2, R3, and R4 are chosen to provide the proper I_Z for minimum T.C. and to minimize errors due to I_{bias}.

The circuits shown should both be compensated for unity-gain operation or, if large capacitive loads are expected, should be overcompensated. Output noise may be reduced in both circuits by bypassing the amplifier input.

The circuits shown employ a single power supply, this requires that common mode range be considered in choosing an amplifier for these applications. If the common mode range requirements are in excess of the capability of the amplifier, two power supplies may be used. The LH101 may be used with a single power supply since the common mode range is from V^+ to within approximately 2 volts of V^-.

THE RESET STABILIZED AMPLIFIER

The reset stabilized amplifier is a form of chopper-stabilized amplifier and is shown in *Figure 21*. As shown, the amplifier is operated closed-loop with a gain of one.

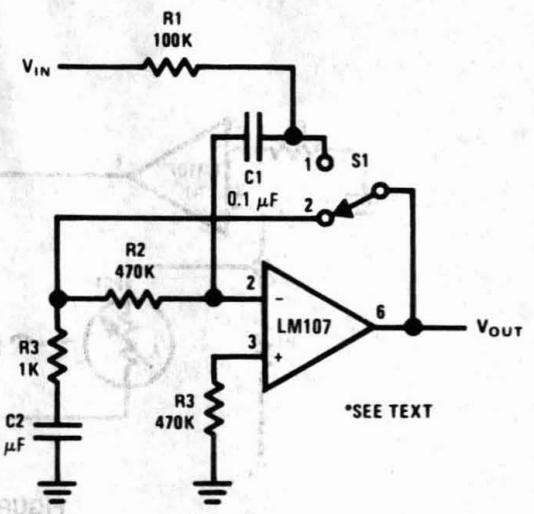

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FIGURE 21. Reset Stabilized Amplifier

The connection is useful in eliminating errors due to offset voltage and bias current. The output of this circuit is a pulse whose amplitude is equal to V_{IN}. Operation may be understood by considering the two conditions corresponding to the position of S_1. When S_1 is in position 2, the amplifier is connected in the unity gain connection and the voltage at the output will be equal to the sum of the input offset voltage and the drop across R2 due to input bias current. The voltage at the inverting input will be equal to input offset voltage. Capacitor C1 will charge to the sum of input offset voltage and V_{IN} through R1. When C1 is charged, no current flows through the source resistance and R1 so there is no error due to input resistance. S_1 is then changed to position 1. The voltage stored on C1 is inserted between the output and inverting input of the amplifier and the output of the amplifier changes by V_{IN} to maintain the amplifier input at the input offset voltage. The output then changes from $(V_{OS} + I_{bias}R2)$ to $(V_{IN} + I_{bias}R2)$ as S_1 is changed from position 2 to position 1. Amplifier bias current is supplied through R2 from the output of the amplifier or from C2 when S_1 is in position 2 and position 1 respectively. R3 serves to reduce the offset at the amplifier output if the amplifier must have maximum linear range or if it is desired to DC couple the amplifier.

An additional advantage of this connection is that input resistance approaches infinity as the capacitor C1 approaches full charge, eliminating errors due to loading of the source resistance. The time spent in position 2 should be long with respect to the charging time of C1 for maximum accuracy.

The amplifier used must be compensated for unity gain operation and it may be necessary to overcompensate because of the phase shift across R2 due to C1 and the amplifier input capacity. Since this connection is usually used at very low switching speeds, slew rate is not normally a practical consideration and overcompensation does not reduce accuracy.

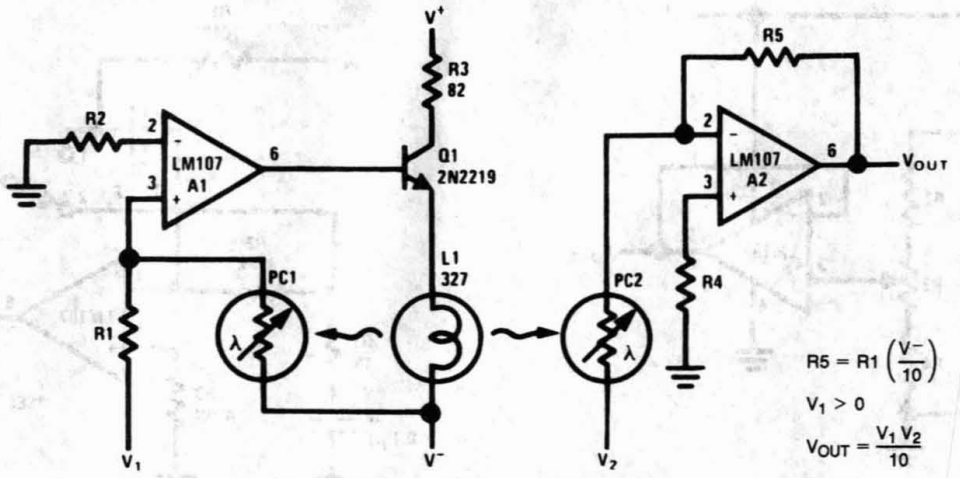

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FIGURE 22. Analog Multiplier

THE ANALOG MULTIPLIER

A simple embodiment of the analog multiplier is shown in *Figure 22*. This circuit circumvents many of the problems associated with the log-antilog circuit and provides three quadrant analog multiplication which is relatively temperature insensitive and which is not subject to the bias current errors which plague most multipliers.

Circuit operation may be understood by considering A2 as a controlled gain amplifier, amplifying V_2, whose gain is dependent on the ratio of the resistance of PC2 to R5 and by considering A1 as a control amplifier which establishes the resistance of PC2 as a function of V_1. In this way it is seen that V_{OUT} is a function of both V_1 and V_2.

A1, the control amplifier, provides drive for the lamp, L1. When an input voltage, V_1, is present, L1 is driven by A1 until the current to the summing junction from the negative supply through PC1 is equal to the current to the summing junction from V_1 through R1. Since the negative supply voltage is fixed, this forces the resistance of PC1 to a value proportional to R1 and to the ratio of V_1 to V^-. L1 also illuminates PC2 and, if the photoconductors are matched, causes PC2 to have a resistance equal to PC1.

A2, the controlled gain amplifier, acts as an inverting amplifier whose gain is equal to the ratio of the resistance of PC2 to R5. If R5 is chosen equal to the product of R1 and V^-, then V_{OUT} becomes simply the product of V_1 and V_2. R5 may be scaled in powers of ten to provide any required output scale factor.

PC1 and PC2 should be matched for best tracking over temperature since the T.C. of resistance is related to resistance match for cells of the same geometry. Small mismatches may be compensated by varying the value of R5 as a scale factor adjustment. The photoconductive cells should receive equal illumination from L1, a convenient method is to mount the cells in holes in an aluminum block and to mount the lamp midway between them. This mounting method provides controlled spacing and also provides a thermal bridge between the two cells to reduce differences in cell temperature. This technique may be extended to the use of FET's or other devices to meet special resistance or environment requirements.

The circuit as shown gives an inverting output whose magnitude is equal to one-tenth the product of the two analog inputs. Input V_1 is restricted to positive values, but V_2 may assume both positive and negative values. This circuit is restricted to low frequency operation by the lamp time constant.

R2 and R4 are chosen to minimize errors due to input offset current as outlined in the section describing the photocell amplifier. R3 is included to reduce in-rush current when first turning on the lamp, L1.

THE FULL-WAVE RECTIFIER AND AVERAGING FILTER

The circuit shown in *Figure 23* is the heart of an average reading, rms calibrated AC voltmeter. As shown, it is a rectifier and averaging filter. Deletion of C2 removes the averaging function and provides a precision full-wave rectifier, and deletion of C1 provides an absolute value generator.

Circuit operation may be understood by following the signal path for negative and then for positive inputs. For negative signals, the output of amplifier A1 is clamped to +0.7V by D1 and disconnected from the summing point of A2 by D2. A2 then functions as a simple unity-gain inverter with input resistor, R1, and feedback resistor, R2, giving a positive going output.

For positive inputs, A1 operates as a normal amplifier connected to the A2 summing point through resistor, R5. Amplifier A1 then acts as a simple unity-gain inverter with input

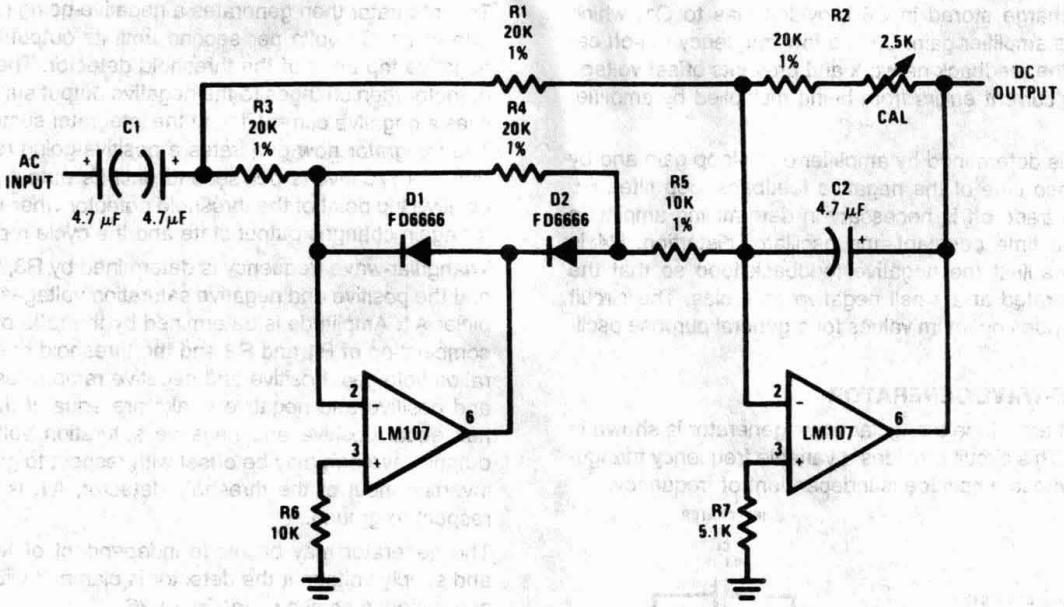

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FIGURE 23. Full-Wave Rectifier and Averaging Filter

resistor, R3, and feedback resistor, R5. A1 gain accuracy is not affected by D2 since it is inside the feedback loop. Positive current enters the A2 summing point through resistor, R1, and negative current is drawn from the A2 summing point through resistor, R5. Since the voltages across R1 and R5 are equal and opposite, and R5 is one-half the value of R1, the net input current at the A2 summing point is equal to and opposite from the current through R1 and amplifier A2 operates as a summing inverter with unity gain, again giving a positive output.

The circuit becomes an averaging filter when C2 is connected across R2. Operation of A2 then is similar to the Simple Low Pass Filter previously described. The time constant R2C2 should be chosen to be much larger than the maximum period of the input voltage which is to be averaged.

Capacitor C1 may be deleted if the circuit is to be used as an absolute value generator. When this is done, the circuit output will be the positive absolute value of the input voltage.

The amplifiers chosen must be compensated for unity-gain operation and R6 and R7 must be chosen to minimize output errors due to input offset current.

SINE WAVE OSCILLATOR

An amplitude-stabilized sine-wave oscillator is shown in *Figure 24*. This circuit provides high purity sine-wave output down to low frequencies with minimum circuit complexity. An important advantage of this circuit is that the traditional tungsten filament lamp amplitude regulator is eliminated along with its time constant and linearity problems.

In addition, the reliability problems associated with a lamp are eliminated.

The Wien Bridge oscillator is widely used and takes advantage of the fact that the phase of the voltage across the parallel branch of a series and a parallel RC network connected in series, is the same as the phase of the applied voltage across the two networks at one particular frequency and that the phase lags with increasing frequency and leads with decreasing frequency. When this network—the Wien Bridge—is used as a positive feedback element around an amplifier, oscillation occurs at the frequency at which the phase shift is zero. Additional negative feedback is provided to set loop gain to unity at the oscillation frequency, to stabilize the frequency of oscillation, and to reduce harmonic distortion.

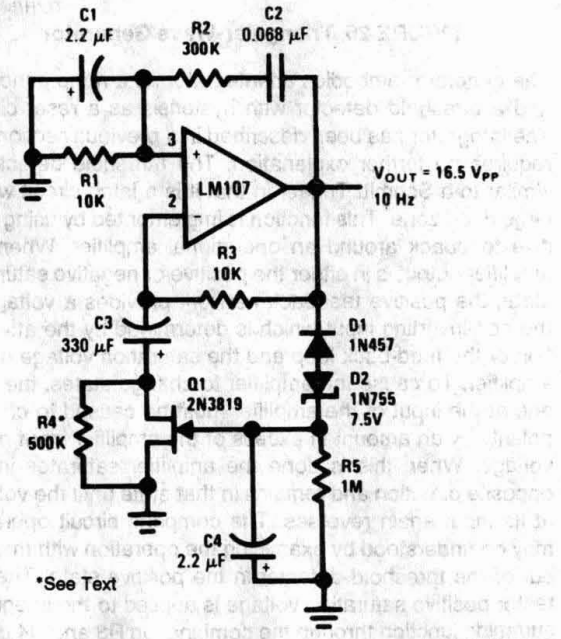

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FIGURE 24. Wien Bridge Sine Wave Oscillator

The circuit presented here differs from the classic usage only in the form of the negative feedback stabilization scheme. Circuit operation is as follows: negative peaks in excess of −8.25V cause D1 and D2 to conduct, charging

C4. The charge stored in C4 provides bias to Q1, which determines amplifier gain. C3 is a low frequency roll-off capacitor in the feedback network and prevents offset voltage and offset current errors from being multiplied by amplifier gain.

Distortion is determined by amplifier open-loop gain and by the response time of the negative feedback loop filter, R5 and C4. A trade-off is necessary in determining amplitude stabilization time constant and oscillator distortion. R4 is chosen to adjust the negative feedback loop so that the FET is operated at a small negative gate bias. The circuit shown provides optimum values for a general purpose oscillator.

TRIANGLE-WAVE GENERATOR

A constant amplitude triangular-wave generator is shown in *Figure 25*. This circuit provides a variable frequency triangular wave whose amplitude is independent of frequency.

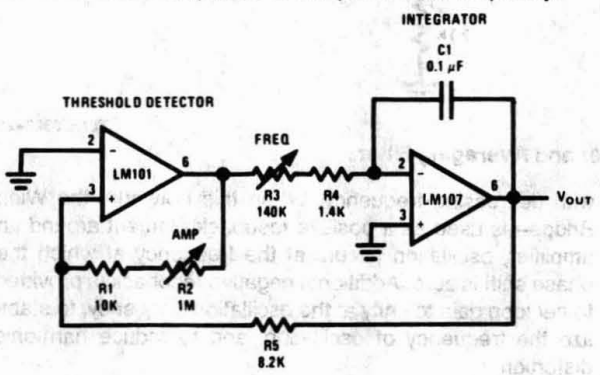

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FIGURE 25. Triangular-Wave Generator

The generator embodies an integrator as a ramp generator and a threshold detector with hysterisis as a reset circuit. The integrator has been described in a previous section and requires no further explanation. The threshold detector is similar to a Schmitt Trigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the non-inverting input which is determined by the attenuation of the feed-back loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must be caused to change polarity by an amount in excess of the amplifier input offset voltage. When this is done the amplifier saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete circuit operation may be understood by examining the operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R3 and R4 causing a current I^+ to flow.

The integrator then generates a negative-going ramp with a rate of $I^+/C1$ volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state and supplies a negative current, I^-, at the integrator summing point. The integrator now generates a positive-going ramp with a rate of $I^-/C1$ volts per second until its output equals the positive trip point of the threshold detector where the detector again changes output state and the cycle repeats.

Triangular-wave frequency is determined by R3, R4 and C1 and the positive and negative saturation voltages of the amplifier A1. Amplitude is determined by the ratio of R5 to the combination of R1 and R2 and the threshold detector saturation voltages. Positive and negative ramp rates are equal and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes as shown in *Figure 26*.

The integrator should be compensated for unity-gain and the detector may be compensated if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to I_{bias} for maximum symmetry, and offset voltage should be small with respect to V_{OUT} peak.

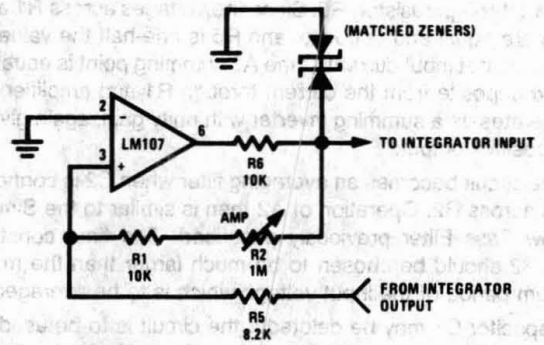

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FIGURE 26. Threshold Detector with Regulated Output

TRACKING REGULATED POWER SUPPLY

A tracking regulated power supply is shown in *Figure 27*. This supply is very suitable for powering an operational amplifier system since positive and negative voltages track, eliminating common mode signals originating in the supply voltage. In addition, only one voltage reference and a minimum number of passive components are required.

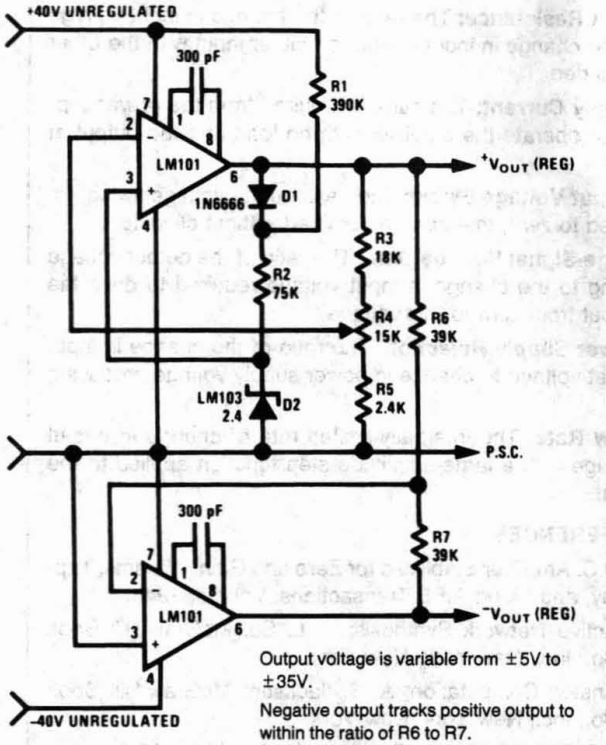


FIGURE 27. Tracking Power Supply

Power supply operation may be understood by considering first the positive regulator. The positive regulator compares the voltage at the wiper of R4 to the voltage reference, D2. The difference between these two voltages is the input voltage for the amplifier and since R3, R4, and R5 form a negative feedback loop, the amplifier output voltage changes in such a way as to minimize this difference. The voltage reference current is supplied from the amplifier output to increase power supply line regulation. This allows the regulator to operate from supplies with large ripple voltages. Regulating the reference current in this way requires a separate source of current for supply start-up. Resistor R1 and diode D1 provide this start-up current. D1 decouples the reference string from the amplifier output during start-up and R1 supplies the start-up current from the unregulated positive supply. After start-up, the low amplifier output impedance reduces reference current variations due to the current through R1.

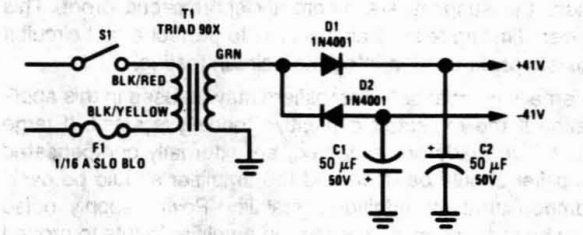
The negative regulator is simply a unity-gain inverter with input resistor, R6, and feedback resistor, R7.

The amplifiers must be compensated for unity-gain operation.

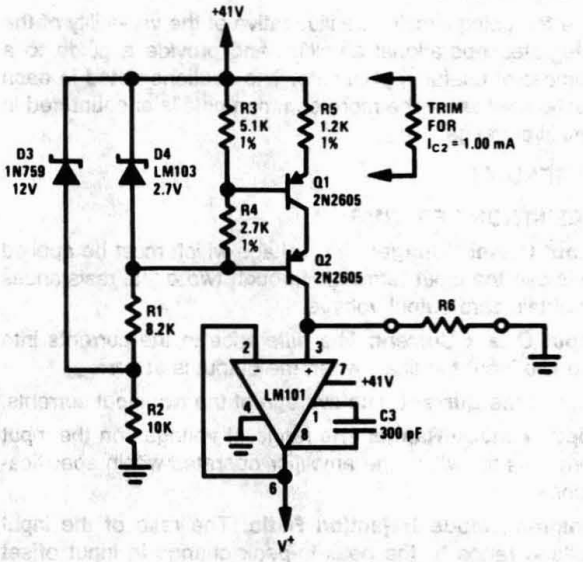
The power supply may be modulated by injecting current into the wiper of R4. In this case, the output voltage variations will be equal and opposite at the positive and negative outputs. The power supply voltage may be controlled by replacing D1, D2, R1 and R2 with a variable voltage reference.

PROGRAMMABLE BENCH POWER SUPPLY

The complete power supply shown in *Figure 28* is a programmable positive and negative power supply. The regulator section of the supply comprises two voltage followers whose input is provided by the voltage drop across a reference resistor of a precision current source.



a.



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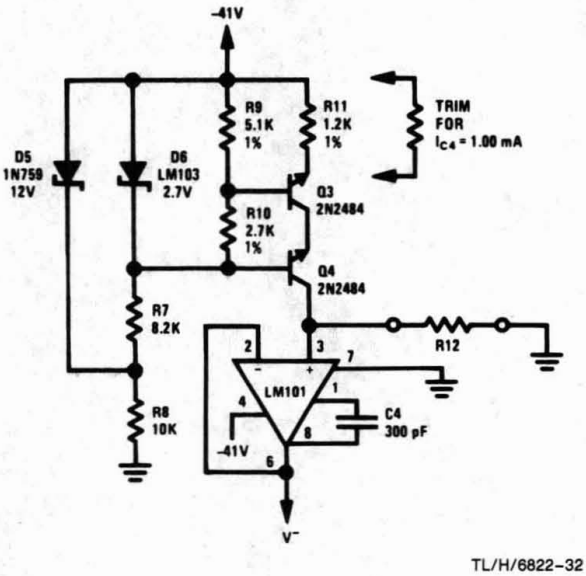
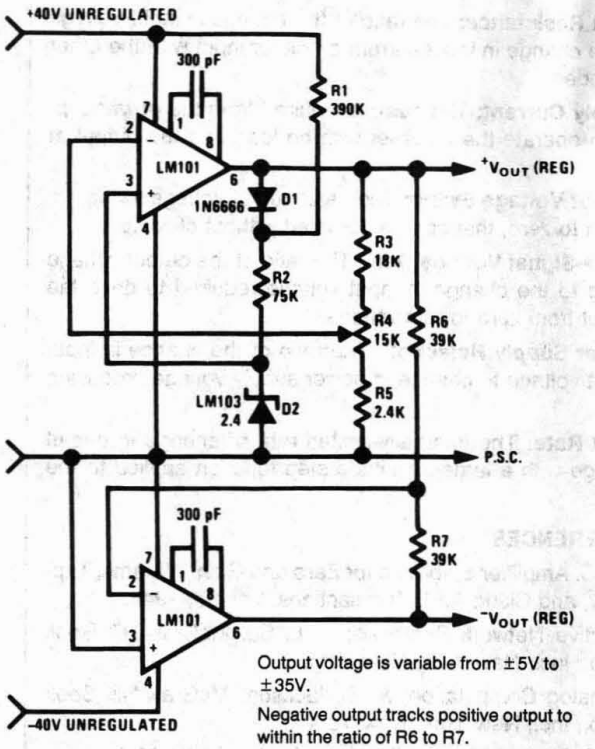


c.

FIGURE 28. Low-Power Supply for Integrated Circuit Testing



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The amplifiers must be compensated for unity-gain operation.

The power supply may be modulated by injecting current into the wiper of R4. In this case, the output voltage variations will be equal and opposite at the positive and negative outputs. The power supply voltage may be controlled by replacing D1, D2, R1 and R2 with a variable voltage reference.

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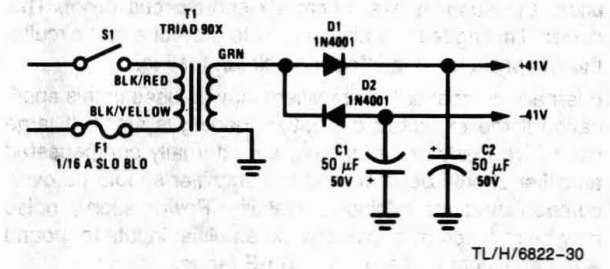

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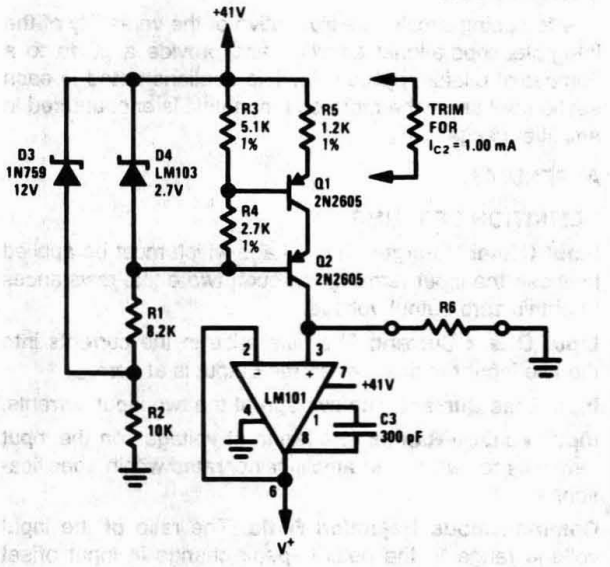

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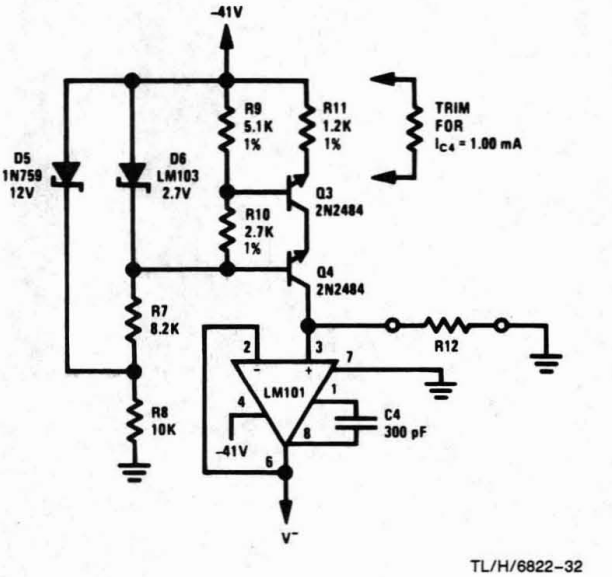

c.

FIGURE 28. Low-Power Supply for Integrated Circuit Testing

Programming sensitivity of the positive and negative supply is 1V/1000Ω of resistors R6 and R12 respectively. The output voltage of the positive regulator may be varied from approximately +2V to +38V with respect to ground and the negative regulator output voltage may be varied from −38V to 0V with respect to ground. Since LM107 amplifiers are used, the supplies are inherently short circuit proof. This current limiting feature also serves to protect a test circuit if this supply is used in integrated circuit testing.

Internally compensated amplifiers may be used in this application if the expected capacitive loading is small. If large capacitive loads are expected, an externally compensated amplifier should be used and the amplifier should be overcompensated for additional stability. Power supply noise may be reduced by bypassing the amplifier inputs to ground with capacitors in the 0.1 to 1.0 μF range.

CONCLUSIONS

The foregoing circuits are illustrative of the versatility of the integrated operational amplifier and provide a guide to a number of useful applications. The cautions noted in each section will show the more common pitfalls encountered in amplifier usage.

APPENDIX I

DEFINITION OF TERMS

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Common Mode Rejection Ratio: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection: The ratio of the change in input offset voltage to change in power supply voltage producing it.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

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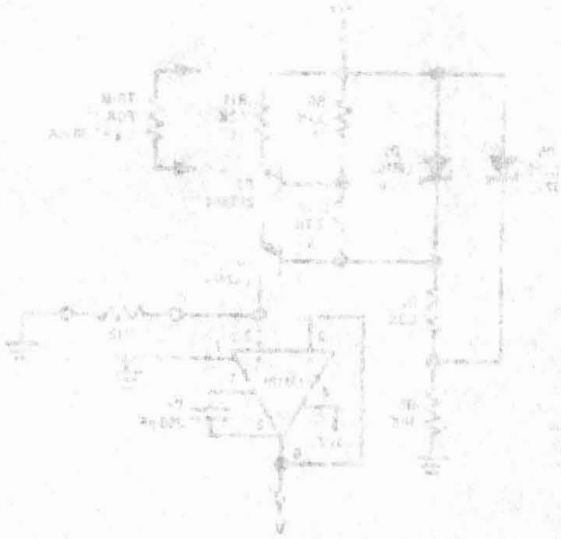

The LM105-An Improved Positive Regulator

National Semiconductor
Application Note 23

Robert J. Widlar
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Mexico

introduction

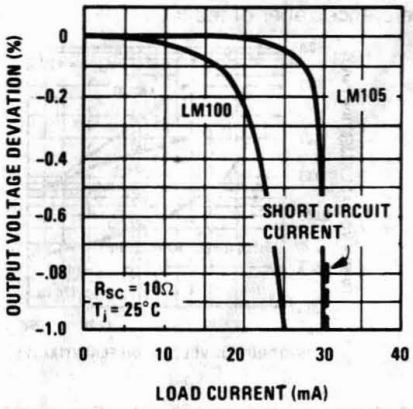
IC voltage regulators are seeing rapidly increasing usage. The LM100, one of the first, has already been widely accepted. Designed for versatility, this circuit can be used as a linear regulator, a switching regulator, a shunt regulator, or even a current regulator. The output voltage can be set between 2V and 30V with a pair of external resistors, and it works with unregulated input voltages down to 7V. Dissipation limitations of the IC package restrict the output current to less than 20 mA, but external transistors can be added to obtain output currents in excess of 5A. The LM100 and an extensive description of its use in many practical circuits are described in References 1–3.

One complaint about the LM100 has been that it does not have good enough regulation for certain applications. In addition, it becomes difficult to prove that the load regulation is satisfactory under worst-case design conditions. These problems prompted development of the LM105, which is nearly identical to the LM100 except that a gain stage has been added for improved regulation. In the great majority of applications, the LM105 is a plug-in replacement for the LM100.

the improved regulator

The load regulation of the LM100 is about 0.1%, no load to full load, without current limiting. When short circuit protection is added, the regulation begins to degrade as the output current becomes greater than about half the limiting current. This is illustrated in *Figure 1*. The LM105, on the other hand, gives 0.1% regulation up to currents closely approaching the short circuit current. As shown in *Figure 1b*, this is particularly significant at high temperatures.

The current limiting characteristics of a regulator are important for two reasons: First, it is almost mandatory that a regulator be short-circuit protected because the output is distributed to enough places that the probability of it becoming shorted is quite high, Secondly, the sharpness of the limiting characteristics is not improved by the addition of external booster transistors. External transistors can increase the maximum output current, but they do not improve the load regulation at currents approaching the short



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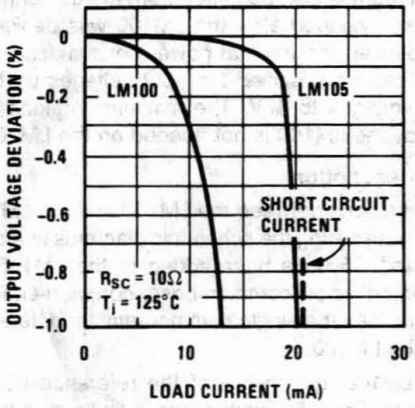
a. T_j = 25°C



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b. T_j = 125°C

Figure 1. Comparison between the load regulation of the LM100 and LM105 for equal short circuit currents

circuit current. Thus, it can be seen that the LM105 provides more than ten times better load regulation in practical power supply designs.

Figure 2 shows that the LM105 also provides better line regulation than the LM100. These curves give the percentage change in output voltage for an incremental change in the unregulated input voltage. They show that the line regulation is worst for small differences between the input and output voltages. The LM105 provides about three times better regulation under worst case conditions. Bypassing the internal reference of the regulator makes the ripple rejection of the LM105 almost a factor of ten better than the LM100 over the entire operating range, as shown in the figure. This bypass capacitor also eliminates noise generated in the internal reference zener of the IC.

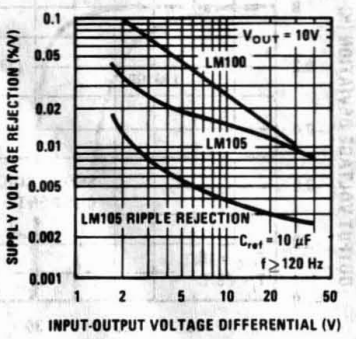

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Figure 2. Comparison between the line regulation characteristics of the LM100 and LM105

The LM105 has also benefited from the use of new IC components developed after the LM100 was designed. These have reduced the internal power consumption so that the LM105 can be specified for input voltages up to 50V and output voltages to 40V. The minimum preload current required by the LM100 is not needed on the LM105.

circuit description

The differences between the LM100 and the LM105 can be seen by comparing the schematic diagrams in *Figures 3* and *4*. Q4 and Q5 have been added to the LM105 to form a common-collector, common-base, common-emitter amplifier, rather than the single common-emitter differential amplifier of the LM100.

In the LM100, generation of the reference voltage starts with zener diode, D1, which is supplied with a fixed current from one of the collectors of Q2. This regulated voltage, which has a positive temperature coefficient, is buffered by

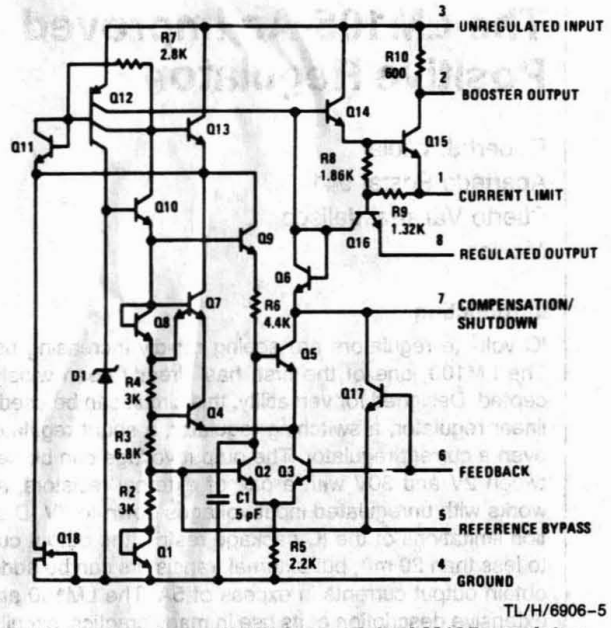

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Figure 4. Schematic diagram of the LM105 regulator

Q4, divided down by R1 and R2 and connected in series with a diode-connected transistor, Q7. The negative temperature coefficient of Q7 cancels out the positive coefficient of the voltage across R2, producing a temperature-compensated 1.8V on the base of Q8. This point is also brought outside the circuit so that an external capacitor can be added to bypass any noise from the zener diode.

Transistors Q8 and Q9 make up the error amplifier of the circuit. A gain of 2000 is obtained from this single stage by using a current source, another collector on Q2, as a collector load. The output of the amplifier is buffered by Q11 and used to drive the series-pass transistor, Q12. The collector of Q12 is brought out so that an external PNP transistor, or PNP—NPN combination, can be added for increased output current.

Current limiting is provided by Q10. When the voltage across an external resistor connected between Pins 1 and 8 becomes high enough to turn on Q10, it removes the base drive from Q11 so the regulator exhibits a constant-current characteristic. Prebiasing the current limit transistor with a portion of the emitter-base voltage of Q12 from R6 and R7 reduces the current limit sense voltage. This increases the

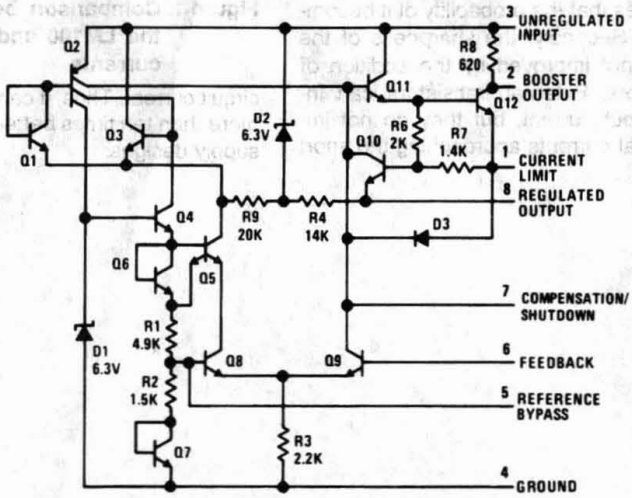

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Figure 3. Schematic diagram of the LM100 regulator

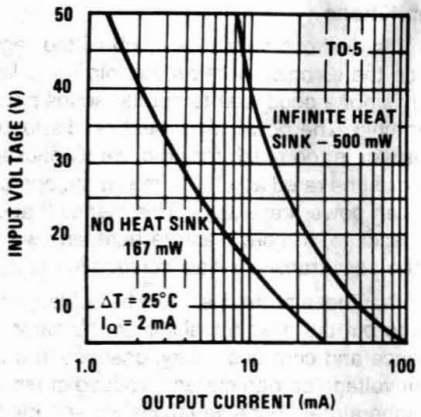

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Figure 5. Dissipation limited short circuit output current for an IC regulator in a TO-5 package

The 25°C temperature rise assumed in arriving at *Figure 5* is not at all unreasonable. With military temperature range parts, this is valid for a maximum junction temperature of 150°C with a 125°C ambient. For low cost parts, marketed for limited temperature range applications, this maximum differential appropriately derates the maximum junction temperature.

In practical designs, the maximum permissible dissipation will always be to the left of the curve shown for an infinite heat sink in *Figure 5*. This curve is realized with the package immersed in circulating acetone, freon or mineral oil. Most heat sinks are not quite as good.

To summarize, power transistors can be run with a temperature differential, junction to ambient, 3 to 5 times as great as an integrated circuit. This means that they can dissipate much more power, even with a smaller heat sink. This, coupled with the fact that low cost, multilead power packages are not available and that there can be thermal interactions between the control circuitry and the pass transistor, strongly suggests that the pass transistors be kept separate from the integrated circuit.

using booster transistors

Figure 6 shows how an external pass transistor is added to the LM105. The addition of an external PNP transistor does not increase the minimum input output voltage differential.

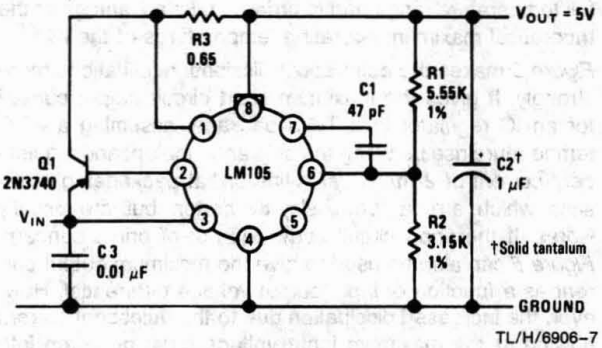

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Figure 6. 0.2A regulator

This would happen if an NPN transistor was used in a compound emitter follower connection with the NPN output transistor of the IC. A single-diffused, wide base transistor like the 2N3740 is recommended because it causes fewer oscillation problems than double-diffused, planar devices. In addition, it seems to be less prone to failure under overload conditions; and low cost devices are available in power packages like the TO-66 or even TO-3.

When the maximum dissipation in the pass transistor is less than about 0.5W, a 2N2905 may be used as a pass transistor. However, it is generally necessary to carefully observe thermal deratings and provide some sort of heat sink.

In the circuit of *Figure 6*, the output voltage is determined by R1 and R2. The resistor values are selected based on a feedback voltage of 1.8V to Pin 6 of the LM105. To keep thermal drift of the output voltage within specifications, the parallel combination of R1 and R2 should be approximately 2K. However, this resistance is not critical. Variations of ±30% will not cause an appreciable degradation of temperature drift.

The 1 μF output capacitor, C2, is required to suppress oscillations in the feedback loop involving the external booster transistor, Q1, and the output transistor of the LM105. C1 compensates the internal regulator circuitry to make the stability independent for all loading conditions. C3 is not normally required if the lead length between the regulator and the output filter of the rectifier is short.

Current limiting is provided by R3. The current limit resistor should be selected so that the maximum voltage drop across it, at full load current, is equal to the voltage given in *Figure 7* at the maximum junction temperature of the IC. This assures a no load to full load regulation better than 0.1% under worst-case conditions.

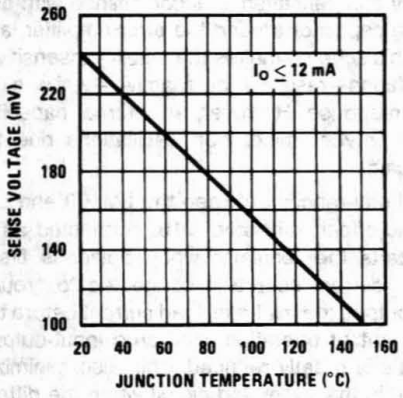

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Figure 7. Maximum voltage drop across current limit resistor at full load for worst case load regulation of 0.1%

The short circuit output current is also determined by R3. *Figure 8* shows the voltage drop across this resistor, when the output is shorted, as a function of junction temperature in the IC.

With the type of current limiting used in *Figure 6*, the dissipation under short circuit conditions can be more than three times the worst-case full load dissipation. Hence, the heat

efficiency of the regulator, especially when foldback current limiting is used. With foldback limiting, the voltage dropped across the current sense resistor is about four times larger than the sense voltage.

As for the remaining details, the collector of the amplifier, Q9, is brought out so that external collector-base capacitance can be added to frequency-stabilize the circuit when it is used as a linear regulator. This terminal can also be grounded to shut the regulator off. R9 and R4 are used to start up the regulator, while the rest of the circuitry establishes the proper operating levels for the current source transistor, Q2.

The reference circuitry of the LM105 is the same, except that the current through the reference divider, R2, R3 and R4, has been reduced by a factor of two on the LM105 for reduced power consumption. In the LM105, Q2 and Q3 form an emitter coupled amplifier, with Q3 being the emitter-follower input and Q2 the common-base output amplifier. R6 is the collector load for this stage, which has a voltage gain of about 20. The second stage is a differential amplifier, using Q4 and Q5. Q5 actually provides the gain. Since it has a current source as a collector load, one of the collectors of Q12, the gain is quite high: about 1500. This gives a total gain in the error amplifier of about 30,000 which is ten times higher than the LM100.

It is not obvious from the schematic, but the first stage (Q2 and Q3) and second stage (Q4 and Q5) of the error amplifier are closely balanced when the circuit is operating. This will be true regardless of the absolute value of components and over the operating temperature range. The only thing affecting balance is component matching, which is good in a monolithic integrated circuit, so the error amplifier has good drift characteristics over a wide temperature range.

Frequency compensation is accomplished with an external integrating capacitor around the error amplifier, as with the LM100. This scheme makes the stability insensitive to loading conditions—resistive or reactive—while giving good transient response. However, an internal capacitor, C1, is added to prevent minor-loop oscillations due to the increased gain.

Additional differences between the LM100 and LM105 are that a field-effect transistor, Q18, connected as a current source starts the regulator when power is first applied. Since this current source is connected to ground, rather than the output, the minimum load current before the regulator drops out of operation with large input-output voltage differentials is greatly reduced. This also minimizes power dissipation in the integrated circuit when the difference between the input and output voltage is at the worst-case value. With the LM105 circuit configuration, it was also necessary to add Q17 to eliminate a latch-up mechanism which could exist with lower output-voltage settings. Without Q17, this could occur when Q3 saturated and cut off the second stage amplifiers, Q4 and Q5, causing the output to latch at a voltage nearly equal to the unregulated input.

power limitations

Although it is desirous to put as much of the regulator as possible on the IC chip, there are certain basic limitations. For one, it is not a good idea to put the series pass transistor on the chip. The power that must be dissipated in the pass transistor is too much for practical IC packages. Further, IC's must be rated at a lower maximum operating temperature than power transistors. This means that even with a power package, a more massive heat sink would be required if the pass transistor was included in the IC.

Assuming that these problems could be solved, it is still not advisable to put the pass transistor on the same chip with the reference and control circuitry: changes in the unregulated input voltage or load current produce gross variations in chip temperature. These variations worsen load and line regulation due to temperature interaction with the control and reference circuitry.

To elaborate, it is reasonable to neglect the package problem since it is potentially solvable. The lower, maximum operating temperatures of IC's, however, present a more basic problem. The control circuitry in an IC regulator runs at fairly low currents. As a result, it is more sensitive to leakage currents and other phenomena which degrades the performance of semiconductors at high temperatures. Hence, the maximum operating temperature is limited to 150°C in military temperature range applications. On the other hand, a power transistor operating at high currents may be run at temperatures up to 200°C, because even a 1 mA leakage current would not affect its operation in a properly designed circuit. Even if the pass transistor developed a permanent 1 mA leakage from channeling, operating under these conditions of high stress, it would not affect circuit operation. These conditions would not trouble the pass transistor, but they would most certainly cause complete failure of the control circuitry.

These problems are not eliminated in applications with a lower maximum operating temperature. Integrated circuits are sold for limited temperature range applications at considerably lower cost. This is mainly based on a lower maximum junction temperature. They may be rated so that they do not blow up at higher temperatures, but they are not guaranteed to operate within specifications at these temperatures. Therefore, in applications with a lower maximum ambient temperature, it is necessary to purchase an expensive full temperature range part in order to take advantage of the theoretical maximum operating temperatures of the IC.

Figure 5 makes the point about dissipation limitations more strongly. It gives the maximum short circuit output current for an IC regulator in a TO-5 package, assuming a 25°C temperature rise between the chip and ambient and a quiescent current of 2 mA. Dual-in-line or flat packages give results which are, at best, slightly better, but are usually worse. If the short circuit current is not of prime concern, *Figure 5* can also be used to give the maximum output current as a function of input-output voltage differential, However, the increased dissipation due to the quiescent current flowing at the maximum input voltage must be taken into account. In addition, the input-output differential must be measured with the maximum expected input voltages.

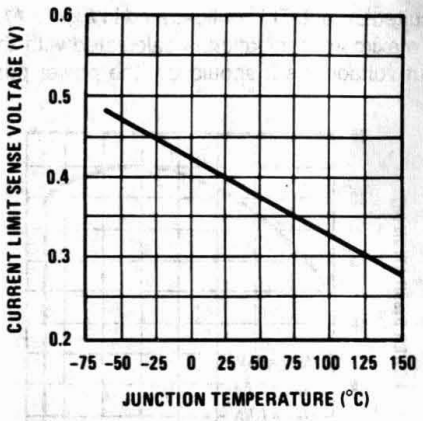

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Figure 8. Voltage drop across current limit resistor required to initiate current limiting

sink for the pass transistor must be designed to accommodate the increased dissipation if the regulator is to survive more than momentarily with a shorted output. It is encouraging to note, however, that the short circuit current will decrease at higher ambient temperatures. This assists in protecting the pass transistor from excessive heating.

foldback current limiting

With high current regulators, the heat sink for the pass transistor must be made quite large in order to handle the power dissipated under worst-case conditions. Making it more than three times larger to withstand short circuits is sometimes inconvenient in the extreme. This problem can be solved with foldback current limiting, which makes the output current under overload conditions decrease below the full load current as the output voltage is pulled down. The short circuit current can be made but a fraction of the full load current.

A high current regulator using foldback limiting is shown in *Figure 9*. A second booster transistor, Q1, has been added to provide 2A output current without causing excessive dissipation in the LM105. The resistor across its emitter base junction bleeds off any collector base leakage and establishes a minimum collector current for Q2 to make the circuit easier to stabilize with light loads. The foldback characteristic is produced with R4 and R5. The voltage across R4 bucks out the voltage dropped across the current sense resistor, R3. Therefore, more voltage must be developed across R3 before current limiting is initiated. After the output voltage begins to fall, the bucking voltage is reduced, as it is proportional to the output voltage. With the output shorted, the current is reduced to a value determined by the current limit resistor and the current limit sense voltage of the LM105.

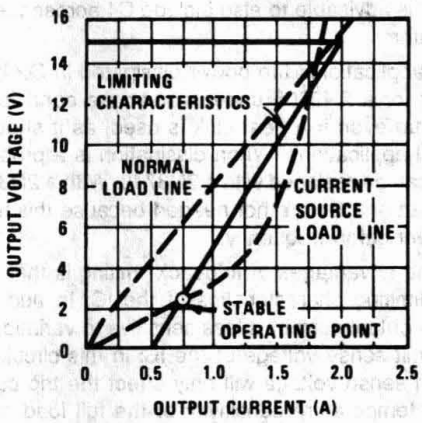

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Figure 10. Limiting characteristics of regulator using foldback current limiting

Figure 10 illustrates the limiting characteristics. The circuit regulates for load currents up to 2A. Heavier loads will cause the output voltage to drop, reducing the available current. With a short on the output, the current is only 0.5A.

In design, the value of R3 is determined from

$$R_3 = \frac{V_{lim}}{I_{SC}}, \quad (1)$$

where V_{lim} is the current limit sense voltage of the LM105, given in *Figure 8*, and I_{SC} is the design value of short circuit current. R5 is then obtained from

$$R_5 = \frac{V_{OUT} + V_{sense}}{I_{bleed} + I_{bias}}, \quad (2)$$

where V_{OUT} is the regulated output voltage, V_{sense} is maximum voltage across the current limit resistor for 0.1% regulation as indicated in *Figure 7*, I_{bleed} is the preload current on the regulator output provided by R5 and I_{bias} is the maximum current coming out of Pin 1 of the LM105 under full load conditions. I_{bias} will be equal to 2 mA plus the worst-case base drive for the PNP booster transistor, Q2. I_{bleed} should be made about ten times greater than I_{bias}.

Finally, R4 is given by

$$R_4 = \frac{I_{FL} R_3 - V_{sense}}{I_{bleed}}, \quad (3)$$

where I_{FL} is the output current of the regulator at full load.

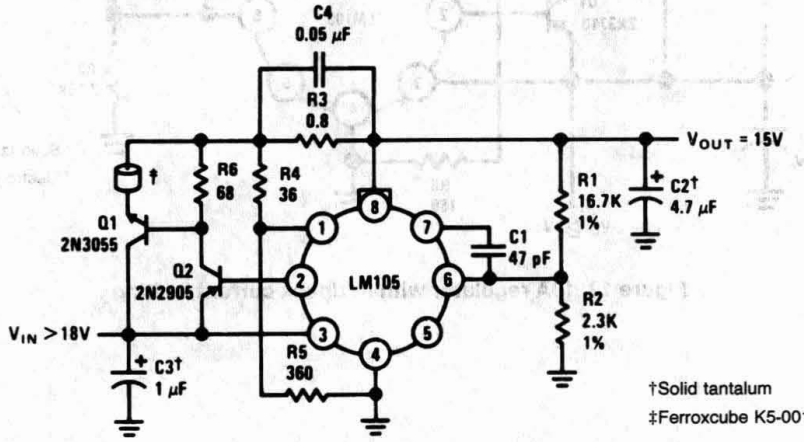

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Figure 9. 2A regulator with foldback current limiting

It is recommended that a ferrite bead be strung on the emitter of the pass transistor, as shown in *Figure 9*, to suppress oscillations that may show up with certain physical configurations. It is advisable to also include C4 across the current limit resistor.

In some applications, the power dissipated in Q2 becomes too great for a 2N2905 under worst-case conditions. This can be true even if a heat sink is used, as it should be in almost all applications. When dissipation is a problem, the 2N2905 can be replaced with a 2N3740. With a 2N3740, the ferrite bead and C4 are not needed because this transistor has a lower cutoff frequency.

One of the advantages of foldback limiting is that it sharpens the limiting characteristics of the IC. In addition, the maximum output current is less sensitive to variations in the current limit sense voltage of the IC: in this circuit, a 20% change in sense voltage will only affect the trip current by 5%. The temperature sensitivity of the full load current is likewise reduced by a factor of four, while the short circuit current is not.

Even though the voltage dropped across the sense resistor is larger with foldback limiting, the minimum input-output voltage differential of the complete regulator is not increased above the 3V specified for the LM105 as long as this drop is less than 2V. This can be attributed to the low sense voltage of the IC by itself.

Figure 10 shows that foldback limiting can only be used with certain kinds of loads. When the load looks predominately like a current source, the load line can intersect the foldback characteristic at a point where it will prevent the regulator from coming up to voltage, even without an overload. Fortunately, most solid state circuitry presents a load line which does not intersect. However, the possibility cannot be ignored, and the regulator must be designed with some knowledge of the load.

With foldback limiting, power dissipation in the pass transistor reaches a maximum at some point between full load and short circuited output. This is illustrated in *Figure 11*. However, if the maximum dissipation is calculated with the worst-case input voltage, as it should be, the power peak is not too high.

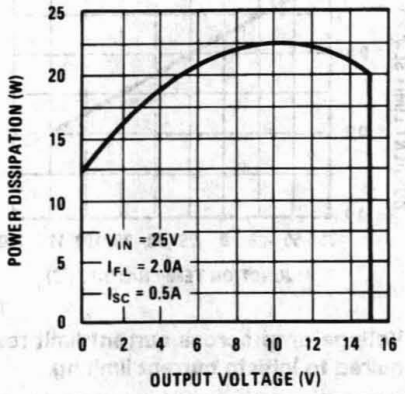

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Figure 11. Power dissipation in series pass transistors under overload conditions in regulator using foldback current limiting

high current regulator

The output current of a regulator using the LM105 as a control element can be increased to any desired level by adding more booster transistors, increasing the effective current gain of the pass transistors. A circuit for a 10A regulator is shown in *Figure 12*. A third NPN transistor has been included to get higher current. A low frequency device is used for Q3 because it seems to better withstand abuse. However, high frequency transistors must be used to drive it. Q2 and Q3 are both double-diffused transistors with good frequency response. This insures that Q3 will present the dominant lag in the feedback loop through the booster transistors, and back around the output transistor of the LM105. This is further insured by the addition of C3.

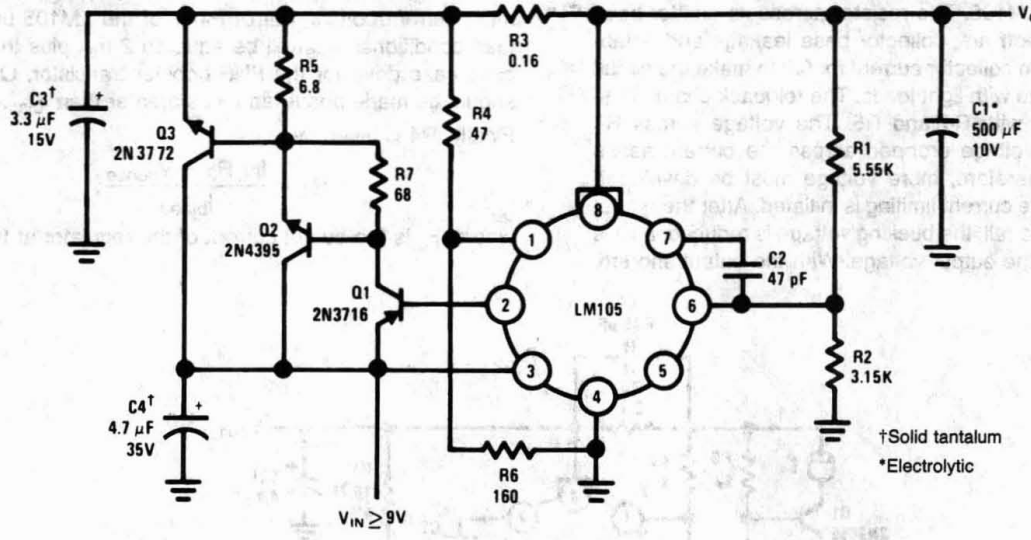

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Figure 12. 10A regulator with foldback current limiting

The circuit, as shown, has a full load capability of 10A. Foldback limiting is used to give a short circuit output current of 2.5A. The addition of Q3 increases the minimum input-output voltage differential, by 1V, to 4V.

dominant failure mechanisms

By far, the biggest reason for regulator failures is overdissipation in the series pass transistors. This has been borne out by experience with the LM100. Excessive heating in the pass transistors causes them to short out, destroying the IC. This has happened most frequently when PNP booster transistors in a TO-5 can, like the 2N2905, were used. Even with a good heat sink, these transistors cannot dissipate much more than 1W. The maximum dissipation is less in many applications. When a single PNP booster is used and power can be a problem, it is best to go to a transistor like the 2N3740, in a TO-66 power package, using a good heat sink.

Using a compound PNP/NPN booster does not solve all problems. Even when breadboarding with transistors in TO-3 power packages, heat sinks must be used. The TO-3 package is not very good, thermally, without a heat sink. Dissipation in the PNP transistor driving the NPN series pass transistor cannot be ignored either. Dissipation in the driver with worst-case current gain in the pass transistor must be taken into account. In certain cases, this could require that a PNP transistor in a power package be used to drive the NPN pass transistor. In almost all cases, a heat sink is required if a PNP driver transistor in a TO-5 package is selected.

With output currents above 3A, it is good practice to replace a 2N3055 pass transistor with a 2N3772. The 2N3055 is rated for higher currents than 3A, but its current gain falls off rapidly. This is especially true at either high temperatures or low input-output voltage differentials. A 2N3772 will give substantially better performance at high currents, and it makes life much easier for the PNP driver.

The second biggest cause of failures has been the output filter capacitors on power inverters providing unregulated power to the regulator. If these capacitors are operated with excessive ripple across them, and simultaneously near their maximum dc voltage rating, they will sputter. That is, they short momentarily and clear themselves. When they short, the output capacitor of the regulator is discharged back through the reverse biased pass transistors or the control circuitry, frequently causing destruction. This phenomenon is especially prevalent when solid tantalum capacitors are used with high-frequency power inverters. The maximum ripple allowed on these capacitors decreases linearly with frequency.

The solution to this problem is to use capacitors with conservative voltage ratings. In addition, the maximum ripple allowed by the manufacturer at the operating frequency should also be observed.

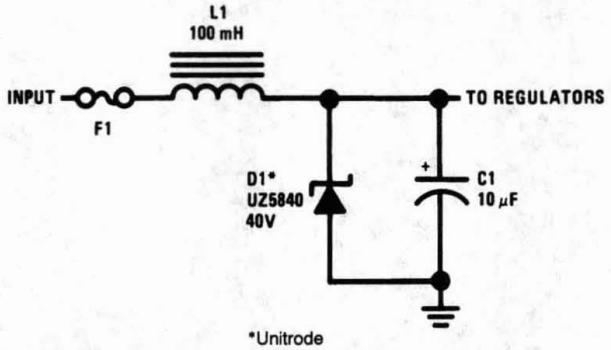
The problem can be eliminated completely by installing a diode between the input and output of the regulator such that the capacitor on the output is discharged through this diode if the input is shorted. A fast switching diode should be used as ordinary rectifier diodes are not always effective.

Another cause of problems with regulators is severe voltage transients on the unregulated input. Even if these transients do not cause immediate failure in the regulator, they can feed through and destroy the load. If the load shorts out, as is frequently the case, the regulator can be destroyed by subsequent transients.

This problem can be solved by specifying all parts of the regulator to withstand the transient conditions. However, when ultimate reliability is needed, this is not a good solution. Especially since the regulator can withstand the transient, yet severely overstress the circuitry on its output by feeding the transients through. Hence, a more logical recourse is to include circuitry which suppresses the transients. A method of doing this is shown in *Figure 13*. A zener diode, which can handle large peak currents, clamps the input voltage to the regulator while an inductor limits the current through the zener during the transient. The size of the inductor is determined from

$$L = \frac{\Delta V \Delta t}{I} \qquad (4)$$

where ΔV is the voltage by which the input transient exceeds the breakdown voltage of the diode, Δt is the duration of the transient and I is the peak current the zener can handle while still clamping the input voltage to the regulator. As shown, the suppression circuit will clamp 70V, 4 ms transients on the unregulated supply.



*Unitrode

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Figure 13. Suppression circuitry to remove large voltage spikes from unregulated supplies

conclusions

The LM105 is an exact replacement for the LM100 in the majority of applications, providing about ten times better regulation. There are, however, a few differences:

In switching regulator applications,[2] the size of the resistor used to provide positive feedback should be doubled as the impedance seen looking back into the reference bypass terminal is twice that of the LM100 (2 kΩ versus 1 kΩ). In addition, the minimum output voltage of the LM105 is 4.5V, compared with 2V for the LM100. In low voltage regulator applications, the effect of this is obvious. However, it also imposes some limitations on current regulator and shunt regulator designs.[3] Lastly, clamping the compensation terminal (Pin 7) within a diode drop of ground or the output terminal will not guarantee that the regulator is shut off, as it will with the LM100. This restricts the LM105 in the overload shutoff schemes[3] which can be used with the LM100.

Dissipation limitations of practical packages dictate that the output current of an IC regulator be less than 20 mA. However, external booster transistors can be added to get any output current desired. Even with satisfactory packages, considerably larger heat sinks would be needed if the pass transistors were put on the same chip as the reference and control circuitry, because an IC must be run at a lower maximum temperature than a power transistor. In addition, heat dissipated in the pass transistor couples into the low level circuitry and degrades performance. All this suggests that the pass transistor be kept separate from the IC.

Overstressing series pass transistors has been the biggest cause of failures with IC regulators. This not only applies to the transistors within the IC, but also to the external booster transistors. Hence, in designing a regulator, it is of utmost importance to determine the worst-case power dissipation in all the driver and pass transistors. Devices must then be selected which can handle the power. Further, adequate heat sinks must be provided as even power transistors cannot dissipate much power by themselves.

Normally, the highest power dissipation occurs when the output of the regulator is shorted. If this condition requires heat sinks which are so large as to be impractical, foldback current limiting can be used. With foldback limiting, the power dissipated under short circuit conditions can actually be made less than the dissipation at full load.

The LM105 is designed primarily as a positive voltage regulator. A negative regulator, the LM104, which is a functional complement to the LM105, is described in Reference 4.

references

1. R. J. Widlar, "A Versatile, Monolithic Voltage Regulator", *National Semiconductor AN-1*, February, 1967.
2. R. J. Widlar, "Designing Switching Regulators," *National Semiconductor AN-2*, April, 1967.
3. R. J. Widlar, "New Uses for the LM100 Regulator," *National Semiconductor AN-8*, June, 1968.
4. R. J. Widlar, "Designs for Negative Voltage Regulators," *National Semiconductor AN-21*, October, 1968.

A Simplified Test Set for Op Amp Characterization

National Semiconductor
Application Note 24
M. Yamatake

INTRODUCTION

The test set described in this paper allows complete quantitative characterization of all dc operational amplifier parameters quickly and with a minimum of additional equipment. The method used is accurate and is equally suitable for laboratory or production test—for quantitative readout or for limit testing. As embodied here, the test set is conditioned for testing the LM709 and LM101 amplifiers; however, simple changes discussed in the text will allow testing of any of the generally available operational amplifiers.

Amplifier parameters are tested over the full range of common mode and power supply voltages with either of two output loads. Test set sensitivity and stability are adequate for testing all presently available integrated amplifiers.

The paper will be divided into two sections, i.e., a functional description, and a discussion of circuit operation. Complete construction information will be given including a layout for the tester circuit boards.

FUNCTIONAL DESCRIPTION

The test set operates in one of three basic modes. These are: (1) Bias Current Test; (2) Offset Voltage, Offset Current Test; and (3) Transfer Function Test. In the first two of these tests, the amplifier under test is exercised throughout its full common mode range. In all three tests, power supply voltages for the circuit under test may be set at ±5V, ±10V, ±15V, or ±20V.

POWER SUPPLY

Basic waveforms and dc operating voltages for the test set are derived from a power supply section comprising a positive and a negative rectifier and filter, a test set voltage regulator, a test circuit voltage regulator, and a function generator. The dc supplies will be discussed in the section dealing with detailed circuit description.

The waveform generator provides three output functions, a ±19V square wave, a −19V to +19V pulse with a 1% duty cycle, and a ±5V triangular wave. The square wave is the basic waveform from which both the pulse and triangular wave outputs are derived.

The square wave generator is an operational amplifier connected as an astable multivibrator. This amplifier provides an output of approximately ±19V at 16 Hz. This square wave is used to drive junction FET switches in the test set and to generate the pulse and triangular waveforms.

The pulse generator is a monostable multivibrator driven by the output of the square wave generator. This multivibrator is allowed to swing from negative saturation to positive saturation on the positive going edge of the square wave input and has a time constant which will provide a duty cycle of approximately 1%. The output is approximately −19V to +19V.

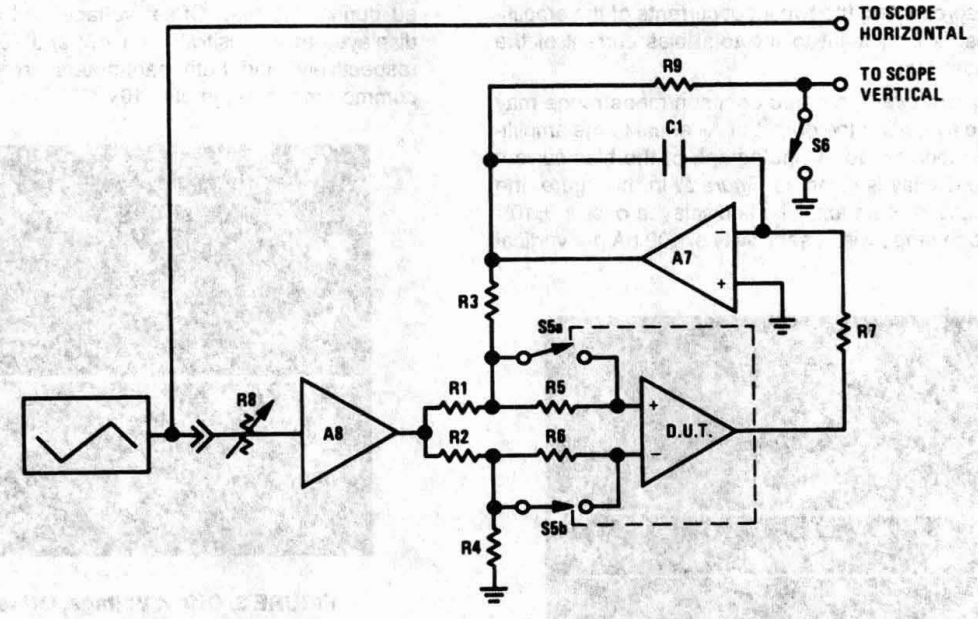

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FIGURE 1. Functional Diagram of Bias Current Test Circuit

The triangular wave generator is a dc stabilized integrator driven by the output of the square wave generator and provides a ±5V output at the square wave frequency, inverted with respect to the square wave.

The purpose of these various outputs from the power supply section will be discussed in the functional description.

BIAS CURRENT TEST

A functional diagram of the bias current test circuit is shown in *Figure 1*. The output of the triangular wave generator and the output of the test circuit, respectively, drive the horizontal and vertical deflection of an oscilloscope.

The device under test, (cascaded with the integrator, A_7), is connected in a differential amplifier configuration by R_1, R_2, R_3, and R_4. The inputs of this differential amplifier are driven in common from the output of the triangular wave generator through attenuator R_8 and amplifier A_8. The inputs of the device under test are connected to the feedback network through resistors R_5 and R_6, shunted by the switch S_{5a} and S_{5b}.

The feedback network provides a closed loop gain of 1,000 and the integrator time constant serves to reduce noise at the output of the test circuit as well as allowing the output of the device under test to remain near zero volts.

The bias current test is accomplished by allowing the device under test to draw input current to one of its inputs through the corresponding input resistor on positive going or negative going halves of the triangular wave generator output. This is accomplished by closing S_{5a} or S_{5b} on alternate halves of the triangular wave input. The voltage appearing across the input resistor is equal to input current times the input resistor. This voltage is multiplied by 1,000 by the feedback loop and appears at the integrator output and the vertical input of the oscilloscope. The vertical separaton of the traces representing the two input currents of the amplifier under test is equivalent to the total bias current of the amplifier under test.

The bias current over the entire common mode range may be examined by setting the output of A_8 equal to the amplifier common mode range. A photograph of the bias current oscilloscope display is given as *Figure 2*. In this figure, the total input current of an amplifier is displayed over a ±10V common mode range with a sensitivity of 100 nA per vertical division.

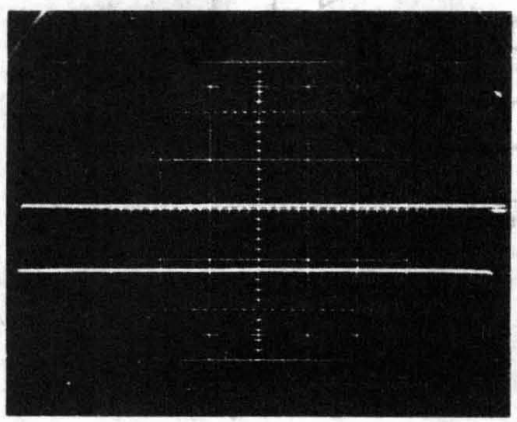

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FIGURE 2. Bias Current and Common Mode Rejection Display

The bias current display of *Figure 2* has the added advantage that incipient breakdown of the input stage of the device under test at the extremes of the common mode range is easily detected.

If either or both the upper or lower trace in the bias current display exhibits curvature near the horizontal ends of the oscilloscope face, then the bias current of that input of the amplifier is shown to be dependent on common mode voltage. The usual causes of this dependency are low breakdown voltage of the differential input stage or current sink.

OFFSET VOLTAGE, OFFSET CURRENT TEST

The offset voltage and offset current tests are performed in the same general way as the bias current test. The only difference is that the switches S_{5a} and S_{5b} are closed on the same half-cycle of the triangular wave input.

The synchronous operation of S_{5a} and S_{5b} forces the amplifier under test to draw its input currents through matched high and low input resistors on alternate halves of the input triangular wave. The difference between the voltage drop across the two values of input resistors is proportional to the difference in input current to the two inputs of the amplifier under test and may be measured as the vertical spacing between the two traces appearing on the face of the oscilloscope.

Offset voltage is measured as the vertical spacing between the trace corresponding to one of the two values of source resistance and the zero volt baseline. Switch S_6 and Resistor R_9 are a base line chopper whose purpose is to provide a baseline reference which is independent of test set and oscilloscope drift. S_6 is driven from the pulse output of the function generator and has a duty cycle of approximately 1% of the triangular wave.

Figure 3 is a photograph of the various waveforms presented during this test. Offset voltage and offset current are displayed at a sensitivity of 1 mV and 100 nA per division, respectively, and both parameters are displayed over a common mode range of ±10V.

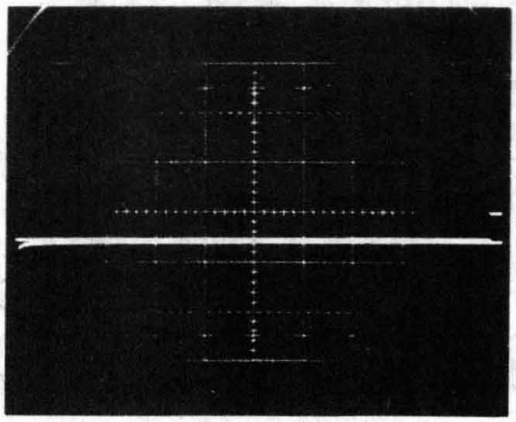

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FIGURE 3. Offset Voltage, Offset Current and Common Mode Rejection Display

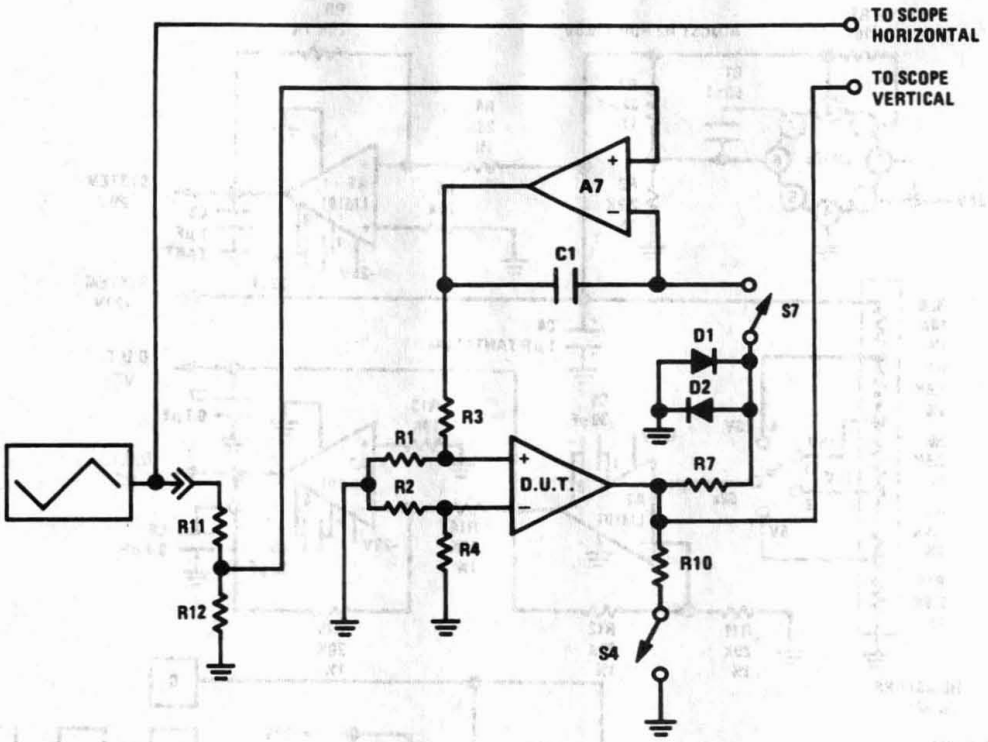

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FIGURE 4. Functional Diagram of Transfer Function Circuit

TRANSFER FUNCTION TEST

A functional diagram of the transfer function test is shown in *Figure 4*. The output of the triangular wave generator and the output of the circuit under test, respectively, drive the horizontal and vertical inputs of an oscilloscope.

The device under test is driven by a ±2.5 mV triangular wave derived from the ±5V output of the triangular wave generator through the attenuators R_{11}, R_{12}, and R_1, R_3 and through the voltage follower, A_7. The output of the device under test is fed to the vertical input of an oscilloscope.

Amplifier A_7 performs a dual function in this test. When S_7 is closed during the bias current test, a voltage is developed across C_1 equal to the amplifier offset voltage multiplied by the gain of the feedback loop. When S_7 is opened in the transfer function test, the charge stored in C_1 continues to provide this offset correction voltage. In addition, A_7 sums the triangular wave test signal with the offset correction voltage and applies this sum to the input of the amplifier under test through the attenuator R_1, R_3. This input sweeps the input of the amplifier under test ±2.5 mV around its offset voltage.

Figure 5 is a photograph of the output of the test set during the transfer function test. This figure illustrates the function of amplifier A_7 in adjusting the dc input of the test device so that its transfer function is displayed on the center of the oscilloscope face.

The transfer function display is a plot of V_{IN} vs V_{OUT} for an amplifier. This display provides information about three amplifier parameters: gain, gain linearity, and output swing.

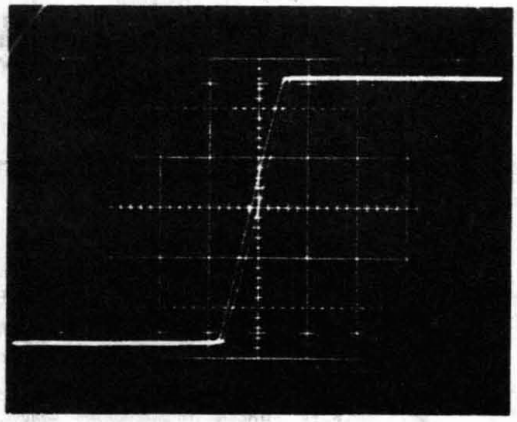

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FIGURE 5. Transfer Function Display

Gain is displayed as the slope, $\Delta V_{OUT}/\Delta V_{IN}$ of the transfer function. Gain linearity is indicated change in slope of the V_{OUT}/V_{IN} display as a function of output voltage. This display is particularly useful in detecting crossover distortion in a Class B output stage. Output swing is measured as the vertical deflection of the transfer function at the horizontal extremes of the display.

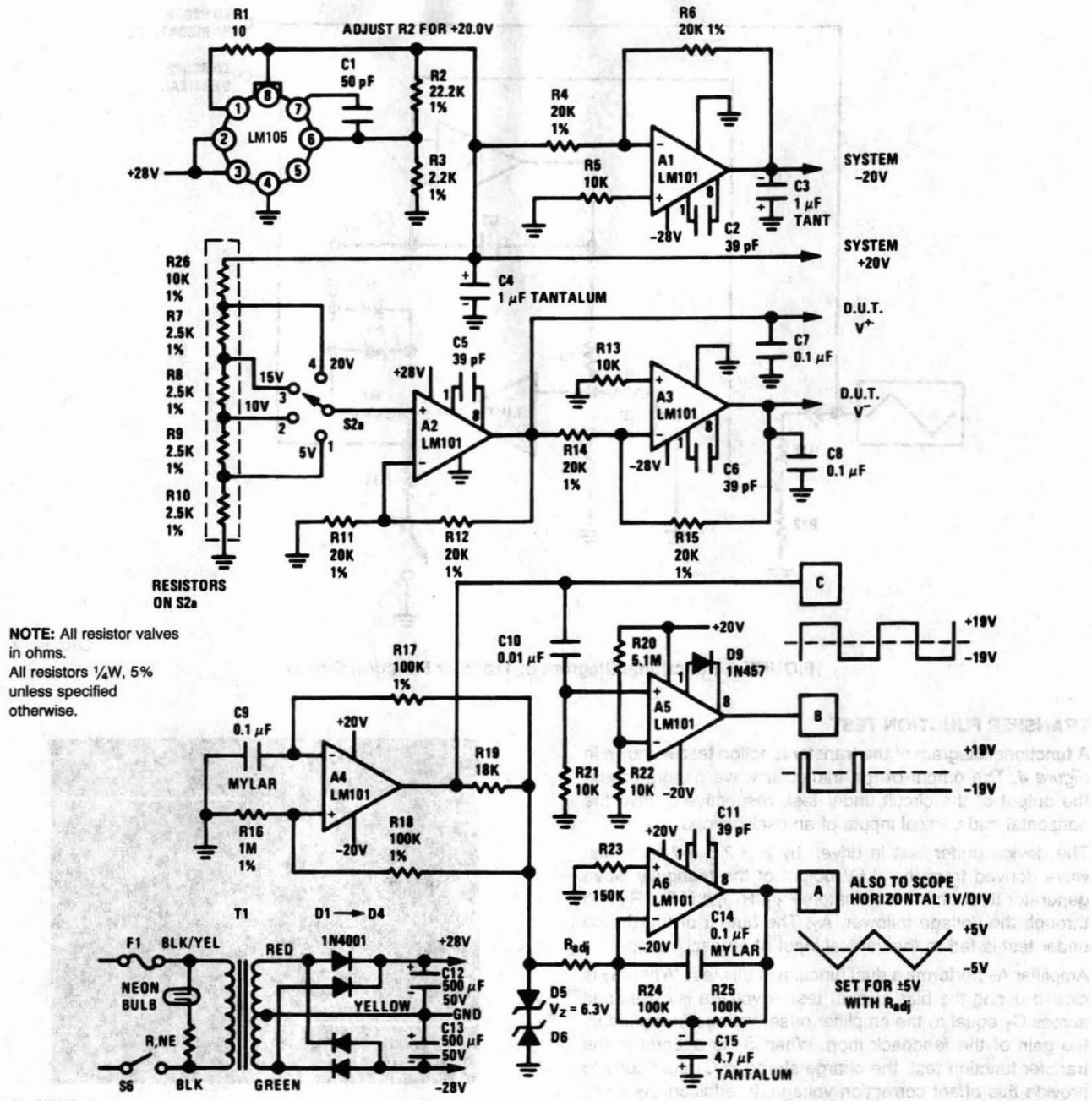

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FIGURE 6. Power Supply and Function Generator

DETAILED CIRCUIT DESCRIPTION

POWER SUPPLIES

As shown in *Figure 6*, which is a complete schematic of the power supply and function generator, two power supplies are provided in the test set. One supply provides a fixed ±20V to power the circuitry in the test set; the other provides ±5V to ±20V to power the circuit under test.

The test set power supply regulator accepts +28V from the positive rectifier and filter and provides +20V through the LM100 positive regulator. Amplifier A_1 is powered from the negative rectifier and filter and operates as a unity gain inverter whose input is +20V from the positive regulator, and whose output is −20V.

The test circuit power supply is referenced to the +20V output of the positive regulator through the variable divider comprising R_7, R_8, R_9, R_{10}, and R_{26}. The output of this divider is +10V to +2.5V according to the position of S_{2a} and is fed to the non-inverting, gain-of-two amplifier, A_2. A_2 is powered from +28V and provides +20V to +5V at its output. A_3 is a unity gain inverter whose input is the output of A_2 and which is powered from −28V. The complementary outputs of amplifiers A_2 and A_3 provide dc power to the circuit under test.

LM101 amplifiers are used as A_2 and A_3 to allow operation from one ground referenced voltage each and to provide protective current limiting for the device under test.

FUNCTION GENERATOR

The function generator provides three outputs, a ±19V square wave, a −19V to +19V pulse having a 1% duty cycle, and a ±5V triangular wave. The square wave is the

basic function from which the pulse and triangular wave are derived, the pulse is referenced to the leading edge of the square wave, and the triangular wave is the inverted and integrated square wave.

Amplifier A_4 is an astable multivibrator generating a square wave from positive to negative saturation. The amplitude of this square wave is approximately ±19V. The square wave frequency is determined by the ratio of R_{18} to R_{16} and by the time constant, $R_{17}C_9$. The operating frequency is stabilized against temperature and power regulation effects by regulating the feedback signal with the divider R_{19}, D_5 and D_6.

Amplifier A_5 is a monostable multivibrator triggered by the positive going output of A_4. The pulse width of A_5 is determined by the ratio of R_{20} to R_{22} and by the time constant $R_{21}C_{10}$. The output pulse of A_5 is an approximately 1% duty cycle pulse from approximately −19V to +19V.

Amplifier A_6 is a dc stabilized integrator driven from the amplitude-regulated output of A_4. Its output is a ±5V triangular wave. The amplitude of the output of A_6 is determined by the square wave voltage developed across D_5 and D_6 and the time constant $R_{adj}C_{14}$. DC stabilization is accomplished by the feedback network R_{24}, R_{25}, and C_{15}. The ac attenuation of this feedback network is high enough so that the integrator action at the square wave frequency is not degraded.

Operating frequency of the function generator may be varied by adjusting the time constants associated with A_4, A_5, and A_6 in the same ratio.

TEST CIRCUIT

A complete schematic diagram of the test circuit is shown in *Figure 7*. The test circuit accepts the outputs of the power supplies and function generator and provides horizontal and vertical outputs for an X-Y oscilloscope, which is used as the measurement system.

The primary elements of the test circuit are the feedback buffer and integrator, comprising amplifier A_7 and its feedback network C_{16}, R_{31}, R_{32}, and C_{17}, and the differential amplifier network, comprising the device under test and the feedback network R_{40}, R_{43}, R_{44}, and R_{52}. The remainder of the test circuit provides the proper conditioning for the device under test and scaling for the oscilloscope, on which the test results are displayed.

The amplifier A_8 provides a variable amplitude source of common mode signal to exercise the amplifier under test over its common mode range. This amplifier is connected as a non-inverting gain-of-3.6 amplifier and receives its input from the triangular wave generator. Potentiometer R_{37} allows the output of this amplifier to be varied from ±0 volts to ±18 volts. The output of this amplifier drives the differential input resistors, R_{43} and R_{44}, for the device under test.

The resistors R_{46} and R_{47} are current sensing resistors which sense the input current of the device under test. These resistors are switched into the circuit in the proper sequence by the field effect transistors Q_6 and Q_7. Q_6 and Q_7 are driven from the square wave output of the function generator by the PNP pair, Q_{10} and Q_{11}, and the NPN pair, Q_8 and Q_9. Switch sections S_{1b} and S_{1c} select the switching sequence for Q_8 and Q_9 and hence for Q_6 and Q_7. In the bias current test, the FET drivers, Q_8 and Q_9, are switched by out of phase signals from Q_{10} and Q_{11}. This opens the FET switches Q_6 and Q_7 on alternate half cycles of the square wave output of the function generator. During the offset voltage, offset current test, the FET drivers are operated synchronously from the output of Q_{11}. During the transfer function test, Q_6 and Q_7 are switched on continuously by turning off Q_{11}. R_{42} and R_{45} maintain the gates of the FET switches at zero gate to source voltage for maximum conductance during their on cycle. Since the sources of these switches are at the common mode input voltage of the device under test, these resistors are connected to the output of the common mode driver amplifier, A_8.

The input for the integrator-feedback buffer, A_7, is selected by the FET switches Q_4 and Q_5. During the bias current and offset voltage offset current tests, A_7 is connected as an integrator and receives its input from the output of the device under test. The output of A_7 drives the feedback resistor, R_{40}. In this connection, the integrator holds the output of the device under test near ground and serves to amplify the voltages corresponding to bias current, offset current, and offset voltage by a factor of 1,000 before presenting them to the measurement system. FET switches Q_4 and Q_5 are turned on by switch section S_{1b} during these tests.

FET switches Q_4 and Q_5 are turned off during the transfer function test. This disconnects A_7 from the output of the device under test and changes it from an integrator to a non-inverting unity gain amplifier driven from the triangular wave output of the function generator through the attenuator R_{33} and R_{34} and switch section S_{1a}. In this connection, amplifier A_7 serves two functions; first, to provide an offset voltage correction to the input of the device under test and, second, to drive the input of the device under test with a ±2.5 mV triangular wave centered about the offset voltage. During this test, the common mode driver amplifier is disabled by switch section S_{1a} and the vertical input of the measurement oscilloscope is transferred from the output of the integrator-buffer, A_7, to the output of the device under test by switch section S_{1d}. S_{2a} allows supply voltages for the device under test to be set at ±5, ±10, ±15, or ±20V. S_{2b} changes the vertical scale factor for the measurement oscilloscope to maintain optimum vertical deflection for the particular power supply voltage used. S_4 is a momentary contact pushbutton switch which is used to change the load on the device under test from 10 kΩ to 2 kΩ.

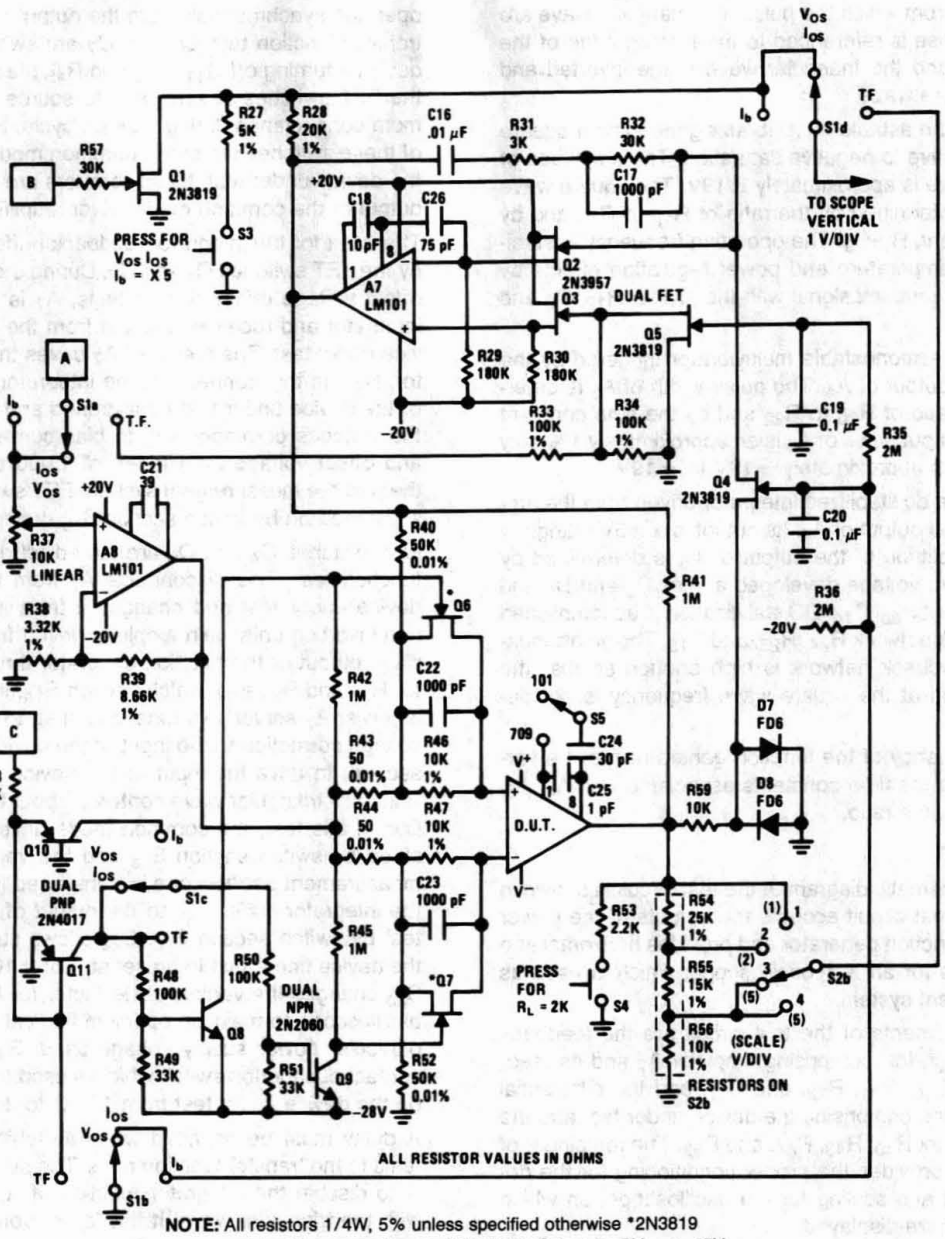
A delay must be provided when switching from the input tests to the transfer function tests. The purpose of this delay is to disable the integrator function of A_7 before driving it with the triangular wave. If this is not done, the offset correction voltage, stored on C_{16}, will be lost. This delay between opening FET switch Q_4, and switch Q_5, is provided by the RC filter, R_{35} and C_{19}.

Resistor R_{41} and diodes D_7 and D_8 are provided to control the integrator when no test device is present, or when a faulty test device is inserted. R_{41} provides a dc feedback path in the absence of a test device and resets the integrator to zero. Diodes D_7 and D_8 clamp the input to the integrator to approximately ±.7 volts when a faulty device is inserted.

FET switch Q_1 and resistor R_{28} provide a ground reference at the beginning of the 50-ohm-source, offset-voltage trace. This trace provides a ground reference which is independent of instrument or oscilloscope calibration. The gate of Q_1 is driven by the output of monostable multivibrator A_5, and shorts the vertical oscilloscope drive signal to ground during the time that A_5 output is positive.

Switch S_3, R_{27}, and R_{28} provide a 5X scale increase during input parameter tests to allow measurement of amplifiers with large offset voltage, offset current, or bias current.

Switch S_5 allows amplifier compensation to be changed for 101 or 709 type amplifiers.



NOTE: All resistors 1/4W, 5% unless specified otherwise *2N3819 matched for on resistance within 200Ω Select for BV_{GS} > 45V

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FIGURE 7. Test Circuit

CALIBRATION

Calibration of the test system is relatively simple and requires only two adjustments. First, the output of the main regulator is set up for 20V. Then, the triangular wave generator is adjusted to provide ±5V output by selecting R_{adj}. This sets the horizontal sweep for the X-Y oscilloscope used as the measurement system. The oscilloscope is then set up for 1V/division vertical and for a full 10 division horizontal sweep.

Scale factors for the three test positions are:

1. Bias Current Display (*Figure 2*)

I_{bias} total	100 nA/div. vertical
Common Mode Voltage	Variable horizontal

2. Offset Voltage-Offset Current (*Figure 3*)

I_{offset}	100 nA/div. vertical
V_{offset}	1 mV/div. vertical
Common Mode Voltage	Variable horizontal

3. Transfer Function (*Figure 5*)

V_{IN}	0.5 mV/div.
V_{OUT}	5V/div. @ V_s ±20V
	5V/div. @ V_s ±15V
	2V/div. @ V_s ±10V
	1V/div. @ V_s ±5V

$$\text{Gain} = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

CONSTRUCTION

Test set construction is simplified through the use of integrated circuits and etched circuit layout.

Figure 8 gives photographs of the completed tester. *Figure 9* shows the parts location for the components on the circuit board layout of *Figure 10*. An attempt should be made to

adhere to this layout to insure that parasitic coupling between elements will not cause oscillations or give calibration problems.

Table I is a listing of special components which are needed to fit the physical layout given for the tester.

TABLE I. Partial Parts List

T_1	Triad F-90X
S_1	Centralab PA2003 non-shorting
S_2	Centralab PA2015 non-shorting
S_3, S_4	Grayhill 30-1 Series 30 subminiature pushbutton switch
S_5, S_6	Alcoswitch MST-105D SPDT

CONCLUSIONS

A semi-automatic test system has been described which will completely test the important operational amplifier parameters over the full power supply and common mode ranges. The system is simple, inexpensive, easily calibrated, and is equally suitable for engineering or quality assurance usage.

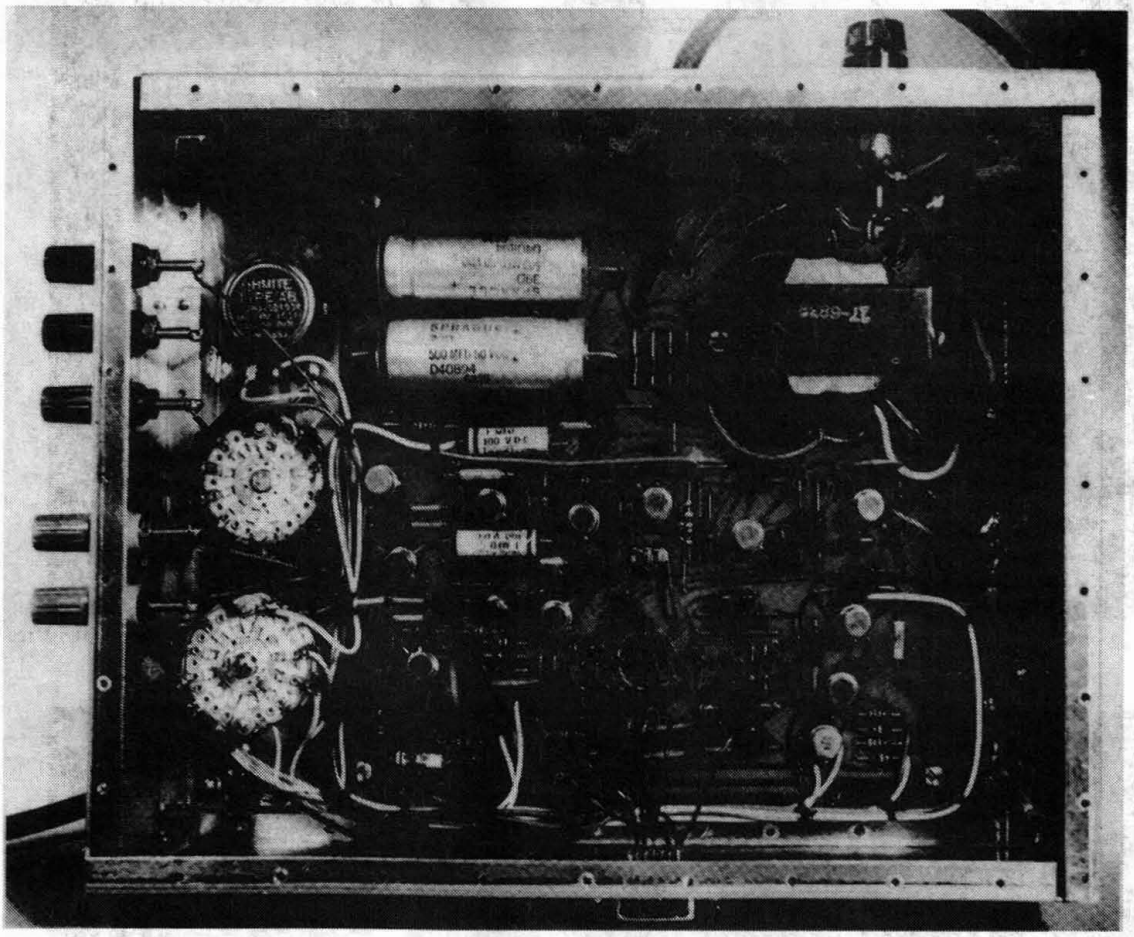

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FIGURE 8a. Bottom of Test Set

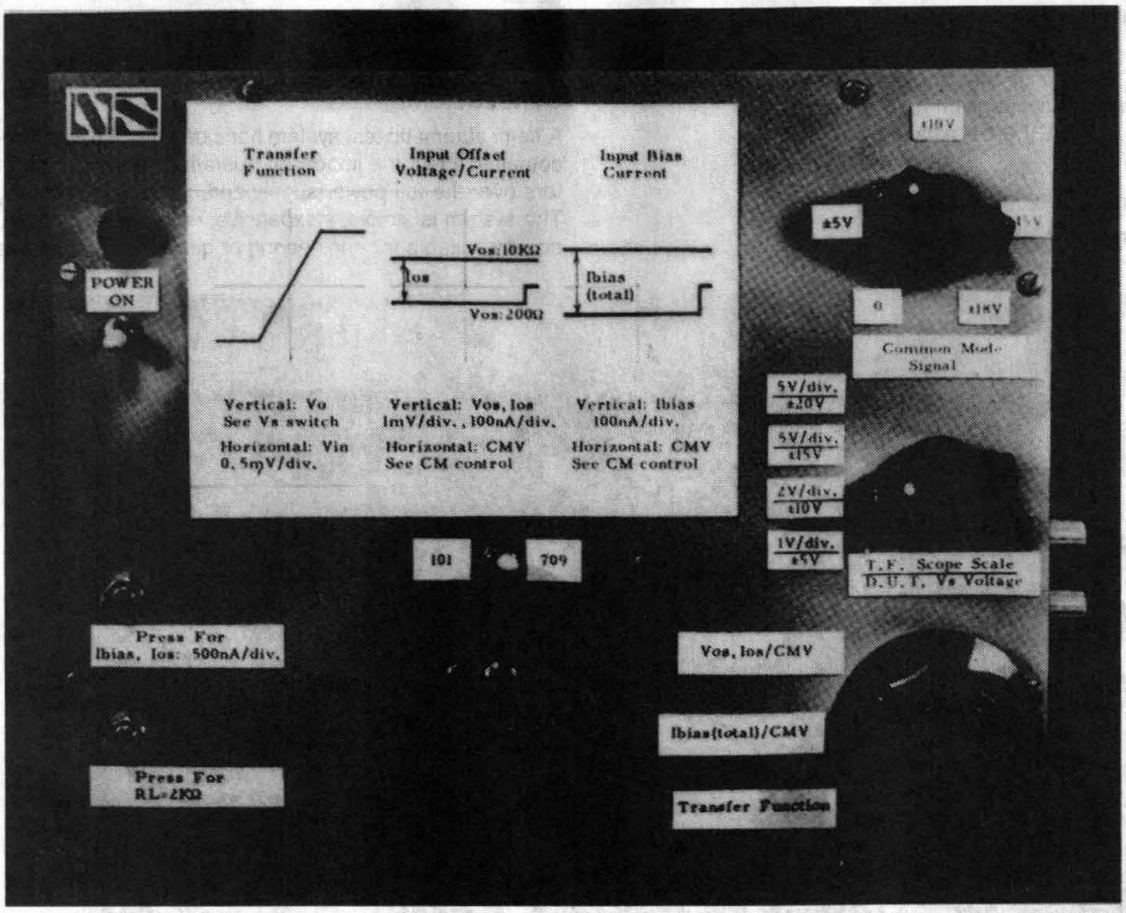

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FIGURE 8b. Front Panel

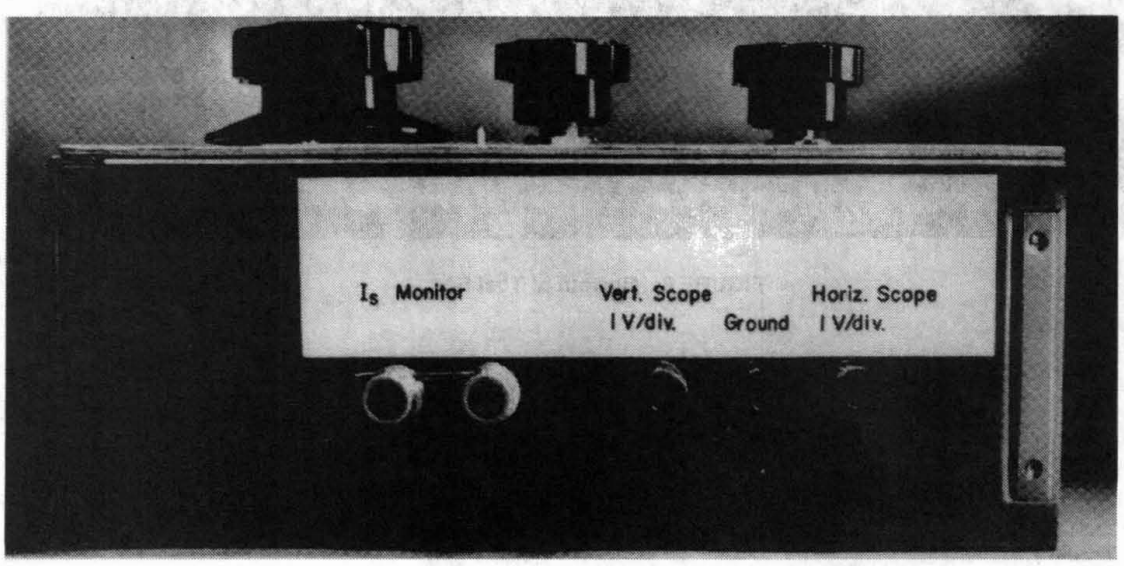

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FIGURE 8c. Jacks

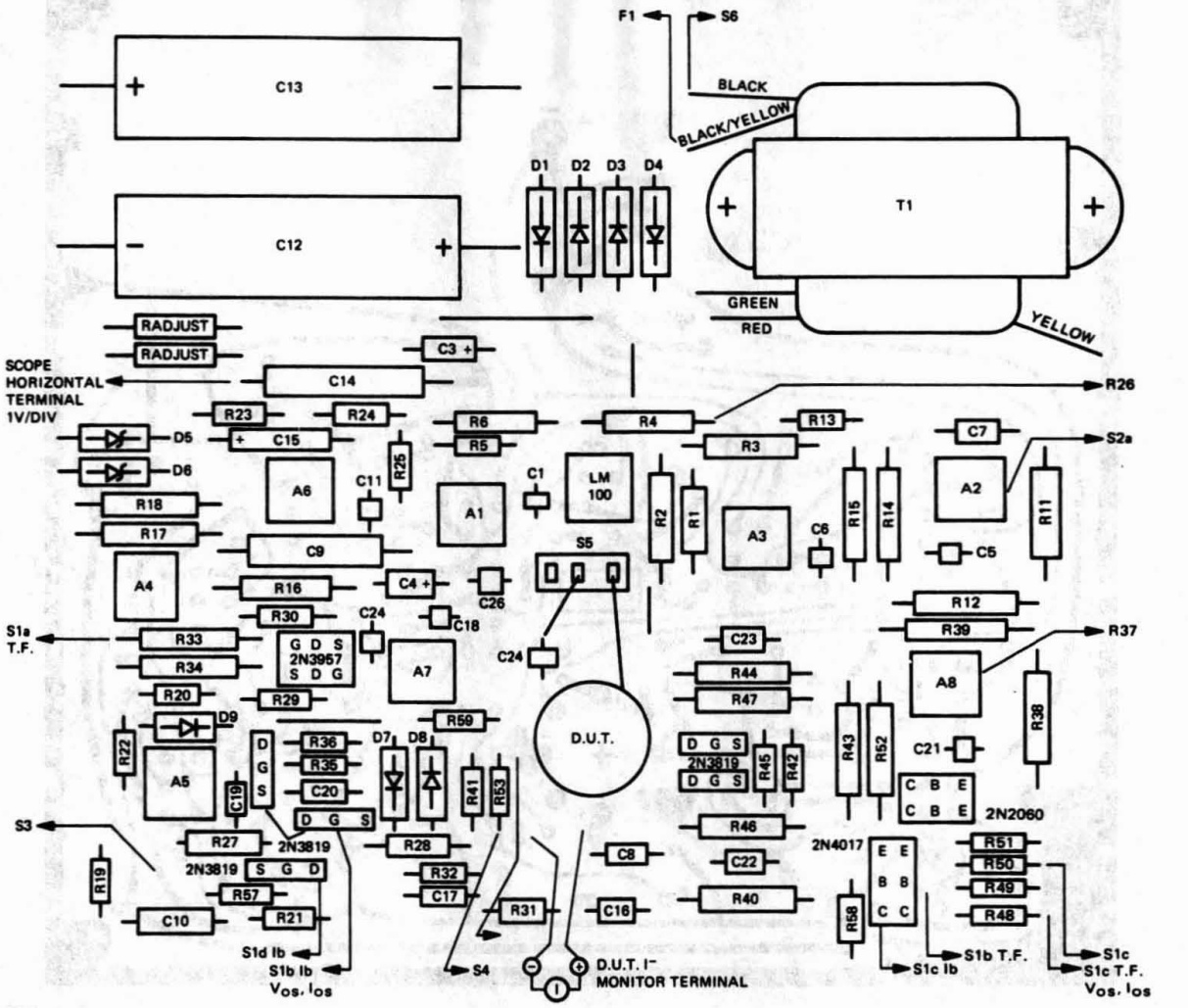

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FIGURE 9. Component Location, Top View

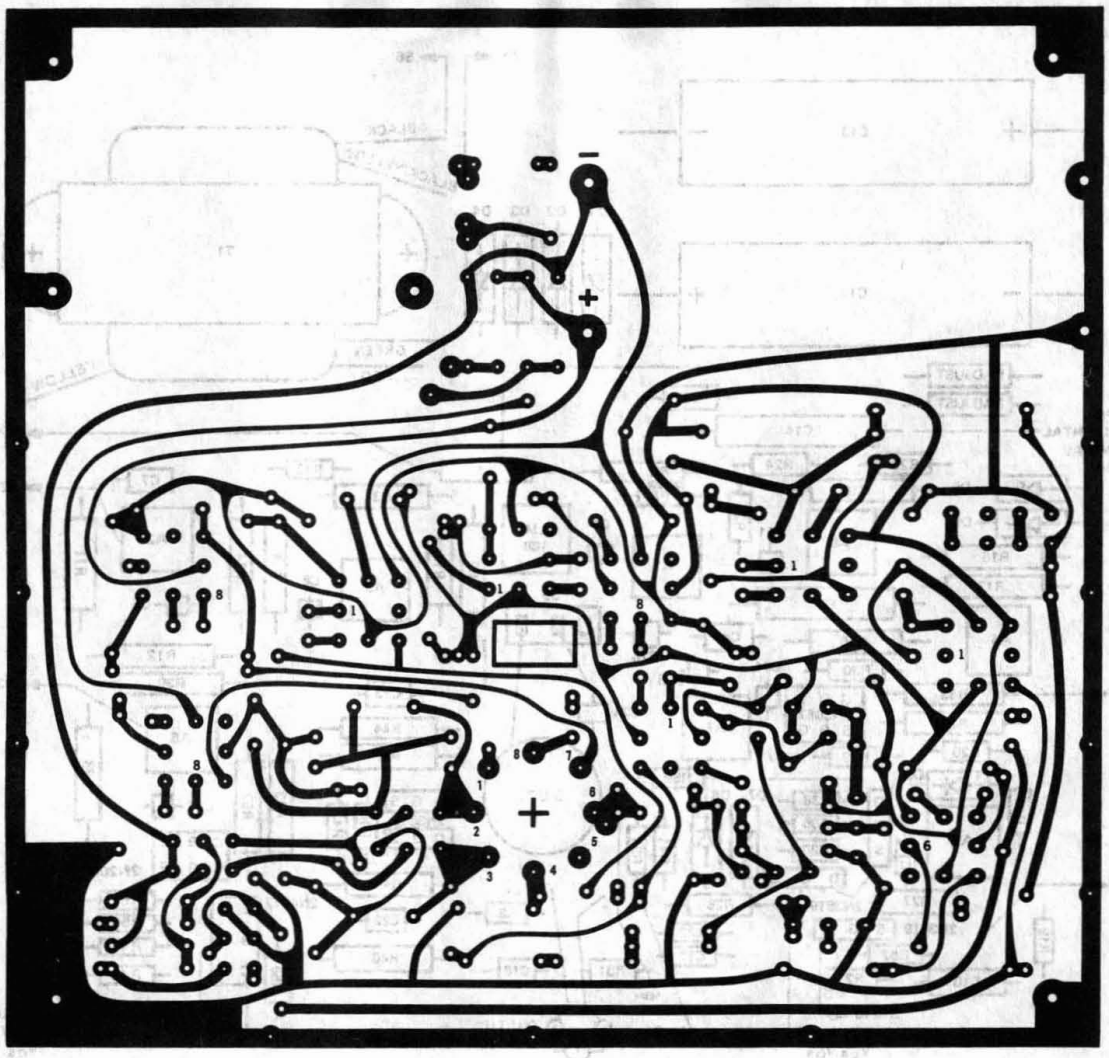

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FIGURE 10. Circuit Board Layout

IC Op Amp Beats FETs on Input Current

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Application Note 29

abstract

A monolithic operational amplifier having input error currents in the order of 100 pA over a −55°C to 125°C temperature range is described. Instead of FETs, the circuit used bipolar transistors with current gains of 5000 so that offset voltage and drift are not degraded. A power consumption of 1 mW at low voltage is also featured.

A number of novel circuits that make use of the low current characteristics of the amplifier are given. Further, special design techniques required to take advantage of these low currents are explored. Component selection and the treatment of printed circuit boards is also covered.

introduction

A year ago, one of the loudest complaints heard about IC op amps was that their input currents were too high. This is no longer the case. Today ICs can provide the ultimate in performance for many applications—even surpassing FET amplifiers.

FET input stages have long been considered the best way to get low input currents in an op amp. Low-picoamp input currents can in fact be obtained at room temperature. However, this current, which is the leakage current of the gate junction, doubles every 10°C, so performance is severely degraded at high temperatures. Another disadvantage is that it is difficult to match FETs closely.[1] Unless expensive selection and trimming techniques are used, typical offset voltages of 50 mV and drifts of 50 μV/°C must be tolerated.

Super gain transistors[2] are now challenging FETs. These devices are standard bipolar transistors which have been diffused for extremely high current gains. Typically, current gains of 5000 can be obtained at 1 μA collector currents. This makes it possible to get input currents which are competitive with FETs. It is also possible to operate these transistors at zero collector base voltage, eliminating the leakage currents that plague the FET. Hence they can provide lower error currents at elevated temperatures. As a bonus, super gain transistors match much better than FETs with typical offset voltages of 1 mV and drifts of 3 μV/°C.

Figure 1 compares the typical input offset currents of IC op amps and FET amplifiers. Although FETs give superior performance at room temperature, their advantage is rapidly lost as temperature increases. Still, they are clearly better than early IC amplifiers like the LM709.[3] Improved devices, like the LM101A,[4] equal FET performance over a −55°C to 125°C temperature range. Yet they use standard transistors in the input stage. Super gain transistors can provide more than an order of magnitude improvement over the LM101A. The LM108 uses these to equal FET performance over a 0°C to 70°C temperature range.

In applications involving 125°C operation, the LM108 is about two orders of magnitude better than FETs. In fact, unless special precautions are taken, overall circuit performance is often limited by leakages in capacitors, diodes, analog switches or printed circuit boards, rather than by the op amp itself.

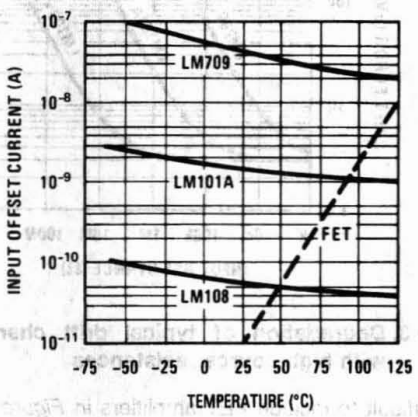

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Figure 1. Comparing IC op amps with FET-input amplifier

effects of error current

In an operational amplifier, the input current produces a voltage drop across the source resistance, causing a dc error. This effect can be minimized by operating the amplifier with equal resistances on the two inputs.[5] The error is then proportional to the difference in the two input currents, or the offset current. Since the current gains of monolithic transistors tend to match well, the offset current is typically a factor of ten less than the input currents.

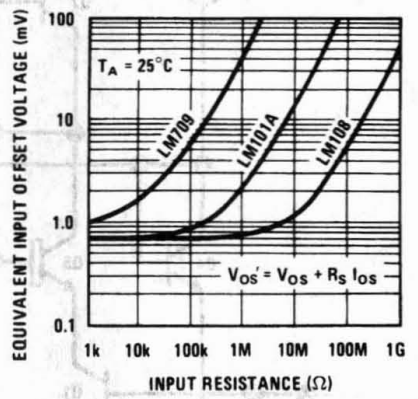

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Figure 2. Illustrating the effect of source resistance on typical input error voltage

Naturally, error current has the greatest effect in high impedance circuitry. *Figure 2* illustrates this point. The offset voltage of the LM709 is degraded significantly with source resistances greater than 10 kΩ. With the LM101A this is extended to source resistances high as 500 kΩ. The LM108, on the other hand, works well with source resistances above 10 MΩ.

Reprinted from *EEE*, December 1969.

High source resistances have an even greater effect on the drift of an amplifier, as shown in *Figure 3*. The performance of the LM709 is worsened with sources greater than 3 kΩ. The LM101A holds out to 100 kΩ sources, while the LM108 still works well at 3 MΩ.

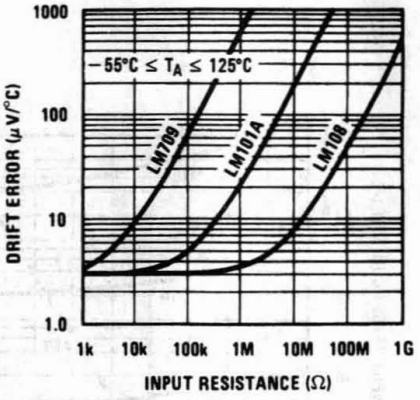

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Figure 3. Degradation of typical drift characteristics with high source resistances

It is difficult to include FET amplifiers in *Figure 3* because their drift is initially 50 μV/°C, unless they are selected and trimmed. Even though their drift may be well controlled (5 μV/°C) over a limited temperature range, trimmed amplifiers generally exhibit a much higher drift over a −55°C to 125°C temperature range. At any rate, their average drift rate would, at best, be like that of the LM101A where 125°C operation is involved.

Applications that require low error currents include amplifiers for photodiodes or capacitive transducers, as these usually operate at megohm impedance levels. Sample-and-hold-circuits, timers, integrators and analog memories also benefit from low error currents. For example, with the LM709, worst case drift rates for these kinds of circuits is in the order of 1.5 V/sec. The LM108 improves this to 3 mV/sec.—worst case over a −55°C to 125°C temperature range. Low input currents are also helpful in oscillators and active filters to get low frequency operation with reasonable capacitor values. The LM108 can be used at a frequency of 1 Hz with capacitors no larger than 0.01 μF. In logarithmic amplifiers, the dynamic range can be extended by nearly 60 dB by going from the LM709 to the LM108. In other applications, having low error currents often permits an entirely different design approach which can greatly simplify circuitry.

the LM108

Figure 4 shows a simplified schematic of the LM108. Two kinds of NPN transistors are used on the IC chip: super gain (primary) transistors which have a current gain of 5000 with a breakdown voltage of 4V and conventional (secondary) transistors which have a current gain of 200 with an 80V breakdown. These are differentiated on the schematic by drawing the secondaries with a wider base.

Primary transistors (Q_1 and Q_2) are used for the input stage; and they are operated in a cascode connection with Q_5 and Q_6. The bases of Q_5 and Q_6 are bootstrapped to the emitters of Q_1 and Q_2 through Q_3 and Q_4, so that the input transistors are operated at zero collector-base voltage. Hence, circuit performance is not impaired by the low breakdown of the primaries, as the secondary transistors stand

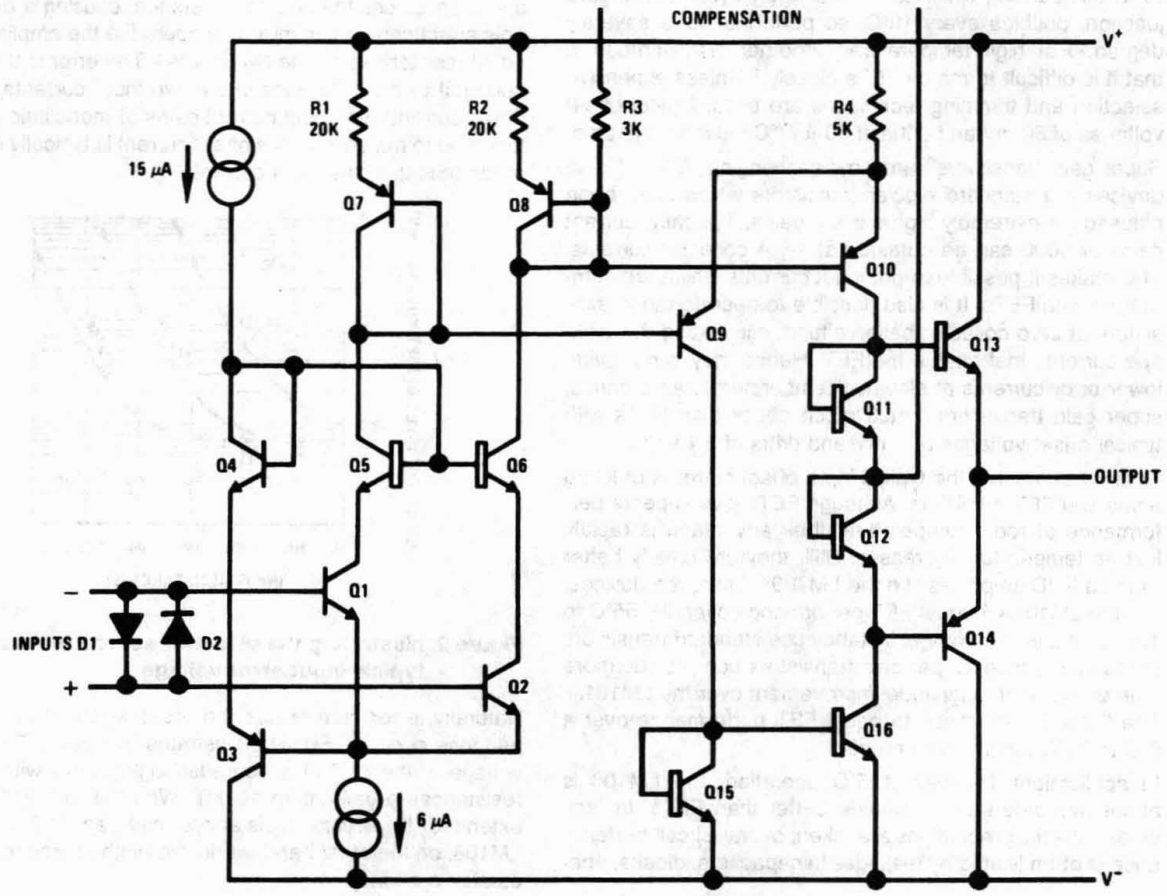

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Figure 4. Simplified schematic of the LM108

off the commom mode voltage. This configuration also improves the commom mode rejection since the input transistors do not see variations in the commom mode voltage. Further, because there is no voltage across their collector-base junctions, leakage currents in the input transistors are effectively eliminated.

The second stage is a differential amplifier using high gain lateral PNPs (Q_9 and Q_{10}).[6] These devices have current gains of 150 and a breakdown voltage of 80V. R_1 and R_2 are the collector load resistors for the input stage. Q_7 and Q_8 are diode connected laterals which compensate for the emitter-base voltage of the second stage so that its operating current is set at twice that of the input stage by R_4.

The second stage uses an active collector load (Q_{15} and Q_{16}) to obtain high gain. It drives a complementary class-B output stage which gives a substantial load driving capability. The dead zone of the output stage is eliminated by biasing it on the verge of conduction with Q_{11} and Q_{12}.

Two methods of frequency compensation are available for the amplifier. In one a 30 pF capacitor is connected from the input to the output of the second stage (between the compensation terminals). This method is pin-compatible with the LM101 or LM101A. It can also be compensated by connecting a 100 pF capacitor from the output of the second stage to ground. This technique has the advantage of improving the high frequency power supply rejection by a factor of ten.

A complete schematic of the LM108 is given in the Appendix along with a description of the circuit. This includes such essential features as overload protection for the inputs and outputs.

performance

The primary design objective for the LM108 was to obtain very low input currents without sacrificing offset voltage or drift. A secondary objective was to reduce the power consumption. Speed was of little concern, as long as it was comparable with the LM709. This is logical as it is quite difficult to make high-impedance circuits fast; and low power circuits are very resistant to being made fast. In other respects, it was desirable to make the LM108 as much like the LM101A as possible.

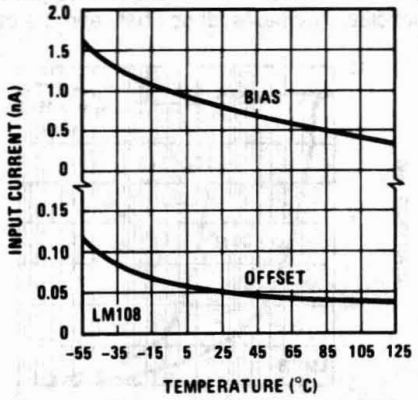

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Figure 5. Input currents

Figure 5 shows the input current characteristics of the LM108 over a −55°C to 125°C temperature range. Not only are the input currents low, but also they do not change radically over temperature. Hence, the device lends itself to relatively simple temperature compensation schemes, that will be described later.

There has been considerable discussion about using Darlington input stages rather than super gain transistors to obtain low input currents.[6,7] It is appropriate to make a few comments about that here.

Darlington inputs can give about the same input bias currents as super gain transistors—at room temperature. However, the bias current varies as the square of the transistor current gain. At low temperatures, super gain devices have a decided advantage. Additionally, the offset current of super gain transistors is considerably lower than Darlingtons, when measured as a percentage of bias current. Further, the offset voltage and offset voltage drift of Darlington transistors is both higher and more unpredictable.

Experience seems to tell the real truth about Darlingtons. Quite a few op amps with Darlington input stages have been introduced. However, none have become industry standards. The reason is that they are more sensitive to variations in the manufacturing process. Therefore, satisfactory performance specifications can only be obtained by sacrificing the manufacturing yield.

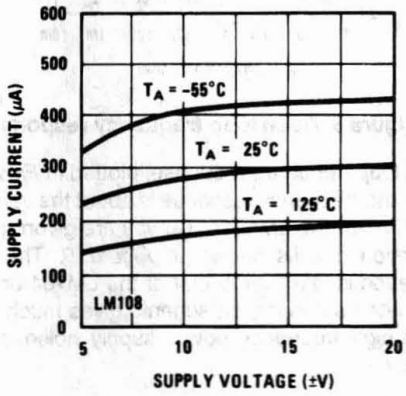

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Figure 6. Supply current

The supply current of the LM108 is plotted as a function of supply voltage in *Figure 6*. The operating current is about an order of magnitude lower than devices like the LM709. Furthermore, it does not vary radically with supply voltage which means that the device performance is maintained at low voltages and power consumption is held down at high voltages.

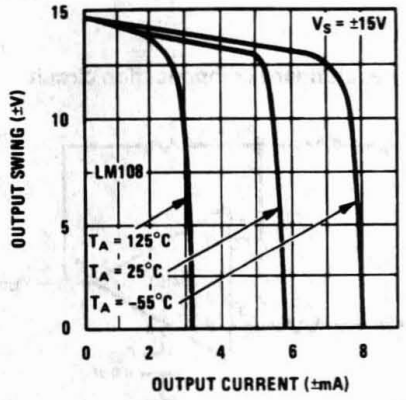

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Figure 7. Output swing

The output drive capability of the circuit is illustrated in *Figure 7*. The output swings to within a volt of the supplies,

which is especially important when operating at low voltages. The output falls off rapidly as the current increases above a certain level and the short circuit protection goes into effect. The useful output drive is limited to about ±2 mA. It could have been increased by the addition of Darlington transistors on the output, but this would have restricted the voltage swing at low supply voltages. The amplifier, incidentally, works with common mode signals to within a volt of the supplies so it can be used with supply voltages as low as ±2V.

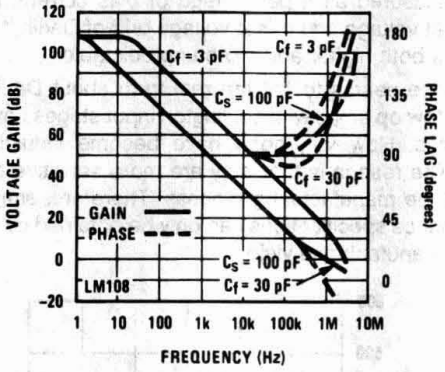

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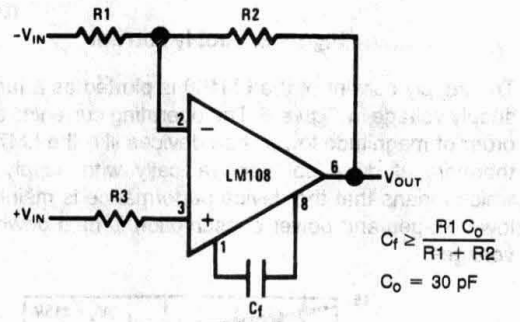
Figure 8. Open loop frequency response

The open loop frequency response, plotted in *Figure 8*, indicates that the frequency response is about the same as that of the LM709 or the LM101A. Curves are given for the two compensation circuits shown in *Figure 9*. The standard compensation is identical to that of the LM101 or LM101A. The alternate compensation scheme gives much better rejection of high frequency power supply noise, as will be shown later.



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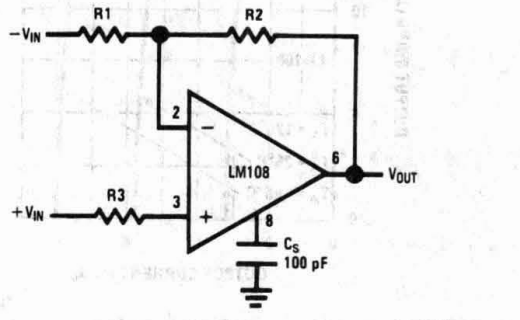
a. standard compensation circuit



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b. alternate compensation circuit

Figure 9. Compensation circuits

With unity gain compensation, both methods give a 75-degree stability margin. However, the shunt compensation has a 300 kHz small signal bandwidth as opposed to 1 MHz for the other scheme. Because the compensation capacitor is not included on the IC chip, it can be tailored to fit the application. When the amplifier is used only at low frequencies, the compensation capacitor can be increased to give a greater stability margin. This makes the circuit less sensitive to capacitive loading, stray capacitances or improper supply bypassing. Overcompensating also reduces the high frequency noise output of the amplifier.

With closed-loop gains greater than one, the high frequency performance can be optimized by making the compensation capacitor smaller. If unity-gain compensation is used for an amplifier with a gain of ten, the gain error will exceed 1-percent at frequencies above 400 Hz. This can be extended to 4 kHz by reducing the compensation capacitor to 3 pF. The formula for determining the minimum capacitor value is given in *Figure 9a*. It should be noted that the capacitor value does not really depend on the closed-loop gain. Instead, it depends on the high frequency attenuation in the feedback networks and, therefore, the values of R_1 and R_2. When it is desirable to optimize performance at high frequencies, the standard compensation should be used. With small capacitor values, the stability margin obtained with shunt compensation is inadequate for conservative designs.

The frequency response of an operational amplifier is considerably different for large output signals than it is for small signals. This is indicated in *Figure 10*. With unity-gain compensation, the small signal bandwidth of the LM108 is 1 MHz. Yet full output swing cannot be obtained above 2 kHz. This corresponds to a slew rate of 0.3 V/μs. Both the full-output bandwidth and the slew rate can be increased by using smaller compensation capacitors, as is indicated in the figure. However, this is only applicable for higher closed loop gains. The results plotted in *Figure 10* are for standard compensations. With unity gain compensation, the same curves are obtained for the shunt compensation scheme.

Classical op amp theory establishes output resistance as an important design parameter. This is not true for IC op amps: The output resistance of most devices is low enough that it can be ignored, because they use class-B output stages. At low frequencies, thermal feedback between the output and

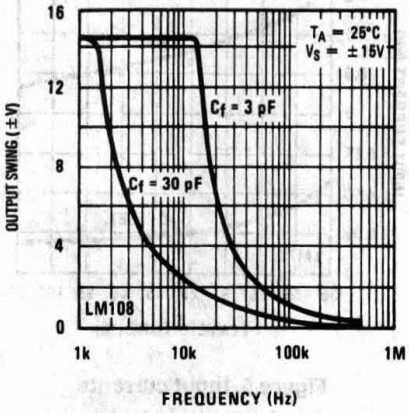

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Figure 10. Large signal frequency response

input stages determines the effective output resistance, and this cannot be accounted for by conventional design theories. Semiconductor manufacturers take care of this by specifying the gain under full load conditions, which combines output resistance with gain as far as it affects overall circuit performance. This avoids the fictitious problem that can be created by an amplifier with infinite gain, which is good, that will cause the open loop output resistance to appear infinite, which is bad, although none of this affects overall performance significantly.

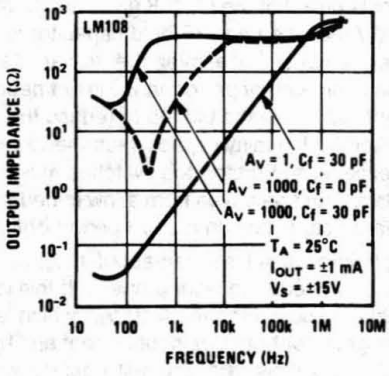

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Figure 11. Closed loop output impedance

The *closed loop* output impedance is, nonetheless, important in some applications. This is plotted for several operating conditions in *Figure 11*. It can be seen that the output impedance rises to about 500Ω at high frequencies. The increase occurs because the compensation capacitor rolls off the open loop gain. The output resistance can be reduced at the intermediate frequencies, for closed loop gains greater than one, by making the capacitor smaller. This is made apparent in the figure by comparing the output resistance with and without frequency compensation for a closed loop gain of 1000.

The output resistance also tends to increase at low frequencies. Thermal feedback is responsible for this phenomenon. The data for *Figure 11* was taken under large-signal conditions with ±15V supplies, the output at zero and ±1 mA current swing. Hence, the thermal feedback is accentuated more than would be the case for most applications.

In an op amp, it is desirable that performance be unaffected by variations in supply voltage. IC amplifiers are generally better than discretes in this respect because it is necessary for one single design to cover a wide range of uses. The LM108 has a power supply rejection which is typically in excess of 100 dB, and it will operate with supply voltages from ±2V to ±20V. Therefore, well-regulated supplies are unnecessary, for most applications, because a 20-percent variation has little effect on performance.

The story is different for high-frequency noise on the supplies, as is evident from *Figure 12*. Above 1 MHz, practically all the noise is fed through to the output. The figure also demonstrates that shunt compensation is about ten times better at rejecting high frequency noise than is standard compensation. This difference is even more pronounced with larger capacitor values. The shunt compensation has the added advantage that it makes the circuit virtually unaffected by the lack of supply bypassing.

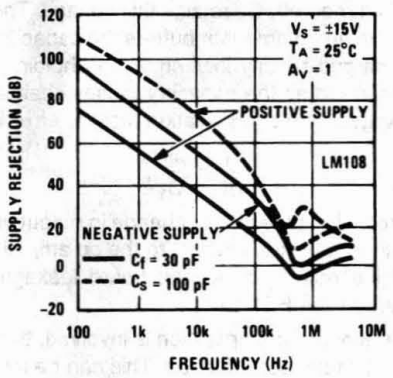

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Figure 12. Power supply rejection

Power supply rejection is defined as the ratio of the change in offset voltage to the change in the supply voltage producing it. Using this definition, the rejection at low frequencies is unaffected by the closed loop gain. However, at high frequencies, the opposite is true. The high frequency rejection is increased by the closed loop gain. Hence, an amplifier with a gain of ten will have an order of magnitude better rejection than that shown in *Figure 12* in the vicinity of 100 kHz to 1 MHz.

The overall performance of the LM108 is summarized in Table I*. It is apparent from the table and the previous discussion that the device is ideally suited for applications that require low input currents or reduced power consumption. The speed of the amplifier is not spectacular, but this is not usually a problem in high-impedance circuitry. Further, the reduced high frequency performance makes the amplifier easier to use in that less attention need be paid to capacitive loading, stray capacitances and supply bypassing.

applications

Because of its low input current the LM108 opens up many new design possibilities. However, extra care must be taken in component selection and the assembly of printed circuit boards to take full advantage of its performance. Further, unusual design techniques must often be applied to get around the limitations of some components.

sample and hold circuits

The holding accuracy of a sample and hold is directly related to the error currents in the components used. Therefore, it is a good circuit to start off with in explaining the problems

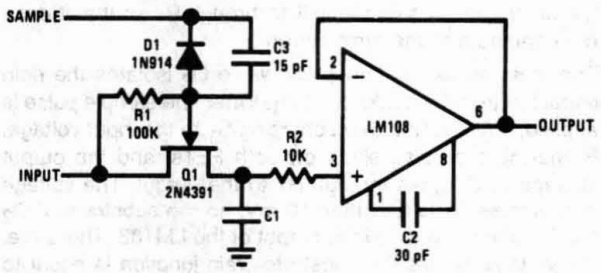

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Figure 13. Sample and hold circuit

involved. *Figure 13* shows one configuration for a sample and hold. During the sample interval, Q_1 is turned on, charging the hold capacitor, C_1, up to the value of the input signal.

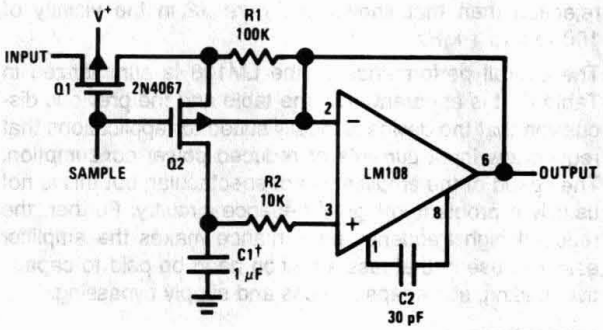
*See Appendix Heading in This Application Note.

When Q_1 is turned off, C_1 retains this voltage. The output is obtained from an op amp that buffers the capacitor so that it is not discharged by any loading. In the holding mode, an error is generated as the capacitor looses charge to supply circuit leakages. The accumulation rate for error is given by

$$\frac{dV}{dt} = \frac{I_E}{C_1},$$

where dV/dt is the time rate of change in output voltage and I_E is the sum of the input current to the op amp, the leakage current of the holding capacitor, board leakages and the "off" current of the FET switch.

When high-temperature operation is involved, the FET leakage can limit circuit performance. This can be minimized by using a junction FET, as indicated, because commercial junction FETs have lower leakage than their MOS counterparts. However, at 125°C even junction devices are a problem. Mechanical switches, such as reed relays, are quite satisfactory from the standpoint of leakage. However, they are often undesirable because they are sensitive to vibration, they are too slow or they require excessive drive power. If this is the case, the circuit in *Figure 14* can be used to eliminate the FET leakage.



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†Teflon, polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 3 mV/sec

Figure 14. Sample and hold that eliminates leakage in FET switches

When using P-channel MOS switches, the substrate must be connected to a voltage which is always more positive than the input signal. The source-to-substrate junction becomes forward biased if this is not done. The troublesome leakage current of a MOS device occurs across the substrate-to-drain junction. In *Figure 14*, this current is routed to the output of the buffer amplifier through R_1 so that it does not contribute to the error current.

The main sample switch is Q_1, while Q_2 isolates the hold capacitor from the leakage of Q_1. When the sample pulse is applied, both FETs turn on charging C_1 to the input voltage. Removing the pulse shuts off both FETs, and the output leakage of Q_1 goes through R_1 to the output. The voltage drop across R_1 is less than 10 mV, so the substrate of Q_2 can be bootstrapped to the output of the LM108. Therefore, the voltage across the substrate-drain junction is equal to the offset voltage of the amplifier. At this low voltage, the leakage of the FET is reduced by about two orders of magnitude.

It is necessary to use MOS switches when bootstrapping the leakages in this fashion. The gate leakage of a MOS device is still negligible at high temperatures; this is not the case with junction FETs. If the MOS transistors have protective diodes on the gates, special arrangements must be made to drive Q_2 so the diode does not become forward biased.

In selecting the hold capacitor, low leakage is not the only requirement. The capacitor must also be free of dielectric polarization phenomena.[8] This rules out such types as paper, mylar, electrolytic, tantalum or high-K ceramic. For small capacitor values, glass or silvered-mica capacitors are recommended. For the larger values, ones with teflon, polyethylene or polycarbonate dielectrics should be used.

The low input current of the LM108 gives a drift rate, in hold, of only 3 mV/sec when a 1 μF hold capacitor is used. And this number is worst case over the military temperature range. Even if this kind of performance is not needed, it may still be beneficial to use the LM108 to reduce the size of the hold capacitor. High quality capacitors in the larger sizes are bulky and expensive. Further, the switches must have a low "on" resistance and be driven from a low impedance source to charge large capacitors in a short period of time.

If the sample interval is less than about 100 μs, the LM108 may not be fast enough to work properly. If this is the case, it is advisable to substitute the LM102A,[9] which is a voltage follower designed for both low input current and high speed. It has a 30 V/μs slew rate and will operate with sample intervals as short as 1 μs.

When the hold capacitor is larger than 0.05 μF, an isolation resistor should be included between the capacitor and the input of the amplifier (R_2 in *Figure 14*). This resistor insures that the IC will not be damaged by shorting the output or abruptly shutting down the supplies when the capacitor is charged. This precaution is not peculiar to the LM108 and should be observed on any IC op amp.

integrators

Integrators are a lot like sample-and-hold circuits and have essentially the same design problems. In an integrator, a capacitor is used as a storage element; and the error accumulation rate is again proportional to the input current of the op amp.

Figure 15 shows a circuit that can compensate for the bias current of the amplifier. A current is fed into the summing node through R_1 to supply the bias current. The potentiometer, R_2, is adjusted so that this current exactly equals the bias current, reducing the drift rate to zero.

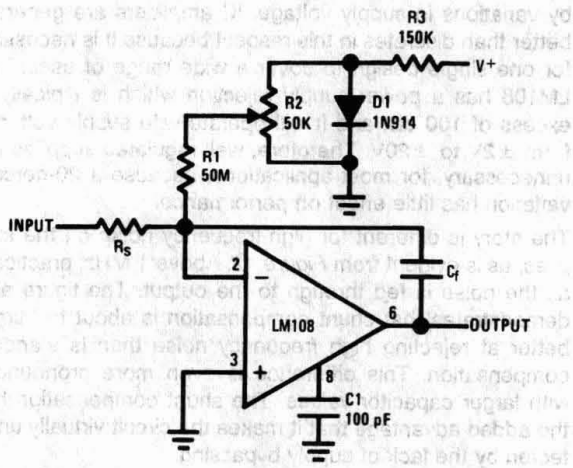

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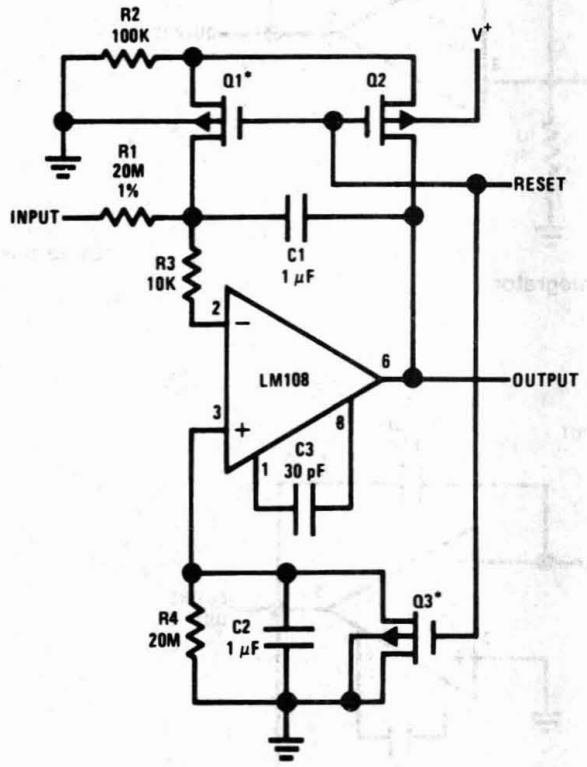
Figure 15. Integrator with bias current compensation

The diode is used for two reasons. First, it acts as a regulator, making the compensation relatively insensitive to variations in supply voltage. Secondly, the temperature drift of diode voltage is approximately the same as the temperature drift of bias current. Therefore, the compensation is more effective if the temperature changes. Over a 0°C to 70°C temperature range, the compensation will give a factor of ten reduction in input current. Even better results are achieved if the temperature change is less.

Normally, it is necessary to reset an integrator to establish the initial conditions for integration. Resetting to zero is readily accomplished by shorting the integrating capacitor with a suitable switch. However, as with the sample and hold circuits, semiconductor switches can cause problems because of high-temperature leakage.

A connection that gets rid of switch leakages is shown in *Figure 16*. A negative-going reset pulse turns on Q_1 and Q_2,



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*Q1 and Q3 should not have internal gate-protection diodes.

Figure 16. Low drift integrator with reset

shorting the integrating capacitor. When the switches turn off, the leakage current of Q_2 is absorbed by R_2 while Q_1 isolates the output of Q_2 from the summing node. Q_1 has practically no voltage across its junctions because the substrate is grounded; hence, leakage currents are negligible.

The additional circuitry shown in *Figure 16* makes the error accumulation rate proportional to the offset current, rather than the bias current. Hence, the drift is reduced by roughly a factor of 10. During the integration interval, the bias current of the non-inverting input accumulates an error across R_4 and C_2 just as the bias current on the inverting input does across R_1 and C_1. Therefore, if R_4 is matched with R_1 and C_2 is matched with C_1 (within about 5 percent) the output will drift at a rate proportional to the difference in these currents. At the end of the integration interval, Q_3 removes the compensating error accumulated on C_2 as the circuit is reset.

In applications involving large temperature changes, the circuit in *Figure 16* gives better results than the compensation scheme in *Figure 15*—especially under worst case conditions. Over a −55°C to 125°C temperature range, the worst case drift is reduced from 3 mV/sec to 0.5 mV/sec when a 1 μF integrating capacitor is used. If this reduction in drift is not needed, the circuit can be simplified by eliminating R_4, C_2 and Q_3 and returning the non-inverting input of the amplifier directly to ground.

In fabricating low drift integrators, it is again necessary to use high quality components and minimize leakage currents in the wiring. The comments made on capacitors in connection with the sample-and-hold circuits also apply here. As an additional precaution, a resistor should be used to isolate the inverting input from the integrating capacitor if it is larger than 0.05 μF. This resistor prevents damage that might occur when the supplies are abruptly shut down while the integrating capacitor is charged.

Some integrator applications require both speed and low error current. The output amplifiers for photomultiplier tubes or solid-state radiation dectectors are examples of this. Although the LM108 is relatively slow, there is a way to speed it up when it is used as an inverting amplifier. This is shown in *Figure 17*.

The circuit is arranged so that the high-frequency gain characteristics are determined by A_2, while A_1 determines the dc and low-frequency characteristics. The non-inverting input of A_1 is connected to the summing node through R_1. A_1 is operated as an integrator, going through unity gain at 500 Hz. Its output drives the non-inverting input of A_2. The inverting input of A_2 is also connected to the summing node through C_3. C_3 and R_3 are chosen to roll off below 750 Hz. Hence, at frequencies above 750 Hz, the feedback path is directly around A_2, with A_1 contributing little. Below 500 Hz, however, the direct feedback path to A_2 rolls off; and the gain of A_1 is added to that of A_2.

The high gain frequency amplifier, A_2, is an LM101A connected with feed-forward compensation.[10] It has a 10 MHz equivalent small-signal bandwidth, a 10V/μs slew rate and a 250 kHz large-signal bandwidth, so these are the high-frequency characteristics of the complete amplifier. The bias current of A_2 is isolated from the summing node by C_3. Hence, it does not contribute to the dc drift of the integrator. The inverting input of A_1 is the only dc connection to the summing junction. Therefore, the error current of the composite amplifier is equal to the bias current of A_1.

If A_2 is allowed to saturate, A_1 will then start towards saturation. If the output of A_1 gets far off zero, recovery from saturation will be slowed drastically. This can be prevented by putting zener clamp diodes across the integrating capacitor. A suitable clamping arrangement is shown in *Figure 17*. D_1 and D_2 are included in the clamp circuit along with R_5 to keep the leakage currents of the zeners from introducing errors.

In addition to increasing speed, this circuit has other advantages. For one, it has the increased output drive capability of the LM101A. Further, thermal feedback is virtually eliminated because the LM108 does not see load variations. Lastly, the open loop gain is nearly infinite at low frequencies as it is the product of the gains of the two amplifiers.

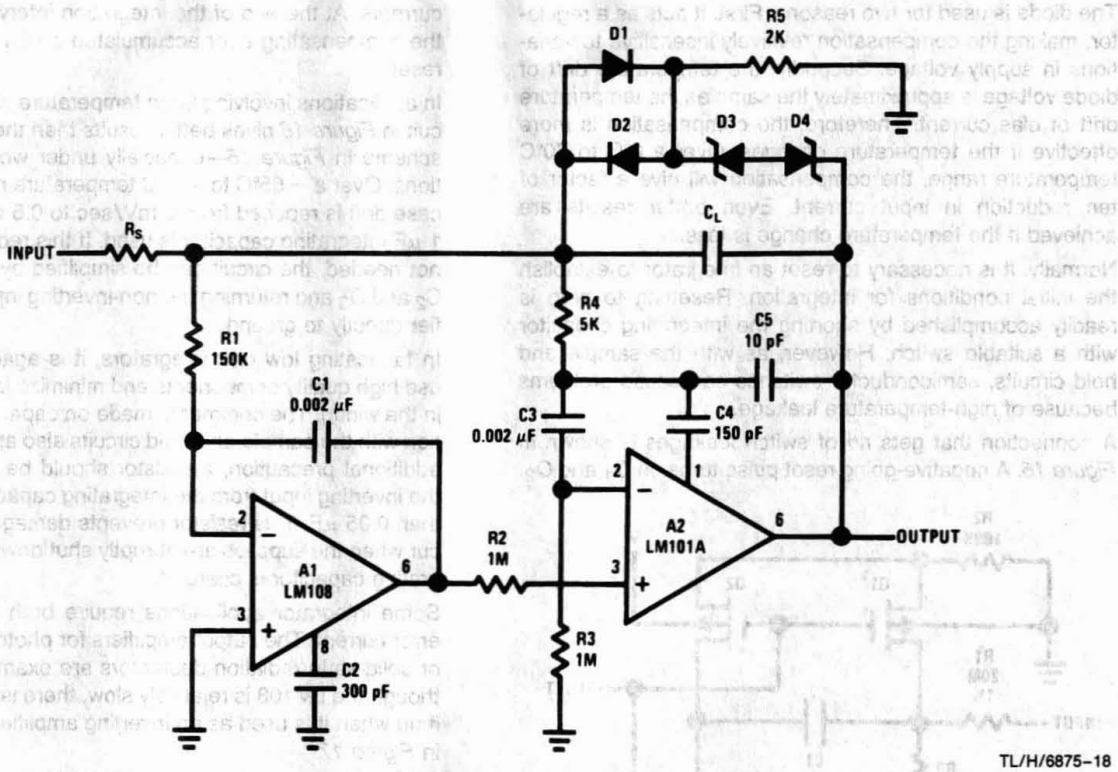

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Figure 17. Fast integrator

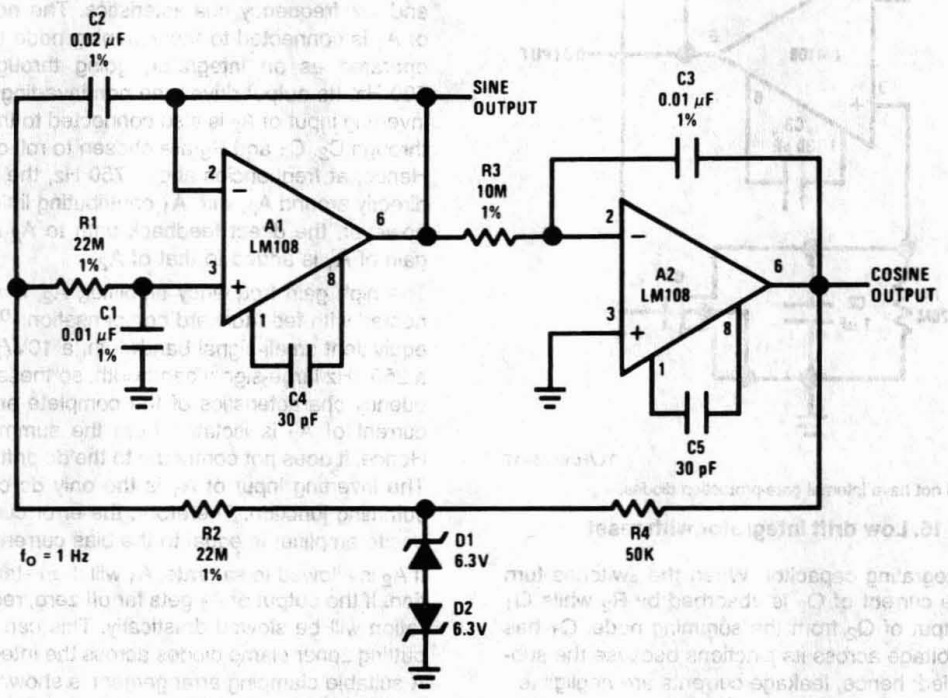

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Figure 18. Sine wave oscillator

sine wave oscillator

Although it is comparatively easy to build an oscillator that aproximates a sine wave, making one that delivers a high-purity sinusoid with a stable frequency and amplitude is another story. Most satisfactory designs are relatively complicated and require individual trimming and temperature compensation to make them work. In addition, they generally take a long time to stabilize to the final output amplitude.

A unique solution to most of these problems is shown in *Figure 18*. A_1 is connected as a two-pole low-pass active filter, and A_2 is connected as an integrator. Since the ultimate phase lag introduced by the amplifiers is 270 degrees, the circuit can be made to oscillate if the loop gain is high enough at the frequency where the lag is 180 degrees. The gain is actually made somewhat higher than is required for oscillation to insure starting. Therefore, the amplitude builds up until it is limited by some nonlinearity in the system.

Amplitude stabilization is accomplished with zener clamp diodes, D_1 and D_2. This does introduce distortion, but it is reduced by the subsequent low pass filters. If D_1 and D_2 have equal breakdown voltages, the resulting symmetrical clipping will virtually eliminate the even-order harmonics. The dominant harmonic is then the third, and this is about 40 dB down at the output of A_1 and about 50 dB down on the output of A_2. This means that the total harmonic distortion on the two outputs is 1 percent and 0.3 percent, respectively.

The frequency of oscillation and the oscillation threshold are determined by R_1, R_2, R_3, C_1, C_2 and C_3. Therefore precision components with low temperature coefficients should be used. If R_3 is made lower than shown, the circuit will accept looser component tolerances before dropping out of oscillation. The start up will also be quicker. However, the price paid is that distortion is increased. The value of R_4 is not critical, but it should be made much smaller than R_2 so that the effective resistance at R_2 does not drop when the clamp diodes conduct.

The output amplitude is determined by the breakdown voltages of D_1 and D_2. Therefore, the clamp level should be temperature compensated for stable operation. Diode-connected (collector shorted to base) NPN transistors with an emitter-base breakdown of about 6.3V work well, as the positive temperature coefficient of the diode in reverse breakdown nearly cancels the negative temperature coefficient of the forward-biased diode. Added advantages of using transistors are that they have less shunt capacitance and sharper breakdowns than conventional zeners.

The LM108 is particularly useful in this circuit at low frequencies, since it permits the use of small capacitors. The circuit shown oscillates at 1 Hz, but uses capacitors in the order of 0.01 μF. This makes it much easier to find temperature-stable precision capacitors. However, some judgment must be used as large value resistors with low temperature coefficients are not exactly easy to come by.*

The LM108s are useful in this circuit for output frequencies up to 1 kHz. Beyond that, better performance can be realized by substituting and LM102A for A_1 and an LM101A with feed-forward compensation for A_2. The improved high-frequency response of these devices extend the operating frequency out to 100 kHz.

capacitance multiplier

Large capacitor values can be eliminated from most systems just by raising the impedance levels, if suitable op amps are available. However, sometimes it is not possible because the impedance levels are already fixed by some element of the system like a low impedance transducer. If this is the case, a capacitance multiplier can be used to increase the effective capacitance of a small capacitor and couple it into a low impedance system.

Previously, IC op amps could not be used effectively as capacitance multipliers because the equivalent leakages generated due to offset current were significantly greater than the leakages of large tantalum capacitors, With the LM108, this has changed. The circuit shown in *Figure 19* generates an equivalent capacitance of 100,000 μF with a worst case leakage of 8 μA—over a −55°C to 125°C temperature range.

*Large-value resistors are available from Victoreen Instrument, Cleveland, Ohio and Pyrofilm Resistor Co., Whippany, New Jersey.

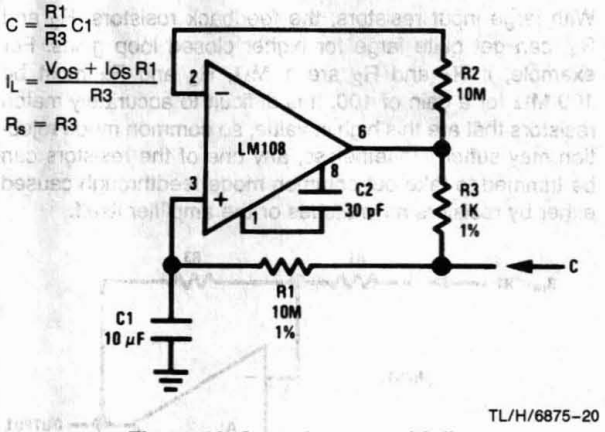

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Figure 19. Capacitance multiplier

The performance of the circuit is described by the equations given in *Figure 19*, where C is the effective output capacitance, I_L is the leakage current of this capacitance and R_S is the series resistance of the multiplied capacitance. The series resistance is relatively high, so high-Q capacitors cannot be realized. Hence, such applications as tuned circuits and filters are ruled out. However, the multiplier can still be used in timing circuits or servo compensation networks where some resistance is usually connected in series with the capacitor or the effect of the resistance can be compensated for.

One final point is that the leakage current of the multiplied capacitance is not a function of the applied voltage. It persists even with no voltage on the output. Therefore, it can generate offset errors in a circuit, rather than the scaling errors caused by conventional capacitors.

instrumentation amplifier

In many instrumentation applications there is frequently a need for an amplifier with a high-impedance differential input and a single ended output. Obvious uses for this are amplifiers for bridge-type signal sources such as strain gages, temperature sensors or pressure transducers. General purpose op amps have satisfactory input characteristics, but feedback must be added to determine the effective gain. And the addition of feedback can drastically reduce the input resistance and degrade common mode rejection.

Figure 20 shows the classical op amp circuit for a differential amplifier. This circuit has three main disadvantages. First, the input resistance on the inverting input is relatively low, being equal to R_1. Second, there usually is a large difference in the input resistance of the two inputs, as is indicated by the equations on the schematic. Third, the common mode rejection is greatly affected by resistor matching and by balancing of the source resistances. A 1-percent deviation in any one of the resistor values reduces the common mode rejection to 46 dB for a closed loop gain of 1, to 60 dB for a gain of 10 and to 80 dB for a gain of 100.

Clearly, the only way to get high input impedance is to use very large resistors in the feedback network. The op amp must operate from a source resistance which is orders of magnitude larger than the resistance of the signal source. Older IC op amps introduced excessive offset and drift when operating from higher resistances and could not be used successfully. The LM108, however, is relatively unaffected by the large resistors, so this approach can sometimes be employed.

With large input resistors, the feedback resistors, R_3 and R_4, can get quite large for higher closed loop gains. For example, if R_1 and R_2 are 1 MΩ, R_3 and R_4 must be 100 MΩ for a gain of 100. It is difficult to accurately match resistors that are this high in value, so common mode rejection may suffer. Nonetheless, any one of the resistors can be trimmed to take out common mode feedthrough caused either by resistors mismatches or the amplifier itself.

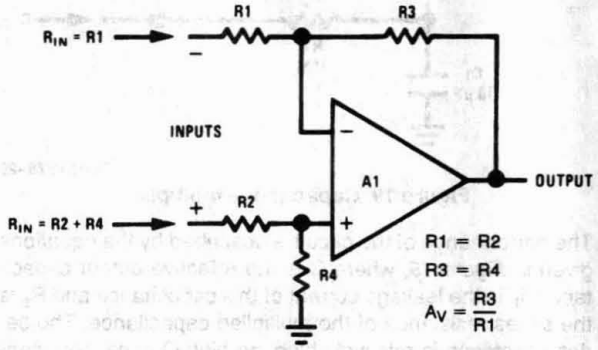

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Figure 20. Feedback connection for a differential amplifier

Another problem caused by large feedback resistors is that stray capacitance can seriously affect the high frequency common mode rejection. With 1 MΩ input resistors, a 1 pF mismatch in stray capacitance from either input to ground can drop the common mode rejection to 40 dB at 1500 Hz. The high frequency rejection can be improved at the expense of frequency response by shunting R_3 and R_4 with matched capacitors.

With high impedance bridges, the feedback resistances become prohibitively large even for the LM108, so the circuit in *Figure 20* cannot be used. One possible alternative is shown in *Figure 21*. R_2 and R_3 are chosen so that their equivalent parallel resistance is equal to R_1. Hence, the output of the amplifier will be zero when the bridge is balanced.

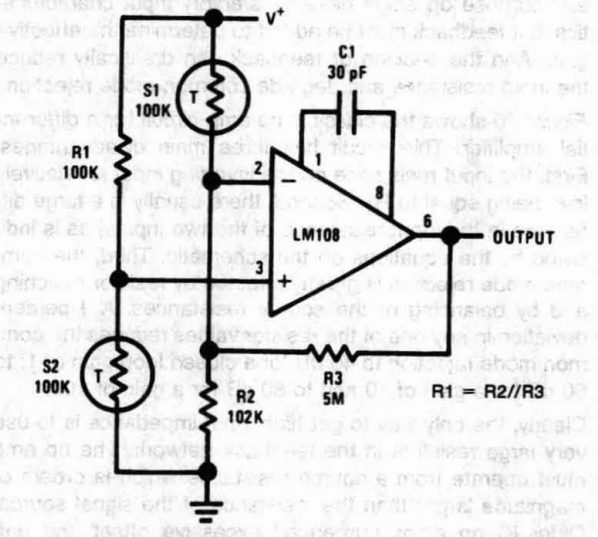

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Figure 21. Amplifier for bridge transducers

When the bridge goes off balance, the op amp maintains the voltage between its input terminals at zero with current fed back from the output through R_3. This circuit does not act like a true differential amplifier for large imbalances in the bridge. The voltage drops across the two sensor resistors, S_1 and S_2, become unequal as the bridge goes off balance, causing some non-linearity in the transfer function. However, this is not usually objectionable for small signal swings.

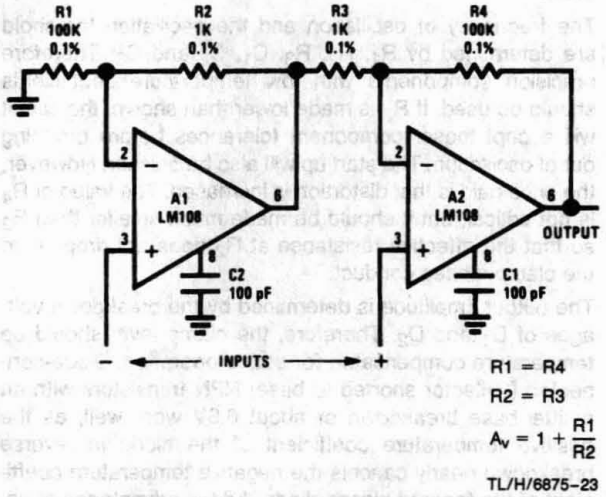

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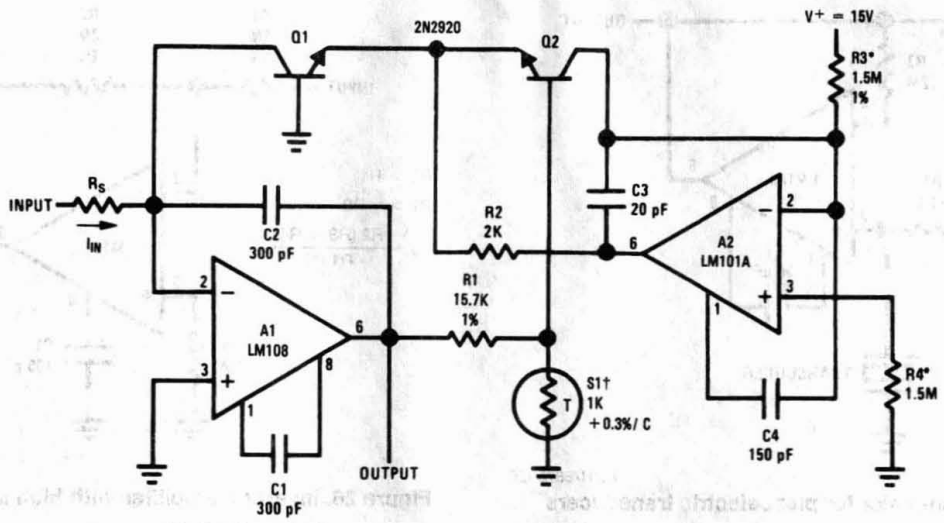
Figure 22. Differential input instrumentation amplifier

Figure 22 shows a true differential connection that has few of the problems mentioned previously. It has an input resistance greater than $10^{10}\Omega$, yet it does not need large resistors in the feedback circuitry. With the component values shown, A_1 is connected as a non-inverting amplifier with a gain of 1.01; and it feeds into A_2 which has an inverting gain of 100. Hence, the total gain from the input of A_1 to the output of A_2 is 101, which is equal to the non-inverting gain of A_2. If all the resistors are matched, the circuit responds only to the differential input signal—not the common mode voltage.

This circuit has the same sensitivity to resistor matching as the previous circuits, with a 1 percent mismatch between two resistors lowering the common mode rejection to 80 dB. However, matching is more easily accomplished because of the lower resistor values. Further, the high frequency common mode rejection is less affected by stray capacitances. The high frequency rejection is limited, though, by the response of A_1

logarithmic converter

A logarithmic amplifier is another circuit that can take advantage of the low input current of an op amp to increase dynamic range. Most practical log converters make use of the logarithmic relationship between the emitter-base voltage of standard double-diffused transistors and their collector current. This logarithmic characteristic has been proven true for over 9 decades of collector current. The only problem involved in using transistors as logging elements is that the scale factor has a temperature sensitivity of 0.3 percent/°C. However, temperature compensating resistors have been developed to compensate for this characteristic, making possible log converters that are accurate over a wide temperature range.



$10\ nA < I_{IN} < 1\ mA$

Sensitivity is 1V per decade.

TL/H/6875–24

†1 kΩ (±1%) at 25°C, +3500 ppm/°C. Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

*Determines current for zero crossing on output: 10 μA as shown.

Figure 23. Temperature compensated one-quadrant logarithmic converter

Figure 23 gives a circuit that uses these techniques. Q_1 is the logging transistor, while Q_2 provides a fixed offset to temperature compensate the emitter-base turn on voltage of Q_1. Q_2 is operated at a fixed collector current of 10 μA by A_2, and its emitter-base voltage is subtracted from that of Q_1 in determining the output voltage of the circuit. The collector current of Q_2 is established by R_3 and V^+ through A_2.

The collector current of Q_1 is proportional to the input current through R_s and, therefore, proportional to the input voltage. The emitter-base voltage of Q_1 varies as the log of the input voltage. The fixed emitter-base voltage of Q_2 subtracts from the voltage on the emitter of Q_1 in determining the voltage on the top end of the temperature-compensating resistor, S_1.

The signal on the top of S_1 will be zero when the input current is equal to the current through R_3 at any temperature. Further, this voltage will vary logarithmically for changes in input current, although the scale factor will have a temperature coefficient of −0.3%/°C. The output of the converter is essentially multiplied by the ratio of R_1 to S_1. Since S_1 has a positive temperature coefficient of 0.3 percent/°C, it compensates for the change in scale factor with temperature.

In this circuit, an LM101A with feedforward compensation is used for A_2 since it is much faster than the LM108 used for A_1. Since both amplifiers are cascaded in the overall feedback loop, the reduced phase shift through A_2 insures stability.

Certain things must be considered in designing this circuit. For one, the sensitivity can be changed by varying R_1. But R_1 must be made considerably larger than the resistance of S_1 for effective temperature compensation of the scale factor. Q_1 and Q_2 should also be matched devices in the same package, and S_1 should be at the same temperature as these transistors. Accuracy for low input currents is determined by the error caused by the bias current of A_1. At high currents, the behavior of Q_1 and Q_2 limits accuracy. For input currents approaching 1 mA, the 2N2920 develops logging errors in excess of 1 percent. If larger input currents are anticipated, bigger transistors must be used; and R_2 should be reduced to insure that A_2 does not saturate.

transducer amplifiers

With certain transducers, accuracy depends on the choice of the circuit configuration as much as it does on the quality of the components. The amplifier for photodiode sensors, shown in *Figure 24*, illustrates this point. Normally, photodiodes are operated with reverse voltage across the junction. At high temperatures, the leakage currents can approach the signal current. However, photodiodes deliver a short-circuit output current, unaffected by leakage currents, which is not significantly lower than the output current with reverse bias.

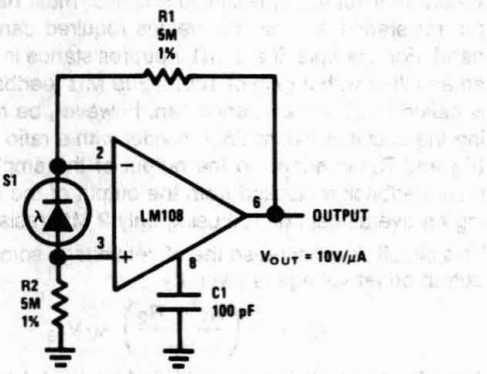


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Figure 24. Amplifier for photodiode sensor

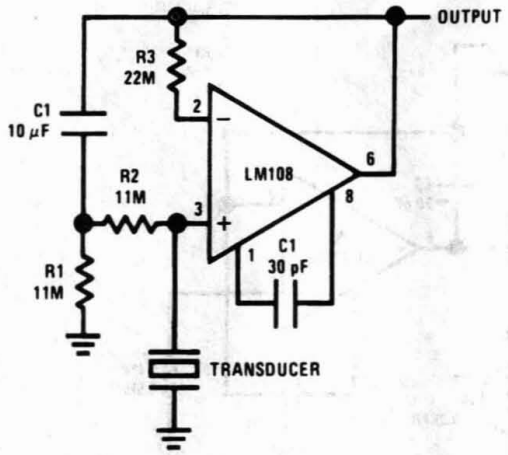

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Figure 25. Amplifier for piezoelectric transducers

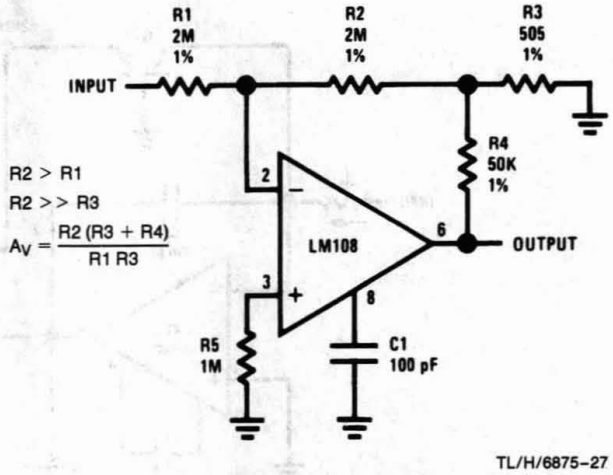

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Figure 26. Inverting amplifier with high input resistance

The circuit shown in *Figure 24* responds to the short-circuit output current of the photodiode. Since the voltage across the diode is only the offset voltage of the amplifier, inherent leakage is reduced by at least two orders of magnitude. Neglecting the offset current of the amplifier, the output current of the sensor is multiplied by R_1 plus R_2 in determining the output voltage.

Figure 25 shows an amplifier for high-impedance ac transducers like a piezoelectric accelerometer. These sensors normally require a high-input-resistance amplifier. The LM108 can provide input resistances in the range of 10 to 100 MΩ, using conventional circuitry. However, conventional designs are sometimes ruled out either because large resistors cannot be used or because prohibitively large input resistances are needed.

Using the circuit in *Figure 25*, input resistances that are orders of magnitude greater than the values of the dc return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency of a capacitive transducer is determined more by the RC product of R_1 and C_1 than it is by resistor values and the equivalent capacitance of the transducer.

resistance multiplication

When an inverting operational amplifier must have high input resistance, the resistor values required can get out of hand. For example, if a 2 MΩ input resistance is needed for an amplifier with a gain of 100, a 200 MΩ feedback resistor is called for. This resistance can, however, be reduced using the circuit in *Figure 26*. A divider with a ratio of 100 to 1 (R_3 and R_4) is added to the output of the amplifier: Unity-gain feedback is applied from the output of the divider, giving an overall gain of 100 using only 2 MΩ resistors.

This circuit does increase the offset voltage somewhat. The output offset voltage is given by

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_2}\right) A_V V_{os}.$$

The offset voltage is only multiplied by $A_V + 1$ in a conventional inverter. Therefore, the circuit in *Figure 26* multiplies the offset by 200, instead of 101. This multiplication factor can be reduced to 110 by increasing R_2 to 20 MΩ and R_3 to 5.55k.

Another disadvantage of the circuit is that four resistors determine the gain, instead of two. Hence, for a given resistor tolerance, the worst-case gain deviation is greater, although this is probably more than offset by the ease of getting better tolerances in the low resistor values.

current sources

Although there are numerous ways to make current sources with op amps, most have limitations as far as their application is concerned. *Figure 27*, however, shows a current source which is fairly flexible and has few restrictions as far as its use is concerned. It supplies a current that is proportional to the input voltage and drives a load referred to ground or any voltage within the output-swing capability of the amplifier.

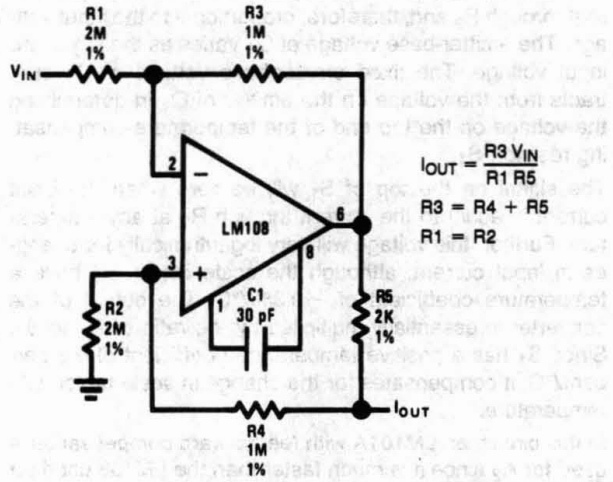

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Figure 27. Bilateral current source

With the output grounded, it is relatively obvious that the output current will be determined by R_5 and the gain setting of the op amp, yielding

$$I_{OUT} = -\frac{R_3 V_{IN}}{R_1 R_5}.$$

When the output is not at zero, it would seem that the current through R_2 and R_4 would reduce accuracy. Nonetheless, if $R_1 = R_2$ and $R_3 = R_4 + R_5$, the output current will

be independent of the output voltage. For $R_1 + R_3 \gg R_5$, the output resistance of the circuit is given by

$$R_{OUT} \cong R_5 \left(\frac{R}{\Delta R}\right)$$

where R is any one of the feedback resistors (R_1, R_2, R_3 or R_4) and ΔR is the incremental change in the resistor value from design center. Hence, for the circuit in *Figure 27*, a 1 percent deviation in one of the resistor values will drop the output resistance to 200 kΩ. Such errors can be trimmed out by adjusting one of the feedback resistors. In design, it is advisable to make the feedback resistors as large as possible. Otherwise, resistor tolerances become even more critical.

The circuit must be driven from a source resistance which is low by comparison to R_1, since this resistance will imbalance the circuit and affect both gain and output resistance. As shown, the circuit gives a negative output current for a positive input voltage. This can be reversed by grounding the input and driving the ground end of R_2. The magnitude of the scale factor will be unchanged as long as $R_4 \gg R_5$.

voltage comparators

Like most op amps, it is possible to use the LM108 as a voltage comparator. *Figure 28* shows the device used as a simple zero-crossing detector. The inputs of the IC are protected internally by back-to-back diodes connected between them, therefore, voltages in excess of 1V cannot be impressed directly across the inputs. This problem is taken care of by R_1 which limits the current so that input voltages in excess of 1 kV can be tolerated. If absolute accuracy is required or if R_1 is made much larger than 1 MΩ, a compensating resistor of equal value should be inserted in series with the other input.

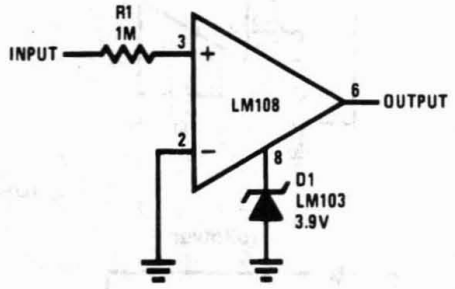

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Figure 28. Zero crossing detector

In *Figure 28*, the output of the op amp is clamped so that it can drive DTL or TTL directly. This is accomplished with a clamp diode on pin 8. When the output swings positive, it is clamped at the breakdown voltage of the zener. When it swings negative, it is clamped at a diode drop below ground. If the 5V logic supply is used as a positive supply for the amplifier, the zener can be replaced with an ordinary silicon diode. The maximum fan out that can be handled by the device is one for standard DTL or TTL under worst case conditions.

As might be expected, the LM108 is not very fast when used as a comparator. The response time is up in the tens of microseconds. An LM103[11] is recommended for D_1, rather than a conventional alloy zener, because it has lower capacitance and will not slow the circuit further. The sharp breakdown of the LM103 at low currents is also an advantage as the current through the diode in clamp is only 10 μA.

Figure 29 shows a comparator for voltages of opposite polarity. The output changes state when the voltage on the junction of R_1 and R_2 is equal to V_{TH}. Mathematically, this is expressed by

$$V_{TH} = V_2 + \frac{R_2 (V_1 - V_2)}{R_1 + R_2}.$$

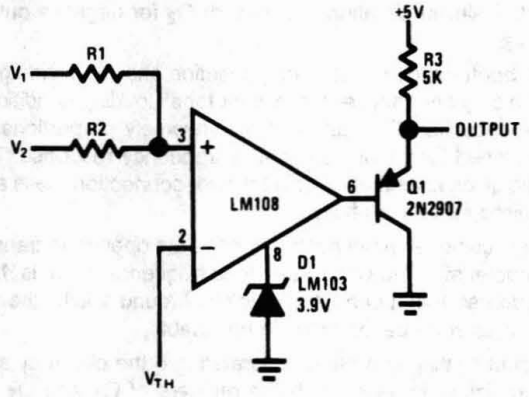

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Figure 29. Voltage comparator with output buffer

The LM108 can also be used as a differential comparator, going through a transition when two input voltages are equal. However, resistors must be inserted in series with the inputs to limit current and minimize loading on the signal sources when the input-protection diodes conduct. *Figure 29* also shows how a PNP transistor can be added on the output to increase the fan out to about 20 with standard DTL or TTL.

power booster

The LM108, which was designed for low power consumption, is not able to drive heavy loads. However, a relatively simple booster can be added to the output to increase the output current to ±50 mA. This circuit, shown in *Figure 30*, has the added advantage that it swings the output up to the supplies, within a fraction of a volt. The increased voltage swing is particularly helpful in low voltage circuits.

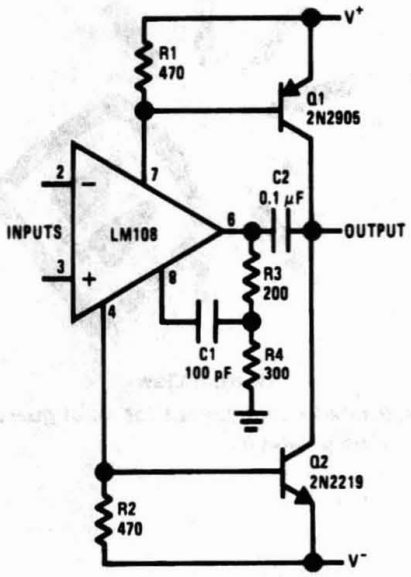

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Figure 30. Power booster

In *Figure 30*, the output transistors are driven from the supply leads of the op amp. It is important that R_1 and R_2 be made low enough so Q_1 and Q_2 are not turned on by the *worst case* quiescent current of the amplifier. The output of the op amp is loaded heavily to ground with R_3 and R_4.

When the output swings about 0.5V positive, the increasing positive supply current will turn on Q_1 which pulls up the load. A similar situation occurs with Q_2 for negative output swings.

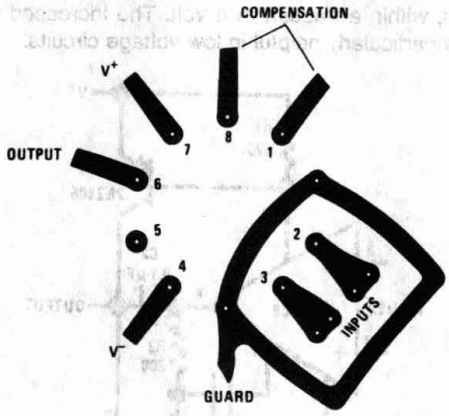
The bootstrapped shunt compensation shown in the figure is the only one that seems to work for all loading conditions. This capacitor, C_1, can be made inversely proportional to the closed loop gain to optimize frequency response. The value given is for a unity-gain follower connection. C_2 is also required for loop stability.

The circuit does have a dead zone in the open loop transfer characteristic. However, the low frequency gain is high enough so that it can be neglected. Around 1 kHz, though, the dead zone becomes quite noticeable.

Current limiting can be incorporated into the circuit by adding resistors in series with the emitters of Q_1 and Q_2 because the short circuit protection of the LM108 limits the maximum voltage drop across R_1 and R_2.

board construction

As indicated previously, certain precautions must be observed when building circuits that are sensitive to very low currents. If proper care is not taken, board leakage currents can easily become much larger than the error currents of the op amp. To prevent this, it is necessary to thoroughly clean printed circuit boards. Even experimental breadboards must be cleaned with trichloroethlene or alcohol to remove solder fluxes, and blown dry with compressed air. These fluxes may be insulators at low impedance levels—like in electric motors—but they certainly are not in high impedance circuits. In addition to causing gross errors, their presence can make the circuit behave erratically, especially as the temperature is changed.



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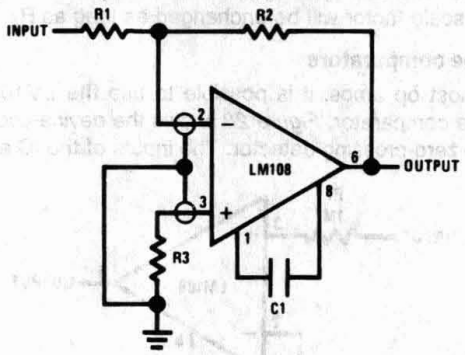
Bottom View

Figure 31. Printed circuit layout for input guarding with TO-5 package

At elevated temperatures, even the leakage of clean boards can be a headache. At 125°C the leakage resistance between adjacent runs on a printed circuit board is about $10^{11}\Omega$ (0.05-inch separation parallel for 1 inch) for high quality epoxy-glass boards that have been properly cleaned. Therefore, the boards can easily produce error currents in the order of 200 pA and much more if they become contaminated. Conservative practice dictates that the boards be coated with epoxy or silicone rubber after cleaning to prevent contamination. Silicone rubber is the easiest to use. However, if the better durability of epoxy is needed, care must be taken to make sure that it gets thoroughly cured. Otherwise, the epoxy will make high temperature leakage much worse.

Care must also be exercised to insure that the circuit board is protected from condensed water vapor when operating in the vicinity of 0°C. This can usually be accomplished by coating the board as mentioned above.

a. inverting amplifier



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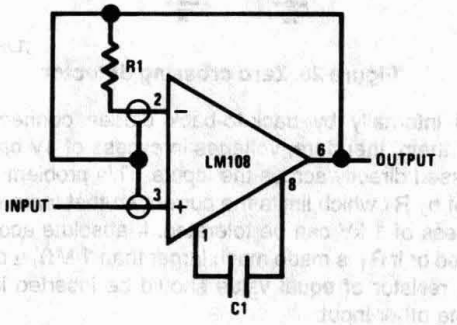
b. follower



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c. non-inverting amplifier

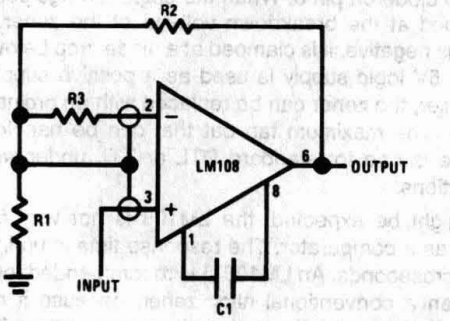

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Figure 32. Connection of input guards

guarding

Even with properly cleaned and coated boards, leakage currents are on the verge of causing trouble at 125°C. The standard pin configuration of most IC op amps has the input pins adjacent to pins which are at the supply potentials. Therefore, it is advisable to employ guarding to reduce the voltage difference between the inputs and adjacent metal runs.

A board layout that includes input guarding is shown in *Figure 31* for the eight lead TO-5 package. A ten-lead pin circle is used, and the leads of the IC are formed so that the holes adjacent to the inputs are vacant when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is then connected to a low impedance point that is at the same potential as the inputs. The leakage currents from the pins at the supply potentials are absorbed by the guard. The voltage difference between the guard and the inputs can be made approximately equal to the offset voltage, reducing the effective leakage by more than three orders of magnitude. If the leads of the integrated circuit, or other components connected to the input, go through the board, it may be necessary to guard both sides.

Figure 32 shows how the guard is commited on the more-common op amp circuits. With an integrator or inverting amplifier, where the inputs are close to ground potential, the guard is simply grounded. With the voltage follower, the guard is bootstrapped to the output. If it is desirable to put a resistor in the inverting input to compensate for the source resistance, it is connected as shown in *Figure 32b*.

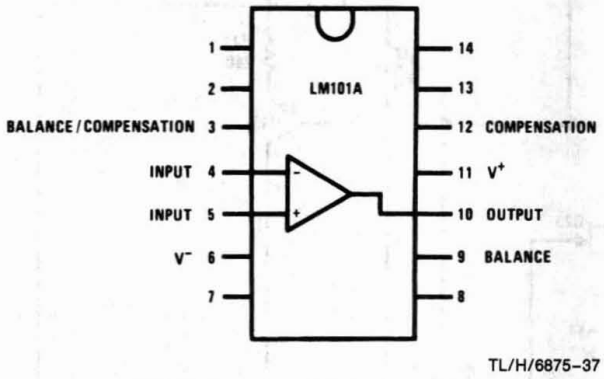
Guarding a non-inverting amplifier is a little more complicated. A low impedance point must be created by using relatively low value feedback resistors to determine the gain (R_1 and R_2 in *Figure 32c*). The guard is then connected to the junction of the feedback resistors. A resistor, R_3, can be connected as shown in the figure to compensate for large source resistances.

With the dual-in-line and flat packages, it is far more difficult to guard the inputs, if the standard pin configuration of the LM709 or LM101A is used, because the pin spacings on these packages are fixed. Therefore, the pin configuration of the LM108 was changed, as shown in *Figure 33*.

conclusions

IC op amps are now available that equal the input current specifications of FET amplifiers in all but the most restricted temperature range applications. At operating temperatures above 85°C, the IC is clearly superior as it uses bipolar transistors that make it possible to eliminate the leakage currents that plague FETs. Additionally, bipolar transistors match better than FETs, so low offset voltage and drifts can be obtained without expensive adjustments or selection. Further, the bipolar devices lend themselves more readily to low-cost monolithic construction.

These amplifiers open up new application areas and vastly improve performance in others. For example, in analog memories, holding intervals can be extended to minutes, even where −55°C to 125°C operation is involved. Instrumentation amplifiers and low frequency waveform generators also benefit from the low error currents.



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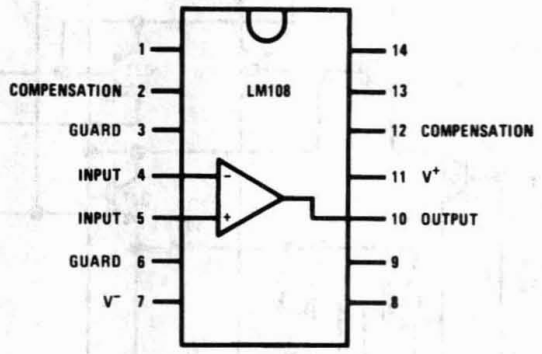
NOTE: Pin 6 connected to bottom of package.

Top View



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NOTE: Pin 7 connected to bottom of package

Top View

Figure 33. Comparing connection diagrams of the LM101A and LM108, showing addition of guarding

When operating above 85°C, overall performance is frequently limited by components other than the op amp, unless certain precautions are observed. It is generally necessary to redesign circuits using semiconductor switches to reduce the effect of their leakage currents. Further, high quality capacitors must be used, and care must be exercised in selecting large value resistors. Printed circuit board leakages can also be troublesome unless the boards are properly treated. And above 100°C, it is almost mandatory to employ guarding on the boards to protect the inputs, if the full potential of the amplifier is to be realized.

appendix

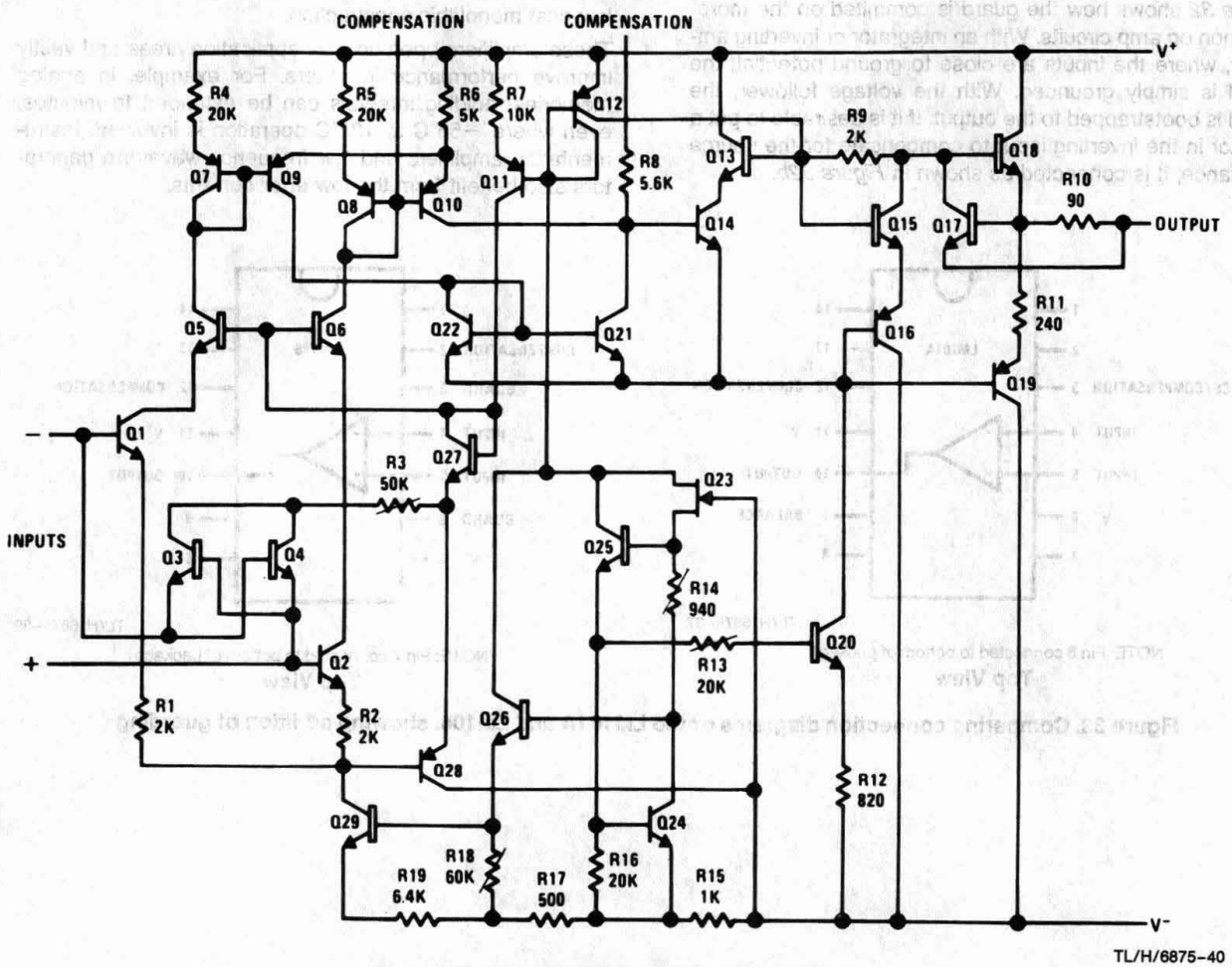
A complete schematic of the LM108 is given in *Figure A1*. A description of the basic circuit is presented along with a simplified schematic earlier in the text. The purpose of this Appendix is to explain some of the more subtle features of the design.

The current source supplying the input transistors is Q_{29}. It is designed to supply a total input stage current of 6 μA at 25°C. This current drops to 3 μA at −55°C but increases to only 7.5 μA at 125°C. This temperature characteristic tends to compensate for the current gain falloff of the input transistors at low temperatures without creating stability problems at high temperatures.

The biasing circuitry for the input current source is nearly identical to that in the LM101A, and a complete description is given in Reference 4. However, a brief explanation follows.

A collector FET,[6] Q_{23}, which has a saturation current of about 30 μA, establishes the collector current of Q_{24}. This FET provides the initial turn-on current for the circuit and insures starting under all conditions. The purpose of R_{14} is to compensate for production and temperature variations in the FET current. It is a collector resistor (indicated by the T through it) made of the same semiconductor material as the FET channel. As the FET current varies, the drop across R_{14} tends to compensate for changes in the emitter base voltage of Q_{24}.

The collector-emitter voltage of Q_{24} is equal to the emitter base voltage of Q_{24} plus that of Q_{25}. This voltage is delivered to Q_{26} and Q_{29}. Q_{25} and Q_{24} are operated at substantially higher currents than Q_{26} and Q_{29}. Hence, there is a



TL/H/6875–40

Figure A1. Complete schematic of the LM108

differential in their emitter base voltages that is dropped across R_{19} to determine the input stage current. R_{18} is a pinched base resistor, as is indicated by the slash bar through it. This resistor, which has a large positive temperature coefficient, operates in conjunction with R_{17} to help shape the temperature characteristics of the input stage current source.

The output currents of Q_{26}, Q_{25}, and Q_{23} are fed to Q_{12}, which is a controlled-gain lateral PNP.[6] It delivers one-half of the combined currents to the output stage. Q_{11} is also connected to Q_{12}, with its output current set at approximately 15 μA by R_7. Since this type of current source makes use of the emitter-base voltage differential between similar transistors operating at different collector currents, the output of Q_{11} is relatively independent of the current delivered to Q_{12}. [12] This current is used for the input stage bootstrapping circuitry.

Q_{20} also supplies current to the class-B output stage. Its output current is determined by the ratio of R_{15} to R_{12} and the current through R_{12}. R_{13} is included so that the biasing circuit is not upset when Q_{20} saturates.

One major departure from the simplified schematic is the bootstrapping of the second stage active loads, Q_{21} and Q_{22}, to the output. This makes the second stage gain dependent only on how well Q_9 and Q_{10} match with variations in output voltage. Hence, the second stage gain is quite high. In fact, the overall gain of the amplifier is typically in excess of 10^6 at dc.

The second stage active loads drive Q_{14}. A high-gain primary transistor is used to prevent loading of the second stage. Its collector is bootstrapped by Q_{13} to operate it at zero collector-base voltage. The class-B output stage is actually driven by the emitter of Q_{14}.

A dead zone in the output stage is prevented by biasing Q_{18} and Q_{19} on the verge of conduction with Q_{15} and Q_{16}. R_9 is used to compensate for the transconductance of Q_{15} and Q_{16}, making the output stage quiescent current relatively independent of the output current of Q_{12}. The drop across this resistor also reduces quiescent current.

For positive-going outputs, short circuit protection is provided by R_{10} and Q_{17}. When the voltage drop across R_{10} turns on Q_{17}, it removes base drive from Q_{18}. For negative-going outputs, current limiting is initiated when the voltage drop across R_{11} becomes large enough for the collector base junction of Q_{17} to become forward biased. When this happens, the base of Q_{19} is clamped so the output current cannot increase further.

Input protection is provided by Q_3 and Q_4 which act as clamp diodes between the inputs. The collectors of these transistors are bootstrapped to the emitter of Q_{28} through R_3. This keeps the collector-isolation leakage of the transistors from showing up on the inputs. R_3 is included so that the bootstrapping is not disrupted when Q_3 or Q_4 saturate with an input overload, Current-limiting resistors were not connected in series with the inputs, since diffused resistors cannot be employed such that they work effectively, without causing high temperature leakages.

TABLE I. Typical Performance of the LM108 Operational Amplifier (T_A = 25°C and V_S = ±15V)

Input Offset Voltage	0.7 mV
Input Offset Current	50 pA
Input Bias Current	0.8 nA
Input Resistance	70 MΩ
Input Common Mode Range	±14V
Common Mode Rejection	100 dB
Offset Voltage Drift	3 μV/°C
Offset Current Drift	0.5 pA/°C
Voltage Gain	300V/mW
Small Signal Bandwidth	1.0 MHz
Slew Rate	0.3V/μs
Output Swing	±14V
Supply Current	300 μA
Power Supply Rejection	100 dB
Operating Voltage Range	±2V to ±20V

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Log Converters

National Semiconductor
Application Note 30

One of the most predictable non-linear elements commonly available is the bipolar transistor. The relationship between collector current and emitter base voltage is precisely logarithmic from currents below one picoamp to currents above one milliamp. Using a matched pair of transistors and integrated circuit operational amplifiers, it is relatively easy to construct a linear to logarithmic converter with a dynamic range in excess of five decades.

The circuit in *Figure 1* generates a logarithmic output voltage for a linear input current. Transistor Q_1 is used as the non-linear feedback element around an LM108 operational amplifier. Negative feedback is applied to the emitter of Q_1 through divider, R_1 and R_2, and the emitter base junction of Q_2. This forces the collector current of Q_1 to be exactly equal to the current through the input resistor. Transistor Q_2 is used as the feedback element of an LM101A operational amplifier. Negative feedback forces the collector current of Q_2 to equal the current through R_3. For the values shown, this current is 10 μA. Since the collector current of Q_2 remains constant, the emitter base voltage also remains constant. Therefore, only the V_{BE} of Q_1 varies with a change of input current. However, the output voltage is a function of the difference in emitter base voltages of Q_1 and Q_2:

$$E_{OUT} = \frac{R_1 + R_2}{R_2}(V_{BE_2} - V_{BE_1}). \qquad (1)$$

For matched transistors operating at different collector currents, the emitter base differential is given by

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C_1}}{I_{C_2}}, \qquad (2)$$

where k is Boltzmann's constant, T is temperature in degrees Kelvin and q is the charge of an electron. Combining these two equations and writing the expression for the output voltage gives

$$E_{OUT} = \frac{-kT}{q}\left[\frac{R_1 + R_2}{R_2}\right] \log_e \left[\frac{E_{IN}\, R_3}{E_{REF}\, R_{IN}}\right] \qquad (3)$$

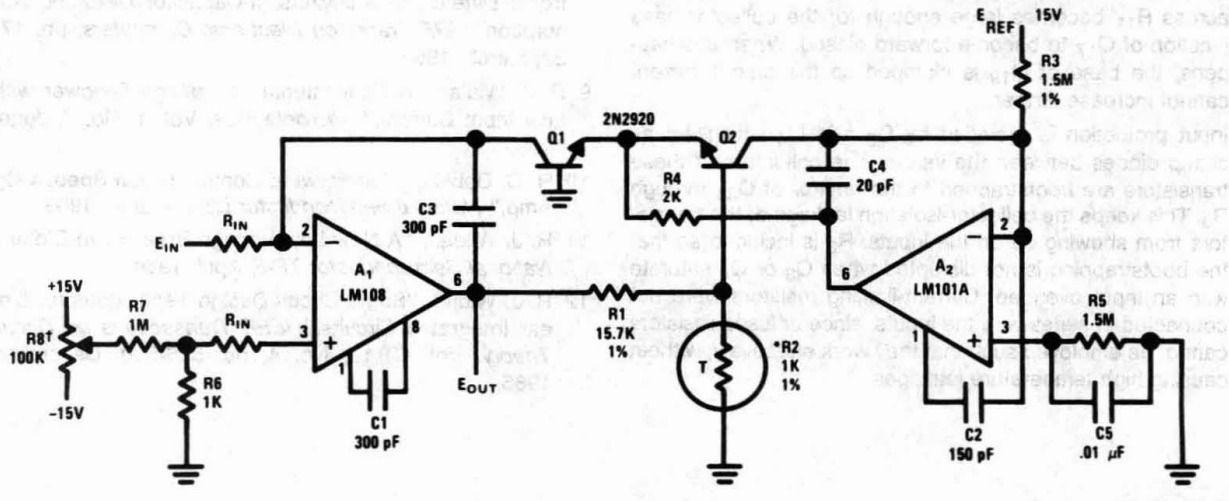
for $E_{IN} \geq 0$. This shows that the output is proportional to the logarithm of the input voltage. The coefficient of the log term is directly proportional to absolute temperature. Without compensation, the scale factor will also vary directly with temperature. However, by making R_2 directly proportional to temperature, constant gain is obtained. The temperature compensation is typically 1% over a temperature range of −25°C to 100°C for the resistor specified. For limited temperature range applications, such as 0°C to 50°C, a 430Ω sensistor in series with a 570Ω resistor may be substituted for the 1k resistor, also with 1% accuracy. The divider, R_1 and R_2, sets the gain while the current through R_3 sets the zero. With the values given, the scale factor is 1V/decade and

$$E_{OUT} = -\left[\log_{10}\left|\frac{E_{IN}}{R_{IN}}\right| + 5\right] \qquad (4)$$

where the absolute value sign indicates that the dimensions of the quantity inside are to be ignored.

Log generator circuits are not limited to inverting operation. In fact, a feature of this circuit is the ease with which non-inverting operation is obtained. Supplying the input signal to A_2 and the reference current to A_1 results in a log output that is not inverted from the input. To achieve the same 100 dB dynamic range in the non-inverting configuration, an LM108 should be used for A_2, and an LM101A for A_1. Since the LM108 cannot use feedforward compensation, it is frequency compensated with the standard 30 pF capacitor.

The only other change is the addition of a clamp diode connected from the emitter of Q_1 to ground. This prevents damage to the logging transistors if the input signal should go negative.



TL/H/7275–1

*1 kΩ (±1%) at 25°C, +3500 ppm/°C.
Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

†Offset Voltage Adjust

FIGURE 1. Log Generator with 100 dB Dynamic Range

The log output is accurate to 1% for any current between 10 nA and 1 mA. This is equivalent to about 3% referred to the input. At currents over 500 μA the transistors used deviate from log characteristics due to resistance in the emitter, while at low currents, the offset current of the LM108 is the major source of error. These errors occur at the ends of the dynamic range, and from 40 nA to 400 μA the log converter is 1% accurate referred to the input. Both of the transistors are used in the grounded base connection, rather than the diode connection, to eliminate errors due to base current. Unfortunately, the grounded base connection increases the loop gain. More frequency compensation is necessary to prevent oscillation, and the log converter is necessarily slow. It may take 1 to 5 ms for the output to settle to 1% of its final value. This is especially true at low currents.

The circuit shown in *Figure 2* is two orders of magnitude faster than the previous circuit and has a dynamic range of 80 dB. Operation is the same as the circuit in *Figure 1*, except the configuration optimizes speed rather than dynamic range. Transistor Q_1 is diode connected to allow the use of feedforward compensation[1] on an LM101A operational amplifier. This compensation extends the bandwidth to 10 MHz and increases the slew rate. To prevent errors due to the finite h_{FE} of Q_1 and the bias current of the LM101A, an LM102 voltage follower buffers the base current and input current. Although the log circuit will operate without the LM102, accuracy will degrade at low input currents. Amplifier A_2 is also compensated for maximum bandwidth. As with the previous log converter, R_1 and R_2 control the sensitivity; and R_3 controls the zero crossing of the transfer function. With the values shown the scale factor is 1V/decade and

$$E_{OUT} = -\left[\log_{10}\left|\frac{E_{IN}}{R_{IN}}\right| + 4\right] \qquad (5)$$

from less than 100 nA to 1 mA.

Anti-log or exponential generation is simply a matter of rearranging the circuitry. *Figure 3* shows the circuitry of the log converter connected to generate an exponential output from a linear input. Amplifier A_1 in conjunction with transistor Q_1 drives the emitter of Q_2 in proportion to the input voltage. The collector current of Q_2 varies exponentially with the emitter-base voltage. This current is converted to a voltage by amplifier A_2. With the values given

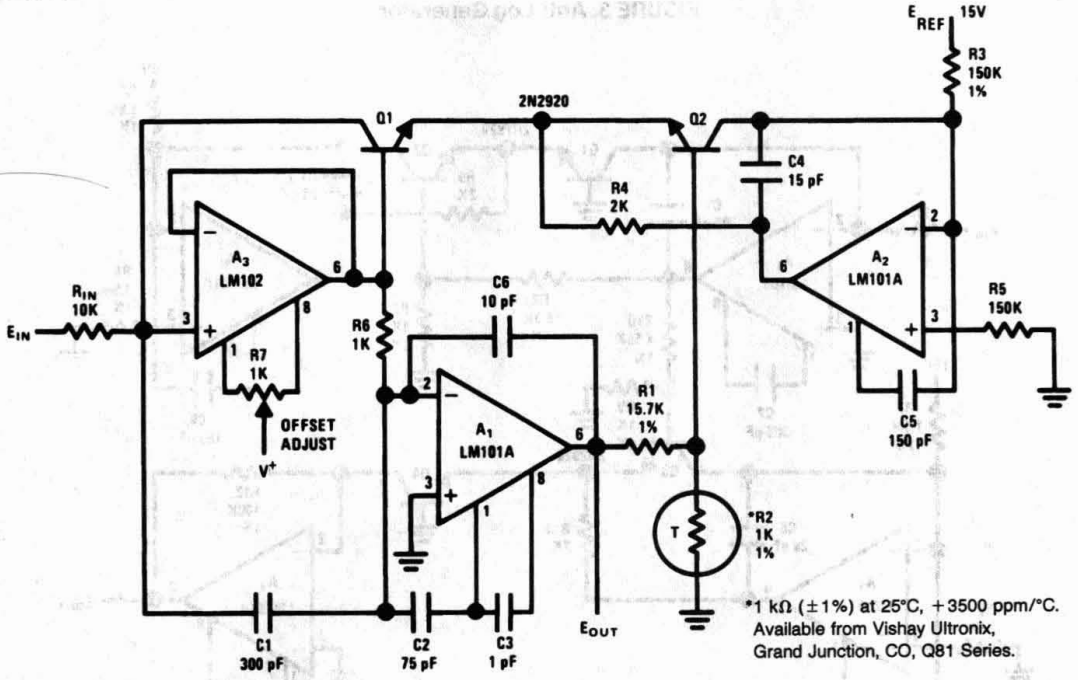
$$E_{OUT} = 10^{-[E_{IN}]}. \qquad (6)$$

Many non-linear functions such as $X^{1/2}$, X^2, X^3, 1/X, XY, and X/Y are easily generated with the use of logs. Multiplication becomes addition, division becomes subtraction and powers become gain coefficients of log terms. *Figure 4* shows a circuit whose output is the cube of the input. Actually, any power function is available from this circuit by changing the values of R_9 and R_{10} in accordance with the expression:

$$E_{OUT} = E_{IN}^{\frac{16.7\,R_9}{R_9 + R_{10}}}. \qquad (7)$$

Note that when log and anti-log circuits are used to perform an operation with a linear output, no temperature compensating resistors at all are needed. If the log and anti-log transistors are at the same temperature, gain changes with temperature cancel. It is a good idea to use a heat sink which couples the two transistors to minimize thermal gradients. A 1°C temperature difference between the log and anti-log transistors results in a 0.3% error. Also, in the log converters, a 1°C difference between the log transistors and the compensating resistor results in a 0.3% error.

Either of the circuits in *Figures 1* or *2* may be used as dividers or reciprocal generators. Equation 3 shows the outputs of the log generators are actually the ratio of two currents:



TL/H/7275–2

FIGURE 2. Fast Log Generator

the input current and the current through R_3. When used as a log generator, the current through R_3 was held constant by connecting R_3 to a fixed voltage. Hence, the output was just the log of the input. If R_3 is driven by an input voltage, rather than the 15V reference, the output of the log generator is the log ratio of the input current to the current through R_3. The anti-log of this voltage is the quotient. Of course, if the divisor is constant, the output is the reciprocal.

A complete one quadrant multiplier/divider is shown in *Figure 5*. It is basically the log generator shown in *Figure 1* driving the anti-log generator shown in *Figure 3*. The log generator output from A_1 drives the base of Q_3 with a voltage proportional to the log of E_1/E_2. Transistor Q_3 adds a voltage proportional to the log of E_3 and drives the anti-log transistor, Q_4. The collector current of Q_4 is converted to an output voltage by A_4 and R_7, with the scale factor set by R_7 at $E_1\ E_3/10E_2$.

Measurement of transistor current gains over a wide range of operating currents is an application particularly suited to log multiplier/dividers. Using the circuit in *Figure 5*, PNP current gains can be measured at currents from 0.4 μA to 1 mA. The collector current is the input signal to A_1, the base current is the input signal to A_2, and a fixed voltage to R_5 sets the scale factor. Since A_2 holds the base at ground, a single resistor from the emitter to the positive supply is all that is needed to establish the operating current. The output is proportional to collector current divided by base current, or h_{FE}.

In addition to their application in performing functional operations, log generators can provide a significant increase in

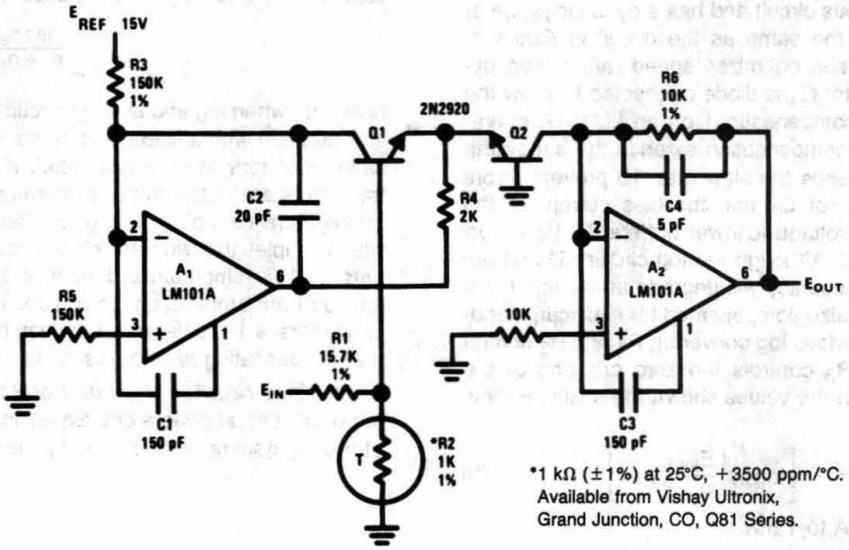


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FIGURE 3. Anti-Log Generator

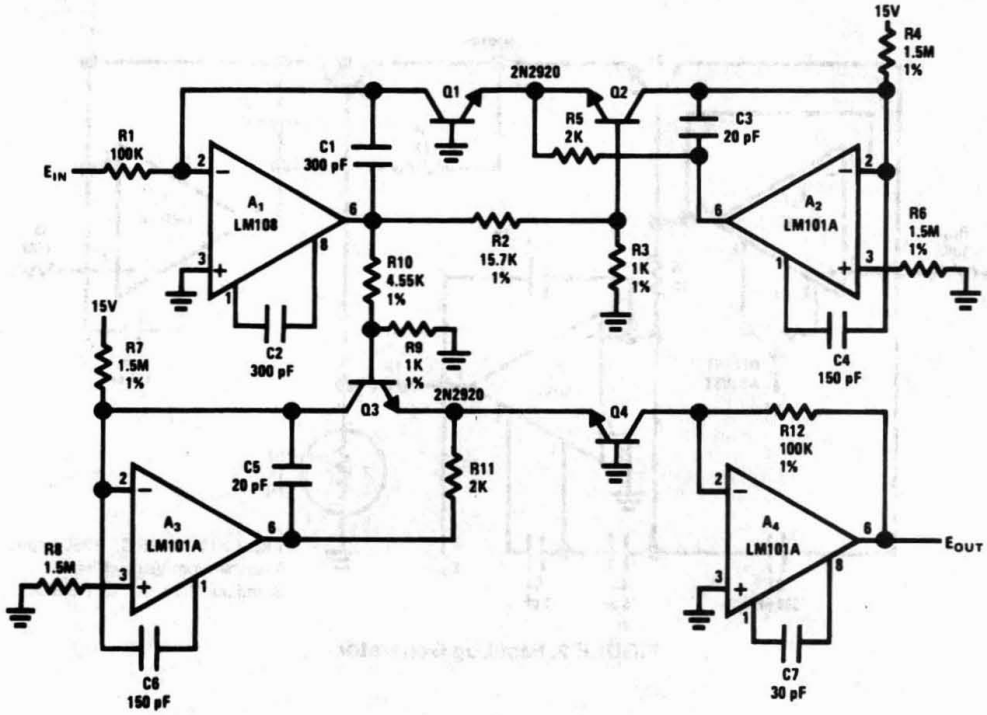

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FIGURE 4. Cube Generator

the dynamic range of signal processing systems. Also, unlike a linear system, there is no loss in accuracy or resolution when the input signal is small compared to full scale. Over most of the dynamic range, the accuracy is a percent-of-signal rather than a percent-of-full-scale. For example, using log generators, a simple meter can display signals with 100 dB dynamic range or an oscilloscope can display a 10 mV and 10V pulse simultaneously. Obviously, without the log generator, the low level signals are completely lost.

To achieve wide dynamic range with high accuracy, the input operational amplifier necessarily must have low offset voltage, bias current and offset current. The LM108 has a maximum bias current of *3 nA* and offset current of *400 pA* over a −55°C to 125°C temperature range. By using equal source resistors, only the offset current of the LM108 causes an error. The offset current of the LM108 is as low as many FET amplifiers. Further, it has a low and constant temperature coefficient rather than doubling every 10°C. This results in greater accuracy over temperature than can be achieved with FET amplifiers. The offset voltage may be zeroed, if necessary, to improve accuracy with low input voltages.

The log converters are low level circuits and some care should be taken during construction. The input leads should be as short as possible and the input circuitry guarded against leakage currents. Solder residues can easily conduct leakage currents, therefore circuit boards should be cleaned before use. High quality glass or mica capacitors should be used on the inputs to minimize leakage currents. Also, when the +15V supply is used as a reference, it must be well regulated.

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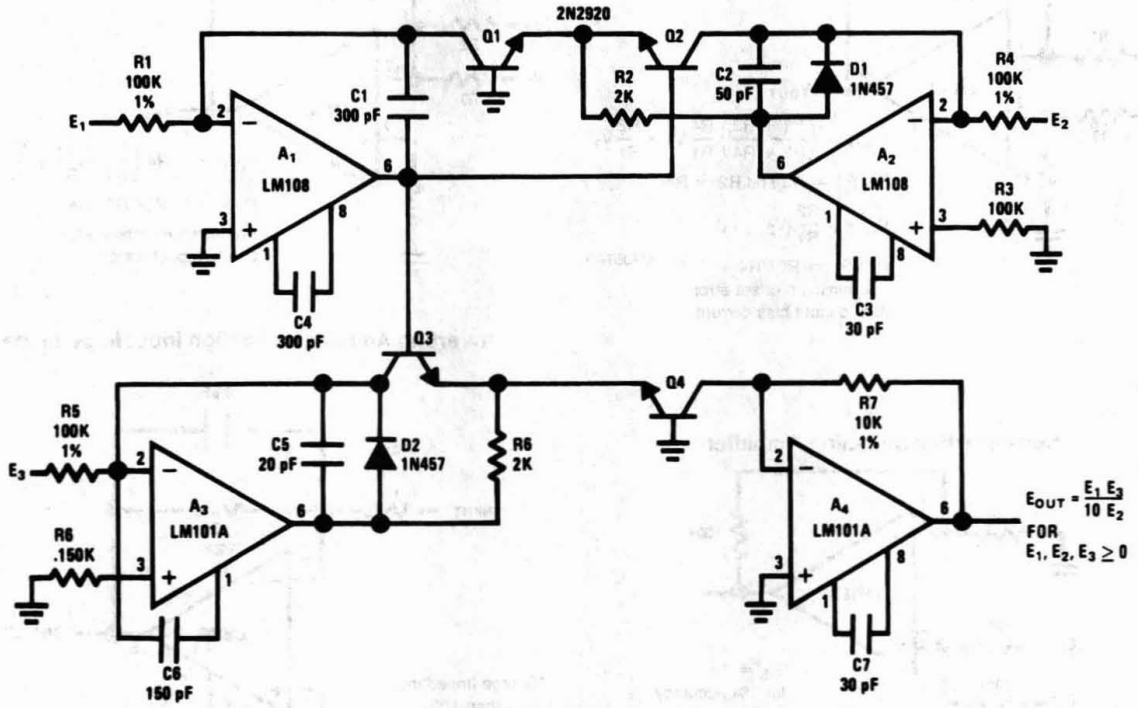

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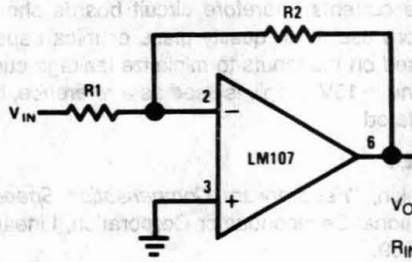
FIGURE 5. Multiplier/Divider

Op Amp Circuit Collection

National Semiconductor
Application Note 31

SECTION 1—BASIC CIRCUITS

Inverting Amplifier



$$V_{OUT} = -\frac{R2}{R1} V_{IN}$$

$$R_{IN} = R1$$

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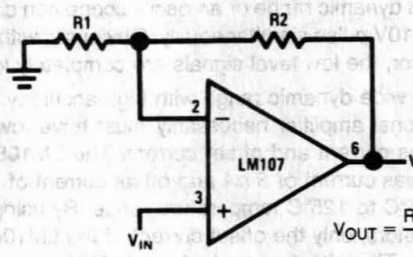
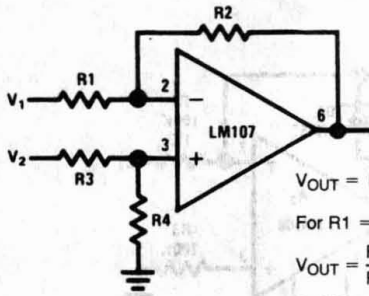
Non-Inverting Amplifier



$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

TL/H/7057-2

Difference Amplifier



$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1} V_2 - \frac{R2}{R1} V_1$$

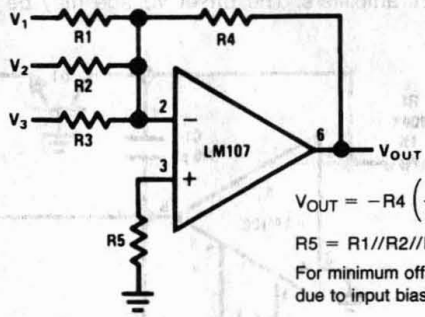
For R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}(V_2 - V_1)$$

R1//R2 = R3//R4
For minimum offset error due to input bias current

TL/H/7057-3

Inverting Summing Amplifier

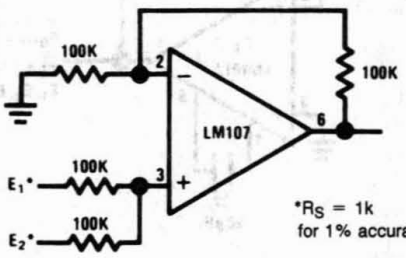


$$V_{OUT} = -R4\left(\frac{V_1}{R1} + \frac{V_2}{R2} + \frac{V_3}{R3}\right)$$

R5 = R1//R2//R3//R4
For minimum offset error due to input bias current

TL/H/7057-4

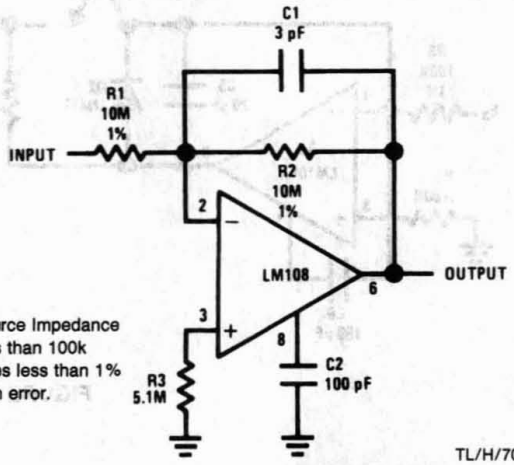
Non-Inverting Summing Amplifier



*R_S = 1k for 1% accuracy

TL/H/7057-5

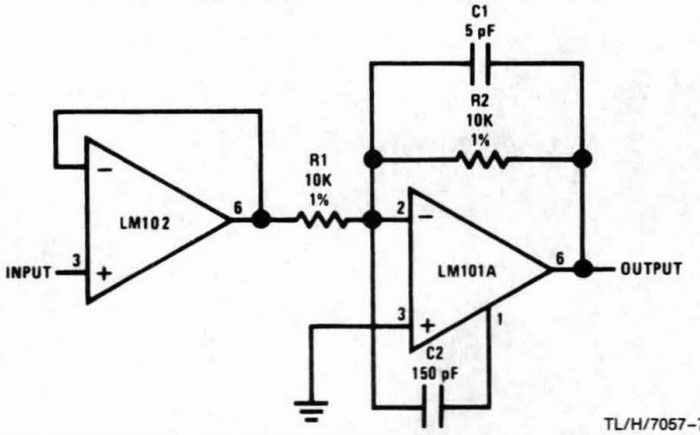
Inverting Amplifier with High Input Impedance



*Source Impedance less than 100k gives less than 1% gain error.

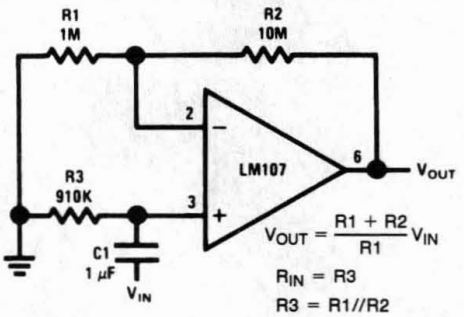
TL/H/7057-6

Fast Inverting Amplifier with High Input Impedance



TL/H/7057-7

Non-Inverting AC Amplifier



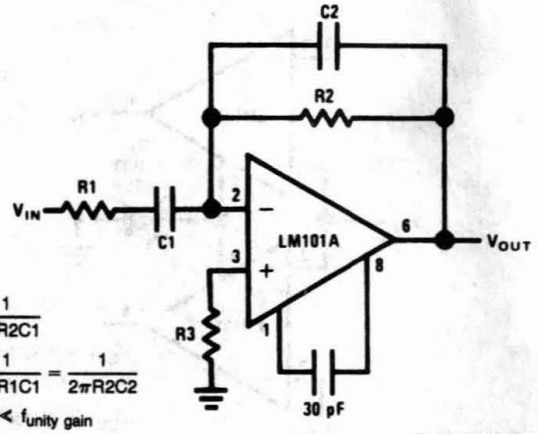
$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

$$R_{IN} = R3$$

$$R3 = R1//R2$$

TL/H/7057-8

Practical Differentiator



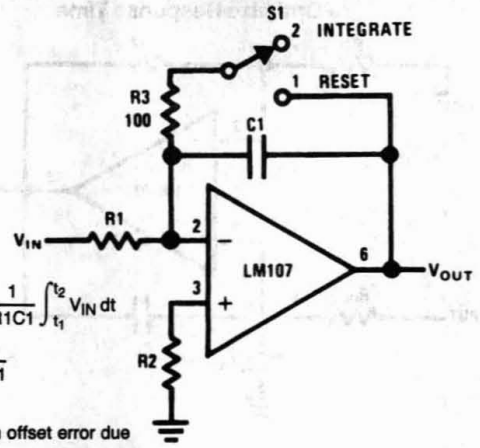
$$f_c = \frac{1}{2\pi R2C1}$$

$$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

$f_c < f_h < f_{unity\ gain}$

TL/H/7057–9

Integrator



$$V_{OUT} = -\frac{1}{R1C1}\int_{t_1}^{t_2} V_{IN}\,dt$$

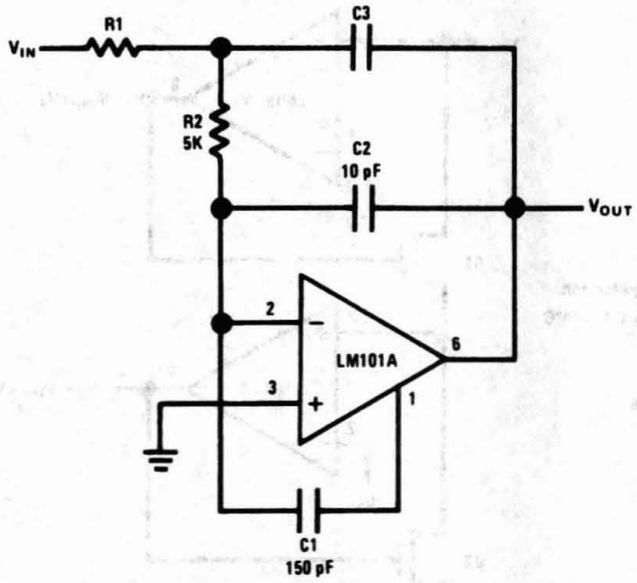
$$f_c = \frac{1}{2\pi R1C1}$$

$R1 = R2$

For minimum offset error due to input bias current

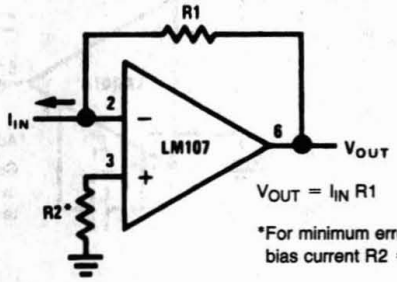
TL/H/7057–10

Fast Integrator



TL/H/7057–11

Current to Voltage Converter

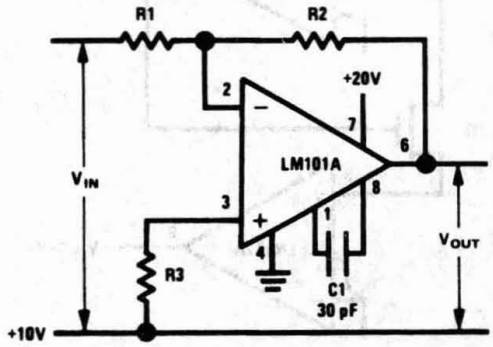


$$V_{OUT} = I_{IN}\,R1$$

*For minimum error due to bias current R2 = R1

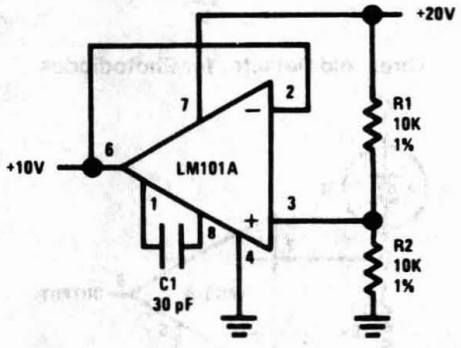
TL/H/7057–12

Circuit for Operating the LM101 without a Negative Supply



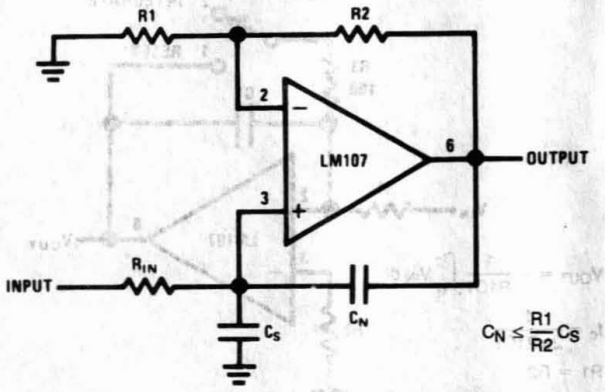
TL/H/7057–13

Circuit for Generating the Second Positive Voltage



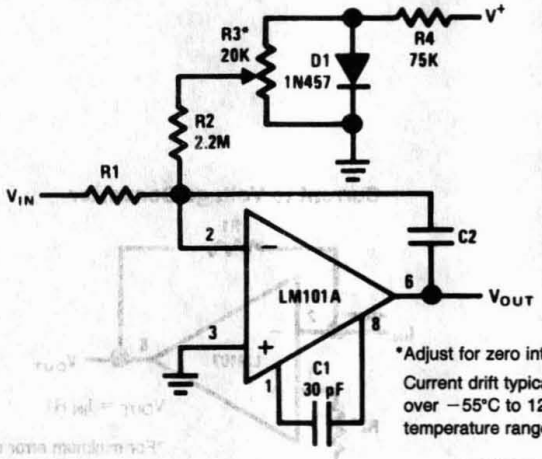
TL/H/7057–14

Neutralizing Input Capacitance to Optimize Response Time



TL/H/7057–15

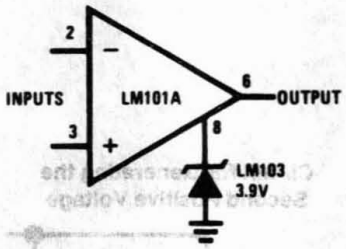
Integrator with Bias Current Compensation



*Adjust for zero integrator drift. Current drift typically 0.1, n/A°C over −55°C to 125°C temperature range.

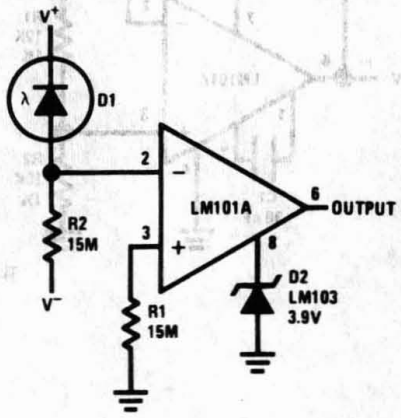
TL/H/7057–16

Voltage Comparator for Driving DTL or TTL Integrated Circuits



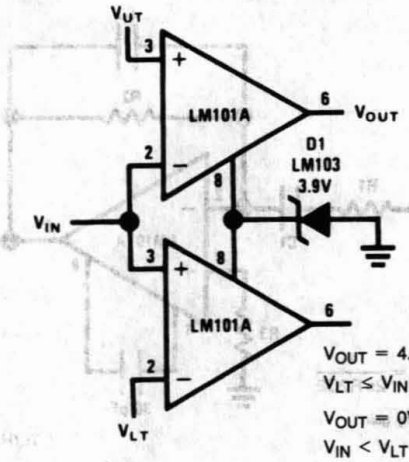
TL/H/7057–17

Threshold Detector for Photodiodes



TL/H/7057–18

Double-Ended Limit Detector

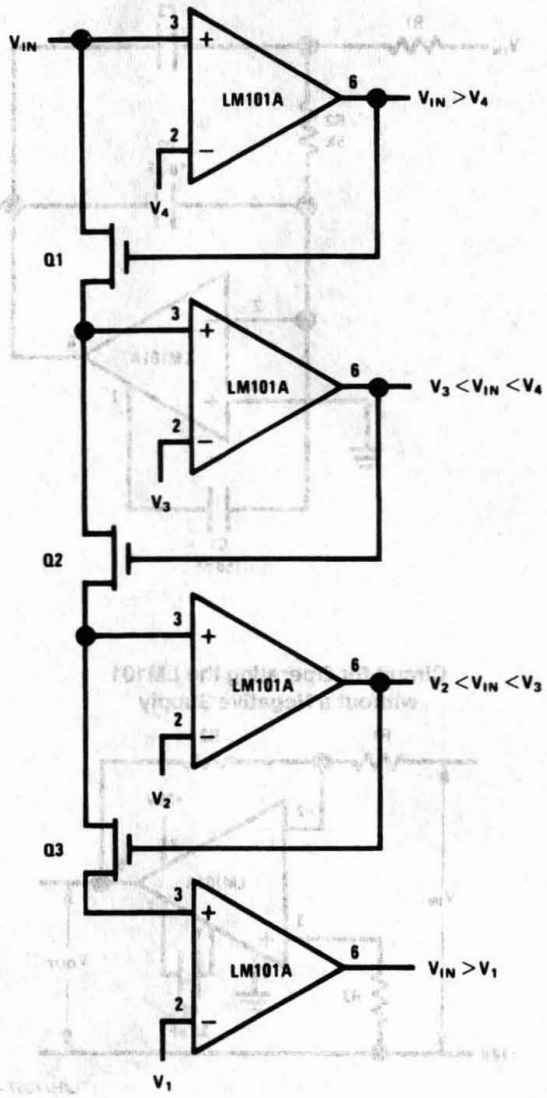


V_{OUT} = 4.6V for $V_{LT} \leq V_{IN} \leq V_{UT}$

V_{OUT} = 0V for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

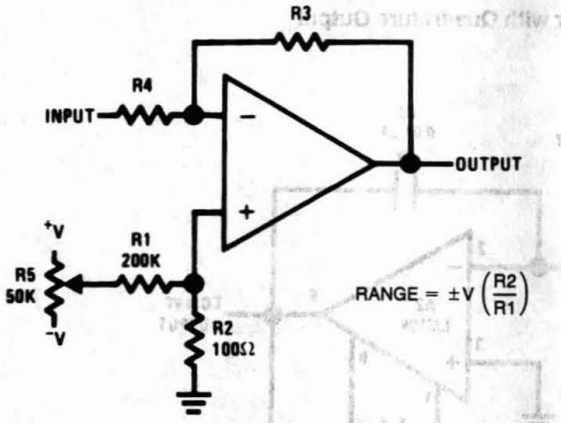
TL/H/7057–19

Multiple Aperture Window Discriminator



TL/H/7057–20

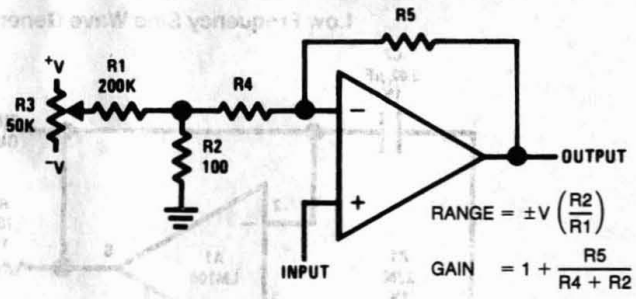
Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element



$$\text{RANGE} = \pm V\left(\frac{R2}{R1}\right)$$

TL/H/7057–21

Offset Voltage Adjustment for Non-Inverting Amplifiers Using Any Type of Feedback Element

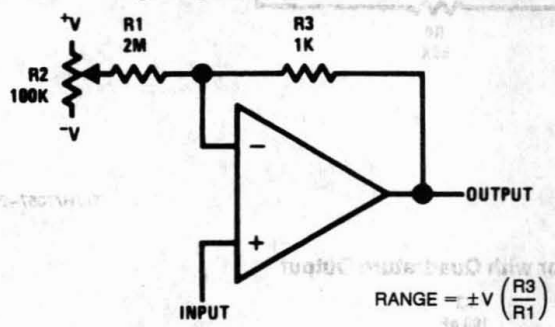


$$\text{RANGE} = \pm V\left(\frac{R2}{R1}\right)$$

$$\text{GAIN} = 1 + \frac{R5}{R4 + R2}$$

TL/H/7057–22

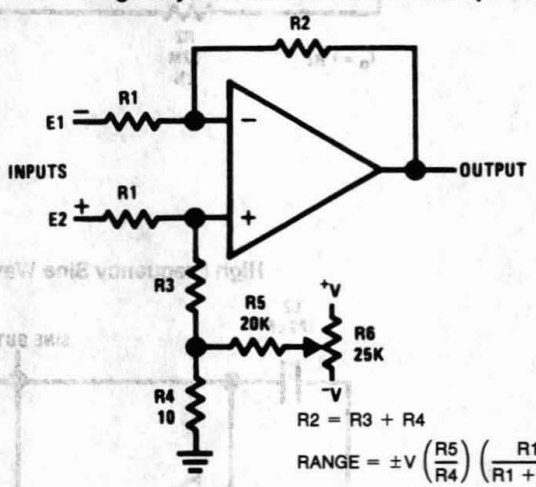
Offset Voltage Adjustment for Voltage Followers



$$\text{RANGE} = \pm V\left(\frac{R3}{R1}\right)$$

TL/H/7057–23

Offset Voltage Adjustment for Differential Amplifiers



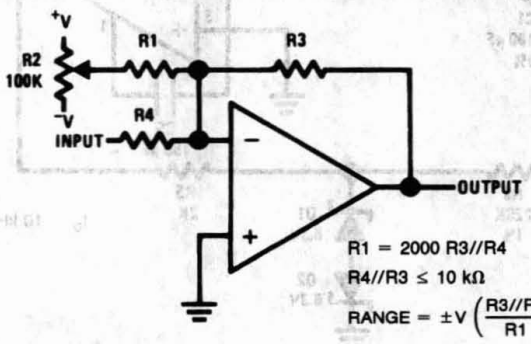
$$R2 = R3 + R4$$

$$\text{RANGE} = \pm V\left(\frac{R5}{R4}\right)\left(\frac{R1}{R1 + R3}\right)$$

$$\text{GAIN} = \frac{R2}{R1}$$

TL/H/7057–24

Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less



$$R1 = 2000\ R3//R4$$

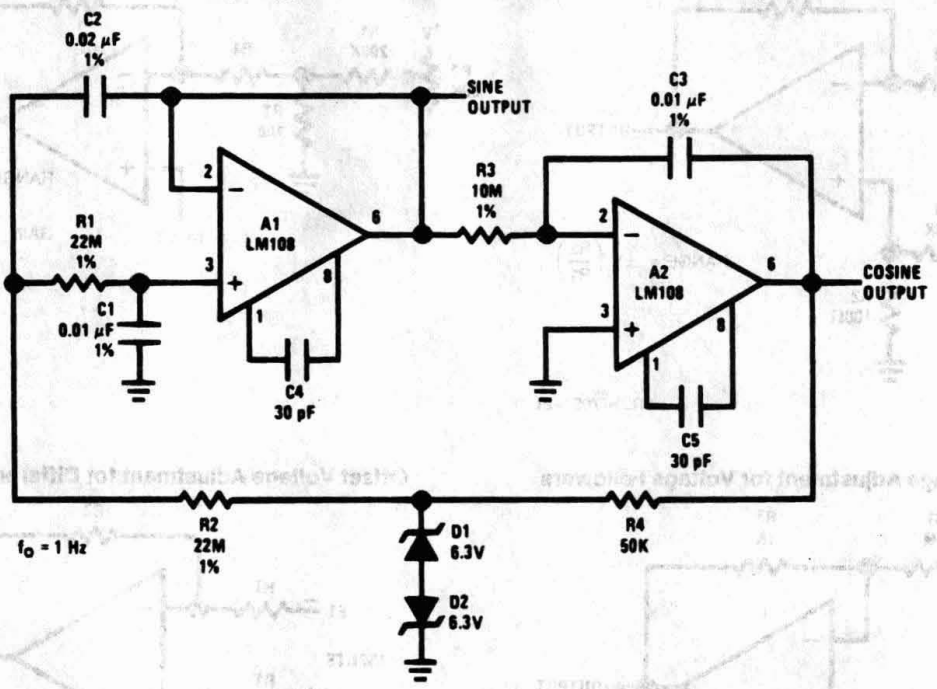
$$R4//R3 \leq 10\ k\Omega$$

$$\text{RANGE} = \pm V\left(\frac{R3//R4}{R1}\right)$$

TL/H/7057–25

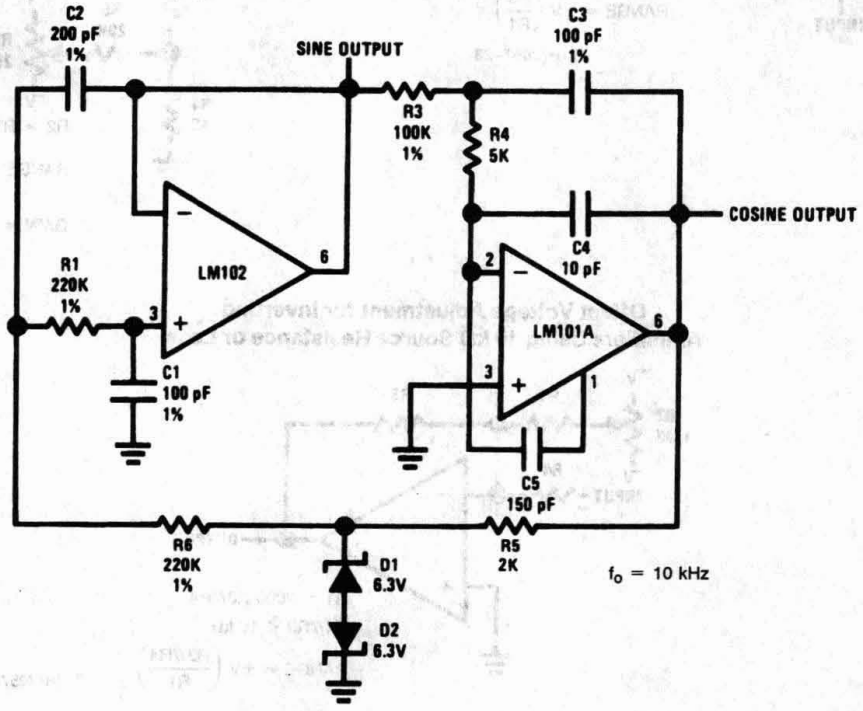
SECTION 2 — SIGNAL GENERATION

Low Frequency Sine Wave Generator with Quadrature Output



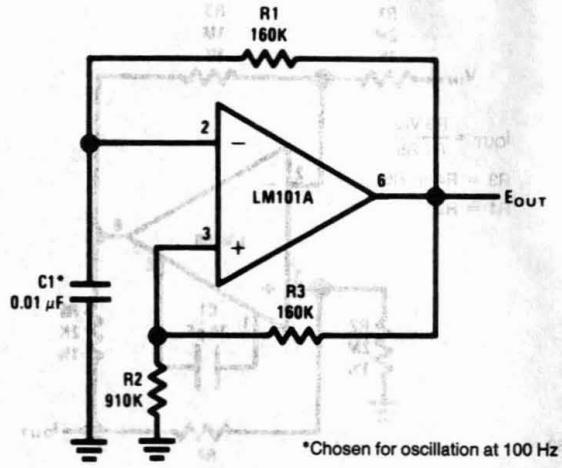
TL/H/7057–26

High Frequency Sine Wave Generator with Quadrature Output



TL/H/7057–27

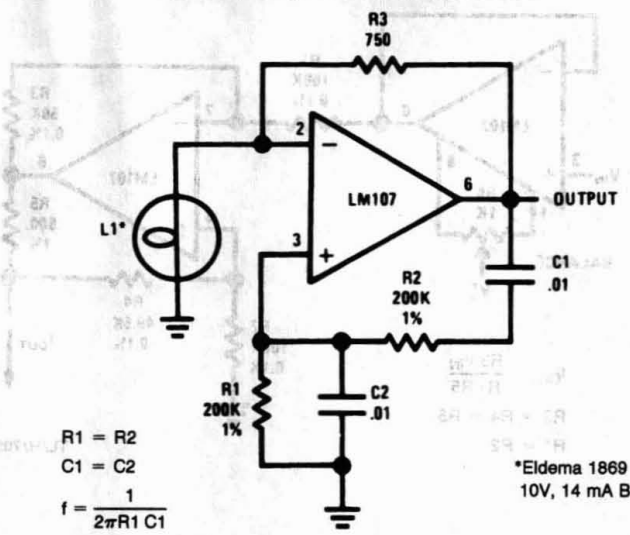
Free-Running Multivibrator



*Chosen for oscillation at 100 Hz

TL/H/7057–28

Wein Bridge Sine Wave Oscillator



$R1 = R2$

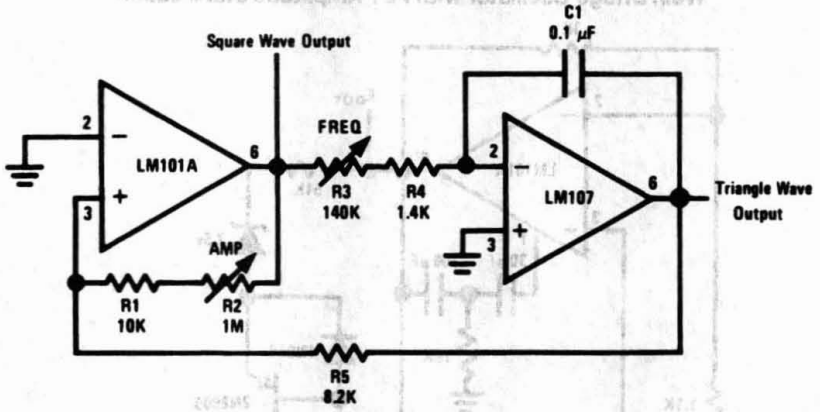
$C1 = C2$

$f = \frac{1}{2\pi R1\,C1}$

*Eldema 1869
10V, 14 mA Bulb

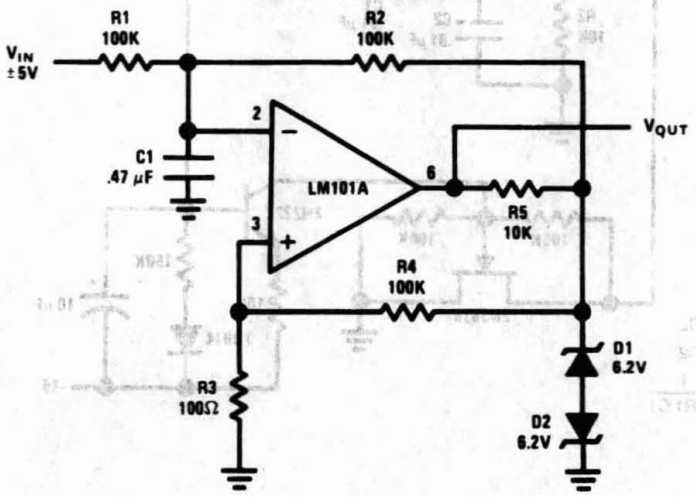
TL/H/7057–29

Function Generator



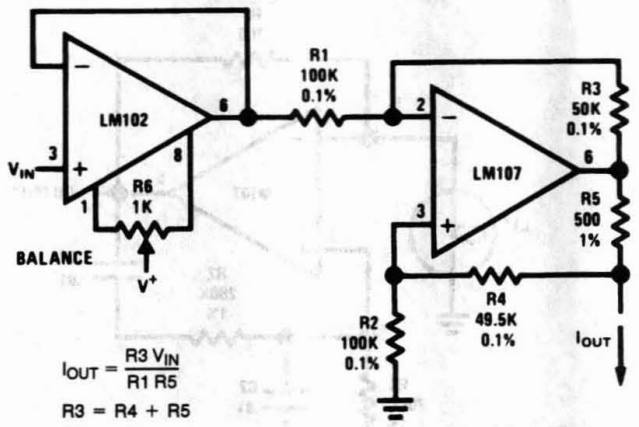
TL/H/7057–30

Pulse Width Modulator



TL/H/7057–31

Bilateral Current Source



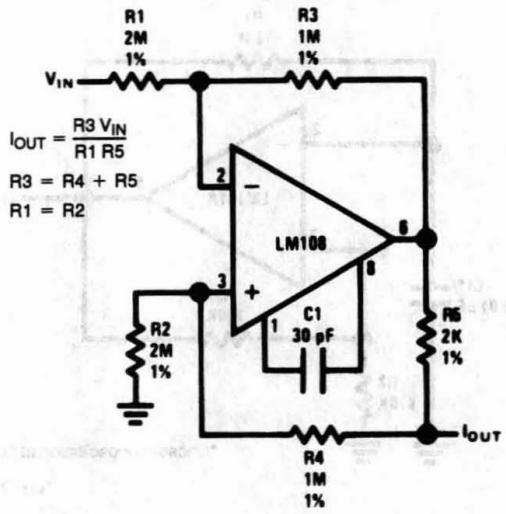
$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

R3 = R4 + R5

R1 = R2

TL/H/7057-32

Bilateral Current Source



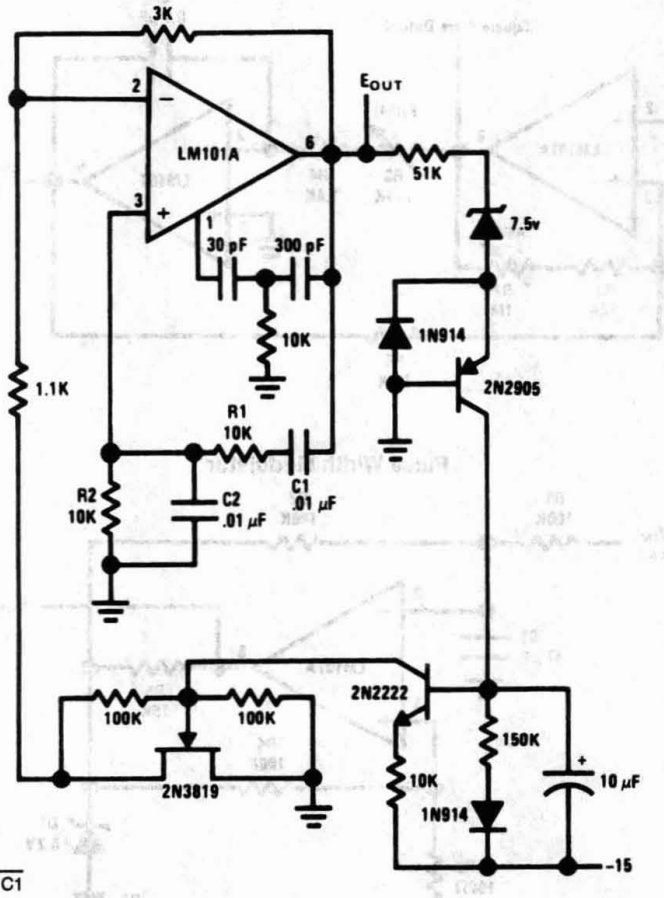
$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

R3 = R4 + R5

R1 = R2

TL/H/7057-33

Wein Bridge Oscillator with FET Amplitude Stabilization



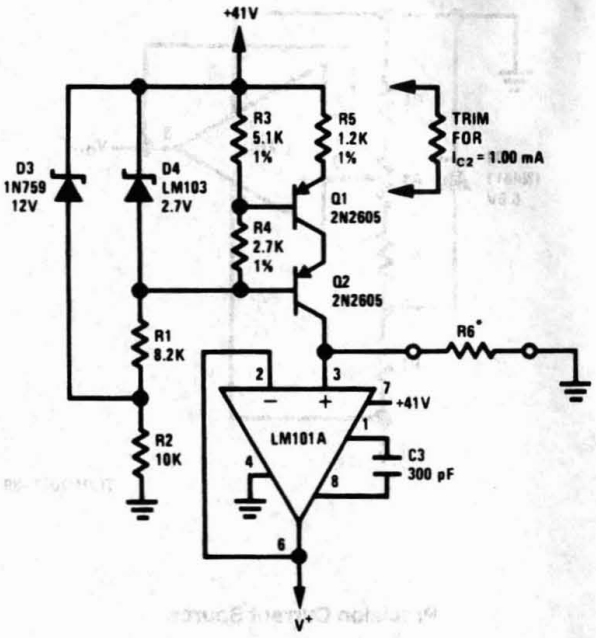
R1 = R2

C1 = C2

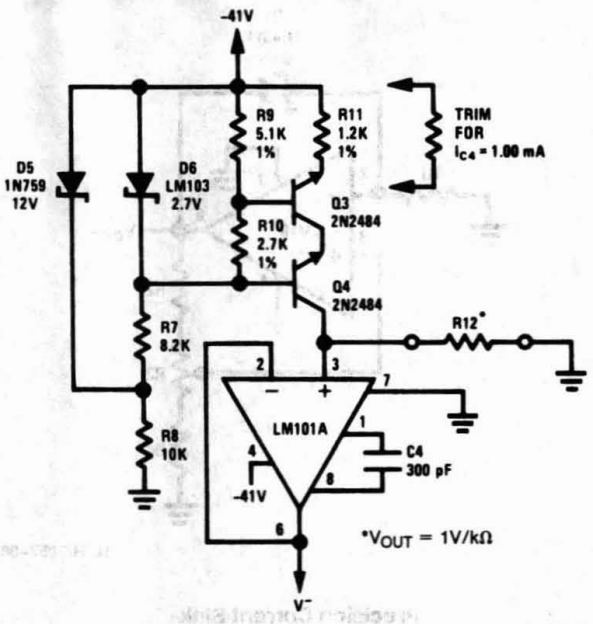
$$f = \frac{1}{2\pi R1\ C1}$$

TL/H/7057-34

Low Power Supply for Integrated Circuit Testing

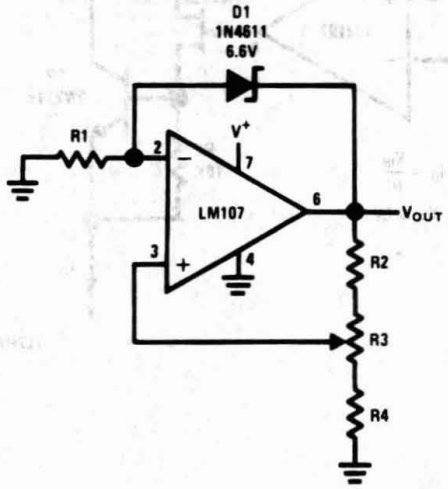


TL/H/7057–35



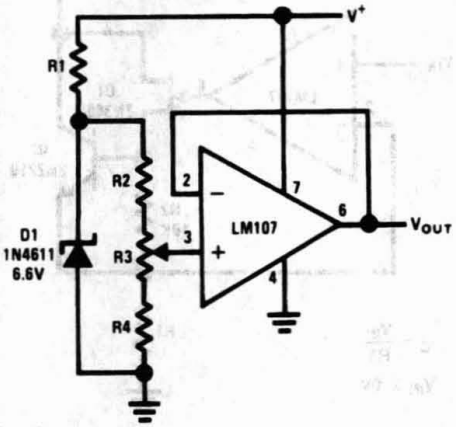
TL/H/7057–91

Positive Voltage Reference



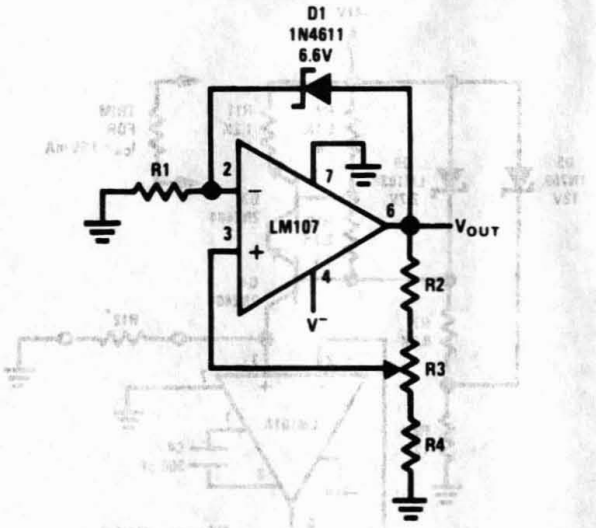
TL/H/7057–36

Positive Voltage Reference



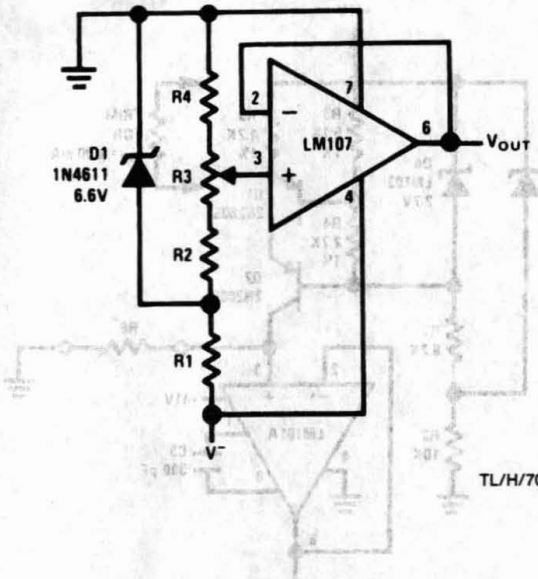
TL/H/7057–37

Negative Voltage Reference



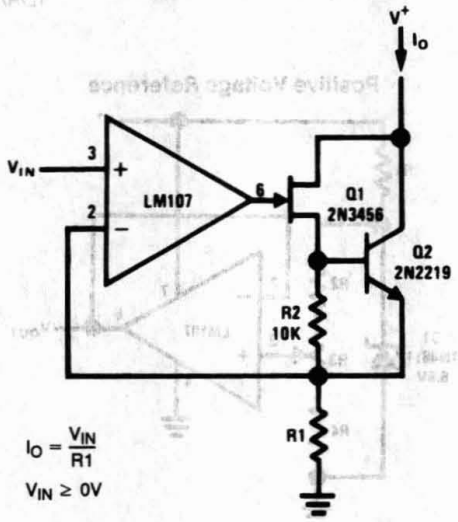
TL/H/7057–38

Negative Voltage Reference



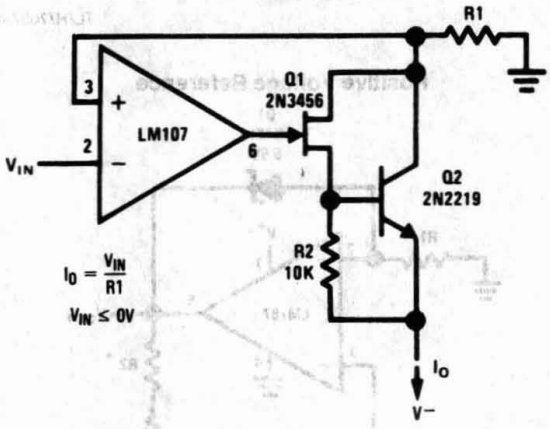
TL/H/7057–39

Precision Current Sink



TL/H/7057–40

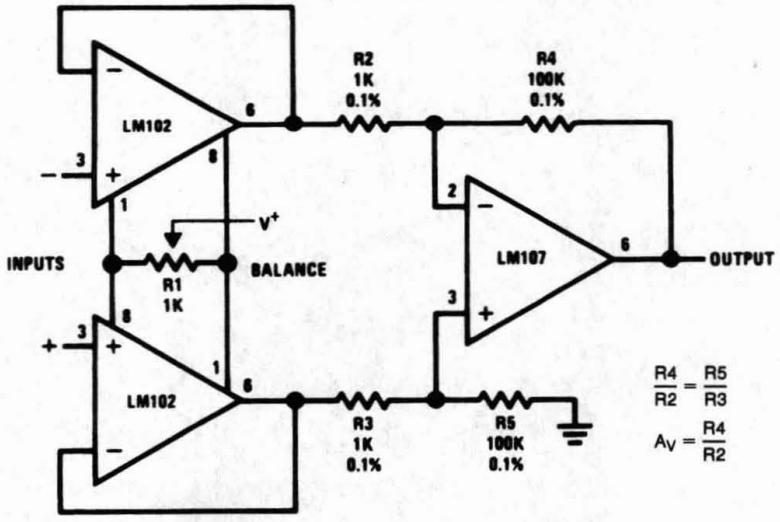
Precision Current Source



TL/H/7057–41

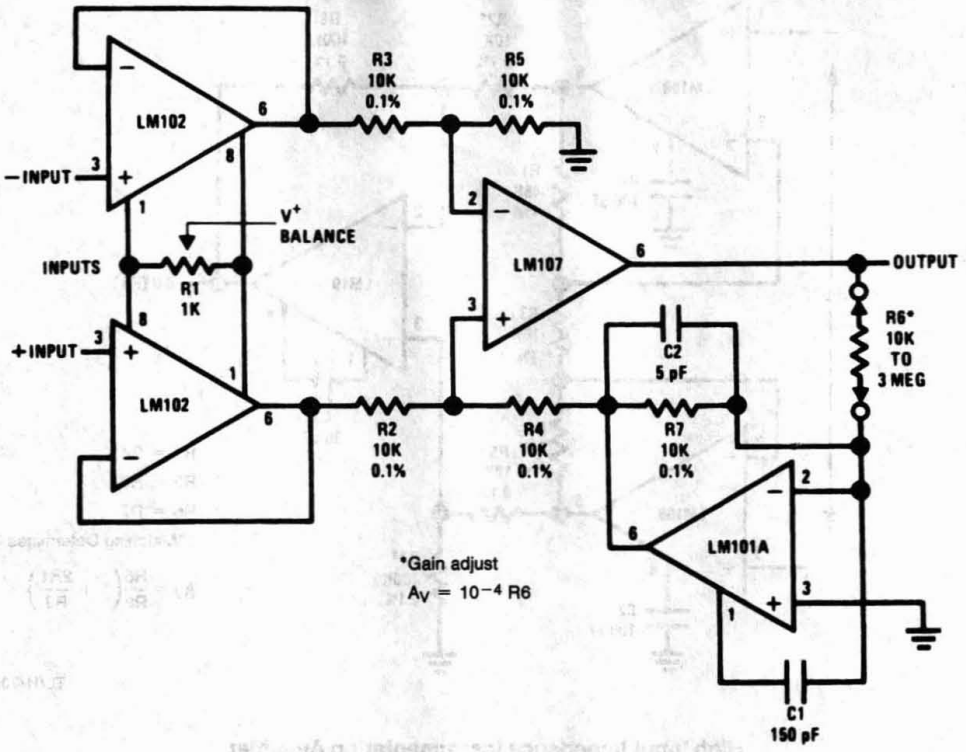
SECTION 3 — SIGNAL PROCESSING

Differential-Input Instrumentation Amplifier



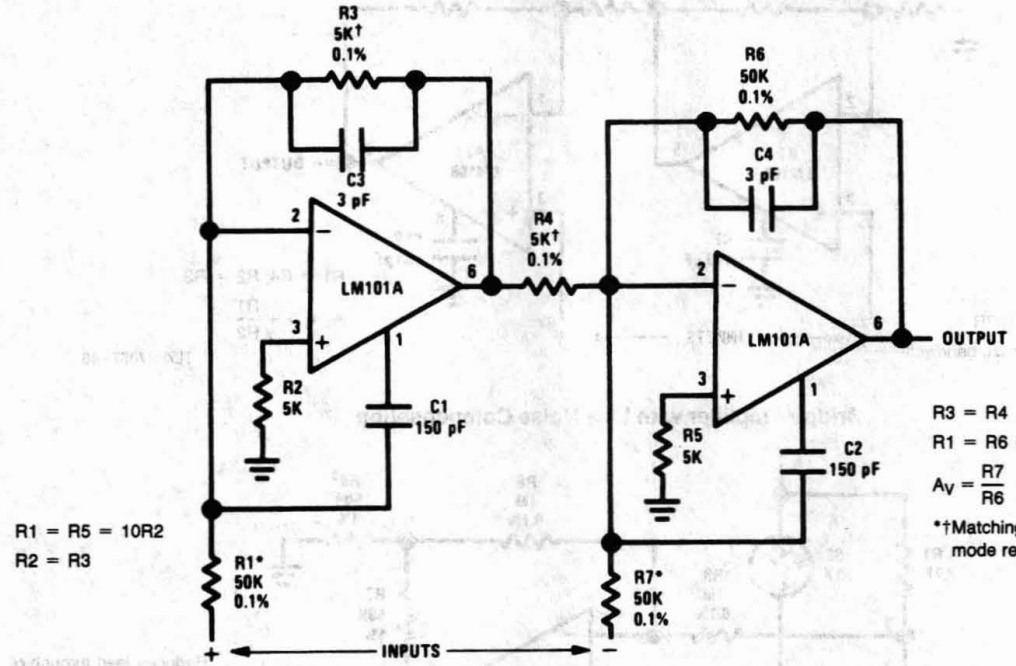
TL/H/7057–42

Variable Gain, Differential-Input Instrumentation Amplifier



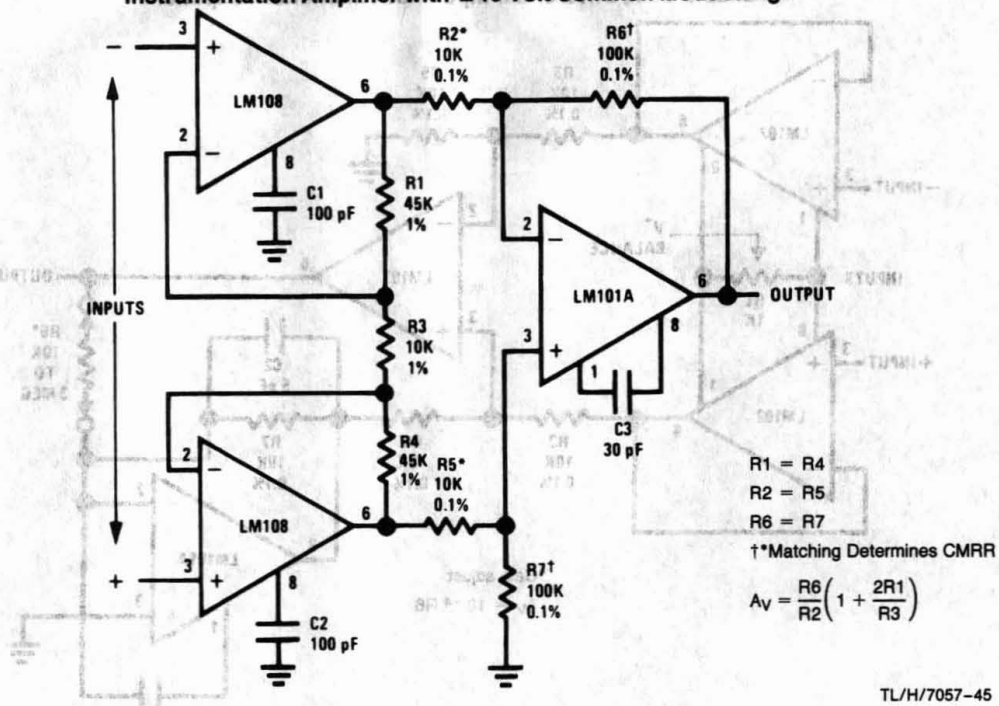
TL/H/7057–43

Instrumentation Amplifier with ±100 Volt Common Mode Range



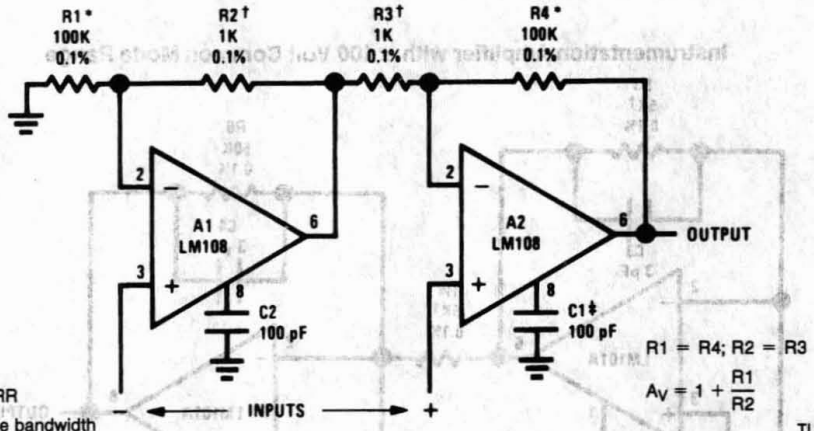
TL/H/7057–44

Instrumentation Amplifier with ±10 Volt Common Mode Range



TL/H/7057–45

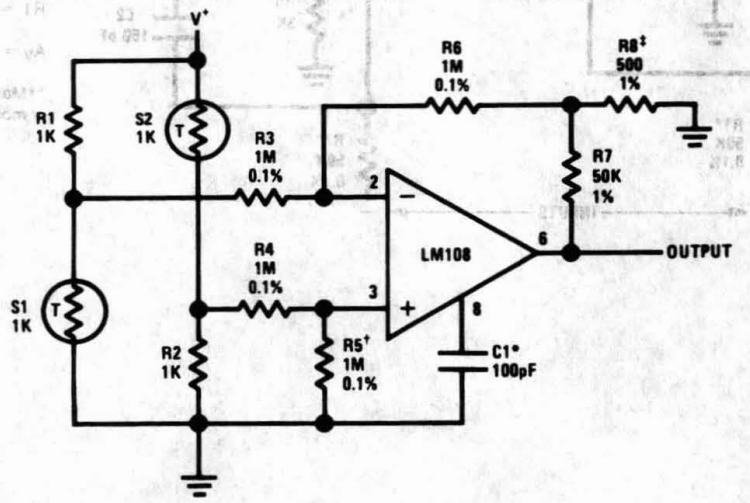
High Input Impedance Instrumentation Amplifier



*†Matching determines CMRR
‡May be deleted to maximize bandwidth

TL/H/7057–46

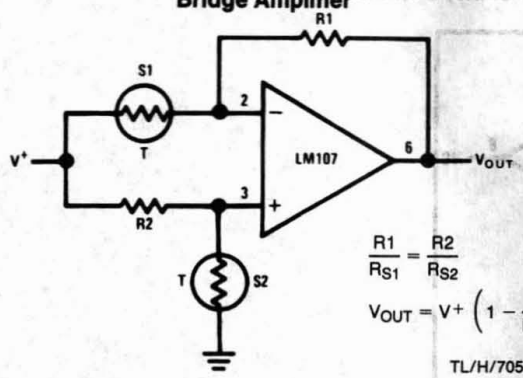
Bridge Amplifier with Low Noise Compensation



*Reduces feed through of power supply noise by 20 dB and makes supply bypassing unnecessary.
†Trim for best common mode rejection
‡Gain adjust

TL/H/7057–47

Bridge Amplifier

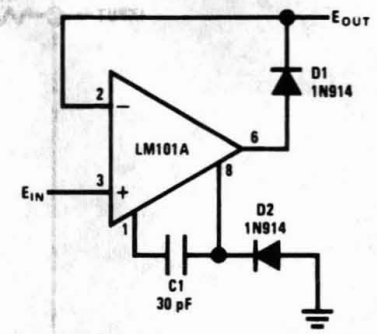


$$\frac{R1}{R_{S1}} = \frac{R2}{R_{S2}}$$

$$V_{OUT} = V^+ \left(1 - \frac{R1}{R_{S1}}\right)$$

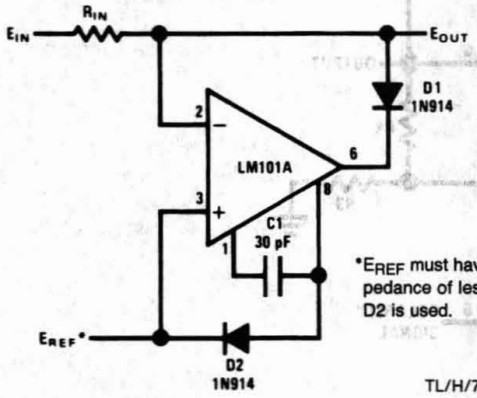
TL/H/7057–48

Precision Diode



TL/H/7057–49

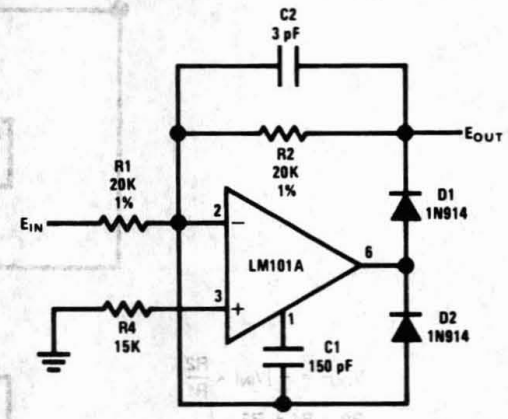
Precision Clamp



*EREF must have a source impedance of less than 200Ω if D2 is used.

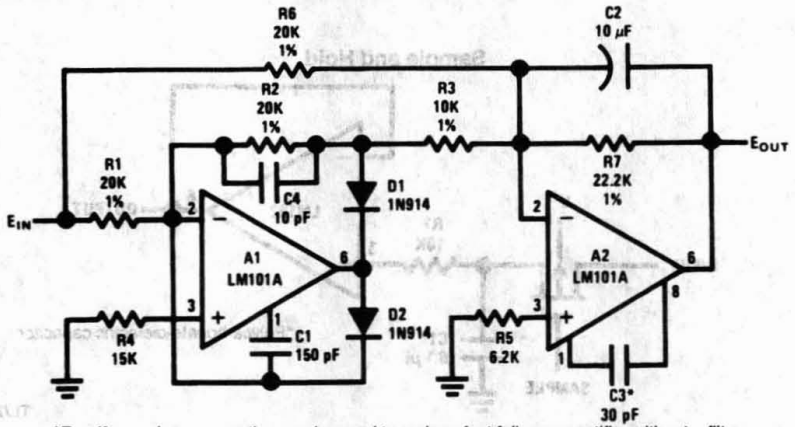
TL/H/7057–50

Fast Half Wave Rectifier



TL/H/7057–51

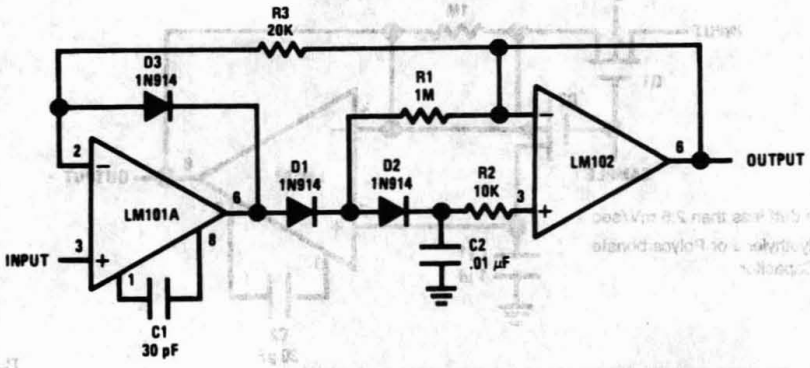
Precision AC to DC Converter



*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

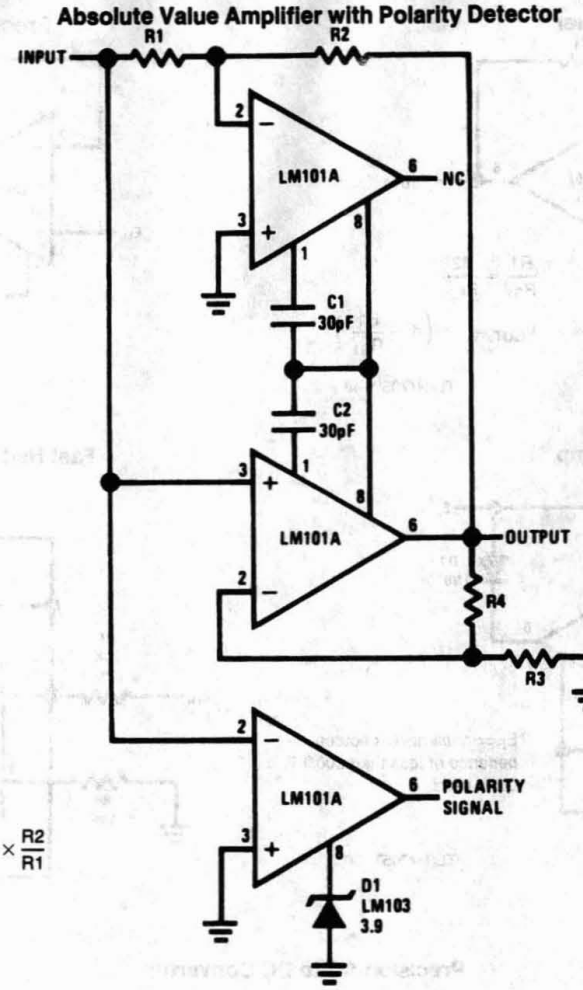
TL/H/7057–52

Low Drift Peak Detector



TL/H/7057–53

Absolute Value Amplifier with Polarity Detector

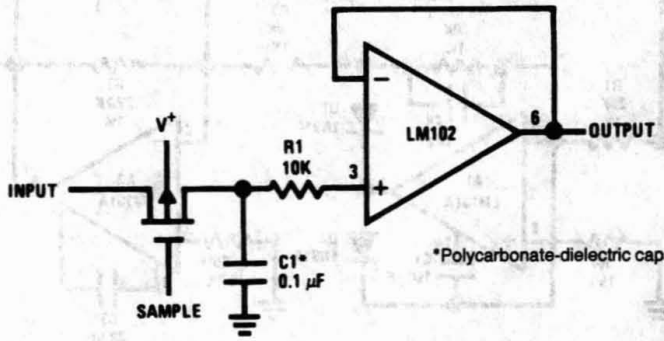


$$V_{OUT} = -|V_{IN}| \times \frac{R2}{R1}$$

$$\frac{R2}{R1} = \frac{R4 + R3}{R3}$$

TL/H/7057–54

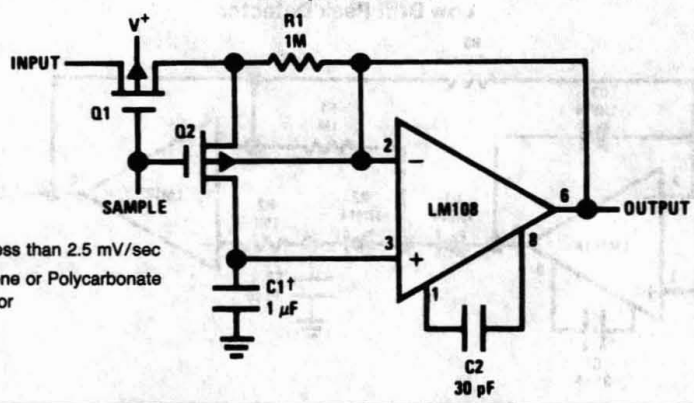
Sample and Hold



*Polycarbonate-dielectric capacitor

TL/H/7057–55

Sample and Hold

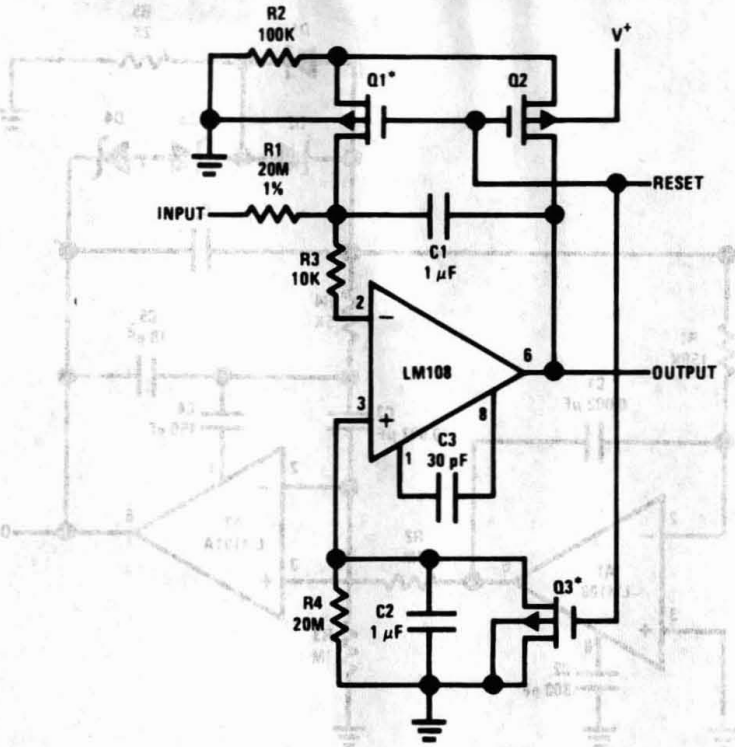


*Worst case drift less than 2.5 mV/sec

†Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

TL/H/7057–56

Low Drift Integrator

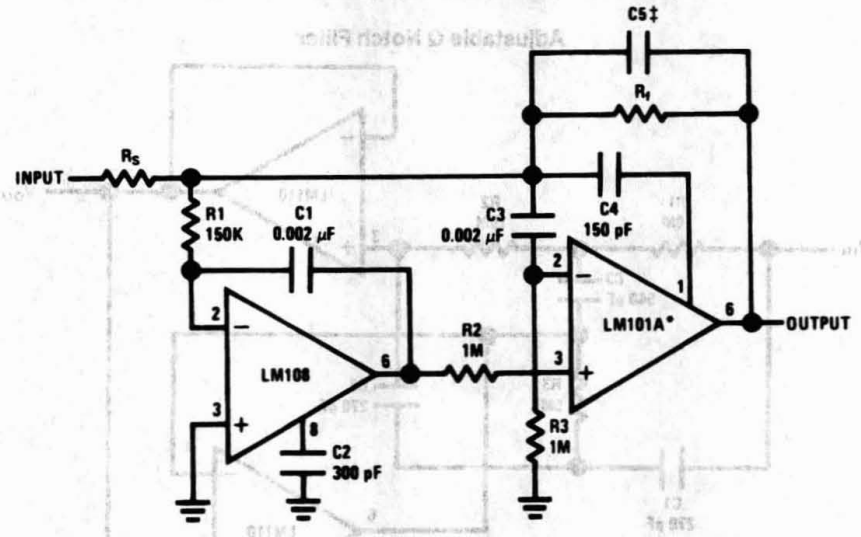


TL/H/7057–57

*Q1 and Q3 should not have internal gate-protection diodes.

Worst case drift less than 500 μV/sec over −55°C to +125°C.

Fast† Summing Amplifier with Low Input Current



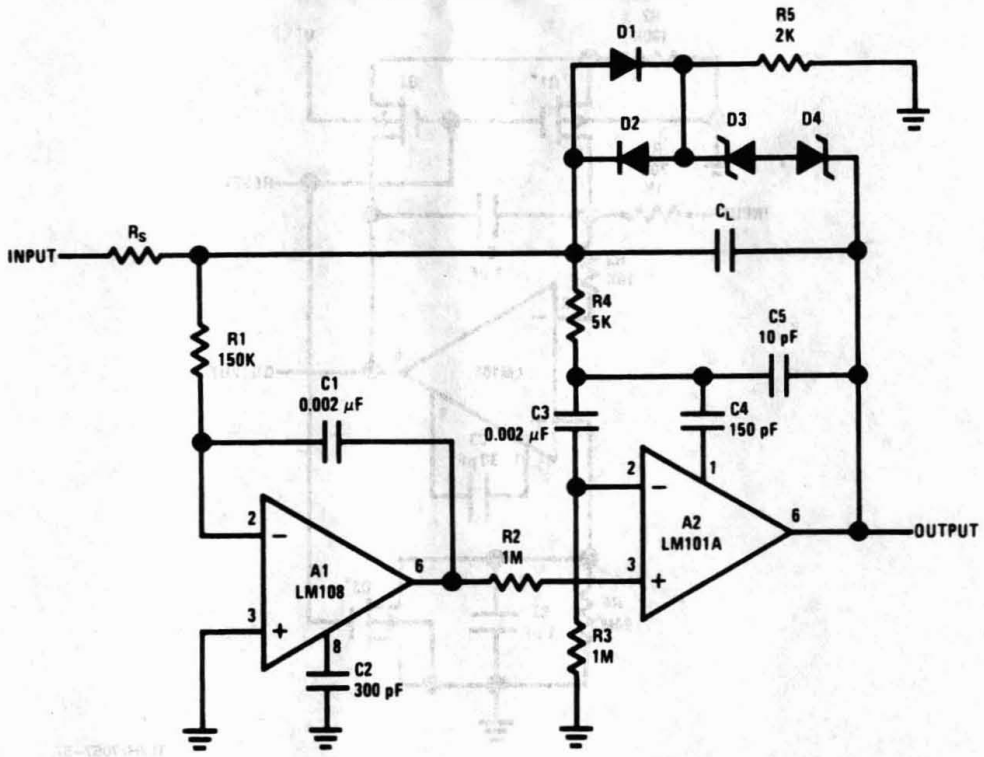
TL/H/7057–58

* In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

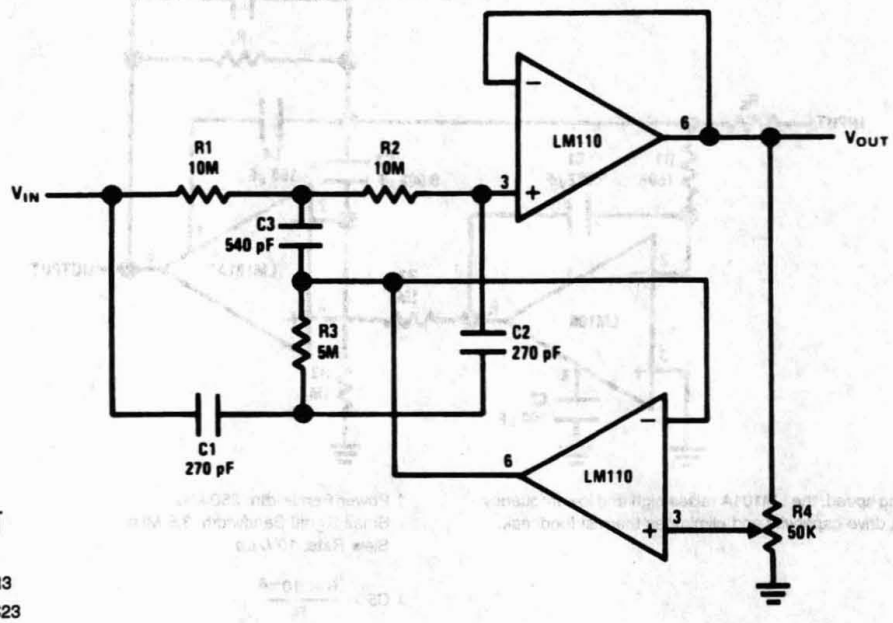
‡ $C5 = \frac{6 \times 10^{-8}}{R_f}$

Fast Integrator with Low Input Current



TL/H/7057-59

Adjustable Q Notch Filter



$$f_O = \frac{1}{2\pi R1C1}$$

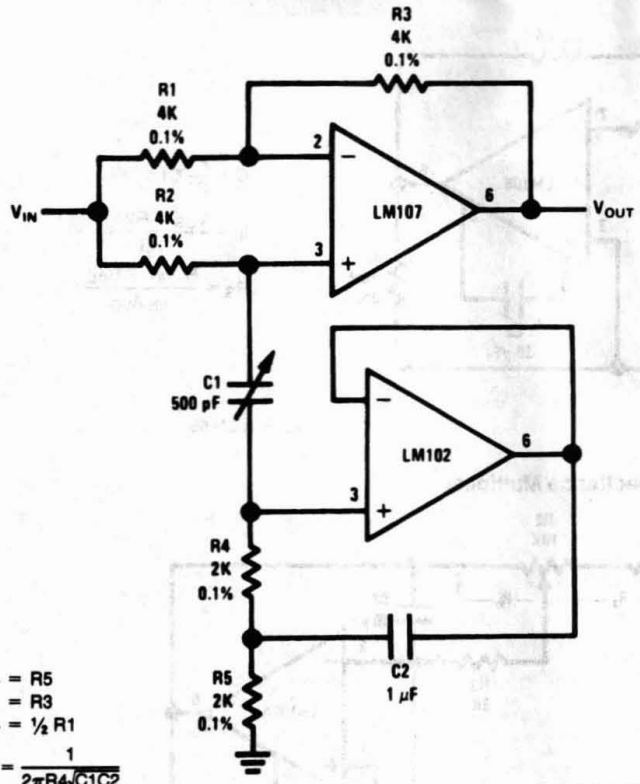
$= 60$ Hz

R1 = R2 = R3

C1 = C2 = C23

TL/H/7057-60

Easily Tuned Notch Filter

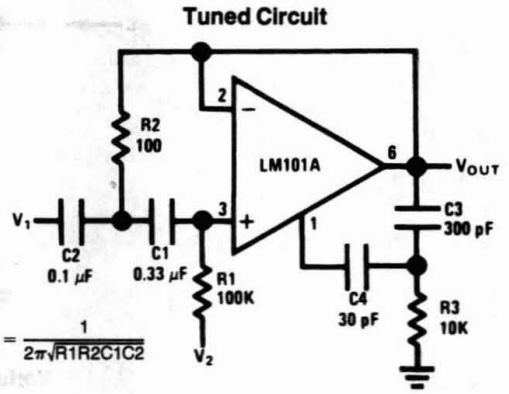


R4 = R5
R1 = R3
R4 = ½ R1

$$f_O = \frac{1}{2\pi R4\sqrt{C1C2}}$$

TL/H/7057-61

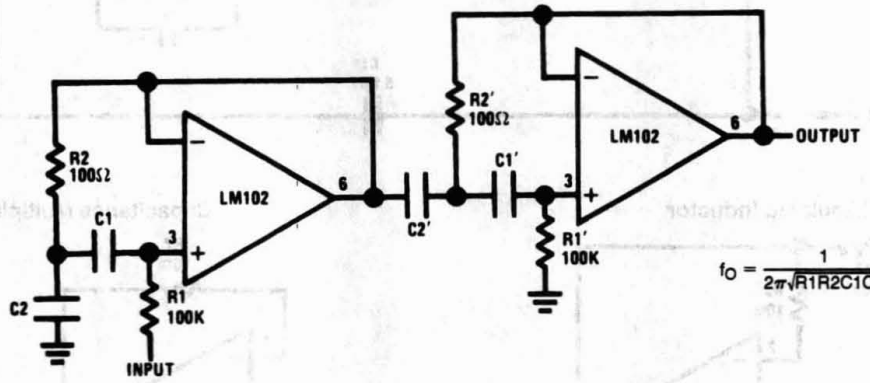
Tuned Circuit



$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

TL/H/7057-62

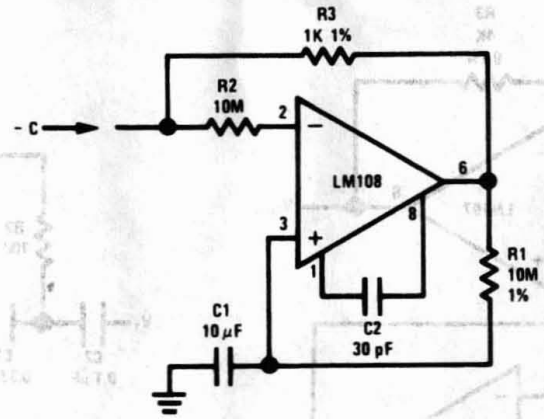
Two-Stage Tuned Circuit



$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

TL/H/7057-63

Negative Capacitance Multiplier



$$C = \frac{R2}{R3} C1$$

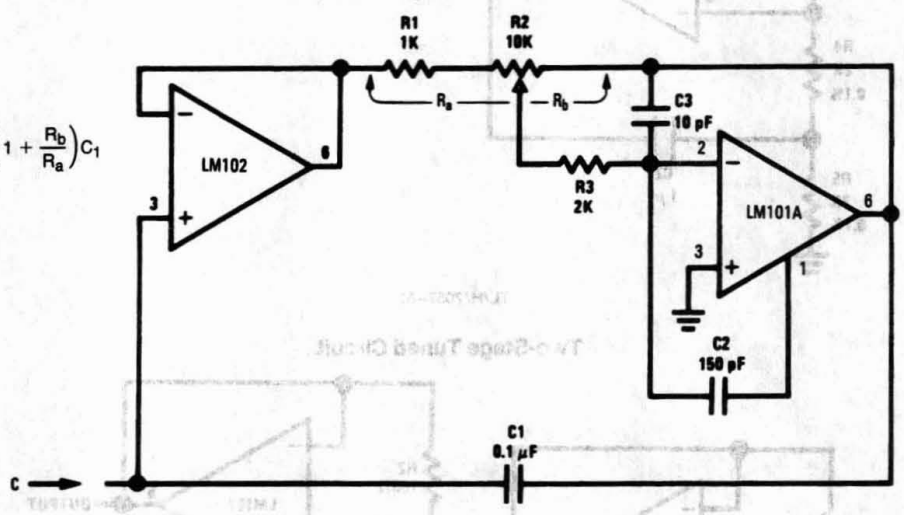
$$I_L = \frac{V_{OS} + R2\, I_{OS}}{R3}$$

$$R_S = \frac{R3(R1 + R_{IN})}{R_{IN}\, A_{VO}}$$

TL/H/7057–65

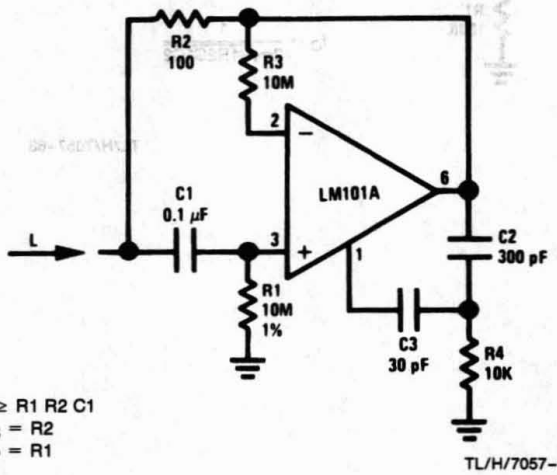
Variable Capacitance Multiplier

$$C = \left(1 + \frac{R_b}{R_a}\right) C_1$$



TL/H/7057–66

Simulated Inductor



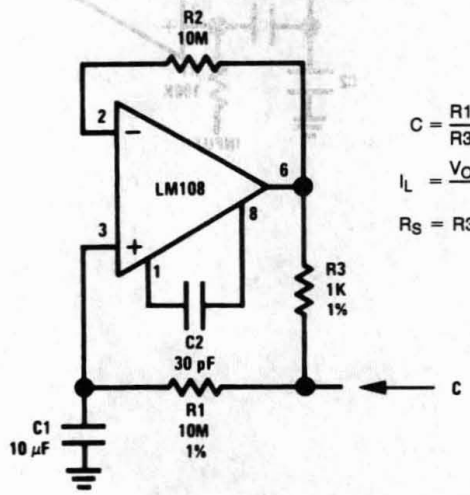
$L \geq R1\, R2\, C1$

$R_S = R2$

$R_P = R1$

TL/H/7057–67

Capacitance Multiplier



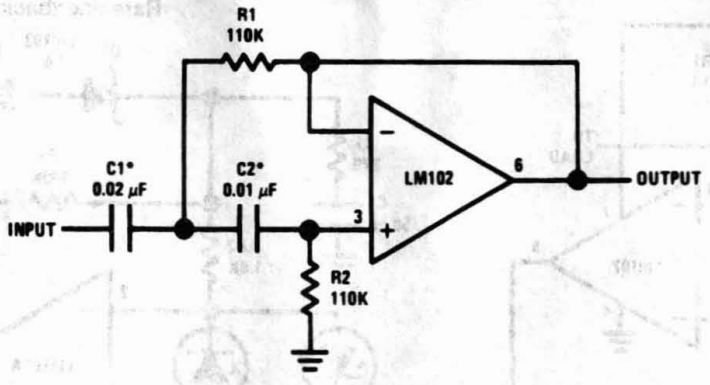
$$C = \frac{R1}{R3} C1$$

$$I_L = \frac{V_{OS} + I_{OS}\, R1}{R3}$$

$$R_S = R3$$

TL/H/7057–68

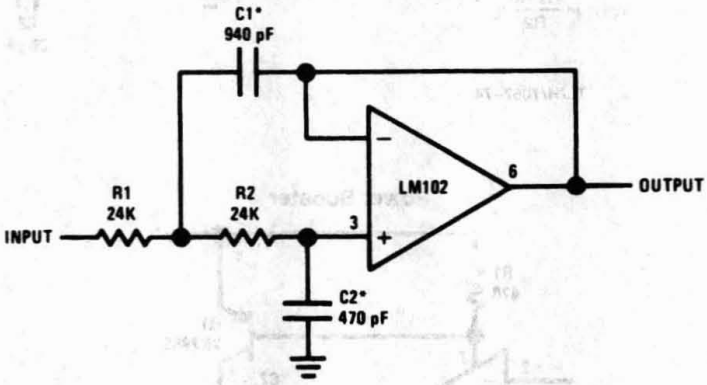
High Pass Active Filter



TL/H/7057–71

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

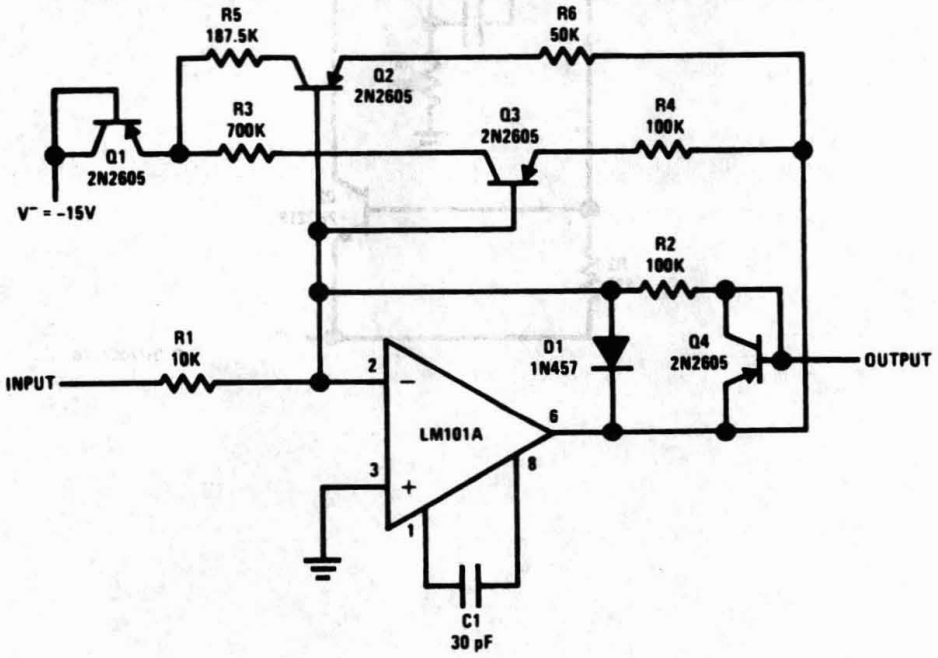
Low Pass Active Filter



TL/H/7057–72

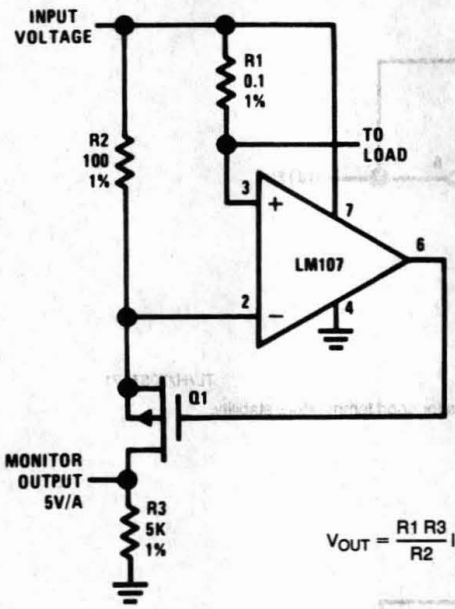
*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

Nonlinear Operational Amplifier with Temperature Compensated Breakpoints



TL/H/7057–73

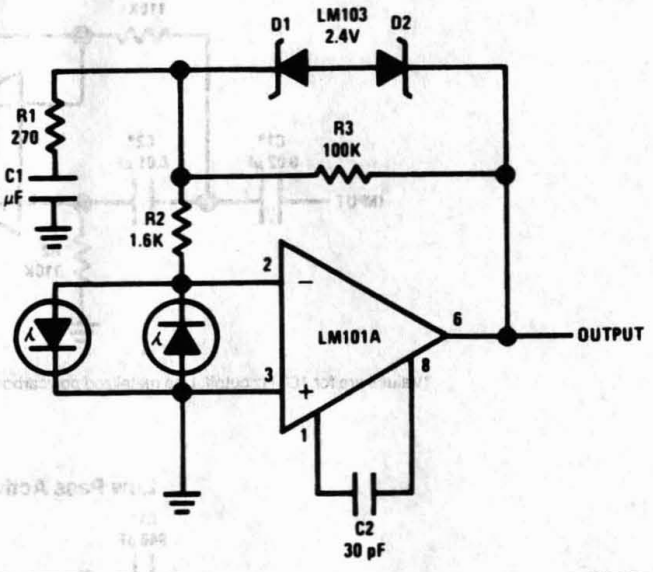
Current Monitor



$$V_{OUT} = \frac{R1\ R3}{R2} I_L$$

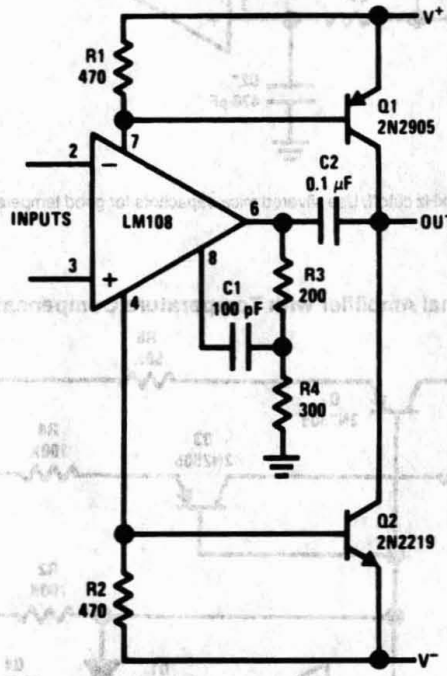
TL/H/7057–74

Saturating Servo Preamplifier with Rate Feedback



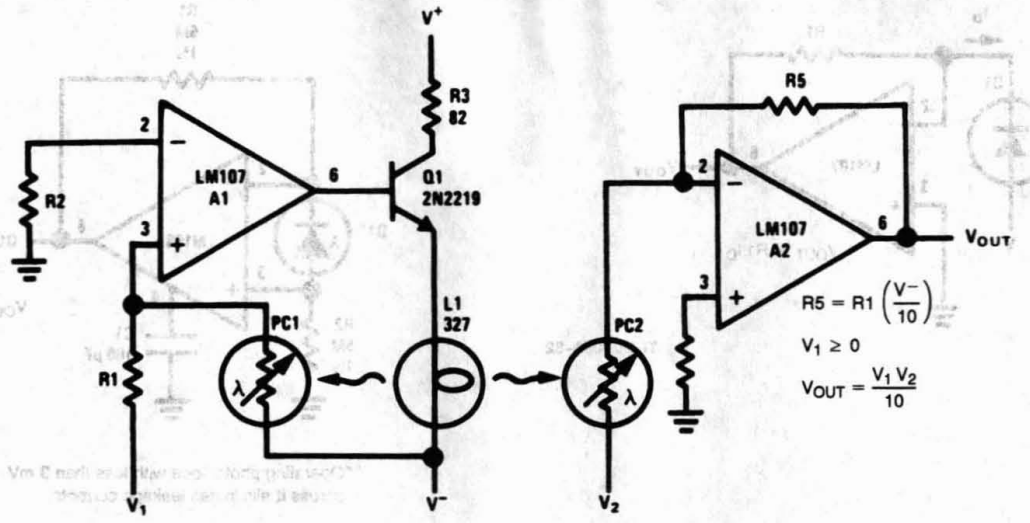
TL/H/7057–75

Power Booster



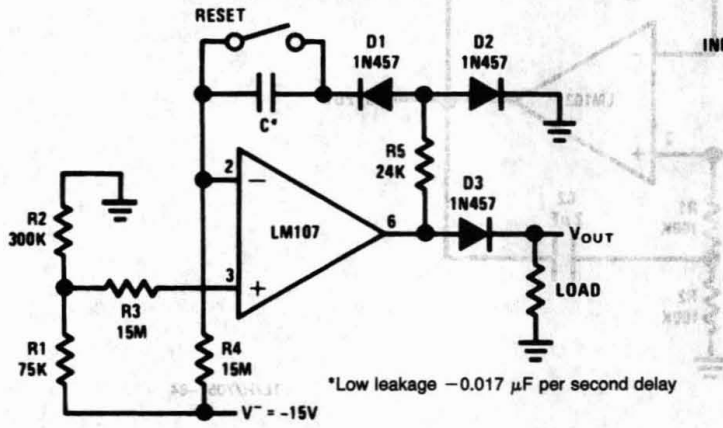
TL/H/7057–76

Analog Multiplier



TL/H/7057–77

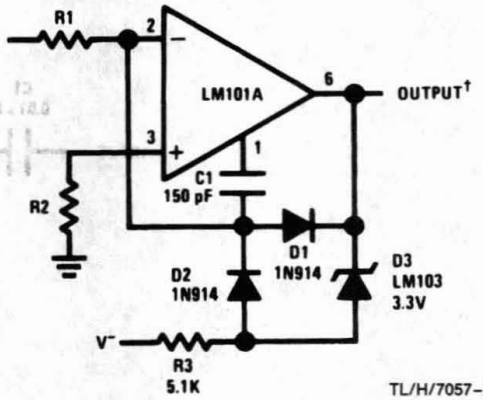
Long Interval Timer



*Low leakage −0.017 μF per second delay

TL/H/7057–78

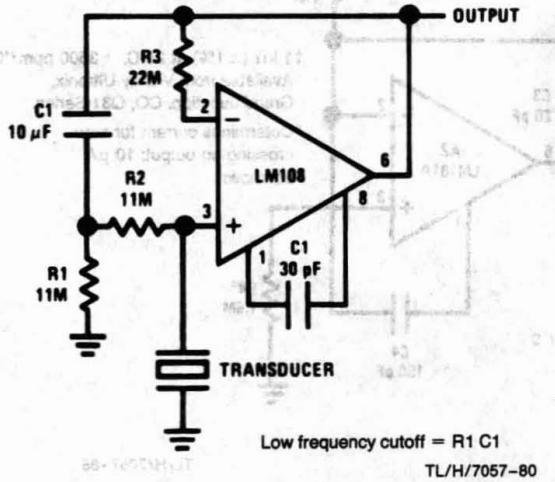
Fast Zero Crossing Detector



TL/H/7057–79

Propagation delay approximately 200 ns
†DTL or TTL fanout of three.
Minimize stray capacitance
Pin 8

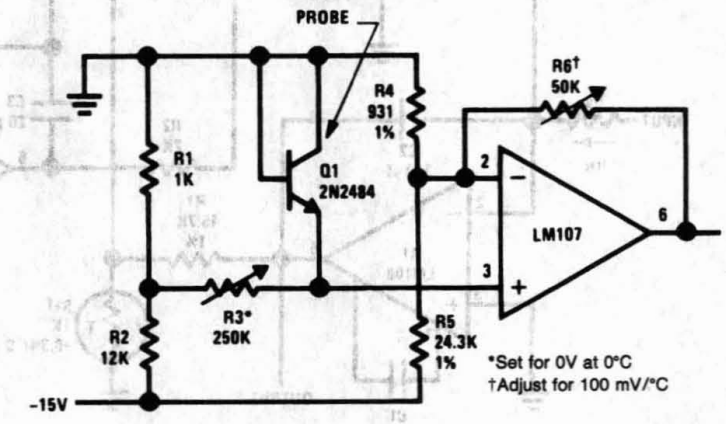
Amplifier for Piezoelectric Transducer



Low frequency cutoff = R1 C1

TL/H/7057–80

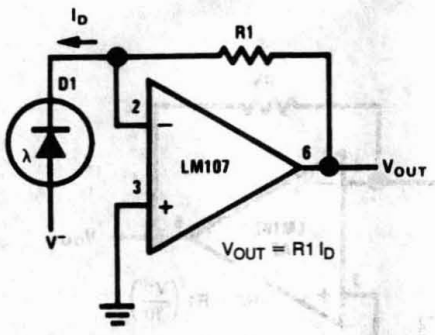
Temperature Probe



*Set for 0V at 0°C
†Adjust for 100 mV/°C

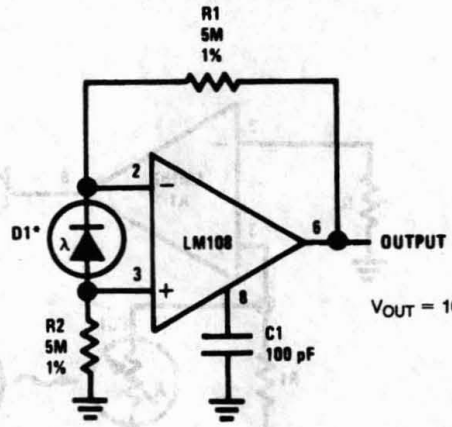
TL/H/7057–81

Photodiode Amplifier



TL/H/7057–82

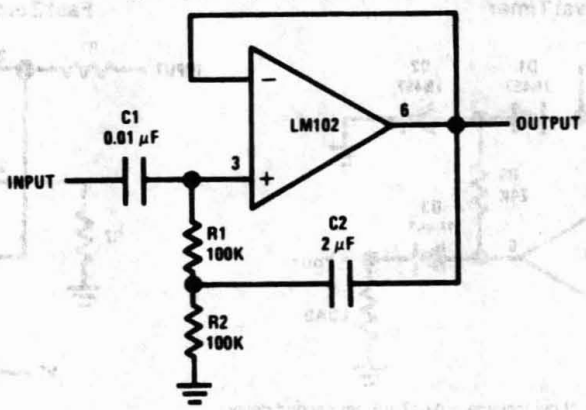
Photodiode Amplifier



TL/H/7057–83

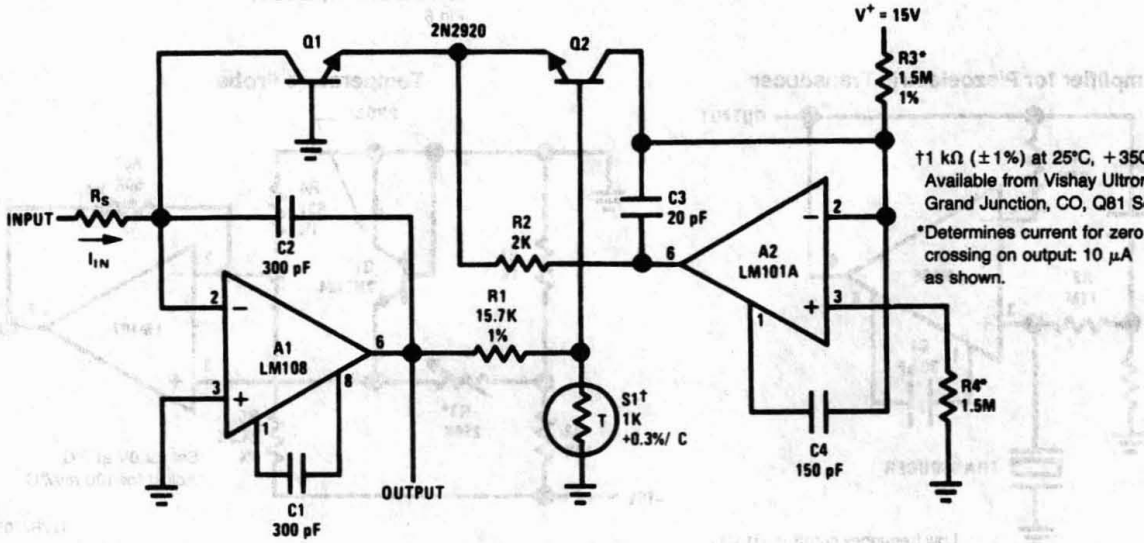
*Operating photodiode with less than 3 mV across it eliminates leakage currents.

High Input Impedance AC Follower



TL/H/7057–84

Temperature Compensated Logarithmic Converter

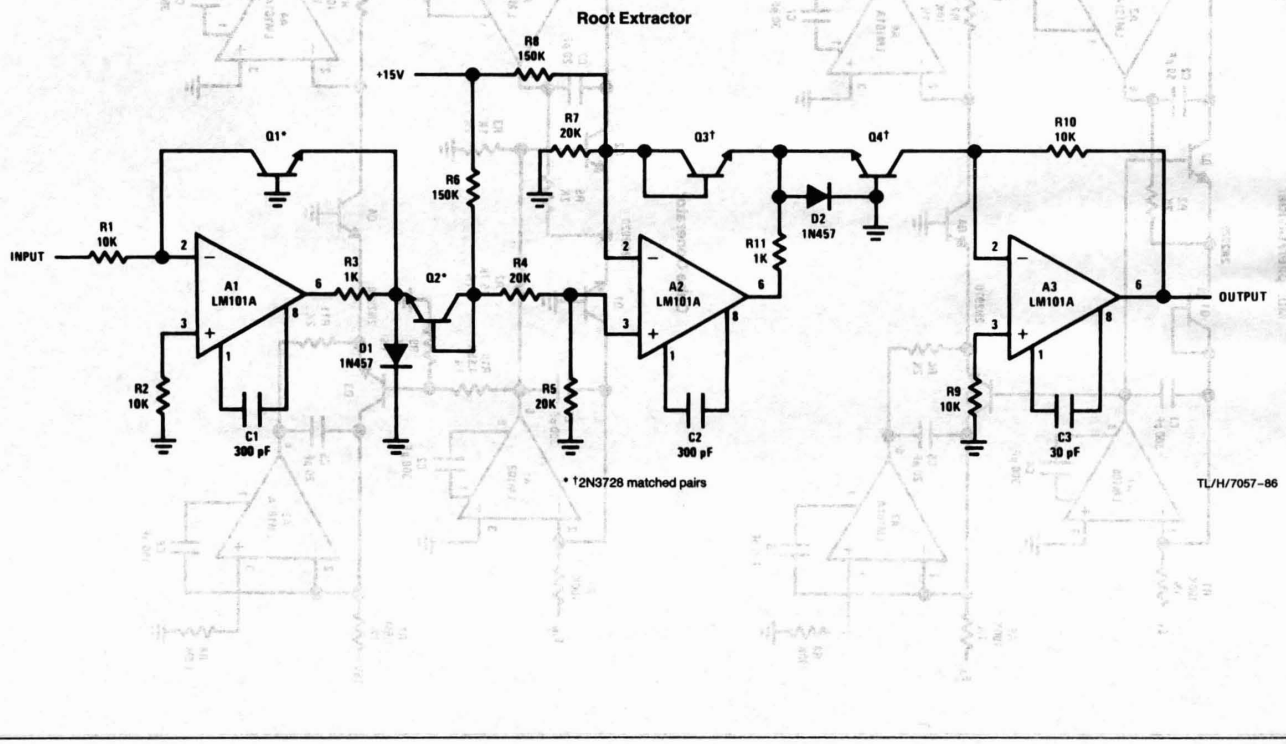


†1 kΩ (±1%) at 25°C, +3500 ppm/°C. Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

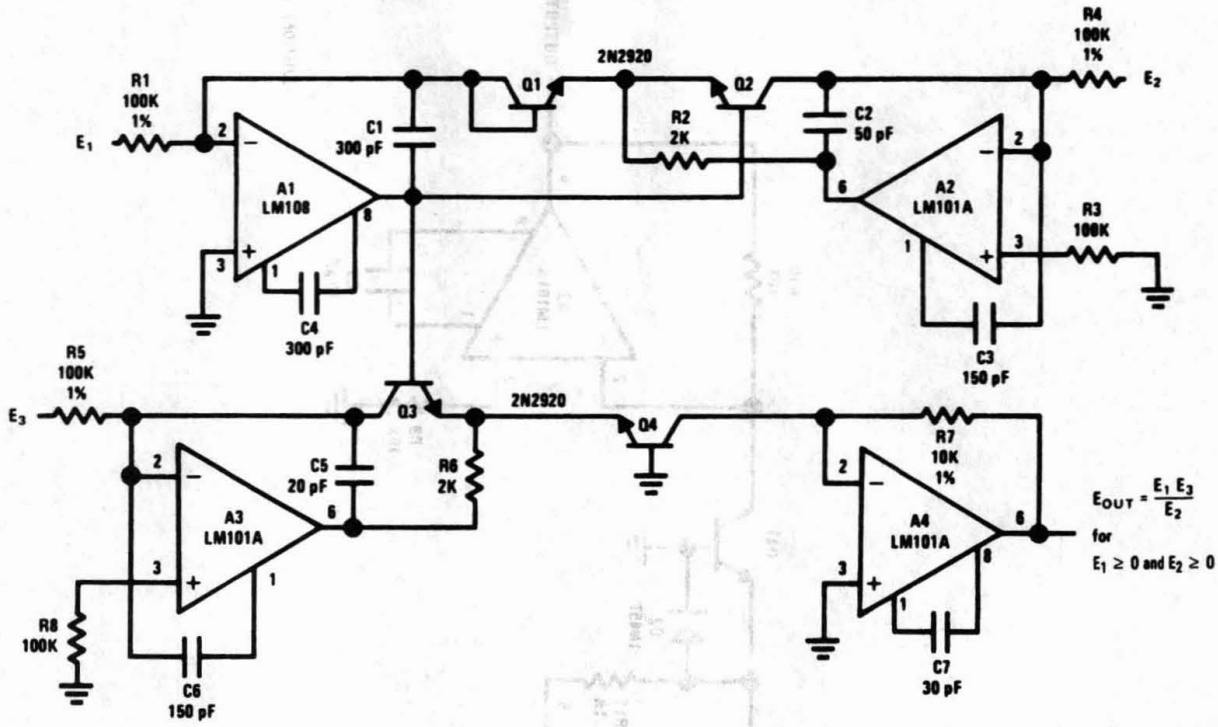
*Determines current for zero crossing on output: 10 μA as shown.

TL/H/7057–85

10 nA < I_{IN} < 1 mA
Sensitivity is 1V per decade

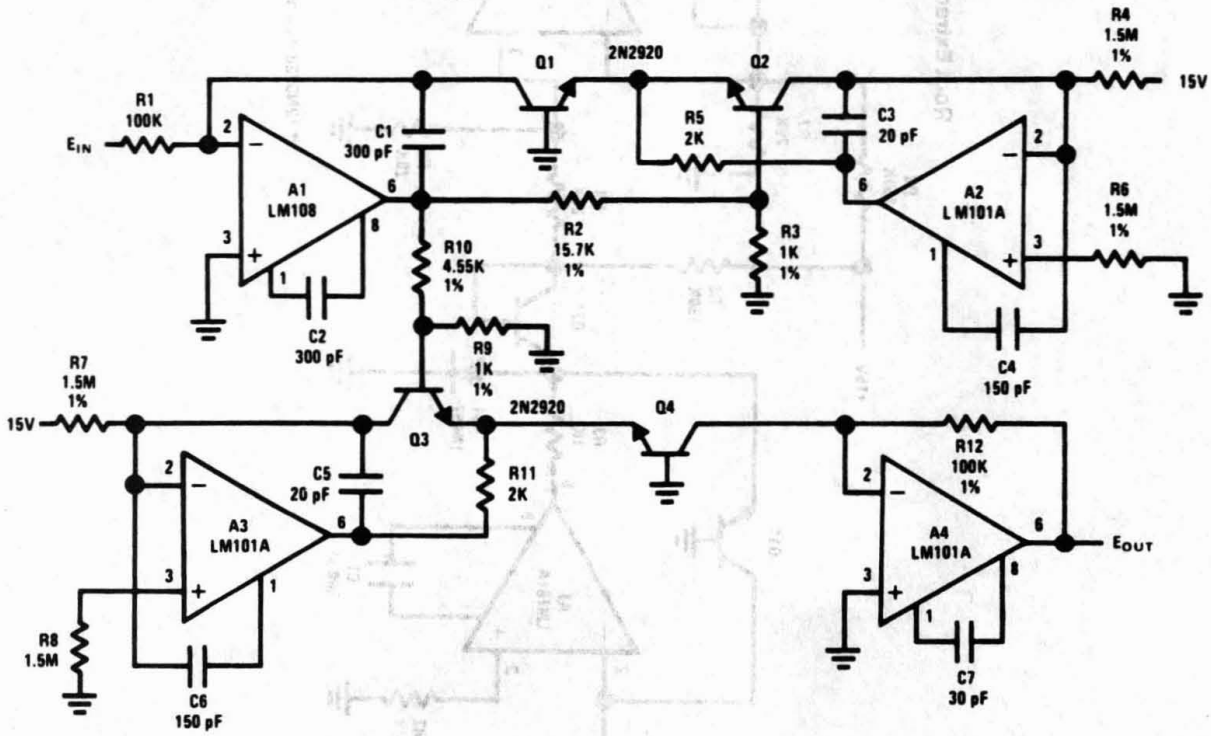

Root Extractor
+15V
R8
150K
R7
20K
Q1*
Q3†
Q4†
R10
10K
R6
150K
D2
1N457
R11
1K
R1
10K
INPUT
A1
LM101A
R3
1K
Q2*
R4
20K
A2
LM101A
A3
LM101A
OUTPUT
D1
1N457
R2
10K
R5
20K
R9
10K
C1
300 pF
C2
300 pF
C3
30 pF
* †2N3728 matched pairs
TL/H/7057–86

Multiplier/Divider



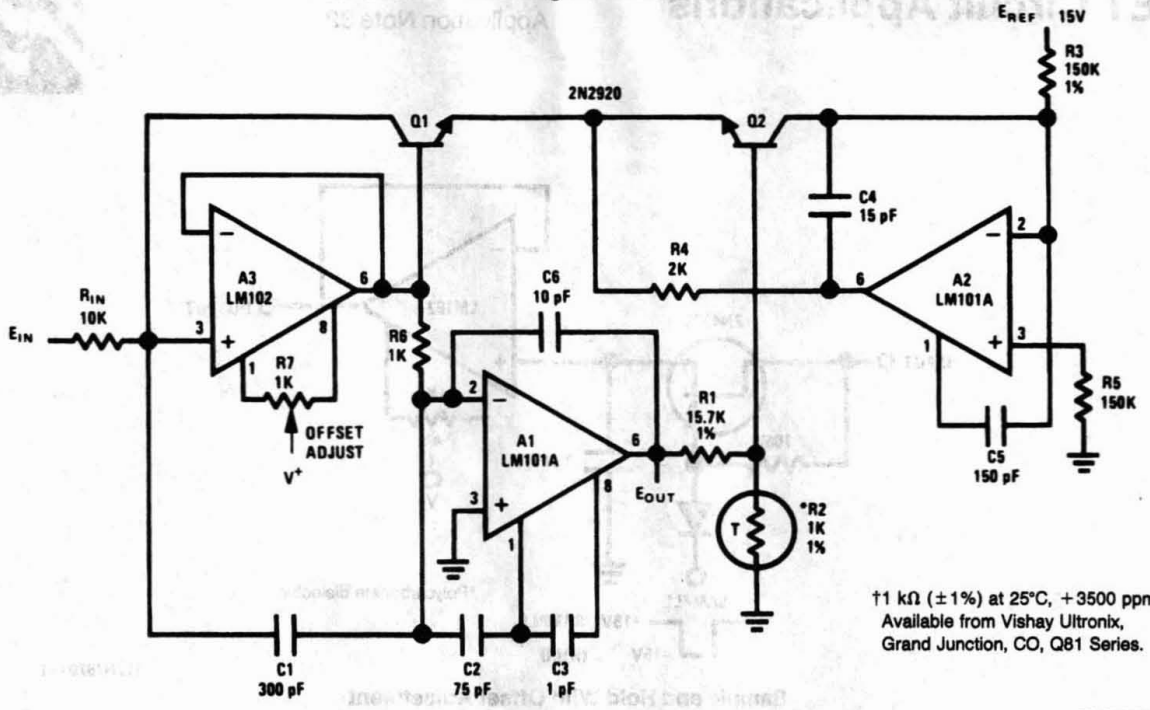
TL/H/7057–87

Cube Generator



TL/H/7057–88

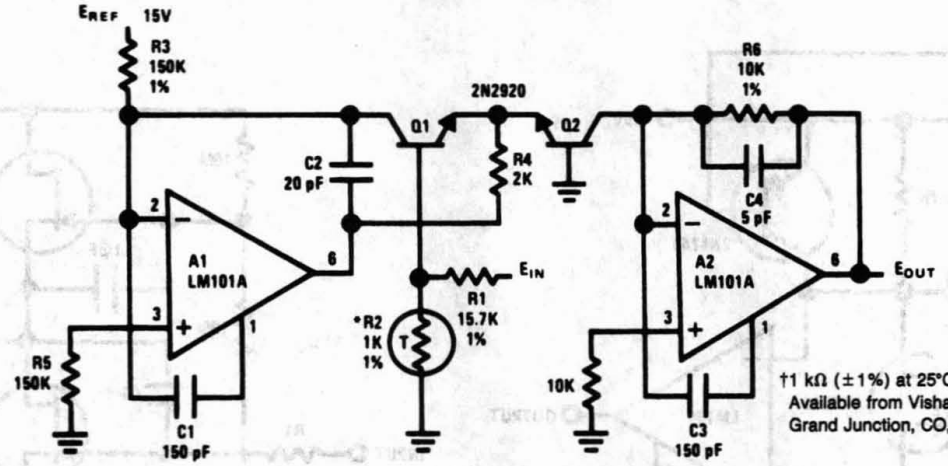
Fast Log Generator



†1 kΩ (±1%) at 25°C, +3500 ppm/°C. Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

TL/H/7057–89

Anti-Log Generator

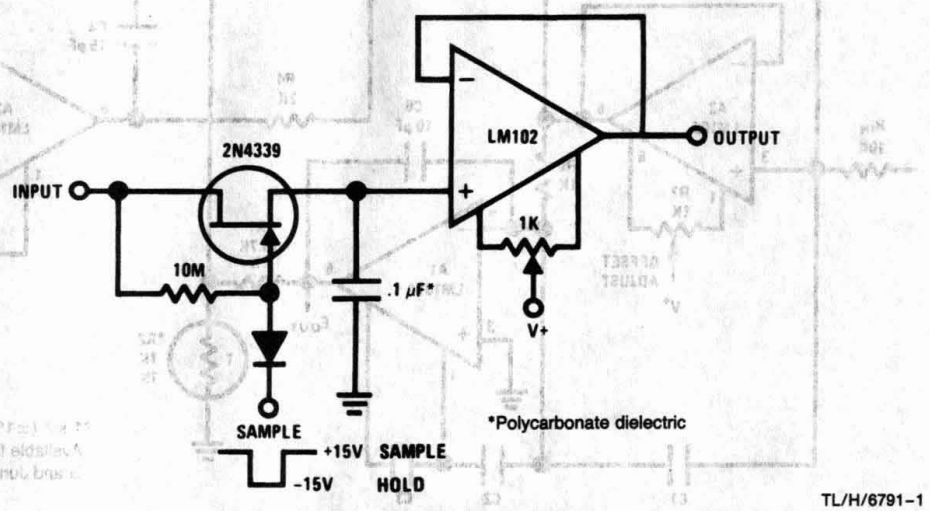


†1 kΩ (±1%) at 25°C, +3500 ppm/°C. Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

TL/H/7057–90

FET Circuit Applications

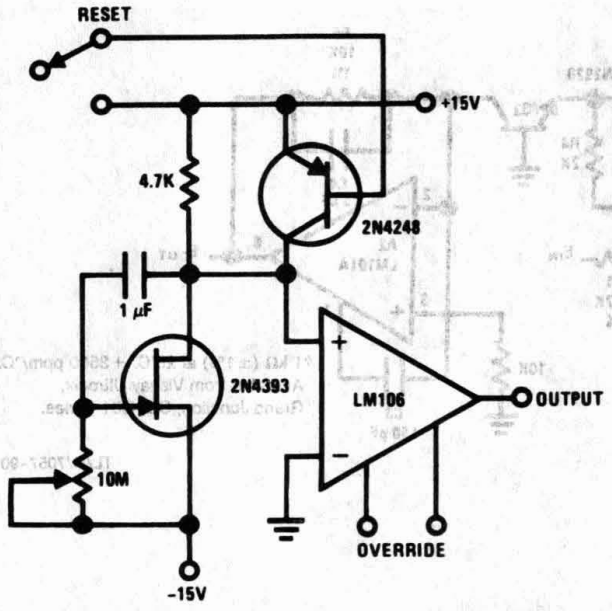
National Semiconductor
Application Note 32



TL/H/6791–1

Sample and Hold With Offset Adjustment

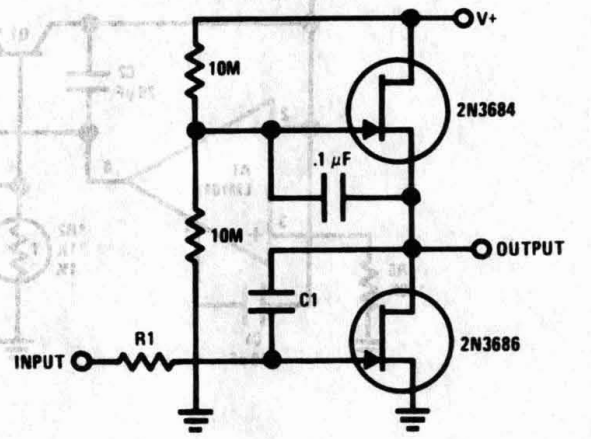
The 2N4339 JFET was selected because of its low I_{GSS} (<100 pA), very-low $I_{D(OFF)}$ (<50 pA) and low pinchoff voltage. Leakages of this level put the burden of circuit performance on clean, solder-resin free, low leakage circuit layout.



TL/H/6791–2

Long Time Comparator

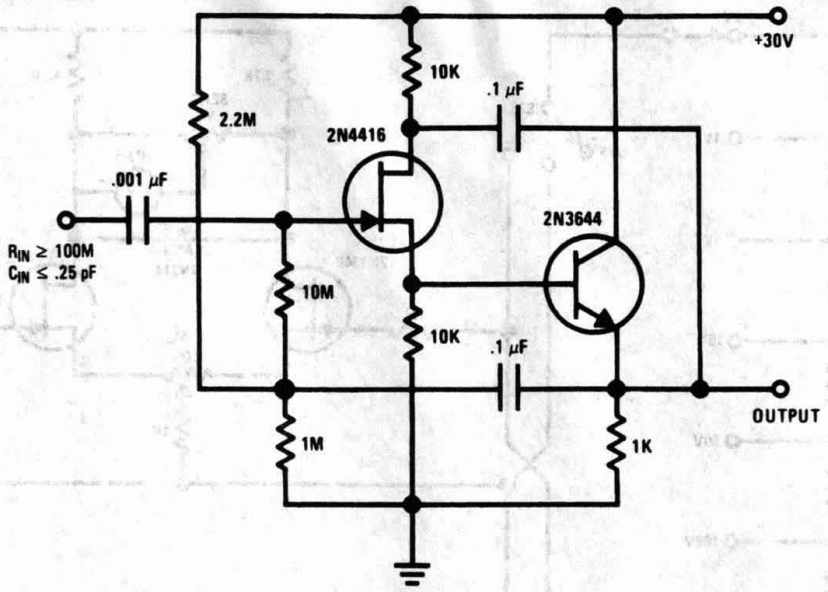
The 2N4393 is operated as a Miller integrator. The high Y_{fs} of the 2N4393 (over 12,000 μmhos @ 5 mA) yields a stage gain of about 60. Since the equivalent capacitance looking into the gate is C times gain and the gate source resistance can be as high as 10 MΩ, time constants as long as a minute can be achieved.



TL/H/6791–3

JFET AC Coupled Integrator

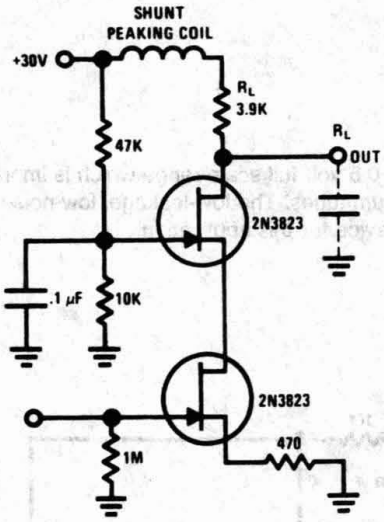
This circuit utilizes the "μ-amp" technique to achieve very high voltage gain. Using C_1 in the circuit as a Miller integrator, or capacitance multiplier, allows this simple circuit to handle very long time constants.



TL/H/6791–4

Ultra-High Z_{IN} AC Unity Gain Amplifier

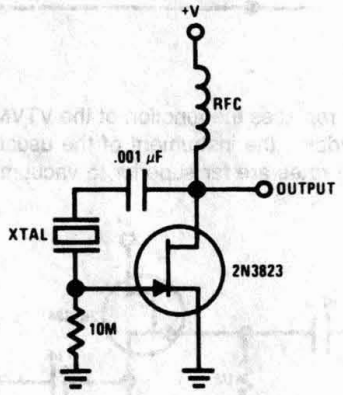
Nothing is left to chance in reducing input capacitance. The 2N4416, which has low capacitance in the first place, is operated as a source follower with bootstrapped gate bias resistor and drain. Any input capacitance you get with this circuit is due to poor layout techniques.



TL/H/6791–5

FET Cascode Video Amplifier

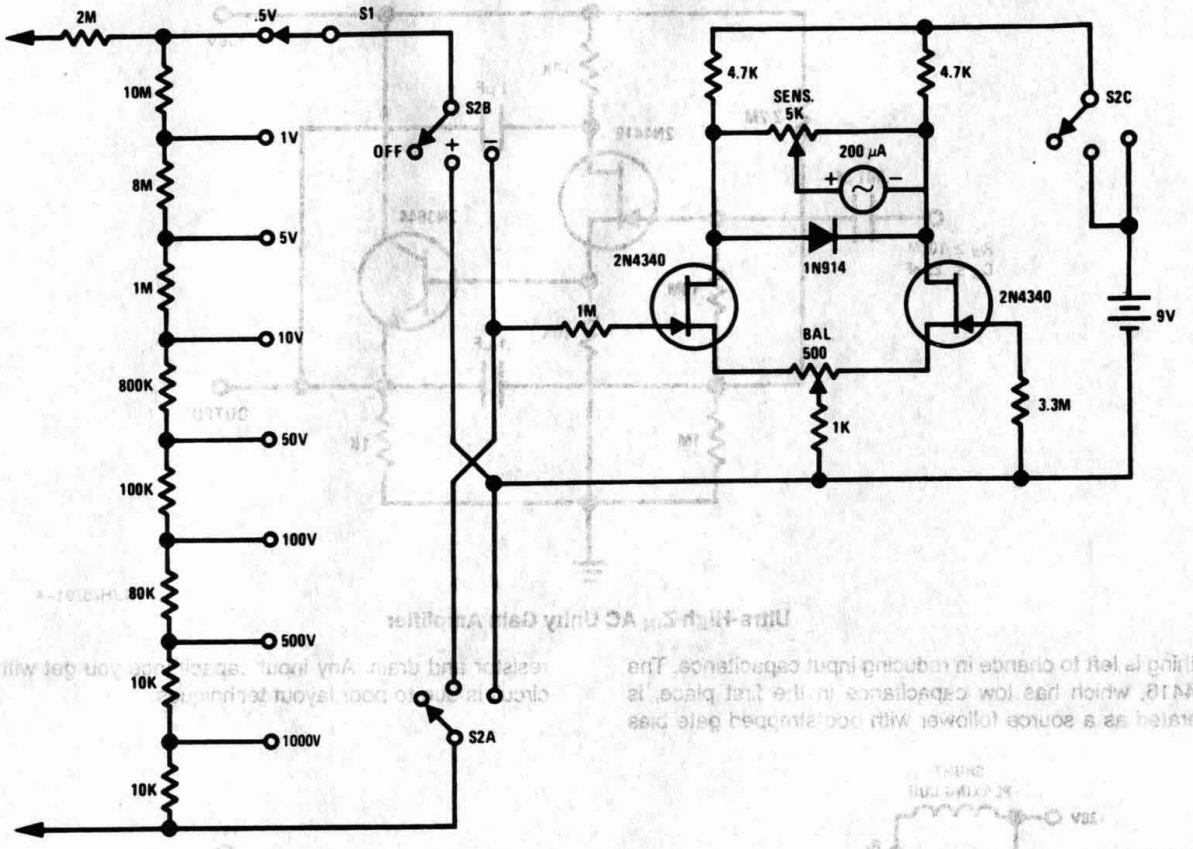
The FET cascode video amplifier features very low input loading and reduction of feedback to almost zero. The 2N3823 is used because of its low capacitance and high Y_{fs}. Bandwidth of this amplifier is limited by R_L and load capacitance.



TL/H/6791–6

JFET Pierce Crystal Oscillator

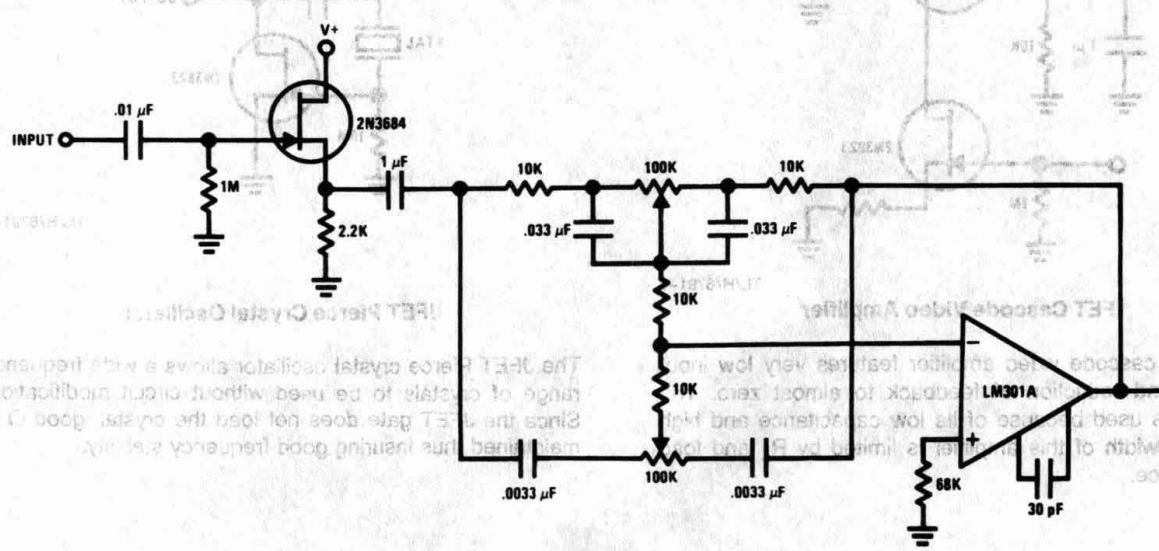
The JFET Pierce crystal oscillator allows a wide frequency range of crystals to be used without circuit modification. Since the JFET gate does not load the crystal, good Q is maintained thus insuring good frequency stability.



TL/H/6791–7

FETVM-FET Voltmeter

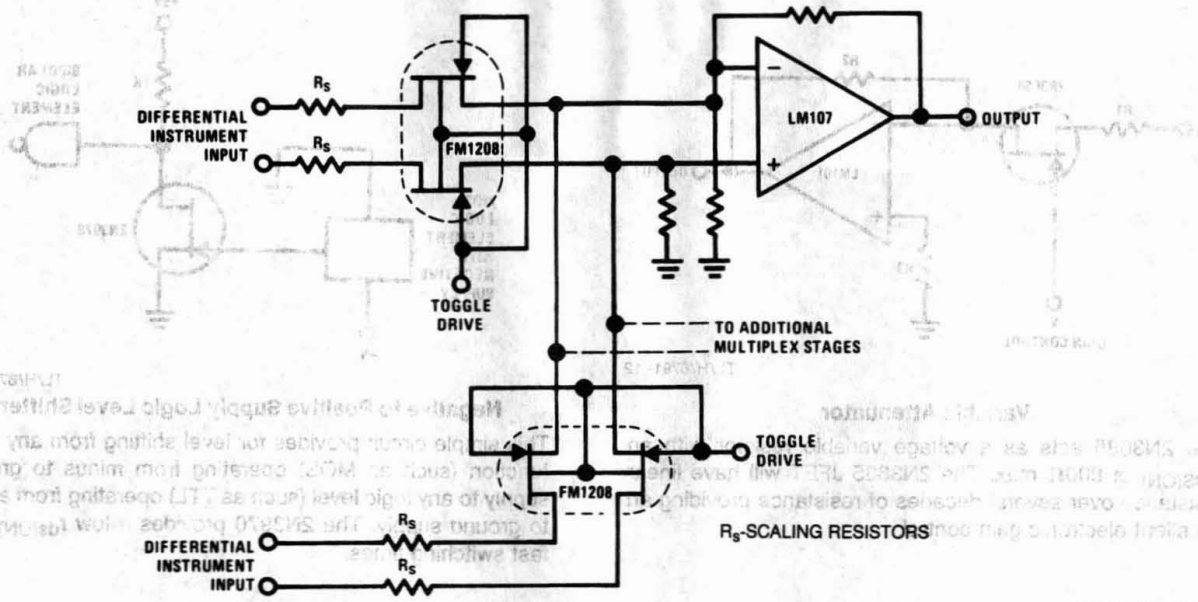
This FETVM replaces the function ot the VTVM while at the same time ridding the instrument of the usual line cord. In addition, drift rates are far superior to vacuum tube circuits allowing a 0.5 volt full scale range which is impractical with most vacuum tubes. The low-leakage, low-noise 2N4340 is an ideal device for this application.



TL/H/6791–8

HI-FI Tone Control Circuit (High Z Input)

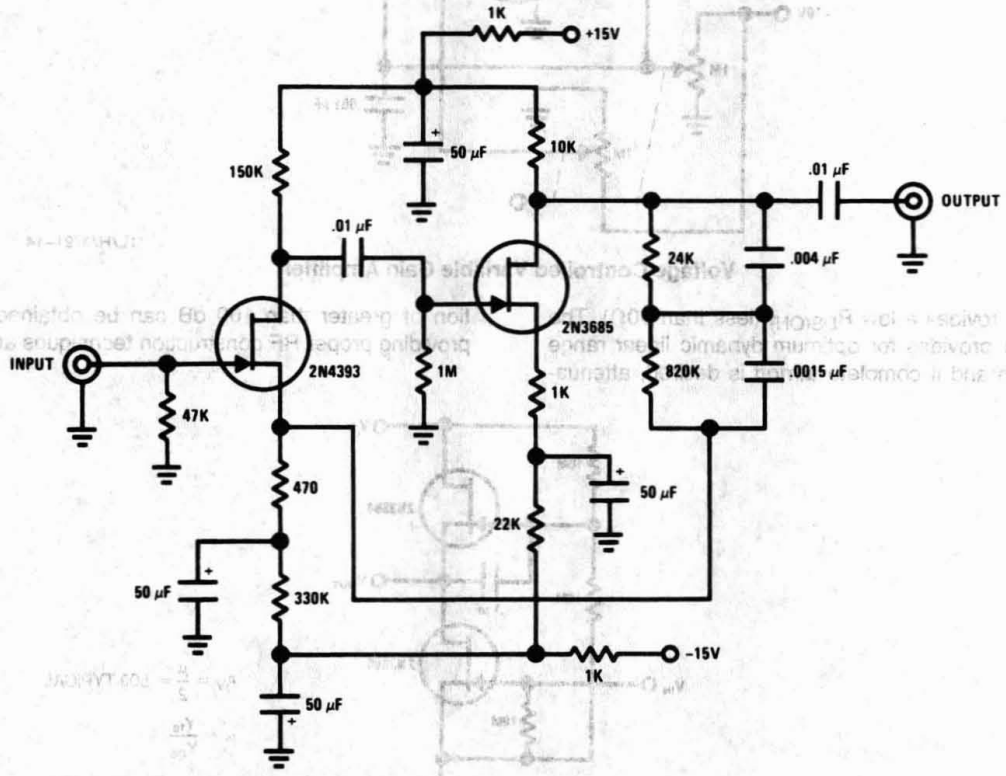
The 2N3684 JFET provides the function of a high input impedance and low noise characteristics to buffer an op amp-operated feedback type tone control circuit.



TL/H/6791–10

Differential Analog Switch

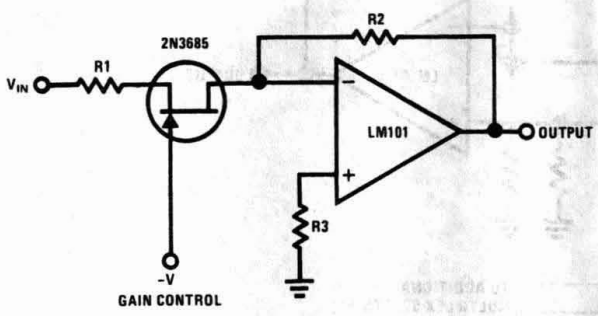
The FM1208 monolithic dual is used in a differential multiplexer application where $R_{DS(ON)}$ should be closely matched. Since $R_{DS(ON)}$ for the monolithic dual tracks at better than ±1% over wide temperature ranges (−25 to +125°C), this makes it an unusual but ideal choice for an accurate multiplexer. This close tracking greatly reduces errors due to common mode signals.



TL/H/6791–11

Magnetic-Pickup Phono Preamplifier

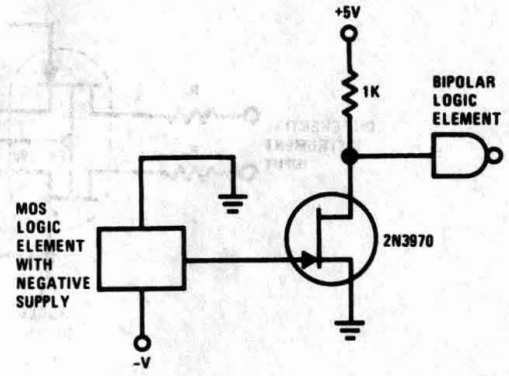
This preamplifier provides proper loading to a reluctance phono cartridge. It provides approximately 25 dB of gain at 1 kHz (2.2 mV input for 100 mV output), it features S + N/N ratio of better than −70 dB (referenced to 10 mV input at 1 kHz) and has a dynamic range of 84 dB (referenced to 1 kHz). The feedback provides for RIAA equalization.



TL/H/6791–12

Variable Attenuator

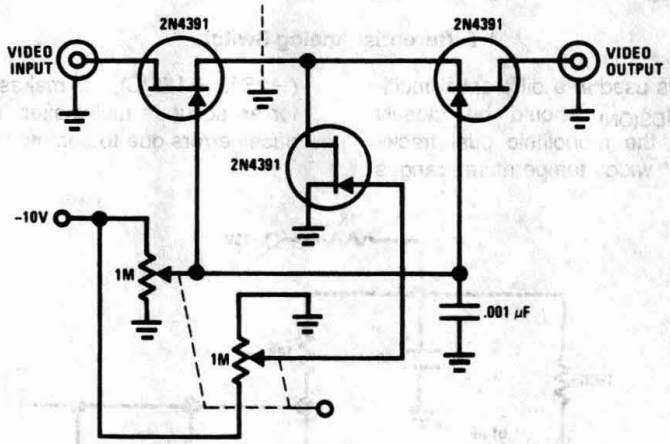
The 2N3685 acts as a voltage variable resistor with an $R_{DS(ON)}$ of 800Ω max. The 2N3685 JFET will have linear resistance over several decades of resistance providing an excellent electronic gain control.



TL/H/6791–13

Negative to Positive Supply Logic Level Shifter

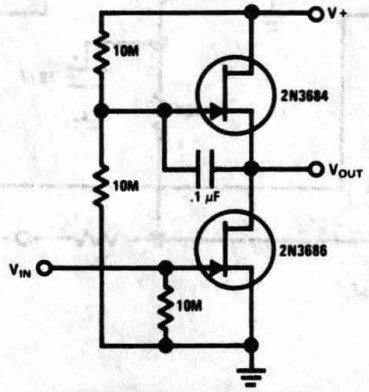
This simple circuit provides for level shifting from any logic function (such as MOS) operating from minus to ground supply to any logic level (such as TTL) operating from a plus to ground supply. The 2N3970 provides a low $r_{ds(ON)}$ and fast switching times.



TL/H/6791–14

Voltage Controlled Variable Gain Amplifier

The 2N4391 provides a low $R_{DS(ON)}$ (less than 30Ω). The tee attenuator provides for optimum dynamic linear range for attenuation and if complete turnoff is desired, attenuation of greater than 100 dB can be obtained at 10 MHz providing proper RF construction techniques are employed.



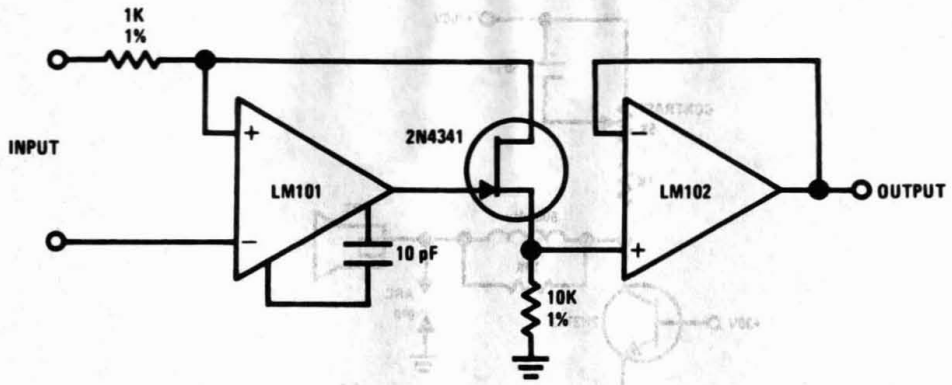
$$A_V = \frac{\mu}{2} = 500 \text{ TYPICAL}$$

$$\mu = \frac{Y_{fs}}{Y_{os}}$$

TL/H/6791–15

Ultra-High Gain Audio Amplifier

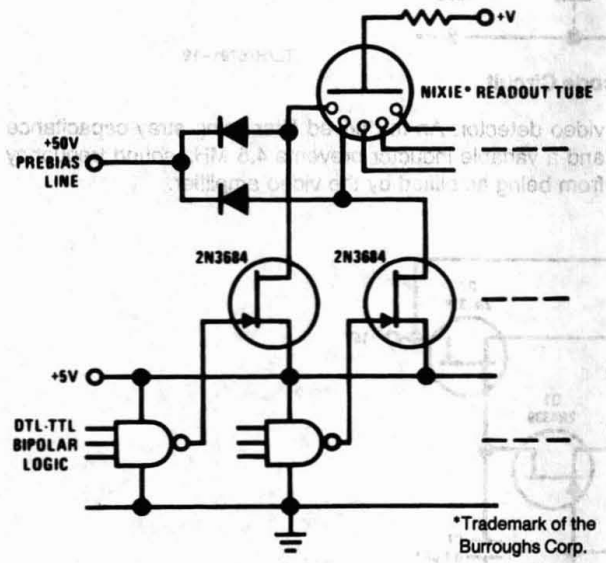
Sometimes called the "JFET" μ amp," this circuit provides a very low power, high gain amplifying function. Since μ of a JFET increases as drain current decreases, the lower drain current is, the more gain you get. You do sacrifice input dynamic range with increasing gain, however.



TL/H/6791–16

Level-Shifting-Isolation Amplifier

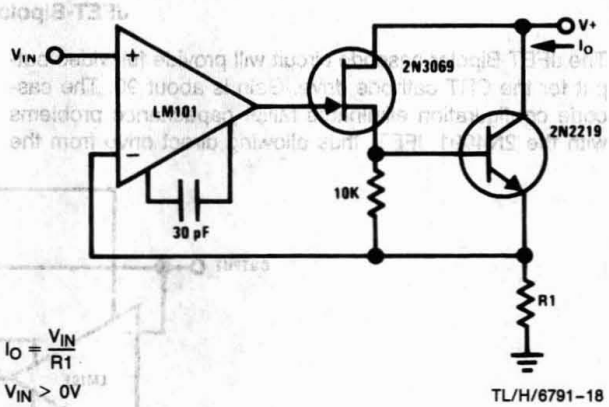
The 2N4341 JFET is used as a level shifter between two op amps operated at different power supply voltages. The JFET is ideally suited for this type of application because $I_D = I_S$.



TL/H/6791–17

FET Nixie* Drivers

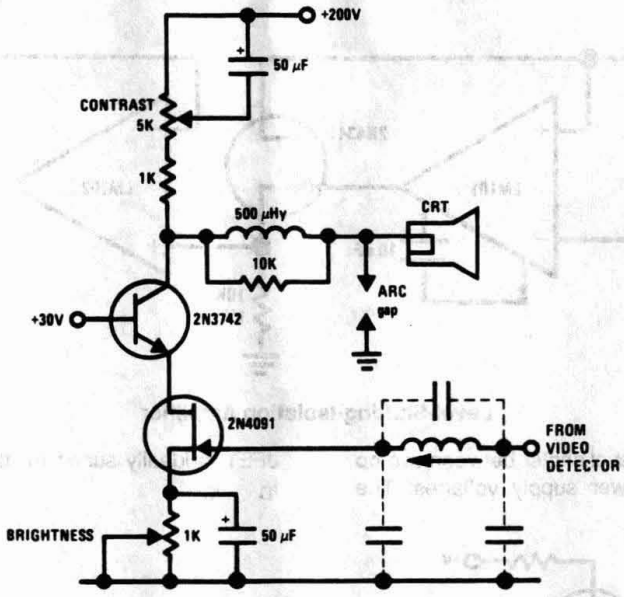
The 2N3684 JFETs are used as Nixie tube drivers. Their V_p of 2-5 volts ideally matches DTL-TTL logic levels. Diodes are used to a +50 volt prebias line to prevent breakdown of the JFETs. Since the 2N3684 is in a TO-72 (4 lead TO-18) package, none of the circuit voltages appear on the can. The JFET is immune to almost all of the failure mechanisms found in bipolar transistors used for this application.



TL/H/6791–18

Precision Current Sink

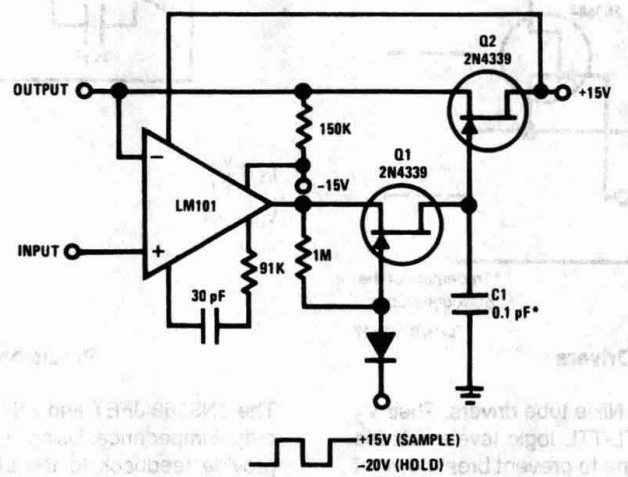
The 2N3069 JFET and 2N2219 bipolar have inherently high output impedance. Using R_1 as a current sensing resistor to provide feedback to the LM101 op amp provides a large amount of loop gain for negative feedback to enhance the true current sink nature of this circuit. For small current values, the 10k resistor and 2N2219 may be eliminated if the source of the JFET is connected to R_1.



TL/H/6791–19

JFET-Bipolar Cascode Circuit

The JFET-Bipolar cascode circuit will provide full video output for the CRT cathode drive. Gain is about 90. The cascode configuration eliminates Miller capacitance problems with the 2N4091 JFET, thus allowing direct drive from the video detector. An m derived filter using stray capacitance and a variable inductor prevents 4.5 MHz sound frequency from being amplified by the video amplifier.

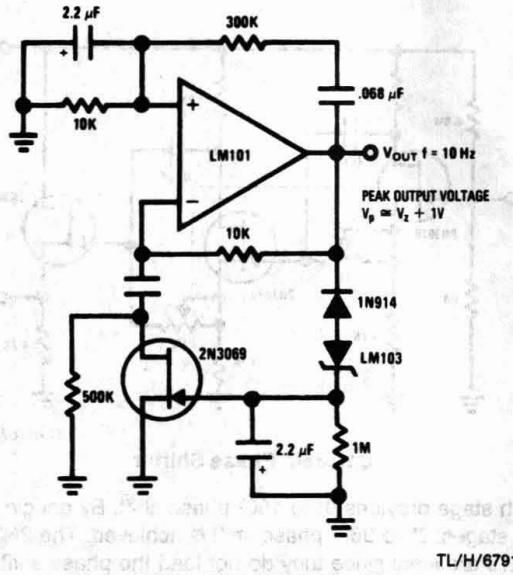


*Polycarbonate dielectric capacitor

TL/H/6791–20

Low Drift Sample and Hold

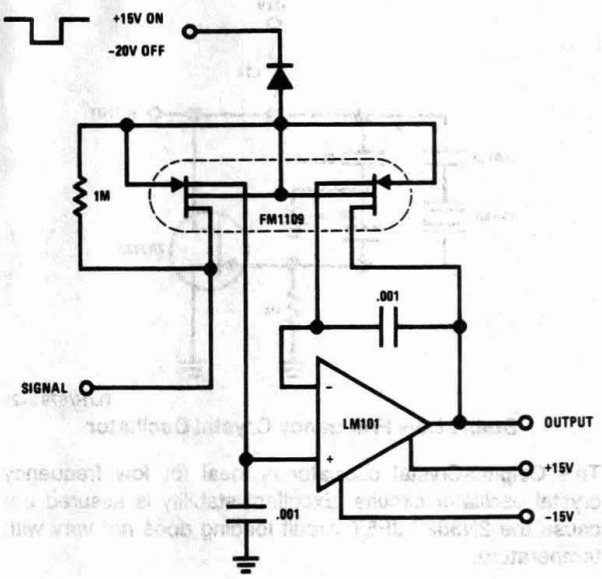
The JFETs, Q_1 and Q_2, provide complete buffering to C_1, the sample and hold capacitor. During sample, Q_1 is turned on and provides a path, $r_{ds(ON)}$, for charging C_1. During hold, Q_1 is turned off thus leaving Q_1 $I_{D(OFF)}$ (<50 pA) and Q_2 I_{GSS} (<100 pA) as the only discharge paths. Q_2 serves a buffering function so feedback to the LM101 and output current are supplied from its source.



TL/H/6791–21

Wein Bridge Sine Wave Oscillator

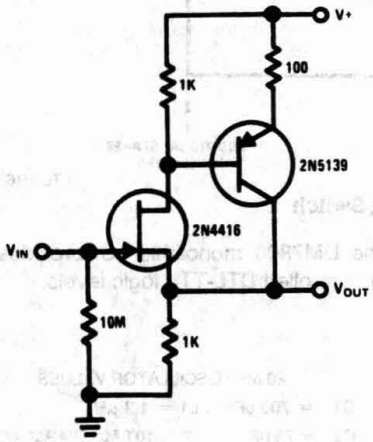
The major problem in producing a low distortion, constant amplitude sine wave is getting the amplifier loop gain just right. By using the 2N3069 JFET as a voltage variable resistor in the amplifier feedback loop, this can be easily achieved. The LM103 zener diode provides the voltage reference for the peak sine wave amplitude; this is rectified and fed to the gate of the 2N3069, thus varying its channel resistance and, hence, loop gain.



TL/H/6791–22

JFET Sample and Hold Circuit

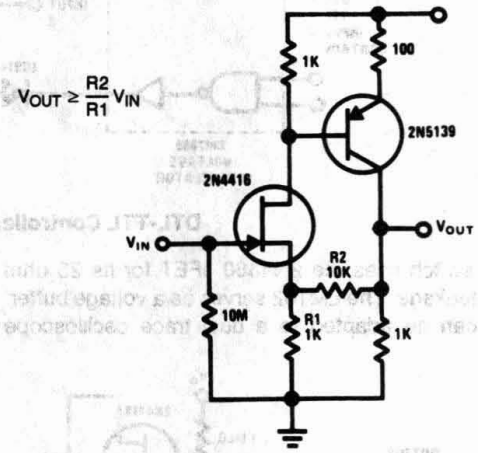
The logic voltage is applied simultaneously to the sample and hold JFETs. By matching input impedance and feedback resistance and capacitance, errors due to $r_{ds(ON)}$ of the JFETs is minimized. The inherent matched $r_{ds(ON)}$ and matched leakage currents of the FM1109 monolithic dual greatly improve circuit performance.



TL/H/6791–23

High Impedance Low Capacitance Wideband Buffer

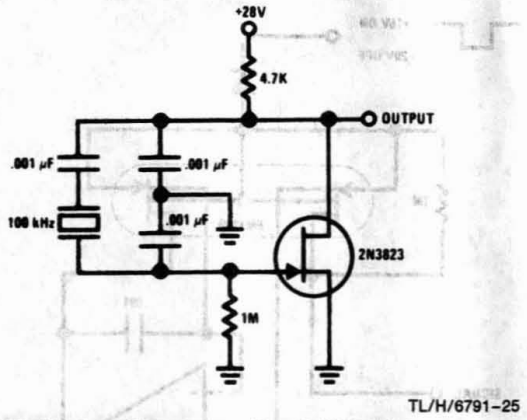
The 2N4416 features low input capacitance which makes this compound-series feedback buffer a wide-band unity gain amplifier.



TL/H/6791–24

High Impedance Low Capacitance Amplifier

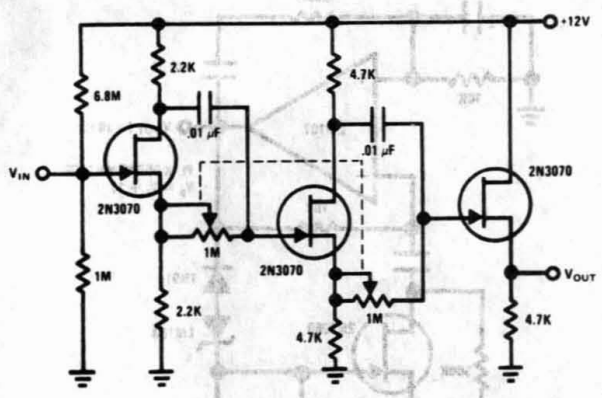
This compound series-feedback circuit provides high input impedance and stable, wide-band gain for general purpose video amplifier applications.



TL/H/6791–25

Stable Low Frequency Crystal Oscillator

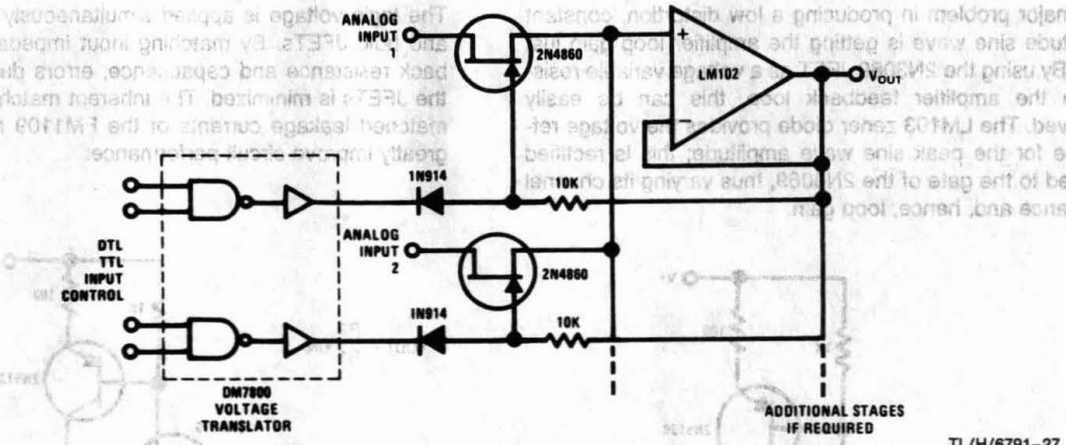
This Colpitts-Crystal oscillator is ideal for low frequency crystal oscillator circuits. Excellent stability is assured because the 2N3823 JFET circuit loading does not vary with temperature.



TL/H/6791–26

0 to 360° Phase Shifter

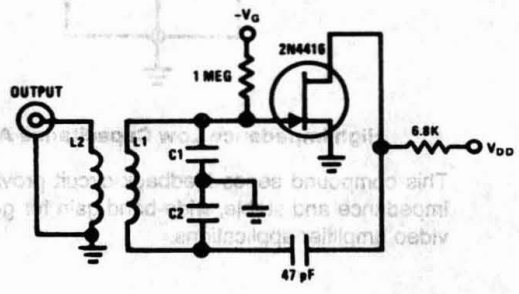
Each stage provides 0° to 180° phase shift. By ganging the two stages, 0° to 360° phase shift is achieved. The 2N3070 JFETs are ideal since they do not load the phase shift networks.



TL/H/6791–27

DTL-TTL Controlled Buffered Analog Switch

This analog switch uses the 2N4860 JFET for its 25 ohm r_{ON} and low leakage. The LM102 serves as a voltage buffer. This circuit can be adapted to a dual trace oscilloscope chopper. The DM7800 monolithic I.C. provides adequate switch drive controlled DTL-TTL logic levels.



20 MHz OSCILLATOR VALUES

C1 ≅ 700 pF L1 = 1.3 μH

C2 = 75 pF L2 = 10T 3/8" DIA 3/4" LONG

V_{DD} = 16V I_D = 1 mA

20 MHz OSCILLATOR PERFORMANCE

LOW DISTORTION 20 MHz OSC.

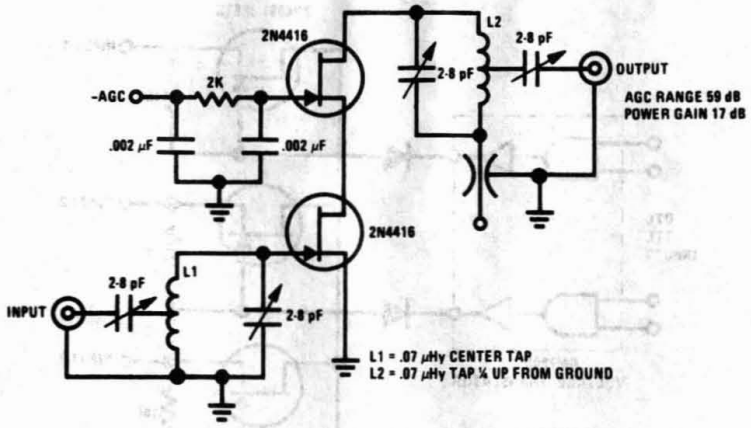
2ND HARMONIC −60 dB

3RD HARMONIC > −70 dB

TL/H/6791–28

Low Distortion Oscillator

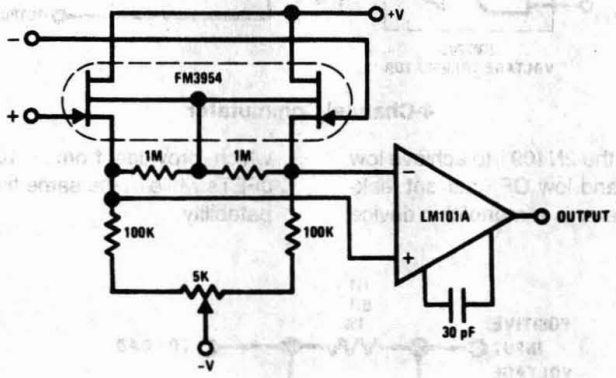
The 2N4416 JFET is capable of oscillating in a circuit where harmonic distortion is very low. The JFET local oscillator is excellent when a low harmonic content is required for a good mixer circuit.



TL/H/6791–29

200 MHz Cascode Amplifier

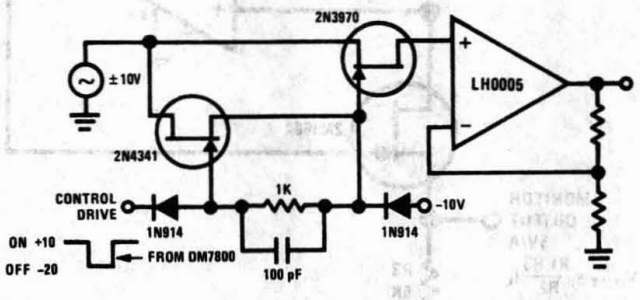
This 200 MHz JFET cascode circuit features low crossmodulation, large-signal handling ability, no neutralization, and AGC controlled by biasing the upper cascode JFET. The only special requirement of this circuit is that I_{DSS} of the upper unit must be greater than that of the lower unit.



TL/H/6791–30

FET Op Amp

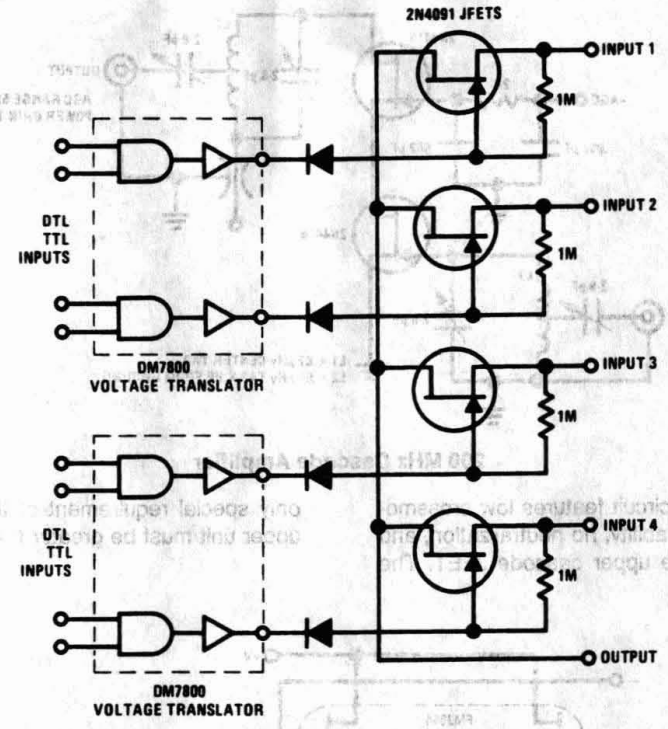
The FM3954 monolithic-dual provides an ideal low-offset, low-drift buffer function for the LM101A op amp. The excellent matching characteristics of the FM3954 track well over its bias current range thus improving common mode rejection.



TL/H/6791–31

High Toggle Rate High Frequency Analog Switch

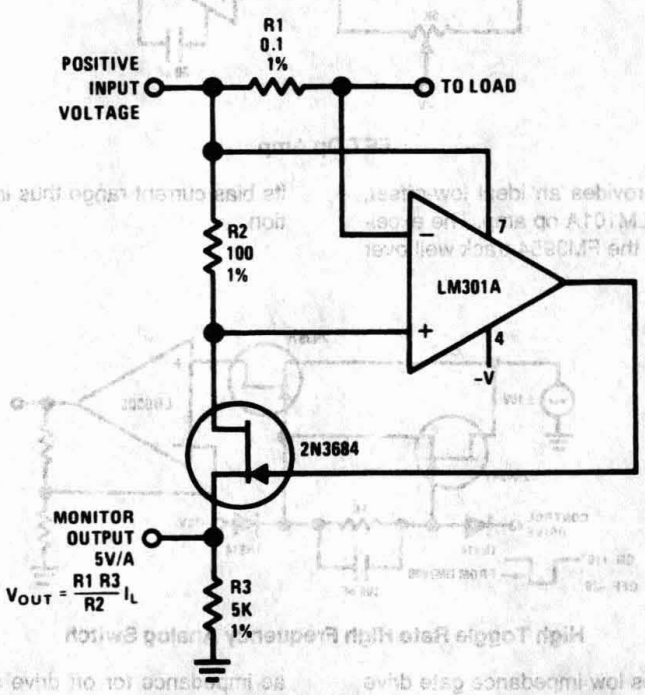
This commutator circuit provides low impedance gate drive to the 2N3970 analog switch for both on and off drive conditions. This circuit also approaches the ideal gate drive conditions for high frequency signal handling by providing a low ac impedance for off drive and high ac impedance for on drive to the 2N3970. The LH0005 op amp does the job of amplifying megahertz signals.



TL/H/6791–32

4-Channel Commutator

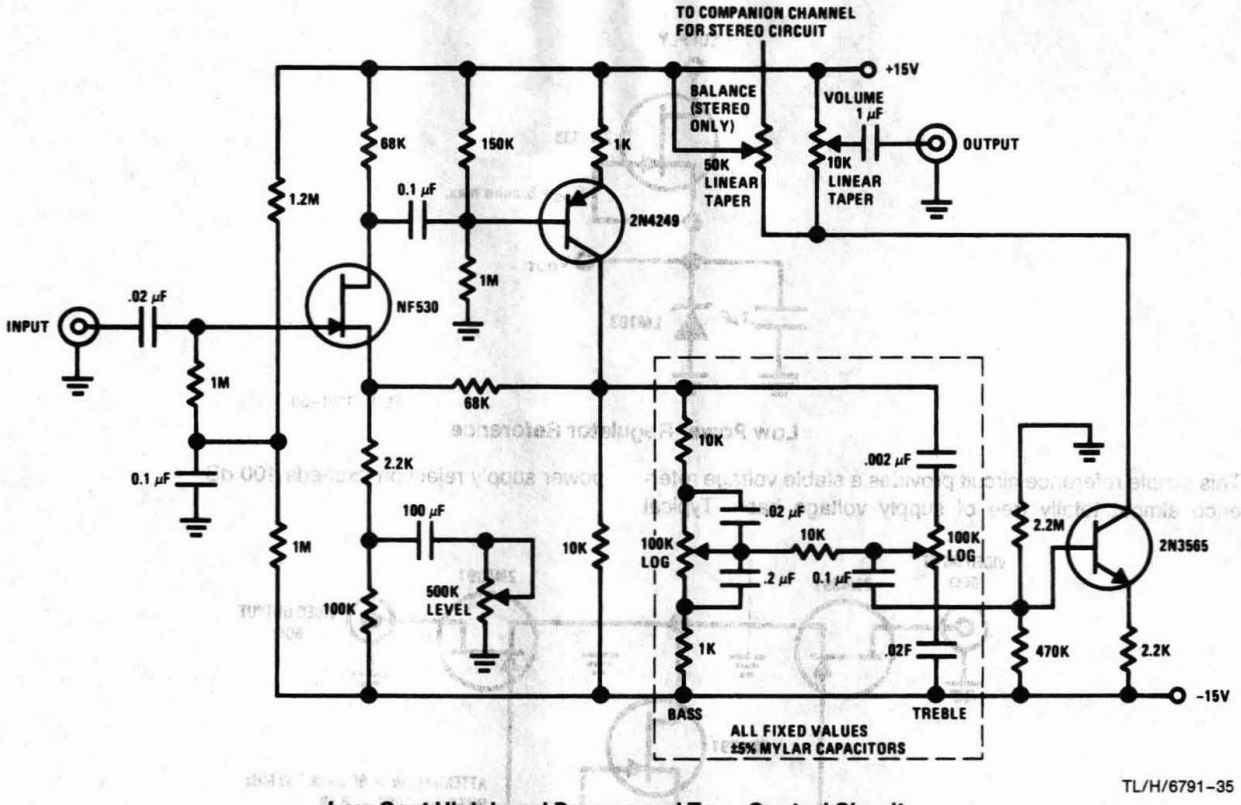
This 4-channel commutator uses the 2N4091 to achieve low channel ON resistance (<30Ω) and low OFF current leakage. The DM7800 voltage translator is a monolithic device which provides from +10V to −20V gate drive to the JFETs while at the same time providing DTL-TTL logic compatability.



TL/H/6791–34

Current Monitor

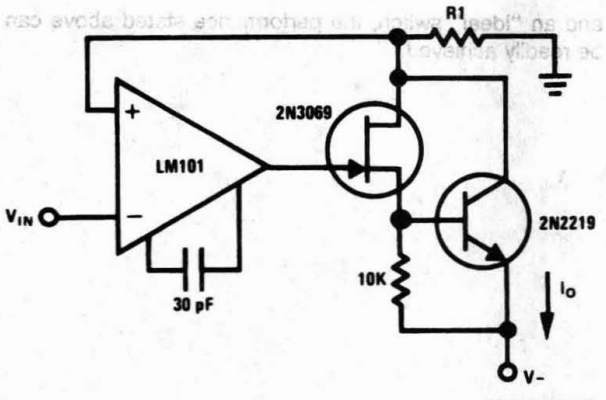
R_1 senses current flow of a power supply. The JFET is used as a buffer because $I_D = I_S$, therefore the output monitor voltage accurately reflects the power supply current flow.



TL/H/6791–35

Low Cost High Level Preamp and Tone Control Circuit

This preamp and tone control uses the JFET to its best advantage; as a low noise high input impedance device. All device parameters are non-critical yet the circuit achieves harmonic distortion levels of less than 0.05% with a S/N ratio of over 85 dB. The tone controls allow 18 dB of cut and boost; the amplifier has a 1 volt output for 100 mV input at maximum level.

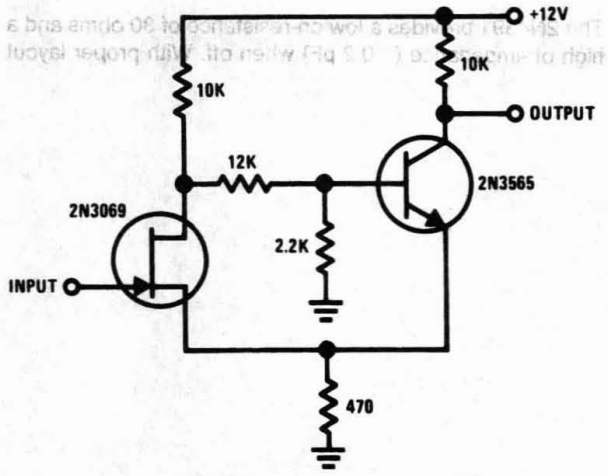


TL/H/6791–36

$$I_O = \frac{V_{IN}}{RI} \qquad V_{IN} \leq 0V$$

Precision Current Source

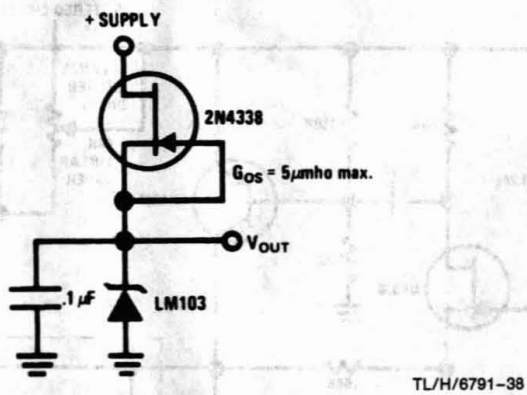
The 2N3069 JFET and 2N2219 bipolar serve as voltage devices between the output and the current sensing resistor, R_1. The LM101 provides a large amount of loop gain to assure that the circuit acts as a current source. For small values of current, the 2N2219 and 10k resistor may be eliminated with the output appearing at the source of the 2N3069.



TL/H/6791–37

Schmitt Trigger

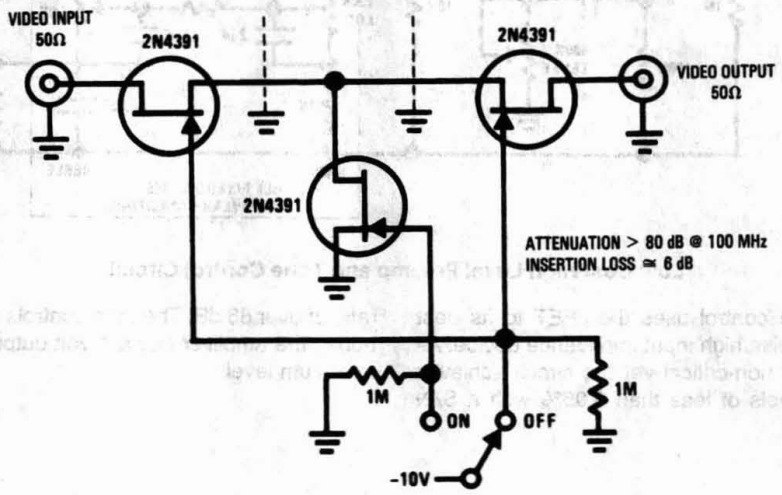
This Schmitt trigger circuit is "emitter coupled" and provides a simple comparator action. The 2N3069 JFET places very little loading on the measured input. The 2N3565 bipolar is a high h_{FE} transistor so the circuit has fast transition action and a distinct hysteresis loop.



TL/H/6791–38

Low Power Regulator Reference

This simple reference circuit provides a stable voltage reference almost totally free of supply voltage hash. Typical power supply rejection exceeds 100 dB.



TL/H/6791–39

High Frequency Switch

The 2N4391 provides a low on-resistance of 30 ohms and a high off-impedance (<0.2 pF) when off. With proper layout and an "ideal" switch, the performance stated above can be readily achieved.

Precision IC Comparator Runs from +5V Logic Supply

National Semiconductor
Application Note 41

Robert J. Widlar
Apartado Postal 541
Puerto Vallarta, Jalisco
Mexico

introduction

In digital systems, it is sometimes necessary to convert low level analog signals into digital information. An example of this might be a detector for the illumination level of a photodiode. Another would be a zero crossing detector for a magnetic transducer such as a magnetometer or a shaft-position pickoff. These transducers have low-level outputs, with currents in the low microamperes or voltages in the low millivolts. Therefore, low level circuitry is required to condition these signals before they can drive logic circuits.

A voltage comparator can perform many of these precision functions. A comparator is essentially a high-gain op amp designed for open loop operation. The function of a comparator is to produce a logic "one" on the output with a positive signal between its two inputs or a logic "zero" with a negative signal between the inputs. Threshold detection is accomplished by putting a reference voltage on one input and the signal on the other. Clearly, an op amp can be used as a comparator, except that its response time is in the tens of microseconds which is often too slow for many applications.

A unique comparator design will be described here along with some of its applications in digital systems. Unlike older IC comparators or op amps, it will operate from the same 5V supply as DTL or TTL logic circuits. It will also operate with the single negative supply used with MOS logic. Hence, low level functions can be performed without the extra supply voltages previously required.

The versatility of the comparator along with the minimal circuit loading and considerable precision recommend it for many uses, in digital systems, other than the detection of low level signals. It can be used as an oscillator or multivibrator, in digital interface circuitry and even for low voltage analog circuitry. Some of these applications will also be discussed.

circuit description

In order to understand how to use this comparator, it is necessary to look briefly at the circuit configuration. *Figure 1* shows a simplified schematic of the device. PNP transistors

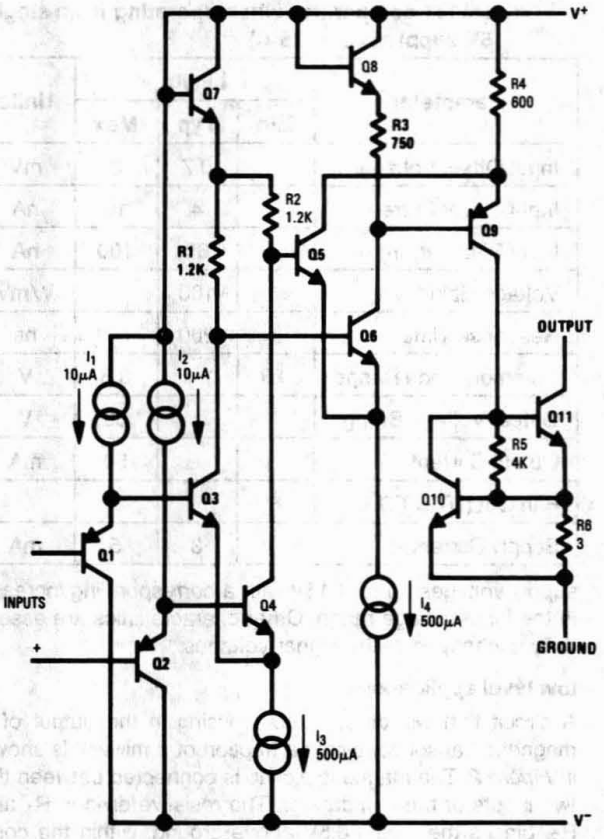


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Figure 1. Simplified schematic of the comparator

buffer the differential input stage to get low input currents without sacrificing speed. The PNP's drive a standard NPN differential stage, Q_3 and Q_4. The output of this stage is further amplified by the Q_5—Q_6 pair. This feeds Q_9 which provides additonal gain and drives the output stage. Current sources are used to determine the bias currents, so that performance is not greatly affected by supply voltages.

The output transistor is Q_{11}, and it is protected by Q_{10} and R_6 which limit the peak output current. The output lead, since it is not connected to any other point in the circuit, can either be returned to the positive supply through a pull-up resistor or switch loads that are connected to a voltage higher than the positive supply voltage. The circuit will operate from a single supply if the negative supply lead is connected to ground. However, if a negative supply is available, it can be used to increase the input common mode range.

Table I summarizes the performance of the comparator when operating from a 5V supply. The circuit will work with

Table I. Important electrical characteristics of the LM111 comparator when operating from single, 5V supply (T_A = 25°C)

Parameter	Limits			Units
	Min	Typ	Max	
Input Offset Voltage		0.7	3	mV
Input Offset Current		4	10	nA
Input Bias Current		60	100	nA
Voltage Gain		100		V/mV
Response Time		200		ns
Common Mode Range	0.3		3.8	V
Output Voltage Swing			50	V
Output Current			50	mA
Fan Out (DTL/TTL)	8			
Supply Current		3	5	mA

supply voltages up to ±15V with a corresponding increase in the input voltage range. Other characteristics are essentially unchanged at the higher voltages.

low level applications

A circuit that will detect zero crossing in the output of a magnetic transducer within a fraction of a millivolt is shown in *Figure 2*. The magnetic pickup is connected between the two inputs of the comparator. The resistive divider, R_1 and R_2, biases the inputs 0.5V above ground, within the common mode range of the IC. The output will directly drive DTL or TTL. The exact value of the pull up resistor, R_5, is determined by the speed required from the circuit since it must drive any capacitive loading for positive-going output signals. An optional offset-balancing circuit using R_3 and R_4 is included in the schematic.

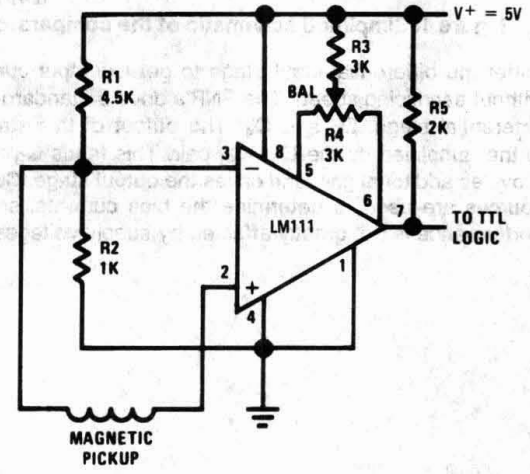

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Figure 2. Zero crossing detector for magnetic transducer

Figure 3 shows a connection for operating with MOS logic. This is a level detector for a photodiode that operates off a −10V supply. The output changes state when the diode current reaches 1 μA. Even at this low current, the error contributed by the comparator is less than 1%.

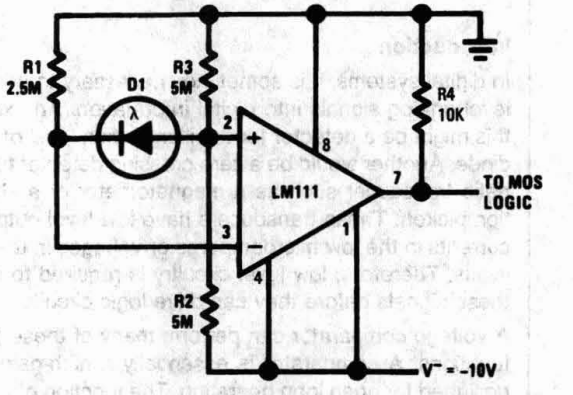

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Figure 3. Level detector for photodiode

Higher threshold currents can be obtained by reducing R_1, R_2 and R_3 proportionally. At the switching point, the voltage across the photodiode is nearly zero, so its leakage current does not cause an error. The output switches between ground and −10V, driving the data inputs of MOS logic directly.

The circuit in *Figure 3* can, of course, be adapted to work with a 5V supply. At any rate, the accuracy of the circuit will depend on the supply-voltage regulation, since the reference is derived from the supply. *Figure 4* shows a method

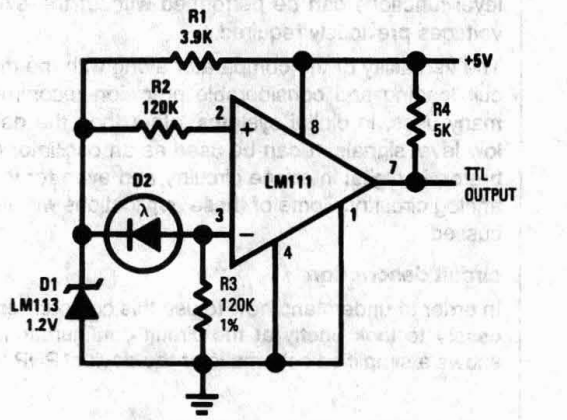

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Figure 4. Precision level detector for photodiode

of making performance independent of supply voltage. D_1 is a temperature-compensated reference diode with a 1.23V breakdown voltage. It acts as a shunt regulator and delivers a stable voltage to the comparator. When the diode current is large enough (about 10 μA) to make the voltage drop

across R_3 equal to the breakdown voltage of D_1, the output will change state. R_2 has been added to make the threshold error proportional to the offset current of the comparator, rather than the bias current. It can be eliminated if the bias current error is not considered significant.

A zero crossing detector that drives the data input of MOS logic is shown in *Figure 5*. Here, both a positive supply and

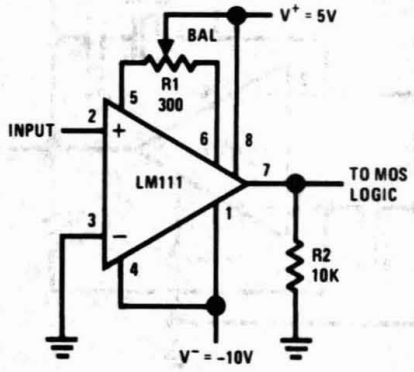

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Figure 5. Zero crossing detector driving MOS logic

the −10V supply for MOS circuits are used. Both supplies are required for the circuit to work with zero common-mode voltage. An alternate balancing scheme is also shown in the schematic. It differs from the circuit in *Figure 2* in that it raises the input-stage current by a factor of three. This increases the rate at which the input voltage follows rapidly-changing signals from 7V/μs to 18V/μs. This increased common-mode slew can be obtained without the balancing potentiometer by shorting both balance terminals to the positive-supply terminal. Increased input bias current is the price that must be paid for the faster operation.

digital interface circuits

Figure 6 shows an interface between high-level logic and DTL or TTL. The input signal, with 0V and 30V logic states is attenuated to 0V and 5V by R_1 and R_2. R_3 and R_4 set up a 2.5V threshold level for the comparator so that it switches when the input goes through 15V. The response time of the circuit can be controlled with C_1, if desired, to make it insensitive to fast noise spikes. Because of the low error currents of the LM111, it is possible to get input impedances even higher than the 300 kΩ obtained with the indicated resistor values.

The comparator can be strobed, as shown in *Figure 6*, by the addition of Q_1 and R_5. With a logic one on the base of Q_1, approximately 2.5 mA is drawn out of the strobe terminal of the LM111, making the output high independent of the input signal.

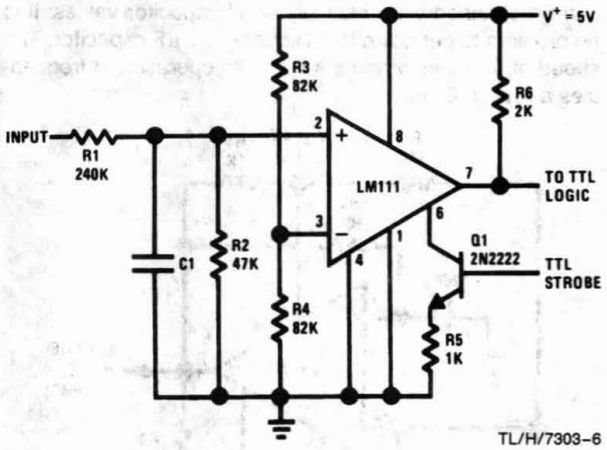

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Figure 6. Circuit for transmitting data between high-level logic and TTL

Sometimes it is necessary to transmit data between digital equipments, yet maintain a high degree of electrical isolation. Normally, this is done with a transformer. However, transformers have problems with low-duty-cycle pulses since they do not preseve the dc level.

The circuit in *Figure 7* is a more satisfactory method of obtaining isolation. At the transmitting end, a TTL gate drives a gallium-arsenide light-emitting diode. The light output is optically coupled to a silicon photodiode, and the comparator detects the photodiode output. The optical coupling makes possible electrical isolation in the thousands of megohms at potentials in the thousands of volts.

The maximum data rate of this circuit is 1 MHz. At lower rates (~200 kHz) R_3 and C_1 can be eliminated.

multivibrators and oscillators

The free-running multivibrator in *Figure 8* is another example of the versatility of the comparator. The inputs are biased within the common mode range by R_1 and R_2. DC stability, which insures starting, is provided by negative feedback through R_3. The negative feedback is reduced at high frequencies by C_1. At some frequency, the positive feedback through R_4 will be greater than the negative feedback; and the circuit will oscillate. For the component values

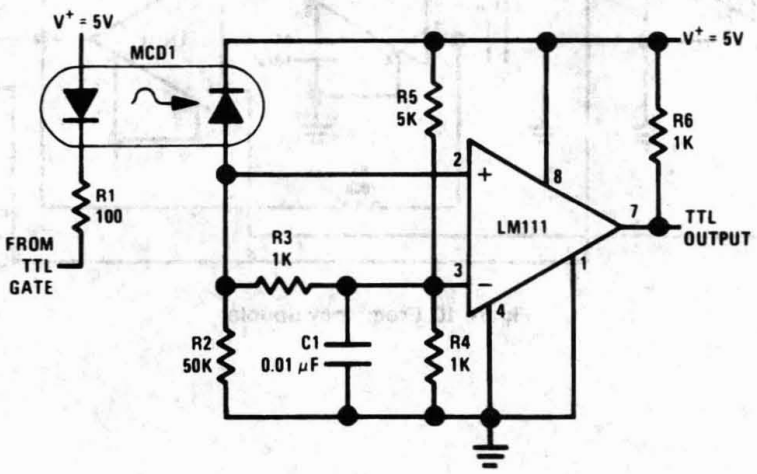

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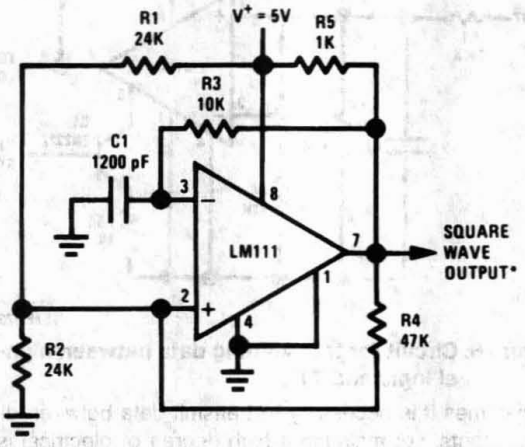
Figure 7. Data transmission system with near-infinite ground isolation

shown, the circuit delivers a 100 kHz square wave output. The frequency can be changed by varying C_1 or by adjusting R_1 through R_4, while keeping their ratios constant.

Because of the low input current of the comparator, large circuit impedances can be used. Therefore, low frequencies can be obtained with relatively-small capacitor values: it is no problem to get down to 1 Hz using a 1 μF capacitor. The speed of the comparator also permits operation at frequencies above 100 kHz.



*TTL or DTL Fanout of two.

Figure 8. Free-running multivibrator

The frequency of oscillation depends almost entirely on the resistance and capacitor values because of the precision of the comparator. Further, the frequency changes by only 1% for a 10% change in supply voltage. Waveform symmetry is also good, but the symmetry can be varied by changing the ratio of R_1 to R_2.

A crystal-controlled oscillator that can be used to generate the clock in slower digital systems is shown in *Figure 9*. It is similar to the free running multivibrator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when transmission through the crystal is at a maximum, so the crystal operates in its series-resonant

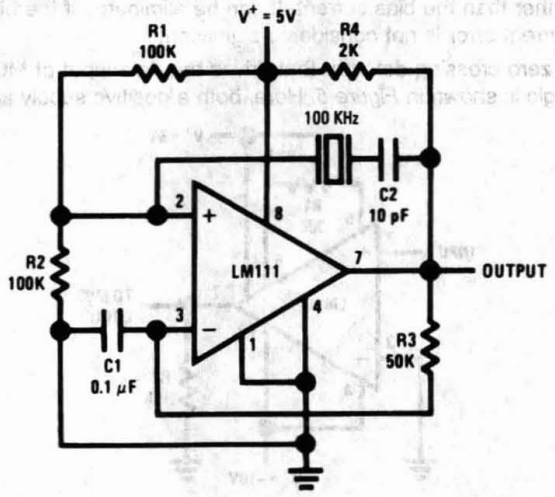


Figure 9. Crystal-controlled oscillator

mode. The high input impedance of the comparator and the isolating capacitor, C_2, minimize loading of the crystal and contribute to frequency stability. As shown, the oscillator delivers a 100 kHz square-wave output.

frequency doubler

In a digital system, it is a relatively simple matter to divide by any integer. However, multiplying by an integer is quite another story especially if operation over a wide frequency range and waveform symmetry are required.

A frequency doubler that satisfies the above requirements is shown in *Figure 10*. A comparator is used to shape the in-

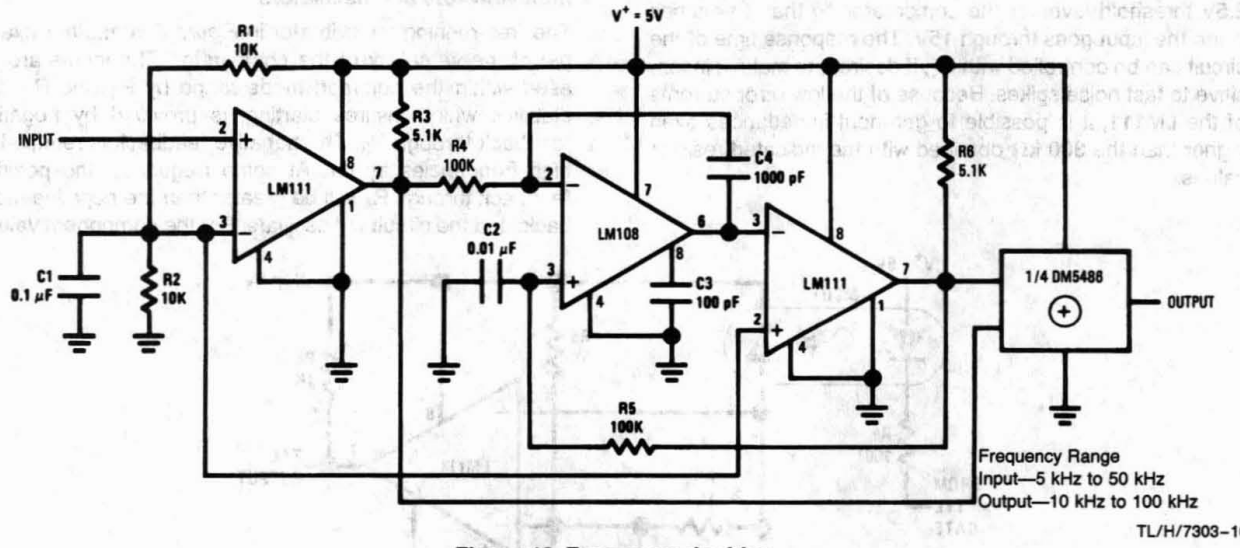


Figure 10. Frequency doubler

put signal and feed it to an integrator. The shaping is required because the input to the integrator must swing between the supply voltage and ground to preserve symmetry in the output waveform. An LM108 op amp, that works from the 5V logic supply, serves as the integrator. This feeds a triangular waveform to a second comparator that detects when the waveform goes through a voltage equal to its average value. Hence, as shown in *Figure 11*, the output of the

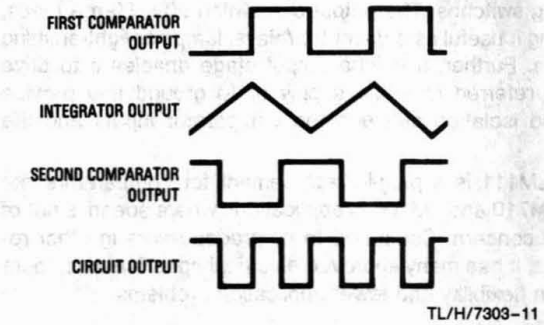


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Figure 11. Waveforms for the frequency doubler

second comparator is delayed by half the duration of the input pulse. The two comparator outputs can then be combined through an exclusive-OR gate to produce the double-frequency output.

With the component values shown, the circuit operates at frequencies from 5 kHz to 50 kHz. Lower frequency operation can be secured by increasing both C_2 and C_4.

application hints

One of the problems encountered in using earlier IC comparators like the LM710 or LM106 was that they were prone to erratic operation caused by oscillations. This was a direct result of the high speed of the devices, which made it mandatory to provide good input-output isolation and low-inductance bypassing on the supplies. These oscillations could be particularly puzzling when they occurred internally, showing up at the external terminals only as erratic dc characteristics.

In general, the LM111 is less susceptible to spurious oscillations both because of its lower speed (200 ns response time vs 40 ns) and because of its better power supply rejection. Feedback between the output and the input is a lesser problem with a given source resistance. However, the LM111 can operate with source resistance that are orders of magnitude higher than the earlier devices, so stray coupling between the input and output should be minimized. With source resistances between 1 kΩ and 10 kΩ, the impedance (both capacitive and resistive) on both inputs should be made equal, as this tends to reject the signal fed back. Even so, it is difficult to completely eliminate oscillations in the linear region with source resistances above 10 kΩ, because the 1 MHz open loop gain of the comparator is about 80 dB. However, this does not affect the dc characteristics and is not a problem unless the input signal dwells within 200 μV of the transition level. But if the oscillation does cause difficulties, it can be eliminated with a small amount of positive feedback around the comparator to give a 1 mV hysteresis.

Stray coupling between the output and the balance terminals can also cause oscillations, so an attempt should be made to keep these leads apart. It is usually advisable to tie the balance pins together to minimize the effect of this feedback. If balancing is used, the same result can be accomplished by connecting a 0.1 μF capacitor between these pins.

Normally, individual supply bypasses on every device are unnecessary, although long leads between the comparator and the bypass capacitors are definitely not recommended. If large current spikes are injected into the supplies in switching the output, bypass capacitors should be included at these points.

When driving the inputs from a low impedance source, a limiting resistor should be placed in series with the input lead to limit the peak current to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Low impedance sources do not cause a problem unless their output voltage exceeds the negative supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. A charged capacitor can hold the inputs outside the supply voltage if the supplies are abruptly shut off.

Precautions should be taken to insure that the power supplies for this or any other IC never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC can conduct excessive current, fuzing internal aluminum interconnects. This usually takes more than 0.5A. If there is a possibility of reversal, clamp diodes with an adequate peak current rating should be installed across the supply bus.

No attempt should be made to operate the circuit with the ground terminal at a voltage exceeding either supply voltage. Further, the 50V output-voltage rating applies to the potential between the output and the V^- terminal. Therefore, if the comparator is operated from a negative supply, the maximum output voltage must be reduced by an amount equal to the voltage on the V^- terminal.

The output circuitry is protected for shorts across the load. It will not, for example, withstand a short to a voltage more negative than the ground terminal. Additionally, with a sustained short, power dissipation can become excessive if the voltage across the output transistor exceeds about 10V.

The input terminals can exceed the positive supply voltage without causing damage. However, the 30V maximum rating between the inputs and the V^- terminal must be observed. As mentioned earlier, the inputs should not be driven more negative than the V^- terminal.

conclusions

A versatile voltage comparator that can perform many of the precision functions required in digital systems has been produced. Unlike older comparators, the IC can operate from the same supply voltage as the digital circuits. The comparator is particularly useful in circuits requiring considerable sensitivity and accuracy, such as threshold detectors for low level sensors, data transmission circuits or stable oscillators and multivibrators.

The comparator can also be used in many analog systems. It operates from standard ±15V op amp supplies, and its dc accuracy equals some of the best op amps. It is also an order of magnitude faster than op amps used as comparators.

The new comparator is considerably more flexible than older devices. Not only will it drive RTL, DTL and TTL logic; but also it can interface with MOS logic or deliver ±15V to FET analog switches. The output can switch 50V, 50 mA loads, making it useful as a driver for relays, lamps or light-emitting diodes. Further, a unique output stage enables it to drive loads referred to either supply or to ground and provide ground isolation between the comparator inputs and the load.

The LM111 is a plug-in replacement for comparators like the LM710 and LM106 in applications where speed is not of prime concern. Compared to its predecessors in other respects, it has many improved electrical specifications, more design flexibility and fewer application problems.

IC Provides On-Card Regulation for Logic Circuits

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Application Note 42

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introduction

Because of the relatively high current requirements of digital systems, there are a number of problems associated with using one centrally-located regulator. Heavy power busses must be used to distribute the regulated voltage. With low voltages and currents of many amperes, voltage drops in connectors and conductors can cause an appreciable percentage change in the voltage delivered to the load. This is aggravated further with TTL logic, as it draws transient currents many times the steady-state current when it switches.

These problems have created a considerable interest in on-card regulation, that is, to provide local regulation for the subsystems of the computer. Rough preregulation can be used, and the power distributed without excessive concern for line drops. The local regulators then smooth out the voltage variations due to line drops and absorb transients.

A monolithic regulator is now available to perform this function. It is quite simple to use in that it requires no external components. The integrated circuit has three active leads—input, output and ground—and can be supplied in standard transistor power packages. Output currents in excess of 1A can be obtained. Further, no adjustments are required to set up the output voltage, and overload protection is provided that makes it virtually impossible to destroy the regulator. The simplicity of the regulator, coupled with low-cost fabrication and improved reliability of monolithic circuits, now makes on-card regulation quite attractive.

design concepts

A useful on-card regulator should include everything within one package—including the power-control element, or pass transistor. The author has previously advanced arguments against including the pass transistor in an integrated circuit regulator.[1] First, there are no standard multi-lead power packages. Second, integrated circuits necessarily have a lower maximum operating temperature because they contain low-level circuitry. This means that an IC regulator needs a more massive heat sink. Third, the gross variations in chip temperature due to dissipation in the pass transistors worsen load and line regulation. However, for a logic-card regulator, these arguments can be answered effectively.

For one, if the series pass transistor is put on the chip, the integrated circuit need only have three terminals. Hence, an ordinary transistor power package can be used. The practicality of this approach depends on eliminating the adjustments usually required to set up the output voltage and limiting current for the particular application, as external adjustments require extra pins. A new solid-state reference, to be described later, has sufficiently-tight manufacturing tolerances that output voltages do not always have to be individually trimmed. Further, thermal overload protection can protect an IC regulator for virtually any set of operating conditions, making current—limit adjustments unnecessary.

Thermal protection limits the maximum junction temperature and protects the regulator regardless of input voltage, type of overload or degree of heat sinking. With an external pass transistor, there is no convenient way to sense junction temperature so it is much more difficult to provide thermal limiting. Thermal protection is, in itself, a very good reason for putting the pass transistor on the chip.

When a regulator is protected by current limiting alone, it is necessary to limit the output current to a value substantially lower than is dictated by dissipation under normal operating conditions to prevent excessive heating when a fault occurs. Thermal limiting provides virtually absolute protection for any overload condition. Hence, the maximum output current under normal operating conditions can be increased. This tends to make up for the fact that an IC has a lower maximum junction temperature than discrete transistors.

Additionally, the 5V regulator works with relatively low voltage across the integrated circuit. Because of the low voltage, the internal circuitry can be operated at comparatively high currents without causing excessive dissipation. Both the low voltage and the larger internal currents permit higher junction temperatures. This can also reduce the heat sinking required—especially for commercial-temperature-range parts.

Lastly, the variations in chip temperature caused by dissipation in the pass transistor do not cause serious problems for a logic-card regulator. The tolerance in output voltage is

loose enough that it is relatively easy to design an internal reference that is much more stable than required, even for temperature variations as large as 150°C.

circuit description

The internal voltage reference for this logic-card regulator is probably the most significant departure from standard design techniques. Temperature-compensated zener diodes are normally used for the reference. However, these have breakdown voltages between 7V and 9V which puts a lower limit on the input voltage to the regulator. For low voltage operation, a different kind of reference is needed.

The reference in the LM109 does not use a zener diode. Instead, it is developed from the highly-predictable emitter-base voltage of the transistors. In its simplest form, the reference developed is equal to the energy-band-gap voltage of the semiconductor material. For silicon, this is 1.205V, so the reference need not impose minimum input voltage limitations on the regulator. An added advantage of this reference is that the output voltage is well determined in a production environment so that individual adjustment of the regulators is frequently unnecessary.

A simplified version of this reference is shown in *Figure 1*. In this circuit, Q_1 is operated at a relatively high current

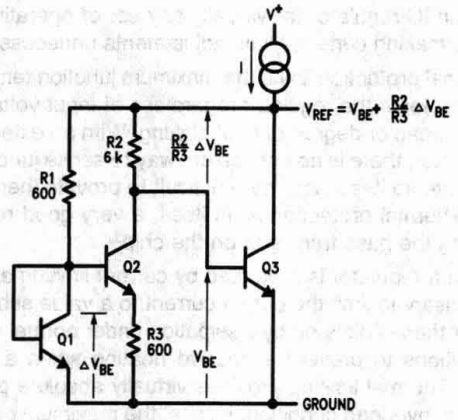

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Figure 1. The low voltage reference in one of its simpler forms.

density. The current density of Q_2 is about ten times lower, and the emitter-base voltage differential (ΔV_{BE}) between the two devices appears across R_3. If the transistors have high current gains, the voltage across R_2 will also be proportional to ΔV_{BE}. Q_3 is a gain stage that will regulate the output at a voltage equal to its emitter base voltage plus the drop across R_2. The emitter base voltage of Q_3 has a negative temperature coefficient while the ΔV_{BE} component across R_2 has a positive temperature coefficient. It will be shown that the output voltage will be temperature compensated when the sum of the two voltages is equal to the energy-band-gap voltage.

Conditions for temperature compensation can be derived starting with the equation for the emitter-base voltage of a transistor which is[2]

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{nkT}{q} \log_e \frac{T_0}{T} + \frac{kT}{q} \log_e \frac{I_C}{I_{C0}}, \quad (1)$$

where V_{gO} is the extrapolated energy-band-gap voltage for the semiconductor material at absolute zero, q is the charge of an electron, n is a constant which depends on how the transistor is made (approximately 1.5 for double-diffused, NPN transistors), k is Boltzmann's constant, T is absolute temperature, I_C is collector current and V_{BE0} is the emitter-base voltage at T_0 and I_{C0}.

The emitter-base voltage differential between two transistors operated at different current densities is given by[3]

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{J_1}{J_2}, \quad (2)$$

where J is current density.

Referring to Equation (1), the last two terms are quite small and are made even smaller by making I_C vary as absolute temperature. At any rate, they can be ignored for now because they are of the same order as errors caused by non-theoretical behavior of the transistors that must be determined empirically.

If the reference is composed of V_{BE} plus a voltage proportional to ΔV_{BE}, the output voltage is obtained by adding (1) in its simplified form to (2):

$$V_{ref} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{kT}{q} \log_e \frac{J_1}{J_2}. \quad (3)$$

Differentiating with respect to temperature yields

$$\frac{\partial V_{ref}}{\partial T} = -\frac{V_{g0}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{k}{q} \log_e \frac{J_1}{J_2}. \quad (4)$$

For zero temperature drift, this quantity should equal zero, giving

$$V_{g0} = V_{BE0} + \frac{kT_0}{q} \log_e \frac{J_1}{J_2}. \quad (5)$$

The first term on the right is the initial emitter-base voltage while the second is the component proportional to emitter-base voltage differential. Hence, if the sum of the two are equal to the energy-band-gap voltage of the semiconductor, the reference will be temperature-compensated.

A simplified schematic for a 5V regulator is given in *Figure 2*. The circuitry produces an output voltage that is approximately four times the basic reference voltage. The emitter-base voltage of Q_3, Q_4, Q_5 and Q_8 provide the negative-temperature-coefficient component of the output voltage. The voltage dropped across R_3 provides the positive-temperature-coefficient component. Q_6 is operated at a considerably higher current density than Q_7, producing a voltage drop across R_4 that is proportional to the emitter-base voltage differential of the two transistors. Assuming large current gain in the transistors, the voltage drop across R_3 will be proportional to this differential, so a temperature-compensated-output voltage can be obtained.

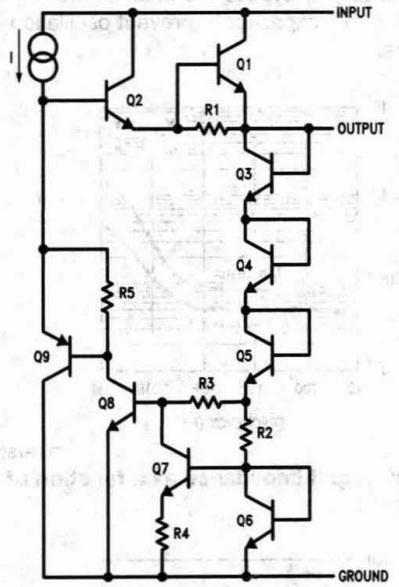

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Figure 2. Schematic showing essential details of the 5V regulator.

In this circuit, Q_8 is the gain stage providing regulation. Its effective gain is increased by using a vertical PNP, Q_9, as a buffer driving the active collector load represented by the current source. Q_9 drives a modified Darlington output stage (Q_1 and Q_2) which acts as the series pass element. With this circuit, the minimum input voltage is not limited by the voltage needed to supply the reference. Instead, it is determined by the output voltage and the saturation voltage of the Darlington output stage.

Figure 3 shows a complete schematic of the LM109, 5V regulator. The ΔV_{BE} component of the output voltage is developed across R_8 by the collector current of Q_7. The emitter-base voltage differential is produced by operating Q_4 and Q_5 at high current densities while operating Q_6 and Q_7 at much lower current levels. The extra transistors improve tolerances by making the emitter-base voltage differential larger. R_3 serves to compensate the transconductance[4] of Q_5, so that the ΔV_{BE} component is not affected by changes in the regular output voltage or the absolute value of components.

The voltage gain for the regulating loop is provided by Q_{10}, with Q_9 buffering its input and Q_{11} its output. The emitter base voltage of Q_9 and Q_{10} is added to that of Q_{12} and Q_{13} and the drop across R_8 to give a temperature-compensated, 5V output. An emitter-base-junction capacitor, C_1, frequency compensates the circuit so that it is stable even without a bypass capacitor on the output.

The active collector load for the error amplifier is Q_{17}. It is a multiple-collector lateral PNP[4]. The output current is essentially equal to the collector current of Q_2, with current being supplied to the zener diode controlling the thermal shutdown, D_2, by an auxiliary collector. Q_1 is a collector FET[4] that, along with R_1, insures starting of the regulator under worst-case conditions.

The output current of the regulator is limited when the voltage across R_{14} becomes large enough to turn on Q_{14}. This insures that the output current cannot get high enough to cause the pass transistor to go into secondary breakdown or damage the aluminum conductors on the chip. Further, when the voltage across the pass transistor exceeds 7V, current through R_{15} and D_3 reduces the limiting current,

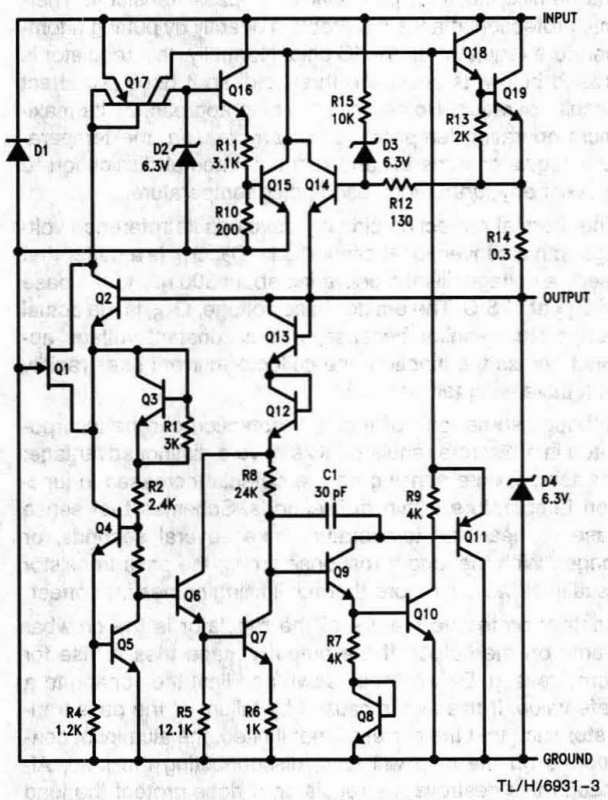

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Figure 3. Detailed schematic of the regulator.

again to minimize the chance of secondary breakdown. The performance of this protection circuitry is illustrated in *Figure 4.*

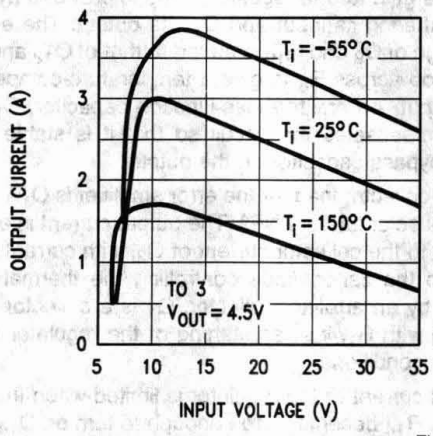

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Figure 4. Current-limiting characteristics.

Even though the current is limited, excessive dissipation can cause the chip to overheat. In fact, the dominant failure mechanism of solid state regulators is excessive heating of the semiconductors, particularly the pass transistor. Thermal protection attacks the problem directly by putting a temperature regulator on the IC chip. Normally, this regulator is biased below its activation threshold; so it does not affect circuit operation. However, if the chip approaches its maximum operating temperature, for any reason, the temperature regulator turns on and reduces internal dissipation to prevent any further increase in chip temperature.

The thermal protection circuitry develops its reference voltage with a conventional zener diode, D_2. Q_{16} is a buffer that feeds a voltage divider, delivering about 300 mV to the base of Q_{15} at 175°C. The emitter-base voltage, Q_{15}, is the actual temperature sensor because, with a constant voltage applied across the junction, the collector current rises rapidly with increasing temperature.

Although some form of thermal protection can be incorporated in a discrete regulator, IC's have a distinct advantage: the temperature sensing device detects increases in junction temperature within milliseconds. Schemes that sense case or heat-sink temperature take several seconds, or longer. With the longer response times, the pass transistor usually blows out before thermal limiting comes into effect.

Another protective feature of the regulator is the crowbar clamp on the output. If the output voltage tries to rise for some reason, D_4 will break down and limit the voltage to a safe value. If this rise is caused by failure of the pass transistor such that the current is not limited, the aluminum conductors on the chip will fuse, disconnecting the load. Although this destroys the regulator, it does protect the load from damage. The regulator is also designed so that it is not damaged in the event the unregulated input is shorted to ground when there is a large capacitor on the output. Further, if the input voltage tries to reverse, D_1 will clamp this for currents up to 1A.

The internal frequency compensation of the regulator permits it to operate with or without a bypass capacitor on the output. However, an output capacitor does improve the transient response and reduce the high frequency output impedance. A plot of the output impedance in *Figure 5* shows that it remains low out to 10 kHz even without a capacitor. The ripple rejection also remains high out to 10 kHz, as shown in *Figure 6.* The irregularities in this curve around 100 Hz are caused by thermal feedback from the pass transistor to the reference circuitry. Although an output capacitor is not required, it is necessary to bypass the input of the regulator with at least a 0.22 μF capacitor to prevent oscillations under all conditions.

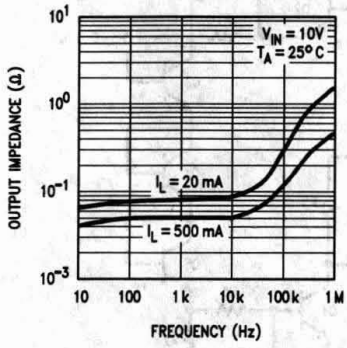

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Figure 5. Plot of output impedance as a function of frequency.

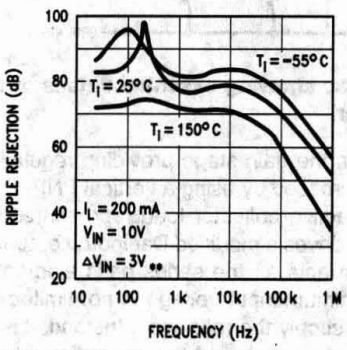

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Figure 6. Ripple rejection of the regulator.

Figure 7 is a photomicrograph of the regulator chip. It can be seen that the pass transistors, which must handle more than 1A, occupy most of the chip area. The output transistor is actually broken into segments. Uniform current distribution is insured by also breaking the current limit resistor into

segments and using them to equalize the currents. The overall electrical performance of this IC is summarized in Table I.

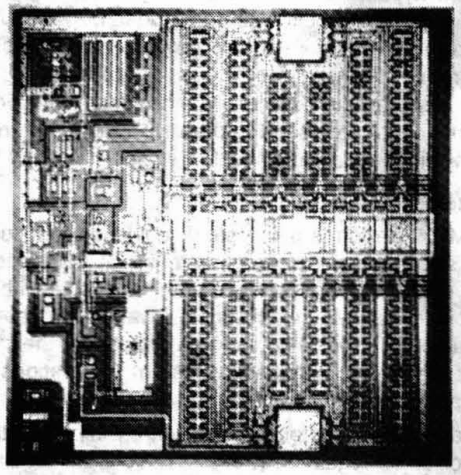

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Figure 7. Photomicrograph of the regulator shows that high current pass transistor (right) takes more area than control circuitry (left).

TABLE I. Typical Characteristics of the Logic-Card Regulator: T_A = 25°C

Parameter	Conditions	Typ
Output Voltage		5.0V
Output Current		1.5A
Output Resistance		0.03Ω
Line Regulation	7.0V ≤ V_{IN} ≤ 35V	0.005%/V
Temperature Drift	−55°C ≤ T_A ≤ 125°C	0.02%/°C
Minimum Input Voltage	I_{OUT} = 1A	6.5V
Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz	40 μV
Thermal Resistance Junction to Case	LM109H (TO-5) LM109K (TO-3)	15°C/W 3°C/W

applications

Because it was designed for virtually foolproof operation and because it has a singular purpose, the LM109 does not require a lot of application information, as do most other linear circuits. Only one precaution must be observed: it is necessary to bypass the unregulated supply with a 0.22 μF capacitor, as shown in *Figure 8*, to prevent oscillations that

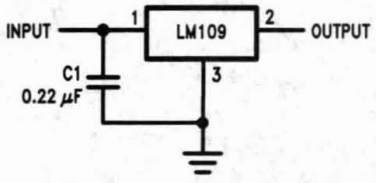

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Figure 8. Fixed 5V regulator.

can cause erratic operation. This, of course, is only necessary if the regulator is located on appreciable distance from the filter capacitors on the output of the dc supply.

Although the LM109 is designed as a fixed 5V regulator, it is also possible to use it as an adjustable regulator for higher output voltages. One circuit for doing this is shown in *Figure 9*.

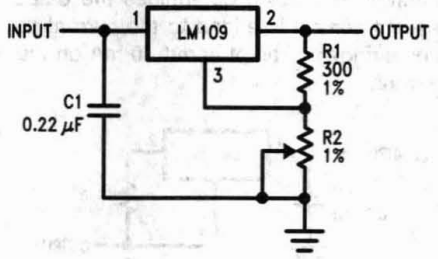

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Figure 9. Using the LM109 as an adjustable-output regulator.

The regulated output voltage is impressed across R_1, developing a reference current. The quiescent current of the regulator, coming out of the ground terminal, is added to this. These combined currents produce a voltage drop across R_2 which raises the output voltage. Hence, any voltage above 5V can be obtained as long as the voltage across the integrated circuit is kept within ratings.

The LM109 was designed so that its quiescent current is not greatly affected by variations in input voltage, load or temperature. However, it is not completely insensitive, as shown in *Figures 10* and *11*, so the changes do affect regulation somewhat. This tendency is minimized by making the reference current though R_1 larger than the quiescent current. Even so, it is difficult to get the regulation tighter than a couple percent.

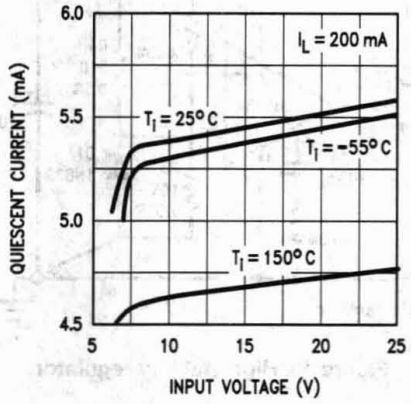

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Figure 10. Variation of quiescent current with input voltage at various temperatures.

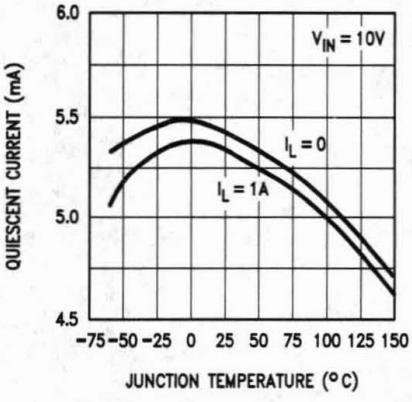

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Figure 11. Variation of quiescent current with temperature for various load currents.

The LM109 can also be used as a current regulator as is shown in *Figure 12*. The regulated output voltage is impressed across R_1, which determines the output current. The quiescent current is added to the current through R_1, and this puts a lower limit of about 10 mA on the available output current.

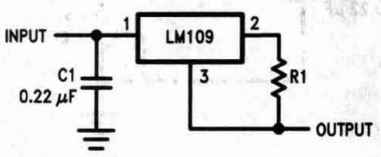

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Figure 12. Current regulator.

The increased failure resistance brought about by thermal overload protection make the LM109 attractive as the pass transistor in other regulator circuits. A precision regulator that employs the IC thusly is shown in *Figure 13*. An operational amplifier compares the output voltage with the output voltage of a reference zener. The op amp controls the LM109 by driving the ground terminal through an FET.

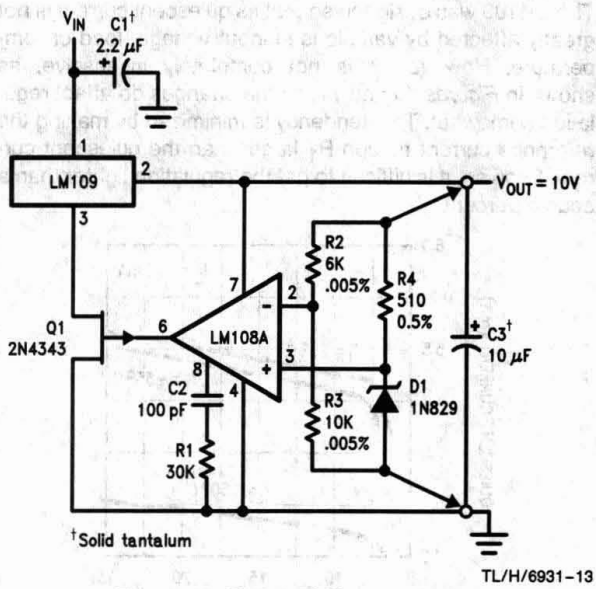

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Figure 13. High stability regulator.

The load and line regulation of this circuit is better than 0.001%. Noise, drift and long term stability are determined by the reference zener, D_1. Noise can be reduced by inserting 100 kΩ, 1% resistors in series with both inputs of the op amp and bypassing the non-inverting input to ground. A 100 pF capacitor should also be included between the output and the inverting input to prevent frequency instability. Temperature drift can be reduced by adjusting R_4, which determines the zener current, for minimum drift. For best performance, remote sensing directly to the load terminals, as shown in the diagram, should be used.

conclusions

The LM109 performs a complete regulation function on a single silicon chip, requiring no external components. It makes use of some unique advantages of monolithic construction to achieve performance advantages that cannot be obtained in discrete-component circuits. Further, the low cost of the device suggests its use in applications where single-point regulation could not be justified previously.

Thermal overload protection significantly improves the reliability of an IC regulator. It even protects the regulator for unforseen fault conditions that may occur in field operation. Although this can be accomplished easily in a monolithic regulator, it is usually not completely effective in a discrete or hybrid device.

The internal reference developed for the LM109 also advances the state of the art for regulators. Not only does it provide a low voltage, temperature-compensated reference for the first time, but also it can be expected to have better long term stability than conventional zeners. Noise is inherently much lower, and it can be manufactured to tighter tolerances.

reference

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The Phase Locked Loop IC as a Communication System Building Block

National Semiconductor
Application Note 46
Thomas B. Mills

INTRODUCTION

The phase locked loop has been found to be a useful element in many types of communication systems. It is used in two fundamentally different ways: (1) as a demodulator, where it is used to follow phase or frequency modulation and (2) to track a carrier or synchronizing signal which may vary in frequency with time.

When operating as a demodulator, the phase locked loop may be thought of as a matched filter operating as a coherent detector. When used to track a carrier, it may be thought of as a narrow-band filter for removing noise from a signal.

Recently, a phase locked loop has been built on a monolithic integrated circuit, incorporating the basic elements necessary for operation: a double balanced phase detector and a highly linear voltage controlled oscillator, the frequency of which can be varied with either a resistor or capacitor.

BASIC PHASE LOCK LOOP OPERATION

Figure 1 shows the basic blocks of a phase locked loop. The input signal e_i is a sinusoid of arbitrary frequency, while the VCO output signal, e_o, is a sinsuoid of the same frequency as the input but of arbitrary phase. If

$$e_i = \sqrt{2}\, E_i \sin [\omega_o t + \theta_1(t)] \quad (1)$$

$$e_o = \sqrt{2}\, E_o \cos [\omega_o t + \theta_2(t)] \quad (2)$$

the output of the multiplier (phase detector) is

$$\begin{aligned} e_d &= e_i \bullet e_o \\ &= 2E_iE_o \sin [\omega_o t + \theta_1(t)] \bullet \cos [\omega_o t + \theta_2(t)] \\ &= E_iE_o \sin [\theta_1(t) - \theta_2(t)] + E_iE_o \sin [2\omega_o t + \theta_1(t) + \theta_2(t)] \end{aligned} \quad (3)$$

the low pass filter of the loop removes the ac components of the multiplier output; the dc term is seen to be a function of the phase angle between the VCO and the input signal.

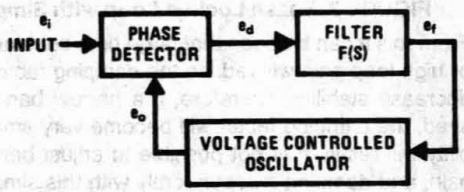

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FIGURE 1. Basic Phase Locked Loop

The output of the VCO is related to its input control voltage by

$$\dot{\theta}_2(t) = K_o e_f \quad (4)$$

for $e_f = 0$, Let $\dot{\theta}_2 = \omega\theta$, then

$$\theta_2(t) = \int e_f(t)\, dt \quad (5)$$

It can be seen that the action of the VCO is that of an integrator in the feedback loop when the phase locked loop is considered in servo theory.

A better understanding of the operation of the loop may be obtained by considering that initially, the loop is not in lock, but that the frequency of the input signal e_i and VCO e_o are very close in frequency. Under these conditions e_d will be a beat note, the frequency of which is equal to the frequency difference of e_o and e_i. This signal is also applied to the VCO input, since it is low enough to pass through the filter. The instantaneous frequency of the VCO is therefore changing and at some point in time, if the VCO frequency equals the input frequency, lock will result. At this instant, e_f will assume a level sufficient to hold the VCO frequency in lock with the input frequency. If the tuning of the VCO is changed (such as by varying the value of the tuning capacitor) the frequency output of the VCO will attempt to change; however, this will result in an instantaneous change in phase angle between e_i and e_o, resulting in a change in the dc level of e_d which will act to maintain frequency lock: no average frequency change will result.

Similarly, if e_i changes frequency, an instantaneous change will result in a phase change between e_i and e_o and hence a dc level change in e_d. This level shift will change the frequency of the VCO to maintain lock.

The amount of phase error resulting from a given frequency shift can be found by knowing the "dc" loop gain of the system. Considering the phase detector to have a transfer function:

$$E_d = K_D (\theta_1 - \theta_2)$$

and the voltage controlled oscillator to have a transfer function:

$$\dot{\theta}_2 = K_o e_f \quad (6)$$

or taking the Laplace transform

$$\theta_2 (s) = \frac{K_o e_f}{s} \quad (7)$$

the phase of the VCO output will be proportional to the integral of the control voltage.

Combining these equations:

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_o K_d F(s)}{s + K_o K_D F(s)} \quad (8)$$

$$\frac{\theta_1(s) - \theta_2(s)}{\theta_1(s)} = \frac{s}{s + K_o K_D F(s)} \quad (9)$$

Application of the final value theorem of Laplace transforms yields

$$\lim_{t \to \infty} \theta_1(s) - \theta_2(s) = \lim_{s \to 0} \frac{s^2\,\theta_1(s)}{s + K_o K_D\,F(s)} \quad (10)$$

With a step change in phase of the input $\Delta\theta_1$, the Laplace transform of the input is

$$\theta_1(s) = \frac{\Delta\theta_1}{s} \text{ which gives } \theta_e(s) = \theta_1(s) - \theta_2(s)$$

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} \frac{s\Delta\theta_1}{s + K_o K_D\,F(s)} = 0 \quad (11)$$

the loop will eventually track out any change of input phase, and there will be no phase error in the steady state solution.

If the input is a step in frequency, of magnitude $\Delta\omega$, the change in input phase will be a ramp:

$$\theta_1(s) = \Delta\omega/s^2$$

substitution of this value θ_i into (10) results in

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} \frac{\Delta\omega}{s + K_o K_D\,F(s)} = \frac{\Delta\omega}{K_o K_D\,F(o)} \quad (12)$$

this result shows the resulting phase error is dependent on the magnitude of the frequency step and the "dc" loop gain K_oK_D, which is also called the velocity error coefficient K_v. It should be noted that the dimensions of K_oK_D are 1/sec. This can also be seen by considering K_D = volts/radian, while K_o = radians/sec/volt. The product is

$$\frac{\text{volts}}{\text{radian}} \times \frac{\text{radians/sec}}{\text{volt}} = \frac{1}{\text{sec}}$$

this can be thought of as the "dc" loop gain. (Note that additional dc gain between the phase detector and the voltage controlled oscillator will increase the loop gain and hence reduce the steady state phase error resulting from a change in frequency of the input).

THE LOOP FILTER

In working with phase locked loops, it is necessary to consider not only the "dc" performance described above, but the "ac" or transient performance which is governed by the components of the loop filter placed between the phase detector and the voltage controlled oscillator. In fact, it is this loop filter that makes the phase locked loop so powerful: only a resistor and capacitor are all that is needed to produce an arbitrarily narrow bandwidth at any selected center frequency.

The simplest filter is a single capacitor, *Figure 2*, and is used for wide bandwith applications, such as where wideband data modulation must be followed. The transfer function of the filter is simply:

$$\frac{e_f}{e_d} = \frac{1}{1 + sR_1\,C_1} \quad (13)$$

substitution into (8) results in

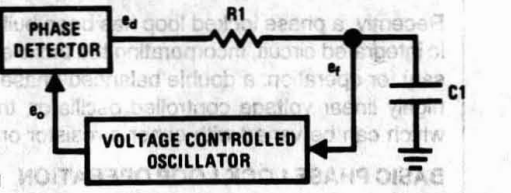
$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_oK_D/\tau_1}{s^2 + s/\tau_1 + K_oK_D/\tau_1} \quad (14)$$

$$\tau_1 = R_1\,C_1$$

In terms of servo theory, the damping factor and natural frequencies are

$$\omega_n = \left[\frac{K_oK_D}{R_1\,C_1}\right]^{1/2} \quad (15)$$

$$\zeta = \frac{1}{2}\left[\frac{1}{(R_1\,C_1\,K_oK_D)}\right]^{1/2} \quad (16)$$



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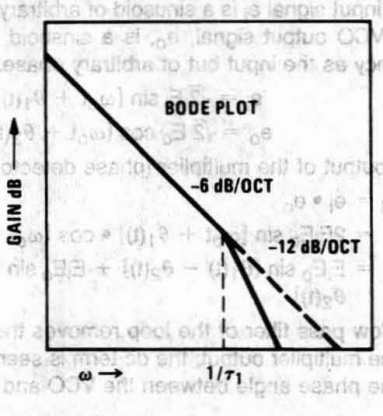

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FIGURE 2. Phase Locked Loop with Simple Filter

From this it can be seen that large time constants for $R_1\,C_1$ or high loop gain will reduce the damping factor and hence decrease stability. Therefore, if a narrow bandwidth is desired, the damping factor will become very small and instability will result. It is not possible to adjust bandwidth, loop gain, and damping independently with this simple filter.

With the addition of a damping resistor R_2 as shown in *Figure 3*, it is possible to choose bandwidth, damping factor and loop gain independently; the transfer function of this filter is

$$\frac{e_d}{e_f} = \frac{1 + s\tau_2}{1 + s\tau_1} \tag{17}$$

the loop transfer function becomes:

$$\frac{\theta_2(s)}{\theta_z(s)} = \frac{K_o K_D (s\tau_2 + 1)(\tau_1 + \tau_2)}{s^2 + s(1 + K_o K_d \tau_2)/\tau_1 + K_o K_D/\tau_1} \tag{18}$$

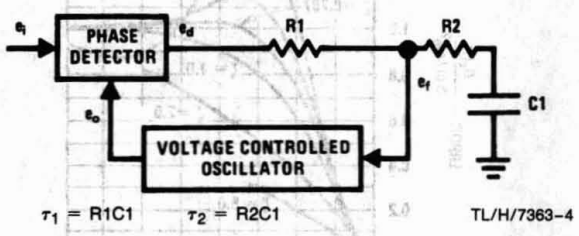
the loop natural frequency is

$$\omega_n = \left[\frac{K_o K_D}{\tau_1}\right]^{1/2} \tag{19}$$

while the damping factor becomes

$$\zeta = \frac{1}{2}\left[\frac{1}{\tau_1 K_o K_D}\right]^{1/2}\left[1 + \tau_2 K_o K_D\right] \tag{20}$$

$$\cong \frac{\omega_n \tau_2}{2} \tag{21}$$



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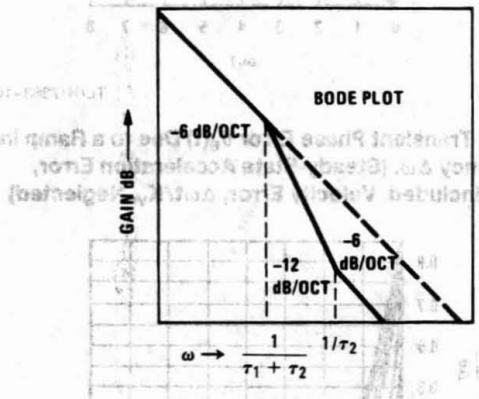

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FIGURE 3. Phase Locked Loop with Damping Resistor Added

In practice, for a fixed loop gain $K_o K_D$, the natural frequency of the loop may be chosen and will be dependent mainly on τ_1, since $\tau_2 \ll \tau_1$ in most cases. Then, according to (21), damping may be determined by τ_2 and for all practical purposes, will be an independent adjustment. These equations are plotted in *Figures 4* and *5* and may be used for design purposes.

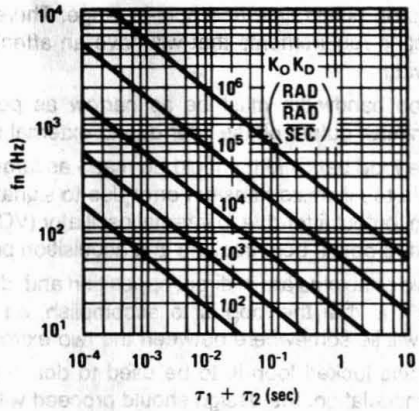

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FIGURE 4. Filter Time Constant vs Natural Frequency

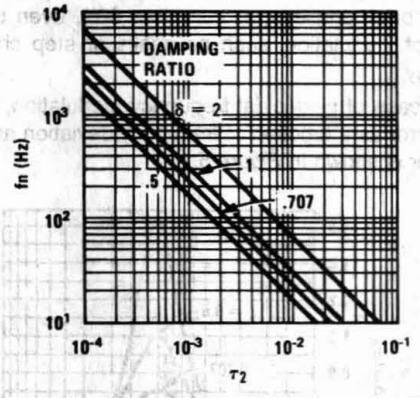

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FIGURE 5. Damping Time Constant vs Natural Frequency

DESIGN CONSIDERATIONS

Considering the above discussion, there are really two primary considerations in designing a phase locked loop. The use to which the loop is to be put will affect the design criterion of the loop components. The two primary factors to consider are:

1. Loop gain. As pointed out previously, this affects the phase error between the input signal and the voltage controlled oscillator for a given frequency shift of the input signal. It also determines the "hold in range" of the loop providing no components of the loop go into limiting or saturation. This is because the loop will remain in lock as long as the phase difference between the input and the VCO is less than $\pm 90°$. The higher the loop gain, the further the input can change in frequency before the 90° phase error is reached. The hold in range is
$$\Delta\omega_H = \pm K_o K_D \tag{22}$$
(providing saturation or limiting does not occur).
2. Natural Frequency. The bandwidth of the loop is determined by the filter components R_1, R_2 and C_1, and the loop gain. Since the loop gain is normally selected by the criterion in 1. above, the filter components are used to select the bandwidth. The selection of loop bandwidth may be governed by several things: noise bandwidth, modulation rates if the loop is to be used as an FM de-

modulator, pull-in time and hold-in range. There are two conflicting requirements that will have an affect on loop bandwidth:

(a) Loop bandwidth must be as narrow as possible to minimize output phase jitter due to external noise.

(b) The loop bandwidth should be made as large as possible to minimize transient error due to signal modulation, output jitter due to internal oscillator (VCO) noise, and to obtain best tracking and acquisition properties.

These two principles are in direct opposition and, depending on what it is that the loop is to accomplish, an optimum solution will lie somewhere between the two extremes.

If the phase locked loop is to be used to demodulate frequency modulation, the design should proceed with the criterion of b above. It is necessary to provide sufficient loop bandwidth to accommodate the expected modulation. It must be remembered that at all times, the loop must remain in lock, (peak phase error less than 90°), even under extremes of modulation, such as peaks or step changes in frequency.

For the case of sinusoidal frequency modulation, the peak phase error as a function of frequency deviation and damping factor is shown in *Figure 6*.

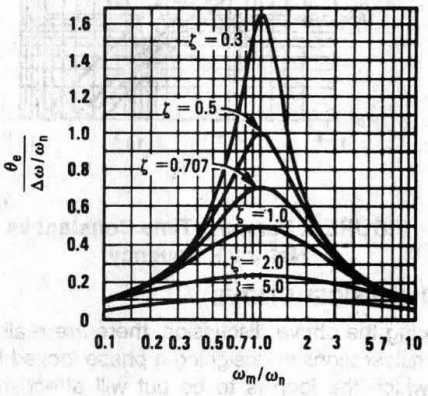

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FIGURE 6. Steady-State Peak Phase Error Due to Sinusoidal FM (High-Gain, Second-Order Loop)

It can be seen that the maximum phase error occurs when the modulating frequency ω_m equals the loop natural frequency ω_n; if the loop has been designed with a damping factor of 0.707, the peak phase error (in radians) will be 0.71 $\Delta\omega/\omega_n$ ($\Delta\omega$ = frequency deviation). From this plot, it is possible to choose ω_n for a given deviation and modulation frequency.

If the loop is to demodulate frequency shift keying (FSK), it must follow step changes in frequency. The filter components must then be chosen in accordance with the transient phase error shown in *Figure 7*. It must be remembered that the loop filter must be wide enough so the loop will not lose lock when a step change in frequency occurs: the greater the frequency step, the wider the loop filter must be to maintain lock.

There is some frequency-step limit below which the loop does not skip cycles, but remains in lock, called the "pull-out frequency" ω_{po}. Viterbi has analyzed this and his results are shown in *Figure 8*, which plots normalized pull out frequency for various damping factors for high gain second order loops. Peak phase errors for other types of input signals are shown in *Figures 8* and *9*.

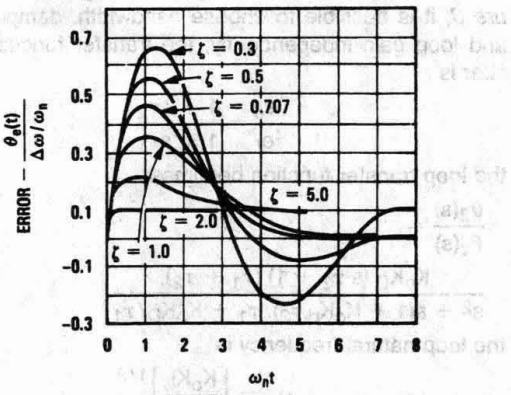

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FIGURE 7. Transient Phase Error $\theta_e(t)$ Due to a Step in Frequency $\Delta\omega$. (Steady-State Velocity Error, $\Delta\omega/K_v$, Neglected)

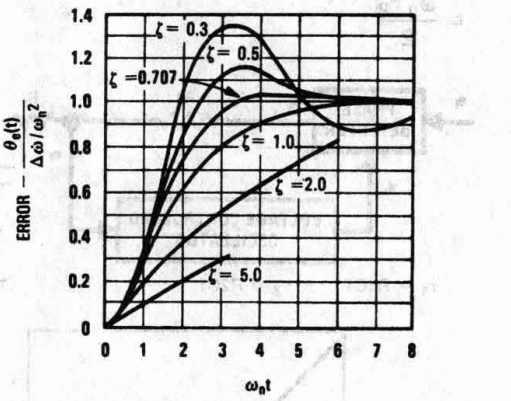

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FIGURE 8. Transient Phase Error $\theta_e(t)$ Due to a Ramp in Frequency $\Delta\omega$. (Steady-State Acceleration Error, $\Delta\omega/\omega_n^2$, Included. Velocity Error, $\Delta\omega t/K_v$, Neglected)

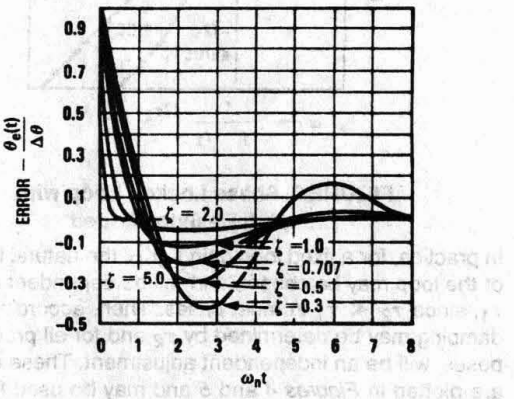

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FIGURE 9. Phase Error $\theta_e(t)$ Due to a Step in Phase $\Delta\theta$

In designing loops to track a carrier or synchronizing signal, it is desirable to make the loop bandwidth narrow so that phase error due to external noise will be small. However, it is necessary to make the loop bandwidth wide enough so that any frequency jitter on the input signal will be followed.

NOISE PERFORMANCE

Since one of the main uses of phase locked loops is to demodulate or track signals in noise, it is helpful to look at how noise affects the operation of the phase locked loop.

The phase locked loop, as mentioned earlier, may be thought of as a filter with a fixed, adjustable bandwidth. We have seen how to calculate the loop natural frequency ω_n (15), (19), and the damping factor ζ (16), (20). Without going through a derivation, the loop noise bandwidth B_L may be shown to be

$$B_L = \int_0^\infty |H(j\omega)|^2 \, df = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right] \text{Hz} \qquad (23)$$

for a high gain, second order loop. This equation is plotted in *Figure 10*. It should be noted that the dimensions of noise bandwidth are cycles per second while the dimensions of ω_n are radians per second.

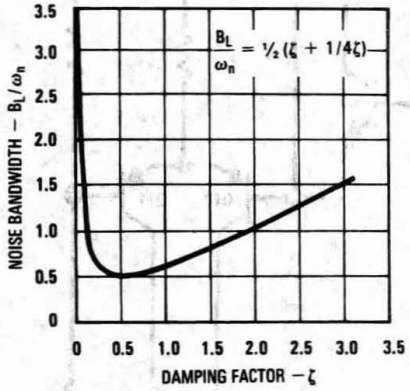

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FIGURE 10. Loop-Noise Bandwidth (For High-Gain, Second-Order Loop)

Noise threshold is a difficult thing to analyze in a phase locked loop, since we are talking about a statistical quantity. Noise will show up in the input signal as both amplitude and phase modulation. It can be shown that near optimum performance of a phase locked loop can be obtained if a limiter is used ahead of the phase detector, or if the phase detector is allowed to operate in limiting. With the use of a limiter, amplitude modulation of the input signal by noise is removed, and the noise appears as phase modulation. As the input signal to noise ratio decreases, the phase jitter of the input signal due to noise increases, and the probability of losing lock due to instantaneous phase excersions will increase. In practice it is nearly impossible to acquire lock if the signal to noise ratio in the loop $(SNR)_L = 0$ dB. In general, $(SNR)_L$ of +6 dB is needed for acquisition. If modulation or transient phase error is present, a higher signal to noise ratio is needed to acquire and hold lock.

A computer simulation performed by Sanneman and Rowbotham has shown the probability of skipping cycles for various loop signal to noise ratios for high gain, second order loops. Their data is shown in *Figure 11*.

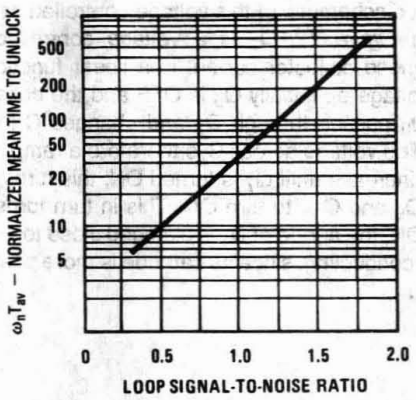

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FIGURE 11. Unlock Behavior of High-Gain, Second-Order Loop, $\zeta = 0.707$

When designing the loop filter components, enough bandwidth in the loop must be allowed for instantaneous phase change due to input noise. In the previous section, the filter was selected on the basis that the peak error due to modulation would be less than 90° (so the loop would not loose lock). However, if noise is present, the peak phase error will increase due to the noise. So if the loop is not to lose lock on these noise peaks the peak allowable error due to modulation must be reduced to something less, on the order of 40° to 50°.

LOCKING

Initially, a loop is unlocked and the VCO is running at some frequency. If a signal is applied to the input, locking may or may not occur depending on several things.

If the signal is within the bandwidth of the loop filter, locking will occur without a beat note being generated or any cycles being skipped. This frequency is given by

$$\Delta\omega_L = \frac{K_o K_D \tau_2}{\tau_1 + \tau_2} \approx 2\zeta\omega_n \qquad (24)$$

If the frequency of the input signal is further away from the VCO frequency, locking may still occur, with a beat note being generated. The greatest frequency that can be pulled in is called the "pull in frequency" and is found from the approximation

$$\Delta\omega_P \approx \sqrt{2}\left(2\zeta\omega_n K_o K_D - \omega_n^2\right)^{1/2} \qquad (25)$$

which works well for moderate and high gain loops $(\omega_n/K_oK_D < 0.4)$.

An approximate expression for pull in time (the time required to achieve lock from some frequency offset $\Delta\omega$) is given by:

$$T_P \approx \frac{(\Delta\omega)^2}{2\zeta\omega_n^3}$$

A MONOLITHIC PHASE LOCKED LOOP

A complete phase locked loop has been built on a monolithic integrated circuit. It features a very linear voltage controlled oscillator and a double balanced phase detector.

A simplified schematic of this voltage controlled oscillator is shown in *Figure 12*. Q_2 is a voltage controlled current source whose collector current is a linear function of the control voltage e_f. Initially Q_5 is OFF and the collector current of Q_2 passes through D_2 and changes C in a linear fashion. The voltage across C is therefore a ramp, and continues to increase until Q_7 is turned ON; this turns OFF Q_8, causing Q_9 and Q_{11} to turn ON. This in turn turns ON Q_5. With Q_5 ON, the anode of D_1 is clamped close to $-V_{CC}$ and D_2 stops conducting, since its cathode is more positive than its anode.

All of the current supplied by Q_2 is diverted through D_1 and Q_3, which sets up an equal current in Q_4. This current is supplied by the charged capacitor C (which now discharges linearly), causing the voltage across it to decrease. This continues until a lower trip point is reached and Q_7 turns OFF and the cycle repeats. Due to the matching of Q_3 and Q_4, the charge current of C is equal to the discharge current and therefore the duty cycle is very nearly 50%. *Figure 13* shows the wave forms at (1) and (2).

Figure 14 shows the double balanced phase detector and amplifier used in the microcircuit. Transistors Q_1 through Q_4 are switched with the output of the VCO, while the input

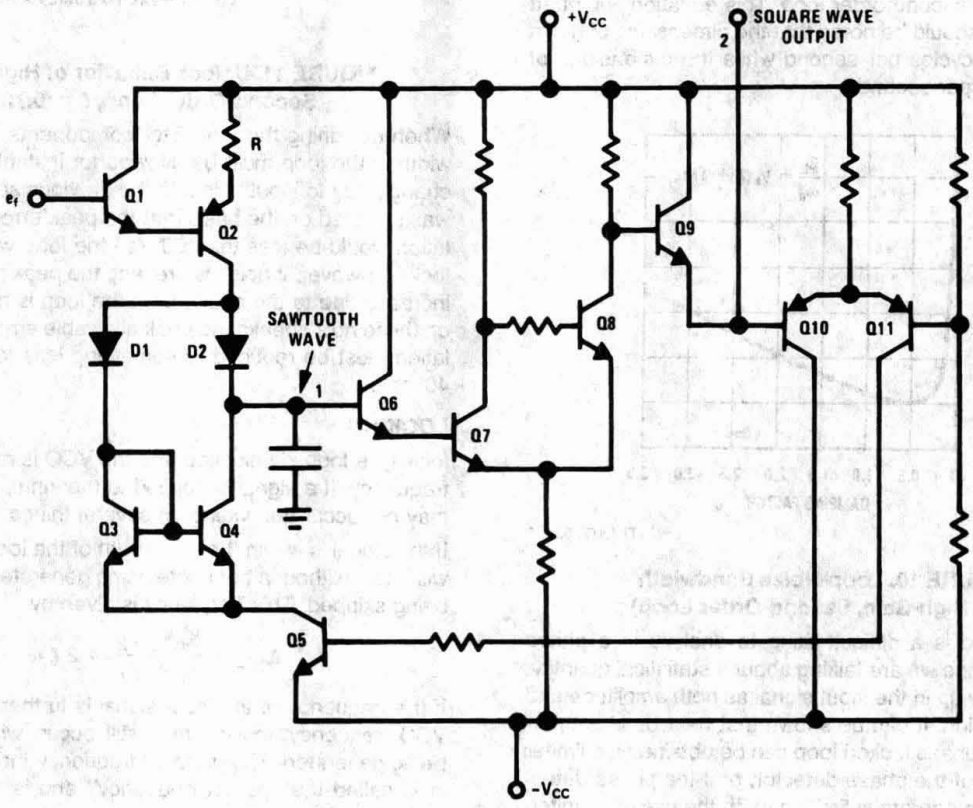

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FIGURE 12. Simplified Voltage Controlled Oscillator

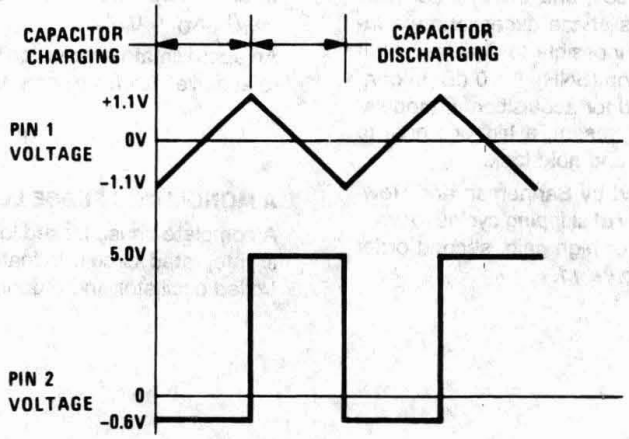

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FIGURE 13. VCO Waveforms

signal is applied to the bases of Q_5 and Q_6. The output current in resistors R_3 and R_4 is then proportional to the difference in phase between the VCO output and the input; the ac component of this current will be at twice the frequency of the VCO due to the full wave switching action transistors Q_1 through Q_4. The waveforms of *Figure 15* illustrate how the phase detector works. Diodes D_1 and D_2 serve to limit the peak to peak amplitude of the collector voltage. The output of the phase detector is further amplified by Q_{10} and Q_{11}, and is taken as a voltage at pin 7.

R_8 serves as the resistive portion of the loop filter, and additional resistance and capacitance may be added here to fix the loop bandwidth. For use as an FM demodulator, the voltage at pin 7 will be the demodulated output; since the dc level here is fairly high, a reference voltage has been provided so that an operational amplifier with differential input can be used for additional gain and level shifting.

The complete microcircuit, called the LM565, is shown in *Figure 16*.

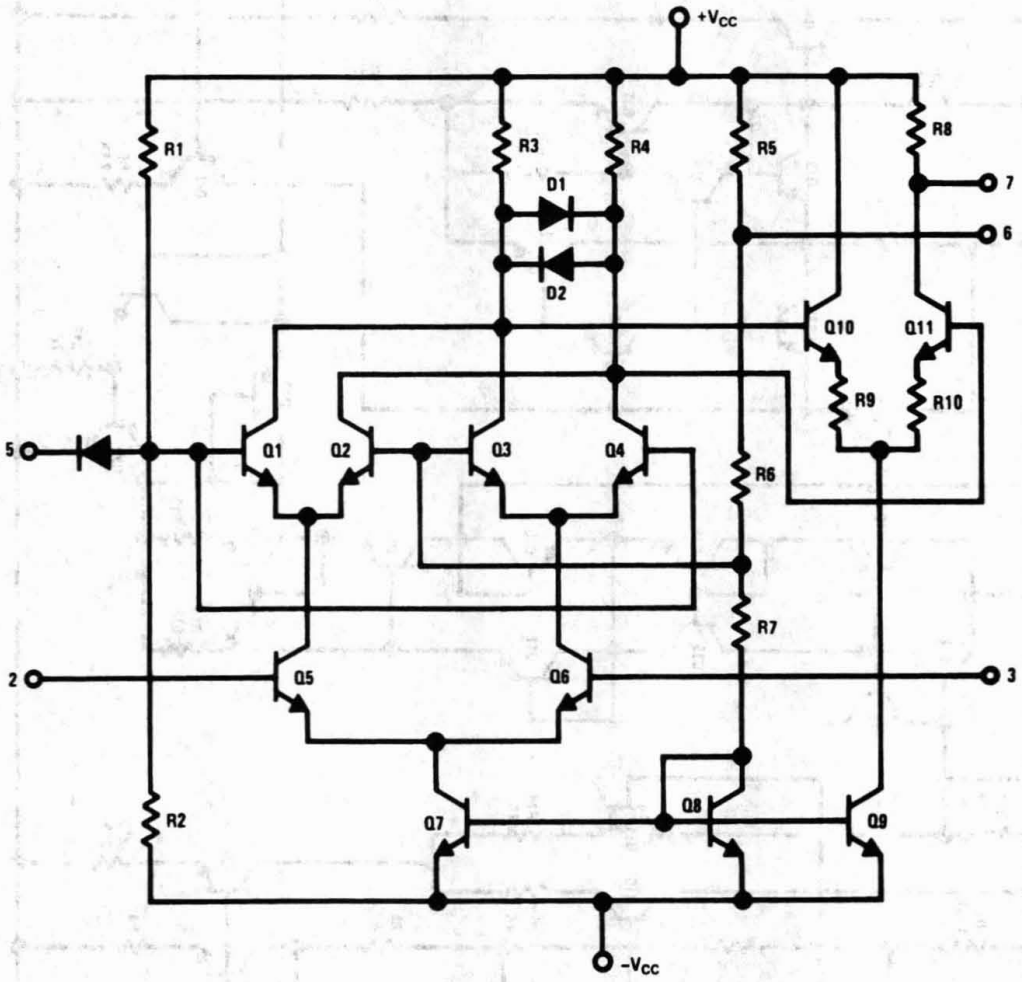

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FIGURE 14. Phase Detector and Amplifier

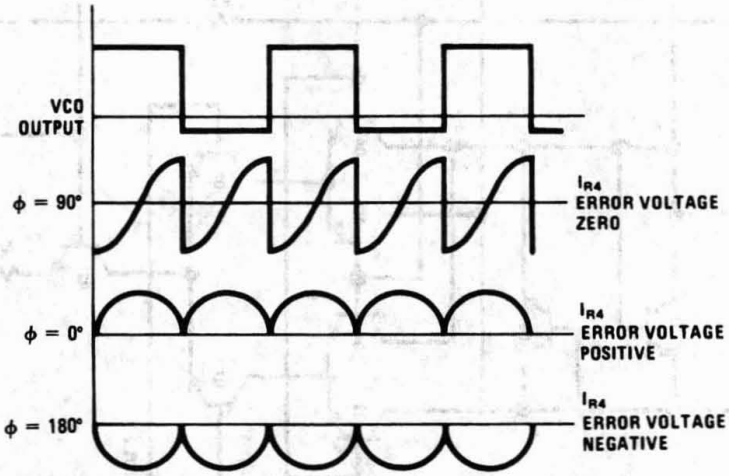

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FIGURE 15. Phase Detector Waveforms, Showing Limit Cases for Phase Shift between Input and VCO Signals

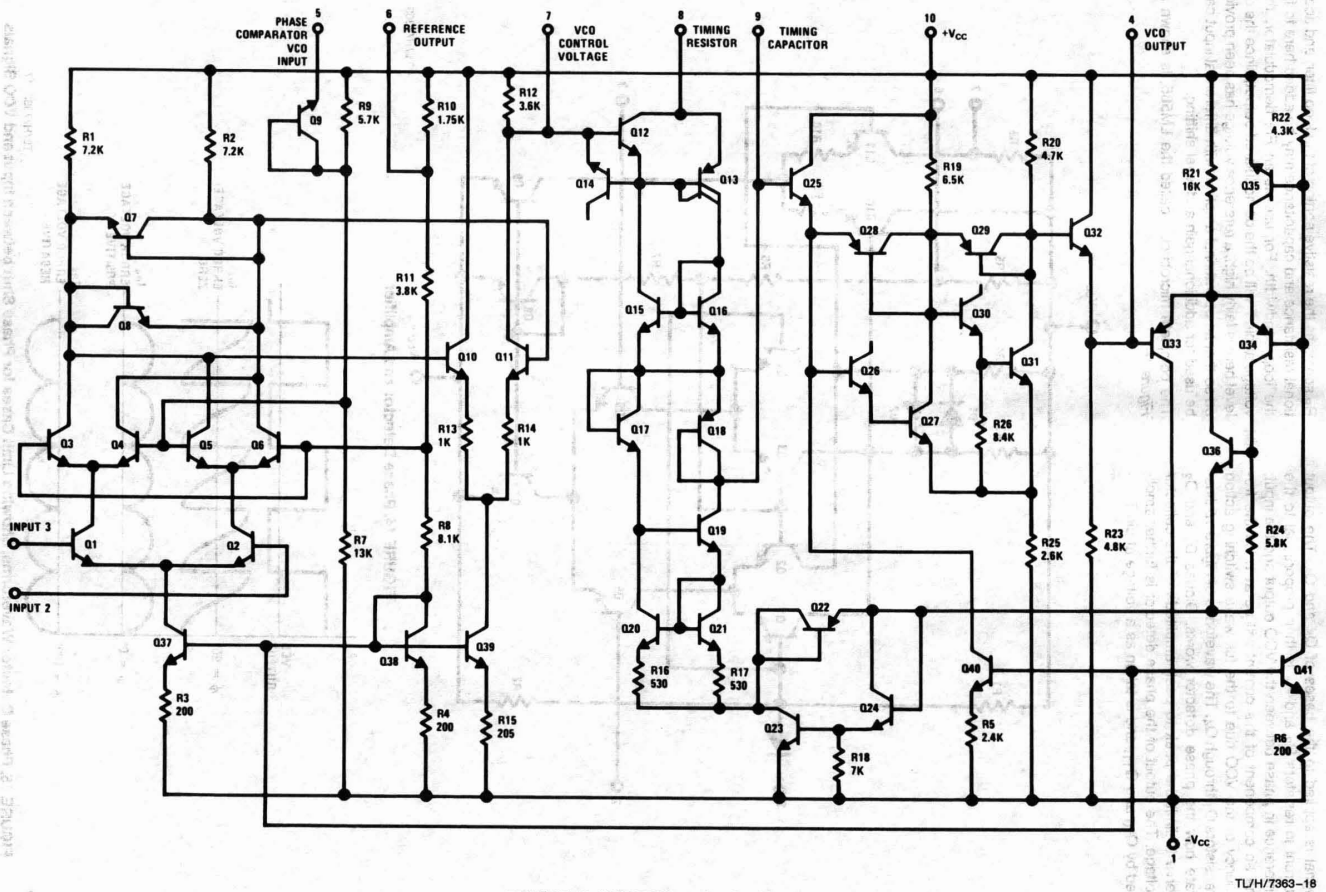

FIGURE 16. LM565 Phase Locked Loop

USING THE LM565

Some of the important operating characteristics of the LM565 are shown in the table below (V_{CC} = ±6V, T_A = 25°C).

Phase Detector	
Input Impedance	5 kΩ
Input Level for Limiting	10 mV
Output Resistance	3.6 kΩ
Output Common Mode Voltage	4.5V
Offset Voltage (Between pins 6 and 7)	100 mV
Sensitivity K_D	.68V/rad
Voltage Controlled Oscillator	
Stability	
Temperature	200 ppm/°C
Supply Voltage	200 ppm/%
Square Wave Output Pin 4	5.4 V_{pp}
Triangle Wave Output Pin 9	2.4 V_{pp}
Maximum Operating Frequency	500 kHz
Sensitivity K_o	4.1 f_o rad/sec/V (f_o: osc, freq. in Hz)
Closed Loop Performance	
Loop Gain K_oK_D	2.8 f_o/sec
Demod. Output, ±10% Deviation	300 mV
(A 0.001 μF capacitor is needed between pins 7 and 8 to stop parasitic oscillations).	

To best illustrate how the LM565 is used, several applications are covered in detail, and should provide insight into the selection of external components for use with the LM565.

IRIG CHANNEL DEMODULATOR

In the field of missile telemetry, it is necessary to send many channels of relatively narrow band data via a radio link. It has been found convenient to frequency modulate this information on a set of subcarriers with center frequencies in the range of 400 Hz to 200 kHz. Standardization of these frequencies was undertaken by the Inter-Range Instrumentation Group (IRIG) and has resulted in several sets of subcarrier channels, some based on deviations that are a fixed percentage of center frequency and other sets that have a constant deviation regardless of center frequency. IRIG channel 13 has been selected as an example to demonstrate the usefulness of the LM565 as an FM demodulator.

IRIG Channel	13
Center Frequency	14.5 kHz
Max Deviation	±7.5%
Frequency Response	220 Hz
Deviation Ratio	5

Since with a deviation of ±10%, the LM565 will produce approximately 300 mV peak to peak output, with a deviation of 7.5% we can expect an output of 225 mV. It is desirable to amplify and level shift this signal to ground so that plus and minus output votages can be obtained for frequency shifts above and below center frequency.

An LM107 can be used to provide the necessary additional gain and the level shift. In *Figure 17*, R_4 is used to set the output at zero volts with no input signal. The frequency of the VCO can be adjusted with R_3 to provide zero output voltage when an input signal is present.

The design of the filter network proceeds as follows:

It is necessary to choose ω_n such that the peak phase error in the loop is less than 90° for all conditions of modulation. Allowing for noise modulation at low levels of signal to noise, a desirable peak phase error might be 1 radian or 57 degrees, leaving a 33 degree margin for noise. Assuming sinusoidal modulation, *Figure 6* can be used to estimate the peak normalized phase error. It will be necessary to make several sample calculations, since the normalized phase error is a function of ω_n.

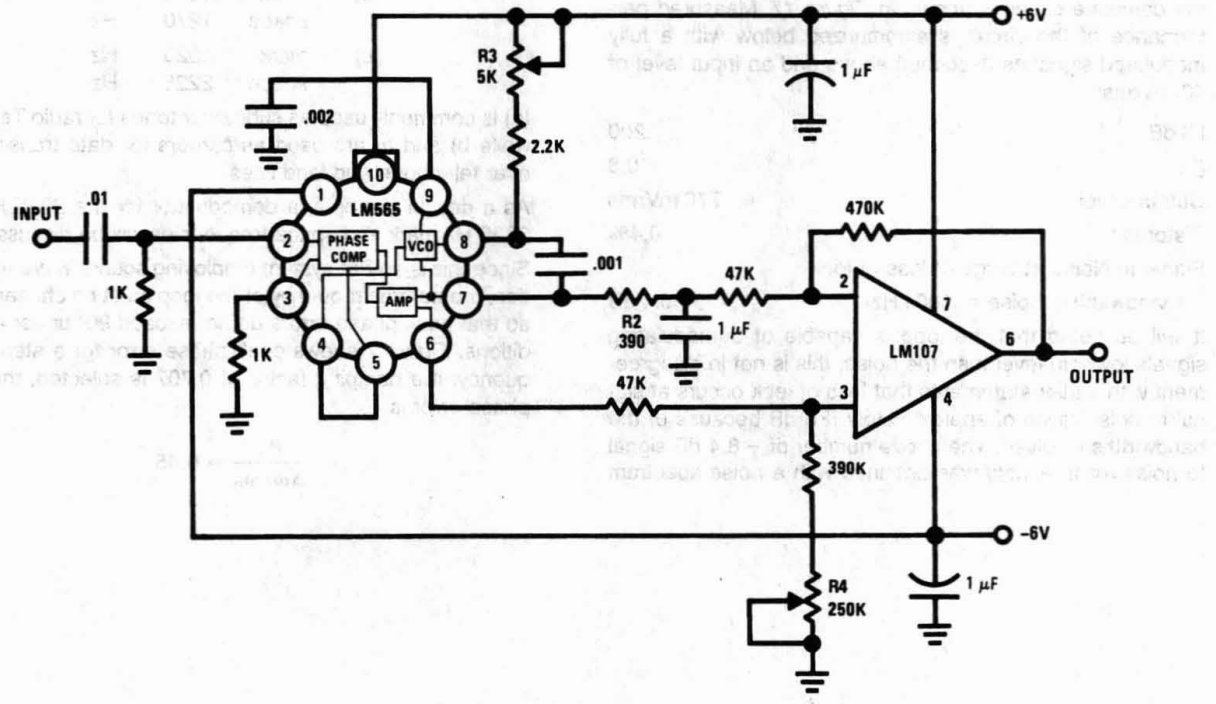

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FIGURE 17. IRIG Channel 13 Demodulator

Selecting a worst case of $\omega_n/\omega_m = 1$, $\omega_n = 2\pi \times 220$ Hz; selecting a damping factor of 0.707,

$$\frac{\theta}{\Delta\omega/\omega_n} = 0.702$$

or

$$\theta_e = 0.702\frac{\Delta\omega}{\omega_n} = 0.702\frac{2\pi \times 1088\ \text{Hz}}{2\pi \times 220\ \text{Hz}} = 3.45\ \text{radians}$$

this is unacceptable, since it would throw the loop out of lock, so it is necessary to try a higher value of ω_n. Let $\omega_n = 2\pi$x 500 Hz, then $\omega_m/\omega_n = 0.44$, and

$$\theta_e = 0.44\frac{\Delta\omega}{\omega_n} = 0.44 \times \frac{2\pi \times 1088}{2\pi \times 500} = 0.95\ \text{radians}$$

this should be a good choice, since it is close to 1 radian. Operating at 14.5 kHz, the LM565 has a loop gain K_OK_D of

$$2.28 \times 14.5 \times 10^3 = 33 \times 10^3\ \text{sec}$$

the value of the loop filter capacitor, C_1, can be found from *Figure 4*:

$$\tau_1 + \tau_2 = 3.5 \times 10^{-3}\ \text{sec}$$

from *Figure 5*, the value of τ_2 can be found (for a damping factor of 0.707)

$$\tau_2 = 4.4 \times 10^{-4}\ \text{sec}$$

$$\tau_1 = (35 - 4.4) \times 10^{-4}\ \text{sec} = 31.4 \times 10^{-4}\ \text{sec}$$

$$C_1 = \frac{\tau_1}{R} = \frac{31.4 \times 10^{-4}\ \text{sec}}{3.6\ \text{k}\Omega} \cong 1\ \mu\text{F}$$

$$R_2 = \frac{4.4 \times 10^{-4}\ \text{sec}}{1 \times 10^{-6}\ \mu\text{F}} = 440\Omega$$

Looking at *Figure 10*, the noise bandwidth B_L can be estimated to be

$$B_L = 0.6\,\omega_n = 0.6 \times 3150\ \text{rad/sec} = 1890\ \text{Hz}$$

the complete circuit is shown in *Figure 17*. Measured performance of the circuit is summarized below with a fully modulated signal as described above and an input level of 40 mVrms:

f 3 dB	200
ζ	0.8
Output Level	770 mVrms
Distortion	0.4%
Signal to Noise at verge of loss of lock (bandwidth of noise = 100 kHz)	−8.4 dB

It will be noted that the loop is capable of demodulating signals lower in level than the noise; this is not in disagreement with earlier statements that loss of lock occurs at signal to noise ratios of approximately +6 dB because of the bandwidths involved. The above number of −8.4 dB signal to noise for threshold was obtained with a noise spectrum 100 kHz wide. The noise power in the loop will be reduced by the ratio of loop noise bandwidth to input noise bandwidth

$$\frac{B_{LOOP}}{B_{INPUT}} = \frac{1890\ \text{Hz}}{100\ \text{kHz}} = 0.02\ \text{or}\ -17\ \text{dB}$$

the equivalent signal to noise in the loop is −8.4 dB +17 dB = +8.6 dB which is close to the above-mentioned limit of +6 dB. It should also be noted that loss of lock was noted with full modulation of the signal which will degrade threshold somewhat (although the measurement is more realistic).

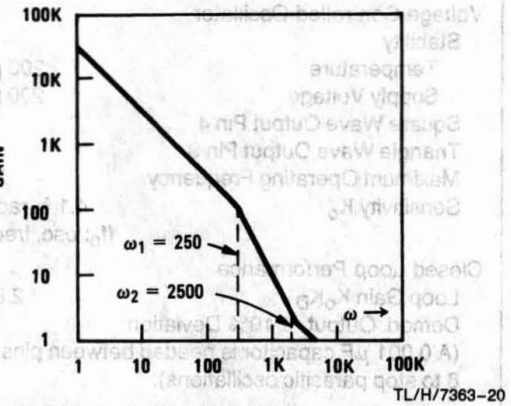

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FIGURE 18. Bode Plot for Circuit of *Figure 17*

FSK DEMODULATOR

Frequency shift keying (FSK) is widely used for the transmission of Teletype information, both in the computer peripheral and communications field. Standards have evolved over the years, and the commonly used frequencies are as follows:

a)	mark	2125	Hz
	space	2975	Hz
b)	mark	1070	Hz
	space	1270	Hz
c)	mark	2025	Hz
	space	2225	Hz

(a) is commonly used as subcarrier tones for radio Teletype, while b) and c) are used as carriers for data transmission over telephone and land lines.

As a design example, a demodulator for the 2025 Hz and 2225 Hz mark and space frequencies will be discussed.

Since this is an FM system employing square wave modulation, the natural frequency of the loop must be chosen again so that peak phase errors do not exceed 90° under all conditions. *Figure 7* shows peak phase error for a step in frequency; if a damping factor of 0.707 is selected, the peak phase error is

$$\frac{\theta_e}{\Delta\omega/\omega_n} = 0.45$$

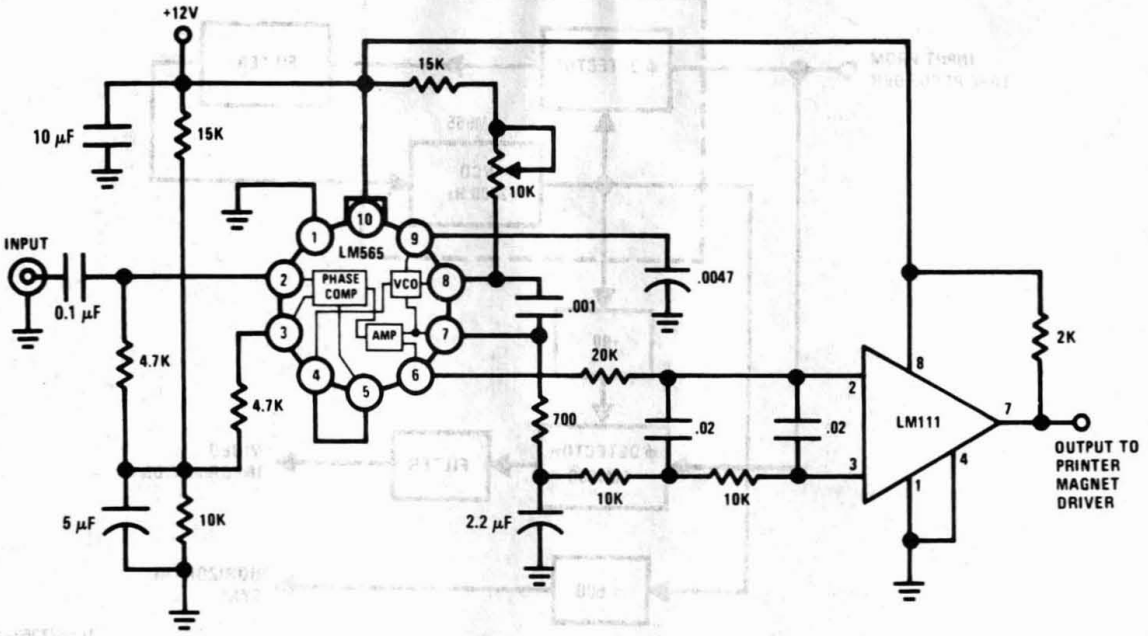

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FIGURE 19. FSK Demodulator (2025–2225 cps)

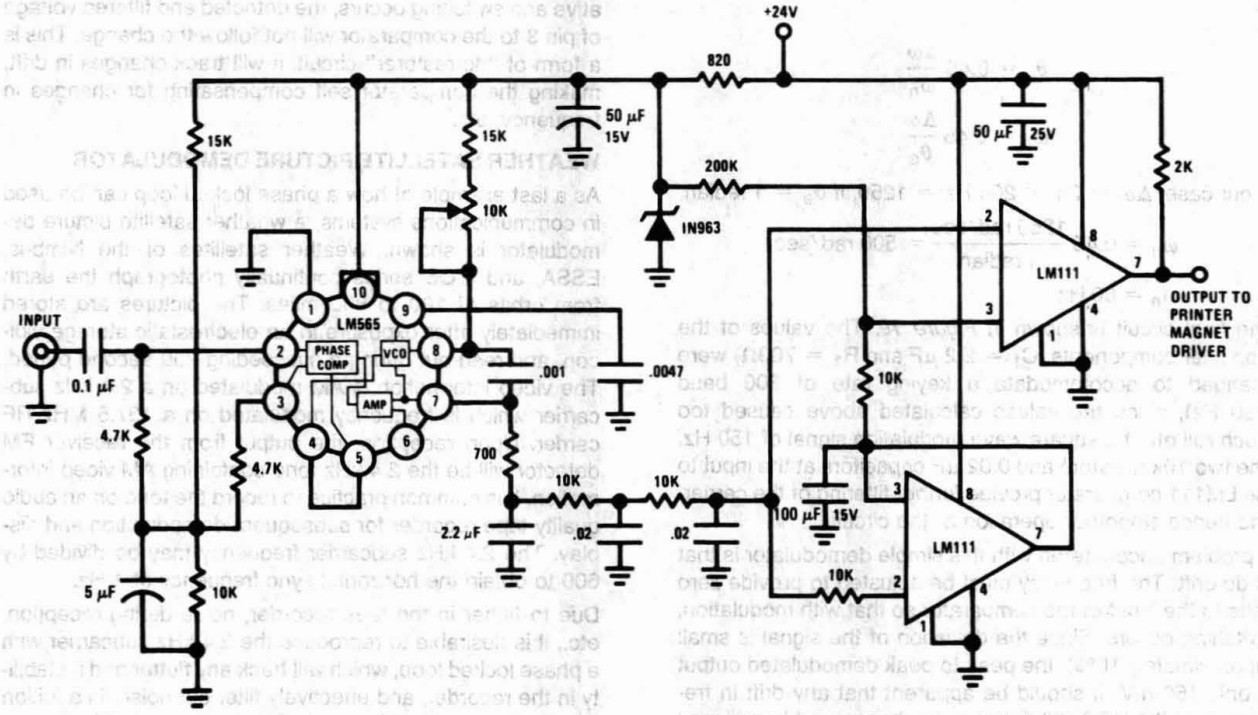

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FIGURE 20. FSK Demodulator with DC Restoration

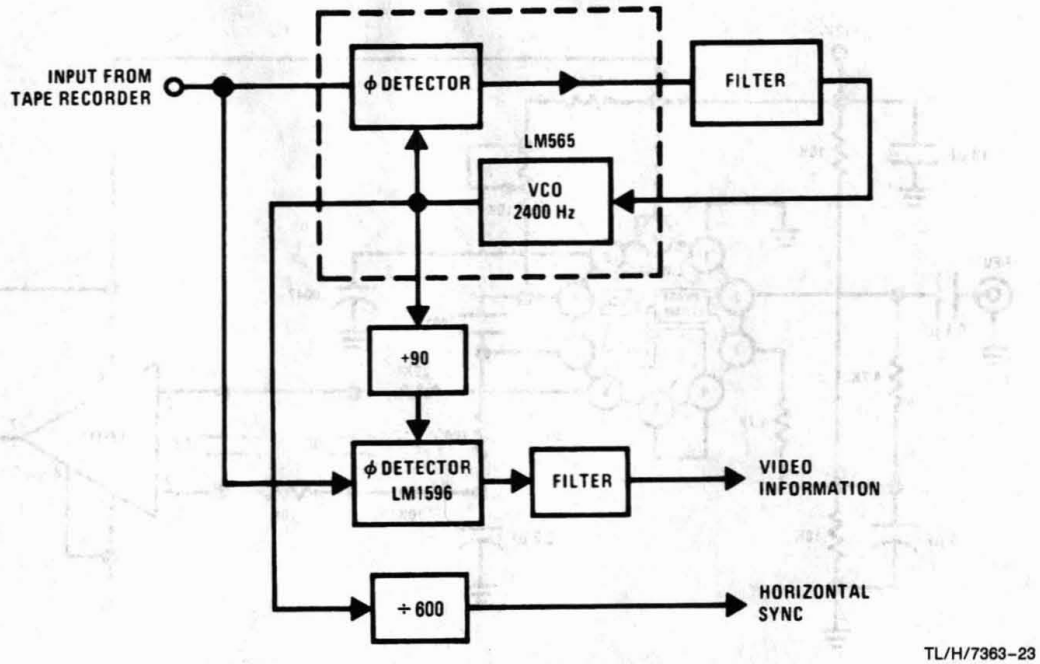

FIGURE 21. Block Diagram of Weather Satellite Demodulator

or

$$\theta_e = 0.45 \frac{\Delta\omega}{\omega_n}$$

$$\omega_n = 0.45 \frac{\Delta\omega}{\theta_e}$$

in our case, $\Delta\omega = 2\pi \times 200\ \text{Hz} = 1250$, if $\theta_e = 1$ radian,

$$\omega_n = 0.45 \frac{1250\ \text{rad/sec}}{1\ \text{radian}} = 500\ \text{rad/sec}$$

$$f_n = 80\ \text{Hz}$$

The final circuit is shown in *Figure 19*. The values of the loop filter components ($C_1 = 2.2\ \mu F$ and $R_1 = 700\Omega$) were changed to accommodate a keying rate of 300 baud (150 Hz), since the values calculated above caused too much roll off of a square wave modulation signal of 150 Hz. The two 10k resistors and 0.02 μF capacitors at the input to the LM111 comparator provide further filtering of the carrier, and hence smoother operation of the circuit.

A problem encountered with this simple demodulator is that of dc drift. The frequency must be adjusted to provide zero volts to the input of the comparator so that with modulation, switching occurs. Since the deviation of the signal is small (approximately 10%), the peak to peak demodulated output is only 150 mV. It should be apparent that any drift in frequency of the VCO will cause a dc change and hence may lock the comparator in one state or the other. A circuit to overcome this problem is shown in *Figure 20*. While using the same basic demodulator configuration, an LM111 is used as an accurate peak detector to provide a dc bias for one input to the comparator. When a "space" frequency is transmitted, and the output at pin 7 of the LM565 goes negative and switching occurs, the detected and filtered voltage of pin 3 to the comparator will not follow the change. This is a form of "dc restorer" circuit: it will track changes in drift, making the comparator self compensating for changes in frequency, etc.

WEATHER SATELLITE PICTURE DEMODULATOR

As a last example of how a phase locked loop can be used in communications systems, a weather satellite picture demodulator is shown. Weather satellites of the Nimbus, ESSA, and ITOS series continually photograph the earth from orbits of 100 to 800 miles. The pictures are stored immediately after exposure in an electrostatic storage vidicon, and read out during a succeeding 200 second period. The video information is AM modulated on a 2.4 kHz subcarrier which is frequency modulated on a 137.5 MHz RF carrier. Upon reception, the output from the receiver FM detector will be the 2.4 kHz tone containing AM video information. It is common practice to record the tone on an audio quality tape recorder for subsequent demodulation and display. The 2.4 kHz subcarrier frequency may be divided by 600 to obtain the horizontal sync frequency of 4 Hz.

Due to flutter in the tape recorder, noise during reception, etc., it is desirable to reproduce the 2.4 kHz subcarrier with a phase locked loop, which will track any flutter and instability in the recorder, and effectively filter out noise, in addition to providing a signal large enough for the digital frequency divider. In addition, an in phase component of the VCO signal may be used to drive a synchronous demodulator to detect the video information. A block diagram of the system is shown in *Figure 21*, and a complete schematic in *Figure 22*.

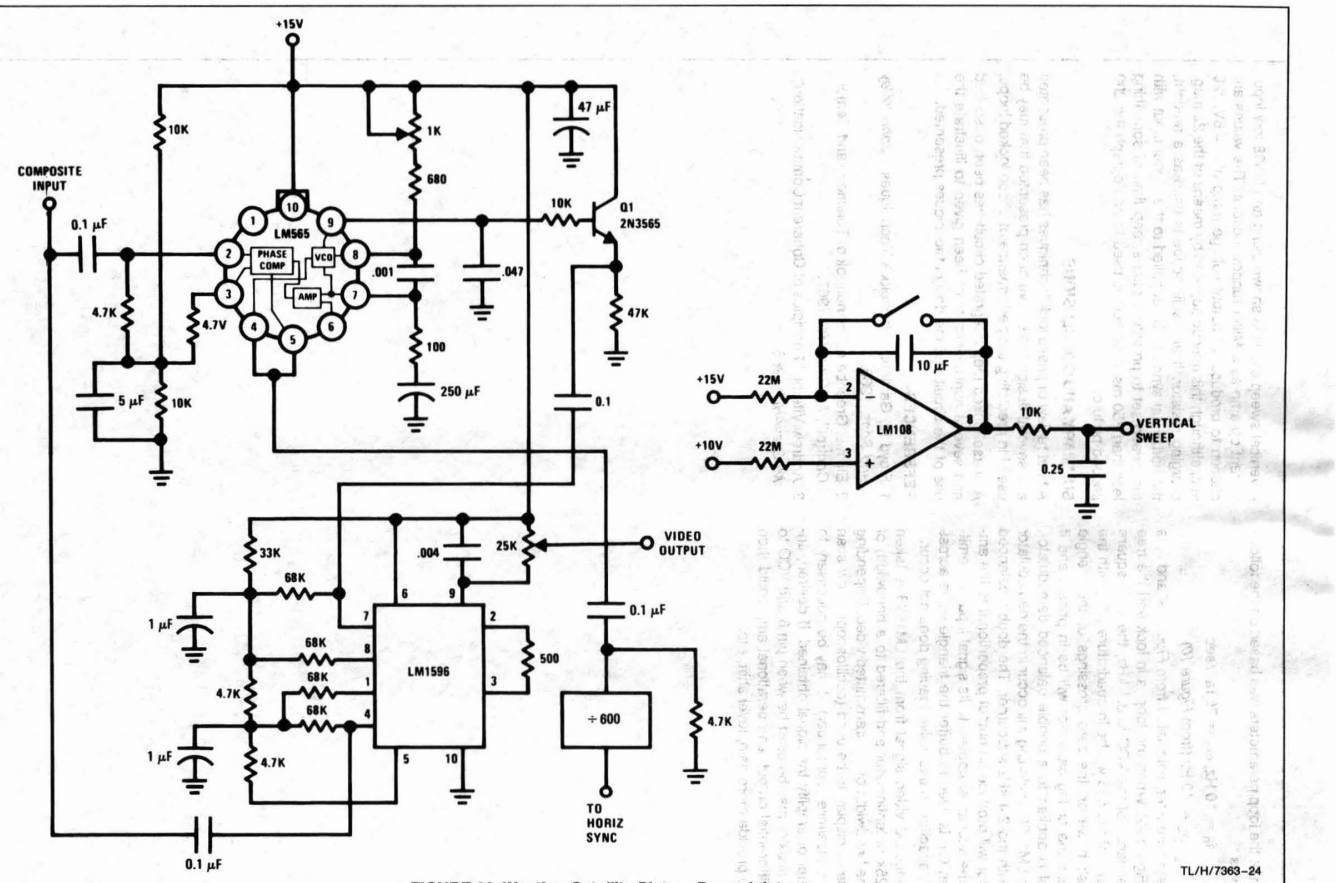

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FIGURE 22. Weather Satellite Picture Demodulator

The design of the loop parameters was based on the following objectives

$$f_n = 10 \text{ Hz}, \omega_n = 75 \text{ rad/sec}$$

$$B_L = 40 \text{ Hz (from } \textit{Figure 10}\text{)}$$

the complete loop filter, calculated from *Figures 4* and *5*, is shown in *Figure 22*. When the loop is in lock and the free running frequency of the VCO is 2.4 kHz, the VCO square wave at pin 4 of the 565 will be in quadrature (90°) with the input signal; however, the zero crossings of the triangle wave across the timing capacitor will be in phase, and if their signal is applied to a double balanced demodulator, such as an LM1596, switching will occur in the demodulator in phase with the 2.4 kHz subcarrier. The double balanced demodulator will produce an output proportional to the amplitude of the subcarrier applied to its signal input. An emitter follower, Q_1, is used to buffer the triangle wave across the timing capacitor so excessive loading does not occur.

The demodulated video signal from the LM1596 is taken across a 25k potentiometer and filtered to a bandwidth of 1.4 kHz, the bandwidth of the transmitted video. Depending on the type of display to be used (oscilloscope, slow scan TV monitor, facsimile reproducer), it may be necessary to further buffer or amplify the signal obtained. If desired, another load resistor may be used between pin 6 and VCO to obtain a differential output; an operational amp could then be used to provide more gain, level shift, etc.

A vertical sweep circuit is shown using an LM308 low input current op amp as a Miller rundown circuit. The values are chosen to produce an output voltage ramp of −4.5V/220 sec, although this may be adjusted by means of the 22 meg. charging resistor. If an oscilloscope is used as a readout, the horizontal sync can be supplied to the trigger input with the sweep set to provide a total sweep time of something less than 250 ms. A camera is used to photograph the 200 second picture.

SUMMARY AND CONCLUSIONS

A brief review of phase lock techniques has been presented and several design tools have been presented that may be useful in predicting the performance of phase locked loops.

A phase locked loop integrated circuit has been described and several applications have been given to illustrate the use of the circuit and the design techniques presented.

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1. Floyd M. Gardner, "Phaselock Techniques", *John Wiley and Sons*, 1966.
2. Elliot L. Greenberg, "Handbook of Telemetry and Remote Control", *McGraw-Hill*, 1967.
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Applications for a New Ultra-High Speed Buffer

National Semiconductor
Application Note 48

INTRODUCTION

Voltage followers have gained in popularity in applications such as sample and hold circuits, general purpose buffers, and active filters since the introduction of IC operational amplifiers. Since they were not specifically designed as followers, these early IC's had limited usage due to low bandwidth, low slew rate and high input current. Usage of voltage followers was expanded in 1967 with the introduction of the LM102, the first IC designed specifically as a voltage follower. With the LM102, engineers were able to obtain an order of magnitude improvement in performance and extend usage into medium speed applications. The LM110, an improved LM102, was introduced in late 1969. However, even higher speeds and lower input currents were needed for very fast sample and holds, A to D and D to A converters, coax cable drivers, and other video applications.

The solution to this application problem was attained by combining technologies into a single package. The result, the LH0033 high speed buffer, utilizes JFET and bipolar technology to produce a ultra-fast voltage follower and buffer whose propagation delay closely approaches speed-of-light delay across its package, while not compromising input impedance or drive characteristics. Table I compares various voltage followers and illustrates the superiority of the LH0033 in both low input current or high speed video applications.

CIRCUIT CONSIDERATIONS

The junction FET makes a nearly ideal input device for a voltage follower, reducing input bias current to the picoamp range. However, FET's exhibit moderate voltage offsets and offset drifts which tend to be difficult to compensate. The simple voltage follower of *Figure 1* eliminates initial offset and offset drift if Q_1 and Q_2 are identically matched transistors. Since the gate to source voltage of Q_2 equals zero volts, then Q_1's gate to source voltage equals zero volts. Furthermore as V_{P1} changes with temperature (approximately 2.2 mV/°C), V_{P2} will change by a corresponding amount. However, as load current is drawn from the output, Q_1 and Q_2 will drift at different rates, A circuit which overcomes offset voltage drift is used in a new high speed buffer amplifier, the LH0033. Initial offset is typically 5 mV and offset drift is 20 μV/°C. Resistor R_2 is used to establish the drain current of current source transistor, Q_2 at 10 mA.

The same drain current flows through Q_1 causing a voltage at the source of approximately 1.1V. The 10 mA flowing through R_1 plus Q_3's V_{BE} of 0.6V causes the output to sit at zero volts for zero volts in. Q_3 and Q_4 eliminate loading the input stage (except for base current) and CR_1 and CR_2 establish the output stage collector current.

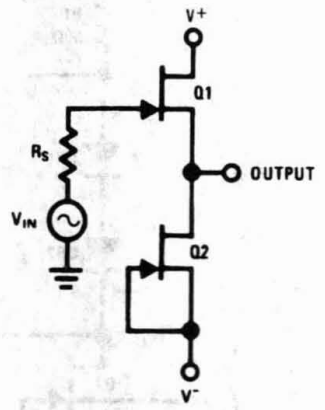

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FIGURE 1. Simple Voltage Follower Schematic

If Q_1 and Q_2 are matched, the resulting drift is reduced to a few μV/°C.

PERFORMANCE OF THE LH0033 FAST VOLTAGE FOLLOWER/BUFFER

The major electrical characteristics of the LH0033 are summarized in Table II. All the virtues of a ultra-high speed buffer have been incorporated.

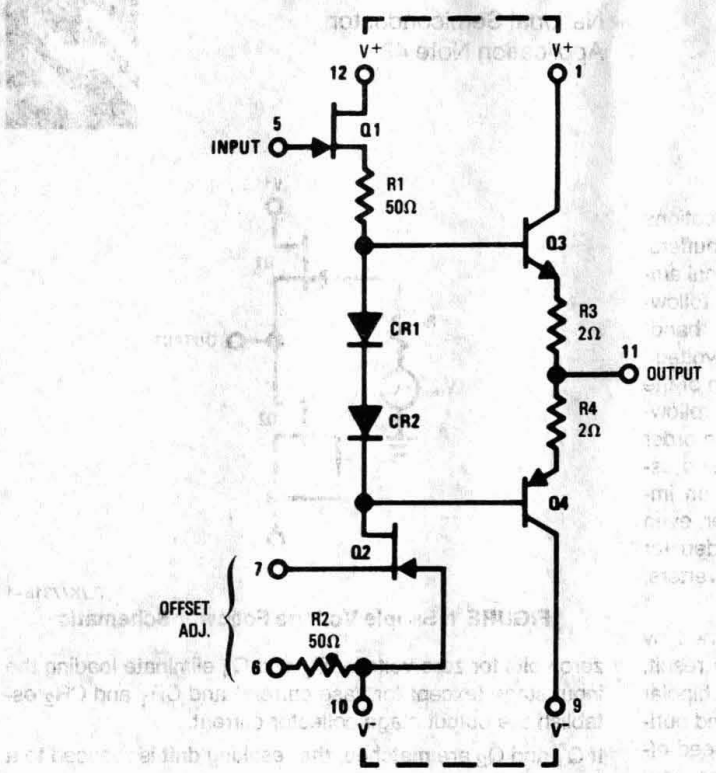
Figure 3 is a plot of input bias current vs temperature and shows the typical FET input characteristics. Other typical performance curves are illustrated in *Figures 4* through *10*. Of particular interest is *Figure 8*, which demonstrates the performance of the LH0033 in video applications to over 100 MHz.

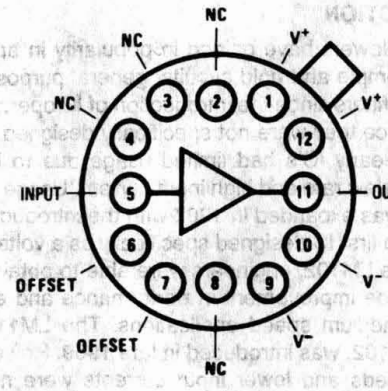
APPLICATIONS FOR ULTRA-FAST FOLLOWERS

The LH0033's high input impedance (10^{11} Ω, shunted by 2 pF) and high slew rate assure minimal loading and high fidelity in following high speed pulses and signals. As shown below, the LH0033 is used as a buffer between MOS logic and a high speed dual limit comparator. The device's high input impedance prevents loading of the MOS logic signal (even a conventional scope probe will distort high output impedance MOS). The LH0033 adds about a 1.5 ns to the total delay of the comparator. Adjustment of voltage divider R_1, R_2 allows interface to TTL, DTL and other high speed logic forms.

TABLE I. COMPARISON OF VOLTAGE FOLLOWERS

Parameter	Conventional Monolithic Op Amp LM741	First Generation Voltage Follower LM102	Second Generation Voltage Follower LM110	Specially Designed Voltage Follower LH0033
Input Bias Current	200 nA	3.0 nA	1.0 nA	0.05 nA
Slew Rate	0.5 V/μs	10V/μs	30V/μs	1500V/μs
Bandwidth	1.0 MHz	10 MHz	20 MHz	100 MHz
Prop. Delay Time	350 ns	35 ns	18 ns	1.2 ns
Output Current Capability	±5 mA	±2 mA	±2 mA	±100 mA





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Top View

FIGURE 2. LH0033 Schematic

TABLE II

Parameter	Conditions	Value	Parameter	Conditions	Value
Output Offset Voltage	R_S = 100 kΩ	5 mV	Output Current Capability		± 100 mA peak
Input Bias Current		50 pA	Slew Rate	R_S = 50Ω, R_L = 1k	1500V/μs
Input Impedance	V_{IN} = 1.0 Vrms R_L = 1k, f = 1 kHz	10^{11} Ω	Propagation Delay		1.2 ns
Voltage Gain	V_{IN} = 1.0 Vrms R_L = 1k, f = 1 kHz, R_S = 100k	0.98	Bandwidth	V_{IN} = 1.0 Vrms R_S = 50Ω, R_L = 1k	100 MHz
Output Voltage Swing	V_S = ±15V, R_S = 100k R_L = 1k	±13V			

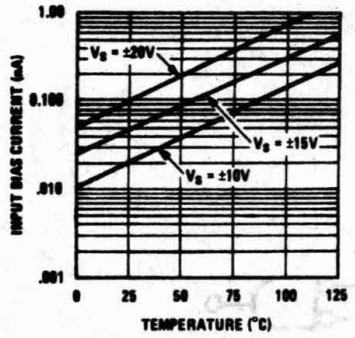

FIGURE 3. Input Bias Current vs Temperature

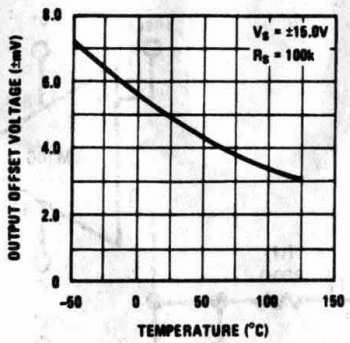

FIGURE 4. Output Offset Voltage vs Temperature

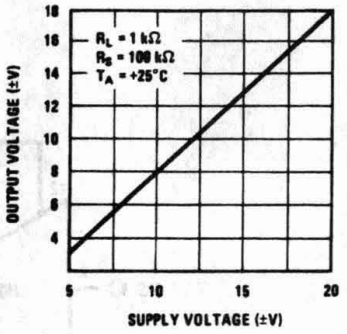

FIGURE 5. Output Voltage vs Supply Voltage

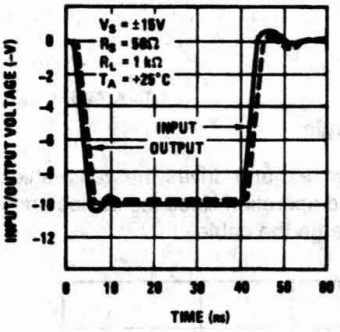

FIGURE 6. Negative Pulse Response

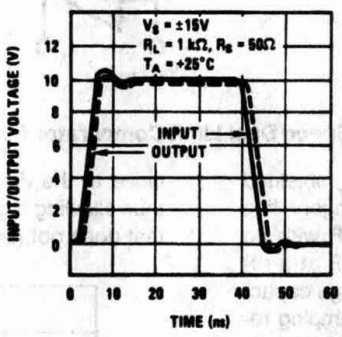

FIGURE 7. Positive Pulse Response

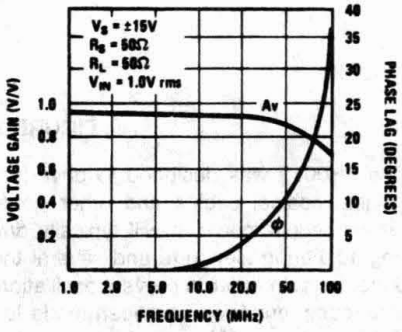

FIGURE 8. Frequency Response

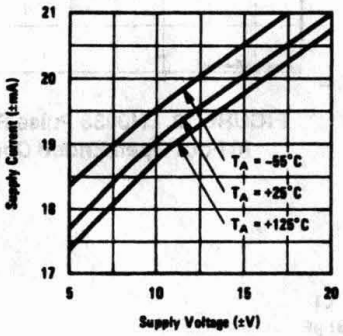

FIGURE 9. Supply Current vs Supply Voltage

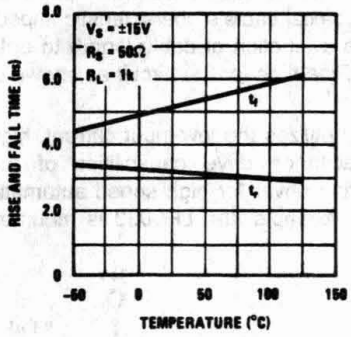

FIGURE 10. Rise and Fall Time vs Temperature

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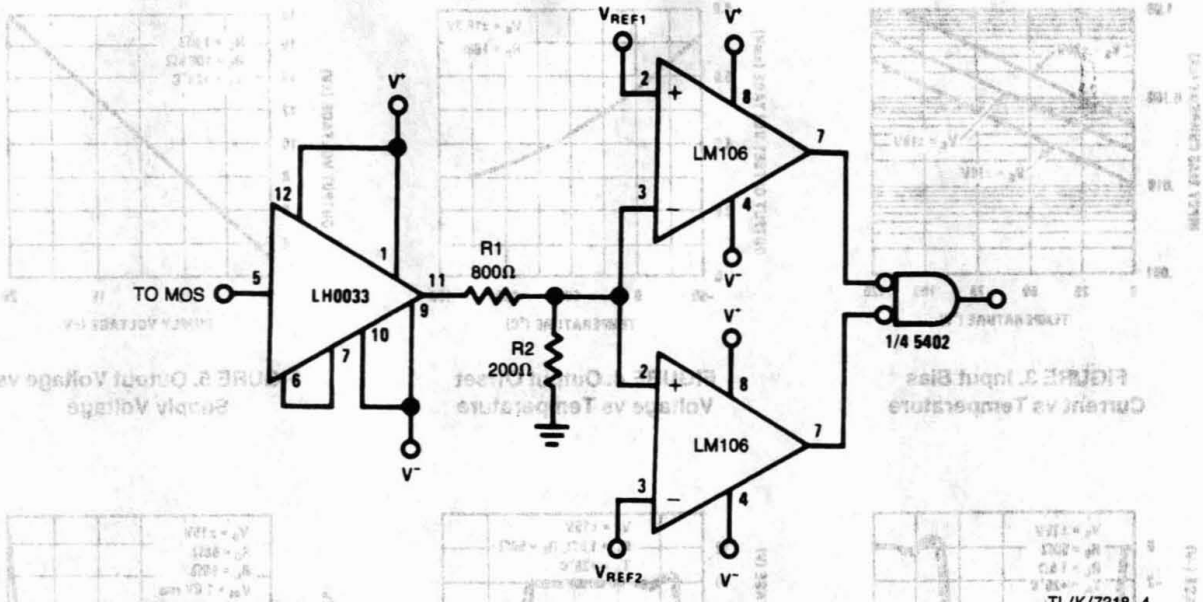

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FIGURE 11. High Speed Dual Limit Comparator for MOS Logic

The LH0033 was designed to drive long cables, shielded cables, coaxial cables and other generally stringent line driving requirements. It will typically drive 200 pF with no degradation in slew rate and several thousand pF at a reduced rate. In order to prevent oscillations with large capacitive loads, provision has been made to insert damping resistors between V^+ and pin 1, and V^- and pin 9. Values between 47 and 100Ω work well for $C_L > 1000$ pF. For non-reactive loads, pin 12 should be shorted to pin 1 and pin 10 shorted to pin 9. A coaxial driver is shown in *Figure 13*. Pin 6 is shorted to pin 7, obtaining an initial offset of 5.0 mV, and the 43Ω coupled with the LH0033's output impedance (about 6Ω) match the coaxial cable's characteristic impedance. C_1 is adjusted as a function of cable length to optimize rise and fall time. Rise time for the circuit as shown in *Figure 12*, is 10 ns.

Another application that utilizes the low input current, high speed and high capacitance drive capabilities of the LH0033 is a shield or line driver for high speed automatic test equipment. In this example, the LH0033 is mounted close to the device under test and drives the cable shield thus allowing higher speed operation since the device under test does not have to charge the cable.

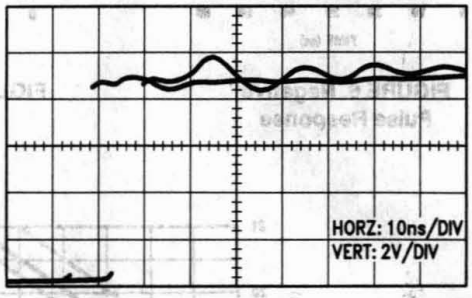

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FIGURE 12. LH0033 Pulse Response into 10 Foot Open Ended Coaxial Cable

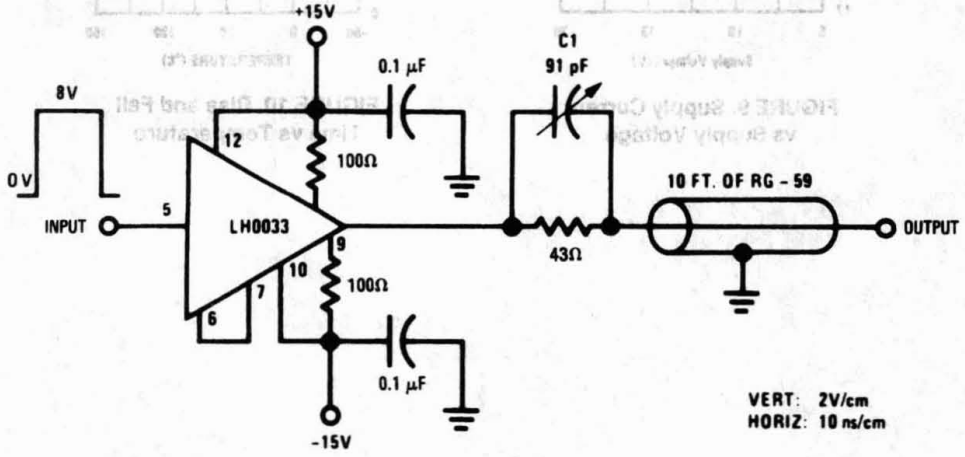

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FIGURE 13

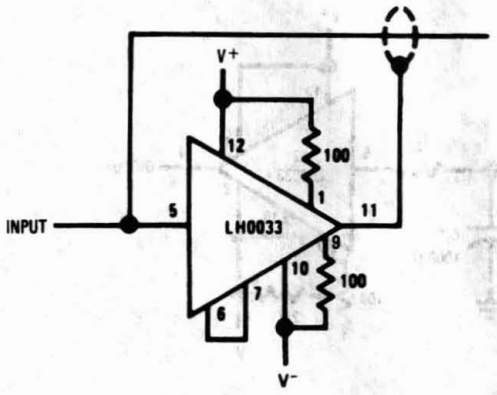

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FIGURE 14. Instrumentation Shield/Line Driver

The LH0033's high input impedance and low input bias current may be utilized in medium speed circuits such as Sample and Hold, and D to A converters. *Figure 15* shows an LH0033 used as a buffer in medium speed D to A converter.

Offset null is accomplished by connecting a 100Ω pot between pin 7 and V⁻. It is generally a good idea to insert 20Ω in series with the pot to prevent excessive power dissipation in the LH0033 when the pot is shorted out. In non-critical or AC coupled applications, pin 6 should be shorted to pin 7. The resulting output offset is typically 5 mV at 25°C.

The high output current capability and slew rate of the LH0033 are utilized in the sample and hold circuit of *Figure 16*. Amplifier, A1 is used to buffer high speed analog signals. With the configuration shown, acquisition time is limited by the time constant of the switch "ON" resistance and sampling capacitor, and is typically 200 or 300 ns.

A_2's low input bias current, results in drifts in hold mode of

$$\frac{50\ \text{mV}}{\text{sec}}\ \text{at}\ 25°\text{C} \quad \text{and} \quad \frac{1\text{V}}{\text{sec}}\ \text{at}\ 125°\text{C}.$$

The LH0033 may be utilized in AC applications such as video amplifiers and active filters. The circuit of *Figure 17* utilizes boot strapping to achieve input impedances in excess of 10 MΩ.

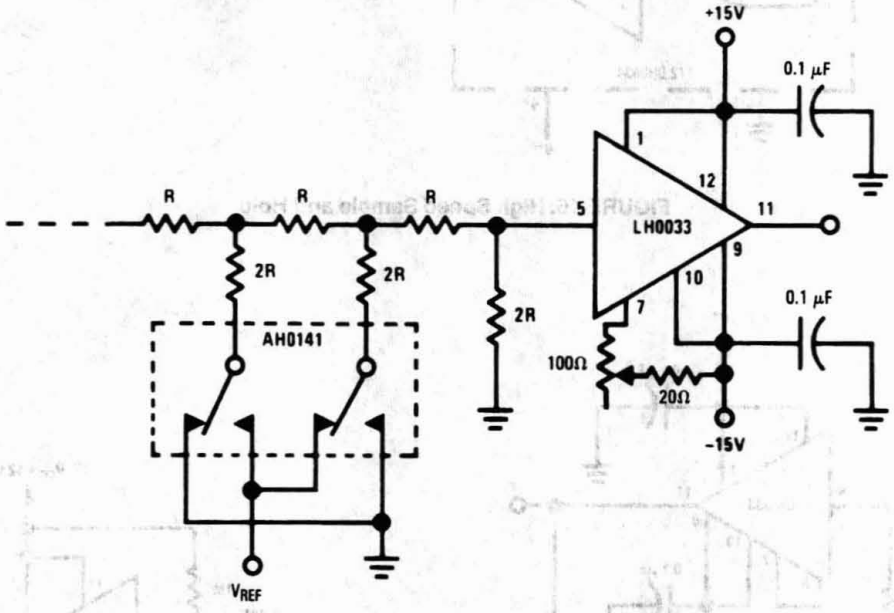

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FIGURE 15

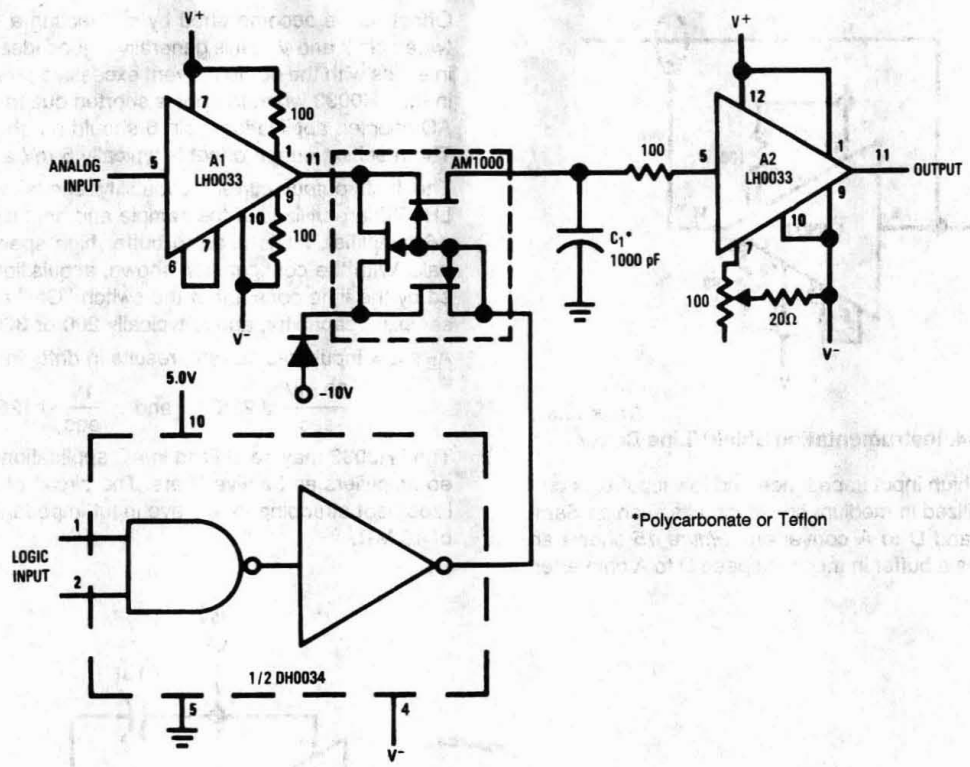

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FIGURE 16. High Speed Sample and Hold

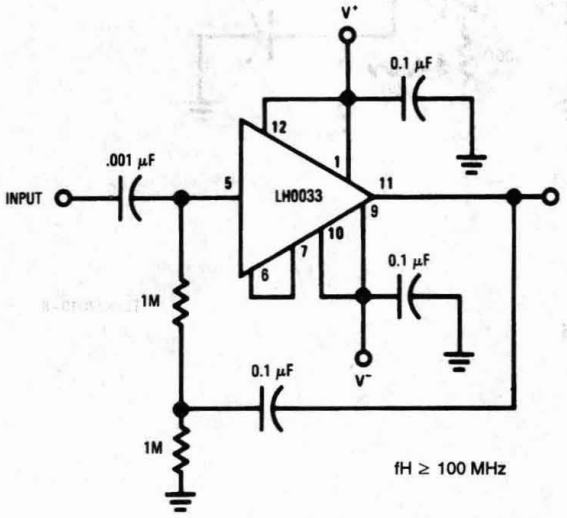

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FIGURE 17. High Input Impedance AC Coupled Amplifier

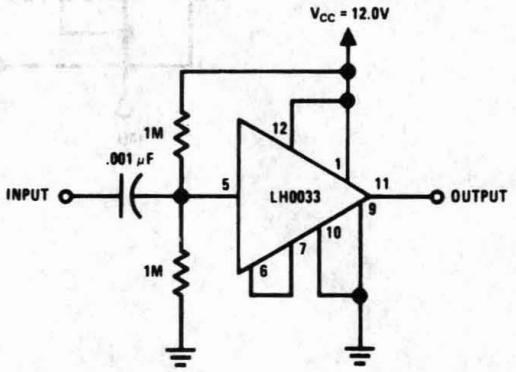

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FIGURE 18. Single Supply AC Amplifier

A single supply, AC coupled amplifier is shown in *Figure 18.* Input impedance is approximately 500k and output swing is in excess of 8V peak-to-peak with a 12V supply.

The LH0033 may be readily used in applications where symmetrical supplies are unavailable or may not be desirable. A typical application might be an interface to an MOS shift register where $V^+ = 5.0V$ and $V^- = -25V$. In this case, an apparent output offset occurs. In reality, the output voltage is due to the LH0033's voltage gain of less than unity.

The output voltage shift due to asymmetrical supplies may be predicted by:

$$\Delta V_O \cong (1 - Av)\frac{(V^+ - V^-)}{2} = .005\,(V^+ - V^-)$$

where: Av = No load voltage gain, typically 0.99.

V^+ = Positive Supply Voltage.

V^- = Negative Supply Voltage.

For the foregoing application, ΔV_O would be −100 mV. This apparent "offset" may be adjusted to zero as outlined above.

Figure 19 shows a high Q, notch filter which takes advantage of the LH0033's wide bandwidth. For the values shown, the center frequency is 4.5 MHz.

The LH0033 can also be used in conjunction with an operational amplifier as current booster as shown in *Figure 20*.

Output currents in excess of 100 mA may be obtained. Inclusion of 150Ω resistors between pins 1 and 12, and 9 and 10 provide short circuit protection, while decoupling pins 1 and 9 with 1000 pF capacitors allow near full output swing.

The value for the short circuit current is given by:

$$I_{SC} \cong \frac{V^+}{R_{LIMIT}} = \frac{V^-}{R_{LIMIT}}$$

where: $I_{SC} \leq 100$ mA.

SUMMARY

The advantages of a FET input buffer have been demonstrated. The LH0033 combined very high input impedance, wide bandwidth, very high slew rate, high output capability, and design flexibility, making it an ideal buffer for applications ranging from DC to in excess of 100 MHz.

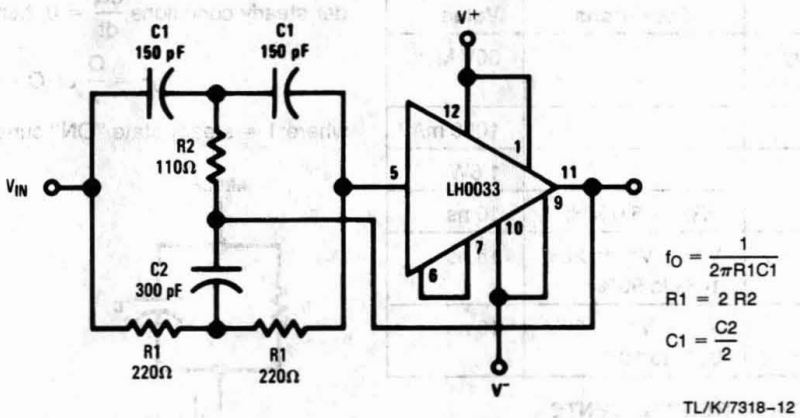

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FIGURE 19. 4.5 MHz Notch Filter

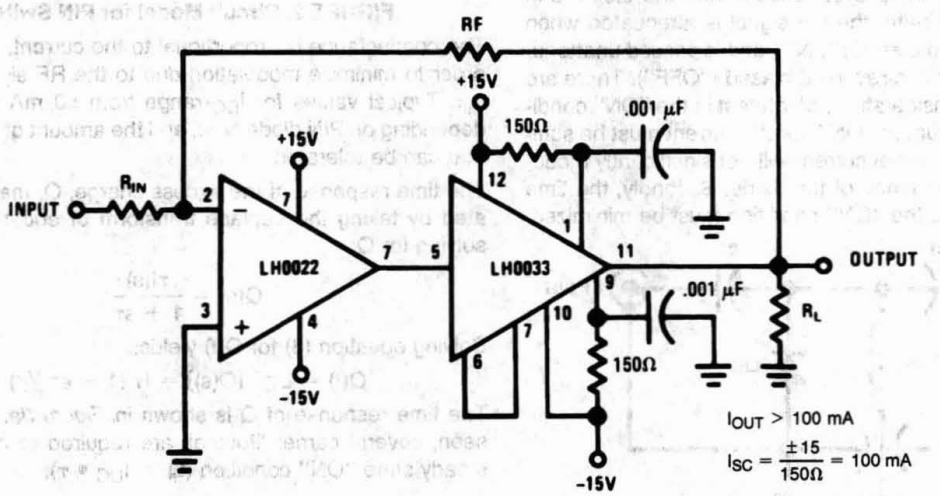

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FIGURE 20. Using LH0033 as an Output Buffer

PIN Diode Drivers

National Semiconductor
Application Note 49

INTRODUCTION

The DH0035/DH0035C is a TTL/DTL compatible, DC coupled, high speed PIN diode driver. It is capable of delivering peak currents in excess of one ampere at speeds up to 10 MHz. This article demonstrates how the DH0035 may be applied to driving PIN diodes and comparable loads which require high peak currents at high repetition rates. The salient characteristics of the device are summarized in Table I.

TABLE I. DH0035 Characteristics

Parameter	Conditions	Value
Differential Supply Voltage ($V^+ - V^-$)		30V Max.
Output Current		1000 mA
Maximum Power		1.5W
t_{delay}	PRF = 5.0 MHz	10 ns
t_{rise}	$V^+ - V^- = 20V$ 10% to 90%	15 ns
t_{fall}	$V^+ - V^- = 20V$ 90% to 10%	10 ns

PIN DIODE SWITCHING REQUIREMENTS

Figure 1 shows a simplified schematic of a PIN diode switch. Typically, the PIN diode is used in RF through microwave frequency modulators and switches. Since the diode is in shunt with the RF path, the RF signal is attenuated when the diode is forward biased ("ON"), and is passed unattenuated when the diode is reversed biased ("OFF"). There are essentially two considerations of interest in the "ON" condition. First, the amount of "ON" control current must be sufficient such that RF signal current will not significantly modulate the "ON" impedance of the diode. Secondly, the time required to achieve the "ON" condition must be minimized.

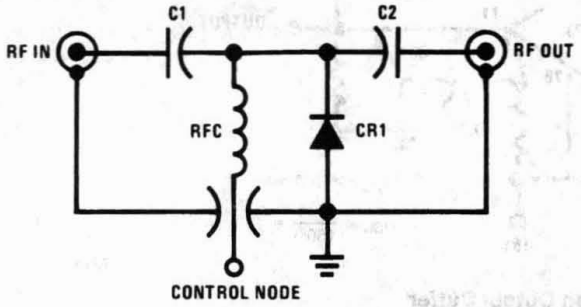

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FIGURE 1. Simplified PIN Diode Switch

The charge control model of a diode[1,2] leads to the charge continuity equation given in equation (1).

$$i = \frac{dQ}{dt} + \frac{Q}{\tau} \quad (1)$$

where: Q = charge due excess minority carriers

τ = mean lifetime of the minority carriers

Equation (1) implies a circuit model shown in *Figure 2*. Under steady conditions $\frac{dQ}{dt} = 0$, hence:

$$I_{DC} = \frac{Q}{\tau} \text{ or } Q = I_{DC} \bullet \tau \quad (2)$$

where: I = steady state "ON" current.

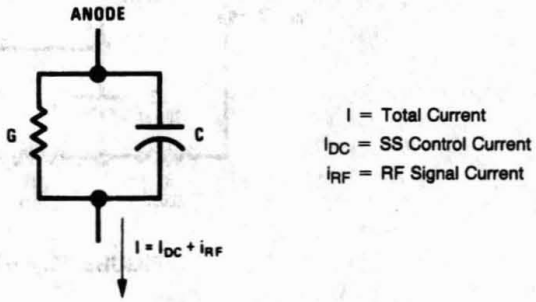

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FIGURE 2. Circuit Model for PIN Switch

The conductance is proportional to the current, I; hence, in order to minimize modulation due to the RF signal, $I_{DC} \gg i_{RF}$. Typical values for I_{DC} range from 50 mA to 200 mA depending on PIN diode type, and the amount of modulation that can be tolerated.

The time response of the excess charge, Q, may be evaluated by taking the Laplace transform of equation (1) and solving for Q:

$$Q(s) = \frac{\tau I(s)}{1 + s\tau} \quad (3)$$

Solving equation (3) for Q(t) yields:

$$Q(t) = L^{-1}[Q(s)] = I\tau\,(1 - \epsilon^{-t/\tau}) \quad (4)$$

The time response of Q is shown in *Figure 3a*. As can be seen, several carrier lifetimes are required to achieve the steady state "ON" condition ($Q = I_{DC} \bullet \tau$).

The time response of the charge, hence the time for the diode to achieve the "ON" state could be shortened by applying a current spike, Ipk, to the diode and then dropping the current to the steady state value, I_{DC}, as shown in *Figure 3b*. The optimum response would be dictated by:

$$(Ipk)\,(t) = \tau \bullet I_{DC} \qquad (5)$$

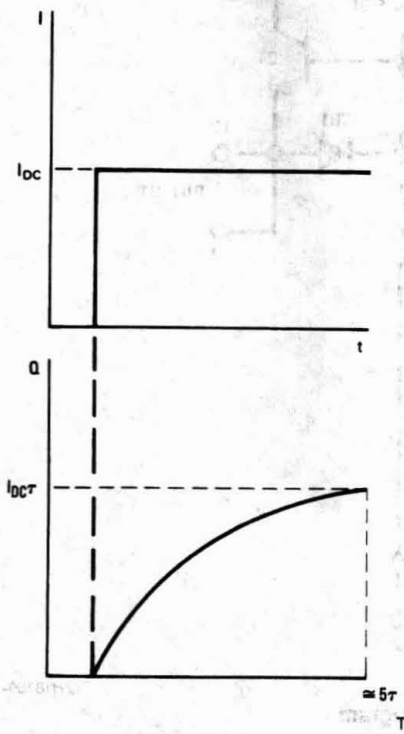

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FIGURE 3a

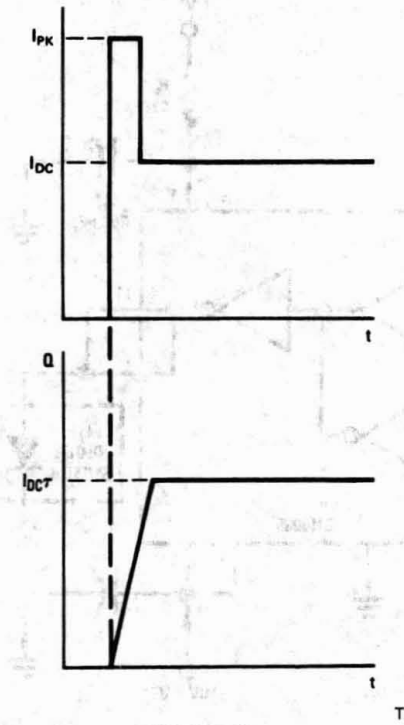

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FIGURE 3b

The turn off requirements for the PIN diode are equal to the turn on, except that in the "OFF" condition, the steady current drops to the diode's reverse leakage current. A charge, $I_{DC} \bullet \tau$, was stored in the diode in the "ON" condition and in order to achieve the "OFF" state this charge must be removed. Again, in order to remove the charge rapidly, a large peak current (in the opposite direction) must be applied to the PIN diode:

$$-Ipk \gg \frac{Q}{\tau} \qquad (6)$$

It is interesting to note an implication of equation (5). If the peak turn on current were maintained for a period of time, say equal to τ, then the diode would acquire an excess charge equal to Ipk • T. This same charge must be removed at turn off, instead of a charge $I_{DC} \bullet \tau$, resulting in a considerably slower turn off. Accordingly, control of the width of turn on current peak is critical in achieving rapid turn off.

APPLICATION OF THE DH0035 AS A PIN DIODE DRIVER

The DH0035 is specifically designed to provide both the current levels and timing intervals required to optimally drive PIN diode switches. Its schematic is shown in *Figure 4*. The device utilizes a complementary TTL input buffer such as the DM7830/DM8830 or DM5440/DM7440 for its input signals.

Two configurations of PIN diode switch are possible: cathode grounded and anode grounded. The design procedures for the two configurations will be considered separately.

ANODE GROUND DESIGN

Selection of power supply voltages is the first consideration. Table I reveals that the DH0035 can withstand a total of 30V differentially. The supply voltage may be divided symmetrically at ±15V, for example. Or asymmetrically at +20V and −10V. The PIN diode driver shown in *Figure 5*, uses ±10V supplies.

When the Q output of the DM8830 goes high a transient current of approximately 50 mA is applied to the emitter of Q_1 and in turn to the base of Q_5.

Q_5 has an $h_{fe} = 20$, and the collector current is $h_{fe} \times 50$ or 1000 mA. This peak current, for the most part, is delivered to the PIN diode turning it "ON" (RF is "OFF").

Ipk flows until C_2 is nearly charged. This time is given by:

$$t = \frac{C2\Delta V}{Ipk} \qquad (7)$$

where: ΔV = the change in voltage across C_2.

Prior to Q_5's turn on, C_2 was charged to the minus supply voltage of −10V. C_2's voltage will rise to within two diode drops plus a V_{sat} of ground:

$$V = |V^-| - Vf(\text{PIN Diode}) - Vf_{CR1} - V_{sat_{Q5}} \qquad (8)$$

for $V^- = -10V$, $\Delta V = 8V$.

Once C_2 is charged, the current will drop to the steady state value, I_{DC}, which is given by:

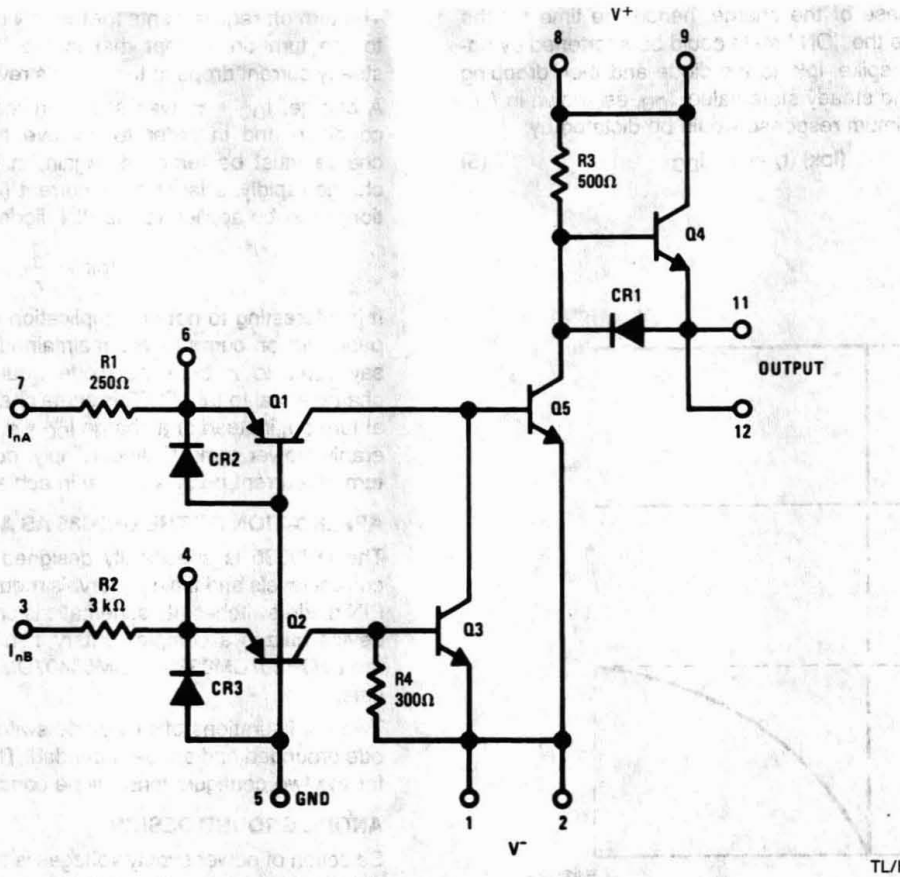
$$I_{DC} = \frac{V}{R_M} - \frac{V^+}{R_3} - \frac{V_{CC}}{R_1} \qquad (9)$$

where: $V_{CC} = 5.0V$

$R_1 = 250\Omega$

$R_3 = 500\Omega$

$$\therefore R_M = \frac{(R_3\,(\Delta V)\,(R_1)}{R_1V^+ + I_{DC}R_3R_1 + V_{CC}R_3} \qquad (9a)$$



TL/H/8750–5

FIGURE 4. DH0035 Schematic Diagram

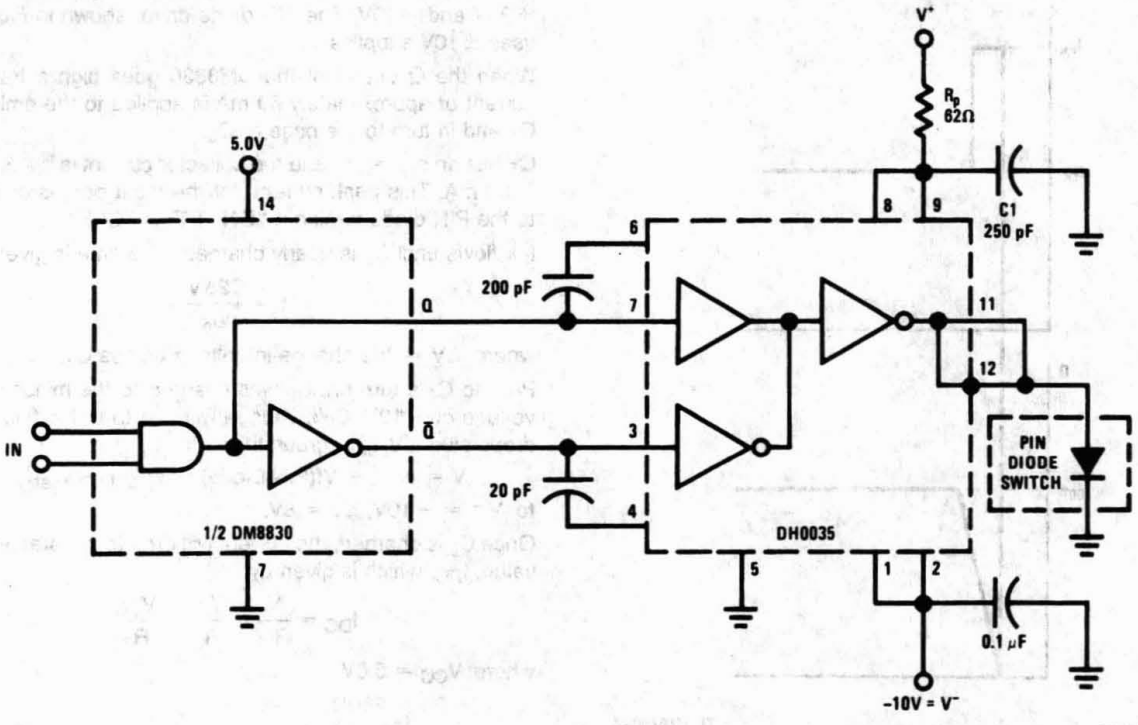


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FIGURE 5. Cathode Grounded Design

For the driver of *Figure 5*, and I_{DC} = 100 mA, R_M is 56Ω (nearest standard value).

Returning to equation (7) and combining it with equation (5) we obtain:

$$t = \frac{\tau I_{DC}}{Ipk} = \frac{C_2 V}{Ipk} \quad (10)$$

Solving equation (10) for C_2 gives:

$$C_2 = \frac{I_{DC}\tau}{V} \quad (11)$$

For τ = 10 ns, C_2 = 120 pF.

One last consideration should be made with the diode in the "ON" state. The power dissipated by the DH0035 is limited to 1.5W (see Table I). The DH0035 dissipates the maximum power with Q_5 "ON". With Q_5 "OFF", negligible power is dissipated by the device. Power dissipation is given by:

$$P\,diss \cong \left[I_{DC}(|V^-| - \Delta V) + \frac{(V^+ - V^-)^2}{R3}\right] \times (D.C.) \leq P_{max} \quad (12)$$

where: D.C. = Duty Cycle =

$$\frac{(\text{"ON" time})}{(\text{"ON" time} + \text{"OFF" time})}$$

Pmax = 1.5W

In terms of I_{DC}:

$$I_{DC} \leq \frac{\left[\frac{(Pmax)}{(D.C.)} - \frac{(V^+ - V^-)^2}{500}\right]}{|V^-| - \Delta V} \quad (12a)$$

For the circuit of *Figure 5* and a 50% duty cycle, P diss = 0.5W.

Turn-off of the PIN diode begins when the Q output of the DM8830 returns to logic "0" and the $\overline{Q}$ output goes to logic "1". Q_2 turns "ON", and in turn, causes Q_3 to saturate. Simultaneously, Q_1 is turned "OFF" stopping the base drive to Q_5. Q_3 absorbs the stored base charge of Q_5 facilitating its rapid turn-off. As Q_5's collector begins to rise, Q_4 turns "ON". At this instant, the PIN diode is still in conduction and the emitter of Q_4 is held at approximately −0.7V. The instantaneous current available to clear stored charge out of the PIN diode is:

$$Ipk = \frac{V^+ - V_{BE\,Q4} + V_{f(PIN)}}{\frac{R3}{h_{fe} + 1}} \cong \frac{(h_{fe} + 1)(V^+)}{R_3} \quad (13)$$

where:

h_{fe} + 1 = current gain of Q_4 = 20

$V_{BE\,Q4}$ = base-emitter drop of Q_4 = 0.7V

$V_{f(PIN)}$ = forward drop of the PIN diode = 0.7V

For typical values given, Ipk = 400 mA. Increasing V^+ above 10V will improve turn-off time of the diode, but at the expense of power dissipation in the DH0035. Once turn-off of the diode has been achieved, the DH0035 output current drops to the reverse leakage of the PIN diode. The attendant power dissipation is reduced to about 35 mW.

CATHODE GROUND DESIGN

Figure 6 shows the DH0035 driving a cathode grounded PIN diode switch. The peak turn-on current is given by:

$$Ipk \cong \frac{(V^+ - V^-)(h_{fe} + 1)}{R3} \quad (14)$$

= 800 mA for the values shown.

The steady state current, I_{DC}, is set by Rp and is given by:

$$I_{DC} = \frac{(V^+ - 2V_{BE}}{\frac{R3}{h_{fe} + 1} + R_P} \quad (15)$$

where: $2V_{BE}$ = forward drop of Q_4 base emitter junction plus V_f of the PIN diode = 1.4V.

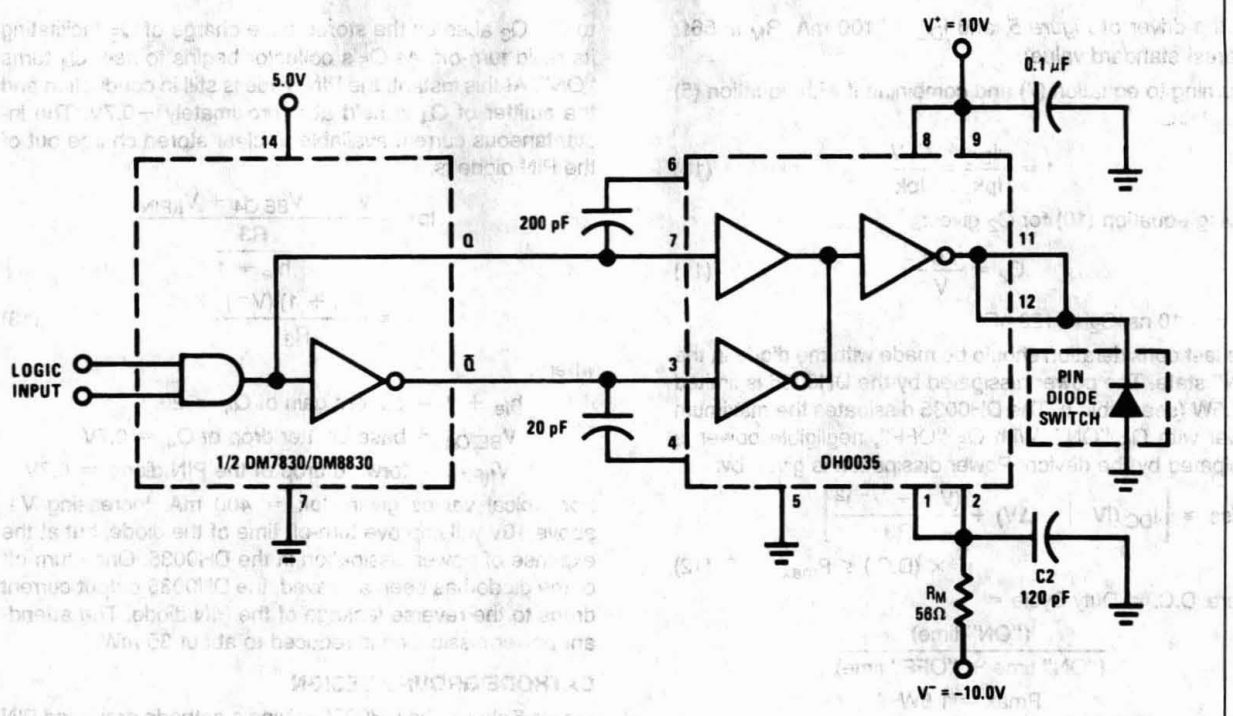

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FIGURE 6. Anode Grounded Driver

In terms of Rp, equation (15) becomes:

$$Rp = \frac{(h_{fe} + 1)(V^+ - 2V_{BE}) - I_{DC}R_9}{(h_{fe} + 1)\, I_{DC}} \qquad (15a)$$

For the circuit of *Figure 6,* and I_{DC} = 100 mA, Rp is 62Ω (nearest standard value).

It now remains to select the value of C_1. To do this, the change in voltage across C_1 must be evaluated. In the "ON" state, the voltage across C_1, Vc, is given by:

$$(Vc)_{ON} = \frac{V^+R_3 + Rp(h_{fe} + 1)(2V_{BE})}{R_3 + (h_{fe} + 1)\, Rp} \qquad (16)$$

For the values indicated above, $(Vc)_{ON}$ = 3.8V.

In the "OFF" state, Vc is given by:

$$(Vc)_{OFF} = \frac{V^+R_3 - |V^-|Rp}{Rp + R_3} \qquad (17)$$

= 8.0V for the circuit of *Figure 6.*

Hence, the change in voltage across C_1 is:

$$V = (Vc)_{OFF} - (Vc)_{ON} \qquad (18)$$
$$= 8.0 - 3.8$$
$$= 4.2V$$

The value of C_4 is given, as before, by equation (11):

$$C_1 = \frac{I_{DC}\tau}{V^-} \qquad (19)$$

For a diode with τ = 10 ns and I_{DC} = 100 mA, C_1 = 250 pF.

Again the power dissipated by the DH0035 must be considered. In the "OFF" state, the power dissipation is given by:

$$P_{OFF} = \left[\frac{V^+ - V^-)^2}{R_3}\right] (D.C.) \qquad (20)$$

where: D.C. = duty cycle =

$$\frac{\text{"OFF" time}}{\text{"OFF" time} + \text{"ON" time}}$$

The "ON" power dissipation is given by:

$$P_{ON} = \left[\frac{(Vc)_{ON}^2}{R_3} + I_{DC} \times (Vc)_{ON}\right](1 - D.C.) \qquad (21)$$

where: $(Vc)_{ON}$ is defined by equation (16).

Total power dissipated by the DH0035 is simply P_{ON} + P_{OFF}. For a 50% duty cycle and the circuit of *Figure 6,* P diss = 616 mW.

The peak turn-off current is, as indicated earlier, equal to 50 mA × h_{fe} which is about 1000 mA. Once the excess stored charge is removed, the current through Q_5 drops to the diodes leakage current. Reverse bias across the diode = $V^- - V_{sat} \cong -10V$ for the circuit of *Figure 6.*

REPETITION RATE CONSIDERATIONS

Although ignored until now, the PRF, in particular, the "OFF" time of the PIN diode is important in selection of C_2, R_M, and C_1, Rp. The capacitors must recharge completely during the diode "OFF" time. In short:

$$4\, R_MC_2 \le t_{OFF} \qquad (22a)$$
$$4\, RpC_1 \le t_{OFF} \qquad (22b)$$

CONCLUSION

The circuit of *Figure 6* was breadboarded and tested in conjunction with a Hewlett-Packard 33622A PIN diode.

I_{DC} was set at 100 mA, $V^+ = 10V$, $V^- = 10V$. Input signal to the DM8830 was a 5V peak, 100 kHz, 5 μs wide pulse train. RF turn-on was accomplished in 10–12 ns while turn-off took approximately 5 ns, as shown in *Figures 7* and *8*.

In practice, adjustment C_2 (C_1) may be required to accommodate the particular PIN diode minority carrier lifetime.

SUMMARY

A unique circuit utilized in the driving of PIN diodes has been presented. Further a technique has been demonstrated which enables the designer to tailor the DH0035 driver to the PIN diode application.

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1.2V Reference

National Semiconductor
Application Note 56

INTRODUCTION

Temperature compensated zener diodes are the most easily used voltage reference. However, the lowest voltage temperature-compensated zener is 6.2V. This makes it inconvenient to obtain a zero temperature-coefficient reference when the operating supply voltage is 6V or lower. With the availability of the LM113, this problem no longer exists.

The LM113 is a 1.2V temperature compensated shunt regulator diode. The reference is synthesized using transistors and resistors rather than a breakdown mechanism. It provides extremely tight regulation over a wide range of operating currents in addition to unusually low breakdown voltage and low temperature coefficient.

DESIGN CONCEPTS

The reference in the LM113 is developed from the highly-predictable emitter-base voltage of integrated transistors. In its simplest form, the voltage is equal to the energy-band-gap voltage of the semiconductor material. For silicon, this is 1.205V. Further, the output voltage is well determined in a production environment.

A simplified version of this reference[1] is shown in *Figure 1*. In this circuit, Q_1 is operated at a relatively high current density. The current density of Q_2 is about ten times lower, and the emitter-base voltage differential (ΔV_{BE}) between the two devices appears across R_3. If the transistors have high current gains, the voltage across R_2 will also be proportional to ΔV_{BE}. Q_3 is a gain stage that will regulate the output at a voltage equal to its emitter base voltage plus the drop across R_2. The emitter base voltage of Q_3 has a negative temperature coefficient while the ΔV_{BE} component across R_2 has a positive temperature coefficient. It will be shown that the output voltage will be temperature compensated when the sum of the two voltages is equal to the energy-band-gap voltage.

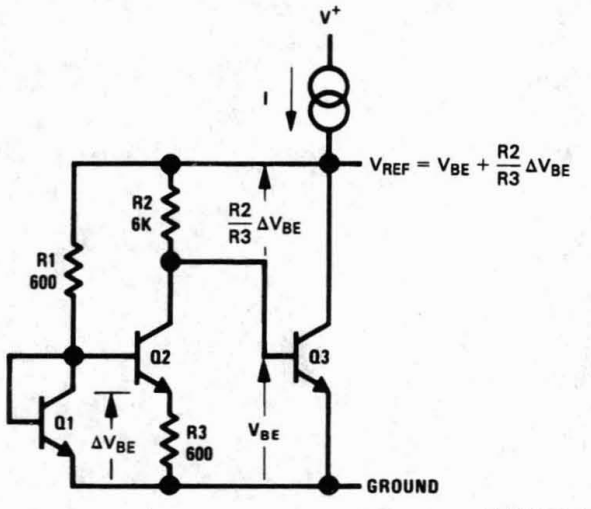

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FIGURE 1. The Low Voltage Reference in One of Its Simpler Forms

Conditions for temperature compensation can be derived starting with the equation for the emitter-base voltage of a transistor which is[2]

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{nkT}{q}\log_e\frac{T_0}{T} + \frac{kT}{q}\log_e\frac{I_C}{I_{C0}}, \quad (1)$$

where V_{g0} is the extrapolated energy-band-gap voltage for the semiconductor material at absolute zero, q is the charge of an electron, n is a constant which depends on how the transistor is made (approximately 1.5 for double-diffused, NPN transistors), k is Boltzmann's constant, T is absolute temperature, I_C is collector current and V_{BE0} is the emitter-base voltage at T_0 and I_{C0}.

The emitter-base voltage differential between two transistors operated at different current densities is given by

$$\Delta V_{BE} = \frac{kT}{q}\log_e\frac{J_1}{J_2} \quad (2)$$

where J is current density.

Referring to Equation (1), the last two terms are quite small and are made even smaller by making I_C vary as absolute temperature. At any rate, they can be ignored for now because they are of the same order as errors caused by non-theoretical behavior of the transistors that must be determined empirically.

If the reference is composed of V_{BE} plus a voltage proportional to ΔV_{BE}, the output voltage is obtained by adding (1) in its simplified form to (2):

$$V_{ref} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{kT}{q}\log_e\frac{J_1}{J_2}. \quad (3)$$

Differentiating with respect to temperature yields

$$\frac{\partial V_{ref}}{\partial T} = -\frac{V_{g0}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{k}{q}\log_e\frac{J_1}{J_2}. \quad (4)$$

For zero temperature drift, this quantity should equal zero, giving

$$V_{g0} = V_{BE0} + \frac{kT_0}{q}\log_e\frac{J_1}{J_2}. \quad (5)$$

The first term on the right is the initial emitter-base voltage while the second is the component proportional to emitter-base voltage differential. Hence, if the sum of the two are equal to the energy-band-gap voltage of the semiconductor, the reference will be temperature-compensated.

Figure 2 shows the actual circuit of the LM113. Q_1 and Q_2 provide the ΔV_{BE} term and Q_4 provides the V_{BE} term as in the simplified circuit. The additional transistors are used to decrease the dynamic resistance, improving the regulation of the reference against current changes. Q_3 in conjunction with current inverter, Q_5 and Q_6, provide a current source load for Q_4 to achieve high gain.

Q_7 and Q_9 buffer Q_4 against changes in operating current and give the reference a very low output resistance. Q_8 sets the minimum operating current of Q_7 and absorbs any leak-

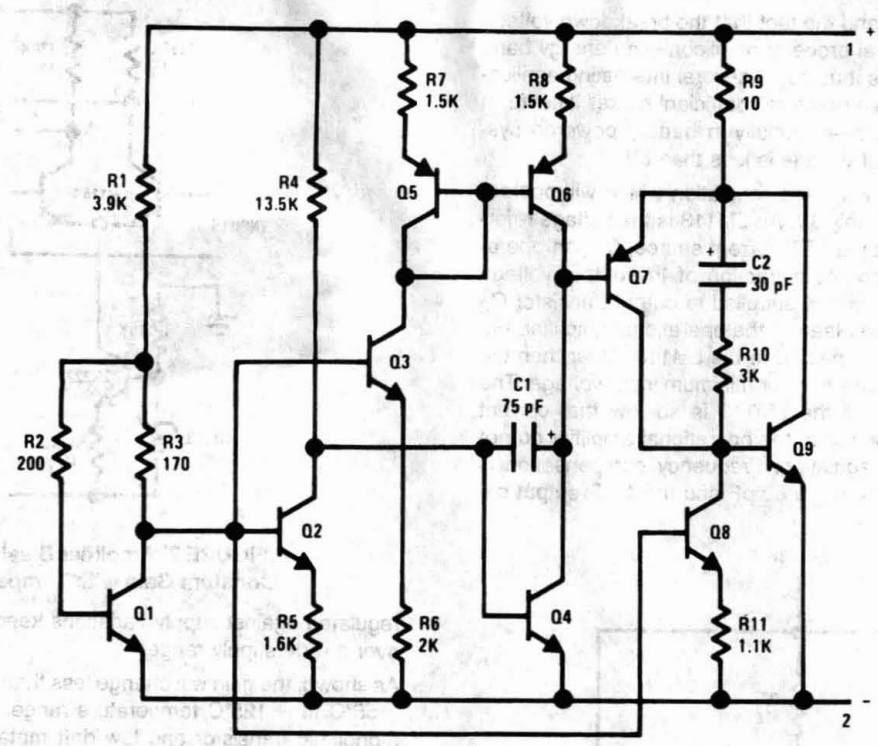

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FIGURE 2. Schematic of the LM113

age from Q_9. Capacitors C_1, C_2 and resistors R_9 and R_{10} frequency compensate the regulator diode.

PERFORMANCE

The most important features of the regulator diode are its good temperature stability and low dynamic resistance. *Figure 3* shows the typical change in output voltage over a −55°C to +125°C temperature range. The reference voltage changes less than 0.5% with temperature, and the temperature coefficient is relatively independent of operating current.

Figure 4 shows the output voltage change with operating current. From 0.5 mA to 20 mA there is only 6 mV of change. A good portion of the output change is due to the resistance of the aluminum bonding wires and the Kovar leads on the package. At currents below about 0.3 mA the diode no longer regulates. This is because there is insufficient current to bias the internal transistors into their active region. *Figure 5* illustrates the breakdown characteristic of the diode.

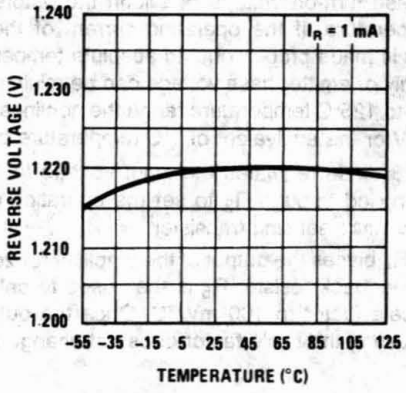

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FIGURE 3. Output Voltage Change with Temperature

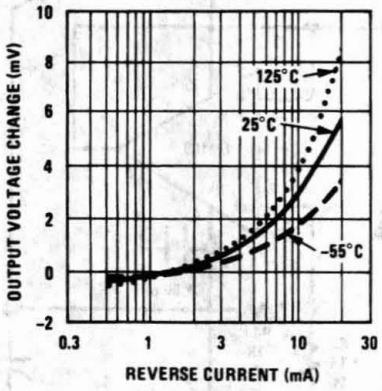

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FIGURE 4. Output Voltage Change with Current

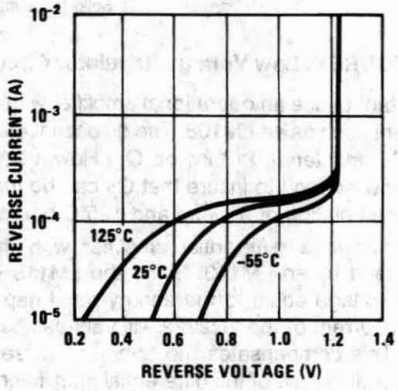

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FIGURE 5. Reverse Breakdown Characteristics

APPLICATIONS

The applications for zener diodes are so numerous that no attempt to delineate them will be made. However, the low

breakdown voltage and the fact that the breakdown voltage is equal to a physical property of silicon—the energy band gap voltage—makes it useful in several interesting applications. Also the low temperature coefficient makes it useful in regulator applications—especially in battery powered systems where the input voltage is less than 6V.

Figure 6 shows a 2V voltage regulation which will operate on input voltages of only 3V. An LM113 is the voltage reference and is driven by a FET current source, Q_1. An operational amplifier compares a fraction of the output voltage with the reference. Drive is supplied to output transistor Q_2 through the V^+ power lead of the operational amplifier. Pin 6 of the op amp is connected to the LM113 rather than the output since this allows a lower minimum input voltage. The dynamic resistance of the LM113 is so low that current changes from the output of the operational amplifier do not appreciably affect regulation. Frequency compensation is accomplished with both the 50 pF and the 1 μF output capacitor.

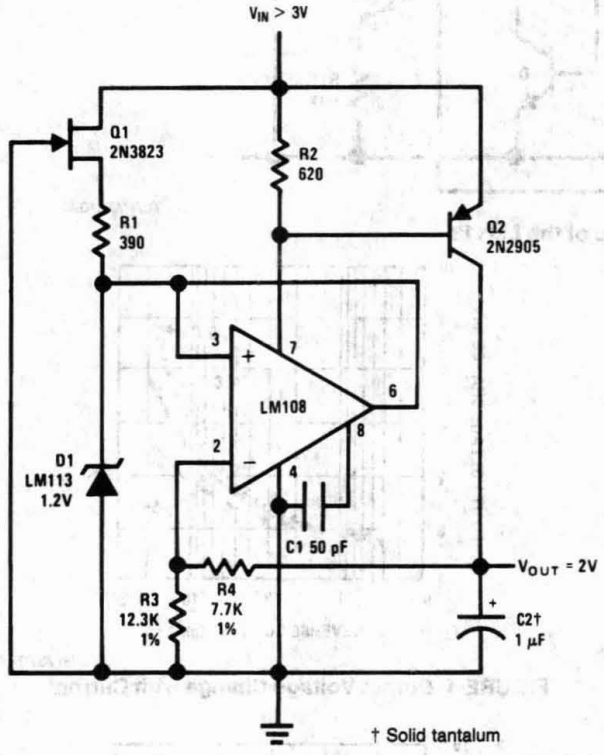

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FIGURE 6. Low Voltage Regulator Circuit

It is important to use an operational amplifier with low quiescent current such as an LM108. The quiescent current flows through R_2 and tends to turn on Q_2. However, the value shown is low enough to insure that Q_2 can be turned off at worst case condition of no load and 125°C operation.

Figure 7 shows a differential amplifier with the current source biased by an LM113. Since the LM113 supplies a reference voltage equal to the energy band gap of silicon, the output current of the 2N2222 will vary as absolute temperature. This compensates the temperature sensitivity of the transconductance of the differential amplifier making the gain temperature stable. Further, the operating current is

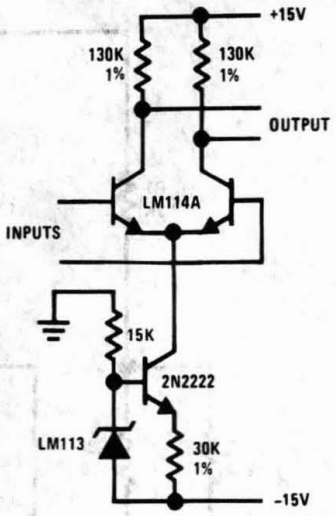

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FIGURE 7. Amplifier Biasing for Constant Gain with Temperature

regulated against supply variations keeping the gain stable over a wide supply range.

As shown, the gain will change less than two per cent over a −55°C to +125°C temperature range. Using the LM114A monolithic transistor and low drift metal film resistors, the amplifier will have less than 2 μV/°C voltage drift. Even lower drift may be obtained by unbalancing the collector load resistors to null out the initial offset. Drift under nulled condition will be typically less than 0.5 μV/°C.

The differential amplifier may be used as a pre-amplifier for a low-cost operational amplifier such as an LM101A to improve its voltage drift characteristics. Since the gain of the operational amplifier is increased by a factor of 100, the frequency compensation capacitor must also be increased from 30 pF to 3000 pF for unity gain operation. To realize low voltage drift, case must be taken to minimize thermoelectric potentials due to temperature gradients. For example, the thermoelectric potential of some resistors may be more than 30 μV/°C, so a 1°C temperature gradient across the resistor on a circuit board will cause much larger errors than the amplifier drift alone. Wirewound resistors such as Evenohm are a good choice for low thermoelectric potential.

Figure 8 illustrates an electronic thermometer using an inexpensive silicon transistor as the temperature sensor. It can provide better than 1°C accuracy over a 100°C range. The emitter-base turn-on voltage of silicon transistors is linear with temperature. If the operating current of the sensing transistor is made proportional to absolute temperature the nonlinearily of emitter-base voltage can be minimized. Over a −55°C to 125°C temperature range the nonlinearily is less than 2 mV or the equivalent of 1°C temperature change.

An LM113 diode regulates the input voltage to 1.2V. The 1.2V is applied through R_2 to set the operating current of the temperature-sensing transistor.

Resistor R_4 biases the output of the amplifier for zero output at 0°C. Feedback resistor R_5 is then used to calibrate the output scale factor to 100 mV/°C. Once the output is zeroed, adjusting the scale factor does not change the zero.

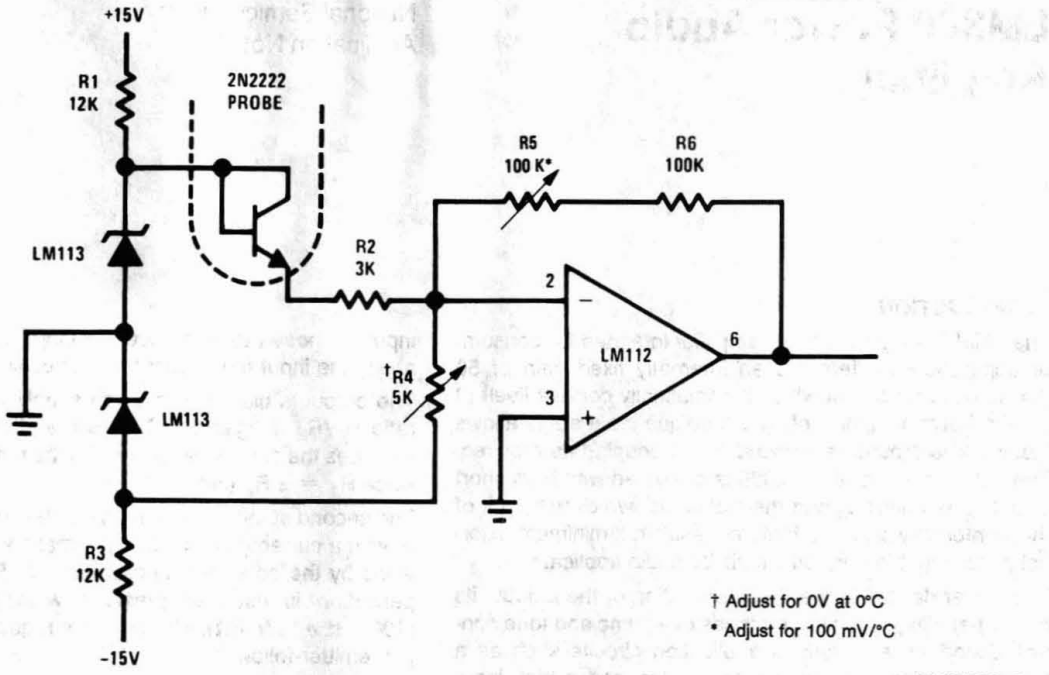

FIGURE 8. Electronic Thermometer

CONCLUSION

A new two terminal low voltage shunt regulator has been described. It is electrically equivalent to a temperature-stable 1.2V breakdown diode. Over a −55°C to 125°C temperature range and operating currents of 0.5 mA to 20 mA the LM113 has one hundred times better reverse characteristics than breakdown diode. Addiitionally, wideband noise and long term stability are good since no breakdown mechanism is involved.

The low temperature coefficient and low regulation voltage make it especially suitable for a low voltage regulator or battery operated equipment. Circuit design is eased by the fact that the output voltage and temperature coefficient are largely independent of operating current. Since the reference voltage is equal to the extrapolated energy-band-gap of silicon, the device is useful in many temperature compensation and temperature measurement applications.

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LM380 Power Audio Amplifier

National Semiconductor
Application Note 69

INTRODUCTION

The LM380 is a power audio amplifier intended for consumer applications. It features an internally fixed gain of 50 (34 dB) and an output which automatically centers itself at one-half of the supply voltage. A unique input stage allows inputs to be ground referenced or AC coupled as required. The output stage of the LM380 is protected with both short circuit current limiting and thermal shutdown circuitry. All of these internally provided features result in a minimum external parts count integrated circuit for audio applications.

This paper describes the circuit operation of the LM380, its power handling capability, methods of volume and tone control, distortion, and various application circuits such as a bridge amplifier, a power supply splitter, and a high input impedance audio amplifier.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified circuit schematic of the LM380. The input stage is a PNP emitter-follower driving a PNP differential pair with a slave current-source load. The PNP input is chosen to reference the input to ground, thus enabling the input transducer to be directly coupled.

The output is biased to half the supply voltage by resistor ratio R_1/R_2. Negative DC feedback, through resistor R_2, balances the differential stage with the output at half supply, since $R_1 = 2\,R_2$ (*Figure 1*).

The second stage is a common emitter voltage gain amplifier with a current-source load. Internal compensation is provided by the pole-splitting capacitor C′. Pole-splitting compensation is used to preserve wide power bandwidth (100 kHz at 2W, 8Ω). The output is a quasi-complementary pair emitter-follower.

The amplifier gain is internally fixed to 34 dB or 50. This is accomplished by the internal feedback network R_2–R_3. The gain is twice that of the ratio R_2/R_3 due to the slave current-source which provides the full differential gain of the input stage.

TABLE I. Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Power Output (rms)	8Ω loads, 3% T.H.D. (Notes 3,4)	2.5			Wrms
Gain		40	50	60	V/V
Output Voltage Swing	8Ω load		14		$V_{p\text{-}p}$
Input Resistance			150k		Ω
Total Harmonic Distortion	P_O = 1W, (Notes 4 & 5)		0.2		%
Power Supply Rejection	C_{bypass} = 5 μF, † = 120 Hz (Note 2)		38		dB
Supply Voltage Range		8		22	V
Bandwidth	P_O = 2W, R_L = 8Ω		100k		Hz
Quiescent Output Voltage		8	9	10	V
Quiescent Supply Current			7	25	mA
Short Circuit Current			1.3		A

Note 1: V_S = 18V; T_A = 25°C unless otherwise specified.

Note 2: Rejection ratio referred to output.

Note 3: With device Pins 3, 4, 5, 10, 11, 12 soldered into a 1/16" epoxy glass board with 2 ounce copper foil with a minimum surface of six square inches.

Note 4: If oscillation exists under some load conditions, add a 2.7Ω resistor and 0.1 μF series network from Pin 8 to ground.

Note 5: C_{bypass} = 0.47 μF on Pin 1.

Note 6: Pins 3, 4, 5, 10, 11, 12 at 50°C derates 25°C/W above 50°C case.

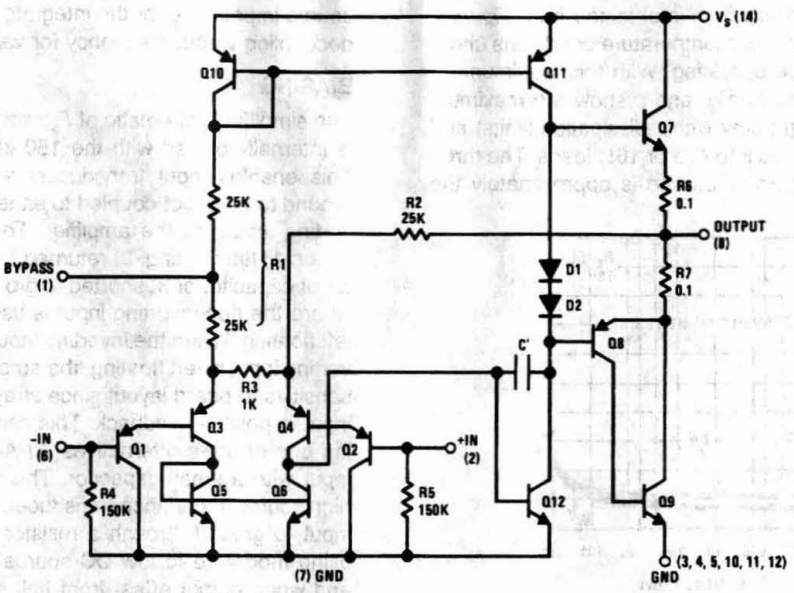

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FIGURE 1

GENERAL OPERATING CHARACTERISTICS

The output current of the LM380 is rated at 1.3A peak. The 14 pin dual-in-line package is rated at 35°C/W when soldered into a printed circuit board with 6 square inches of 2 ounce copper foil (*Figure 2*). Since the device junction temperature is limited to 150°C via the thermal shutdown circuitry, the package will support 3 watts dissipation at 50°C ambient or 3.7 watts at 25°C ambient.

Figure 2 shows the maximum package dissipation versus ambient temperature for various amounts of heat sinking.

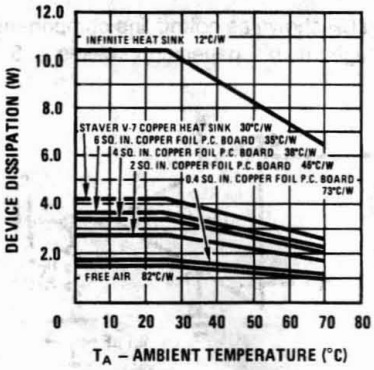
DEVICE DISSIPATION (W)
INFINITE HEAT SINK 12°C/W
STAVER V-7 COPPER HEAT SINK 30°C/W
6 SQ. IN. COPPER FOIL P.C. BOARD 35°C/W
4 SQ. IN. COPPER FOIL P.C. BOARD 38°C/W
2 SQ. IN. COPPER FOIL P.C. BOARD 46°C/W
0.4 SQ. IN. COPPER FOIL P.C. BOARD 73°C/W
FREE AIR 82°C/W
T_A – AMBIENT TEMPERATURE (°C)

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FIGURE 2. Device Dissipation vs Ambient Temperature

Figures 3a, b, and *c* show device dissipation versus output power for various supply voltages and loads.

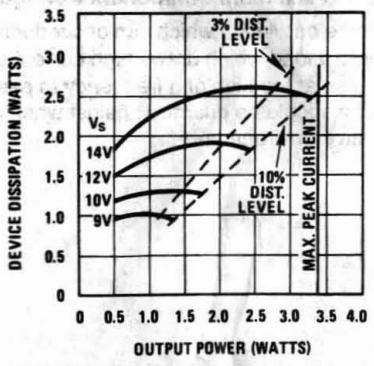

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FIGURE 3a. Device Dissipation vs Output Power — 4Ω Load

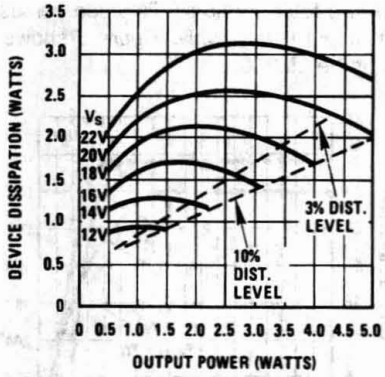

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FIGURE 3b. Device Dissipation vs Output Power — 8Ω Load

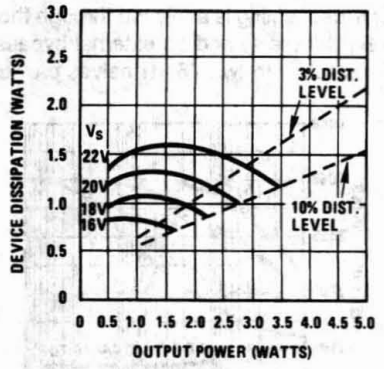

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FIGURE 3c. Device Dissipation vs Output Power — 16Ω Load

The maximum device dissipation is obtained from *Figure 2* for the heat sink and ambient temperature conditions under which the device will be operating. With this maximum allowed dissipation, *Figures 3a, b* and *c* show the maximum power supply allowed (to stay within dissipation limits) and the output power delivered into 4, 8 or 16Ω loads. The three percent total-harmonic distortion line is approximately the on-set of clipping.

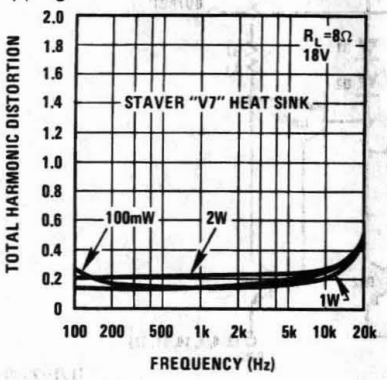

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FIGURE 4. Total Harmonic Distortion vs Frequency

Figure 4 shows total harmonic distortion versus frequency for various output levels, while *Figure 5* shows the power bandwidth of the LM380.

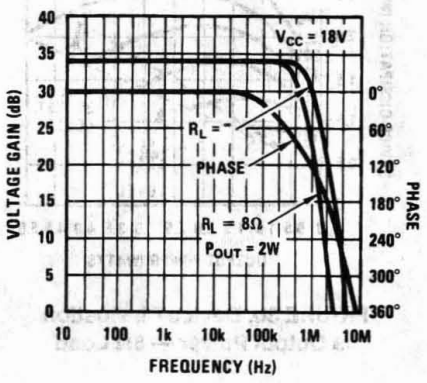

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FIGURE 5. Output Voltage Gain vs Frequency

Power supply decoupling is achieved through the AC divider formed by R_1 (Figure 1) and an external bypass capacitor. Resistor R_1 is split into two 25 kΩ halves providing a high

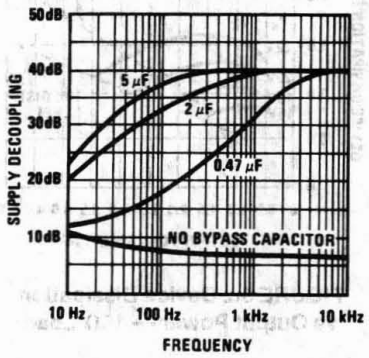

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FIGURE 6. Supply Decoupling vs Frequency

source impedance for the integrator. *Figure 6* shows supply decoupling versus frequency for various bypass capacitors.

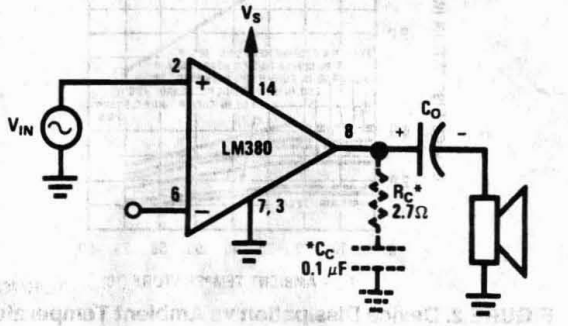
BIASING

The simplified schematic of *Figure 1* shows that the LM380 is internally biased with the 150 kΩ resistance to ground. This enables input transducers which are referenced to ground to be direct-coupled to either the inverting or non-inverting inputs of the amplifier. The unused input may be either: 1) left floating, 2) returned to ground through a resistor or capacitor or 3) shorted to ground. In most applications where the non-inverting input is used, the inverting input is left floating. When the inverting input is used and the non-inverting input is left floating, the amplifier may be found to be sensitive to board layout since stray coupling to the floating input is positive feedback. This can be avoided by employing one of three alternatives: 1) AC grounding the unused input with a small capacitor. This is preferred when using high source impedance transducer. 2) Returning the unused input to ground through a resistor. This is preferred when using moderate to low DC source impedance transducers and when output offset from half supply voltage is critical. The resistor is made equal to the resistance of the input transducer, thus maintaining balance in the input differential amplifier and minimizing output offset. 3) Shorting the unused input to ground. This is used with low DC source impedance transducers or when output offset voltage is non-critical.

OSCILLATION

The normal power supply decoupling precautions should be taken when installing the LM380. If V_S is more than 2″ to 3″ from the power supply filter capacitor it should be decoupled with a 0.1 μF disc ceramic capacitor at the V_S terminal of the IC.

The R_C and C_C shown as dotted line components on *Figure 7* and throughout this paper suppresses a 5 to 10 MHz



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*For Stability With High Current Loads

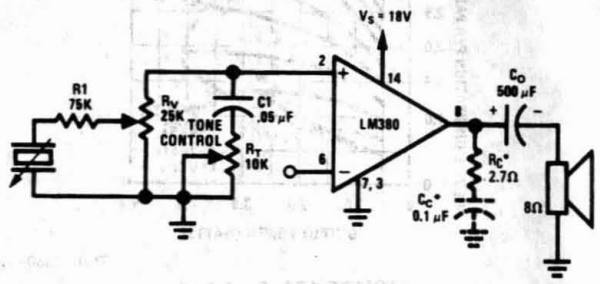
FIGURE 7. Minimum Component Configuration

small amplitude oscillation which can occur during the negative swing into a load which draws high current. The oscillation is of course at too high of a frequency to pass through a speaker, but it should be guarded against when operating in an RF sensitive environment.

APPLICATIONS

With the internal biasing and compensation of the LM380, the simplest and most basic circuit configuration requires only an output coupling capacitor as seen in *Figure 7*.

An application of this basic configuration is the phonograph amplifier where the addition of volume and tone controls is required. *Figure 8* shows the LM380 with a voltage divider volume control and high frequency roll-off tone control.



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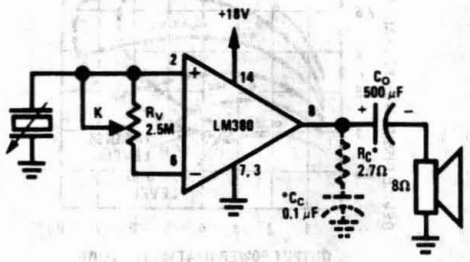
*For Stability with High Current Loads

FIGURE 8. Phono Amp

When maximum input impedance is required or the signal attenuation of the voltage divider volume control is undesirable, a "common mode" volume control may be used as seen in *Figure 9*.



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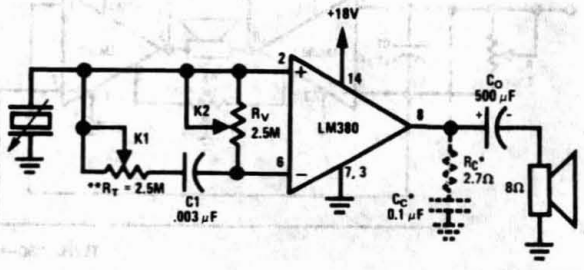
*For Stability with High Current Loads

FIGURE 9. "Common Mode" Volume Control

With this volume control the source loading impedance is only the input impedance of the amplifier when in the full-volume position. This reduces to one-half the amplifier input impedance at the zero volume position. Equation 1 describes the output voltage as a function of the potentiometer setting.

$$V_{OUT} = 50\,V_{IN}\left(1 - \frac{150 \times 10^3}{k_1 R_V + 150 \times 10^3}\right)_{0 \le k_1 \le 1} \quad (1)$$



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*For Stability with High Current Loads

**Audio Tape Potentiometer (10% of R_T at 50% Rotation)

FIGURE 10. "Common Mode" Volume and Tone Control

This "common mode" volume control can be combined with a "common mode" tone control as seen in *Figure 10*.

This circuit has a distinct advantage over the circuit of *Figure 7* when transducers of high source impedance are used, in that, the full input impedance of the amplifier is realized. It also has an advantage with transducers of low source impedance since the signal attenuation of the input voltage divider is eliminated. The transfer function of the circuit of *Figure 10* is given by:

$$\frac{V_{OUT}}{V_{IN}} = 50\left(1 - \frac{150k}{150k + \dfrac{k_1 R_T k_2 R_V + \dfrac{k_2 R_V}{j2\pi f c_1}}{k_1 R_T + k_2 R_V + \dfrac{1}{j2\pi f c_1}}}\right)_{\substack{0 \le k_1 \le 1 \\ 0 \le k_2 \le 1}} \quad (2)$$

Figure 11 shows the response of the circuit of *Figure 10*.

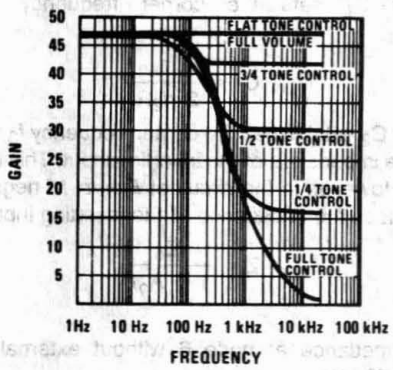

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FIGURE 11. Tone Control Response

Most phonograph applications require frequency response shaping to provide the RIAA equalization characteristic. When recording, the low frequencies are attenuated to prevent large undulations from destroying the record groove walls. (Bass tones have higher energy content than high frequency tones). Conversely, the high frequencies are emphasized to achieve greater signal-to-noise ratio. Therefore, when played back the phono amplifier should have the inverse frequency response as shown in *Figure 12*.

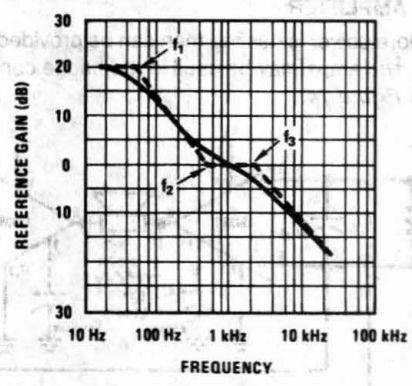

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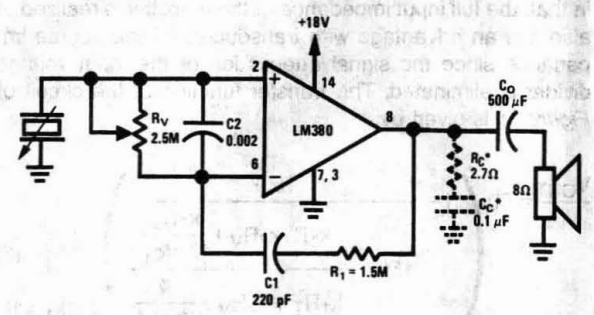
FIGURE 12. RIAA Playback Equalization

This response is achieved with the circuit of *Figure 13*.

The mid-band gain, between frequencies f_2 and f_3, *Figure 12*, is established by the ratio of R_1 to the input resistance of the amplifier (150 kΩ).

$$\text{Mid-band Gain} = \frac{R_1 + 150\ k\Omega}{150\ k\Omega} \quad (3)$$



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* For Stability with High Current Loads

FIGURE 13. RIAA Phono Amplifier

Capacitor C_1 sets the corner frequency f_2 where $R_1 = X_{C1}$.

$$C_1 = \frac{1}{2\pi f_2 R_1} \quad (4)$$

Capacitor C_2 establishes the corner frequency f_3 where X_{C2} equals the impedance of the inverting input. This is normally 150 kΩ. However, in the circuit of *Figure 13* negative feedback reduces the impedance at the inverting input as:

$$Z = \frac{Z_o}{1 + A_o\beta} \quad (5)$$

Where:

Z_o = impedance at node 6 without external feedback (150 kΩ)

A_o = gain without external feedback (50)

β = feedback transfer function $\beta = \dfrac{A_o - A}{A_o A}$

A = closed loop gain with external feedback.

Therefore

$$C_2 = \frac{1}{2\pi f_3 \left(\dfrac{Z_o}{1 + A_o\beta}\right)} = \frac{1}{2\pi f_3 \left(\dfrac{150k}{1 + 50\beta}\right)} \quad (6)$$

BRIDGE AMPLIFIER

Where more power is desired than can be provided with one amplifier, two amps may be used in the bridge configuration shown in *Figure 14*.

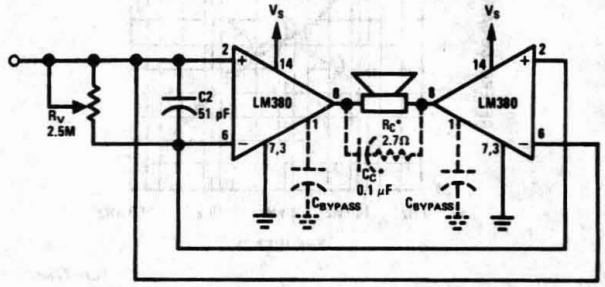

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FIGURE 14. Bridge Configuration

This provides twice the voltage swing across the load for a given supply, thereby, increasing the power capability by a factor of four over the single amplifier. However, in most cases the package dissipation will be the first parameter limiting power delivered to the load. When this is the case, the power capability of the bridge will be only twice that of the single amplifier. *Figures 15A* and *B* show output power versus device package dissipation for both 8 and 16Ω loads in the bridge configuration. The 3% and 10% harmonic distortion contours double back due to the thermal limiting of the LM380. Different amounts of heat sinking will change the point at which the distortion contours bend.

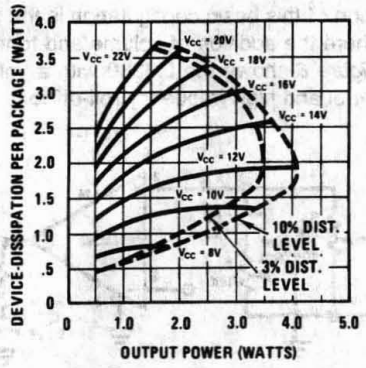

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FIGURE 15A. 8Ω Load

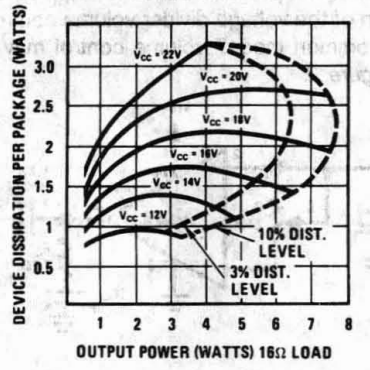

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FIGURE 15B. 16Ω Load

The quiescent output voltage of the LM380 is specified at 9 ± 1 volts with an 18 volt supply. Therefore, under the worst case condition, it is possible to have two volts DC across the load.

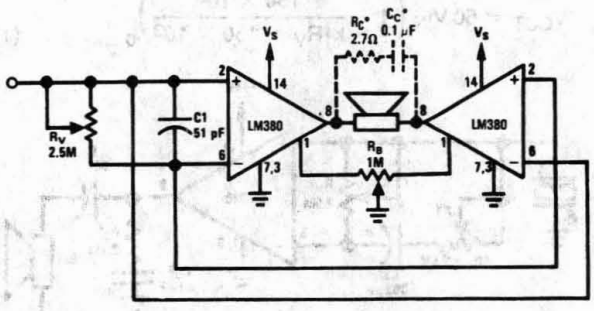

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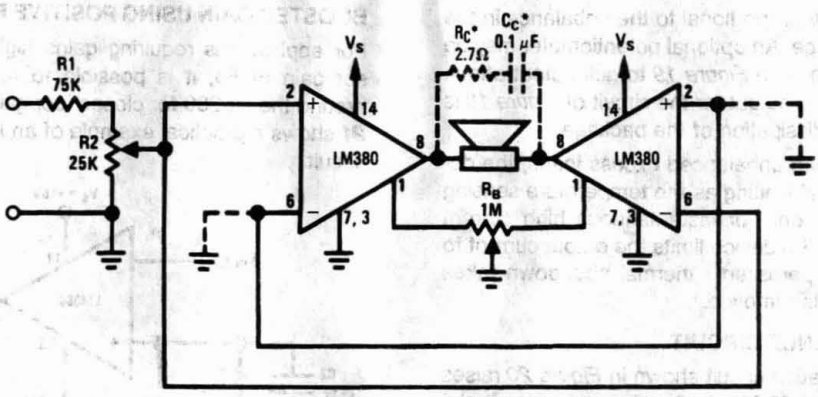
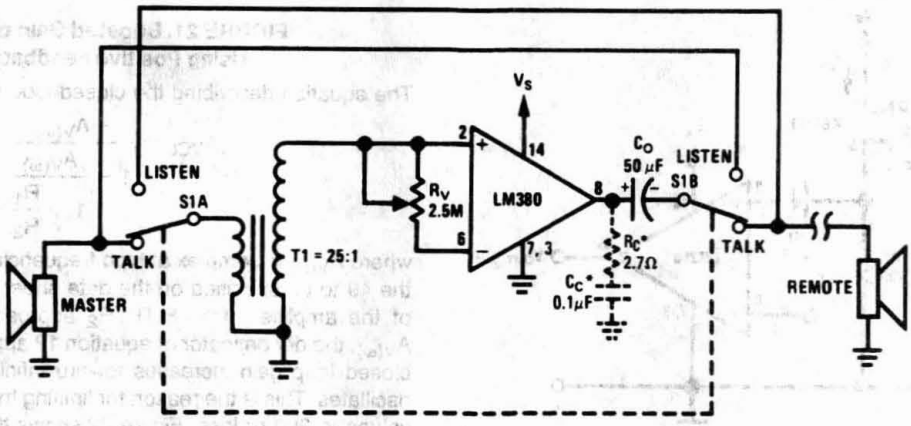
FIGURE 16. Quiescent Balance Control

With an 8Ω speaker this 0.25A which may be excessive. Three alternatives are available; 1) care can be taken to match the quiescent voltages, 2) a non-polar capacitor may be placed in series with the load, 3) the offset balance control of *Figure 16* may be used.



*For Stability with High Current Loads

FIGURE 17. Voltage Divider Input



*For Stability with High Current Loads

FIGURE 18. Intercom

The circuits of *Figures 14* and *16* employ the "common mode" volume control as shown before. However, any of the various input connection schemes discussed previously may be used. *Figure 17* shows the bridge configuration with the voltage divider input. As discussed in the "Biasing" section the undriven input may be AC or DC grounded. If V_S is an appreciable distance from the power supply (>3") filter capacitor it should be decoupled with a 1 μF tantaulum capacitor.

INTERCOM

The circuit of *Figure 18* provides a minimum component intercom. With switch S_1 in the talk position, the speaker of the master station acts as the microphone with the aid of step-up transformer T_1.

A turns ratio of 25 and a device gain of 50 allows a maximum loop gain of 1250. R_V provides a "common mode" volume control. Switching S_1 to the listen position reverses the role of the master and remote speakers.

LOW COST DUAL SUPPLY

The circuit shown in *Figure 19* demonstrates a minimum parts count method of symmetrically splitting a supply voltage. Unlike the normal R, C, and power zener diode technique the LM380 circuit does not require a high standby current and power dissipation to maintain regulation.

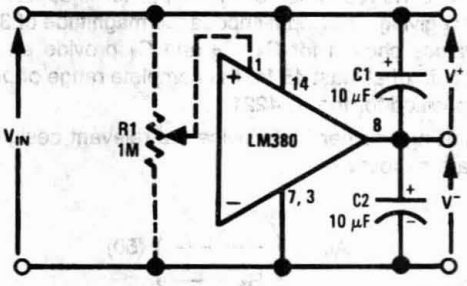


FIGURE 19. Dual Supply

With a 20 volt input voltage (±10 volt output) the circuit exhibits a change in output voltage of approximately 2% per 100 mA of unbalanced load change. Any balanced load change will reflect only the regulation of the source voltage V_{IN}.

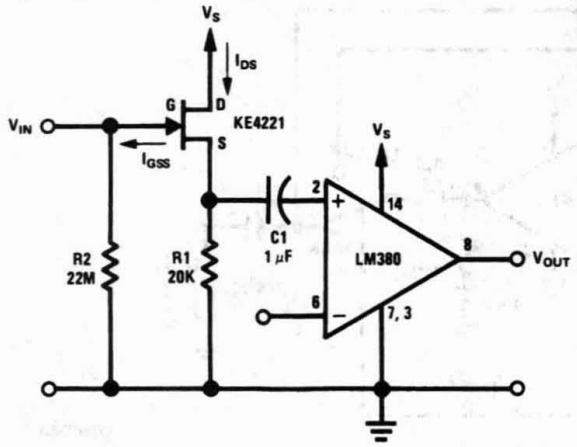
The theoretical plus and minus output tracking ability is 100% since the device will provide an output voltage at one-half of the instantaneous supply voltage in the absence of a capacitor on the bypass terminal. The actual error in

tracking will be directly proportional to the unbalance in the quiescent output voltage. An optional potentiometer may be placed at pin 1 as shown in *Figure 19* to null output offset. The unbalanced current output for the circuit of *Figure 18* is limited by the power dissipation of the package.

In the case of sustained unbalanced excess loads, the device will go into thermal limiting as the temperature sensing circuit begins to function. For instantaneous high current loads or short circuits the device limits the output current to approximately 1.3 amperes until thermal shut-down takes over or until the fault is removed.

HIGH INPUT IMPEDANCE CIRCUIT

The junction FET isolation circuit shown in *Figure 20* raises the input impedance to 22 MΩ for low frequency input signals. The gate to drain capacitance (2 pF maximum for the KE4221 shown) of the FET limits the input impedance as frequency increases.



TL/H/7380–23

FIGURE 20

At 20 kHz the reactance of this capacitor is approximately −j4 MΩ giving a net input impedance magnitude of 3.9 MΩ. The values chosen for R_1, R_2 and C_1 provide an overall circuit gain of at least 45 for the complete range of parameters specified for the KE4221.

When using another FET device the relevant design equations are as follows:

$$A_V = \left(\frac{R_1}{R_1 + \frac{1}{g_m}}\right)(50) \tag{7}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right) \tag{8}$$

$$V_{GS} = I_{DS}R_1 \tag{9}$$

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{10}$$

The maximum value of R_2 is determined by the product of the gate reverse leakage I_{GSS} and R_2. This voltage should be 10 to 100 times smaller than V_P. The output impedance of the FET source follower is:

$$R_o = \frac{1}{g_m} \tag{11}$$

so that the determining resistance for the interstage RC time constant is the input resistance of the LM380.

BOOSTED GAIN USING POSITIVE FEEDBACK

For applications requiring gains higher than the internally set gain of 50, it is possible to apply positive feedback around the LM380 for closed loopgains of up to 300. *Figure 21* shows a practical example of an LM380 in a gain of 200 circuit.

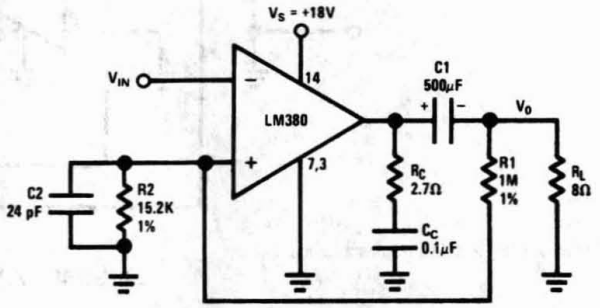


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FIGURE 21. Boosted Gain of 200 Using Positive Feedback

The equation describing the closed loop gain is:

$$A_{VCL} = \frac{-A_{V(\omega)}}{1 - \frac{A_{V(\omega)}}{1 + \frac{R_1}{R_2}}} \tag{12}$$

where $A_{V(\omega)}$ is complex at high frequencies but is nominally the 40 to 60 specified on the data sheet for the pass band of the amplifier. If $1 + R_1/R_2$ approaches the value of $A_{V(\omega)}$, the denominator of equation 12 approaches zero, the closed loop gain increases toward infinity, and the circuit oscillates. This is the reason for limiting the closed loop gain values to 300 or less. *Figure 22* shows the loaded and unloaded bode plot for the circuit shown in *Figure 21*.

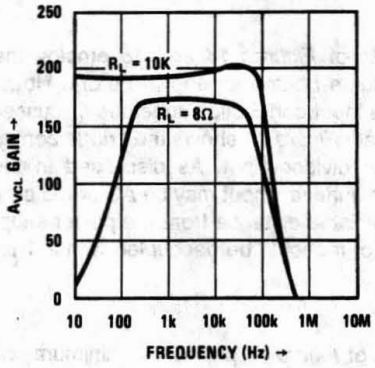

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FIGURE 22. Boosted Gain Bode Plot

The 24 pF capacitor C_2 shown on *Figure 21* was added to give an overdamped square wave response under full load conditions. It causes a high frequency roll-off of:

$$f_2 = \frac{1}{2\pi R_2 C_2} \tag{13}$$

The circuit of *Figure 21* will have a very long (1000 sec) turn on time if R_L is not present, but only a 0.01 second turn on time with an 8Ω load.

Micropower Circuits Using the LM4250 Programmable Op Amp

National Semiconductor
Application Note 71
George Cleveland

INTRODUCTION

The LM4250 is a highly versatile monolithic operational amplifier. A single external programming resistor determines the quiescent power dissipation, input offset and bias currents, slew rate, gain-bandwidth product, and input noise characteristics of the amplifier. Since the device is in effect a different op amp for each externally programmed set current, it is possible to use a single stock item for a variety of circuit functions in a system.

This paper describes the circuit operation of the LM4250, various methods of biasing the device, frequency response considerations, and some circuit applications exercising the unique characteristics of the LM4250.

CIRCUIT DESCRIPTION LM4250

The LM4250 has two special features when compared with other monolithic operational amplifiers. One is the ability to externally set the bias current levels of the amplifiers, and the other is the use of PNP transistors as the differential input pair.

Referring to *Figure 1*, Q_1 and Q_2 are high current gain lateral PNPs connected as a differential pair. R_1 and R_2 provide emitter degeneration for greater stability at high bias currents. Q_3 and Q_4 are used as active loads for Q_1 and Q_2 to provide high gain and also form a current inverter to provide the maximum drive for the single ended output into Q_5. Q_5 is an emitter follower which prevents loading of the input stage by the succeeding amplifier stage.

One advantage of this lateral PNP input stage is a common mode swing to within 200 mV of the negative supply. This feature is especially useful in single supply operation with signals referred to ground. Another advantage is the almost constant input bias current over a wide temperature range. The input resistance R_{IN} is approximately equal to 2β ($R_E + r_e$) where β is the current gain, r_e is the emitter resistance of one of the input lateral PNPs, and R_E is the resistance of one of the 10 kΩ emitter resistor. Using a DC beta of 100 and the normal temperature dependent expression for r_e gives:

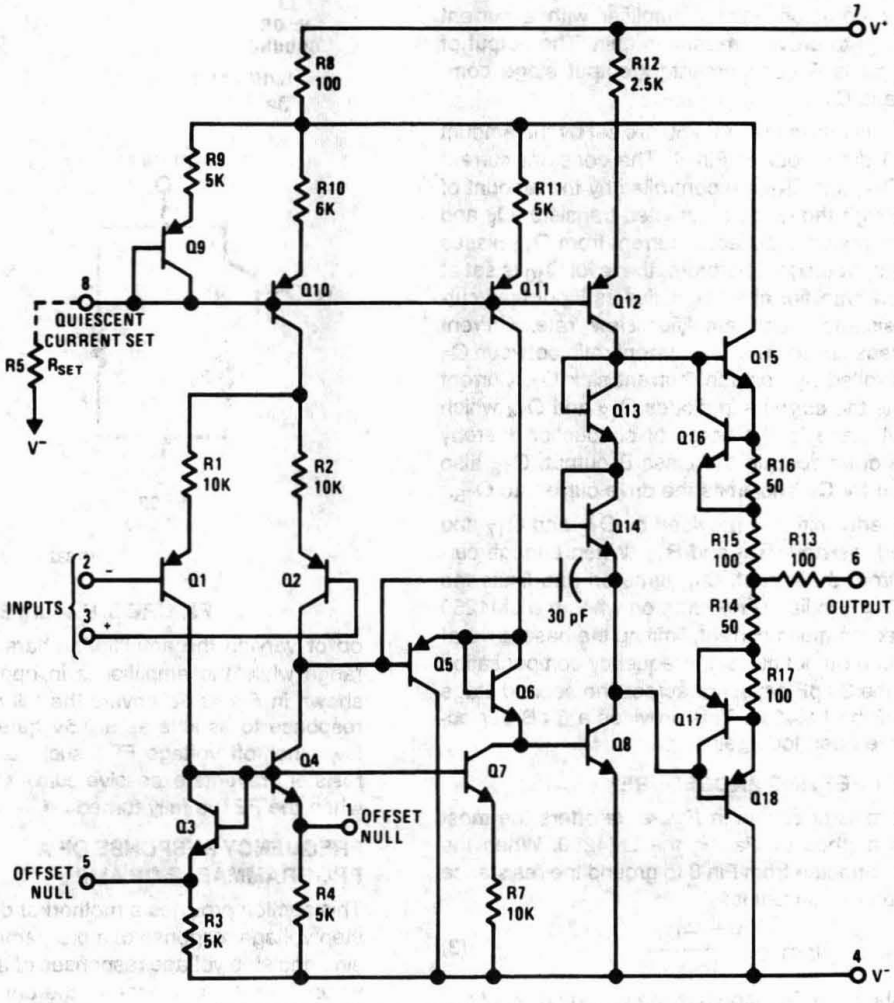

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FIGURE 1. LM4250 Schematic Diagram

$$R_{IN} \approx 2\,M\Omega + 2\frac{kT}{qI_B} \quad (1)$$

where I_B is input bias current. At room temperature this formula becomes:

$$R_{IN} \approx 2\,M\Omega + \frac{52\,mV}{I_B} \quad (2)$$

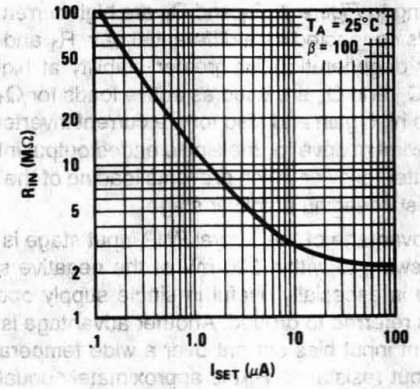

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FIGURE 2. Input Resistance vs I_{SET}

Figure 2 gives a typical plot of R_{IN} vs I_{set} derived from the above equation.

Continuing with the circuit description, Q_6 level shifts downward to the base of Q_8 which is the second stage amplifier. Q_8 is run as a common emitter amplifier with a current source load (Q_{12}) to provide maximum gain. The output of Q_8 drives the class B complementary output stage composed of Q_{15} and Q_{18}.

The bias current levels in the LM4250 are set by the amount of current (I_{set}) drawn out of Pin 8. The constant current sources Q_{10}, Q_{11}, and Q_{12} are controlled by the amount of I_{set} current through the diode connected transistor Q_9 and resistor R_9. The constant collector current from Q_{10} biases the differential input stage. Therefore, the level Q_{10} is set at will control such amplifier characteristics as input bias current, input resistance, and amplifier slew rate. Current source Q_{11} biases Q_5 and Q_6. The current ratio between Q_5 and Q_6 is controlled by constant current sink Q_7. Current source Q_{12} sets the currents in diodes Q_{13} and Q_{14} which bias the output stage to the verge of conduction thereby eliminating the dead zone in the class B output. Q_{12} also acts as the load for Q_8 and limits the drive current to Q_{15}.

The output current limiting is provided by Q_{16} and Q_{17} and their associated resistors R_{16} and R_{17}. When enough current is drawn from the output, Q_{16} turns on and limits the base drive of Q_{15}. Similarly Q_{17} turns on when the LM4250 attempts to sink too much current, limiting the base drive of Q_{18} and therefore output current. Frequency compensation is provided by the 30 pF capacitor across the second stage amplifier, Q_8, of the LM4250. This provides a 6 dB per octave rolloff of the open loop gain.

BIAS CURRENT SETTING PROCEDURE

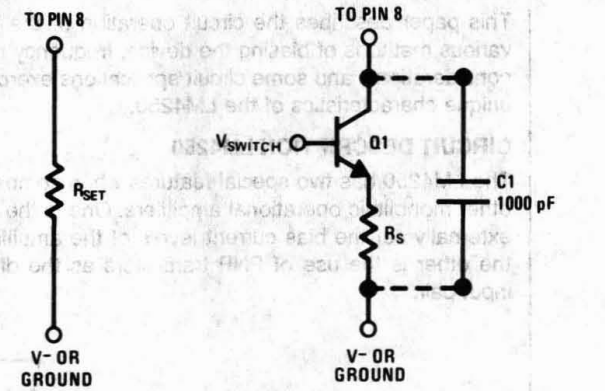
The single set resistor shown in *Figure 3a* offers the most straightforward method of biasing the LM4250. When the set resistor is connected from Pin 8 to ground the resistance value for a given set current is:

$$R_{SET} = \frac{V^+ - 0.5}{I_{SET}} \quad (3)$$

The 0.5 volts shown in Equation 3 is the voltage drop of the master bias current diode connected transistor on the integrated circuit chip. In applications where the regulation of the V^+ supply with respect to the V^- supply (as in the case of tracking regulators) is better than the V^+ supply with respect to ground the set resistor should be connected from Pin 8 to V^-. R_{SET} is then:

$$R_{SET} = \frac{V^+ + |V^-| - 0.5}{I_{SET}} \quad (4)$$

The transistor and resistor scheme shown in *Figure 3b* allows one to switch the amplifier off without disturbing the main V^+ and V^- power supply connections. Attaching C_1 across the circuit prevents any switching transient from appearing at the amplifier output. The dual scheme shown in *Figure 3c* has a constant set current flowing through R_{S1} and a variable current through R_{S2}. Transistor Q_2 acts as an emitter follower current sink whose value depends on the control voltage V_C on the base. This circuit provides a meth-



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3a

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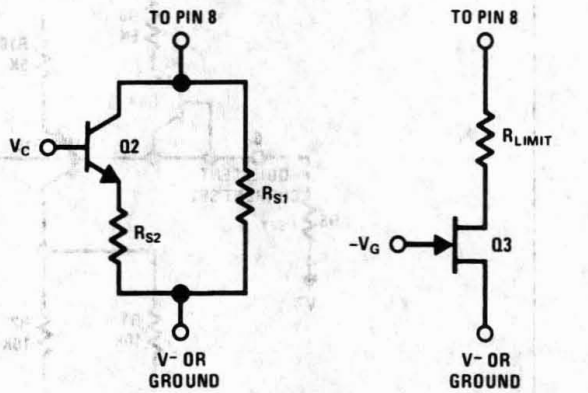
3b



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3c

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3d

FIGURE 3. Biasing Schemes

od of varying the amplifier's characteristics over a limited range while the amplifier is in operation. The FET circuit shown in *Figure 3d* covers the full range of set currents in response to as little as a 0.5V gate potential change on a low pinch-off voltage FET such as the 2N3687. The limit resistor prevents excessive current flow out of the LM4250 when the FET is fully turned on.

FREQUENCY RESPONSE OF A PROGRAMMABLE OP AMP

This section provides a method of determining the sine and step voltage response of a programmable op amp. Both the sine and step voltage responses of an amplifier are modified when the rate of change of the output voltage reaches the slew rate limit of the amplifier. The following analysis devel-

ops the Bode plot as well as the small signal and slew rate limited responses of an amplifier to these two basic categories of waveforms.

SMALL SIGNAL SINE WAVE RESPONSE

The key to constructing the Bode plot for a programmable op amp is to find the gain bandwidth product, GBWP, for a given set current. Quiescent power drain, input bias current, or slew rate considerations usually dictate the desired set current. The data sheet curve relating GBWP to set current provides the value of GBWP which when divided by one yields the unity gain crossover of f_u. Assuming a set current of 6 μA gives a GBWP of 200,000 Hz and therefore an f_u of 200 kHz for the example shown in *Figure 4*. Since the device has a single dominant pole, the rolloff slope is −20 dB of gain per decade of frequency (−6 dB/octave). The dotted line shown on *Figure 4* has this slope and passes

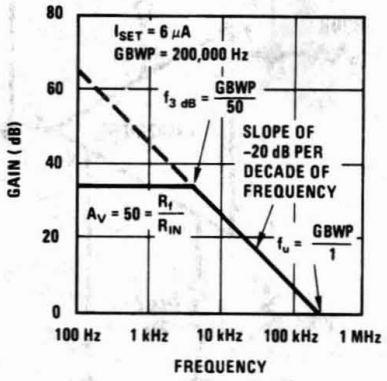

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FIGURE 4. Bode Plot

through the 200 kHz f_u point. Arbitrarily choosing an inverting amplifier with a closed loop gain magnitude of 50 determines the height of the 34 dB horizontal line shown in *Figure 4*. Graphically finding the intersection of the sloped line and the horizontal line or mathematically dividing GBWP by 50 determines the 3 dB down frequency of 4 kHz for the closed loop response of this amplifier configuration. Therefore, the amplifier will now apply a gain of −50 to all small signal sine waves at frequencies up to 4 kHz. For frequencies above 4 kHz, the gain will be as shown on the sloped portion of the Bode plot.

SMALL SIGNAL STEP INPUT RESPONSE

The amplifier's response to a positive step voltage change at the input will be an exponentially rising waveform whose rise time is a function of the closed loop 3 dB down bandwidth of the amplifier. The amplifier may be modeled as a single pole low pass filter followed by a gain of 50 wideband amplifier. From basic filter theory*, the 10% to 90% rise time of a single pole low pass filter is:

$$t_r = \frac{0.35}{f_{3\,dB}} \qquad (5)$$

For the example shown in *Figure 4* the 4 kHz 3 dB down frequency would give a rise time of 87.5 μs.

SLEW RATE LIMITED LARGE SIGNAL RESPONSE

The final consideration, which determines the upper speed limitation on the previous two types of signal responses, is the amplifier slew rate. The slew rate of an amplifier is the maximum rate of change of the output signal which the amplifier is capable of delivering. In the case of sinosoidal signals, the maximum rate of change occurs at the zero crossing and may be derived as follows:

*See reference.

$$V_O = V_p \sin 2\pi f t \qquad (6)$$

$$\frac{d V_O}{d t} = 2\pi f V_p \cos 2\pi f t \qquad (7)$$

$$\left.\frac{d V_O}{d t}\right|_{t=o} = 2\pi f V_p \qquad (8)$$

$$S_r = 2\pi f_{MAX} V_P \qquad (9)$$

where:

V_O = output voltage

V_p = peak output voltage

S_r = maximum $\frac{d V_O}{dt}$

The maximum sine wave frequency an amplifier with a given slew rate will sustain without causing the output to take on a triangular shape is therefore a function of the peak amplitude of the output and is expressed as:

$$f_{MAX} = \frac{S_r}{2\pi V_p} \qquad (10)$$

Figure 5 shows a quick reference graphical presentation of this formula with the area below any V_{peak} line representing an undistorted small signal sine wave response for a given frequency and amplifier slew rate and the area above the V_{peak} line representing a distorted sine wave response due to slew rate limiting for a sine wave with the given V_{peak}.

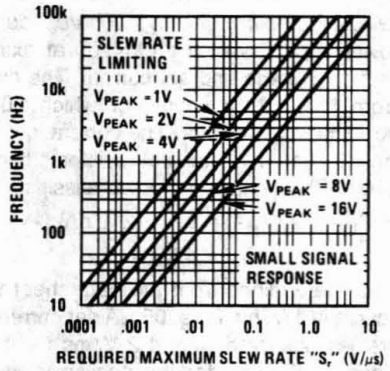

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FIGURE 5. Frequency vs Slew Rate Limit vs Peak Output Voltage

Large signal step voltage changes at the output will have a rise time as shown in equation 5 until a signal with a rate of output voltage change equal to the slew rate of the amplifier occurs. At this point the output will become a ramp function with a slope equal to S_r. This action occurs when:

$$S_r \leq \frac{V_{step}}{t_r} \qquad (11)$$

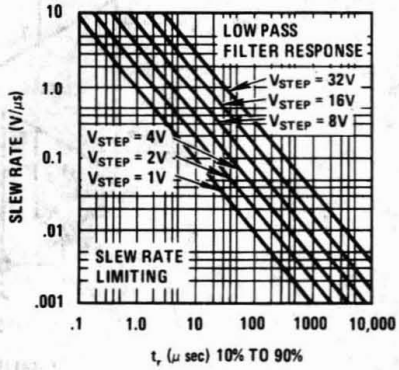

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FIGURE 6. Slew Rate vs Rise Time vs Step Voltage

Figure 6 graphically expresses this formula and shows the maximum amplitude of undistorted step voltage for a given slew rate and rise time. The area above each step voltage line represents the undistorted low pass filter type response mode of the amplifier. If the intersection of the rise time and slew rate values of a particular amplifier configuration falls below the expected step voltage amplitude line, the rise time will be determined by the slew rate of the amplifier. The rise time will then be equal to the amplitude of the step divided by the slew rate S_r.

FULL POWER BANDWIDTH

The full power bandwidth often found on amplifier specification sheets is the range of frequencies from zero to the frequency found at the intersection on *Figure 5* of the maximum rated output voltage and the slew rate S_r of the amplifier. Mathematically this is:

$$f_{\text{full power}} = \frac{S_r}{2\pi V_{\text{rated}}} \qquad (12)$$

The full power bandwidth of a programmable amplifier such as the LM4250 varies with the master bias set current.

The above analysis of sine wave and step voltage amplifier responses applies for all single dominant pole op amps such as the LM101A, LM1107, LM108A, LM112, LM118, and LM741 as well as the LM4250 programmable op amp.

500 MANO-WATT X10 AMPLIFIER

The X10 inverting amplifier shown in *Figure 7* demonstrates the low power capability of the LM4250 at extremely low values of supply voltage and set current. The circuit draws 260 nA from the +1.0V supply of which 50 nA flows through the 12 MΩ set resistor. The current into the −1.0V supply is only 210 nA since the set resistor is tied to ground rather than V^-. Total quiescent power dissipation is:

$$P_D = (260\text{ nA})(1\text{V}) + (210\text{ nA})(1\text{V}) \qquad (13)$$

$$P_D = 470\text{ nW} \qquad (14)$$

The slew rate determined from the data sheet typical performance curve is 1 V/ms for a .05 μA set current. Samples of actual values observed were 1.2 V/ms for the negative slew rate and 0.85 V/ms for the positive slew rate. This difference occurs due to the non-symmetry in the current sources used for charging and discharging the internal 30 pF compensation capacitor.

The 3 dB down (gain of −7.07) frequency observed for this configuration was approximately 300 Hz which agrees fairly closely with the 3.5 kHz GBWP divided by 10 taken from an extrapolation of the data sheet typical GBWP versus set current curve.

Peak-to-peak output voltage swing into a 100 kΩ load is 0.7V or ±0.35V peak. An increase in supply voltage to ±1.35V such as delivered by a pair of mercury cells directly increases the output swing by ±0.35V to 1.4V peak-to-peak. Although this increases the power dissipation to approximately 1 μW per battery, a power drain of 15 μW or less will not affect the shelf life of a mercury cell.

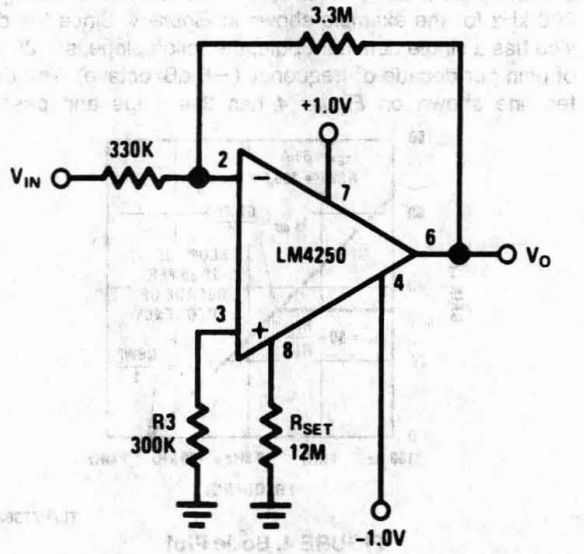

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FIGURE 7. 500 nW x 10 Amplifier

MICRO-POWER MONITOR WITH HIGH CURRENT SWITCH

Figure 8 shows the combination of a micro-power comparator and a high current switch run from a separate supply. This circuit provides a method of continuously monitoring an input voltage while dissipating only 100 μW of power and still being capable of switching a 500 mA load if the input exceeds a given value. The reference voltage can be any value between +8.5V and −8.5V. With a minimum gain of approximately 100,000 the comparator can resolve input voltage differences down into the 0.2 mV region.

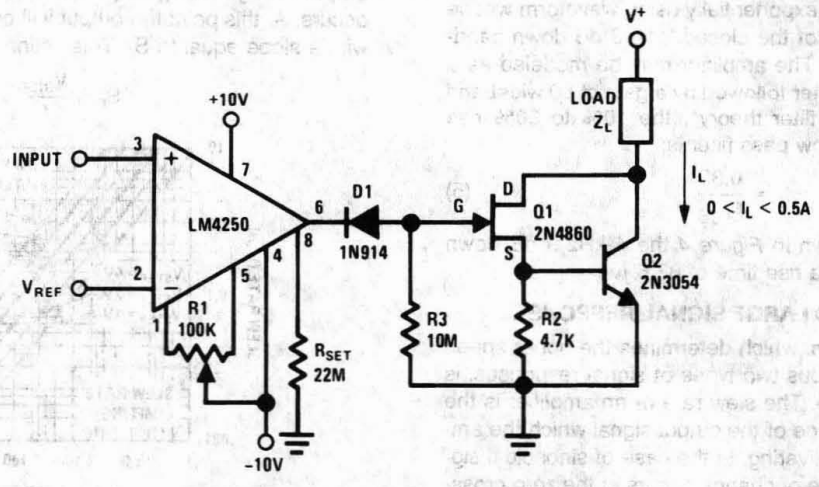

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FIGURE 8. μ–Power Comparator with High Current Switch

The bias current for the LM4250 shown in *Figure 8* is set at 0.44 μA by the 200 MΩ R_{set} resistor. This results in a total comparator power drain of 100 μW and a slew rate of approximately 11 V/ms in the positive direction and 12.8 V/ms in the negative direction. Potentiometer R_1 provides input offset nulling capability for high accuracy applications. When the input voltage is less than the reference voltage, the output of the LM4250 is at approximately −9.5V causing diode D_1 to conduct. The gate of Q_1 is held at −8.8V by the voltage developed across R_3. With a large negative voltage on the gate of Q_1 it turns off and removes the base drive from Q_2. This results in a high voltage or open switch condition at the collector of Q_2. When the input voltage exceeds the reference voltage, the LM4250 output goes to +9.5V causing D_1 to be reverse biased. Q_1 turns on as does Q_2, and the collector of Q_2 drops to approximately 1V while sinking the 500 mA of load current.

The load denoted as Z_L can be resistor, relay coil, or indicator lamp as required; but the load current should not exceed 500 mA. For V^+ values of less than 15V and I_L values of less than 25 mA both Q_2 and R_2 may be omitted. With only the 2N4860 JFET as an output device the circuit is still capable of driving most common types of indicator lamps.

IC METER AMPLIFIER RUNS ON TWO FLASHLIGHT BATTERIES

Meter amplifiers normally require one or two 9V transistor batteries. Due to the heavy current drain on these supplies, the meters must be switched to the OFF position when not in use. The meter circuit described here operates on two 1.5V flashlight batteries and has a quiescent power drain so low that no ON-OFF switch is needed. A pair of Eveready No. 950 "D" cells will serve for a minimum of one year without replacement. As a DC ammeter, the circuit will provide current ranges as low as 100 nA full-scale.

The basic meter amplifier circuit shown in *Figure 9* is a current-to-voltage converter. Negative feedback around the amplifier insures that currents I_{IN} and I_f are always equal, and the high gain of the op amp insures that the input voltage between Pins 2 and 3 is in the microvolt region. Output

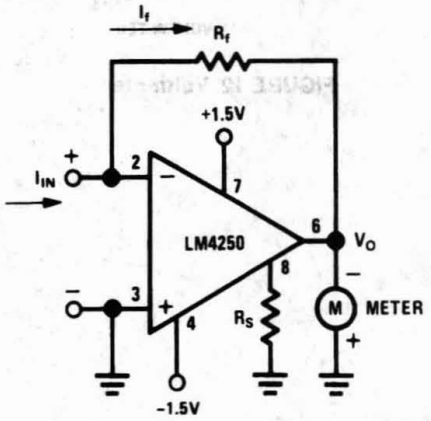

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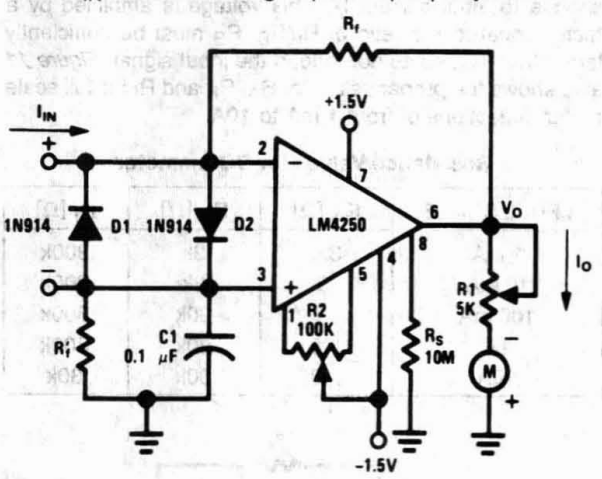
FIGURE 9. Basic Meter Amplifier

voltage V_O is therefore equal to $-I_fR_f$. Considering the ±1.5V sources (±1.2V end-of-life) a practical value of V_O for full scale meter deflection is 300 mV. With the master bias-current setting resistor (R_S) set at 10 MΩ, the total quiescent current drain of the circuit is 0.6 μA for a total power supply drain of 1.8 μW. The input bias current, required by the amplifier at this low level of quiescent current, is in the range of 600 pA.

THE COMPLETE NANOAMMETER

The complete meter amplifier shown in *Figure 10* is a differential current-to-voltage converter with input protection, zeroing and full scale adjust provisions, and input resistor balancing for minimum offset voltage. Resistor R'_f (equal in value to R_f for measurements of less than 1 μA) insures that the input bias currents for the two input terminals of the amplifier do not contribute significantly to an output error voltage. The output voltage V_O for the differential current-to-voltage converter is equal to $-2\ I_fR_f$ since the floating input current I_{IN} must flow through R_f and R'_f. R'_f may be omitted



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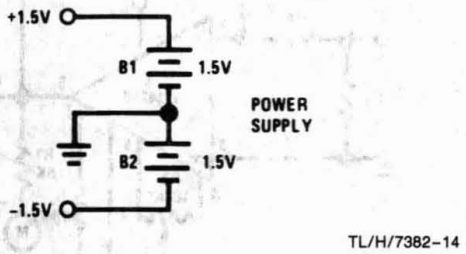

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FIGURE 10. Complete Meter Amplifier

Resistance Values for DC Nano and Micro Ammeter

I FULL SCALE	R_f [Ω]	R'_f [Ω]
100 nA	1.5M	1.5M
500 nA	300k	300k
1 μA	300k	0
5 μA	60k	0
10 μA	30k	0
50 μA	6k	0
100 μA	3k	0

for R_f values of 500 kΩ or less, since a resistance of this value contributes an error of less than 0.1% in output voltage. Potentiometer R_2 provides an electrical meter zero by forcing the input offset voltage V_{OS} to zero. Full scale meter deflection is set by R_1. Both R_1 and R_2 only need to be set once for each op amp and meter combination. For a 50 microamp 2 kΩ meter movement, R_1 should be about 4 kΩ to give full scale meter deflection in response to a 300 mV output voltage. Diodes D_1 and D_2 provide full input protection for overcurrents up to 75 mA.

With an R_f resistor value of 1.5M the circuit in *Figure 10* becomes a nanommeter with a full scale reading capability

of 100 nA. Reducing R_f to 3 kΩ in steps, as shown in *Figure 10* increases the full scale deflection to 100 μA, the maximum for this circuit configuration. The voltage drop across the two input terminals is equal to the output voltage V_o divided by the open loop gain. Assuming an open loop gain of 10,000 gives an input voltage drop of 30 μV or less.

CIRCUIT FOR HIGHER CURRENT READINGS

For DC current readings higher than 100 μA, the inverting amplifier configuration shown in *Figure 11* provides the required gain. Resistor R_A develops a voltage drop in response to input current I_A. This voltage is amplified by a factor equal to the ratio of R_f/R_B. R_B must be sufficiently larger than R_A, so as not to load the input signal. *Figure 11* also shows the proper values of R_A, R_B and R_f for full scale meter deflections of from 1 mA to 10A.

Resistance Values for DC Ammeter

I FULL SCALE	R_A [Ω]	R_B [Ω]	R_f [Ω]
1 mA	3.0	3k	300k
10 mA	.3	3k	300k
100 mA	.3	30k	300k
1A	.03	30k	300k
10A	.03	30k	30k

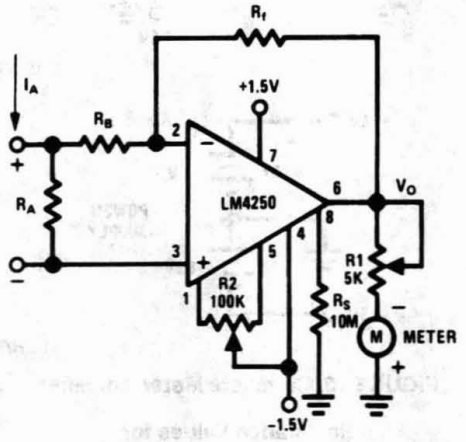

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FIGURE 11. Ammeter

A 10 mV TO 100V FULL-SCALE VOLTMETER

A resistor inserted in series with one of the input leads of the basic meter amplifier converts it to a wide range voltmeter circuit, as shown in *Figure 12*. This inverting amplifier has a gain varying from −30 for the 10 mV full scale range to −0.003 for the 100V full scale range. *Figure 12* also lists the proper values of R_v, R_f, and R'_f for each range. Diodes D_1 and D_2 provide complete amplifier protection for input overvoltages as high as 500V on the 10 mV range, but if overvoltages of this magnitude are expected under continuous operation, the power rating of R_v should be adjusted accordingly.

Resistance Values for a DC Voltmeter

V FULL SCALE	R_V [Ω]	R_f [Ω]	R'_f [Ω]
10 mV	100k	1.5M	1.5M
100 mV	1M	1.5M	1.5M
1V	10M	1.M	1.5M
10V	10M	300k	0
100V	10M	30k	0

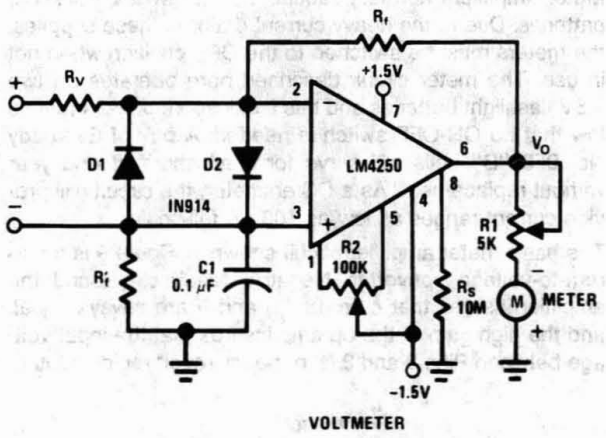

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FIGURE 12. Voltmeter

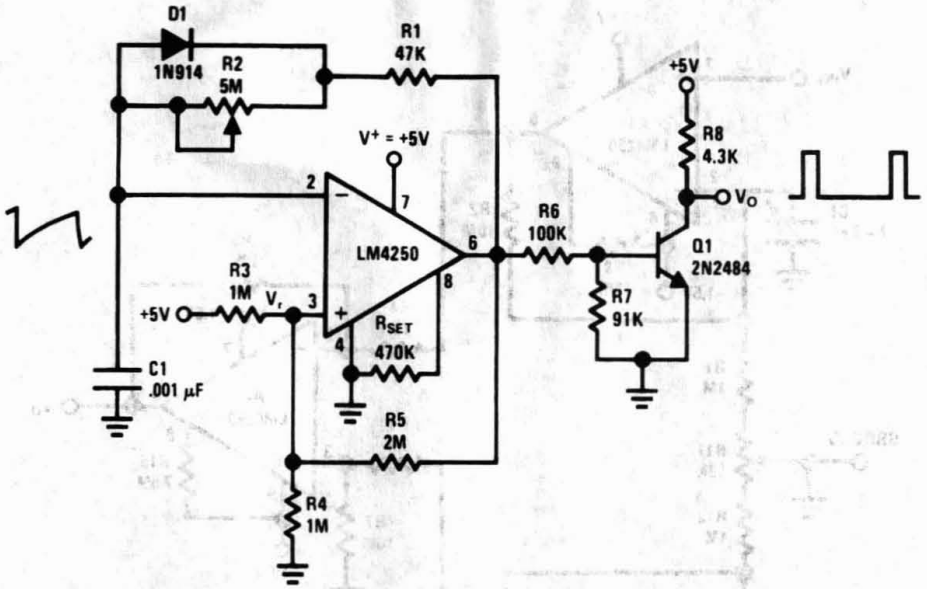

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FIGURE 13. Pulse Generator

LOW FREQUENCY PULSE GENERATOR USING A SINGLE +5V SUPPLY

The variable frequency pulse generator shown in *Figure 13* provides an example of the LM4250 operated from a single supply. The circuit is a buffered output free running multivibrator with a constant width output pulse occurring with a frequency determined by potentiometer R_2.

The LM4250 acts as a comparator for the voltages found at the upper plate of capacitor C_1 and at the reference point denoted as V_r on *Figure 13*. Capacitor C_1 charges and discharges with a peak-to-peak amplitude of approximately 1V determined by the shift in reference voltage V_r at Pin 3 of the op amp. The charge path of C_1 is from the amplifier output, which is at its maximum positive voltage V_{HIGH} (approximately $V^+ - 0.5V$), through R_1 and through the potentiometer R_2. Diode D_1 is reverse biased during the charge period. When C_1 charges to the V_r value determined by the net result of V_{HIGH} through resistor R_5 and V^+ through the voltage divider made up of resistors R_3 and R_4 the amplifier swings to its lower limit of approximately 0.5V causing C_1 to begin discharging. The discharge path is through the forward biased diode D_1, through resistor R_1, and into Pin 6 of the op amp. Since the impedance in the discharge path does not vary for R_2 settings of from 3 kΩ to 5 MΩ, the output pulse maintains a constant pulse width of 41 μs ±1.5 μs over this range of potentiometer settings. *Figure 14* shows the output pulse frequency variation from 6 kHz down to 360 Hz as R_2 places from 100 kΩ up to 5 MΩ of additional resistance in the charge path of C_1. Setting R_2 to zero ohms will short out diode D_1 and cause a symmetrical square wave output at a frequency of 10 kHz. Increasing the value of C_1 will lower the range of frequencies available in response to the R_2 variation shown on *Figure 14*. Electrolytic capacitors may be used for the larger values of C_1 since it has only positive voltages applied to it.

The output buffer Q_1 presents a constant load to the op amp output thereby preventing frequency variations caused by V_{HIGH} and V_{LOW} voltages changing as a function of load current. The output of Q_1 will interface directly with a standard TTL or DTL logic device. Reversing diode D1 will invert the polarity of the generator output providing a series of negative going pulses dropping from +5V to the saturation voltage of Q_1.

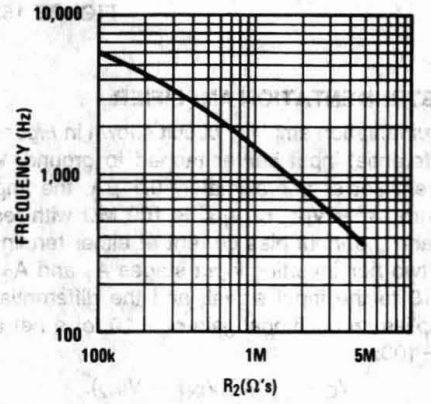

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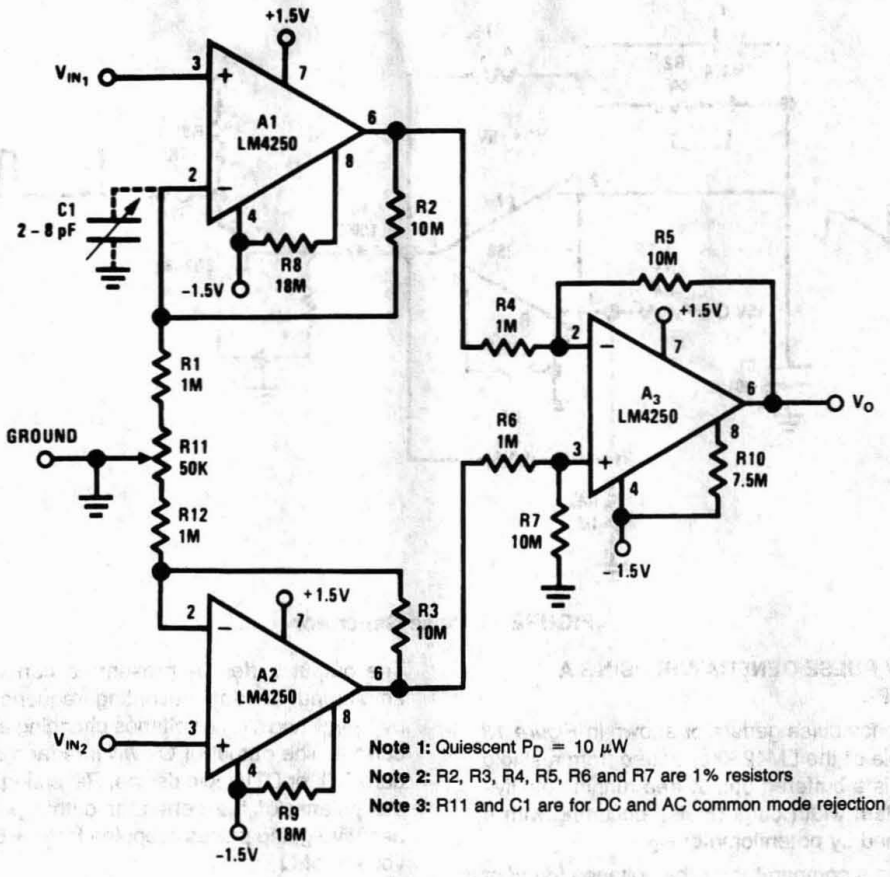
FIGURE 14. Pulse Frequency vs R_2

The change in output frequency as a function of supply voltage is less than ±4% for a V^+ change of from 4V to 10V. This stability of frequency versus supply voltage is due to the fact that the reference voltage V_r and the drive voltage for the capacitor are both direct functions of V^+.

The power dissipation of the free running multivibrator is 300 μW and the power dissipation of the buffer circuit is approximately 5.8 mW.



Note 1: Quiescent P_D = 10 μW

Note 2: R2, R3, R4, R5, R6 and R7 are 1% resistors

Note 3: R11 and C1 are for DC and AC common mode rejection adjustments

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FIGURE 15. × 100 Instrumentation Amplifier

X100 INSTRUMENTATION AMPLIFIER

The instrumentation amplifier circuit shown in *Figure 15* has a full differential input center tapped to ground. With the bias current set at approximately 0.1 μA, the impedance looking into either V_{IN_1} or V_{IN_2} is 100 MΩ with respect to ground, and the input bias current at either terminal is 0.2 nA. The two non-inverting input stages A_1 and A_2 apply a gain of 10 to the input signal, and the differential output stage applies an additional gain of −10 for a net amplifier gain of −100:

$$V_O = -100(V_{IN_1} - V_{IN2}). \quad (15)$$

The entire circuit can run from two 1.5V batteries connected directly (no power switch) to the V^+ and V^- terminals. With a total current drain of 2.8 μA the quiescent power dissipation of the circuit is 8.4 μW. This is low enough to have no significant effect on the shelf life of most batteries.

Potentiometer R_{11} provides a means for matching the gains of A_1 and A_2 to achieve maximum DC common mode rejection ratio CMRR. With R_{11} adjusted to its null point for DC common mode rejection the small AC CMRR trimmer capacitor C_1 will normally give an additional 10 to 20 dB of CMRR over the operating frequency range. Since C_1 actually balances wiring capacitance rather than amplifier frequency characteristics, it may be necessary to attach it to Pin 2 of either A_1 or A_2 as required. *Figure 16* shows the variation of CMRR (referred to the input) with frequency for this configuration. Since the circuit applies a gain of 100 or 40 dB to an input signal, the actual observed rejection ratio

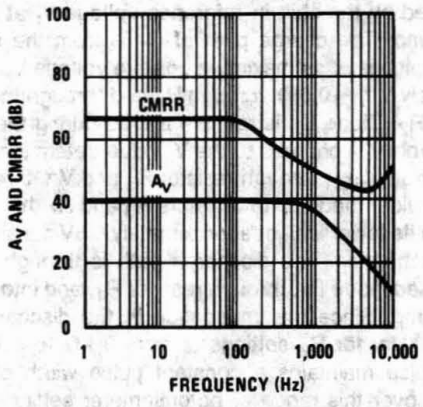

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FIGURE 16. A_V and CMRR vs Frequency

is the difference between the CMRR curve and A_V curve. For example, a 60 Hz common mode signal will be attenuated by 67 dB minus 40 db or 27 dB for an actual rejection ratio of V_{IN}/V_O equal to 22.4.

The maximum peak-to-peak output signal into a 100 kΩ load resistor is approximately 1.8V. With no input signal, the noise seen at the output is approximately 0.8 mV_{RMS} or 8 μV_{RMS} referred to the input. When doing power dissipation measurements on this circuit, it should be kept in mind that even a 1 MΩ oscilloscope probe placed between +1.5V and −1.5V will more than double the power drawn from the batteries.

5V REGULATOR FOR CMOS LOGIC CIRCUITS

The ideal regulator for low power CMOS logic elements should dissipate essentially no power when the CMOS devices are running at low frequencies, but be capable of delivering full output power on demand when the CMOS devices are running in the 0.1 MHz to 10 MHz region. With a 10V input voltage, the regulator shown in *Figure 17* will dissipate 350 μW in the stand-by mode but will deliver up to 50 mA of continuous load current when required.

The circuit is basically a boosted output voltage-follower referenced to a low current zener diode. The voltage divider consisting of R_2 and R_3 provides a 5V tap voltage from the 6.5V reference diode to determine the regulator output. Since a standard 6.5V zener diode does not exhibit good regulation in the 2 μA to 60 μA reverse current region, Q_2 must be a special device. An NPN transistor with its collector and base terminals grounded and its emitter tied to the junction of R_1 and R_2 exhibits a well-controlled base emitter reverse breakdown voltage. A National Semiconductor process 25 small signal NPN transistor sorted to a 2N registration such as 2N3252 has a BV_{EBO} at 10 μA specified as 5.5V minimum, 6.5V typical, and 7.0V maximum. Using a diode connected 2N3252 as a reference, the regulator output voltage changed 78 mV in response to an 8V to 36V change in the input voltage. This test was done under both no load and full load conditions and represents a line regulation of better than 1.6%.

A load change from 10 μA to 50 mA caused a 1 mV change in output voltage giving a load regulation value of 0.05%. When operating the regulator at load currents of less than 25 mA, no heat sink is required for Q_1. For load currents in excess of 50 mA, Q_1 should be replaced by a Darlington pair with the 2N3019 acting as a driver for a higher power device such as a 2N3054.

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Millman, J. and Halkias, C.C.: *"Electronic Device and Circuits,"* pp. 465–466, McGraw-Hill Book Company, New York, 1967.

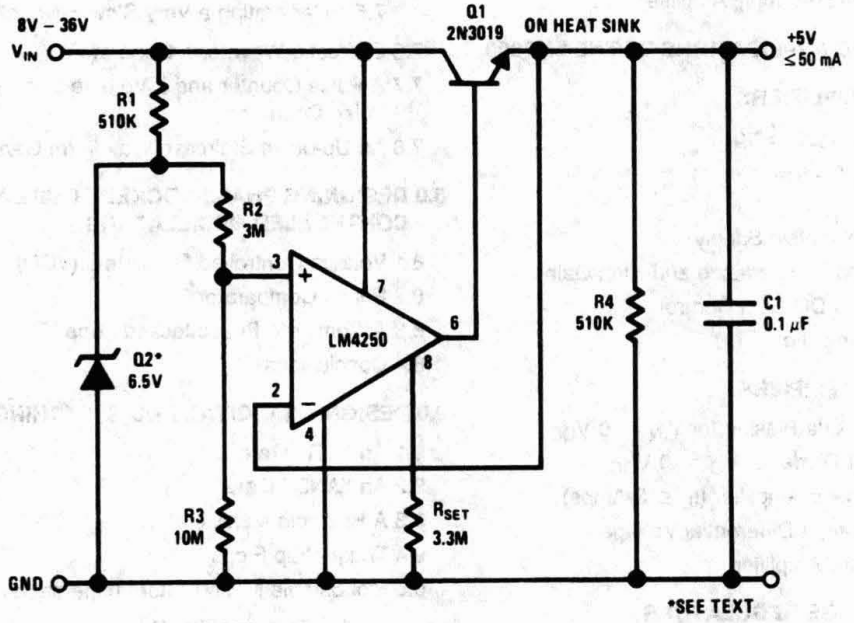

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FIGURE 17. 350 μW Quiescent Drain 5 Volt Regulator

The LM3900: A New Current-Differencing Quad of ± Input Amplifiers

National Semiconductor
Application Note 72

PREFACE

With all the existing literature on "how to apply op amps" why should another application note be produced on this subject? There are two answers to this question; 1) the LM3900 operates in quite an unusual manner (compared to a conventional op amp) and therefore needs some explanation to familiarize a new user with this product, and 2) the standard op amp applications assume a split power supply ($\pm 15\ V_{DC}$) is available and our emphasis here is directed toward circuits for lower cost single power supply control systems. Some of these circuits are simply "re-biased" versions of conventional handbook circuits but many are new approaches which are made possible by some of the unique features of the LM3900.

Table of Contents

1.0 AN INTRODUCTION TO THE NEW "NORTON" AMPLIFIER

1.1 Basic Gain Stage
1.2 Obtaining a Non-inverting Input Function
1.3 The Complete Single-Supply Amplifier

2.0 INTRODUCTION TO APPLICATIONS OF THE LM3900

3.0 DESIGNING AC AMPLIFIERS

3.1 Single Power Supply Biasing
3.2 A Non-inverting Amplifier
3.3 "N V_{BE}" Biasing
3.4 Biasing Using a Negative Supply
3.5 Obtaining High Input Impedance and High Gain
3.6 An Amplifier with a DC Gain Control
3.7 A Line-receiver Amplifier

4.0 DESIGNING DC AMPLIFIERS

4.1 Using Common-mode Biasing for $V_{IN} = 0\ V_{DC}$
4.2 Adding an Output Diode for $V_O = 0\ V_{DC}$
4.3 A DC Coupled Power Amplifier ($I_L \leq 3$ Amps)
4.4 Ground Referencing a Differential Voltage
4.5 A Unity Gain Buffer Amplifier

5.0 DESIGNING VOLTAGE REGULATORS

5.1 Reducing the Input-output Voltage
5.2 Providing High Input Voltage Protection
5.3 High Input Voltage Protection and Low ($V_{IN} - V_{OUT}$)
5.4 Reducing Input Voltage Dependence and Adding Short-Circuit Protection

6.0 DESIGNING RC ACTIVE FILTERS

6.1 Biasing the Amplifiers
6.2 A High Pass Active Filter
6.3 A Low Pass Active Filter
6.4 A Single-amplifier Bandpass Active Filter
6.5 A Two-amplifier Bandpass Active Filter
6.6 A Three-amplifier Bandpass Active Filter
6.7 Conclusions

7.0 DESIGNING WAVEFORM GENERATORS

7.1 Sinewave Oscillator
7.2 Squarewave Generator

7.0 DESIGNING WAVEFORM GENERATORS (Continued)

7.3 Pulse Generator
7.4 Triangle Waveform Generator
7.5 Sawtooth Waveform Generator
7.5.1 Generating a Very Slow Sawtooth Waveform
7.6 Staircase Waveform Generators
7.7 A Pulse Counter and a Voltage Variable Pulse Counter
7.8 An Up-down Staircase Waveform Generator

8.0 DESIGNING PHASE-LOCKED LOOPS AND VOLTAGE CONTROLLED OSCILLATORS

8.1 Voltage Controlled Oscillators (VCO)
8.2 Phase Comparator
8.3 A Complete Phase-locked Loop
8.4 Conclusions

9.0 DESIGNING DIGITAL AND SWITCHING CIRCUITS

9.1 An "OR" Gate
9.2 An "AND" Gate
9.3 A Bi-stable Multivibrator
9.4 Trigger Flip Flops
9.5 Monostable Multivibrators (One-shots)
9.5.1 A Two-amplifier One-shot
9.5.2 A Combination One-shot/Comparator Circuit
9.5.3 A One-amplifier One-shot (Positive Pulse)
9.5.4 A One-amplifier One-shot (Negative Pulse)
9.6 Comparators
9.6.1 A Comparator for Positive Input Voltages
9.6.2 A Comparator for Negative Input Voltages
9.6.3 A Power Comparator
9.6.4 A More Precise Comparator
9.7 Schmitt Triggers

10.0 SOME SPECIAL CIRCUIT APPLICATIONS

10.1 Current Sources and Sinks
10.1.1 A Fixed Current Source
10.1.2 A Voltage Variable Current Source
10.1.3 A Fixed Current Sink
10.1.4 A Voltage Variable Current Sink

Table of Contents (Continued)

10.0 SOME SPECIAL CIRCUIT APPLICATIONS (Continued)

10.2 Operation from ±15 V_{DC} Power Supplies

10.2.1 An AC Amplifier Operating with ±15 V_{DC} Power Supplies

10.2.2 A DC Amplifier Operating with ±15 V_{DC} Power Supplies

10.3 Tachometers

10.3.1 A Basic Tachometer

10.3.2 Extending V_{OUT} (Minimum) to Ground

10.3.3 A Frequency Doubling Tachometer

10.4 A Squaring Amplifier

10.5 A Differentiator

10.6 A Difference Integrator

10.7 A Low Drift Sample and Hold Circuit

10.7.1 Reducing the "Effective" Input Biasing Current

10.7.2 A Low Drift Ramp and Hold

10.7.3 Sample-Hold and Compare with New $+V_{IN}$

10.0 SOME SPECIAL CIRCUIT APPLICATIONS (Continued)

10.8 Audio Mixer or Channel Selector

10.9 A Low Frequency Mixer

10.10 A Peak Detector

10.11 Power Circuits

10.11.1 Lamp and/or Relay Drivers (≤30 mA)

10.11.2 Lamp and/or Relay Drivers (≤300 mA)

10.11.3 Positive Feedback Oscillators

10.12 High Voltage Operation

10.12.1 A High Voltage Inverting Amplifier

10.12.2 A High Voltage Non-inverting Amplifier

10.12.3 A Line Operated Audio Amplifier

10.13 Temperature Sensing

10.14 A "Programmable Unijunction"

10.15 Adding a Differential Input Stage

List of Illustrations

1 Basic Gain Stage
2 Adding a PNP Transistor to the Basic Gain Stage
3 Adding a Current Mirror to Achieve a Non-inverting Input
4 The Amplifier Stage
5 Open-loop Gain Characteristics
6 Schematic Diagram of the LM3900
7 An Equivalent Circuit of a Standard IC Op Amp
8 An Equivalent Circuit of the "Norton" Amplifier
9 Applying the LM3900 Equivalent Circuit
10 Biasing Equivalent Circuit
11 AC Equivalent Circuit
12 Inverting AC Amplifier Using Single-supply Biasing
13 Non-inverting AC Amplifier Using Voltage Reference Biasing
14 Inverting AC Amplifier Using N V_{BE} Biasing
15 Negative Supply Biasing
16 A High Z_{IN} High Gain Inverting AC Amplifier
17 An Amplifier with a DC Gain Control
18 A Line-receiver Amplifier
19 A DC Amplifier Employing Common-mode Biasing
20 An Ideal Circuit Model of a DC Amplifier with Zero Input Voltage
21 A Non-inverting DC Amplifier with Zero Volts Output for Zero Volts Input
22 Voltage Transfer Function for a DC Amplifier with a Voltage Gain of 10
23 A DC Power Amplifier
24 Ground Referencing a Differential Input DC Voltage
25 A Network to Invert and to Ground Reference a Negative DC Differential Input Voltage
26 A Unity-gain DC Buffer Amplifier
27 Simple Voltage Regulators
28 Reducing ($V_{IN} - V_{OUT}$)
29 High V_{IN} Protection and Self-regulation
30 A High V_{IN} Protected, Low ($V_{IN} - V_{OUT}$) Regulator

List of Illustrations (Continued)

31 Reducing V_{IN} Dependence
32 Adding Short-Circuit Current Limiting
33 Biasing Considerations
34 A High Pass Active Filter
35 A Low Pass Active Filter
36 Biasing the Low Pass Filter
37 Biasing Equivalent Circuit
38 A One Op amp Bandpass Filter
39 A Two Op amp Bandpass Filter
40 The "Bi-quad" RC Active Bandpass Filter
41 A Sinewave Oscillator
42 A Squarewave Oscillator
43 A Pulse Generator
44 A Triangle Waveform Generator
45 Gated Sawtooth Generators
46 Generating Very Slow Sawtooth Waveforms
47 Pumping the Staircase Via Input Differentiator
48 A Free Running Staircase Generator
49 An Up-down Staircase Generator
50 A Voltage Controlled Oscillator
51 Adding Input Common-Mode Biasing Resistors
52 Reducing Temperature Drift
53 Improving Mark/Space Ratio
54 Phase Comparator
55 A Phase-Locked Loop
56 An "OR" Gate
57 An "AND" Gate
58 A Large Fan-in "AND" Gate
59 A Bi-Stable Multivibrator
60 A Trigger Flip Flop
61 A Two-amplifier Trigger Flip Flop
62 A One-Shot Multivibrator
63 A One-Shot Multivibrator with an Input Comparator
64 A One-Amplifier One-Shot (Positive Output)
65 A One-Amplifier One-Shot (Negative Output)
66 An Inverting Voltage Comparator
67 A Non-Inverting Low-voltage Comparator
68 A Non-Inverting Power Comparator
69 A More Precise Comparator
70 Schmitt Triggers
71 Fixed Current Sources
72 A Voltage Controlled Current Source
73 Fixed Current Sinks
74 A Voltage Controlled Current Sink
75 An AC Amplifier Operating with $\pm 15\ V_{DC}$
76 DC Biasing for $\pm 15\ V_{DC}$ Operation
77 A DC Amplifier Operating with $\pm 15\ V_{DC}$
78 A Basic Tachometer
79 Adding Biasing to Provide $V_O = 0\ V_{DC}$
80 A Frequency Doubling Tachometer
81 A Squaring Amplifier with Hysteresis
82 A Differentiator Circuit
83 A Difference Integrator

List of Illustrations (Continued)

84 Reducing I_B "Effective"to Zero
85 A Low-Drift Ramp and Hold Circuit
86 Sample-Hold and Compare with New $+V_{IN}$
87 Audio Mixing or Selection
88 A Low Frequency Mixer
89 A Peak Detector
90 Sinking 20 to 30 mA Loads
91 Boosting to 300 mA Loads
92 Positive Feedback Power Oscillators
93 A High Voltage Inverting Amplifier
94 A High Voltage Non-Inverting Amplifier
95 A Line Operated Audio Amplifier
96 Temperature Sensing
97 A "Programmable Unijunction"
98 Adding a Differential Input Stage

The LM3900: A New Current-Differencing Quad of ± Input Amplifiers

1.0 An Introduction to the New "Norton" Amplifier

The LM3900 represents a departure from conventional amplifier designs. Instead of using a standard transistor differential amplifier at the input, the non-inverting input function has been achieved by making use of a "current-mirror" to "mirror" the non-inverting input current about ground and then to extract this current from that which is entering the inverting input terminal. Whereas the conventional op amp differences input voltages, this amplifier differences input currents and therefore the name "Norton Amp" has been used to indicate this new type of operation. Many biasing advantages are realized when operating with only a single power supply voltage. The fact that currents can be passed between the input terminals allows some unusual applications. If external, large valued input resistors are used (to convert from input voltages to input currents) most of the standard op amp applications can be realized.

Many industrial electronic control systems are designed that operate off of only a single power supply voltage. The conventional integrated-circuit operational amplifier (IC op amp) is typically designed for split power supplies ($\pm 15\ V_{DC}$) and suffers from a poor output voltage swing and a rather large minimum common-mode input voltage range (approximately $+ 2\ V_{DC}$) when used in a single power supply application. In addition, some of the performance characteristics of these op amps could be sacrificed—especially in favor of reduced costs.

To meet the needs of the designers of low-cost, single-power-supply control systems, a new internally compensated amplifier has been designed that operates over a power supply voltage range of $+4\ V_{DC}$ to $36\ V_{DC}$ with small changes in performance characteristics and provides an output peak-to-peak voltage swing that is only 1V less than the magnitude of the power supply voltage. Four of these amplifiers have been fabricated on a single chip and are provided in the standard 14-pin dual-in-line package.

The cost, application and performance advantages of this new quad amplifier will guarantee it a place in many single power supply electronic systems. Many of the "housekeeping" applications which are now handled by standard IC op amps can also be handled by this "Norton" amplifier operating off the existing $\pm 15\ V_{DC}$ power supplies.

1.1 BASIC GAIN STAGE

The gain stage is basically a single common-emitter amplifier. By making use of current source loads, a large voltage gain has been achieved which is very constant over temperature changes. The output voltage has a large dynamic range, from essentially ground to one V_{BE} less than the power supply voltage. The output stage is biased class A for small signals but converts to class B to increase the load current which can be "absorbed" by the amplifier under large signal conditions. Power supply current drain is essentially independent of the power supply voltage and ripple on the supply line is also rejected. A very small input biasing current allows high impedance feedback elements to be used and even lower "effective" input biasing currents can be realized by using one of the amplifiers to supply essentially all of the bias currents for the other amplifiers by making use of the "matching" which exists between the 4 amplifiers which are on the same IC chip (see *Figure 84*).

The simplest inverting amplifier is the common-emitter stage. If a current source is used in place of a load resistor, a large open-loop gain can be obtained, even at low power-supply voltages. This basic stage (*Figure 1*) is used for the amplifier.

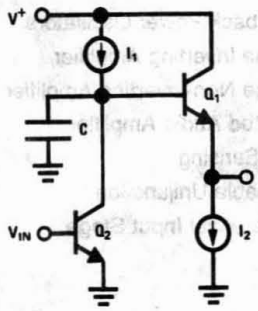

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FIGURE 1. Basic Gain Stage

All of the voltage gain is provided by the gain transistor, Q_2, and an output emitter-follower transistor, Q_1, serves to isolate the load impedance from the high impedance that exists at the collector of the gain transistor, Q_2. Closed-loop stability is guaranteed by an on-chip capacitor C = 3 pF, which provides the single dominant open-loop pole. The output emitter-follower is biased for class-A operation by the current source I_2.

This basic stage can provide an adequate open-loop voltage gain (70 dB) and has the desired large output voltage swing capability. A disadvantage of this circuit is that the DC input current, I_{IN}, is large; as it is essentially equal to the maximum output current, I_{OUT}, divided by β^2. For example, for an output current capability of 10 mA the input current would be at least 1 μA (assuming $\beta^2 = 10^4$). It would be desirable to further reduce this by adding an additional transistor to achieve an overall β^3 reduction. Unfortunately, if a transistor is added at the output (by making Q_1 a Darlington pair) the peak-to-peak output voltage swing would be somewhat reduced and if Q_2 were made a Darlington pair the DC input voltage level would be undesirably doubled.

To overcome these problems, a lateral PNP transistor has been added as shown in *Figure 2*. This connection neither reduces the output voltage swing nor raises the DC input voltage, but does provide the additional gain that was needed to reduce the input current.

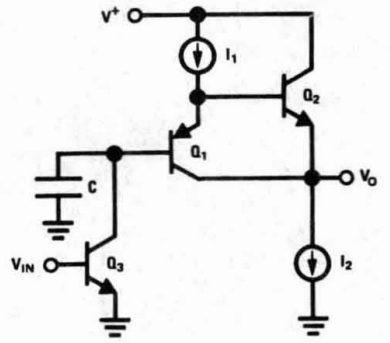

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FIGURE 2. Adding a PNP Transistor to the Basic Gain Stage

Notice that the collector of this PNP transistor, Q_1, is connected directly to the output terminal. This "bootstraps" the output impedance of Q_1 and therefore reduces the loading at the high-impedance collector of the gain transistor, Q_3.

In addition, the collector-base junction of the PNP transistor becomes forward biased under a large-signal negative output voltage swing condition. The design of this device has allowed Q_1 to convert to a vertical PNP transistor during this operating mode which causes the output to change from the class A bias to a class B output stage. This allows the amplifier to sink more current than that provided by the current source I_2, (1.3 mA) under large signal conditions.

1.2 OBTAINING A NON-INVERTING INPUT FUNCTION

The circuit of *Figure 2* has only the inverting input. A general purpose amplifier requires two input terminals to obtain both an inverting and a non-inverting input. In conventional op amp designs, an input differential amplifier provides these required inputs. The output voltage then depends upon the difference (or error) between the two input voltages. An input common-mode voltage range specification exists and, basically, input voltages are compared.

For circuit simplicity, and ease of application in single power supply systems, a non-inverting input can be provided by adding a standard IC "current-mirror" circuit directly across the inverting input terminal, as shown in *Figure 3*.

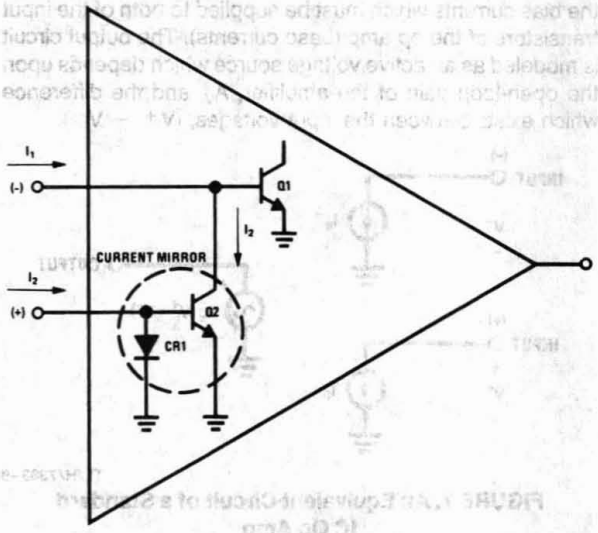

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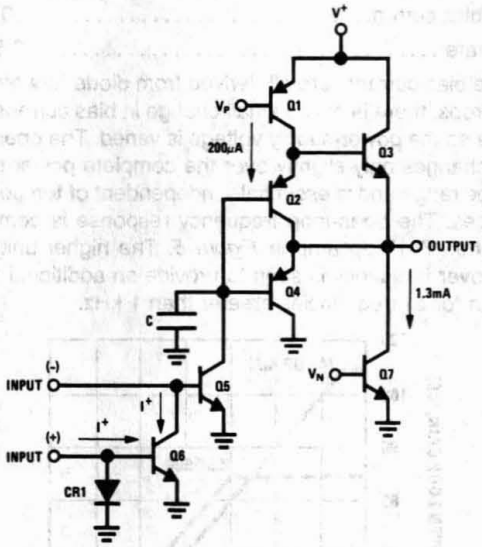
FIGURE 3. Adding a Current Mirror to Achieve a Non-Inverting Input

This operates in the current mode as now input currents are compared or differenced (this can be thought of as a Norton differential amplifier). There is essentially no input common-mode voltage range directly at the input terminals (as both inputs will bias at one diode drop above ground) but if the input voltages are converted to currents (by use of input resistors), there is then no limit to the common-mode input voltage range. This is especially useful in high-voltage comparator applications. By making use of the input resistors, to convert input voltages to input currents, all of the standard op amp applications can be realized. Many additional applications are easily achieved, especially when operating with only a single power supply voltage. This results from the built-in voltage biasing that exists at both inputs (each input biases at $+ V_{BE}$) and additional resistors are not required to provide a suitable common-mode input DC biasing voltage level. Further, input summing can be performed at the relatively low impedance level of the input diode of the current-mirror circuit.

1.3 THE COMPLETE SINGLE-SUPPLY AMPLIFIER

The circuit schematic for a single amplifier stage is shown in *Figure 4a*. Due to the circuit simplicity, four of these amplifiers can be fabricated on a single chip. One common biasing circuit is used for all of the individual amplifiers.

A new symbol for this "Norton" amplifier is shown in *Figure 4b*. This is recommended to avoid using the standard op amp symbol as the basic operation is different. The current source symbol between the inputs implies this new current-mode of operation. In addition, it signifies that current is removed from the (−) input terminal. Also, the current arrow on the (+) input lead is used to indicate that this functions as a current input. The use of this symbol is helpful in understanding the operation of the application circuits and also in doing additional design work with the LM3900.



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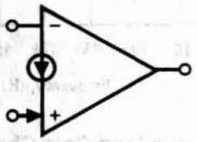
(a) Circuit Schematic



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(b) New "NORTON" Amplifier Symbol

FIGURE 4. The Amplifier Stage

The bias reference for the PNP current source, V_p which biases Q_1, is designed to cause the upper current source (200 μA) to change with temperature to give first order compensation for the β variations of the NPN output transistor, Q_3. The bias reference for the NPN "pull-down" current sink, V_n, (which biases Q_7) is designed to stabilize this current (1.3 mA) to reduce the variation when the temperature is changed. This provides a more constant pull-down capability for the amplifier over the temperature range. The transistor, Q_4, provides the class B action which exists under large signal operating conditions.

The performance characteristics of each amplifier stage are summarized below:

Power-supply voltage range ..... 4 to 36 V_{DC} or ±2 to ±18 V_{DC}

Bias current drain per amplifier stage ..... 1.3 mA_{DC}

Open loop:

- Voltage gain (R_L = 10k) ..... 70 dB
- Unity-gain frequency ..... 2.5 MHz
- Phase margin ..... 40°
- Input resistance ..... 1 MΩ
- Output resistance ..... 8 kΩ

Output voltage swing ..... (V_{CC} − 1) V_{pp}

Input bias current ..... 30 nA_{DC}

Slew rate 0.5V/μs

As the bias currents are all derived from diode forward voltage drops, there is only a small change in bias current magnitude as the power-supply voltage is varied. The open-loop gain changes only slightly over the complete power supply voltage range and is essentially independent of temperature changes. The open-loop frequency response is compared with the "741" op amp in *Figure 5*. The higher unity-gain crossover frequency is seen to provide an additional 10 dB of gain for all frequencies greater than 1 kHz.

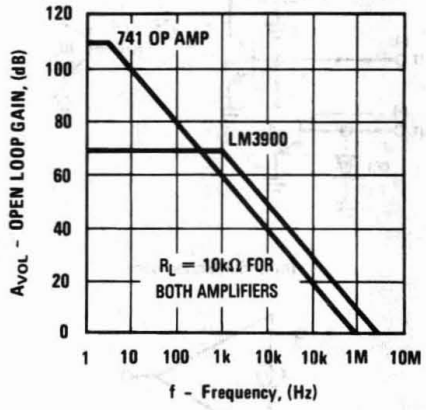

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FIGURE 5. Open-loop Gain Characteristics

The complete schematic diagram of the LM3900 is shown in *Figure 6*. The one resistor, R_5, establishes the power consumption of the circuit as it controls the conduction of transistor Q_{28}. The emitter current of Q_{28} is used to bias the NPN output class-A biasing current sources and the collector current of Q_{28} is the reference for the PNP current source of each amplifier.

The biasing circuit is initially "started" by Q_{20}, Q_{30} and CR_6. After start-up is achieved, Q_{30} goes OFF and the current flow through the reference diodes: CR_5, CR_7 and CR_8, is dependent only on $V_{BE}/(R_6 + R_7)$. This guarantees that the power supply current drain is essentially independent of the magnitude of the power supply voltage.

The input clamp for negative voltages is provided by the multi-emitter NPN transistor Q_{21}. One of the emitters of this transistor goes to each of the input terminals. The reference voltage for the base of Q_{21} is provided by R_6 and R_7 and is approximately $V_{BE}/2$.

2.0 Introduction to Applications of the LM3900

Like the standard IC op amp, the LM3900 has a wide range of applications. A new approach must be taken to design circuits with this "Norton" amplifier and the object of this note is to present a variety of useful circuits to indicate how conventional and unique new applications can be designed—especially when operating with only a single power supply voltage.

To understand the operation of the LM3900 we will compare it with the more familiar standard IC op amp. When operating on a single power supply voltage, the minimum input common-mode voltage range of a standard op amp limits the smallest value of voltage which can be applied to both inputs and still have the amplifier respond to a differential input signal. In addition, the output voltage will not swing completely from ground to the power supply voltage. The output voltage depends upon the difference between the input voltages and a bias current must be supplied to both inputs. A simplified diagram of a standard IC op amp operating from a single power supply is shown in *Figure 7*. The (+) and (−) inputs go only to current sources and therefore are free to be biased or operated at any voltage values which are within the input common-mode voltage range. The current sources at the input terminals, I_B^+ and I_B^-, represent the bias currents which must be supplied to both of the input transistors of the op amp (base currents). The output circuit is modeled as an active voltage source which depends upon the open-loop gain of the amplifier, A_V, and the difference which exists between the input voltages, ($V^+ - V^-$).

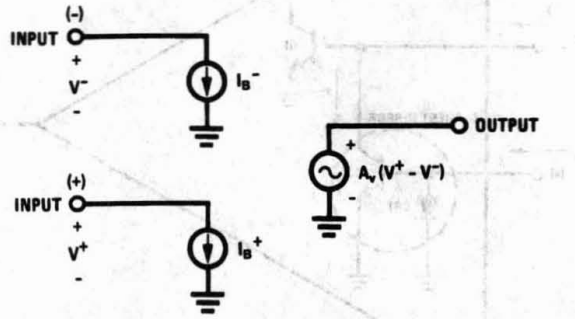

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FIGURE 7. An Equivalent Circuit of a Standard IC Op Amp

An equivalent circuit for the "Norton" amplifier is shown in *Figure 8*. The (+) and (−) inputs are both clamped by diodes to force them to be one-diode drop above ground—always! They are not free to move and the "input common-mode voltage range" directly at these input terminals is very small—a few hundred mV centered about 0.5 V_{DC}. This is

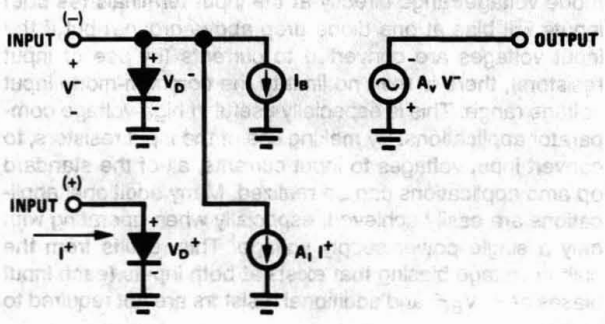

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FIGURE 8. An Equivalent Circuit of the "Norton" Amplifier

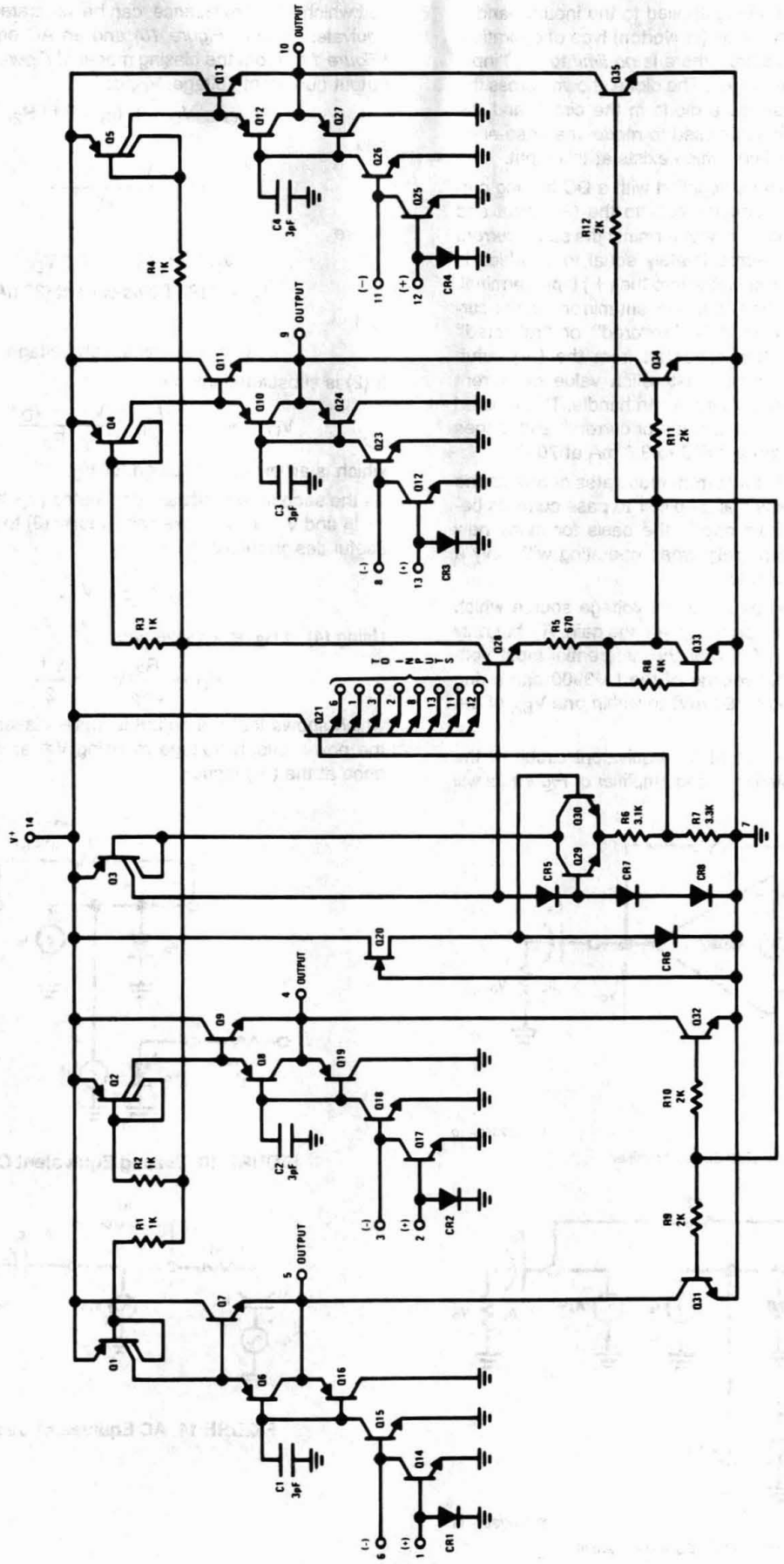


FIGURE 6. Schematic Diagram of the LM3900

why external voltages must be first converted to currents (using resistors) before being applied to the inputs—and is the basis for the current-mode (or Norton) type of operation. With external input resistors—there is *no limit* to the "input common-mode voltage range". The diode shown across the (+) input actually exists as a diode in the circuit and the diode across the (−) input is used to model the base-emitter junction of the transistor which exists at this input.

Only the (−) input must be supplied with a DC biasing current, I_B. The (+) input couples only to the (−) input and then to extract from this (−) input terminal the same current (A_I, the mirror gain, is approximately equal to 1) which is entered (by the external circuitry) into the (+) input terminal. This operation is described as a "current-mirror" as the current entering the (+) input is "mirrored" or "reflected" about ground and is then extracted from the (−) input. There is a maximum or near saturation value of current which the "mirror" at the (+) input can handle. This is listed on the data sheet as "maximum mirror current" and ranges from approximately 6 mA at 25°C to 3.8 mA at 70°C.

This fact that the (+) input current modulates or affects the (−) input current causes this amplifier to pass currents between the input terminals and is the basis for many new application circuits—especially when operating with only a single power supply voltage.

The output is modeled as an active voltage source which also depends upon the open-loop voltage gain, A_V, but only the (−) input voltage, V^-, (not the differential input voltage). Finally, the output voltage of the LM3900 can swing from essentially ground (+90 mV) to within one V_{BE} of the power supply voltage.

As an example of the use of the equivalent circuit of the LM3900, the AC coupled inverting amplifier of *Figure 9a* will be analyzed. *Figure 9b* shows the complete equivalent circuit which, for convenience, can be separated into a biasing equivalent circuit (*Figure 10*) and an AC equivalent circuit (*Figure 11*). From the biasing model of *Figure 10* we find the output quiescent voltage, V_O, is:

$$V_O = V_D^- + (I_B + I^+)\,R_2, \tag{1}$$

and

$$I^+ = \frac{V^+ - V_D^+}{R_3} \tag{2}$$

where

$$V_D^+ \cong V_D^- \cong 0.5\,V_{DC}$$

I_B = INPUT bias current (30 nA)

and

V^+ = Power supply voltage.

If (2) is substituted into (1)

$$V_O = V_D^- + \left(I_B + \frac{V^+ - V_D^+}{R_3}\right) R_2 \tag{3}$$

which is an exact expression for V_O.

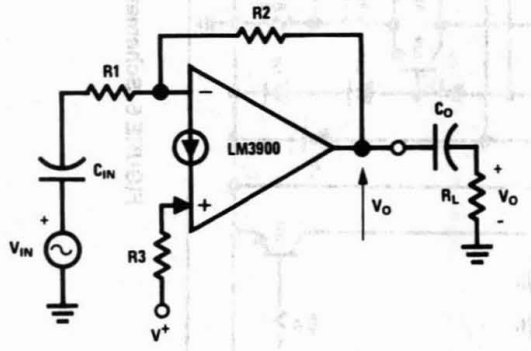
As the second term usually dominates ($V_O \gg V_D^-$) and $I^+ \gg I_B$ and $V^+ \gg V_D^+$ we can simplify (3) to provide a more useful design relationship

$$V_O \cong \frac{R_2}{R_3}\ V^+. \tag{4}$$

Using (4), if $R_3 = 2R_2$ we find

$$V_O \cong \frac{R_2}{2R_2} V^+ = \frac{V^+}{2}, \tag{5}$$

which shows that the output is easily biased to one-half of the power supply voltage by using V^+ as a biasing reference at the (+) input.



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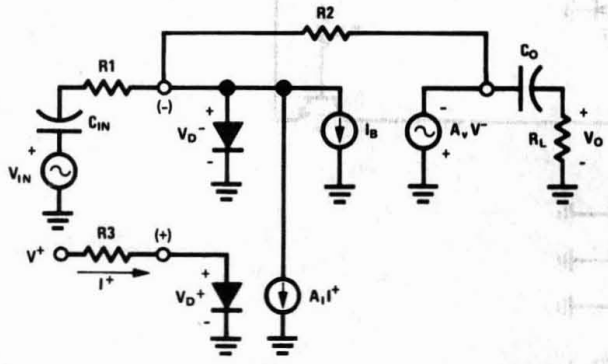
(a) A Typical Biased Amplifier



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(b) Using the LM3900 Equivalent Circuit

FIGURE 9. Applying the LM3900 Equivalent Circuit

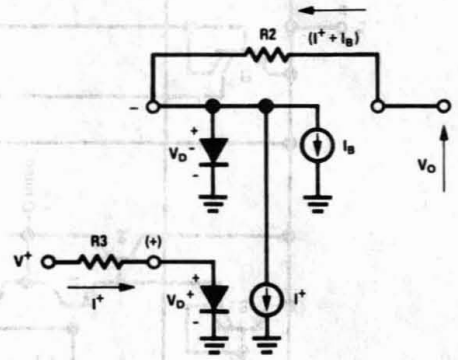

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FIGURE 10. Biasing Equivalent Circuit

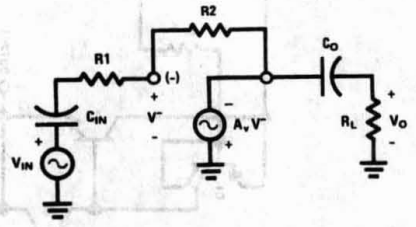

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FIGURE 11. AC Equivalent Circuit

The AC equivalent circuit of *Figure 11* is the same as that which would result if a standard IC op amp were used with the (+) input grounded. The closed-loop voltage gain A_{VCL}, is given by:

$$A_{VCL} \equiv \frac{V_O}{V_{IN}} \cong -\frac{R_2}{R_1} \quad (6)$$

if A_V (open-loop) $> \frac{R_2}{R_1}$.

The design procedure for an AC coupled inverting amplifier using the LM3900 is therefore to first select R_1, C_{IN}, R_2, and C_O as with a standard IC op amp and then to simply add $R_3 = 2R_2$ as a final biasing consideration. Other biasing techniques are presented in the following sections of this note. For the switching circuit applications, the biasing model of *Figure 10* is adequate to predict circuit operation.

Although the LM3900 has four independent amplifiers, the use of the label "¼LM3900" will be shortened to simply "LM3900" for the application drawings contained in this note.

3.0 Designing AC Amplifiers

The LM3900 readily lends itself to use as an AC amplifier because the output can be biased to any desired DC level within the range of the output voltage swing and the AC gain is independent of the biasing network. In addition, the single power supply requirement makes the LM3900 attractive for any low frequency gain application. For lowest noise performance, the (+) input should be grounded (*Figure 9a*) and the output will then bias at $+V_{BE}$. Although the LM3900 is not suitable as an ultra low noise tape pre-amp, it is useful in most other applications. The restriction to only shunt feedback causes a small input impedance. Transducers which can be loaded can operate with this low input impedance. The noise degradation which would result from the use of a large input resistor limits the usefulness where low noise and high input impedance are both required.

3.1 SINGLE POWER SUPPLY BIASING

The LM3900 can be biased in several different ways. The circuit in *Figure 12* is a standard inverting AC amplifier which has been biased from the same power supply which is used to operate the amplifier. (The design of this amplifier has been presented in the previous section). Notice that if AC ripple voltages are present on the V^+ power supply line they will couple to the output with a "gain" of ½. To eliminate this, one source of ripple filtered voltage can be provided and then used for many amplifiers. This is shown in the next section.

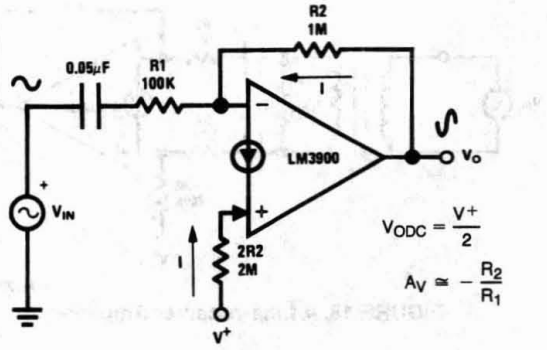

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FIGURE 12. Inverting AC Amplifier Using Single-Supply Biasing

3.2 A NON-INVERTING AMPLIFIER

The amplifier in *Figure 13* shows both a non-inverting AC amplifier and a second method for DC biasing. Once again the AC gain of the amplifier is set by the ratio of feedback resistor to input resistor. The small signal impedance of the diode at the (+) input should be added to the value of R_1 when calculating gain, as shown in *Figure 13*.

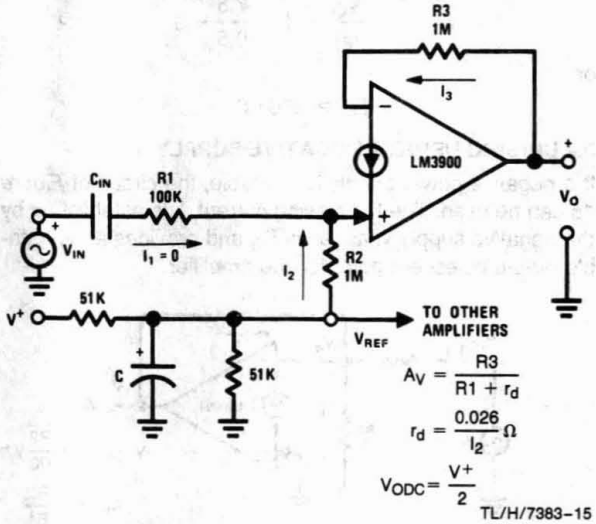

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FIGURE 13. Non-Inverting AC Amplifier Using Voltage Reference Biasing

By making $R_2 = R_3$, V_{ODC} will be equal to the reference voltage which is applied to the resistor R_2. The filtered $V^+/2$ reference shown can also be used for other amplifiers.

3.3 "N V_{BE}" BIASING

A third technique of output DC biasing is best described as the "N V_{BE}" method. This technique is shown in *Figure 14* and is most useful with inverting AC amplifier applications.

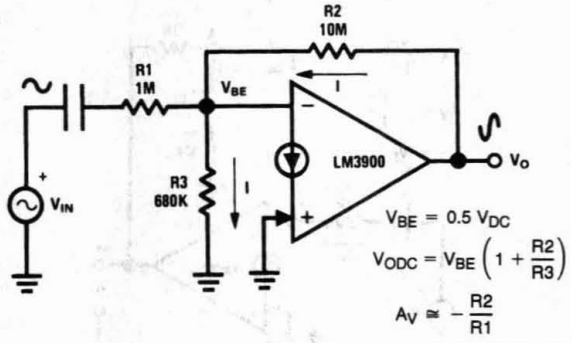

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FIGURE 14. Inverting AC Amplifier Using N V_{BE} Biasing

The input bias voltage (V_{BE}) at the inverting input establishes a current through resistor R_3 to ground. This current must come from the output of the amplifier. Therefore, V_O must rise to a level which will cause this current to flow through R_2. The bias voltage, V_O, may be calculated from the ratio of R_2 to R_3 as follows:

$$V_{ODC} = V_{BE}\left(1 + \frac{R_2}{R_3}\right)$$

When NV_{BE} biasing is employed, values for resistors R_1 and R_2 are first established and then resistor R_3 is added to provide the desired DC output voltage.

For a design example (*Figure 14*), a Z in = 1M and $A_v \cong 10$ are required.

Select $R_1 = 1M$.

Calculate $R_2 \cong A_v R_1 = 10M$.

To bias the output voltage at 7.5 V_{DC}, R_3 is found as:

$$R_3 = \frac{R_2}{\frac{V_O}{V_{BE}} - 1} = \frac{10M}{\frac{7.5}{0.5} - 1}$$

or

$$R_3 \cong 680\ k\Omega.$$

3.4 BIASING USING A NEGATIVE SUPPLY

If a negative power supply is available, the circuit of *Figure 15* can be used. The DC biasing current, I, is established by the negative supply voltage via R_3 and provides a very stable output quiescent point for the amplifier.

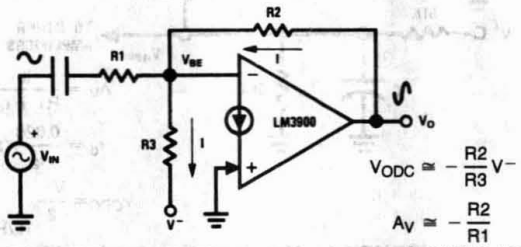

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FIGURE 15. Negative Supply Biasing

3.5 OBTAINING HIGH INPUT IMPEDANCE AND HIGH GAIN

For the AC amplifiers which have been presented, a designer is able to obtain either high gain or high input impedance with very little difficulty. The application which requires both and still employs only one amplifier presents a new problem. This can be achieved by the use of a circuit similar to the one shown in *Figure 16*. When the A_v from the input to point A is unity ($R_1 = R_3$), the A_v of the complete stage will be set by the voltage divider network composed of R_4, R_5, and C_2. As the value of R_5 is decreased, the A_v of the stage will approach the AC open loop limit of the amplifier. The insertion of capacitor C_2 allows the DC bias to be controlled by the series combination of R_3 and R_4 with no effect from R_5. Therefore, R_2 may be selected to obtain the desired output DC biasing level using any of the methods which have been discussed. The circuit in *Figure 16* has an input impedance of 1M and a gain of 100.

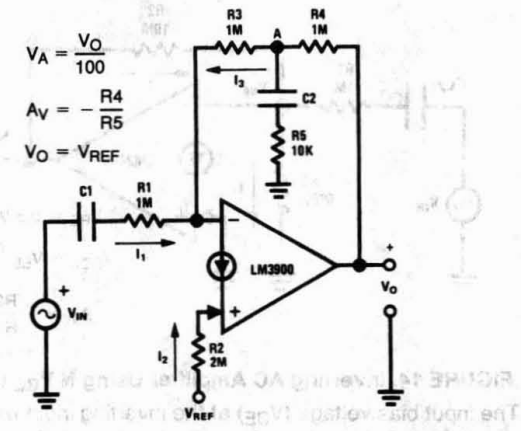

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FIGURE 16. A High Z_{IN} High Gain Inverting AC Amplifier

3.6 AN AMPLIFIER WITH A DC GAIN CONTROL

A DC gain control can be added to an amplifier as shown in *Figure 17*. The output of the amplifier is kept from being driven to saturation as the DC gain control is varied by providing a minimum biasing current via R_3. For maximum gain, CR_2 is OFF and both the current through R_2 and R_3 enter the (+) input and cause the output of the amplifier to bias at approximately 0.6 V^+. For minimum gain, CR_2 is ON and only the current through R_3 enters the (+) input to bias the output at approximately 0.3 V^+. The proper output bias for large output signal accommodation is provided for the maximum gain situation. The DC gain control input ranges from 0 V_{DC} for minimum gain to less than 10 V_{DC} for maximum gain.

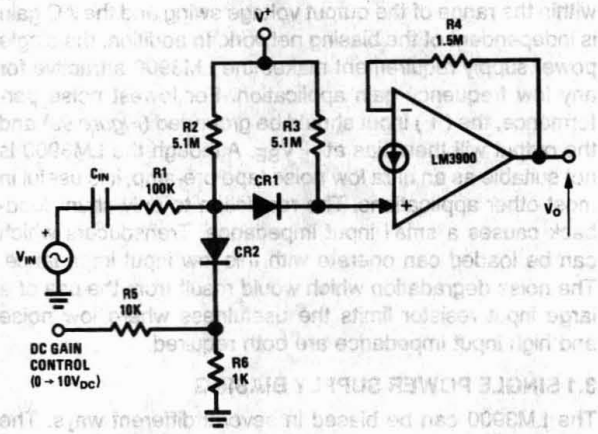

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FIGURE 17. An Amplifier with a DC Gain Control

3.7 A LINE-RECEIVER AMPLIFIER

The line-receiver amplifier is shown in *Figure 18*. The use of both inputs cancels out common-mode signals. The line is terminated by R_{LINE} and the larger input impedance of the amplifier will not affect this matched loading.

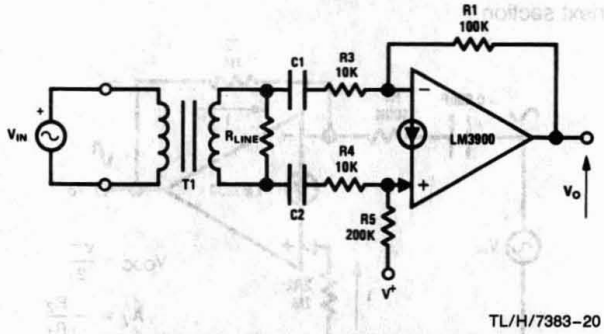

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FIGURE 18. A Line-receiver Amplifier

4.0 Designing DC Amplifiers

The design of DC amplifiers using the LM3900 tends to be more difficult than the design of AC amplifiers. These difficulties occur when designing a DC amplifier which will operate from only a single power supply voltage and yet provide an output voltage which goes to zero volts DC and also will accept input voltages of zero volts DC. To accomplish this, the inputs must be biased into the linear region ($+V_{BE}$) with DC input signals of zero volts and the output must be modified if operation to actual ground (and not V_{SAT}) is required. Therefore, the problem becomes one of determining what type of network is necessary to provide an output voltage (V_O) equal to zero when the input voltage (V_{IN}) is equal to zero. (See also section 10.15, "adding a Differential Input Stage").

We will start with a careful evaluation of what actually takes place at the amplifier inputs. The mirror circuit demands that the current flowing into the positive input (+) be equaled by a current flowing into the negative input (−). The difference between the current demanded and the current provided by an external source must flow in the feedback circuit. The output voltage is then forced to seek the level required to cause this amount of current to flow. If, in the steady state condition $V_O = V_{IN} = 0$, the amplifier will operate in the desired manner. This condition can be established by the use of common-mode biasing at the inputs.

4.1 USING COMMON-MODE BIASING FOR $V_{IN} = 0\ V_{DC}$

Common-mode biasing is achieved by placing equal resistors between the amplifier input terminals and the supply voltage (V+), as shown in *Figure 19*. When V_{IN} is set to 0 volts the circuit can be modeled as shown in *Figure 20*,

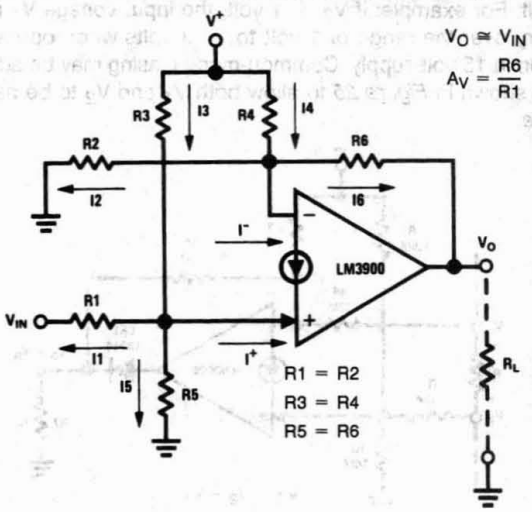

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FIGURE 19. A DC Amplifier Employing Common-mode Biasing

where:

$$R_{EQ_1} = R_1 \parallel R_5,$$

$$R_{EQ_2} = R_2 \parallel R_6,$$

and

$$R_3 = R_4.$$

Because the current mirror demands that the two current sources be equal, the current in the two equivalent resistors must be identical.

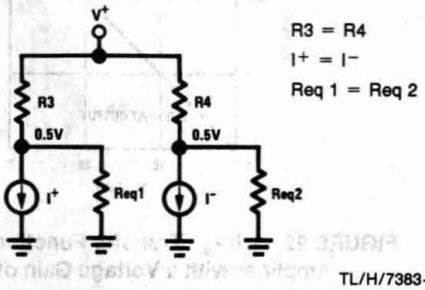

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FIGURE 20. An Ideal Circuit Model of a DC Amplifier with Zero Input Voltage

If this is true, both R_2 and R_6 must have a voltage drop of 0.5 volt across them, which forces V_O to go to $V_{O\ MIN}$ (V_{SAT}).

4.2 ADDING AN OUTPUT DIODE FOR $V_O = 0\ V_{DC}$

For many applications a $V_{O\ MIN}$ Of 100 mV may not be acceptable. To overcome this problem a diode can be added between the output of the amplifier and the output terminal (*Figure 21*).

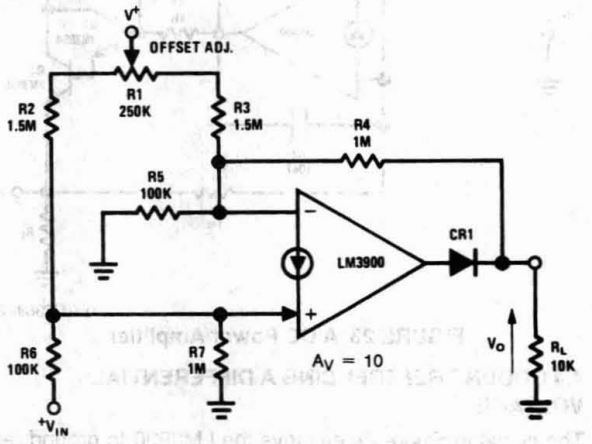

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FIGURE 21. A Non-inverting DC Amplifier with Zero Volts Output for Zero Volts Input

The function of the diode is to provide a DC level shift which will allow V_O to go to ground. With a load impedance (R_L) connected, V_O becomes a function of the voltage divider formed by the series connection of R_4 and R_L.

If $R_4 = 100\ R_L$, then $V_{O\ MIN} = \frac{0.5\ R_L}{101\ R_L}$,

or $V_{O\ MIN} \cong 5\ mV_{DC}$.

An offset voltage adjustment can be added as shown (R_1) to adjust V_O to $0V_{DC}$ with $V_{IN} = 0\ V_{DC}$.

The voltage transfer functions for the circuit in *Figure 21*, both with and without the diode, are shown in *Figure 22*. While the diode greatly improves the operation around 0 volts, the voltage drop across the diode will reduce the peak output voltage swing of the state by approximately 0.5 volt.

When using a DC amplifier similar to the one in *Figure 21*, the load impedance should be large enough to avoid excessively loading the amplifier. The value of R_L may be significantly reduced by replacing the diode with an NPN transistor.

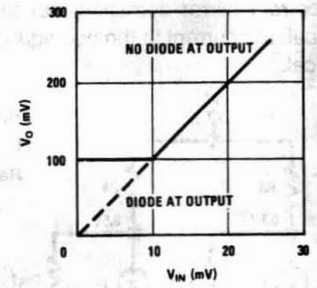

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FIGURE 22. Voltage Transfer Function for a DC Amplifier with a Voltage Gain of 10

4.3 A DC COUPLED POWER AMPLIFIER ($I_L \leq 3$ AMPS)

The LM3900 may be used as a power amplifier by the addition of a Darlington pair at the output. The circuit shown in *Figure 23* can deliver in excess of 3 amps to the load when the transistors are properly mounted on heat sinks.

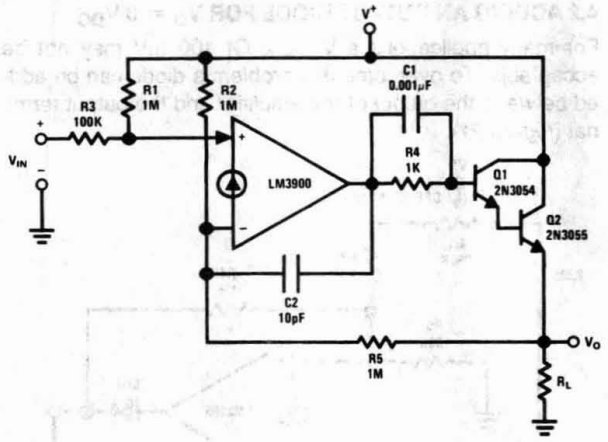

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FIGURE 23. A DC Power Amplifier

4.4 GROUND REFERENCING A DIFFERENTIAL VOLTAGE

The circuit in *Figure 24* employs the LM3900 to ground reference a DC differential input voltage. Current I_1 is larger

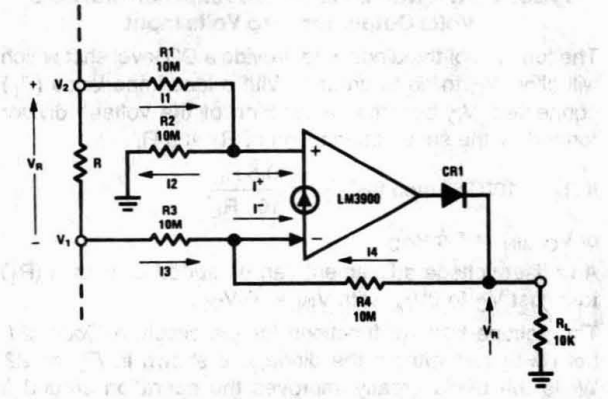

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FIGURE 24. Ground Referencing a Differential Input DC Voltage

than current I_3 by a factor proportional to the differential voltage, V_R. The currents labeled on *Figure 24* are given by:

$$I_1 = \frac{V_1 + V_R - \phi}{R_1}$$

$$I_2 = \phi/R_2$$

$$I_3 = \frac{(V_1 - \phi)}{R_3}$$

and

$$I_4 = \frac{V_O - \phi}{R_4}$$

where

$\phi \equiv V_{BE}$ at either input terminal of the LM3900.

Since the input current mirror demands that

$$I^- = I^+;$$

and

$$I^+ = I_1 - I_2$$

and

$$I^- = I_3 + I_4$$

Therefore

$$I_4 = I_1 - I_2 - I_3.$$

Substituting in from the above equation

$$\frac{V_O - \phi}{R_4} = \frac{(V_1 + V_R - \phi)}{R_1} - \frac{(\phi)}{R_2} - \frac{(V_1 - \phi)}{R_3}$$

and as $R_1 = R_2 = R_3 = R_4$

$$V_O = (V_1 + V_R - \phi) - (\phi) - V_1 + \phi + \phi$$

or

$$V_O = V_R.$$

The resistors are kept large to minimize loading. With the 10 MΩ resistors which are shown on the figure, an error exists at small values of V_1 due to the input bias current at the (−) input. For simplicity this has been neglected in the circuit description. Smaller R values reduce the percentage error or the bias current can be supplied by an additional amplifier (see Section 10.7.1).

For proper operation, the differential input voltage must be limited to be within the output dynamic voltage range of the amplifier and the input voltage V_2 must be greater than 1 volt. For example; if $V_2 = 1$ volt, the input voltage V_1 may vary over the range of 1 volt to −13 volts when operating from a 15 volt supply. Common-mode biasing may be added as shown in *Figure 25* to allow both V_1 and V_2 to be negative.

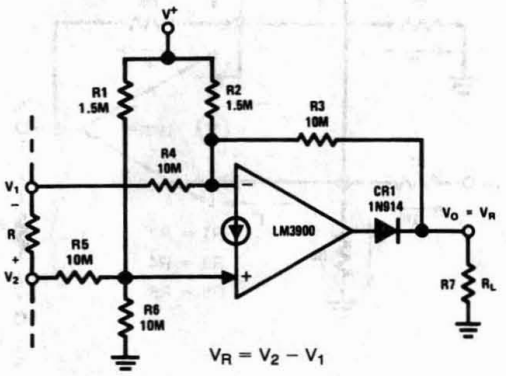

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FIGURE 25. A Network to Invert and to Ground Reference a Negative DC Differential Input Voltage

4.5 A UNITY GAIN BUFFER AMPLIFIER

The buffer amplifier with a gain of one is the simplest DC application for the LM3900. The voltage applied to the input (*Figure 26*) will be reproduced at the output. However, the input voltage must be greater than one V_{BE} but less than the maximum output swing. Common-mode biasing can be added to extend V_{IN} to 0 V_{DC}, if desired.

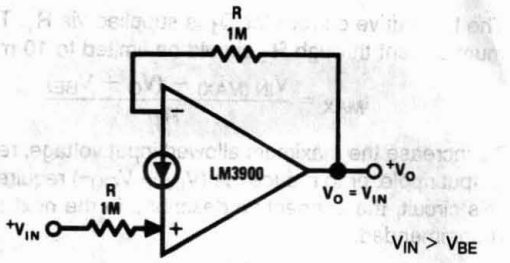

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FIGURE 26. A Unity-gain DC Buffer Amplifier

5.0 Designing Voltage Regulators

Many voltage regulators can be designed which make use of the basic amplifier of the LM3900. The simplest is shown in *Figure 27a* where only a Zener diode and a resistor are added. The voltage at the (–) input (one $V_{BE} \cong 0.5\ V_{DC}$) appears across R and therefore a resistor value of 510Ω will cause approximately 1 mA of bias current to be drawn through the Zener. This biasing is used to reduce the noise output of the Zener as the 30 nA input current is too small for proper Zener biasing. To compensate for a positive temperature coefficient of the Zener, an additional resistor can be added, R_2, (*Figure 27b*) to introduce an arbitrary number, N, of "effective" V_{BE} drops into the expression for the output voltage. The negative temperature coefficient of these diodes will also be added to temperature compensate the DC output voltage. For a larger output current, an emitter follower (Q_1 of *Figure 27c*) can be added. This will multiply the 10 mA (max.) output current of the LM3900 by the β of the added transistor. For example, a $\beta = 30$ will provide a max. load current of 300 mA. This added transistor also reduces the output impedance. An output frequency compensation capacitor is generally not required but may be added, if desired, to reduce the output impedance at high frequencies.

The DC output voltage can be increased and still preserve the temperature compensation of *Figure 27b* by adding resistors R_A and R_B as shown in *Figure 27d*. This also can be accomplished without the added transistor, Q_1. The unregulated input voltage, which is applied to pin 14 of the LM3900 (and to the collector of Q_1, if used) must always exceed the regulated DC output voltage by approximately 1V, when the unit is not current boosted or approximately 2V when the NPN current boosting transistor is added.

5.1 REDUCING THE INPUT-OUTPUT VOLTAGE

The use of an external PNP transistor will reduce the required ($V_{IN} - V_{OUT}$) to a few tenths of a volt. This will depend on the saturation characteristics of the external transistor at the operating current level. The circuit, shown in *Figure 28*, uses the LM3900 to supply base drive to the PNP transistor. The resistors R_1 and R_2 are used to allow the output of the amplifier to turn OFF the PNP transistor. It is important that pin 14 of the LM3900 be tied to the $+V_{IN}$ line to allow this OFF control to properly operate. Larger voltages are permissible (if the base-emitter junction of Q_1 is prevented from entering a breakdown by a shunting diode, for example), but smaller voltages will not allow the output of the amplifier to raise enough to give the OFF control.

The resistor, R_3, is used to supply the required bias current for the amplifier and R_4 is again used to bias the Zener diode. Due to a larger gain, a compensation capacitor, C_O, is required. Temperature compensation could be added as was shown in *Figure 27b*.

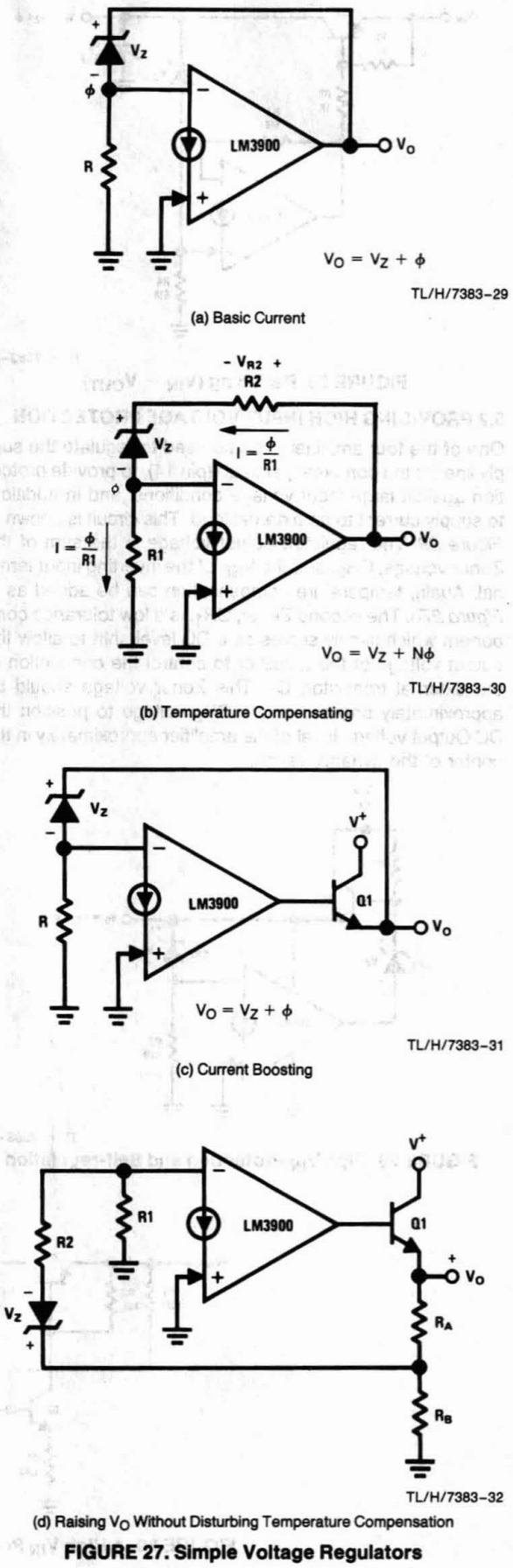

FIGURE 27. Simple Voltage Regulators

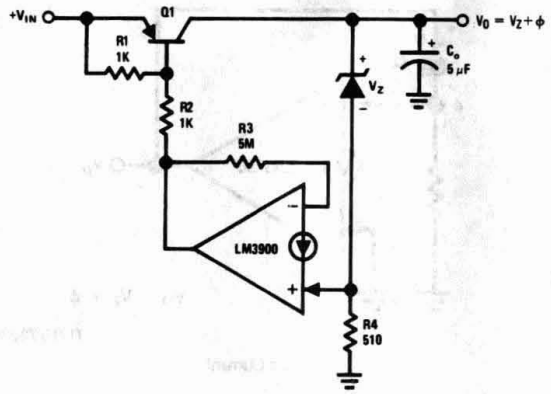

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FIGURE 28. Reducing ($V_{IN} - V_{OUT}$)

5.2 PROVIDING HIGH INPUT VOLTAGE PROTECTION

One of the four amplifiers can be used to regulate the supply line for the complete package (pin 14), to provide protection against large input voltage conditions, and in addition, to supply current to an external load. This circuit is shown in *Figure 29*. The regulated output voltage is the sum of the Zener voltage, CR_2, and the V_{BE} of the inverting input terminal. Again, temperature compensation can be added as in *Figure 27b*. The second Zener, CR_1, is a low tolerance component which simply serves as a DC level shift to allow the output voltage of the amplifier to control the conduction of the external transistor, Q_1. This Zener voltage should be approximately one-half of the CR_2 voltage to position the DC Output voltage level of the amplifier approximately in the center of the dynamic range.

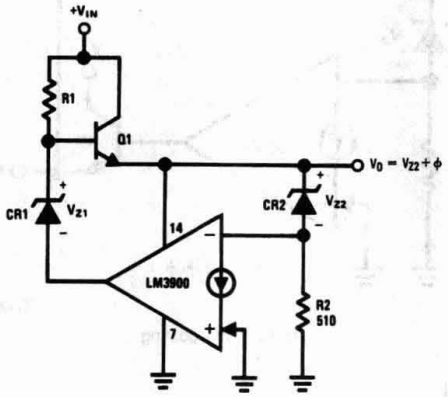

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FIGURE 29. High V_{IN} Protection and Self-regulation

The base drive current for Q_1 is supplied via R_1. The maximum current through R_1 should be limited to 10 mA as

$$I_{MAX} = \frac{V_{IN\,(MAX)} - (V_O + V_{BE})}{R_1}$$

To increase the maximum allowed input voltage, reduce the output ripple, or to reduce the ($V_{IN} - V_{OUT}$) requirements of this circuit, the connection described in the next section is recommended.

5.3 HIGH INPUT VOLTAGE PROTECTION AND LOW ($V_{IN} - V_{OUT}$)

The circuit shown in *Figure 30* basically adds one additional transistor to the circuit of *Figure 29* to improve the performance. In this circuit both transistors (Q_1 and Q_2) absorb any high input voltages (and therefore need to be high voltage devices) without any increases in current (as with R_1 of *Figure 29*). The resistor R_1 (of *Figure 30*) provides a "start-up" current into the base of Q_2.

A new input connection is shown on this regulator (the type on *Figure 29* could also be used) to control the DC output voltage. The Zener is biased via R_4 (at approximately 1 mA). The resistors R_3 and R_6 provide gain (non-inverting) to allow establishing V_O at any desired voltage larger than V_Z. Temperature compensation of either sign (±TC) can be obtained by shunting a resistor from either the (+) input to ground (to add + TC to V_O) or from the (−) input to ground (to add −TC to V_O). To understand this, notice that the resistor, R, from the (+) input to ground will add $-N\,V_{BE}$ to V_O where

$$N = 1 + \frac{R_3}{R},$$

and V_{BE} is the base emitter voltage of the transistor at the (+) input. This then also adds a positive temperature change at the output to provide the desired temperature correction.

The added transistor, Q_2, also increases the gain (which reduces the output impedance) and if a power device is used for Q_1 large load currents (amps) can be supplied. This regulator also supplies the power to the other three amplifiers of the LM3900.

5.4 REDUCING INPUT VOLTAGE DEPENDENCE AND ADDING SHORT-CIRCUIT PROTECTION

To reduce ripple feedthrough and input voltage dependence, diodes can be added as shown in *Figure 31* to drop-out the start once start-up has been achieved. Short-circuit protection can also be added as shown in *Figure 32*.

The emitter resistor of Q_2 will limit the maximum current of Q_2 to $(V_O - 2\,V_{BE})/R_5$.

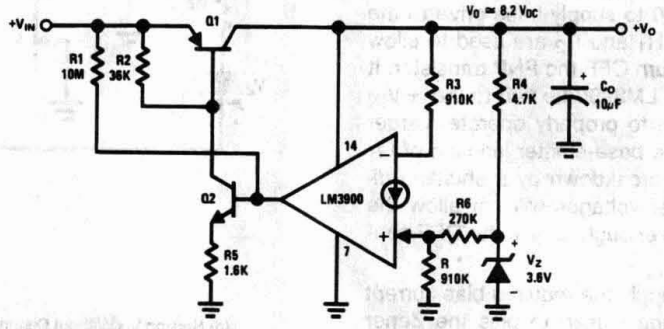

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FIGURE 30. A High V_{IN} Protected, Low ($V_{IN} - V_{OUT}$) Regulator

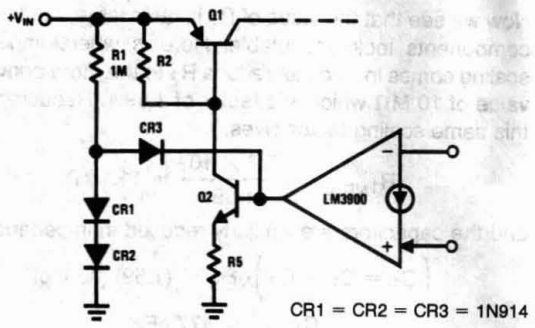

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FIGURE 31. Reducing V_{IN} Dependence

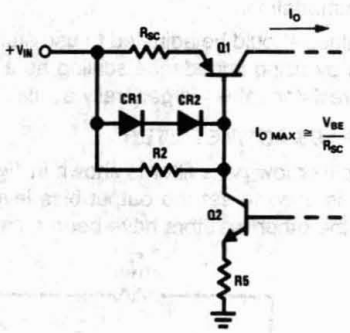

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FIGURE 32. Adding Short-circuit Current Limiting

6.0 Designing RC Active Filters

Recent work in RC active filters has shown that the performance characteristics of multiple-amplifier filters are relatively insensitive to the tolerance of the RC components used. This makes the performance of these filters easier to control in production runs. In many cases where gain is needed in a system design it is now relatively easy to also get frequency selectivity.

The basis of active filters is a gain stage and therefore a multiple amplifier product is a valuable addition to this application area. When additional amplifiers are available, less component selection and trimming is needed as the performance of the filter is less disturbed by the tolerance and temperature drifts of the passive components.

The *passive components* do *control* the *performance* of the filter and for this reason carbon composition resistors are useful mainly for room temperature breadboarding or for final trimming of the more stable metal film or wire-wound resistors. Capacitors present more of a problem in range of values available, tolerance and stability (with temperature, frequency, voltage and time). For example, the disk ceramic type of capacitors are generally not suited to active filter applications due to their relatively poor performance.

The impedance level of the passive components can be scaled without (theoretically) affecting the filter characteristics. In an actual circuit; if the resistor values become too small ($\leq$10 kΩ) an excessive loading may be placed on the output of the amplifier which will reduce gain or actually exceed either the output current or the package dissipation capabilities of the amplifier. This can easily be checked by calculating (or noticing) the impedance which is presented to the output terminal of the amplifier at the highest operating frequency. A second limit sets the upper range of impedance levels, this is due to the DC bias currents ($\cong$30 nA) and the input impedance of actual amplifiers. The solution to this problem is to reduce the impedance levels of the passive components ($\leq$10 MΩ). In general, better performance is obtained with relatively low passive component impedance levels and in filters which do not demand high gain, high Q (Q $\geq$ 50) and high frequency (f_o > 1 kHz) simultaneously.

A measure of the effects of changes in the values of the passive components on the filter performance has been given by "sensitivity functions". These assume infinite amplifier gain and relate the percentage change in a parameter of the filter, such as center frequency (f_o), Q, or gain to a percentage change in a particular passive component. Sensitivity functions which are small are desirable (as 1 or ½).

Negative signs simply mean an increase in the value of a passive component causes a decrease in that filter performance characteristic. As an example, if a bandpass filter listed the following sensitivity factor

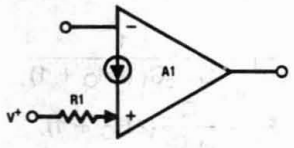
$$S^{\omega_o}_{C_3} = -\frac{1}{2}.$$

This states that "if C_3 were to increase by 1%, the center frequency, ω_o, would decrease by 0.5%." Sensitivity functions are tabulated in the reference listed at the end of this section and will therefore not be included here.

A brief look at low pass, high pass and bandpass filters will indicate how the LM3900 can be applied in these areas. A recommended text (which provided these circuts) is, "Operational Amplifiers", Tobey, Graeme, and Huelsman, McGraw Hill, 1971.

6.1 BIASING THE AMPLIFIERS

Active filters can be easily operated off of a single power supply when using these multiple single supply amplifiers. The general technique is to use the (+) input to accomplish the biasing function. The power supply voltage, V^+, is used as the DC reference to bias the output voltage of each amplifier at approximately $V^+/2$. As shown in *Figure 33*, undesired AC components on the power supply line may have to



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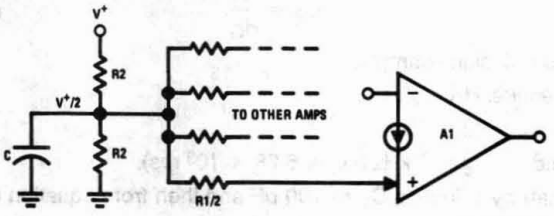
(a) Biasing From a "Noise-Free" Power Supply



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(b) Biasing From a "Noisy" Power Supply

FIGURE 33. Biasing Considerations

be removed (by a filter capacitor, *Figure 33b*) to keep the filter output free of this noise. One filtered DC reference can generally be used for all of the amplifiers as there is essentially no signal feedback to this bias point.

In the filter circuits presented here, all amplifiers will be biased at $V^+/2$ to allow the maximum AC voltage swing for any given DC power supply voltage. The inputs to these filters will also be assumed at a DC level of $V^+/2$ (for those which are direct coupled).

6.2 A HIGH PASS ACTIVE FILTER

A single amplifier high pass RC active filter is shown in *Figure 34*. This circuit is easily biased using the (+) input of the LM3900. The resistor, R_3, can be simply made equal to R_2 and a bias reference of $V^+/2$ will establish the output Q point at this value ($V^+/2$). The input is capacitively coupled (C_1) and there are therefore no further DC biasing problems.

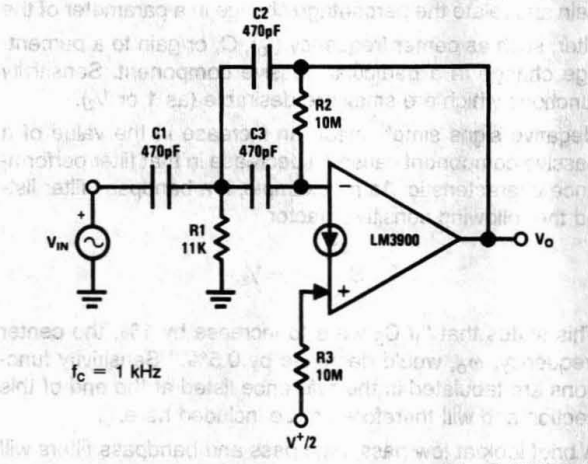

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FIGURE 34. A High Pass Active Filter

The design procedure for this filter is to select the pass band gain, H_O, the Q and the corner frequency, f_c. A Q value of 1 gives only a slight peaking near the bandedge (<2 dB) and smaller Q values decrease this peaking. The slope of the skirt of this filter is 12 dB/octave (or 40 dB/decade). If the gain, H_O, is unity all capacitors have the same value. The design proceeds as:

Given: H_O, Q and $\omega_c = 2\pi f_c$

To find: R_1, R_2, C_1, C_2, and C_3

let $C_1 = C_3$ and choose a convenient starting value.

Then:

$$R_1 = \frac{1}{Q\,\omega_c C_1\,(2H_O + 1)} \qquad (1)$$

$$R_2 = \frac{Q}{\omega_c C_1}\,(2\,H_O + 1), \qquad (2)$$

and

$$C_2 = \frac{C_1}{H_O}. \qquad (3)$$

As a design example,

Require: $H_O = 1$,

$Q = 10$,

and $f_c = 1$ kHz ($\omega_c = 6.28 \times 10^3$ rps).

Start by selecting $C_1 = 300$ pF and then from equation (1)

$$R_1 = \frac{1}{(10)\,(6.28 \times 10^3)\,(3 \times 10^{-10})\,(3)}$$

$$R_1 = 17.7\ \text{k}\Omega$$

and from equation (2)

$$R_2 = \frac{10 \quad (3)}{(6.28 \times 10^3)\,(3 \times 10^{-10})}$$

$$R_2 = 15.9\ \text{M}\Omega$$

and from equation (3)

$$C_2 = \frac{C_1}{1} = C_1$$

Now we see that the value of R_2 is quite large; but the other components look acceptable. Here is where impedance scaling comes in. We can reduce R_2 to the more convenient value of 10 MΩ which is a factor of 1.59:1. Reducing R_1 by this same scaling factor gives:

$$R_{1\text{NEW}} = \frac{17.7 \times 10^3}{1.59} = 11.1\ \text{k}\Omega$$

and the capacitors are similarly reduced in impedance as:

$$\left(C_1 = C_2 = C_3\right)_{\text{NEW}} = (1.59)\,(300)\ \text{pF}$$

$$C_{1\text{NEW}} = 477\ \text{pF}.$$

To complete the design, R_3 is made equal to R_2 (10 MΩ) and a V_{REF} of $V^+/2$ is used to bias the output for large signal accommodation.

Capacitor values should be adjusted to use standard valued components by using impedance scaling as a wider range of standard resistor values is generally available.

6.3 A LOW PASS ACTIVE FILTER

A single amplifier low pass filter is shown in *Figure 35*. The resistor, R_4, is used to set the output bias level and is selected after the other resistors have been established.

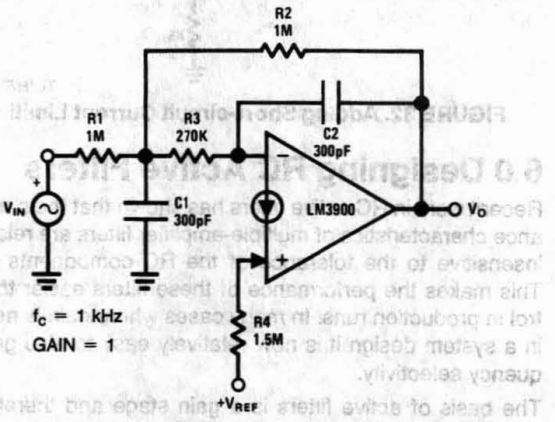

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FIGURE 35. A Low Pass Active Filter

The design procedure is as follows:

Given: H_O, Q, and $\omega_c = 2\pi f_c$

To find: R_1, R_2, R_3, R_4, C_1, and C_2

Let C_1 be a convenient value,

then

$$C_2 = KC_1 \qquad (4)$$

where K is a constant which can be used to adjust component values. For example, with $K = 1$, $C_1 = C_2$. Larger values of K can be used to reduce R_2 and R_3 at the expense of a larger value for C_2.

$$R_1 = \frac{R_2}{H_O}, \qquad (5)$$

$$R_2 = \frac{1}{2Q\,\omega_C\,C_1}\left[1 \pm \sqrt{1 + \frac{4Q^2\,(H_O + 1)}{K}}\right] \qquad (6)$$

and

$$R_3 = \frac{1}{\omega_c{}^2 C_1{}^2 R_2 (K)} \qquad (7)$$

As a design example:

Require: $H_O = 1$,

$Q = 1$,

and $f_c = 1$ kHz ($\omega_c = 6.28 \times 10^3$ rps).

Start by selecting $C_1 = 300$ pF and K = 1 so C_2 is also 300 pF (equation 4).

Now from equation (6)

$$R_2 = \frac{1}{2\,(1)\,(6.28 \times 10^3)\,(3 \times 10^{-10})}\left[1 \pm \sqrt{1 + 4\,(2)}\right]$$

$R_2 = 1.06\ M\Omega$

Then from equation (5)

$$R_1 = R_2 = 1.06\ M\Omega$$

and finally from equation (7)

$$R_3 = \frac{1}{(6.28 \times 10^3)^2\,(3 \times 10^{-10})^2\,(1.06 \times 10^6)\,(1)}$$

$R_3 = 266\ k\Omega$.

To select R_4, we assume the DC input level is 7 V_{DC} and the DC output of this filter is to also be 7 V_{DC}. This gives us the circuit of *Figure 36*. Notice that $H_O = 1$ gives us not only

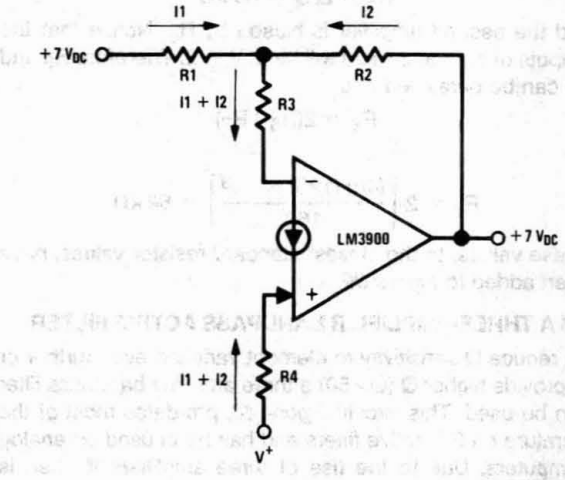

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FIGURE 36. Biasing the Low Pass Filter

equal resistor values (R_1 and R_2) but simplifies the DC bias calculation as $I_1 = I_2$ and we have a DC amplifier with a gain of −1 (so if the DC input voltage increases 1 V_{DC} the output voltage decreases 1 V_{DC}). The resistors R_1 and R_2 are in parallel so that the circuit simplifies to that shown in *Figure 37* where the actual resistance values have been added. The resistor R_4 is given by

$$R_4 = 2\left(\frac{R_1}{2} + R_3\right) + R_3$$

or, using values

$$R_4 = 2\left(\frac{1\ M\Omega}{2} + 266k\right) \cong 1.5\ M\Omega$$

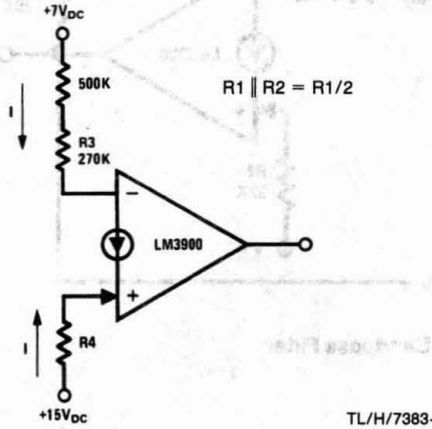

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FIGURE 37. Biasing Equivalent Circuit

6.4 A SINGLE-AMPLIFIER BANDPASS ACTIVE FILTER

The bandpass filter is perhaps the most interesting. For low frequencies, low gain and low Q (≤10) requirements, a single amplifier realization can be used. A one amplifier circuit is shown in *Figure 38* and the design procedure is as follows;

Given: H_O, Q and $\omega_o = 2\pi f$.

To find: R_1, R_2, R_3, R_4, C_1 and C_2.

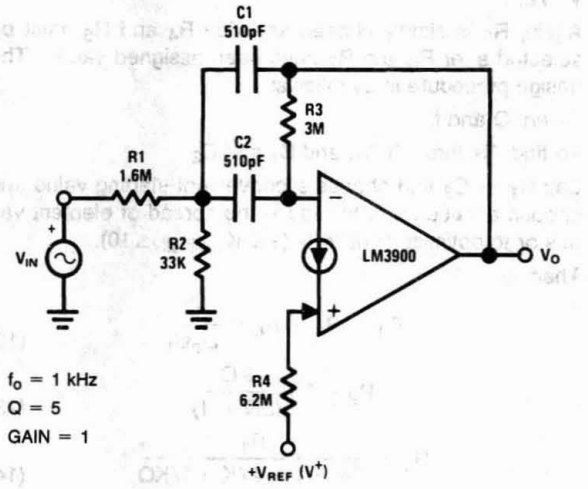

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FIGURE 38. A One Op Amp Bandpass Filter

Let $C_1 = C_2$ and select a convenient starting value.

Then

$$R_1 = \frac{Q}{H_O \omega_o C_1} \quad (8)$$

$$R_2 = \frac{Q}{(2\,Q^2 - H_O)\,\omega_o\,C_1} \quad (9)$$

$$R_3 = \frac{2Q}{\omega_o C_1} \quad (10)$$

and

$$R_4 = 2R_3\ (\text{for } V_{REF} = V^+) \quad (11)$$

As a design example:

Require: $H_O = 1$

$Q = 5$

$f_o = 1$ kHz ($\omega_o = 6.28 \times 10^3$ rps).

Start by selecting

$C_1 = C_2 = 510$ pF.

Then using equation (8)

$$R_1 = \frac{5}{(6.28 \times 10^3)\,(5.1 \times 10^{-10})}$$

$R_1 = 1.57\ M\Omega$,

and using equation (9)

$$R_2 = \frac{5}{[2(25) - 1]\,(6.28 \times 10^3)\,(5.1 \times 10^{-10})}$$

$R_2 = 32\ k\Omega$

from equation (10)

$$R_3 = \frac{2(5)}{(6.28 \times 10^3)\,(5.1 \times 10^{-10})}$$

$R_3 = 3.13\ M\Omega$,

and finally, for biasing, using equation (11)

$R_4 = 6.2\ M\Omega$.

6.5 A TWO-AMPLIFIER BANDPASS ACTIVE FILTER

To allow higher Q (between 10 and 50) and higher gain, a two amplifier filter is required. This circuit, shown in *Figure 39*, uses only two capacitors. It is similar to the previous single amplifier bandpass circuit and the added amplifier supplies a controlled amount of positive feedback to improve the response characteristics. The resistors R_5 and R_8 are used to bias the output voltage of the amplifiers at $V^+/2$.

Again, R_5 is simply chosen as twice R_4 and R_8 must be selected after R_6 and R_7 have been assigned values. The design procedure is as follows:

Given: Q and f_o

To find: R_1 through R_7, and C_1 and C_2

Let: $C_1 = C_2$ and choose a convenient starting value and choose a value for K to reduce the spread of element values or to optimize sensitivity ($1 \leq K_{Typically} \leq 10$).

Then

$$R_1 = R_4 = R_6 = \frac{Q}{\omega_o C_1} \quad (12)$$

$$R_2 = R_1 \frac{KQ}{(2Q-1)} \quad (13)$$

$$R_3 = \frac{R_1}{Q^2 - 1 - 2/K + 1/KQ} \quad (14)$$

and

$$R_7 = KR_1 \quad (15)$$

$$H_O = \sqrt{Q}\,K. \quad (16)$$

As a design example:

Require: Q = 25 and f_o = 1 kHz.

Select: $C_1 = C_2 = 0.1\ \mu F$

and K = 3.

Then from equation (12)

$$R_1 = R_4 = R_6 = \frac{25}{(2\pi \times 10^3)(10^{-7})}$$

$$R_1 = 40\ k\Omega$$

and from equation (13)

$$R_2 = (40 \times 10^3)\frac{3(25)}{[2(25)-1]}$$

$$R_2 = 61\ k\Omega$$

and from equation (14)

$$R_3 = \frac{40 \times 10^3}{(25)^2 - 1 - 2/3 + \frac{1}{3(25)}}$$

$$R_3 = 64\Omega$$

And R_7 is given by equation (15)

$$R_7 = 3\,(40\ k\Omega) = 120\ k\Omega,$$

and the gain is obtained from equation (16)

$$H_O = \sqrt{25}\,(3) = 15\ (23\ dB).$$

To properly bias the first amplifier

$$R_5 = 2R_4 = 80\ k\Omega$$

and the second amplifier is biased by R_8. Notice that the outputs of both amplifiers will be at $V^+/2$. Therefore R_6 and R_7 can be paralleled and

$$R_8 = 2(R_6 \parallel R_7)$$

or

$$R_8 = 2\left[\frac{(40)\,(120) \times 10^3}{160}\right] = 59\ k\Omega$$

These values, to the closest standard resistor values, have been added to *Figure 39*.

6.6 A THREE-AMPLIFIER BANDPASS ACTIVE FILTER

To reduce Q sensitivity to element variation even further or to provide higher Q (Q>50) a three amplifier bandpass filter can be used. This circuit, *Figure 40*, pre-dates most of the literature on RC active filters and has been used on analog computers. Due to the use of three amplifiers it often is considered too costly—especially for low Q applications. The multiple amplifiers of the LM3900 make this a very useful circuit. It has been called the "Bi-Quad" as it can produce a transfer function which is "Quad"-ratic in both numerator and denominator (to give the "Bi"). A newer real-

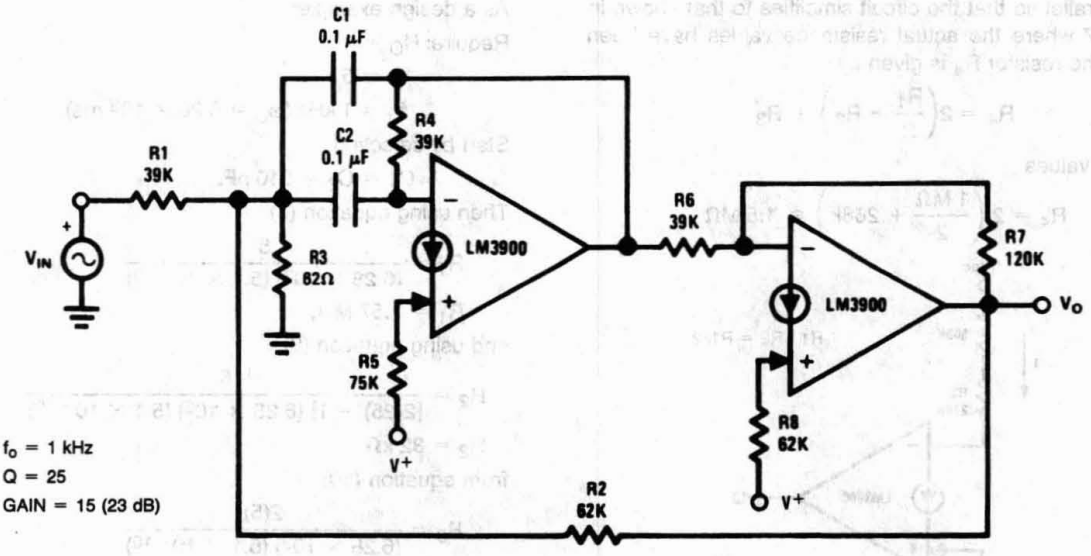

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FIGURE 39. A Two Op Amp Bandpass Filter

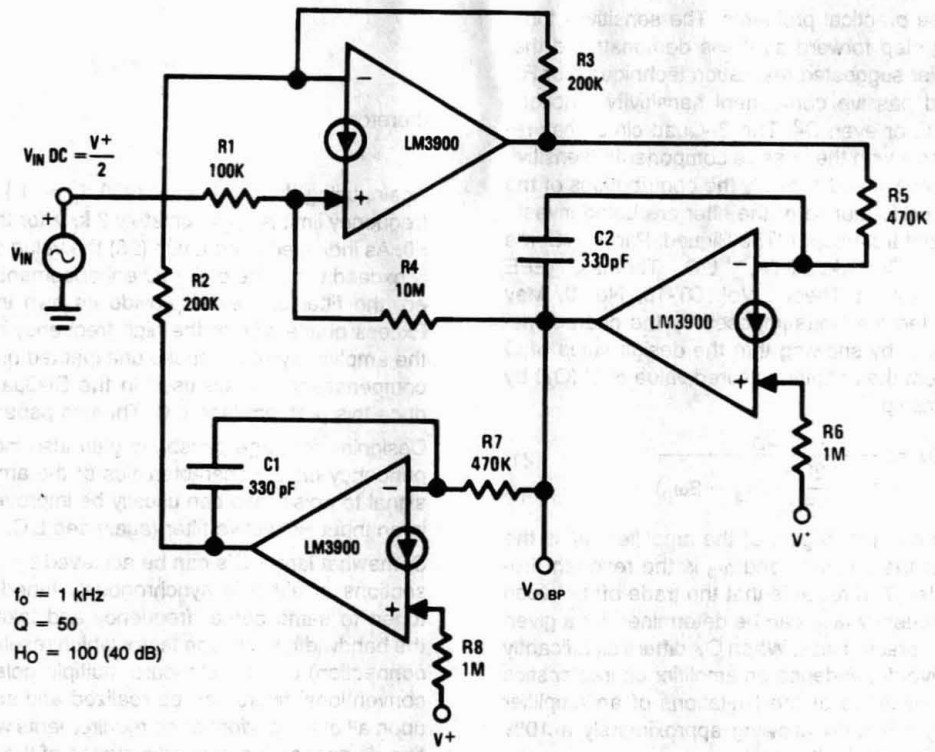

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FIGURE 40. The "Bi-quad" RC Active Bandpass Filter

ization technique for this type of filter is the "second-degree state-variable network." Outputs can be taken at any of three points to give low pass, high pass or bandpass response characteristics (see the reference cited).

The bandpass filter is shown in *Figure 40* and the design procedure is:

Given: Q and f_o.

To simplify: Let $C_1 = C_2$ and choose a convenient starting value and also let $2R_1 = R_2 = R_3$ and choose a convenient starting value.

Then:

$$R_4 = R_1 (2Q - 1), \quad (17)$$

$$R_5 = R_7 = \frac{1}{\omega_o C_1}, \quad (18)$$

and for biasing the amplifiers we require

$$R_6 = R_8 = 2R_5. \quad (19)$$

The mid-band gain is:

$$H_O = \frac{R_4}{R_1}. \quad (20)$$

As a design example;

Require: $f_o = 1$ kHz and $Q = 50$.

To find: C_1, C_2 and R_1 through R_8.

Choose: $C_1 = C_2 = 330$ pF

and $2R_1 = R_2 = R_3 = 360\ k\Omega$, and $R_1 = 180\ k\Omega$.

Then from equation (17),

$$R_4 = (1.8 \times 10^5)\,[2(50) - 1]$$

$$R_4 = 17.8\ M\Omega$$

From equation (18),

$$R_5 = R_7 = \frac{1}{(2\pi \times 10^3)\,(3.3 \times 10^{-10})}$$

$$R_5 = 483\ k\Omega.$$

And from equation (19),

$$R_6 = R_8 \cong 1\ M\Omega.$$

From equation (20) the midband gain is 100 (40 dB). The value of R_4 is high and can be lowered by scaling only R_1 through R_4 by the factor 1.78 to give:

$$2R_1 = R_2 = R_3 = \frac{360 \times 10^3}{1.78} = 200\ k\Omega,\ R_1 = 100\ k\Omega.$$

and

$$R_4 = \frac{17.8 \times 10^6}{1.78} = 10\ M\Omega.$$

These values (to the nearest 5% standard) have been added to *Figure 40*.

6.7 CONCLUSIONS

The unity-gain cross frequency of the LM3900 is 2.5 MHz which is approximately three times that of a "741" op amp. The performance of the amplifier does limit the performance of the filter. Historically, RC active filters started with little

concern for these practical problems. The sensitivity functions were a big step forward as these demonstrated that many of the earlier suggested realization techniques for RC active filters had passive component sensitivity functions which varied as Q or even Q^2. The Bi-Quad circuit has reduced the problems with the passive components (sensitivity functions of 1 or ½) and recently the contributions of the amplifier on the performance of the filter are being investigated. An excellent treatment ("The Biquad: Part I — Some Practical Design Considerations," L.C. Thomas, IEEE Transactions on Circuit Theory, Vol. CT-18, No. 3, May 1971) has indicated the limits imposed by the characteristics of the amplifier by showing that the design value of Q (Q_D) will differ from the actual measured value of Q (Q_A) by the given relationship

$$Q_A = \frac{Q_D}{1 + \frac{2Q_D}{A_O\omega_a}(\omega_a - 2\omega_p)} \qquad (21)$$

where A_O is the open loop gain of the amplifier, ω_a is the dominant pole of the amplifier and ω_p is the resonant frequency of the filter. The result is that the trade-off between Q and center frequency (ω_p) can be determined for a given set of amplifier characteristics. When Q_A differs significantly from Q_D excessive dependence on amplifier characteristics is indicated. An estimate of the limitations of an amplifier can be made by arbitrarily allowing approximately a 10% effect on Q_A which results if

$$\frac{2Q_D}{A_O\omega_a}(\omega_a - 2\omega_p) = 0.1$$

or

$$\left(\frac{\omega_p}{\omega_a}\right) = 2.5 \times 10^{-2}\left(\frac{A_O}{Q_D}\right) + 0.5. \qquad (22)$$

As an example, using $A_O = 2800$ for the LM3900 we can estimate the maximum frequency where a $Q_D = 50$ would be reasonable as

$$\frac{f_p}{f_a} = 2.5 \times 10^{-2}\left(\frac{2.8 \times 10^3}{5 \times 10}\right) + 0.5$$

or

$$\frac{f_p}{f_a} = 1.9$$

therefore

$$f_p = 1.9\, f_a.$$

Again, using data of the LM3900, $f_a = 1$ kHz so this upper frequency limit is approximately 2 kHz for the assumed Q of 50. As indicated in equation (26) the value of Q_A can actually exceed the value of Q_D (Q enhancement) and, as expected, the filter can even provide its own input (oscillating). Excess phase shift in the high frequency characteristics of the amplifier typically cause unexpected oscillations. Phase compensation can be used in the Bi-Quad network to reduce this problem (see L.C. Thomas paper).

Designing for large passband gain also increases filter dependency on the characteristics of the amplifier and finally signal to noise ratio can usually be improved by taking gain in an input RC active filter (again see L.C. Thomas paper).

Somewhat larger Q's can be achieved by adding more filter sections in either a synchronously tuned cascade (filters tuned to same center frequency and taking advantage of the bandwidth shrinkage factor which results from the series connection) or as a standard multiple pole filter. All of the conventional filters can be realized and selection is based upon all of the performance requirements which the application demands. The cost advantages of the LM3900, the relatively large bandwidth and the ease of operation on a single power supply voltage make this product an excellent "building block" for RC active filters.

7.0 Designing Waveform Generators

The multiple amplifiers of the LM3900 can be used to easily generate a wide variety of waveforms in the low frequency range (f ≤ 10 kHz). Voltage controlled oscillators (VCO)'s) are also possible and are presented in section 8.0 "Designing Phase-locked Loops and Voltage Controlled

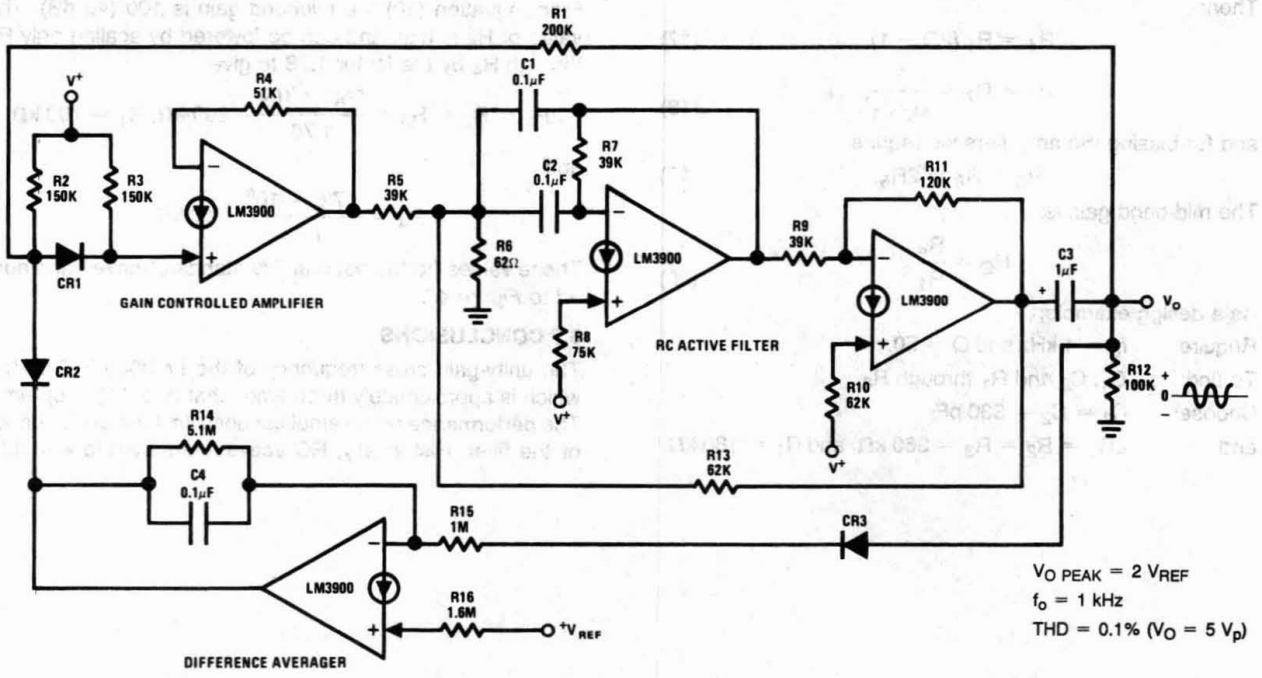

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FIGURE 41. A Sinewave Oscillator

Oscillators." In addition, power oscillators (such as noise makers, etc.) are presented in section 10.11.3. The waveform generators which will be presented in this section are mainly of the switching type, but for completeness a sinewave oscillator has been included.

7.1 A SINEWAVE OSCILLATOR

The design of a sinewave oscillator presents problems in both amplitude stability (and predictability) and output waveform purity (THD). If an RC bandpass filter is used as a high Q resonator for the oscillator circuit we can obtain an output waveform with low distortion and eliminate the problem of relative center frequency drift which exists if the active filter were used simply to filter the output of a separate oscillator.

A sinewave oscillator which is based on this principle is shown in *Figure 41*. The two-amplifier RC active filter is used as it requires only two capacitors and provides an overall non-inverting phase characteristic. If we add a non-inverting gain controlled amplifier around the filter we obtain the desired oscillator configuration. Finally, the sinewave output voltage is sensed and regulated as the average value is compared to a DC reference voltage, V_{REF}, by use of a differential averaging circuit. It can be shown that with the values selected for R_{15} and R_{16} (ratio of 0.64/1) that there is first order temperature compensation for CR_3 and the internal input diodes of the IC amplifier which is used for the "difference averager". Further, this also provides a simple way to regulate and to predict the magnitude of the output sinewave as

$$V_O \text{ peak} = 2\,V_{REF}$$

which is essentially independent of both temperature and the magnitude of the power supply voltage (if V_{REF} is derived from a stable voltage source).

7.2 SQUAREWAVE GENERATOR

The standard op amp squarewave generator has been modified as shown in *Figure 42*. The capacitor, C_1, alternately

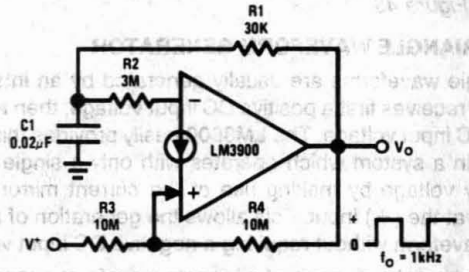

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FIGURE 42. A Squarewave Oscillator

charges and discharges (via R_1) between the voltage limits which are established by the resistors R_2, R_3 and R_4. This combination produces a Schmitt Trigger circuit and the operation can be understood by noticing that when the output is low (and if we neglect the current flow through R_4) the resistor R_2 (3M) will cause the trigger to fire when the current through this resistor equals the current which enters the (+) input (via R_3). This gives a firing voltage of approximately $R_2/(R_3)\ V^+$ (or $V^+/3$). The other trip point, when the output voltage is high, is approximately $[2(R_2/R_3)]\ V^+$, as $R_3 = R_4$, or $\frac{2}{3}(V^+)$. Therefore the voltage across the capacitor, C_1, will be the first one-half of an exponential waveform between these voltage trip limits and will have good symmetry and be essentially independent of the magnitude of the power supply voltage. If an unsymmetrical squarewave is desired, the trip points can be shifted to produce any desired mark/space ratio.

7.3 PULSE GENERATOR

The squarewave generator can be slightly modified to provide a pulse generator. The slew rate limits of the LM3900 (0.5V/μsec) must be kept in mind as this limits the ability to produce a narrow pulse when operating at a high power supply voltage level. For example, with a +15 V_{DC} power supply the rise time, t_r, to change 15V is given by:

$$t_r = \frac{15V}{\text{Slew Rate}} = \frac{15V}{0.5V/\mu\text{sec}}$$

$$t_r = 30\ \mu\text{sec}.$$

The schematic of a pulse generator is shown in *Figure 43*. A diode has been added, CR_1, to allow separating the charge path to C_1 (via R_1) from the discharge path (via R_2). The

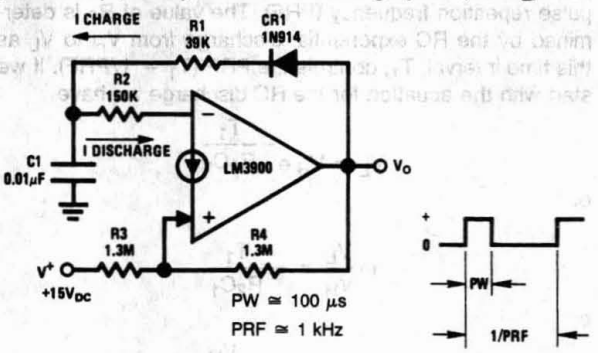

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FIGURE 43. A Pulse Generator

circuit operates as follows: Assume first that the output voltage has just switched low (and we will neglect the current flow through R_4). The voltage across C_1 is high and the magnitude of the discharge current (through R_2) is given by

$$I_{\text{Discharge}} \cong \frac{V_{C_1} - V_{BE}}{R_2}.$$

This current is larger than that entering the (+) input which is given by

$$I_{R_3} = \frac{V^+ - V_{BE}}{R_3}.$$

The excess current entering the (−) input terminal causes the amplifier to be driven to a low output voltage state (saturation). This condition remains for the long time interval (1/Pulse Repetition Frequency) until the R_2C_1 discharge current equals the I_{R_3} value (as CR_1 is OFF during this interval). The voltage across C_1 at the trip point, V_L, is given by

$$V_L = (I_{R_3})\,(R_2),$$

or

$$V_L = (V^+ - V_{BE})\left(\frac{R_2}{R_3}\right). \qquad (1)$$

At this time the output voltage will switch to a high state, V_{OHi}, and the current entering the (+) input will increase to

$$I_{M^+} = \frac{V^+ - V_{BE}}{R_3} + \frac{V_{OHi} - V_{BE}}{R_4}.$$

Also CR_1 goes ON and the capacitor, C_1, charges via R_1. Some of this charge current is diverted via R_2 to ground (the (−) input is at V_{CESAT} during this interval as the current mirror is demanding more current than the (−) input terminal can provide). The high trip voltage, V_H, is given by

$$V_H = (I_M{}^+)\, R_2 \quad \text{or}$$

$$V_H = \left(\frac{V^+ - V_{BE}}{R_3} + \frac{V_{OHi} - V_{BE}}{R_4}\right) R_2. \tag{2}$$

A design proceeds by first choosing the trip points for the voltage across C_1. The resistors R_3 and R_4 are used only for this trip voltage control. The resistor R_2 affects the discharge time (the long interval) and also both of the trip voltages so this resistor is determined first from the required pulse repetition frequency (PRF). The value of R_2 is determined by the RC exponential discharge from V_H to V_L as this time interval, T_1, controls the PRF ($T_1 = 1/PRF$). If we start with the equation for the RC discharge we have

$$V_L = V_H\, e^{-\frac{T_1}{R_2C_1}}$$

or

$$\ln\frac{V_L}{V_H} = -\frac{T_1}{R_2C_1}$$

or

$$T_1 = R_2C_1 \ln\frac{V_H}{V_L} \tag{3}$$

To provide a low duty cycle pulse train we select small values for both V_H and V_L (such as 3V and 1.5V) and choose a starting value for C_1. Then R_2 is given by

$$R_2 = \frac{T_1}{C_1 \ln\frac{V_H}{V_L}}. \tag{4}$$

If R_2 from (4) is not in the range of approximately 100 kΩ to 1 MΩ, choose another value for C_1. Now equation (1) can be used to find a value for R_3 to provide the V_L which was initially assumed. Similarly equation (2) allows R_4 to be calculated. Finally R_1 is determined by the required pulse width (PW) as the capacitor, C_1, must be charged from V_L to V_H by R_1. This RC charging is given by (neglecting the loading due to R_2)

$$V_H \cong (V_{OHi} - V_D)\left(1 - e^{-\frac{T_2}{R_1C_1}}\right)$$

or

$$T_2 \cong -R_1C_1 \ln\left[1 - \frac{V_H}{V_{OHi} - V_D}\right], \text{ and finally}$$

$$R_1 \cong \frac{T_2}{-C_1 \ln\left[1 - \frac{V_H}{V_{OHi} - V_D}\right]} \tag{5}$$

where T_2 is the pulse width desired and V_D is the forward voltage drop across CR_1.

As a design example:

Required: Provide a 100 μs pulse every 1 ms. The power supply voltage is +15 V_{DC}

1.0 Start by choosing $V_L = 1.5V$

and $V_H = 3.0V$

2.0 Find R_2 from equation (4) assuming $C_1 = 0.01\ \mu F$,

$$R_2 = \frac{10^{-3}}{10^{-8} \ln\left(\frac{3.0}{1.5}\right)}$$

$$R_2 = \frac{10^5}{0.694} = 144\ k\Omega$$

3.0 Find R_3 from equation (1)

$$R_3 = \frac{(V^+ - V_{BE})\, R_2}{V_L}$$

$$R_3 = \frac{(15 - 0.5)\ 1.44 \times 10^5}{1.5}$$

$$R_3 = 1.39\ M\Omega$$

4.0 Find R_4 from equation (2),

$$R_4 = \frac{(V_{OHi} - V_{BE})}{\frac{V_H}{R_2} - \frac{V^+ - V_{BE}}{R_3}}$$

$$R_4 = \frac{(14.2 - 0.5)}{\frac{3}{1.44 \times 10^5} - \frac{15 - 0.5}{1.39 \times 10^6}}$$

$$R_4 = 1.32\ M\Omega$$

5.0 Find R_1 from equation (5),

$$R_1 = \frac{10^{-4}}{-10^{-8} \ln\left(1 - \frac{3}{(14.2 - 0.7)}\right)}$$

$$R_1 = \frac{10^4}{-\ln\left(1 - \frac{3}{13.5}\right)}$$

$$R_1 = \frac{10^4}{0.252} = 39.7\ k\Omega.$$

These values (to the nearest 5% standard) have been added to *Figure 43*.

7.4 TRIANGLE WAVEFORM GENERATOR

Triangle waveforms are usually generated by an integrator which receives first a positive DC input voltage, then a negative DC input voltage. The LM3900 easily provides this operation in a system which operates with only a single power supply voltage by making use of the current mirror which exists at the (+) input. This allows the generation of a triangle waveform without requiring a negative DC input voltage.

The schematic diagram of a triangle waveform generator is shown in *Figure 44*. One amplifier is doing the integration by

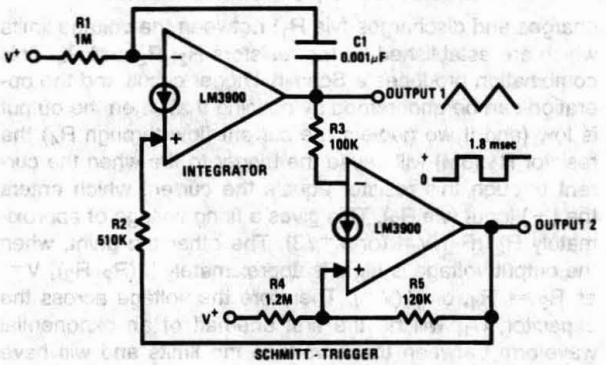

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FIGURE 44. A Triangle Waveform Generator

operating first with the current through R_1 to produce the negative output voltage slope, and then when the output of the second amplifier (the Schmitt Trigger) is high, the current through R_2 causes the output voltage to increase. If $R_1 = 2R_2$, the output waveform will have good symmetry. The timing for one-half of the period (T/2) is given by

$$\frac{T}{2} = \frac{(R_1C_1)\Delta V_O}{V^+ - V_{BE}}$$

or the output frequency becomes

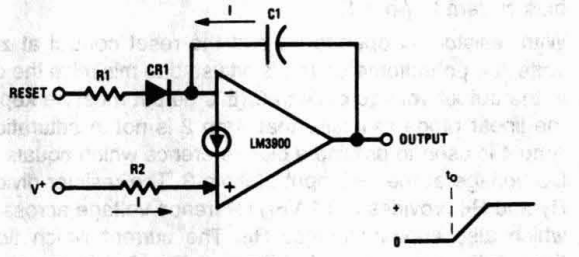
$$f_o = \frac{V^+ - V_{BE}}{2R_1C_1\Delta V_O}$$

where we have assumed $R_1 = 2R_2$, V_{BE} is the DC voltage at the (−) input (0.5 V_{DC}), and ΔV_O is the difference between the trip points of the Schmitt Trigger. The design of the Schmitt Trigger has been presented in the section on Digital and Switching Circuits (9.0) and the trip voltages control the peak-to-peak excursion of the triangle output voltage waveform. The output of the Schmitt circuit provides a squarewave of the same frequency.

7.5 SAWTOOTH WAVEFORM GENERATOR

The previously described triangle waveform generator, *Figure 44*, can be modified to produce a sawtooth waveform. Two types of waveforms can be provided, both a positive ramp and a negative ramp sawtooth waveform by selecting R_1 and R_2. The reset time is also controlled by the ratio of R_1 and R_2. For example, if $R_1 = 10\ R_2$ a positive ramp sawtooth results and if $R_2 = 10\ R_1$ a negative ramp sawtooth can be obtained. Again, the slew rate limits of the amplifier (0.5V/μs) will limit the minimum retrace time, and the increased slew rate of a negative going output will allow a faster retrace for a positive ramp sawtooth waveform.

To provide a gated sawtooth waveform, the circuits shown in *Figure 45* can be used. In *Figure 45(a)*, a positive ramp is generated by integrating the current, I, which is entering the (+) input. Reset is provided via R_1 and CR_1 keeps R_1 from loading at the (−) input during the sweep interval. This will sweep from $V_{O\ MIN}$ to $V_{O\ MAX}$ and will remain at $V_{O\ MAX}$ until reset. The interchange of the input leads, *Figure 45(b)*, will generate a negative ramp, from $V_{O\ MAX}$ to $V_{O\ MIN}$.



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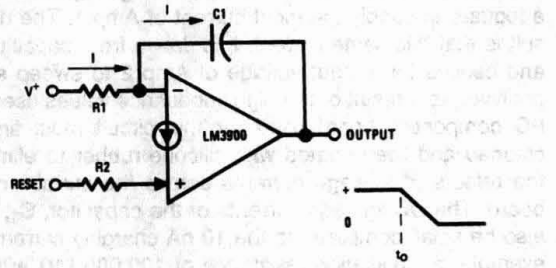
(a) Positive Ramp



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(b) Negative Ramp

FIGURE 45. Gated Sawtooth Generators

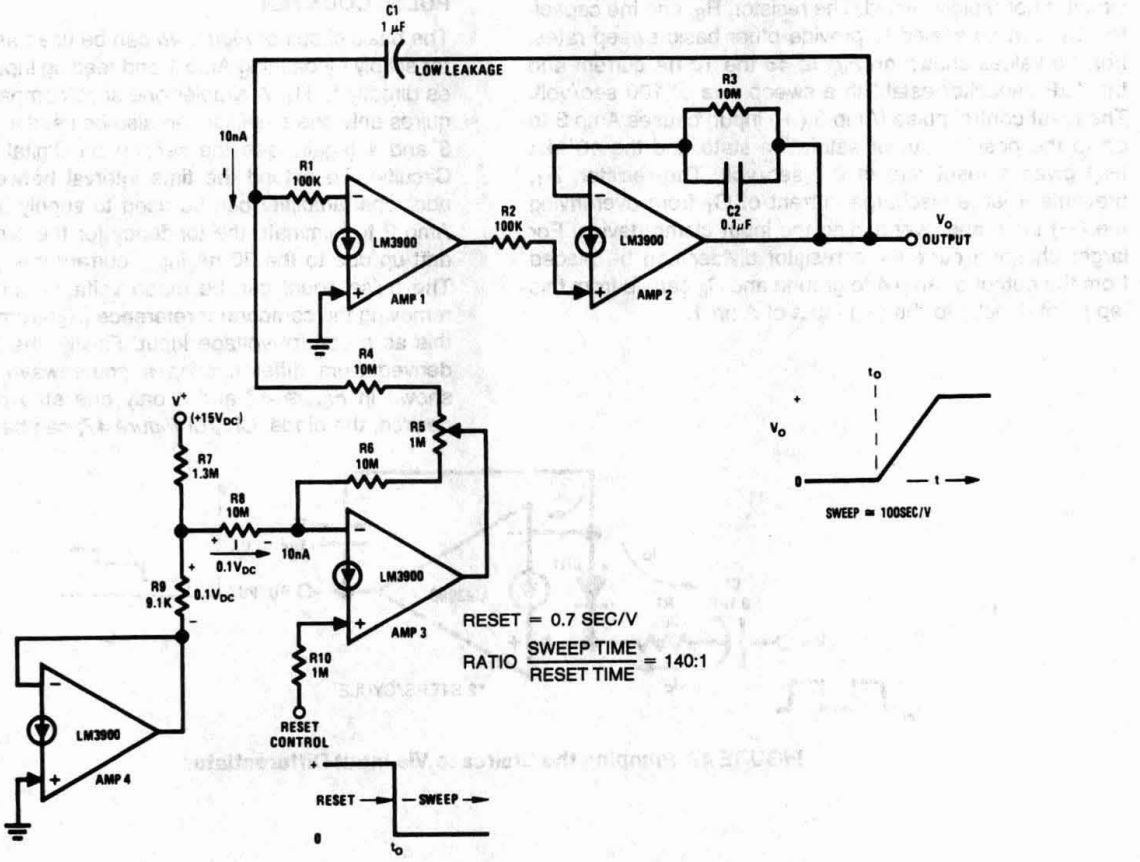

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FIGURE 46. Generating Very Slow Sawtooth Waveforms

7.5.1 GENERATING A VERY SLOW SAWTOOTH WAVEFORM

The LM3900 can be used to generate a very slow sawtooth waveform which can be used to generate long time delay intervals. The circuit is shown in *Figure 46* and uses four amplifiers. Amps 1 and 2 are cascaded to increase the gain of the integrator and the output is the desired very slow sawtooth waveform. Amp 3 is used to exactly supply the bias current to Amp 1.

With resistor R_8 opened up and the reset control at zero volts, the potentiometer, R_5, is adjusted to minimize the drift in the output voltage of Amp 2 (this output must be kept in the linear range to insure that Amp 2 is not in saturation). Amp 4 is used to provide a bias reference which equals the DC voltage at the (−) input of Amp 3. The resistor divider, R_7 and R_9 provides a 0.1 V_{DC} reference voltage across R_9 which also appears across R_8. The current which flows through R_8, I, enters the (−) input of Amp 3 and causes the current through R_6 to drop by this amount. This causes an imbalance as now the current flow through R_4 is no longer adequate to supply the input current of Amp 1. The net result is that this same current, I, is drawn from capacitor C_1 and causes the output voltage of Amp 2 to sweep slowly positive. As a result of the high impedance values used, the PC component board used for this circuit must first be cleaned and then coated with silicone rubber to eliminate the effects of leakage currents across the surface of the board. The DC leakage currents of the capacitor, C_1, must also be small compared to the 10 nA charging current. For example, an insulation resistance of 100,000 MΩ will leak 0.1 nA with 10 V_{DC} across the capacitor and this leakage rapidly increases at higher temperatures. Dielectric polarization of the dielectric material may not cause problems if the circuit is not rapidly cycled. The resistor, R_8, and the capacitor, C_1, can be scaled to provide other basic sweep rates. For the values shown on *Figure 46* the 10 nA current and the 1μF capacitor establish a sweep rate of 100 sec/volt. The reset control pulse (Amp 3 (+) input) causes Amp 3 to go to the positive output saturation state and the 10 MΩ (R_4) gives a reset rate of 0.7 sec/volt. The resistor, R_1, prevents a large discharge current of C_1 from overdriving the (−) input and overloading the input clamp device. For larger charging currents, a resistor divider can be placed from the output of Amp 4 to ground and R_8 can tie from this tap point directly to the (−) input of Amp 1.

7.6 STAIRCASE WAVEFORM GENERATORS

A staircase generator can be realized by supplying pulses to an integrator circuit. The LM3900 also can be used with a squarewave input signal and a differentiating network where each transition of the input squarewave causes a step in the output waveform (or two steps per input cycle). This is shown in *Figure 47*. These pulses of current are the charge and discharge currents of the input capacitor, C_1. The charge current, I_C, enters the (+) input and is mirrored about ground and is "drawn into" the (−) input. The discharge current, I_D, is drawn through the diode at the input, CR_1, and therefore also causes a step on the output staircase.

A free running staircase generator is shown in *Figure 48*. This uses all four of the amplifiers which are available in one LM3900 package.

Amp 1 provides the input pulses which "pump up" the staircase via resistor R_1 (see section 7.3 for the design of this pulse generator). Amp 2 does the integrate and hold function and also supplies the output staircase waveform. Amps 3 and 4 provide both a compare and a one-shot multivibrator function (see the section on Digital and Switching Circuits for the design of this dual function one-shot). Resistor R_4 is used to sample the staircase output voltage and to compare it with the power supply voltage (V^+) via R_3. When the output exceeds approximately 80% of V^+ the connection of Amps 3 and 4 causes a 100 μsec reset pulse to be generated. This is coupled to the integrator (Amp 2) via R_2 and causes the staircase output voltage to fall to approximately zero volts. The next pulse out of Amp 1 then starts a new stepping cycle.

7.7 A PULSE COUNTER AND A VOLTAGE VARIABLE PULSE COUNTER

The basic circuit of *Figure 48* can be used as a pulse counter simply by omitting Amp 1 and feeding input voltage pulses directly to R_1. A simpler one-shot/comparator which requires only one amplifier can also be used in place of Amps 3 and 4 (again, see the section on Digital and Switching Circuits). To extend the time interval between pulses, an additional amplifier can be used to supply base current to Amp 2 to eliminate the tendency for the output voltage to drift up due to the 30 nA input current (see section 7.5.1). The pulse count can be made voltage variable simply by removing the comparator reference (R_3) from V^+ and using this as a control voltage input. Finally, the input could be derived from differentiating a squarewave input as was shown in *Figure 47* and if only one step per cycle were desired, the diode, CR_1 of *Figure 47*, can be eliminated.

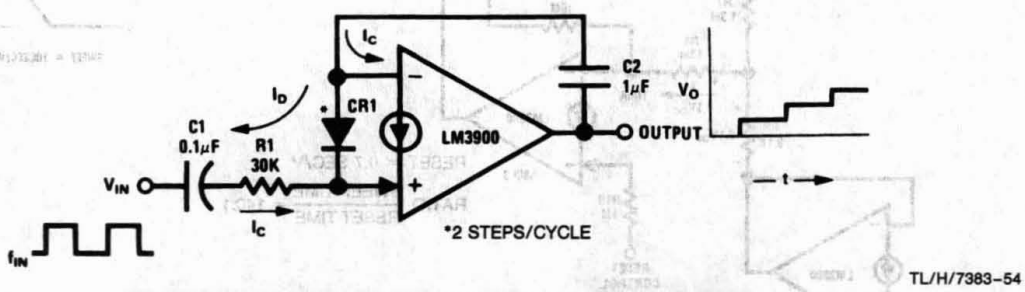

FIGURE 47. Pumping the Staircase Via Input Differentiator

7.8 AN UP-DOWN STAIRCASE WAVEFORM GENERATOR

A staircase waveform which first steps up and then steps down is provided by the circuit shown in *Figure 49*. An input pulse generator provides the pulses which cause the output to step up or down depending on the conduction of the clamp transistor, Q_1. When this is ON, the "down" current pulse is diverted to ground and the staircase then steps "up". When the upper voltage trip point of Amp 2 (Schmitt Trigger—see section on Digital and Switching Circuits) is reached, Q_1 goes OFF and as a result of the smaller "down" input resistor (one-half the value of the "up" resistor, R_1) the staircase steps "down" to the low voltage trip point of Amp 2. The output voltage therefore steps up and down between the trip voltages of the Schmitt Trigger.

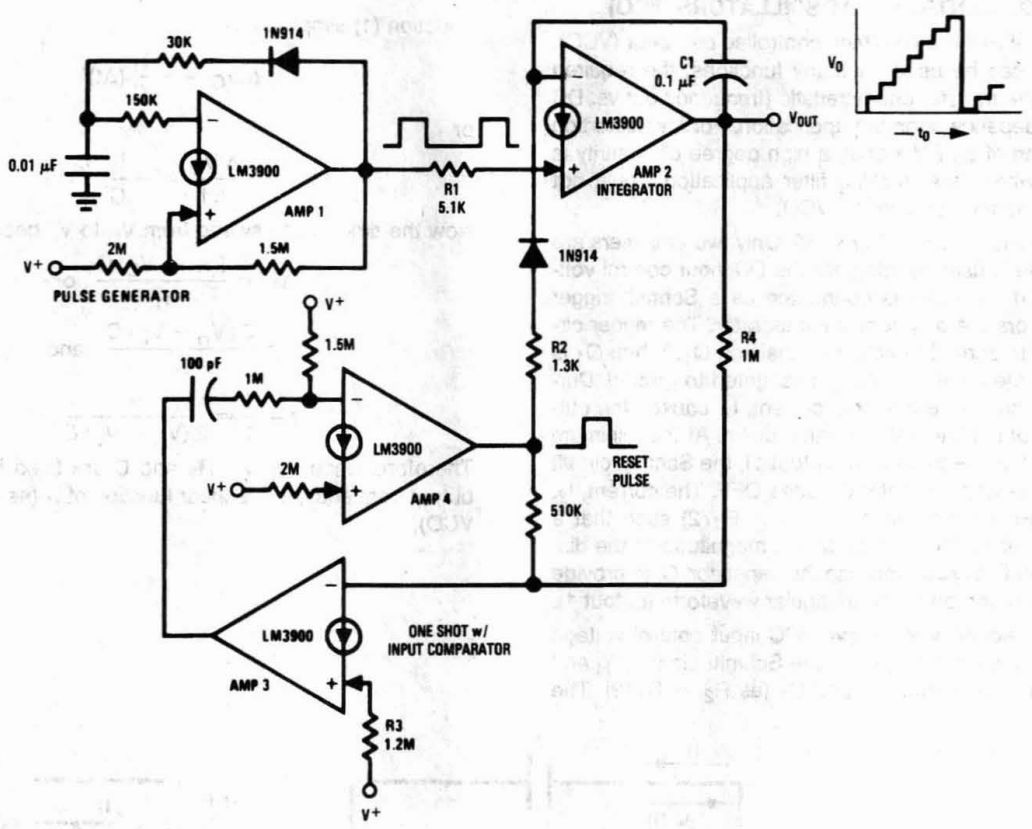

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FIGURE 48. A Free Running Staircase Generator

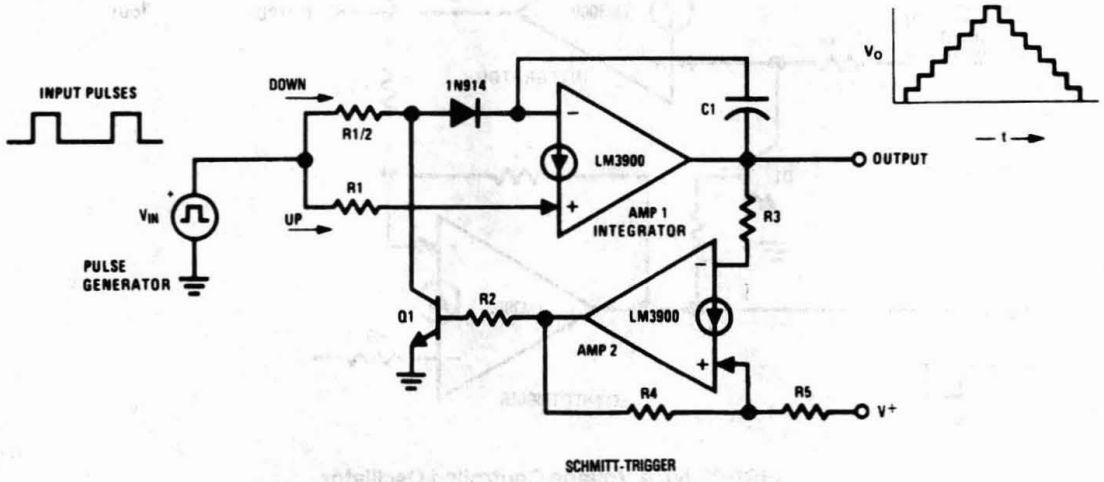

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FIGURE 49. An Up-down Staircase Generator

8.0 Designing Phase-Locked Loops and Voltage Controlled Oscillators

The LM3900 can be connected to provide a low frequency ($f < 10$ kHz) phase-locked loop (PL^2). This is a useful circuit for many control applications. Tracking filters, frequency to DC converters, FM modulators and demodulators are applications of a PL^2.

8.1 VOLTAGE CONTROLLED OSCILLATORS (VCO)

The heart of a PL^2 is the voltage controlled oscillator (VCO). As the PL^2 can be used for many functions, the required linearity of the transfer characteristic (frequency out vs. DC voltage in) depends upon the application. For low distortion demodulation of an FM signal, a high degree of linearity is necessary whereas a tracking filter application would not require this performance in the VCO.

A VCO circuit is shown in *Figure 50*. Only two amplifiers are required, one is used to integrate the DC input control voltage, V_C, and the other is connected as a Schmitt-trigger which monitors the output of the integrator. The trigger circuit is used to control the clamp transistor, Q_1. When Q_1 is conducting, the input current, I_2, is shunted to ground. During this one-half cycle the input current, I_1, causes the output voltage of the integrator to ramp down. At the minimum point of the triangle waveform (output 1), the Schmitt circuit changes state and transistor Q_1 goes OFF. The current, I_2, is exactly twice the value of I_1 ($R_2 = R_1/2$) such that a charge current (which is equal to the magnitude of the discharge current) is drawn through the capacitor, C, to provide the increasing portion of the triangular waveform (output 1).

The output frequency for a given DC input control voltage depends on the trip voltages of the Schmitt circuit (V_H and V_L) and the components R_1 and C_1 (as $R_2 = R_1/2$). The time to ramp down from V_H to V_L corresponds to one-half the period (T) of the output frequency and can be found by starting with the basic equation of the integrator

$$V_O = -\frac{1}{C}\int I_1\,dt \qquad (1)$$

as I_1 is a constant (for a given value of V_C) which is given by

$$I_1 = \frac{V_C - V_{BE}}{R_1} \qquad (2)$$

equation (1) simplifies to

$$\Delta V_O = -\frac{I_1}{C}(\Delta t)$$

or

$$\frac{\Delta V_O}{\Delta t} = -\frac{I_1}{C} \qquad (3)$$

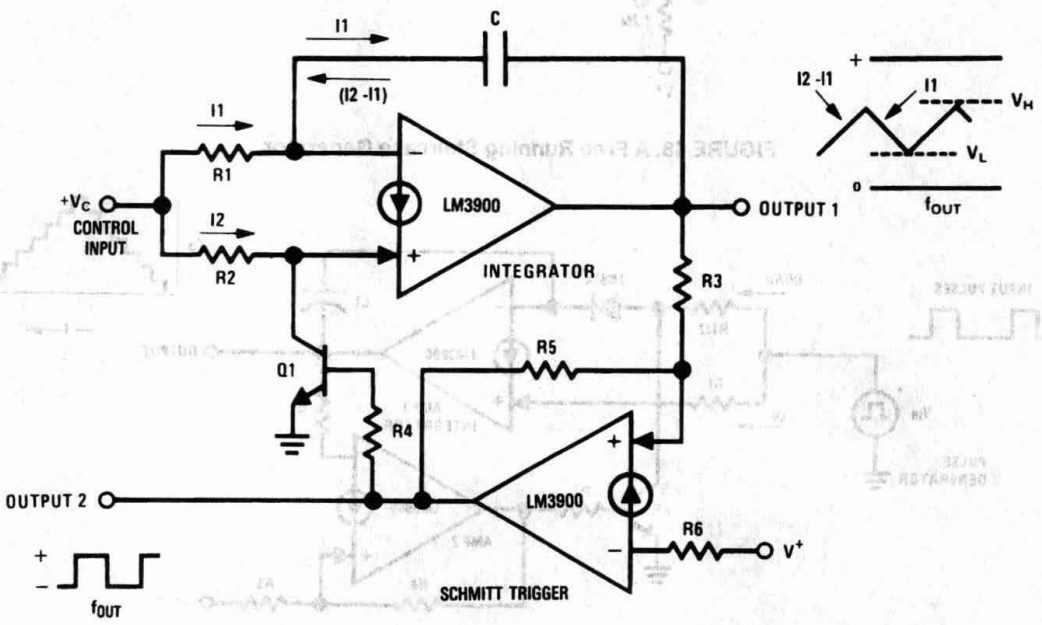
Now the time, Δt, to sweep from V_H to V_L becomes

$$\Delta t_1 = \frac{(V_H - V_L)\,C}{I_1} \quad \text{or}$$

$$T = \frac{2\,(V_H - V_L)\,C}{I_1} \quad \text{and}$$

$$f = \frac{1}{T} = \frac{I_1}{2\,(V_H - V_L)\,C}. \qquad (4)$$

Therefore, once V_H, V_L, R_1 and C are fixed in value, the output frequency, f, is a linear function of I_1 (as desired for a VCO).



TL/H/7383–57

FIGURE 50. A Voltage Controlled Oscillator

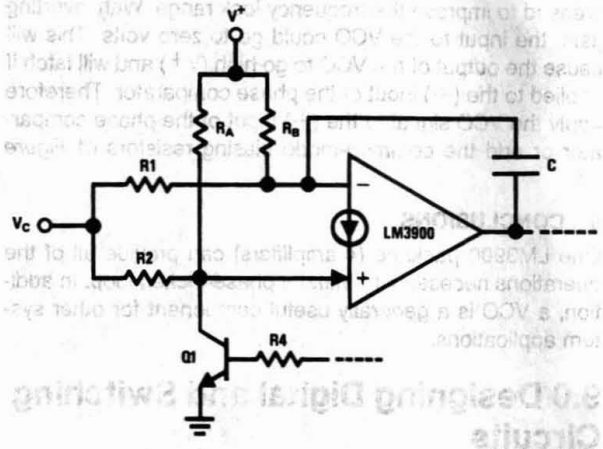


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FIGURE 51. Adding Input Common-mode Biasing Resistors

The circuit shown in *Figure 50* will require $V_C > V_{BE}$ to oscillate. A value of $V_C = 0$ provides $f_{OUT} = 0$, which may or may not be desired. Two common-mode input biasing resistors can be added as shown in *Figure 51* to allow $f_{OUT} = f_{MIN}$ for $V_C = 0$. In general, if these resistors are a factor of 10 larger than their corresponding resistor (R_1 or R_2) a large control frequency ratio can be realized. Actually, V_C could range outside the supply voltage limit of V^+ and this circuit will still function properly.

The output frequency of this circuit can be increased by reducing the peak-to-peak excursion of the triangle waveform (output 1) by design of the trip points of the Schmitt circuit. A limit is reached when the triangular sweep output waveform exceeds the slew rate limit of the LM3900 (0.5 V/μs). Note that the output of the Schmitt circuit has to move up only one V_{BE} to bring the clamp transistor, Q_1, ON, and therefore output slew rate of this circuit is not a limit.

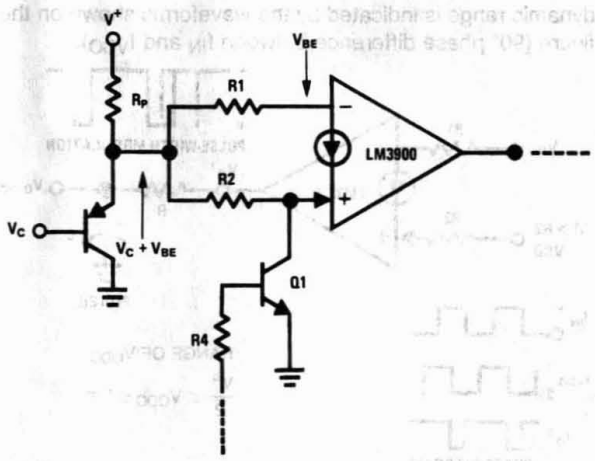

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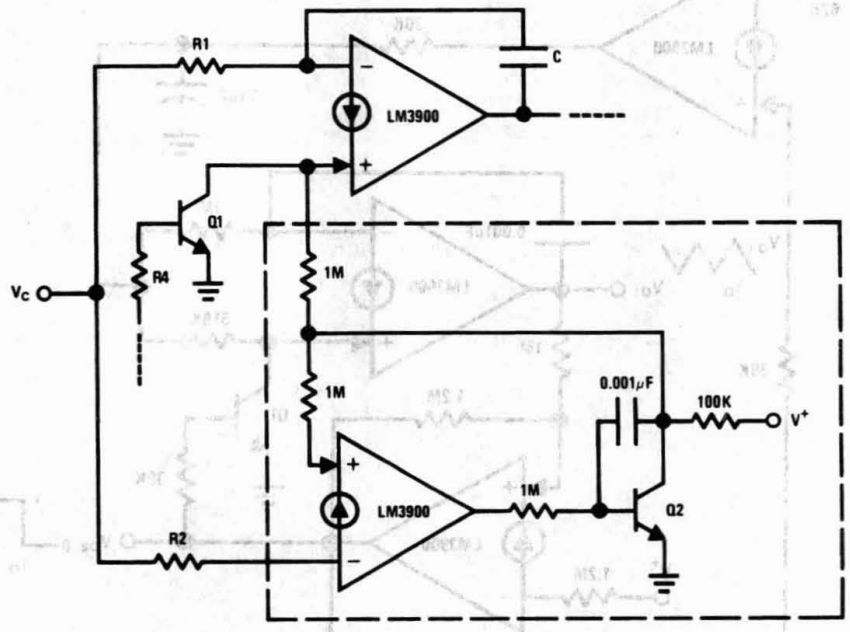
FIGURE 52. Reducing Temperature Drift

To improve the temperature stability of the VCO, a PNP emitter follower can be used to give approximate compensation for the V_{BE}'s at the inputs to the amplifier (see *Figure 52*). Finally to improve the mark to space ratio accuracy over temperature and at low control voltages, an additional amplifier can be added such that both reference currents are applied to the same type of (inverting) inputs of the LM3900. The circuit to accomplish this is shown within dotted lines in *Figure 53*.

8.2 PHASE COMPARATOR

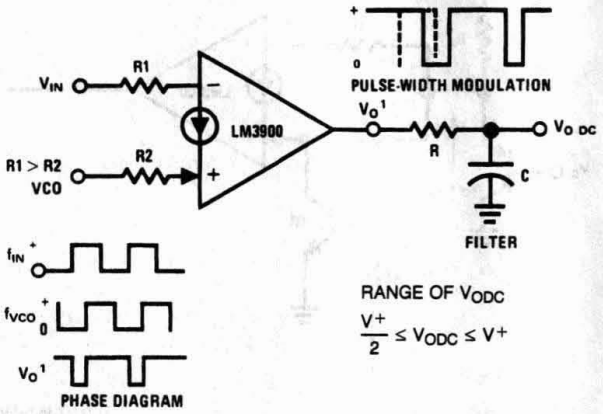
A basic phase comparator is shown in *Figure 54*. This circuit provides a pulse-width modulated output voltage waveform, V_O[1], which must be filtered to provide a DC output voltage (this filter can be the same as the one needed in the PL[2]). The resistor R_2 is made smaller than R_1 so the (+) input serves to inhibit the (−) input signal. The center of the



TL/H/7383–60

FIGURE 53. Improving Mark/Space Ratio

dynamic range is indicated by the waveforms shown on the figure (90° phase difference between f_{IN} and f_{VCO}).



TL/H/7383–61

FIGURE 54. Phase Comparator

The filtered DC output voltage will center at $3V^+/4$ and can range from $V^+/2$ to V^+ as the phase error ranges from 0 degrees to 180 degrees.

8.3 A COMPLETE PHASE-LOCKED LOOP

A phase-locked loop can be realized with three of the amplifiers as shown in *Figure 55*. This has a center frequency of approximately 3 kHz. To increase the lock range, DC gain can be added at the input to the VCO by using the fourth amplifier of the LM3900. If the gain is inverting, the limited DC dynamic range out of the phase detector can be increased to improve the frequency lock range. With inverting gain, the input to the VCO could go to zero volts. This will cause the output of the VCO to go high (V^+) and will latch if applied to the (+) input of the phase comparator. Therefore apply the VCO signal to the (−) input of the phase comparator or add the common-mode biasing resistors of *Figure 51*.

8.4 CONCLUSIONS

One LM3900 package (4 amplifiers) can provide all of the operations necessary to make a phase-locked loop. In addition, a VCO is a generally useful component for other system applications.

9.0 Designing Digital and Switching Circuits

The amplifiers of the LM3900 can be over-driven and used to provide a large number of low speed digital and switching circuit applications for control systems which operate off of single power supply voltages larger than the standard +5 V_{DC} digital limit. The large voltage swing and slower speed are both advantages for most industrial control systems. Each amplifier of the LM3900 can be thought of as "a super transistor" with a β of 1,000,000 (25 nA input current and 25 mA output current) and with a non-inverting input feature. In addition, the active pull-up and pull-down which exists at the output will supply larger currents than the simple resistor pull-ups which are used in digital logic gates. Finally, the low input currents allow timing circuits which minimize the capacitor values as large impedance levels can be used with the LM3900.

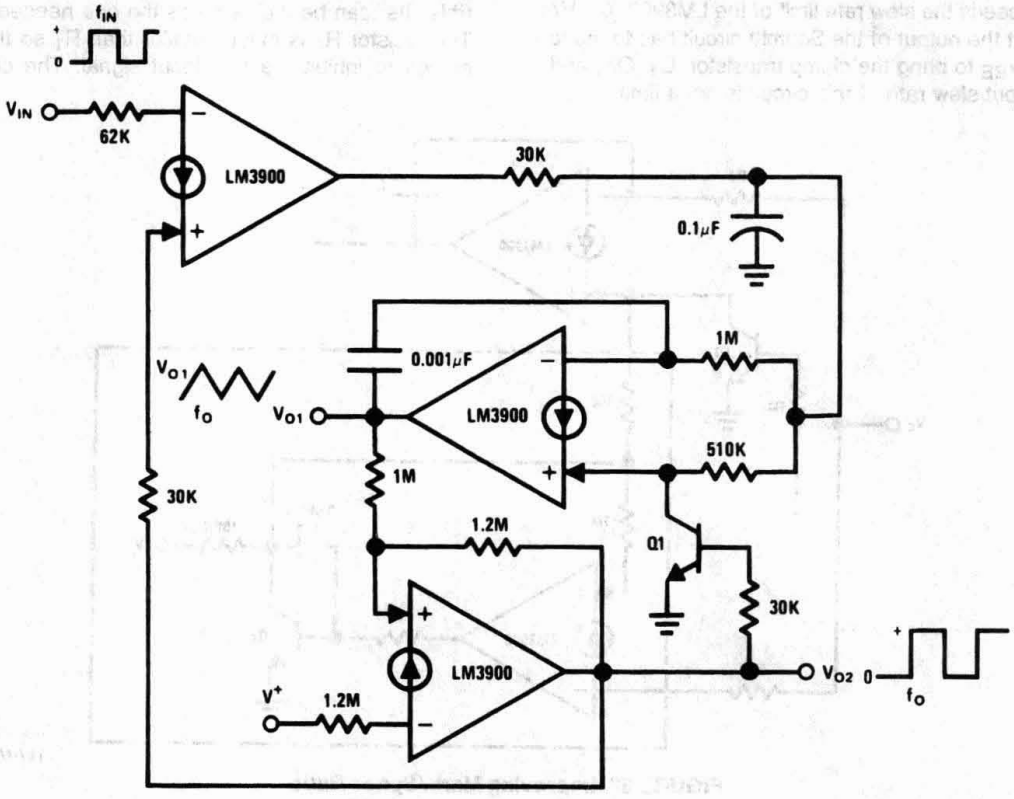


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FIGURE 55. A Phase-locked Loop

9.1 AN "OR" GATE

An OR gate can be realized by the circuit shown in *Figure 56*. A resistor (150 kΩ) from V^+ to the (−) input keeps the output of the amplifier in a low voltage saturated state for all inputs A, B, and C at 0V. If any one of the input signals were to go high ($\cong V^+$) the current flow through the 75 kΩ input resistor will cause the amplifier to switch to the positive output saturation state ($V_O \cong V^+$). The current loss through the other input resistors (which have an input in the low voltage state) represents an insignificant amount of the total input current which is provided by the, at least one, high voltage input. More than three inputs can be OR'ed if desired.

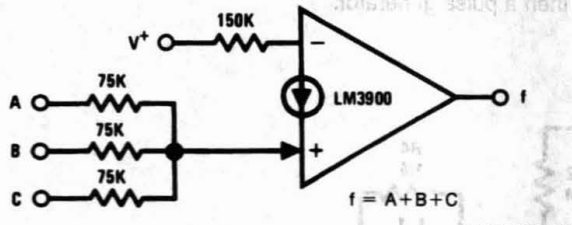

FIGURE 56. An "OR" Gate

The "fan-out" or logical drive capability is large (50 gates if each gate input has a 75 kΩ resistor) due to the 10 mA output current capability of the LM3900. A NOR gate can be obtained by interchanging the inputs to the LM3900.

9.2 AN "AND" GATE

A three input AND gate is shown in *Figure 57*. This gate requires all three inputs to be high in order to have sufficient current entering the (+) input to cause the output of the amplifier to switch high. The addition of R_2 causes a smaller current to enter the (+) input when only two of the inputs are high. (A two input AND gate would not require a resistor

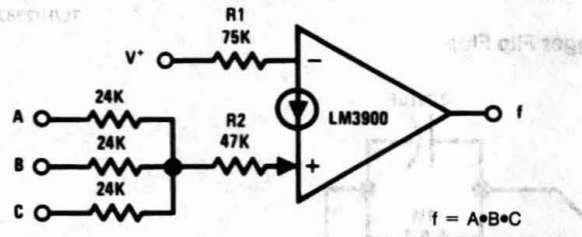

FIGURE 57. An "AND" Gate

as R_2). More than three inputs becomes difficult with this resistor summing approach as the (+) input is too close to having the necessary current to switch just prior to the last input going high. For a larger fan-in an input diode network (similar to DTL) is recommended as shown in *Figure 58*. Interchange the inputs for a NAND gate.

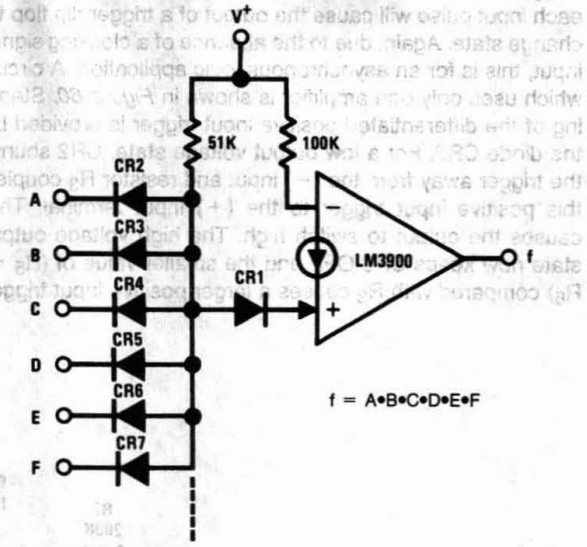

FIGURE 58. A Large Fan-in "AND" Gate

9.3 A BI-STABLE MULTIVIBRATOR

A bi-stable multivibrator (as asynchronous RS flip-flop) can be realized as shown in *Figure 59*. Positive feedback is provided by resistor R_4 which causes the latching. A positive pulse at the "set" input causes the output to go high and a "reset" positive pulse will return the output to essentially $0V_{DC}$.

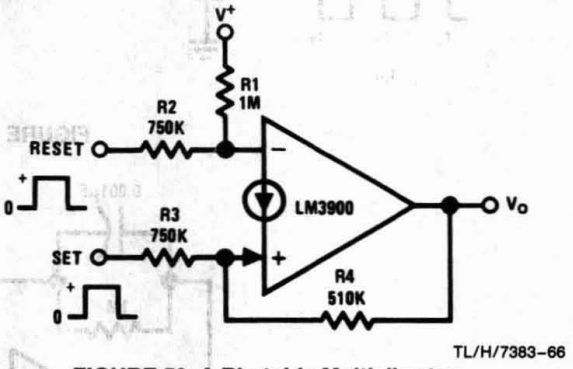

FIGURE 59. A Bi-stable Multivibrator

9.4 TRIGGER FLIP FLOPS

Trigger flip flops are useful to divide an input frequency as each input pulse will cause the output of a trigger flip flop to change state. Again, due to the absence of a clocking signal input, this is for an asynchronous logic application. A circuit which uses only one amplifier is shown in *Figure 60*. Steering of the differentiated positive input trigger is provided by the diode CR2. For a low output voltage state, CR2 shunts the trigger away from the (−) input and resistor R_3 couples this positive input trigger to the (+) input terminal. This causes the output to switch high. The high voltage output state now keeps CR2 OFF and the smaller value of (R_5 + R_6) compared with R_3 causes a larger positive input trigger to be coupled to the (−) input which causes the output to switch to the low voltage state.

A second trigger flip flop can be made which consists of two amplifiers and also provides a complementary output. This connection is shown in *Figure 61*.

9.5 MONOSTABLE MULTIVIBRATORS (ONE-SHOTS)

Monostable multivibrators can be made using one or two of the amplifiers of the LM3900. In addition, the output can be designed to be either high or low in the quiescent state. Further, to increase the usefulness, a one-shot can be designed which triggers at a particular DC input voltage level to serve the dual role of providing first a comparator and then a pulse generator.

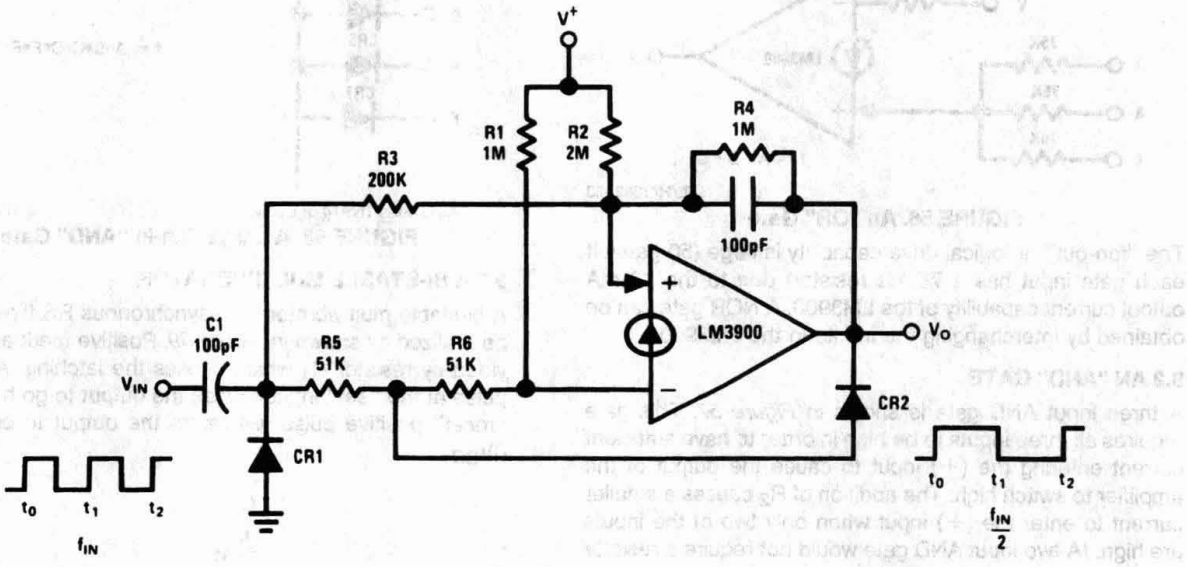

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FIGURE 60. A Trigger Flip Flop

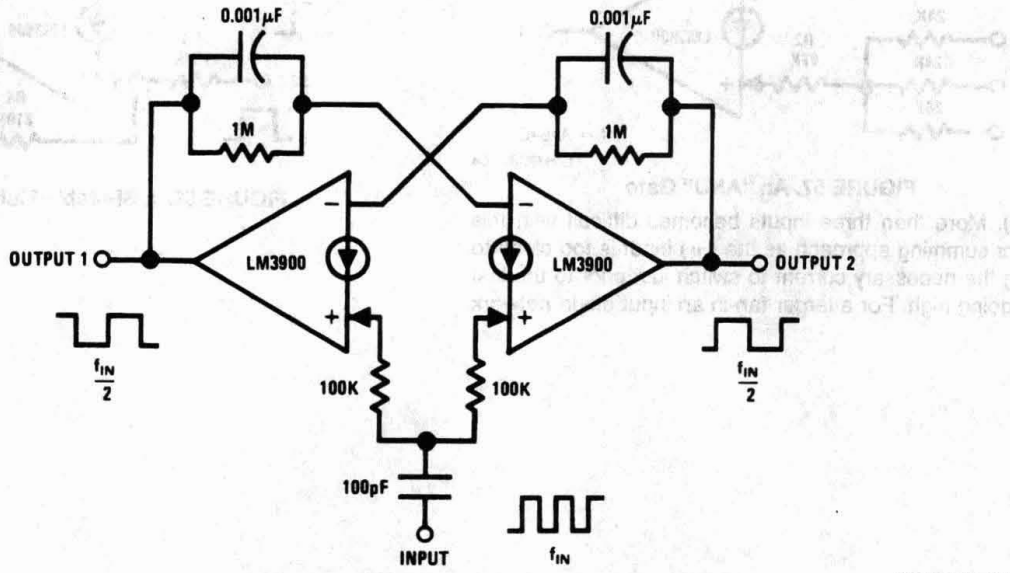

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FIGURE 61. A Two-amplifier Trigger Flip Flop

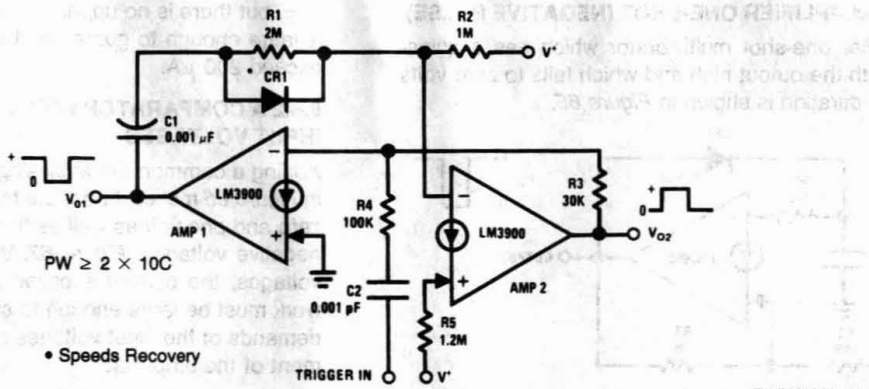

FIGURE 62. A One-shot Multivibrator

9.5.1 A TWO-AMPLIFIER ONE-SHOT

A circuit for a two-amplifier one-shot is shown in *Figure 62*. As the resistor, R_2, from V^+ to the (−) input is smaller than R_5 (from V^+ to the (+) input), amplifier 2 will be biased to a low-voltage output in the quiescent state. As a result, no current is supplied to the (−) input of amplifier 1 (via R_3) which causes the output of this amplifier to be in the high voltage state. Capacitor C_1 therefore has essentially the full V^+ supply voltage across it ($V^+ - 2\ V_{BE}$). Now when a differentiated trigger (due to C_2) causes amplifier 1 to be driven ON (output voltage drops to essentially zero volts) this negative transient is coupled (via C_1) to the (−) input of amplifier 2 which causes the output of this amplifier to be driven high (to positive saturation). This condition remains while C_1 discharges via (R_1) from approximately V^+ to approximately $V^+/2$. This time interval is the pulse width (PW). After C_1 no longer diverts sufficient current of R_2 away from the (−) input of amplifier 2 (i.e., C_1 is discharged to approximately $V^+/2$ V) the stable DC state is restored—amplifier 2 output low and amplifier 1 output high.

This circuit can be rapidly re-triggered due to the action of the diode, CR_1. This re-charges C_1 as amplifier 1 drives full output current capability (approximately 10 mA) through C_1, CR_1 and into the saturated (−) input of amplifier 2 to ground. The only time limit is the 10 mA available from amplifier 1 and the value of C_1. If a rapid reset is not required, CR_1 can be omitted.

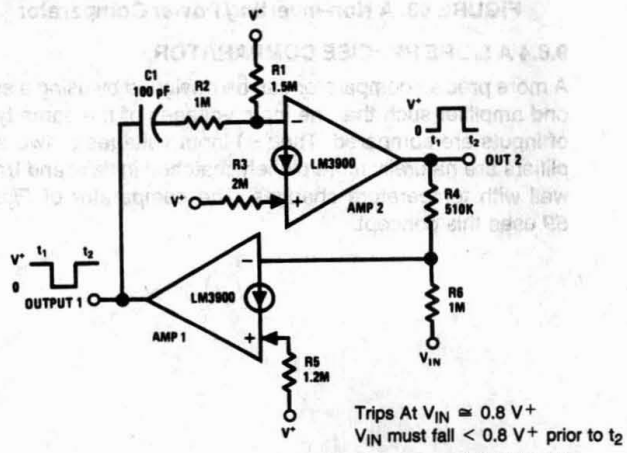

FIGURE 63. A One-shot Multivibrator with an Input Comparator

9.5.2 A COMBINATION ONE-SHOT/COMPARATOR CIRCUIT

In many applications a pulse is required if a DC input signal exceeds a predetermined value. This exists in free-running oscillators where after a particular output level has been reached a reset pulse must be generated to recycle the oscillator. This double function is provided with the circuit of *Figure 63*. The resistors R_5 and R_6 of amplifier 1 provide the inputs to a comparator and, as shown, an input signal, V_{IN}, is compared with the supply voltage, V^+. The output voltage of amplifier 1 is normally in a high voltage state and will fall and initiate the generation of the output pulse when V_{IN} is $R_6/R_5\ V^+$ or approximately 80% of V^+. To keep V_{IN} from disturbing the pulse generation it is required that V_{IN} fall to less than the trip voltage prior to the termination of the output pulse. This is the case when this circuit is used to generate a reset pulse and therefore this causes no problems.

9.5.3 A ONE-AMPLIFIER ONE-SHOT (POSITIVE PULSE)

A one-shot circuit can be realized using only one amplifier as shown in *Figure 64*.

The resistor R_2 keeps the output in the low voltage state. A differentiated positive trigger causes the output to switch to the high voltage state and resistor R_5 latches this state. The capacitor, C_1, charges from essentially ground to approximately $V^+/4$ where the circuit latches back to the quiescent state. The diode, CR_1, is used to allow a rapid re-triggering.

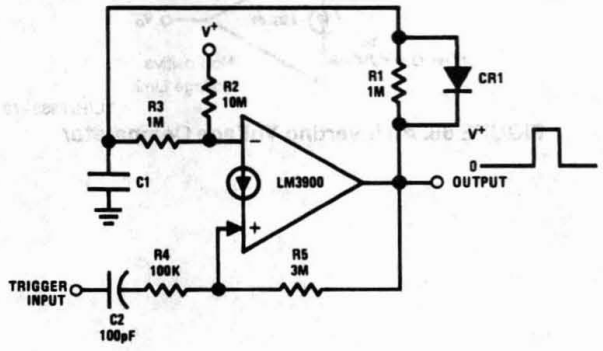

FIGURE 64. A One-amplifier One-shot (Positive Output)

9.5.4 A ONE-AMPLIFIER ONE-SHOT (NEGATIVE PULSE)

A one-amplifier one-shot multivibrator which has a quiescent state with the output high and which falls to zero volts for the pulse duration is shown in *Figure 65*.

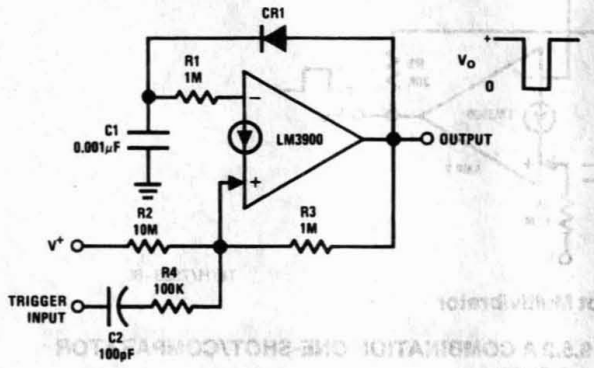

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FIGURE 65. A One-Amplifier One-Shot (Negative Output)

The sum of the currents through R_2 and R_3 keeps the (−) input at essentially ground. This causes V_O to be in the high voltage state. A differentiated negative trigger waveform causes the output to switch to the low voltage state. The large voltage across C_1 now provides input current via R_1 to keep the output low until C_1 is discharged to approximately $V^+/10$. At this time the output switches to the stable high voltage state.

If the R_4C_2 network is moved to the (−) input terminal, the circuit will trigger on a differentiated positive trigger waveform.

9.6 COMPARATORS

The voltage comparator is a function required for most system operations and can easily be performed by the LM3900. Both an inverting and a non-inverting comparator can be obtained.

9.6.1 A COMPARATOR FOR POSITIVE INPUT VOLTAGES

The circuit in *Figure 66* is an inverting comparator. To insure proper operation, the reference voltage must be larger than V_{BE}, but there is no upper limit as long as the input resistor is large enough to guarantee that the input current will not exceed 200 μA.

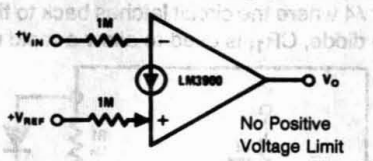

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FIGURE 66. An Inverting Voltage Comparator

9.6.2 A COMPARATOR FOR NEGATIVE INPUT VOLTAGES

Adding a common-mode biasing network to the comparator in *Figure 66* makes it possible to compare voltages between zero and one volt as well as the comparison of rather large negative voltages, *Figure 67*. When working with negative voltages, the current supplied by the common-mode network must be large enough to satisfy both the current drain demands of the input voltages and the bias current requirement of the amplifier.

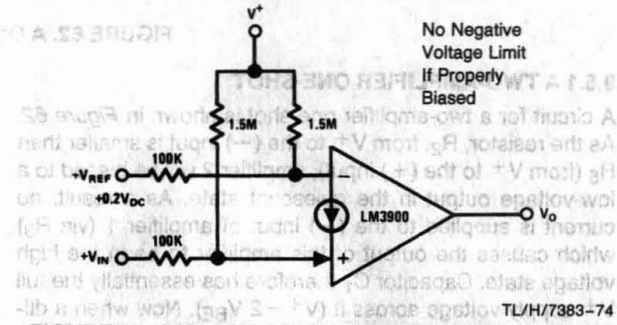

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FIGURE 67. A Non-Inverting Low-voltage Comparator

9.6.3 A POWER COMPARATOR

When used in conjunction with an external transistor, this power comparator will drive loads which require more current than the IC amplifier is capable of supplying. *Figure 68* shows a non-inverting comparator which is capable of driving a 12V, 40 mA panel lamp.

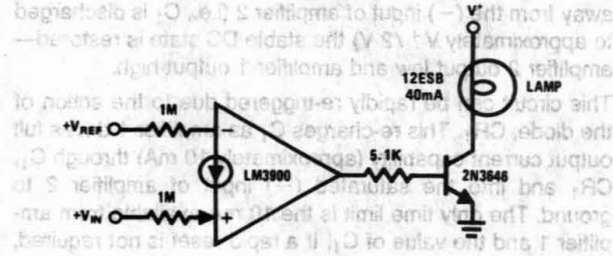

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FIGURE 68. A Non-Inverting Power Comparator

9.6.4 A MORE PRECISE COMPARATOR

A more precise comparator can be designed by using a second amplifier such that the input voltages of the same type of inputs are compared. The (−) input voltages of two amplifiers are naturally more closely matched initially and track well with temperature changes. The comparator of *Figure 69* uses this concept.

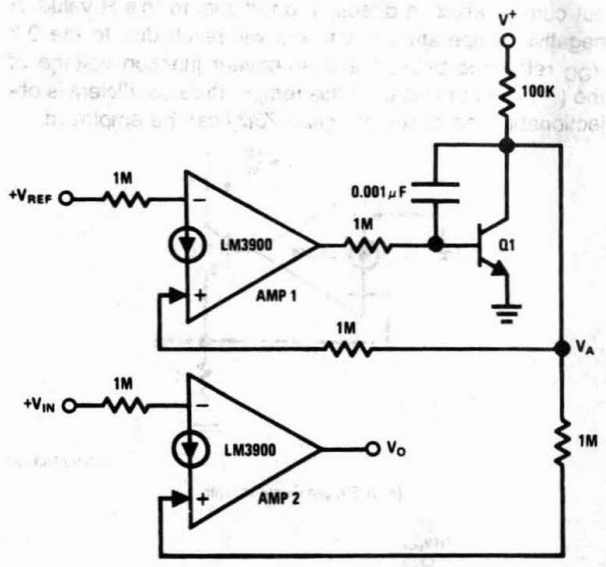

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FIGURE 69. A More Precise Comparator

The current established by V_{REF} at the inverting input of amplifier 1 will cause transistor Q_1 to adjust the value of V_A to supply this current. This value of V_A will cause an equal current to flow into the non-inverting input of amplifier 2. This current corresponds more exactly to the reference current of amplifier 1.

A differential input stage can also be added to the LM3900 (see section 10.16) and the resulting circuit can provide a precision comparator circuit.

9.7 SCHMITT TRIGGERS

Hysteresis may be designed into comparators which use the LM3900 as shown in *Figure 70.*

The lower switch point for the inverting Schmitt-Trigger is determined by the amount of current flowing into the positive input with the output voltage low. When the input current, I_3, drops below the level required by the current mirror, the output will switch to the high limit. With V_O high, the current demanded by the mirror is increased by a fixed amount, I_2. As a result, the I_3 required to switch the output increases this same amount. Therefore, the switch points are determined by selecting resistors which will establish the required currents at the desired input voltages. Reference current (I_1) and feedback current (I_2) are set by the following equation.

$$I_1 = \frac{V^+ - \phi}{R_B}$$

$$I_2 = \frac{V_{O\,MAX} - \phi}{R_F}$$

By adjusting the values of R_B, R_F, and R_{IN}, the switching values of V_{IN} may be set to any levels desired.

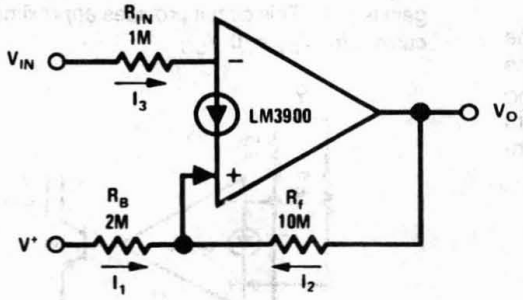
The non-inverting Schmitt Trigger works in the same way except that the input voltage is applied to the (+) input. The range of V_{IN} may be very large when compared with the operating voltage of the amplifier.

10.0 Some Special Circuit Applications

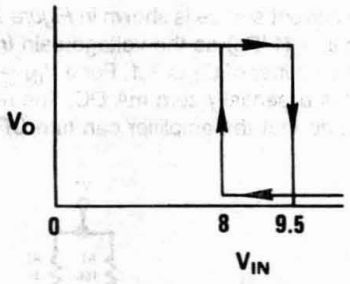
This section contains various special circuits which did not fit the order of things or which are one-of-a-kind type of applications.

10.1 CURRENT SOURCES AND SINKS

The amplifiers of the LM3900 can be used in feedback loops which regulate the current in external PNP transistors to provide current sources or in external NPN transistors to provide current sinks. These can be multiple sources or single sources which are fixed in value or made voltage variable.



(a) Inverting



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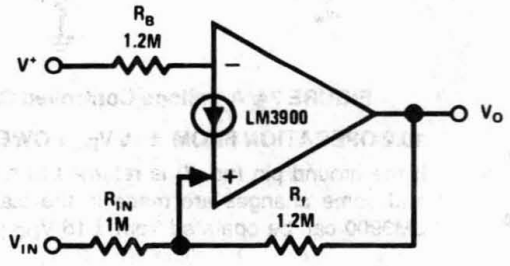

(b) Non-inverting

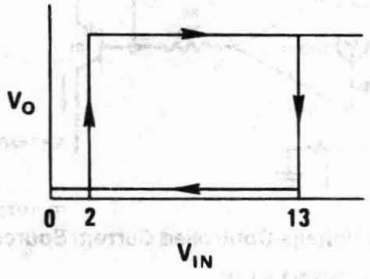

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FIGURE 70. Schmitt Triggers

10.1.1 A FIXED CURRENT SOURCE

A multiple fixed current source is provided by the circuit of *Figure 71*. A reference voltage (1 V_{DC}) is established across resistor R_3 by the resistive divider (R_3 and R_4). Negative feedback is used to cause the voltage drop across R_1 to also be 1 V_{DC}. This controls the emitter current of transistor Q_1 and if we neglect the small current diverted into the (−) input via the 1M input resistor (13.5 μA) and the base current of Q_1 and Q_2 (an additional 2% loss if the β of these transistors is 100), essentially this same current is available out of the collector of Q_1.

Larger input resistors can be used to reduce current loss and a Darlington connection can be used to reduce errors due to the β of Q_1.

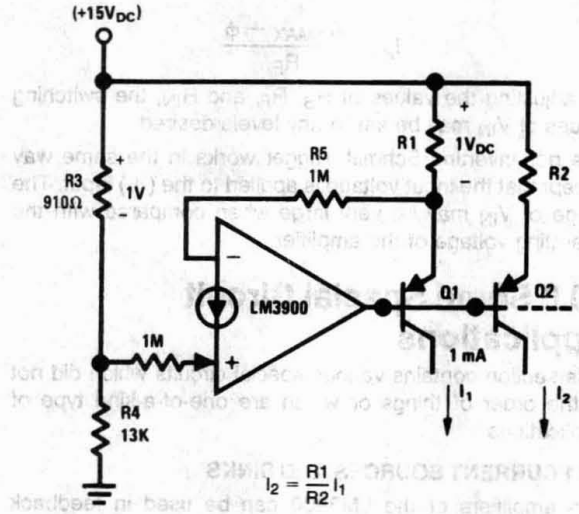

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FIGURE 71. Fixed Current Sources

The resistor, R_2, can be used to scale the collector current of Q_2 either above or below the 1 mA reference value.

10.1.2 A VOLTAGE VARIABLE CURRENT SOURCE

A voltage variable current source is shown in *Figure 72*. The transconductance is $-(1/R_2)$ as the voltage gain from the input terminal to the emitter of Q_1 is −1. For a V_{IN} = 0 V_{DC} the output current is essentially zero mA DC. The resistors R_1 and R_6 guarantee that the amplifier can turn OFF transistor Q_1.

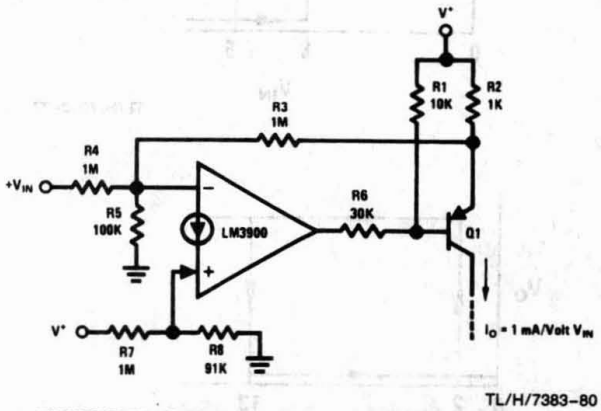

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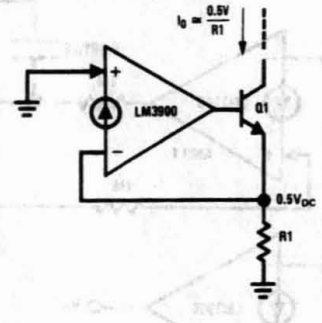
FIGURE 72. A Voltage Controlled Current Source

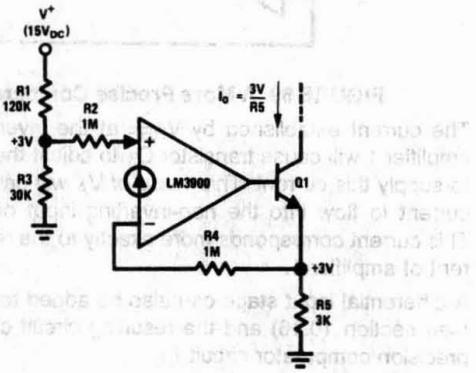
10.1.3 A FIXED CURRENT SINK

Two current sinks are shown in *Figure 73*. The circuit of *Figure 73(a)* requires only one resistor and supplies an output current which is directly proportional to this R value. A negative temperature coefficient will result due to the 0.5 V_{DC} reference being the base-emitter junction voltage of the (−) input transistor. If this temperature coefficient is objectionable, the circuit of *Figure 73(b)* can be employed.



TL/H/7383–81

(a) A Simple Current Sink



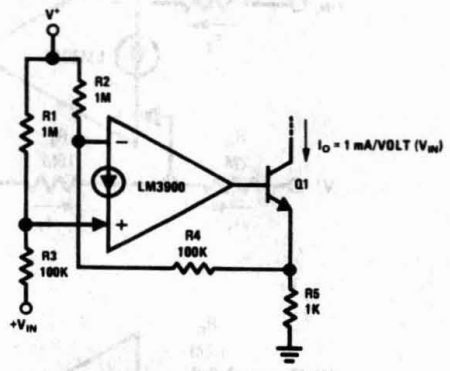
TL/H/7383–82

(b) Reducing Temperature Drift Of I_O

FIGURE 73. Fixed Current Sinks

10.1.4 A VOLTAGE VARIABLE CURRENT SINK

A voltage variable current sink is shown in *Figure 74*. The output current is 1 mA per volt of V_{IN} (as R_5 = 1 kΩ and the gain is +1). This circuit provides approximately 0 mA output current for V_{IN} = 0 V_{DC}.



TL/H/7383–83

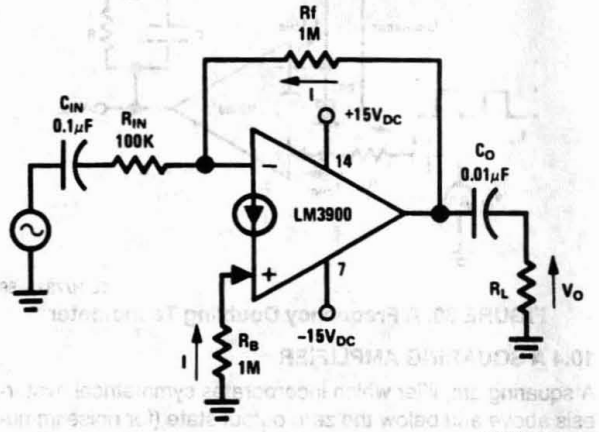
FIGURE 74. A Voltage Controlled Current Sink

10.2 OPERATION FROM ±15 V_{DC} POWER SUPPLIES

If the ground pin (no. 7) is returned to a negative voltage and some changes are made in the biasing circuits, the LM3900 can be operated from ±15 V_{DC} power supplies.

10.2.1 AN AC AMPLIFIER OPERATING WITH ±15 V_{DC} POWER SUPPLIES

An AC coupled amplifier is shown in *Figure 75*. The biasing resistor, R_B, is now returned to ground and both inputs bias at one V_{BE} above the $-V_{EE}$ voltage (approximately -15 V_{DC}).



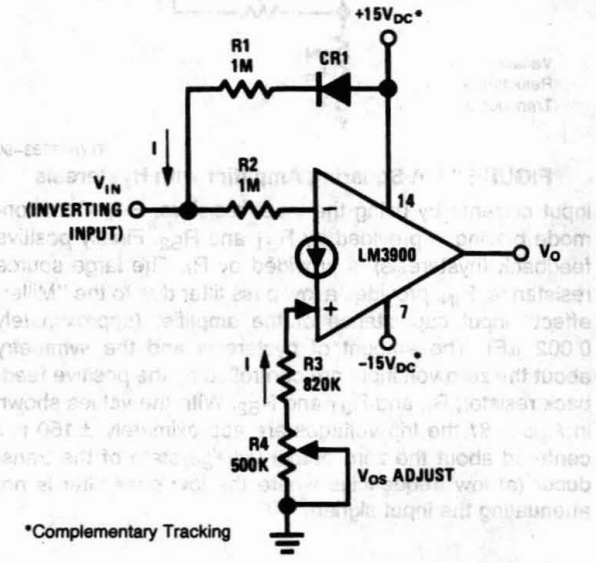
TL/H/7383–84

FIGURE 75. An AC Amplifier Operating With ±15 V_{DC}

With $R_f = R_B$, V_O will bias at approximately 0 V_{DC} to allow a maximum output voltage swing. As pin 7 is common to all four of the amplifiers which are in the same package, the other amplifiers are also biased for operation off of ±15 V_{DC}.

10.2.2 A DC AMPLIFIER OPERATING WITH ±15 V_{DC} POWER SUPPLIES

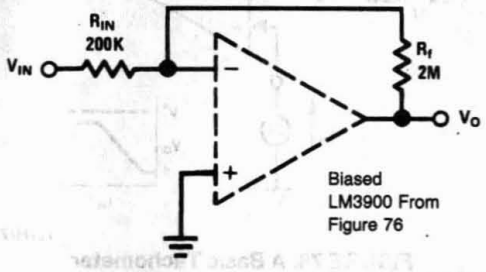
Biasing a DC amplifier is more difficult and requires that the ± power supplies be complementary tracking (i.e., $|+V_{CC}| = |-V_{EE}|$). The operation of this biasing can be understood if we start by first considering the amplifier without including the feedback resistors, as shown in *Figure 76*. If $R_1 = R_2 = R_3 + R_4 = 1\ M\Omega$ and $|+V_{CC}| = |-V_{EE}|$,



TL/H/7383–85

FIGURE 76. DC Biasing for ±15 V_{DC} Operation

then the current, I, will bias V_{IN} at zero volts DC (resistor R_4 can be used to adjust this). The diode, CR_1, has been added for temperature compensation of this biasing. Now, if we include these biasing resistors, we have a DC amplifier with the input biased at approximately zero volts. If feedback resistors are added around this biased amplifier we get the schematic shown in *Figure 77*.



TL/H/7383–86

FIGURE 77. A DC Amplifier Operating with ±15 V_{DC}

This is a standard inverting DC amplifier connection. The (+) input is "effectively" at ground and the biasing shown in *Figure 76* is used to take care of DC levels at the inputs.

10.3 TACHOMETERS

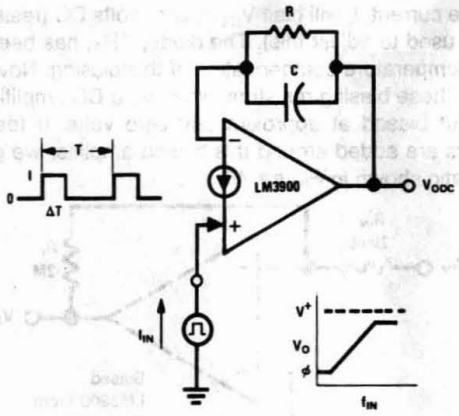
Many pulse averaging tachometers can be built using the LM3900. Inputs can be voltage pulses, current pulses or the differentiated transitions of squarewaves. The DC output voltage can be made to increase with increasing input frequency, can be made proportional to twice the input frequency (frequency doubling for reduced output ripple), and can also be made proportional to either the sum or the difference between two input frequencies. Due to the small bias current and the high gain of the LM3900, the transfer function is linear between the saturation states of the amplifier.

10.3.1 A BASIC TACHOMETER

If an RC averaging network is added from the output to the (−) input, the basic tachometer of *Figure 78* results. Current pulse inputs will provide the desired transfer function shown on the figure. Each input current pulse causes a small change in the output voltage. Neglecting the effects of R we have

$$\Delta V_O \cong \frac{I\Delta t}{C}$$

The inclusion of R gives a discharge path so the output voltage does not continue to integrate, but rather provides the time dependency which is necessary to average the input pulses. If an additional signal source is simply placed in parallel with the one shown, the output becomes proportional to the sum of these input frequencies. If this additional source were applied to the (−) input, the output voltage would be proportional to the difference between these input frequencies. Voltage pulses can be converted to current pulses by using an input resistor. A series isolating diode should be used if a signal is applied to the (−) input to prevent loading during the low voltage state of this input signal.

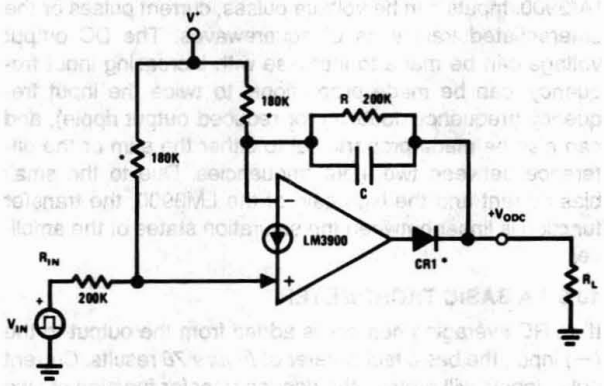


TL/H/7383–87

FIGURE 78. A Basic Tachometer

10.3.2 EXTENDING V_{OUT} (MINIMUM) TO GROUND

The output voltage of the circuit of *Figure 78* does not go to ground level but has a minimum value which is equal to the V_{BE} of the (−) input (0.5 V_{DC}). If it is desired that the output voltage go exactly to ground, the circuit of *Figure 79* can be used. Now with V_{IN} = 0 V_{DC}, V_O = 0 V_{DC} due to the addition of the common-mode biasing resistors (180 kΩ).



TL/H/7383–88

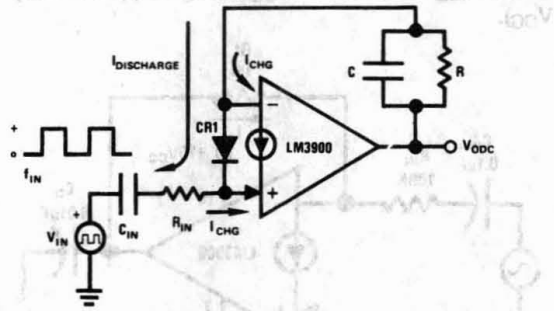
FIGURE 79. Adding Biasing to Provide V_O = 0 V_{DC}

The diode, CR_1, allows the output to go below $V_{CE\ SAT}$ of the output, if desired (a load is required to provide a DC path for the biasing current flow via the R of the averaging network).

10.3.3 A FREQUENCY DOUBLING TACHOMETER

To reduce the ripple on the DC output voltage, the circuit of *Figure 80* can be used to effectively double the input frequency. Input pulses are not required, a squarewave is all that is needed. The operation of the circuit is to average the charge and discharge transient currents of the input capacitor, C_{IN}. The resistor, R_{IN}, is used to convert the voltage pulses to current pulses and to limit the surge currents (to approximately 200 μA peak—or less if operating at high temperatures).

When the input voltage goes high, the charging current of C_{IN}, I_{CHG} enters the (+) input, is mirrored about ground and is drawn from the RC averaging network into the (−) input terminal. When the input voltage goes back to ground, the discharge current of C_{IN}, $I_{DISCHARGE}$ will also be drawn from the RC averaging network via the now conducting diode, CR_1. This full wave action causes two current pulses to be drawn through the RC averaging network for each cycle of the input frequency.

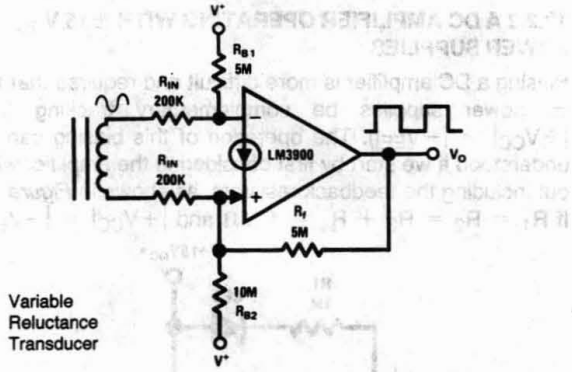


TL/H/7333–89

FIGURE 80. A Frequency Doubling Tachometer

10.4 A SQUARING AMPLIFIER

A squaring amplifier which incorporates symmetrical hysteresis above and below the zero output state (for noise immunity) is often needed to amplify the low level signals which are provided by variable reluctance transducers. In addition, a high frequency roll-off (low pass characteristic) is desirable both to reduce the natural voltage buildup at high frequencies and to also filter high frequency input noise disturbances. A simple circuit which accomplishes this function is shown in *Figure 81*. The input voltage is converted to



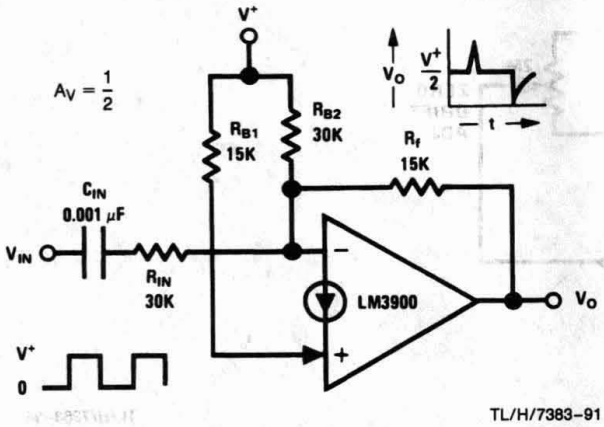
TL/H/7383–90

FIGURE 81. A Squaring Amplifier with Hysteresis

input currents by using the input resistors, R_{IN}. Common-mode biasing is provided by R_{B1} and R_{B2}. Finally positive feedback (hysteresis) is provided by R_f. The large source resistance, R_{IN}, provides a low pass filter due to the "Miller-effect" input capacitance of the amplifier (approximately 0.002 μF). The amount of hysteresis and the symmetry about the zero volt input are controlled by the positive feedback resistor, R_f, and R_{B1} and R_{B2}. With the values shown in *Figure 81* the trip voltages are approximately ±150 mV centered about the zero output voltage state of the transducer (at low frequencies where the low pass filter is not attenuating the input signal).

10.5 A DIFFERENTIATOR

An input differentiating capacitor can cause the input of the LM3900 to swing below ground and actuate the input clamp circuit. Again, common-mode biasing can be used to prevent this negative swing at the input terminals of the LM3900. The schematic of a differentiator circuit is shown in *Figure 82*. Common-mode biasing is provided by R_{B1} and



TL/H/7383–91

FIGURE 82. A Differentiator Circuit

R_{B2}. The feedback resistor, R_f, is one-half the value of R_{IN} so the gain is 1/2. The output voltage will bias at $V^+/2$ which thereby allows both a positive and a negative swing above and below this bias point. The resistor, R_{IN}, keeps the negative swing isolated from the (−) input terminal and therefore both inputs remain biased at $+V_{BE}$.

10.6 A DIFFERENCE INTEGRATOR

A difference integrator is the basis of many of the sweep circuits which can be realized using the LM3900 operating on only a single power supply voltage. This circuit can also be used to provide the time integral of the difference between two input waveforms. The schematic of the difference integrator is shown in *Figure 83*.

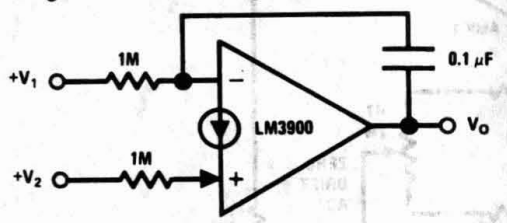


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FIGURE 83. A Difference Integrator

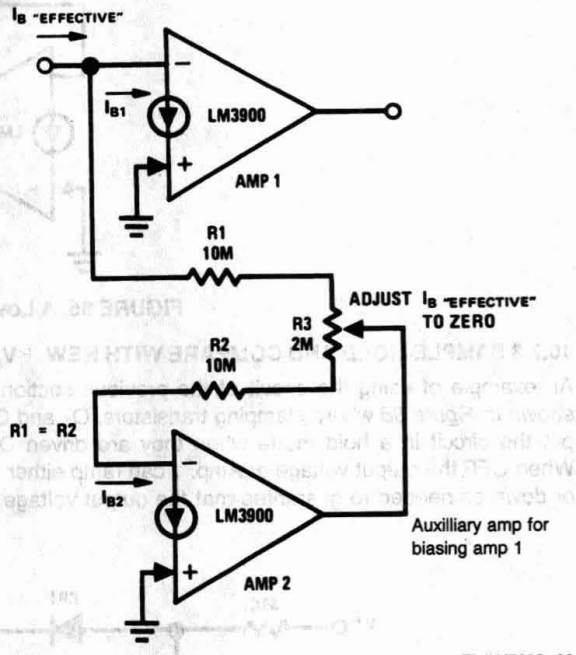
This is a useful component for DC feedback loops as both the comparison to a reference and the integration take place in one amplifier.

10.7 A LOW DRIFT SAMPLE AND HOLD CIRCUIT

In sample and hold applications a very low input biasing current is required. This is usually achieved by using a FET transistor or a special low input current IC op amp. The existence of many matched amplifiers in the same package allows the LM3900 to provide some interesting low "equivalent" input biasing current applications.

10.7.1 REDUCING THE "EFFECTIVE" INPUT BIASING CURRENT

One amplifier can be used to bias one or more additional amplifiers as shown in *Figure 84*.



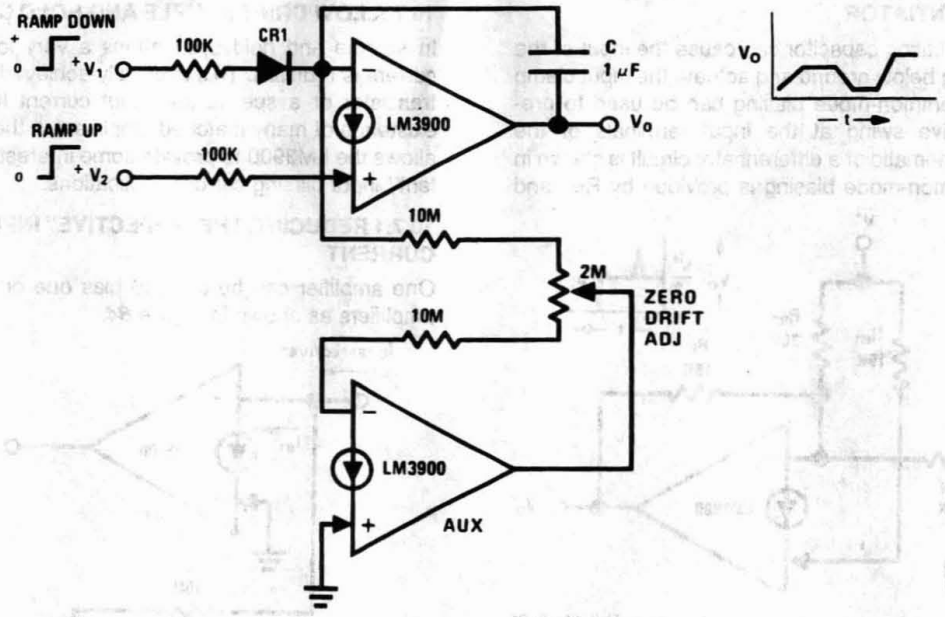
TL/H/7383–93

FIGURE 84. Reducing I_B "Effective" to Zero

The input terminal of Amp. 1 will only need to supply the signal current if the DC biasing current, I_{B1}, is accurately supplied via R_1. The adjustment, R_3, allows a zeroing of "I_B effective" but simply omitting R_3 and letting $R_1 = R_2$ (and relying on amplifier symmetry) can cause I_B "effective" to be less than $I_B/10$ (3 nA). This is useful in circuit applications such as sample and hold, where small values of I_B "effective" are desirable.

10.7.2 A LOW DRIFT RAMP AND HOLD CIRCUIT

The input current reduction technique of the previous section allows a relatively simple ramp and hold circuit to be built which can be ramped up or down or allowed to remain at any desired output DC level in a "hold" mode. This is shown in *Figure 85*. If both inputs are at 0 V_{DC} the circuit is in a hold mode. Raising either input will cause the DC output voltage to ramp either up or down depending on which one goes positive. The slope is a function of the magnitude of the input voltage and additional inputs can be placed in parallel, if desired, to increase the input control variables.

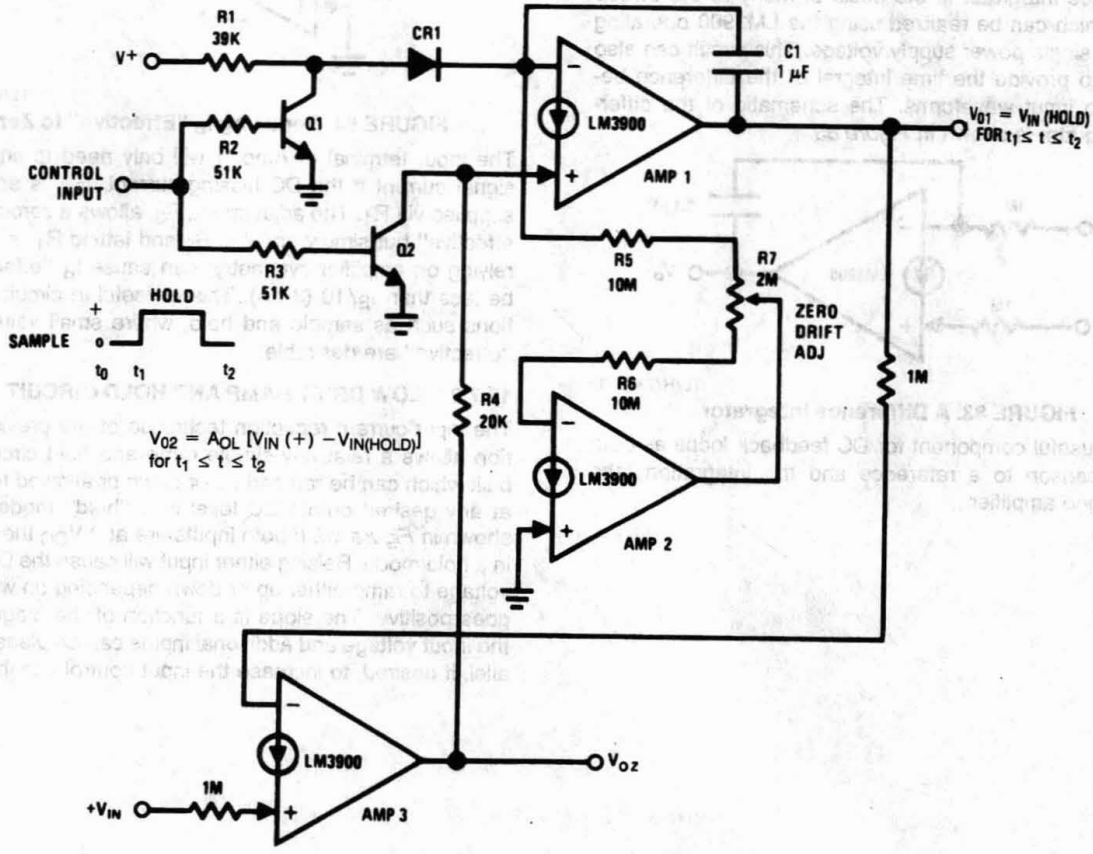


TL/H/7383–94

FIGURE 85. A Low-Drift Ramp and Hold Circuit

10.7.3 SAMPLE-HOLD AND COMPARE WITH NEW $+V_{IN}$

An example of using the circuit of the previous section is shown in *Figure 86* where clamping transistors, Q_1 and Q_2, put the circuit in a hold mode when they are driven ON. When OFF the output voltage of Amp. 1 can ramp either up or down as needed to guarantee that the output voltage of Amp. 1 is equal to the DC input voltage which is applied to Amp. 3. Resistor R_1 provides a fixed "down" ramp current which is balanced or controlled via the comparator, Amp. 3, and the resistor R_4. When Q_1 and Q_2 are OFF a feedback loop guarantees that V_{01} (from Amp. 1) is equal to $+V_{IN}$ (to Amp. 3). Amplifier 2 is used to supply the input biasing current to Amp. 1.



TL/H/7383–95

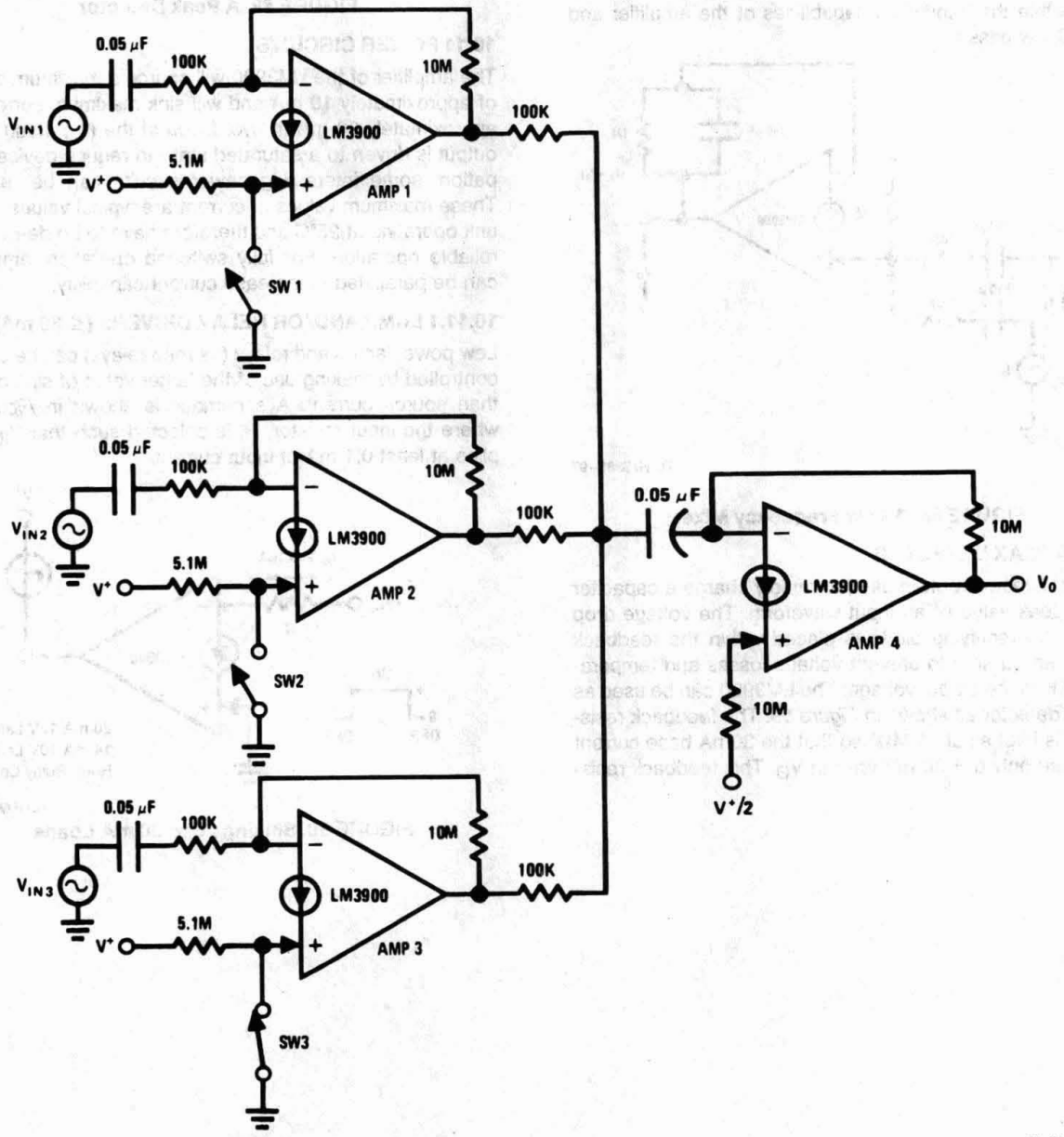
FIGURE 86. Sample-Hold and Compare with New $+V_{IN}$

The stored voltage appears at the output, V_{01} of Amp. 1, and as Amp. 3 is active, a continued comparison is made between V_{01} and V_{IN} and the output of Amp. 3 fully switches based on this comparison. A second loop could force V_{IN} to be maintained at the stored value (V_{01}) by making use of V_{02} as an error signal for this second loop. Therefore, a control system could be manually controlled to bring it to a particular operating condition; then, by exercising the hold control, the system would maintain this operating condition due to the analog memory provided by V_{01}.

10.8 AUDIO MIXER OR CHANNEL SELECTOR

The multiple amplifiers of the LM3900 can be used for audio mixing (many amplifiers simultaneously providing signals which are added to generate a composite output signal) or for channel selection (only one channel enabled at a time). Three amplifiers are shown being summed into a fourth amplifier in *Figure 87*.

If a power amplifier were available, all four amplifiers could feed the single input of the power amplifier. For audio mixing all amplifiers are simultaneously active. Particular amplifiers can be gated OFF by making use of DC control signals which are applied to the (+) inputs to provide a channel select feature. As shown on *Figure 87*, Amp. 3 is active (as sw 3 is closed) and Amps. 1 and 2 are driven to positive output voltage saturation by the 5.1M which is applied to the (+) inputs. The DC output voltage bias level of the active amplifier is approximately 0.8 V_{DC} and could be raised if larger signal levels were to be accommodated. Frequency shaping networks can be added either to the individual amplifiers or to the common amplifier, as desired. Switching transients may need to be filtered at the DC control points if the output amplifier is active during the switching intervals.



TL/H/7383–96

FIGURE 87. Audio Mixing or Selection

10.9 A LOW FREQUENCY MIXER

The diode which exists at the (+) input can be used for nonlinear signal processing. An example of this is a mixer which allows two input frequencies to produce a sum and difference frequency (in addition to other high frequency components). Using the amplifier of the LM3900, gain and filtering can also be accomplished with the same circuit in addition to the high input impedance and low output impedance advantages. The schematic of *Figure 88* shows a mixer with a gain of 10 and a low pass single pole filter (1M and 150 pF feedback elements) with a corner frequency of 1 kHz. With one signal larger in amplitude, to serve as the local oscillator input (V_1), the transconductance of the input diode is gated at this rate (f_1). A small signal (V_2) can now be added at the second input and the difference frequency is filtered from the composite resulting waveform and is made available at the output. Relatively high frequencies can be applied at the inputs as long as the desired difference frequency is within the bandwidth capabilities of the amplifier and the RC low pass filter.

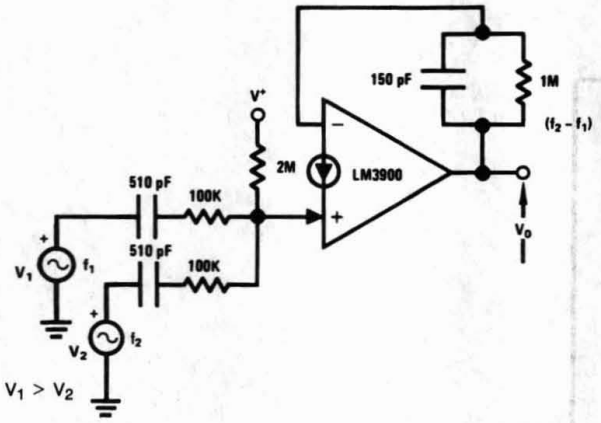


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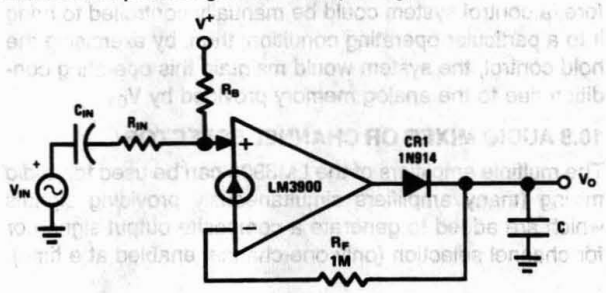
FIGURE 88. A Low Frequency Mixer

10.10 A PEAK DETECTOR

A peak detector is often used to rapidly charge a capacitor to the peak value of an input waveform. The voltage drop across the rectifying diode is placed within the feedback loop of an op amp to prevent voltage losses and temperature drifts in the output voltage. The LM3900 can be used as a peak detector as shown in *Figure 89*. The feedback resistor, R_f, is kept small (1 MΩ) so that the 30 nA base current will cause only a +30 mV error in V_O. This feedback resistor is constantly loading C in addition to the current drawn by the circuitry which samples V_O. These loading effects must be considered when selecting a value for C.

The biasing resistor, R_B, allows a minimum DC voltage to exist across the capacitor and the input resistor, R_{IN}, can be selected to provide gain to the input signal.



TL/H/7383–98

FIGURE 89. A Peak Detector

10.11 POWER CIRCUITS

The amplifier of the LM3900 will source a maximum current of approximately 10 mA and will sink maximum currents of approximately 80 mA (if overdriven at the (−) input). If the output is driven to a saturated state to reduce device dissipation, some interesting power circuits can be realized. These maximum values of current are typical values for the unit operating at 25°C and therefore have to be de-rated for reliable operation. For fully switched operation, amplifiers can be paralleled to increase current capability.

10.11.1 LAMP AND/OR RELAY DRIVERS (≤ 30 mA)

Low power lamps and relays (as reed relays) can be directly controlled by making use of the larger value of sink current than source current. A schematic is shown in *Figure 90* where the input resistor, R, is selected such that V_{IN} supplies at least 0.1 mA of input current.

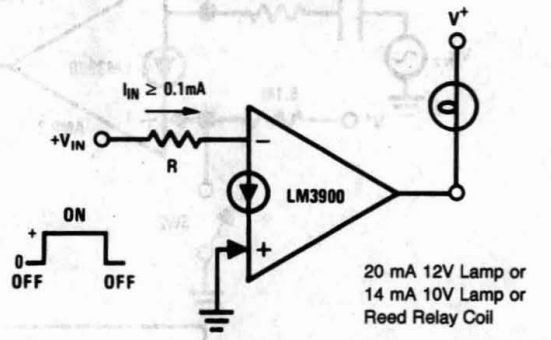


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FIGURE 90. Sinking 20 to 30 mA Loads

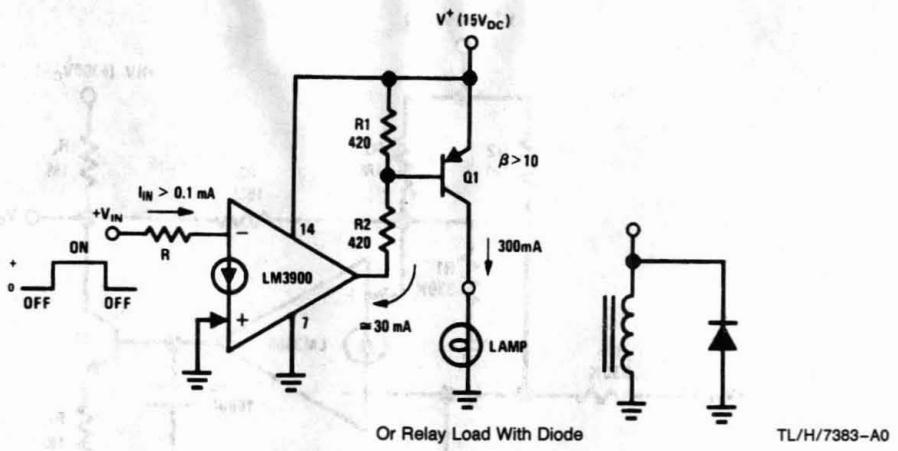


FIGURE 91. Boosting to 300 mA Loads

10.11.2 LAMP AND/OR RELAY DRIVERS (≤ 300 mA)

To increase the power capability, an external transistor can be added as shown in *Figure 91*. The resistors R_1 and R_2 hold Q_1 OFF when the output of the LM3900 is high. The resistor, R_2, limits the base drive when Q_1 goes ON. It is required that pin 14 tie to the same power supply as the emitter of Q_1 to guarantee that Q_1 can be held OFF. If an inductive load is used, such as a relay coil, a backswing diode should be added to prevent large inductive voltage kicks during the switching interval, ON to OFF.

10.11.3 POSITIVE FEEDBACK OSCILLATORS

If the LM3900 is biased into the active region and a resonant circuit is connected from the output to the (+) input, a positive feedback oscillator results. A driver for a piezoelectric transducer (a warning type of noise maker) is shown in *Figure 92*. The resistors R_1 and R_2 bias the output voltage at $V^+/2$ and keep the amplifier active. Large currents can be entered into the (+) input and negative currents (or currents out of this terminal) are provided by the epi-substrate diode of the IC fabrication.

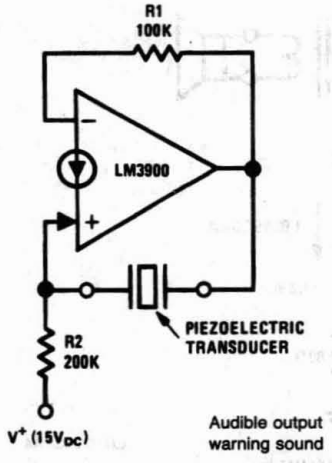


FIGURE 92. Positive Feedback Power Oscillators

When one of the amplifiers is operated in this large negative input current mode, the other amplifiers will be disturbed due to interaction. Multiple sounds may be generated as a result of using two or more transducers in various combinations, but this has not been investigated. Other two-terminal RC, RLC or piezoelectric resonators can be connected in this circuit to produce an oscillator.

10.12 HIGH VOLTAGE OPERATION

The amplifiers of the LM3900 can drive an external high voltage NPN transistor to provide a larger output voltage swing (as for an electrostatic CRT deflection system) or to operate off of an existing high voltage power supply (as the +98 V_{DC} rectified line). Examples of both types of circuits are presented in this section.

10.12.1 A HIGH VOLTAGE INVERTING AMPLIFIER

An inverting amplifier with an ouput voltage swing from essentially 0 V_{DC} to +300 V_{DC} is shown in *Figure 93*. The transistor, Q_1, must be a high breakdown device as it will have the full HV supply across it. The biasing resistor R_3 is used to center the transfer characteristic and the gain is the ratio of R_2 to R_1. The load resistor, R_L, can be increased, if desired, to reduce the HV current drain.

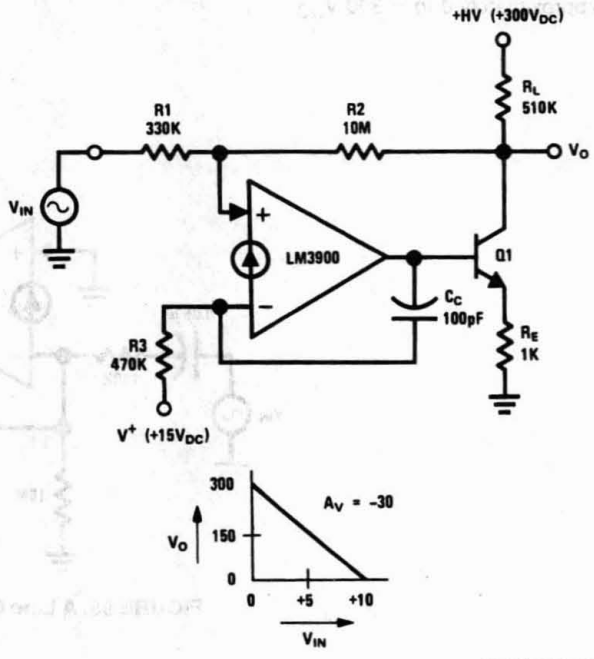
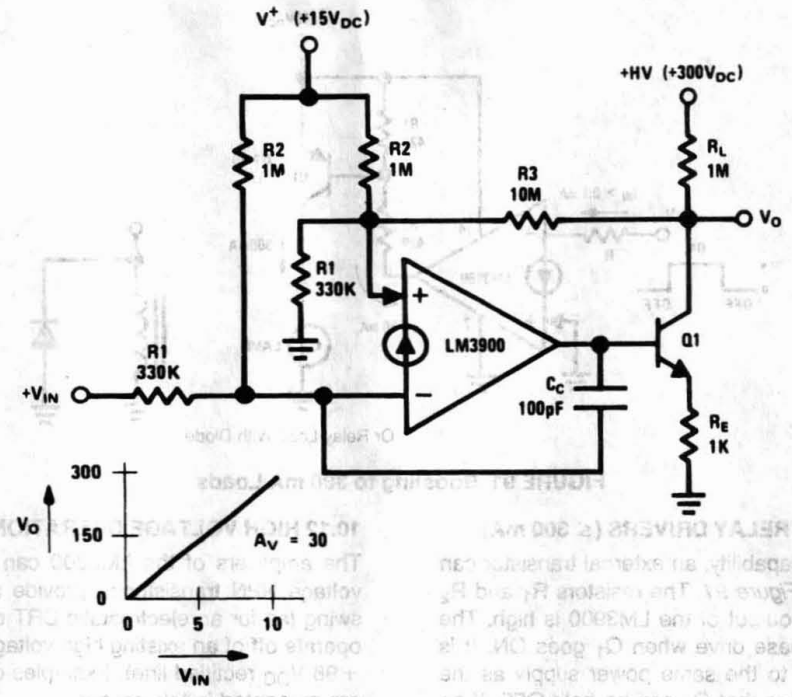


FIGURE 93. A High Voltage Inverting Amplifier



TL/H/7383–A3

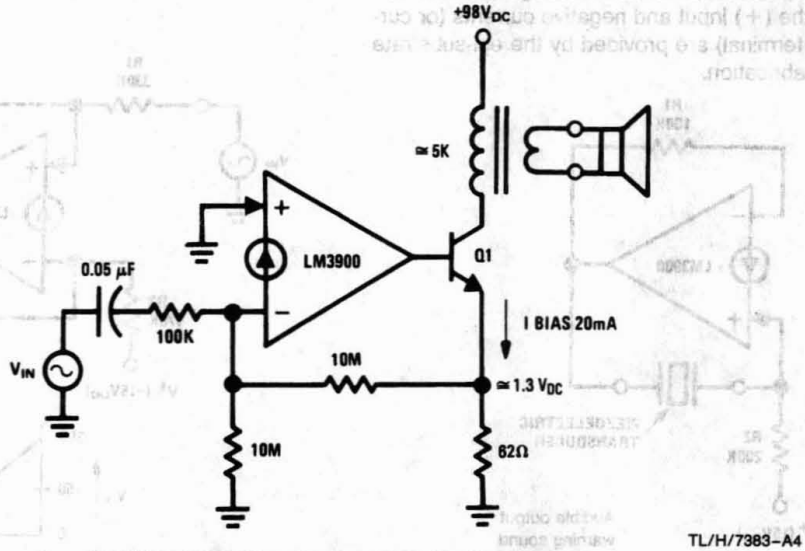
FIGURE 94. A High Voltage Non-Inverting Amplifier

10.12.2 A HIGH VOLTAGE NON-INVERTING AMPLIFIER

A high voltage non-inverting amplifier is shown in *Figure 94*. Common-mode biasing resistors (R_2) are used to allow V_{IN} to go to 0 V_{DC}. The output voltage, V_O, will not actually go to zero due to R_E, but should go to approximately 0.3 V_{DC}. Again, the gain is 30 and a range of the input voltage of from 0 to +10 V_{DC} will cause the output voltage to range from approximately 0 to +300 V_{DC}.

10.12.3 A LINE OPERATED AUDIO AMPLIFIER

An audio amplifier which operates off a +98 V_{DC} power supply (the rectified line voltage) is often used in consumer products. The external high voltage transistor, Q_1 of *Figure 95*, is biased and controlled by the LM3900. The magnitude of the DC biasing voltage which appears across the emitter resistor of Q_1 is controlled by the resistor which is placed from the (−) input to ground.



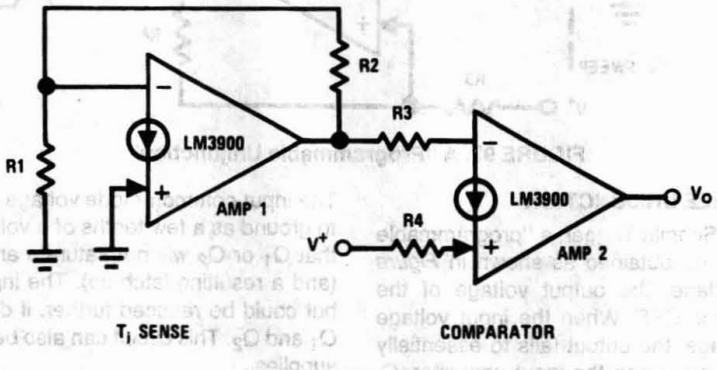
TL/H/7383–A4

FIGURE 95. A Line Operated Audio Amplifier

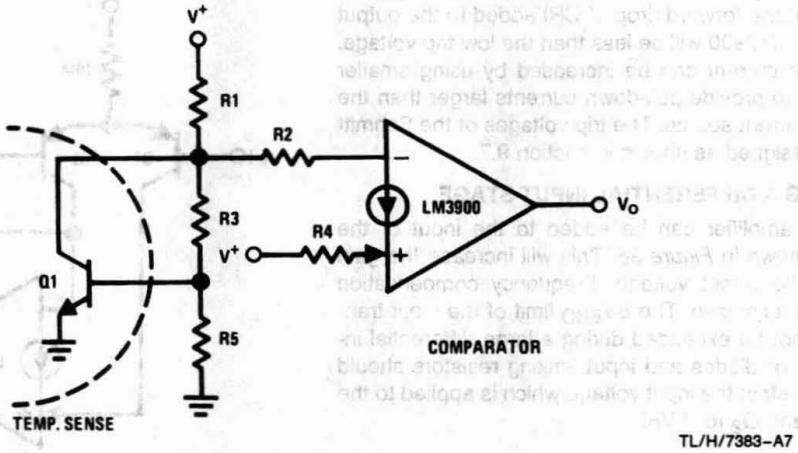
10.13 TEMPERATURE SENSING

The LM3900 can be used to monitor the junction temperature of the monolithic chip as shown in *Figure 96(a)*. Amp. 1 will generate an output voltage which can be designed to undergo a large negative temperature change by design of R_1 and R_2. The second amplifier compares this temperature dependent voltage with the power supply voltage and goes high at a designed maximum T_j of the IC.

For remote sensing, an NPN transistor, Q_1 of *Figure 96(b)*, is connected as an N V_{BE} generator (with R_3 and R_5) and biased via R_1 from the power supply voltage, V^+. The LM3900 again compares this temperature dependent voltage with the supply voltage and can be designed to have V_O go high at a maximum temperature of the remote temperature sensor, Q_1.



(a) IC T_j Monitor



(b) Remote Temperature Sense

FIGURE 96. Temperature Sensing

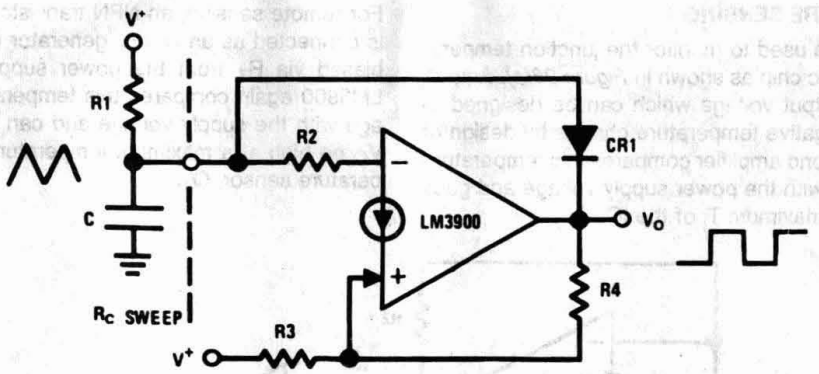


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FIGURE 97. A "Programmable Unijunction"

10.14 A "PROGRAMMABLE UNIJUNCTION"

If a diode is added to the Schmitt Trigger, a "programmable unijunction" function can be obtained as shown in *Figure 97*. For a low input voltage, the output voltage of the LM3900 is high and CRI is OFF. When the input voltage rises to the high trip voltage, the output falls to essentially 0V and CRI goes ON to discharge the input capacitor, C.

The low trip voltage must be larger than approximately 1V to guarantee that the forward drop of CRI added to the output voltage of the LM3900 will be less than the low trip voltage. The discharge current can be increased by using smaller values for R_2 to provide pull-down currents larger than the 1.3 mA bias current source. The trip voltages of the Schmitt Trigger are designed as shown in section 9.7.

10.15 ADDING A DIFFERENTIAL INPUT STAGE

A differential amplifier can be added to the input of the LM3900 as shown in *Figure 98*. This will increase the gain and reduce the offset voltage. Frequency compensation can be added as shown. The BV_{EBO} limit of the input transistors must not be exceeded during a large differential input condition, or diodes and input limiting resistors should be added to restrict the input voltage which is applied to the bases of Q_1 and Q_2 to $\pm V_D$.

The input common-mode voltage range does not go exactly to ground as a few tenths of a volt are needed to guarantee that Q_1 or Q_2 will not saturate and cause a phase change (and a resulting latch-up). The input currents will be small, but could be reduced further, if desired, by using FETS for Q_1 and Q_2. This circuit can also be operated off of $\pm 15\ V_{DC}$ supplies.

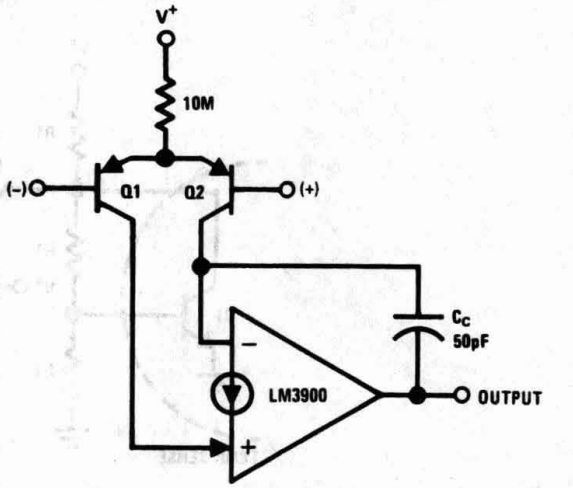

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FIGURE 98. Adding a Differential Input Stage

LM139/LM239/LM339 A Quad of Independently Functioning Comparators

National Semiconductor
Application Note 74

INTRODUCTION

The LM139/LM239/LM339 family of devices is a monolithic quad of independently functioning comparators designed to meet the needs for a medium speed, TTL compatible comparator for industrial applications. Since no antisaturation clamps are used on the output such as a Baker clamp or other active circuitry, the output leakage current in the OFF state is typically 0.5 nA. This makes the device ideal for system applications where it is desired to switch a node to ground while leaving it totally unaffected in the OFF state.

Other features include single supply, low voltage operation with an input common mode range from ground up to approximately one volt below V_{CC}. The output is an uncommitted collector so it may be used with a pull-up resistor and a separate output supply to give switching levels from any voltage up to 36V down to a $V_{CE\ SAT}$ above ground (approx. 100 mV), sinking currents up to 15 mA. In addition it may be used as a single pole switch to ground, leaving the switched node unaffected while in the OFF state. Power dissipation with all four comparators in the OFF state is typically 4 mW from a single 5V supply (1 mW/comparator).

CIRCUIT DESCRIPTION

Figure 1 shows the basic input stage of one of the four comparators of the LM139. Transistors Q_1 through Q_4 make up a PNP Darlington differential input stage with Q_5 and Q_6 serving to give single-ended output from differential input with no loss in gain. Any differential input at Q_1 and Q_4 will be amplified causing Q_6 to switch OFF or ON depending on input signal polarity. It can easily be seen that operation with an input common mode voltage of ground is possible. With both inputs at ground potential, the emitters of Q_1 and Q_4 will be at one V_{BE} above ground and the emitters of Q_2 and Q_3 at 2 V_{BE}. For switching action the base of Q_5 and Q_6 need only go to one V_{BE} above ground and since Q_2 and Q_3 can operate with zero volts collector to base, enough voltage is present at a zero volt common mode input to insure comparator action. The bases should not be taken more than several hundred millivolts below ground, however, to prevent forward biasing a substrate diode which would stop all comparator action and possibly damage the device, if very large input currents were provided.

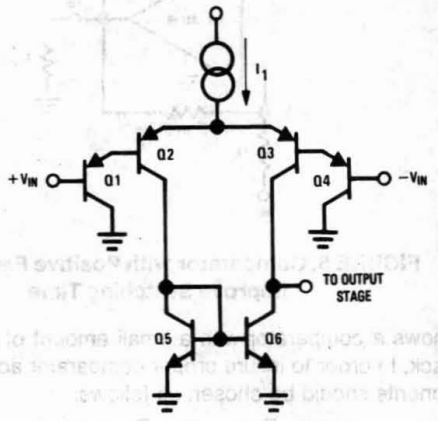

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FIGURE 1. Basic LM139 Input Stage

Figure 2 shows the comparator with the output stage added. Additional voltage gain is taken through Q_7 and Q_8 with the collector of Q_8 left open to offer a wide variety of possible applications. The addition of a large pull-up resistor from the collector of Q_8 to either $+V_{CC}$ or any other supply up to 36V both increases the LM139 gain and makes possible output switching levels to match practically any application. Several outputs may be tied together to provide an ORing function or the pull-up resistor may be omitted entirely with the comparator then serving as a SPST switch to ground.

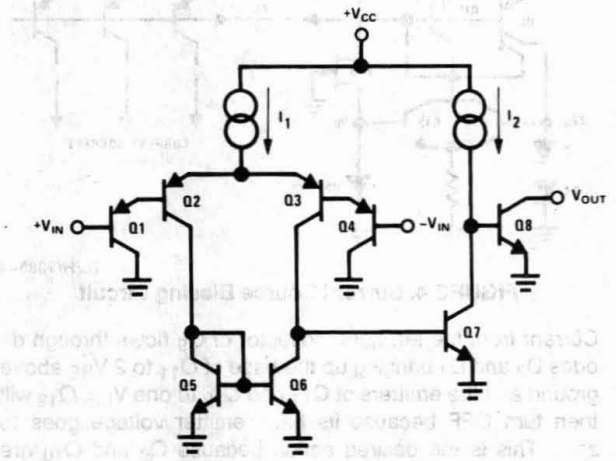

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FIGURE 2. Basic LM139 Comparator

Output transistor Q_8 will sink up to 15 mA before the output ON voltage rises above several hundred millivolts. The output current sink capability may be boosted by the addition of a discrete transistor at the output.

The complete circuit for one comparator of the LM139 is shown in *Figure 3*. Current sources I_3 and I_4 are added to help charge any parasitic capacitance at the emitters of Q_1 and Q_4 to improve the slew rate of the input stage. Diodes D_1 and D_2 are added to speed up the voltage swing at the emitters of Q_1 and Q_2 for large input voltage swings.

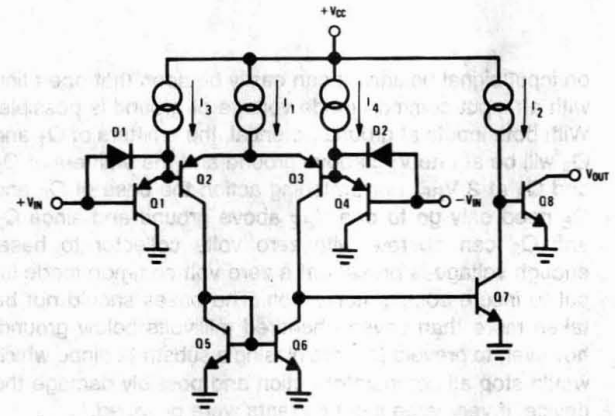

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FIGURE 3. Complete LM139 Comparator Circuit

Biasing for current sources I_1 through I_4 is shown in *Figure 4*. When power is first applied to the circuit, current flows through the JFET Q_{13} to bias up diode D_5. This biases transistor Q_{12} which turns ON transistors Q_9 and Q_{10} by allowing a path to ground for their base and collector currents.

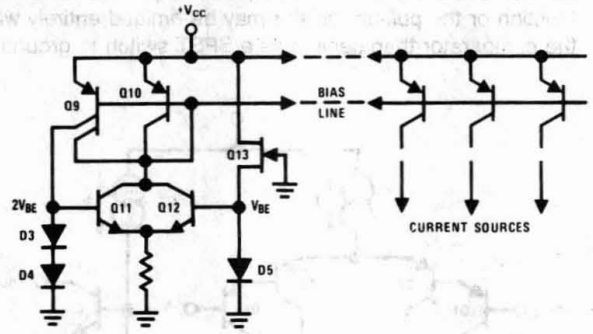

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FIGURE 4. Current Source Biasing Circuit

Current from the left hand collector of Q_9 flows through diodes D_3 and D_4 bringing up the base of Q_{11} to 2 V_{BE} above ground and the emitters of Q_{11} and Q_{12} to one V_{BE}. Q_{12} will then turn OFF because its base emitter voltage goes to zero. This is the desired action because Q_9 and Q_{10} are biased ON through Q_{11}, D_3 and D_4 so Q_{12} is no longer needed. The "bias line" is now sitting at a V_{BE} below $+V_{CC}$ which is the voltage needed to bias the remaining current sources in the LM139 which will have a constant bias regardless of $+V_{CC}$ fluctuations. The upper input common mode voltage is V_{CC} minus the saturation voltage of the current sources (appoximately 100 mV) minus the 2 V_{BE} of the input devices Q_1 and Q_2 (or Q_3 and Q_4).

COMPARATOR CIRCUITS

Figure 5 shows a basic comparator circuit for converting low level analog signals to a high level digital output. The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. Resistors R_1 and R_2 are used to set the input threshold trip voltage (V_{REF}) at any value desired within the input common mode range of the comparator.

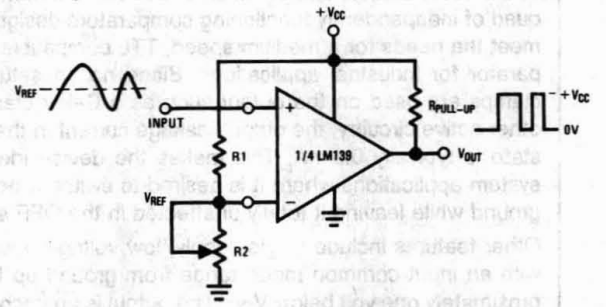

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FIGURE 5. Basic Comparator Circuit

COMPARATORS WITH HYSTERESIS

The circuit shown in *Figure 5* suffers from one basic drawback in that if the input signal is a slowly varying low level signal, the comparator may be forced to stay within its linear region between the output high and low states for an undesireable length of time. If this happens, it runs the risk of oscillating since it is basically an uncompensated, high gain op amp. To prevent this, a small amount of positive feedback or hysteresis is added around the comparator. *Figure 6* shows a comparator with a small amount of positive feedback. In order to insure proper comparator action, the components should be chosen as follows:

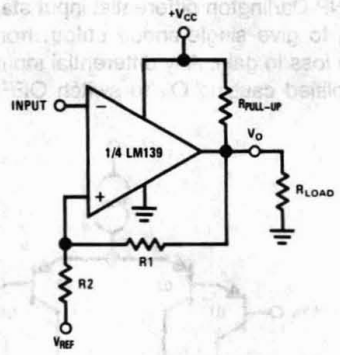

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FIGURE 6. Comparator with Positive Feedback to Improve Switching Time

$$R_{PULL\text{-}UP} < R_{LOAD} \text{ and}$$

$$R_1 > R_{PULL\text{-}UP}$$

This will insure that the comparator will always switch fully up to $+V_{CC}$ and not be pulled down by the load or feedback. The amount of feedback is chosen arbitrarily to insure proper switching with the particular type of input signal

used. If the output swing is 5V, for example, and it is desired to feedback 1% or 50 mV, then $R_1 \approx 100\ R_2$. To describe circuit operation, assume that the inverting input goes above the reference input ($V_{IN} > V_{REF}$). This will drive the output, V_O, towards ground which in turn pulls V_{REF} down through R_1. Since V_{REF} is actually the noninverting input to the comparator, it too will drive the output towards ground insuring the fastest possible switching time regardless of how slow the input moves. If the input then travels down to V_{REF}, the same procedure will occur only in the opposite direction insuring that the output will be driven hard towards $+V_{CC}$.

Putting hysteresis in the feedback loop of the comparator has far more use, however, than simply as an oscillation suppressor. It can be made to function as a Schmitt trigger with presettable trigger points. A typical circuit is shown in *Figure 7*. Again, the hysteresis is achieved by shifting the reference voltage at the positive input when the output voltage V_O changes state. This network requires only three resistors and is referenced to the positive supply $+V_{CC}$ of the comparator. This can be modeled as a resistive divider, R_1 and R_2, between $+V_{CC}$ and ground with the third resistor, R_3, alternately connected to $+V_{CC}$ or ground, paralleling either R_1 or R_2. To analyze this circuit, assume that the input voltage, V_{IN}, at the inverting input is less than V_A. With $V_{IN} \leq V_A$ the output will be high ($V_O = +V_{CC}$). The upper input trip voltage, V_{A1}, is defined by:

$$V_{A1} = \frac{+V_{CC}\, R_2}{(R_1 \parallel R_3) + R_2}$$

or

$$V_{A1} = \frac{+V_{CC}\, R_2\, (R_1 + R_3)}{R_1\, R_2 + R_1\, R_3 + R_2\, R_3} \qquad (1)$$

When the input voltage V_{IN}, rises above the reference voltage ($V_{IN} > V_{A1}$), voltage, V_O, will go low (V_O = GND). The lower input trip voltage, V_{A2}, is now defined by:

$$V_{A2} = \frac{+V_{CC}\, R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}$$

or

$$V_{A2} = \frac{+V_{CC}\, R_2\, R_3}{R_1\, R_2 + R_1\, R_3 + R_2\, R_3} \qquad (2)$$

When the input voltage, V_{IN}, decreases to V_{A2} or lower, the output will again switch high. The total hysteresis, ΔV_A, provided by this network is defined by:

$$\Delta V_A = V_{A1} - V_{A2}$$

or, subtracting equation 2 from equation 1

$$\Delta V_A\, \Delta\, \frac{+V_{CC}\, R_1\, R_2}{R_1\, R_2 + R_1\, R_3 + R_2\, R_3} \qquad (3)$$

To insure that V_O will swing between $+V_{CC}$ and ground, choose:

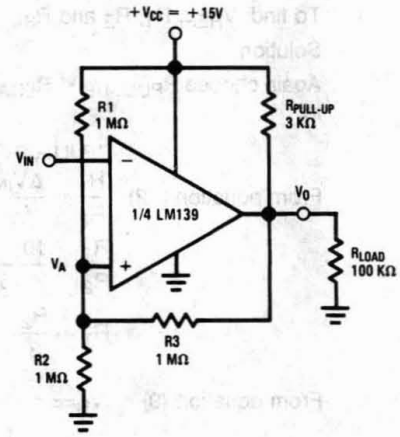
$$R_{PULL\text{-}UP} < R_{LOAD} \text{ and} \qquad (4)$$

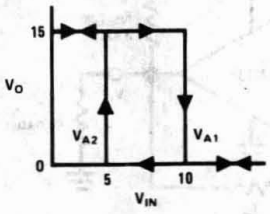
$$R_3 > R_{PULL\text{-}UP} \qquad (5)$$

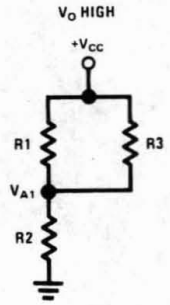
Heavier loading on $R_{PULL\text{-}UP}$ (i.e. smaller values of R_3 or R_{LOAD}) simply reduces the value of the maximum output voltage thereby reducing the amount of hysteresis by lowering the value of V_{A1}. For simplicity, we have assumed in the above equations that V_O high switches all the way up to $+V_{CC}$.

To find the resistor values needed for a given set of trip points, we first divide equation (3) by equation (2). This gives us the ratio:

$$\frac{\Delta V_A}{V_{A2}} = \frac{1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}}{1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}} \qquad (6)$$







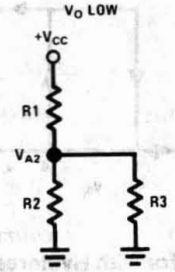


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FIGURE 7. Inverting Comparator with Hysteresis

If we let $R_1 = n\,R_3$, equation (6) becomes:

$$\frac{\Delta V_A}{V_{A2}} = n \tag{7}$$

We can then obtain an expression for R_2 from equation (1) which gives

$$R_2 = \frac{R_1 \parallel R_3}{\frac{+V_{CC}}{V_{A1}} - 1} \tag{8}$$

The following design example is offered:

Given: $V^+ = +15V$
$R_{LOAD} = 100\,k\Omega$
$V_{A1} = +10V$
$V_{A2} = +5V$

To find: R_1, R_2, R_3, $R_{PULL\text{-}UP}$

Solution:

From equation (4) $R_{PULL\text{-}UP} < R_{LOAD}$
$R_{PULL\text{-}UP} < 100\,k\Omega$
so let $R_{PULL\text{-}UP} = 3\,k\Omega$

From equation (5) $R_3 > R_{LOAD}$
$R_3 > 100\,k\Omega$
so let $R_3 = 1\,M\Omega$

From equation (7) $n = \frac{\Delta V_A}{V_{A2}} = \frac{10-5}{5} = 1$

and since $R_1 = n\,R_3$
this gives $R_1 = 1\,R_3 = 1\,M\Omega$

From equation (8) $R_2 = \frac{500\,k\Omega}{\frac{15}{10} - 1} = 1\,M\Omega$

These are the values shown in *Figure 7*.

The circuit shown in *Figure 8* is a non-inverting comparator with hysteresis which is obtained with only two resistors, R_1 and R_2. In contrast to the first method, however, this circuit requires a separate reference voltage at the negative input. The trip voltage, V_A, at the positive input is shifted about V_{REF} as V_O changes between $+V_{CC}$ and ground.

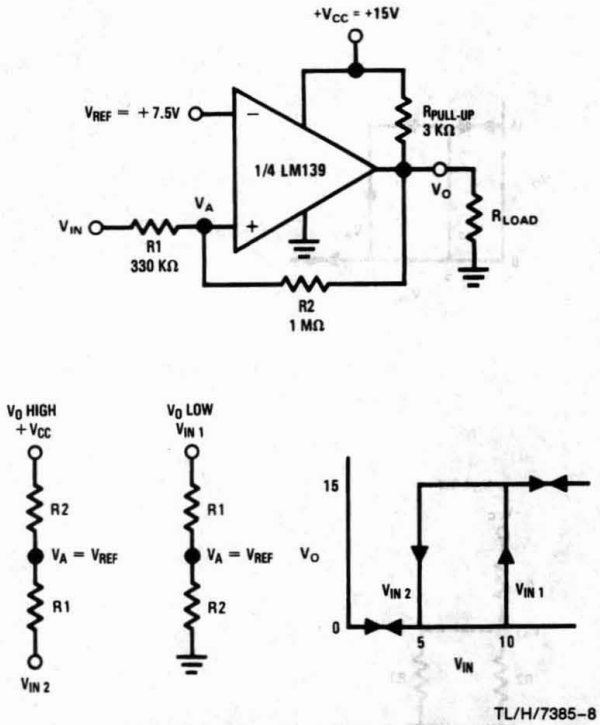

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FIGURE 8. Non-Inverting Comparator with Hysteresis

Again for analysis, assume that the input voltage, V_{IN}, is low so that the output, V_O, is also low (V_O = GND). For the output to switch, V_{IN} must rise up to $V_{IN\,1}$ where $V_{IN\,1}$ is given by:

$$V_{IN\,1} = \frac{V_{REF}(R_1 + R_2)}{R_2} \tag{9}$$

As soon as V_O switches to $+V_{CC}$, V_A will step to a value greater than V_{REF} which is given by:

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN\,1})\,R_1}{R_1 + R_2} \tag{10}$$

To make the comparator switch back to its low state (V_O = GND) V_{IN} must go below V_{REF} before V_A will again equal V_{REF}. This lower trip point is now given by:

$$V_{IN\,2} = \frac{V_{REF}(R_1 + R_2) - V_{CC}\,R_1}{R_2} \tag{11}$$

The hysteresis for this circuit, ΔV_{IN}, is the difference between $V_{IN\,1}$ and $V_{IN\,2}$ and is given by:

$$\Delta V_{IN} = V_{IN\,1} - V_{IN\,2} = \frac{V_{REF}(R_1 + R_2)}{R_2} - \frac{V_{REF}(R_1 + R_2) - V_{CC}\,R_1}{R_2}$$

or

$$\Delta V_{IN} = \frac{V_{CC}\,R_1}{R_2} \tag{12}$$

As a design example consider the following:

Given: $R_{LOAD} = 100\,k\Omega$
$V_{IN\,1} = 10V$
$V_{IN\,2} = 5V$
$+V_{CC} = 15V$

To find: V_{REF}, R_1, R_2 and R_3

Solution:

Again choose $R_{PULL\text{-}UP} < R_{LOAD}$ to minimize loading, so let

$R_{PULL\text{-}UP} = 3\,k\Omega$

From equation (12) $\frac{R_1}{R_2} = \frac{\Delta V_{IN}}{V_{CC}}$

$\frac{R_1}{R_2} = \frac{10-5}{15} = \frac{1}{3}$

$R_1 = \frac{R_2}{3}$

From equation (9) $V_{REF} = \frac{10}{1 + \frac{R_1}{R_2}}$

$V_{REF} = \frac{V_{IN}}{1 + \frac{1}{3}} = 7.5V$

To minimize output loading choose

$$R_2 > R_{PULL\text{-}UP}$$

or $R_2 > 3\ k\Omega$

so let $R_2 = 1\ M\Omega$

The value of R_1 is now obtained from equation (12)

$$R_1 = \frac{R_2}{3}$$

$$R_1 = \frac{1\ M\Omega}{3} \cong 330\ k\Omega$$

These are the values shown in *Figure 8*.

LIMIT COMPARATOR WITH LAMP DRIVER

The limit comparator shown in *Figure 9* provides a range of input voltages between which the output devices of both LM139 comparators will be OFF.

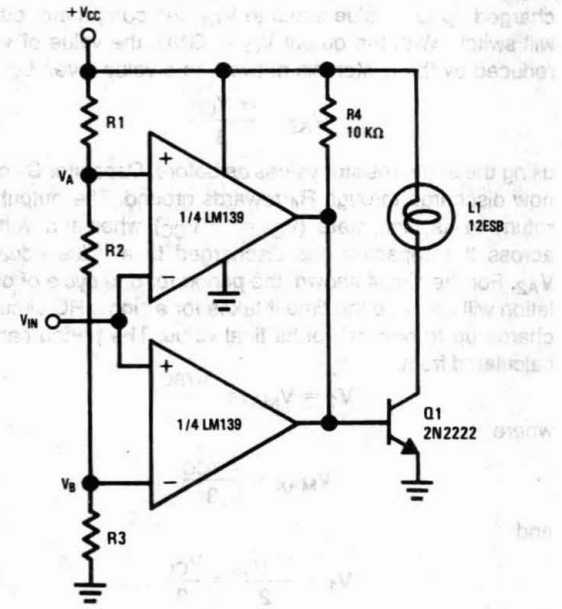

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FIGURE 9. Limit Comparator with Lamp Driver

This will allow base current for Q_1 to flow through pull-up resistor R_4, turning ON Q_1 which lights the lamp. If the input voltage, V_{IN}, changes to a value greater than V_A or less than V_B, one of the comparators will switch ON, shorting the base of Q_1 to ground, causing the lamp to go OFF. If a PNP transistor is substituted for Q_1 (with emitter tied to $+V_{CC}$) the lamp will light when the input is above V_A or below V_B. V_A and V_B are arbitrarily set by varying resistors R_1, R_2 and R_3.

ZERO CROSSING DETECTOR

The LM139 can be used to symmetrically square up a sine wave centered around zero volts by incorporating a small amount of positive feedback to improve switching times and centering the input threshold at ground (see *Figure 10*). Voltage divider R_4 and R_5 establishes a reference voltage, V_1, at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5, the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$. The positive feedback resistor, R_6, is made very large with respect to R_5 ($R_6 = 2000\ R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10$ mV) but it is sufficient to insure rapid output voltage transitions. Diode D_1 is used to insure that

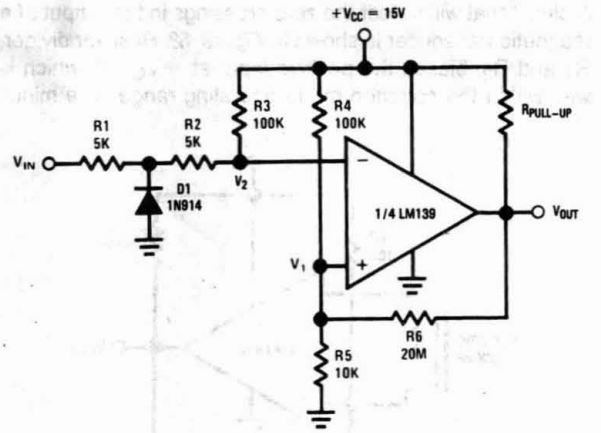

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FIGURE 10. Zero Crossing Detector

the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1.

COMPARING THE MAGNITUDE OF VOLTAGES OF OPPOSITE POLARITY

The comparator circuit shown in *Figure 11* compares the magnitude of two voltages, $V_{IN\ 1}$ and $V_{IN\ 2}$ which have opposite polarities. The resultant input voltage at the minus input terminal to the comparator, V_A, is a function of the voltage divider from $V_{IN\ 1}$ and $V_{IN\ 2}$ and the values of R_1 and R_2. Diode connected transistor Q_1 provides protection

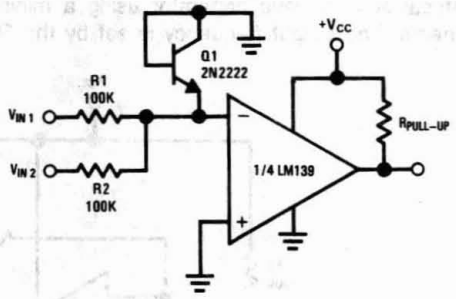

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FIGURE 11. Comparing the Magnitude of Voltages of Opposite Polarity

for the minus input terminal by clamping it at several hundred millivolts below ground. A 2N2222 was chosen over a 1N914 diode because of its lower diode voltage. If desired, a small amount of hysteresis may be added using the techniques described previously. Correct magnitude comparison can be seen as follows: Let $V_{IN\ 1}$ be the input for the positive polarity input voltage and $V_{IN\ 2}$ the input for the negative polarity. If the magnitude of $V_{IN\ 1}$ is greater than that

of $V_{IN\,2}$ the output will go low (V_{OUT} = GND). If the magnitude of $V_{IN\,1}$ is less than that of $V_{IN\,2}$, however, the output will go high ($V_{OUT} = V_{CC}$).

MAGNETIC TRANSDUCER AMPLIFIER

A circuit that will detect the zero crossings in the output of a magnetic transducer is shown in *Figure 12*. Resistor divider, R_1 and R_2, biases the positive input at $+V_{CC}/2$, which is well within the common mode operating range. The minus

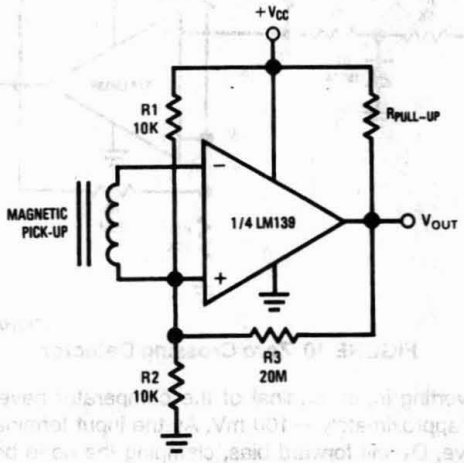

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FIGURE 12. Magnetic Transducer Amplifier

input is biased through the magnetic transducer. This allows large signal swings to be handled without exceeding the input voltage limits. A symmetrical square wave output is insured through the positive feedback resistor R_3. Resistors R_1 and R_2 can be used to set the DC bias voltage at the positive input at any desired voltage within the input common mode voltage range of the comparator.

OSCILLATORS USING THE LM139

The LM139 lends itself well to oscillator applications for frequencies below several megacycles. *Figure 13* shows a symmetrical square wave generator using a minimum of components. The output frequency is set by the RC time constant of R_4 and C_1 and the total hysteresis of the loop is set by R_1, R_2 and R_3. The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output which would degrade the output slew rate.

To analyze this circuit assume that the output is initially high. For this to be true, the voltage at the negative input must be less than the voltage at the positive input. Therefore, capacitor C_1 is discharged. The voltage at the positive input, V_{A1}, will then be given by:

$$V_{A1} = \frac{+V_{CC}\,R_2}{R_2 + (R_1 \parallel R_3)} \tag{13}$$

where if $R_1 = R_2 = R_3$

then $$V_{A1} = \frac{2\,V_{CC}}{3} \tag{14}$$

Capacitor C_1 will charge up through R_4 so that when it has charged up to a value equal to V_{A1}, the comparator output will switch. With the output V_O = GND, the value of V_A is reduced by the hysteresis network to a value given by:

$$V_{A2} = \frac{+V_{CC}}{3} \tag{15}$$

using the same resistor values as before. Capacitor C_1 must now discharge through R_4 towards ground. The output will return to its high state ($V_O = +V_{CC}$) when the voltage across the capacitor has discharged to a value equal to V_{A2}. For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The period can be calculated from:

$$V_1 = V_{MAX}e^{-t_1/RC} \tag{16}$$

where

$$V_{MAX} = \frac{2\,V_{CC}}{3} \tag{17}$$

and

$$V_1 = \frac{V_{MAX}}{2} = \frac{V_{CC}}{3} \tag{18}$$

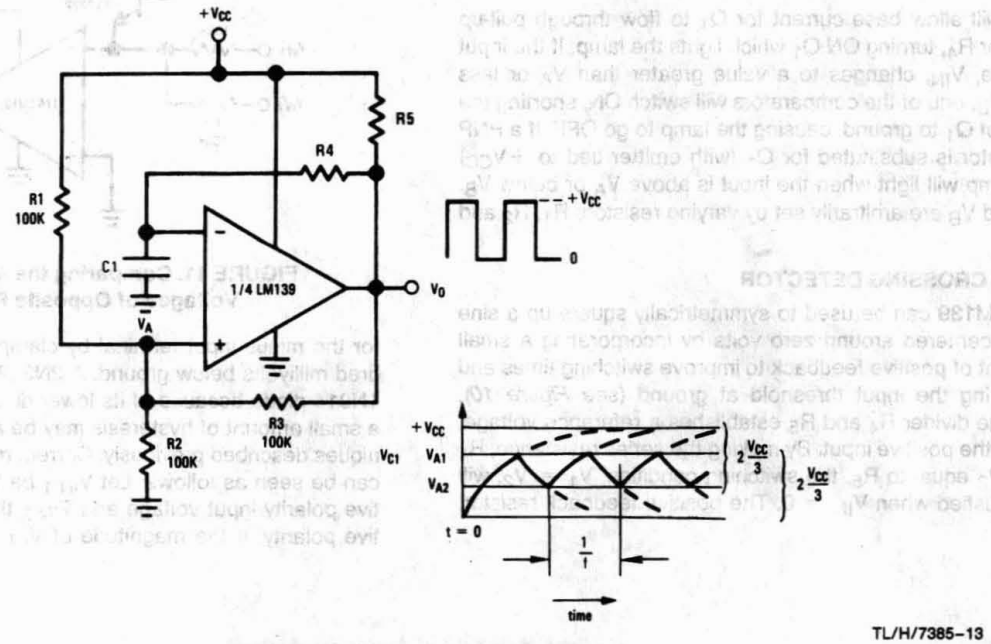

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FIGURE 13. Square Wave Generator

One period will be given by:

$$\frac{1}{\text{freq.}} = 2t_1 \tag{19}$$

or calculating the exponential gives

$$\frac{1}{\text{freq.}} = 2\,(0.694)\,R_4\,C_1 \tag{20}$$

Resistors R_3 and R_4 must be at least 10 times larger than R_5 to insure that V_O will go all the way up to $+V_{CC}$ in the high state. The frequency stability of this circuit should strictly be a function of the external components.

PULSE GENERATOR WITH VARIABLE DUTY CYCLE

The basic square wave generator of *Figure 13* can be modified to obtain an adjustable duty cycle pulse generator, as shown in *Figure 14*, by providing a separate charge and discharge path for capacitor C_1. One path, through R_4 and D_1 will charge the capacitor and set the pulse width (t_1). The other path, R_5 and D_2, will discharge the capacitor and set the time between pulses (t_2). By varying resistor R_5, the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying R_4, the pulse width will be altered without affecting the time between pulses. Both controls will change the frequency of the generator, however. With the values given in *Figure 14*, the pulse width and time between pulses can be found from:

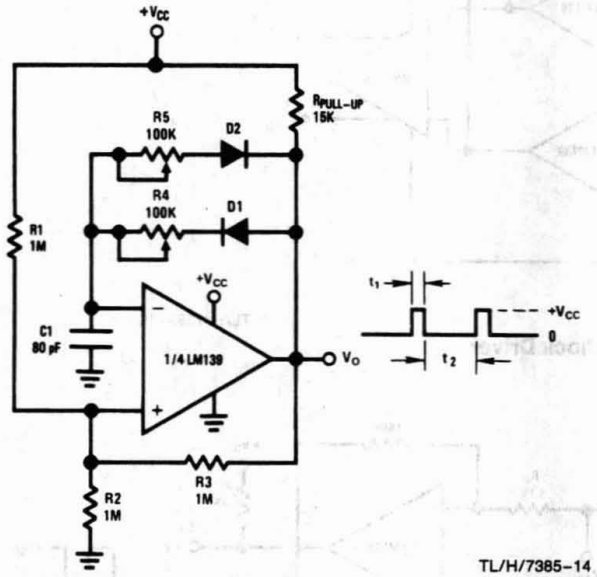

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FIGURE 14. Pulse Generator with Variable Duty Cycle

$$V_1 = V_{MAX}\,(1 - e^{-t_1/R_4C_1}) \text{ risetime} \tag{21a}$$

$$V_1 = V_{MAX}\,e^{-t_2/R_5C_1} \text{ falltime} \tag{21b}$$

where

$$V_{MAX} = \frac{2\,V_{CC}}{3} \tag{22}$$

and

$$V_1 = \frac{V_{MAX}}{2} = \frac{V_{CC}}{3} \tag{23}$$

which gives

$$\frac{1}{2} = e^{-t_1/R_4C_1} \tag{24}$$

t_2 is then given by:

$$\frac{1}{2} = e^{-t_2/R_5C_1} \tag{25}$$

These terms will have a slight error due to the fact that V_{MAX} is not exactly equal to $\frac{2}{3}\,V_{CC}$ but is actually reduced by the diode drop to:

$$V_{MAX} = \frac{2}{3}\,(V_{CC} - V_{BE}) \tag{26}$$

therefore

$$\frac{1}{2\,(1 - V_{BE})} = e^{-t_1/R_4C_1} \tag{27}$$

and

$$\frac{1}{2\,(1 - V_{BE})} = e^{-t_2/R_5C_1} \tag{28}$$

CRYSTAL CONTROLLED OSCILLATOR

A simple yet very stable oscillator can be obtained by using a quartz crystal resonator as the feedback element. *Figure 15* gives a typical circuit diagram of this. This value of R_1 and R_2 are equal so that the comparator will switch symmetrically about $+V_{CC}/2$. The RC time constant of R_3 and C_1 is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.

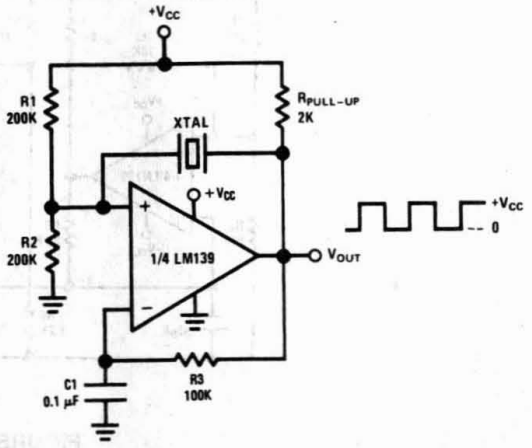

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FIGURE 15. Crystal Controlled Oscillator

When specifying the crystal, be sure to order series resonant along with the desired temperature coefficient and load capacitance to be used.

MOS CLOCK DRIVER

The LM139 can be used to provide the oscillator and clock delay timing for a two phase MOS clock driver (see *Figure 16*). The oscillator is a standard comparator square wave generator similar to the one shown in *Figure 13*. Two other comparators of the LM139 are used to establish the desired phasing between the two outputs to the clock driver. A more detailed explanation of the delay circuit is given in the section under "Digital and Switching Circuits."

WIDE RANGE VCO

A simple yet very stable voltage controlled oscillator using a mimimum of external components can be realized using three comparators of the LM139. The schematic is shown in *Figure 17a*. Comparator 1 is used closed loop as an integrator (for further discussion of closed loop operation see section on Operational Amplifiers) with comparator 2 used as a triangle to square wave converter and comparator 3 as the switch driving the integrator. To analyze the circuit, assume

that comparator 2 is its high state ($V_{SQ} = +V_{CC}$) which drives comparator 3 to its high state also. The output device of comparator 3 will be OFF which prevents any current from flowing through R_2 to ground. With a control voltage, V_C, at the input to comparator 1, a current I_1 will flow through R_1 and begin discharging capacitor C_1, at a linear rate. This discharge current is given by:

$$I_1 = \frac{V_C}{2\,R_1} \tag{29}$$

and the discharge time is given by:

$$I_1 = C_1 \frac{\Delta V}{\Delta t}. \tag{30}$$

ΔV will be the maximum peak change in the voltage across capacitor C_1 which will be set by the switch points of comparator 2. These trip points can be changed by simply altering the ratio of R_F to R_S, thereby increasing or decreasing the amount of hysteresis around comparator 2. With $R_F = 100\ k\Omega$ and $R_S = 5\ k\Omega$, the amount of hysteresis is approximately $\pm 5\%$ which will give switch points of $+V_{CC}/2 \pm 750$ mV from a 30V supply. (See "Comparators with Hysteresis").

As capacitor C_1 discharges, the output voltage of comparator 1 will decrease until it reaches the lower trip point of comparator 2, which will then force the output of comparator 2 to go to its low state (V_{SQ} = GND).

This in turn causes comparator 3 to go to its low state where its output device will be in saturation. A current I_2 can now

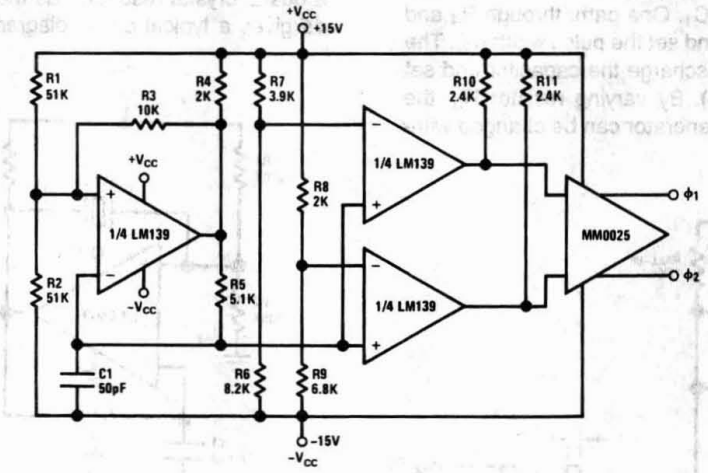

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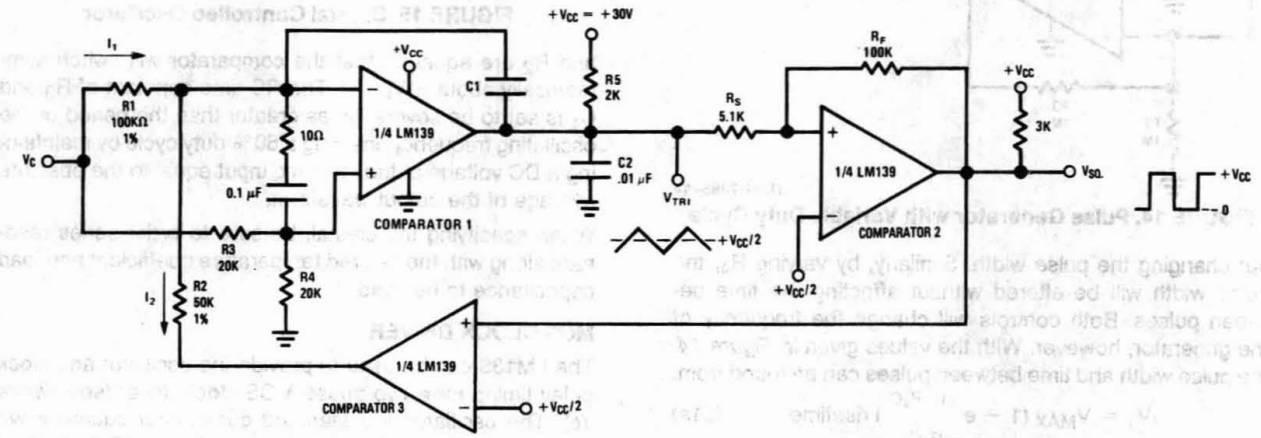
FIGURE 16. MOS Clock Driver



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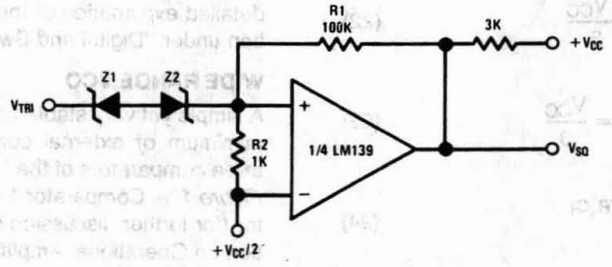
(a)



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(b)

FIGURE 17. Voltage Controlled Oscillator

flow through resistor R_2 to ground. If the value of R_2 is chosen as $R_1/2$ a current equal to the capacitor discharge current can be made to flow out of C_1 charging it at the same rate as it was discharged. By making $R_2 = R_1/2$, current I_2 will equal twice I_1. This is the control circuitry which guararantees a constant 50% duty cycle oscillation independent of frequency or temperature. As capacitor C_1 charges, the output of comparator 1 will ramp up until it trips comparator 2 to its high state ($V_{SQ} = +V_{CC}$) and the cycle will repeat.

The circuit shown in *Figure 17a* uses a +30V supply and gives a triangle wave of 1.5V peak-to-peak. With a timing capacitor, C_1 equal to 500 pF, a frequency range from approximately 115 kHz down to approximately 670 Hz was obtained with a control voltage ranging from 50V down to 250 mV. By reducing the hysteresis around comparator 2 down to ±150 mV (R_f = 100 kΩ, R_S = 1 kΩ) and reducing the compensating capacitor C_2 down to .001 μF, frequencies up to 1 MHz may be obtained. For lower frequencies ($f_o \leq 1$ Hz) the timing capacitor, C_1, should be increased up to approximately 1 μF to insure that the charging currents, I_1 and I_2, are much larger than the input bias currents of comparator 1.

Figure 17b shows another interesting approach to provide the hysteresis for comparator 2. Two identical Zener diodes, Z_1 and Z_2, are used to set the trip points of comparator 2. When the triangle wave is less than the value required to Zener one of the diodes, the resistive network, R_1 and R_2, provides enough feedback to keep the comparator in its proper state, (the input would otherwise be floating). The advantage of this circuit is that the trip points of comparator 2 will be completely independent of supply voltage fluctuations. The disadvantage is that Zeners with less than one volt breakdown voltage are not obtainable. This limits the maximum upper frequency obtainable because of the larger amplitude of the triangle wave. If a regulated supply is available, *Figure 17a* is preferable simply because of less parts count and lower cost.

Both circuits provide good control over at least two decades in frequency with a temperature coefficient largely dependent on the TC of the external timing resistors and capacitors. Remember that good circuit layout is essential along with the 0.01 μF compensation capacitor at the output of comparator 1 and the series 10Ω, resistor and 0.1 μF capacitor between its inputs, for proper operation. Comparator 1 is a high gain amplifier used closed loop as an integrator so long leads and loose layout should be avoided.

DIGITAL AND SWITCHING CIRCUITS

The LM139 lends itself well to low speed (<1 MHz) high level logic circuits. They have the advantage of operating with high signal levels, giving high noise immunity, which is highly desirable for industrial applications. The output signal level can be selected by setting the V_{CC} to which the pull-up resistor is connected to any desired level.

AND/NAND GATES

A three input AND gate is shown in *Figure 18*. Operation of this gate is as follows: resistor divider R_1 and R_2 establishes a reference voltage at the inverting input to the comparator. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers comprised of R_3, R_4, R_5 and R_6. The output will go high only when all three inputs are high, causing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a "0" equal to ground and a "1" equal +15V. The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are the "1" state. This circuit with increased fan-in is shown in *Figure 19*.

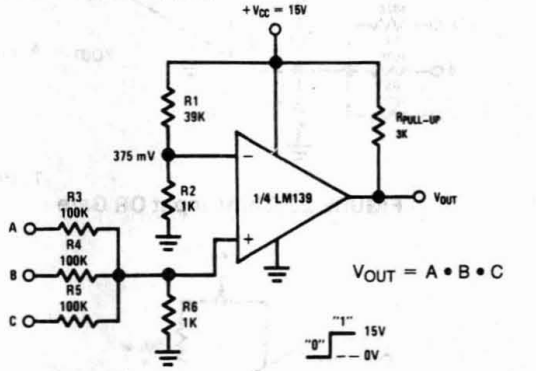

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FIGURE 18. Three Input AND Gate

To convert these AND gates to NAND gates simply interchange the inverting and non-inverting inputs to the comparator. Hysteresis can be added to speed up output transitions if low speed input signals are used.

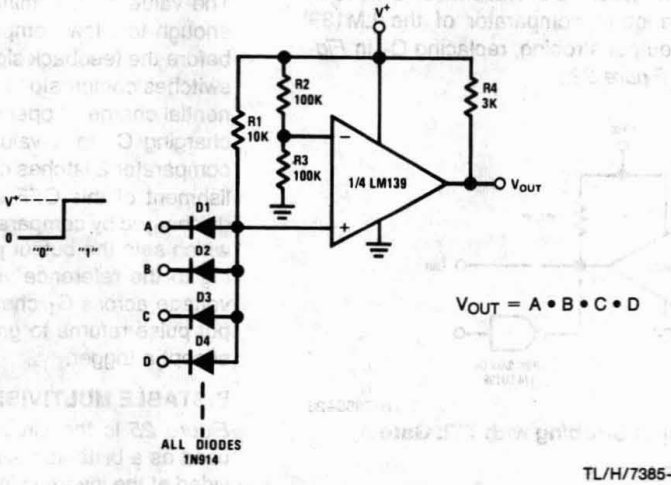

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FIGURE 19. AND Gate with Large Fan-In

OR/NOR GATES

The three input OR gate (positive logic) shown in *Figure 20* is achieved from the basic AND gate simply by increasing R_1 thereby reducing the reference voltage. A logic "1" at any of the inputs will produce a logic "1" at the output. Again a NOR gate may be implemented by simply reversing the comparator inputs. Resistor R_6 may be added for the OR or NOR function at the expense of noise immunity if so desired.

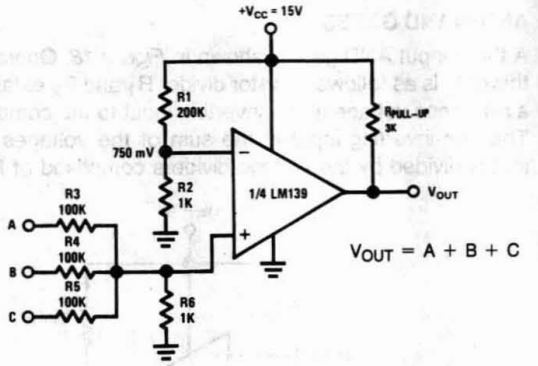

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FIGURE 20. Three Input OR Gate

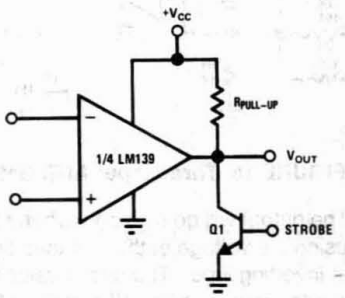

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FIGURE 21. Output Strobing Using a Discrete Transistor

OUTPUT STROBING

The output of the LM139 may be disabled by adding a clamp transistor as shown in *Figure 21*. A strobe control voltage at the base of Q_1 will clamp the comparator output to ground, making it immune to any input changes.

If the LM139 is being used in a digital system the output may be strobed using any other type of gate having an uncommitted collector output (such as National's DM5401/DM7401). In addition another comparator of the LM139 could also be used for output strobing, replacing Q_1 in *Figure 21*, if desired. (See *Figure 22*.)

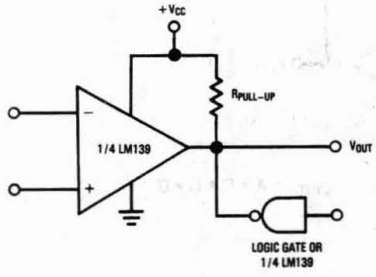

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FIGURE 22. Output Strobing with TTL Gate

ONE SHOT MULTIVIBRATORS

A simple one shot multivibrator can be realized using one comparator of the LM139 as shown in *Figure 23*. The output pulse width is set by the values of C_2 and R_4 (with $R_4 > 10\ R_3$ to avoid loading the output). The magnitude of the input trigger pulse required is determined by the resistive divider R_1 and R_2. Temperature stability can be achieved by balancing the temperature coefficients of R_4 and C_2 or by using components with very low TC. In addition, the TC of resistors R_1 and R_2 should be matched so as to maintain a fixed reference voltage of $+V_{CC}/2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset the one shot at the end of its pulse. It also prevents the non-inverting input from being driven below ground. The output pulse width is relatively independent of the magnitude of the supply voltage and will change less than 2% for a five volt change in $+V_{CC}$.

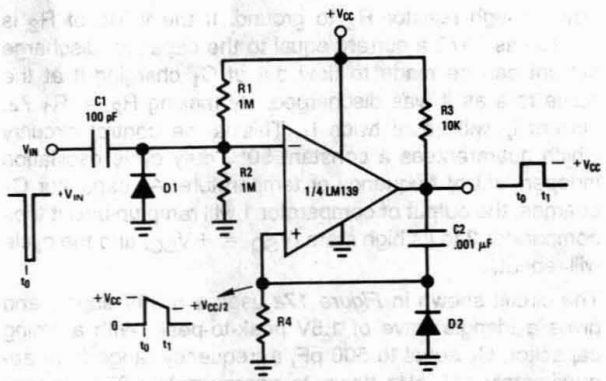

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FIGURE 23. One Shot Multivibrator

The one shot multivibrator shown in *Figure 24* has several characteristics which make it superior to that shown in *Figure 23*. First, the pulse width is independent of the magnitude of the power supply voltage because the charging voltage and the intercept voltage are a fixed percentage of $+V_{CC}$. In addition this one-shot is capable of 99% duty cycle and exhibits input trigger lock-out to insure that the circuit will not re-trigger before the output pulse has been completed. The trigger level is the voltage required at the input to raise the voltage at point A higher than the voltage at point B, and is set by the resistive divider R_4 and R_{10} and the network R_1, R_2 and R_3. When the multivibrator has been triggered, the output of comparator 2 is high causing the reference voltage at the non-inverting input of comparator 1 to go to $+ V_{CC}$. This prevents any additional input pulses from disturbing the circuit until the output pulse has been completed.

The value of the timing capacitor, C_1, must be kept small enough to allow comparator 1 to completely discharge C_1 before the feedback signal from comparator 2 (through R_{10}) switches comparator 1 OFF and allows C_1 to start an exponential charge. Proper circuit action depends on rapidly discharging C_1 to a value set by R_6 and R_9 at which time comparator 2 latches comparator 1 OFF. Prior to the establishment of this OFF state, C_1 will have been completely discharged by comparator 1 in the ON state. The time delay, which sets the output pulse width, results from C_1 recharging to the reference voltage set by R_6 and R_9. When the voltage across C_1 charges beyond this reference, the output pulse returns to ground and the input is again reset to accept a trigger.

BISTABLE MULTIVIBRATOR

Figure 25 is the circuit of one comparator of the LM139 used as a bistable multivibrator. A reference voltage is provided at the inverting input by a voltage divider comprised of R_2 and R_3. A pulse applied to the SET terminal will switch the output high. Resistor divider network R_1, R_4, and R_5

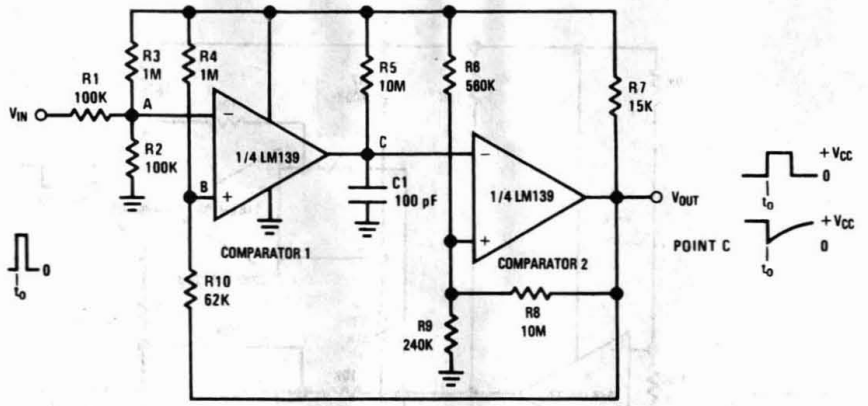

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FIGURE 24. Multivibrator with Input Lock-Out

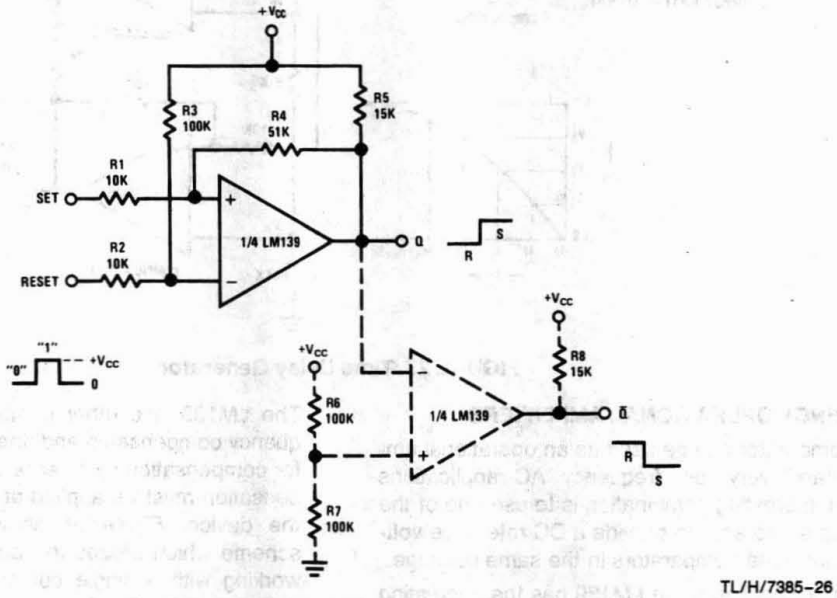

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FIGURE 25. Bistable Multivibrator

now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse now applied to the RESET Input will pull the output low. If both Q and $\overline{Q}$ outputs are needed, another comparator can be added as shown dashed in *Figure 25*.

Figure 26 shows the output saturation voltage of the LM139 comparator versus the amount of current being passed to ground. The end point of 1 mV at zero current along with an R_{SAT} of 60Ω shows why the LM139 so easily adapts itself to oscillator and digital switching circuits by allowing the DC output voltage to go practically to ground while in the ON state.

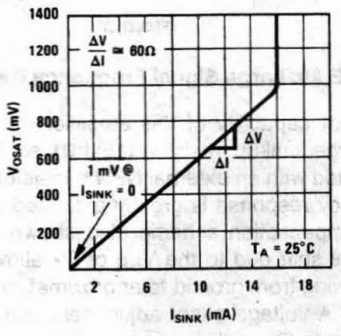

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FIGURE 26. Typical Output Saturation Characteristics

TIME DELAY GENERATOR

The final circuit to be presented "Digital and Switching Circuits" is a time delay generator (or sequence generator) as shown in *Figure 27*.

This timer will provide output signals at prescribed time intervals from a time reference t_o and will automatically reset when the input signal returns to ground. For circuit evaluation, first consider the quiescent state (V_{IN} = O) where the output of comparator 4 is ON which keeps the voltage across C_1 at zero volts. This keeps the outputs of comparators 1, 2 and 3 in their ON state (V_{OUT} = GND). When an input signal is applied, comparator 4 turns OFF allowing C_1 to charge at an exponential rate through R_1. As this voltage rises past the present trip points V_A, V_B, and V_C of comparators 1, 2 and 3 respectively, the output voltage of each of these comparators will switch to the high state (V_{OUT} = $+V_{CC}$). A small amount of hysteresis has been provided to insure fast switching for the case where the R_C time constant has been chosen large to give long delay times. It is not necessary that all comparator outputs be low in the quiescent state. Several or all may be reversed as desired simply by reversing the inverting and non-inverting input connections. Hysteresis again is optional.

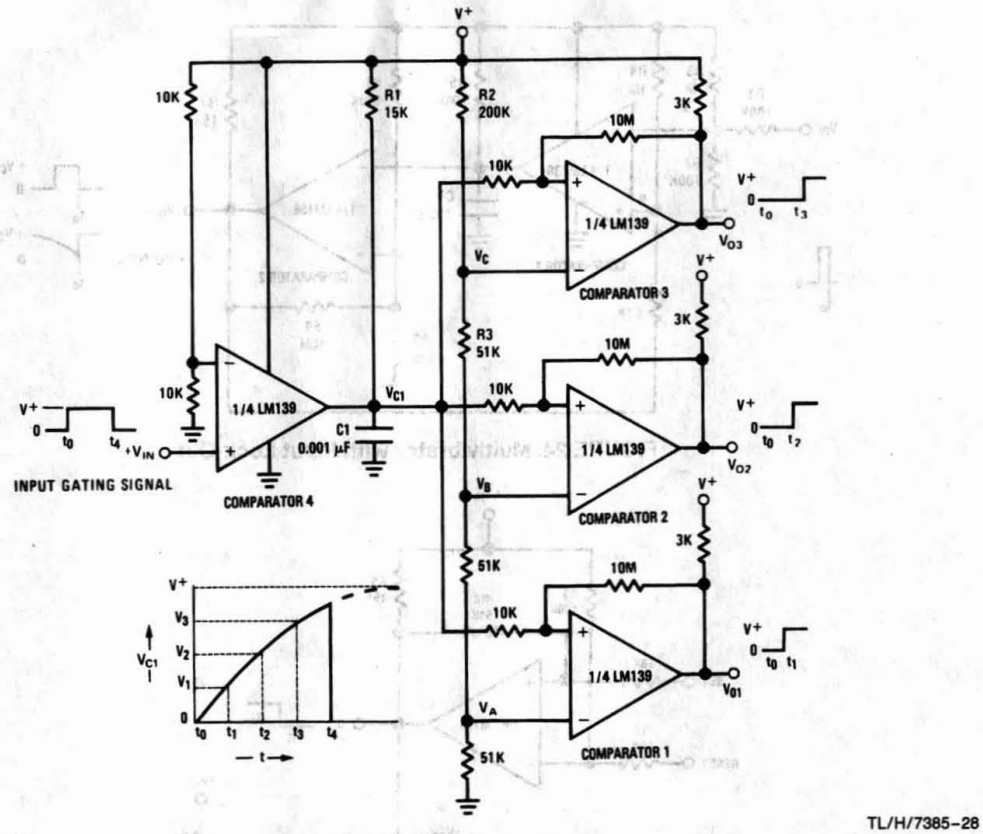

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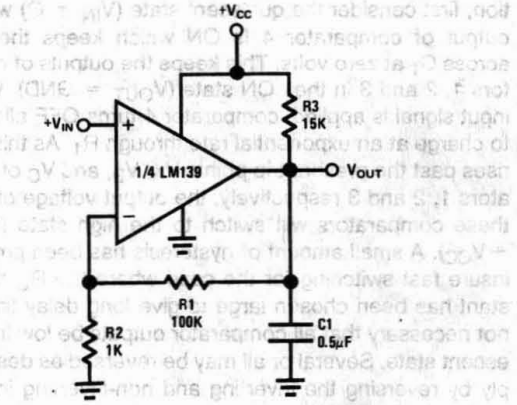
FIGURE 27. Time Delay Generator

LOW FREQUENCY OPERATIONAL AMPLIFIERS

The LM139 comparator can be used as an operational amplifier in DC and very low frequency AC applications (≤100 Hz). An interesting combination is to use one of the comparators as an op amp to provide a DC reference voltage for the other three comparators in the same package.

Another useful application of an LM139 has the interesting feature that the input common mode voltage range includes ground even though the amplifier is biased from a single supply and ground. These op amps are also low power drain devices and will not drive large load currents unless current boosted with an external NPN transistor. The largest application limitation comes from a relatively slow slew rate which restricts the power bandwidth and the output voltage response time.



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$$A_V = 1 + \frac{R1}{R2} = 101$$

FIGURE 28. Non-Inverting Amplifier

The LM139, like other comparators, is not internally frequency compensated and does not have internal provisions for compensation by external components. Therefore, compensation must be applied at either the inputs or output of the device. *Figure 28* shows an output compensation scheme which utilizes the output collector pull-up resistor working with a single compensation capacitor to form a dominant pole. The feedback network, R_1 and R_2 sets the closed loop gain at $1 + R_1/R_2$ or 101 (40 dB). *Figure 29* shows the output swing limitations versus frequency. The

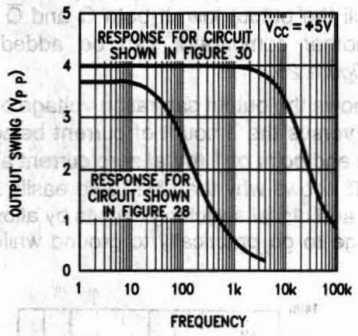

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FIGURE 29. Large Signal Frequency Response

output current capability of this amplifier is limited by the relatively large pull-up resistor (15 kΩ) so the output is shown boosted with an external NPN transistor in *Figure 30*. The frequency response is greatly extended by the use of the new compensation scheme also shown in *Figure 30*. The DC level shift due to the V_{BE} of Q_1 allows the output voltage to swing from ground to approximately one volt less than $+V_{CC}$. A voltage offset adjustment can be added as shown in *Figure 31*.

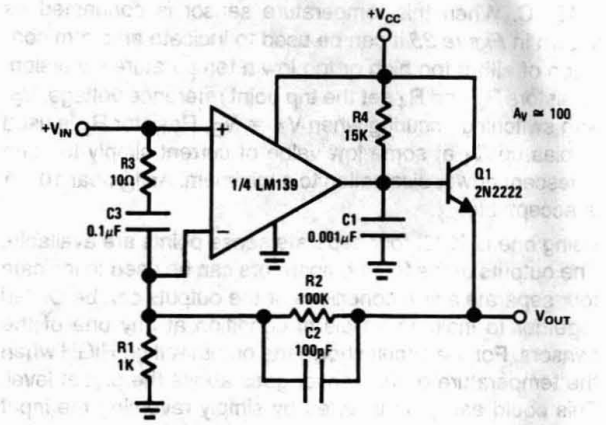

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FIGURE 30. Improved Operational Amplifier

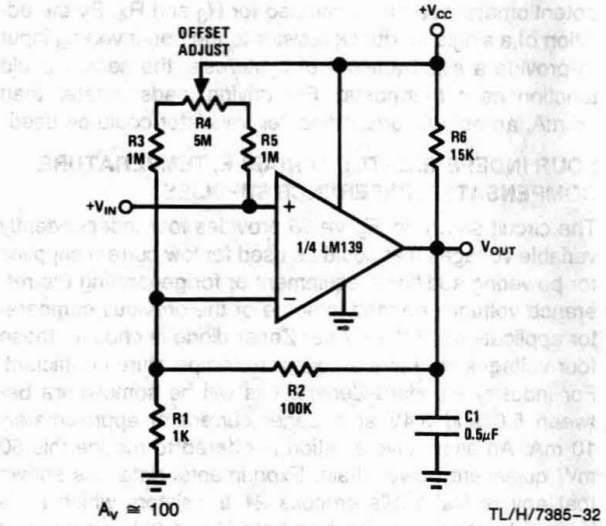

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FIGURE 31. Input Offset Null Adjustment

DUAL SUPPLY OPERATION

The applications presented here have been shown biased typically between $+V_{CC}$ and ground for simplicity. The LM139, however, works equally well from dual (plus and minus) supplies commonly used with most industry standard op amps and comparators, with some applications actually requiring fewer parts than the single supply equivalent.

The zero crossing detector shown in *Figure 10* can be implemented with fewer parts as shown in *Figure 32*. Hysteresis has been added to insure fast transitions if used with slowly moving input signals. It may be omitted if not needed, bringing the total parts count down to one pull-up resistor.

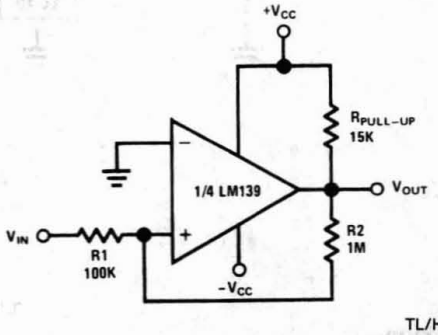

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FIGURE 32. Zero Crossing Detector Using Dual Supplies

The MOS clock driver shown in *Figure 16* uses dual supplies to properly drive the MM0025 clock driver.

The square wave generator shown in *Figure 13* can be used with dual supplies giving an output that swings symmetrically above and below ground (see *Figure 33*). Operation is identical to the single supply oscillator with only change being in the lower trip point.

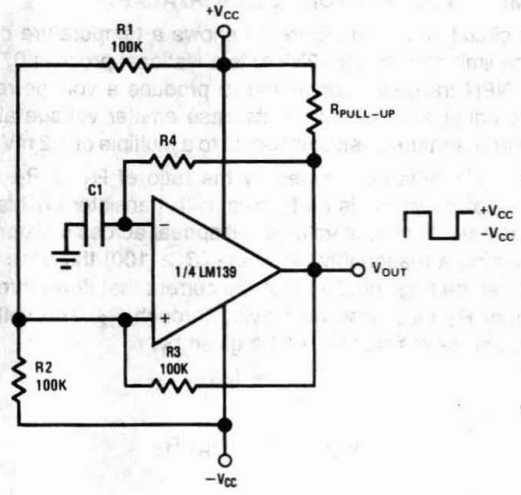

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FIGURE 33. Squarewave Generator Using Dual Supplies

Figure 34 shows an LM139 connected as an op amp using dual supplies. Biasing is actually simpler if full output swing at low gain settings is required by biasing the inverting input from ground rather than from a resistive divider to some voltage between $+V_{CC}$ and ground.

All the applications shown will work equally well biased with dual supplies. If the total voltage across the device is increased from that shown, the output pull-up resistor should be increased to prevent the output transistor from being pulled out of saturation by drawing excessive current, thereby preventing the output low state from going all the way to $-V_{CC}$.

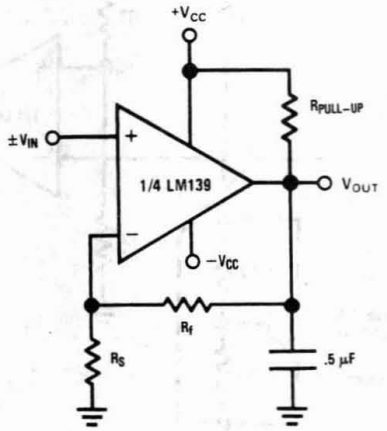

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FIGURE 34. Non-Inverting Amplifier Using Dual Supplies

MISCELLANEOUS APPLICATIONS

The following is a collection of various applications intended primarily to further show the wide versatility that the LM139 quad comparator has to offer. No new modes of operation are presented here so all of the previous formulas and circuit descriptions will hold true. It is hoped that all of the circuits presented in this application note will suggest to the user a few of the many areas in which the LM139 can be utilized.

REMOTE TEMPERATURE SENSOR/ALARM

The circuit shown in *Figure 35* shows a temperature overrange limit sensor. The 2N930 is a National process 07 silicon NPN transistor connected to produce a voltage reference equal to a multiple of its base emitter voltage along with temperature coefficient equal to a multiple of 2.2 mV/°C.

That multiple is determined by the ratio of R_1 to R_2. The theory of operation is as follows: with transistor Q_1 biased up, its base to emitter voltage will appear across resistor R_1. Assuming a reasonably high beta ($\beta \geq 100$) the base current can be neglected so that the current that flows through resistor R_1 must also be flowing through R_2. The voltage drop across resistor R_2 will be given by:

$$I_{R1} = I_{R2}$$

and

$$V_{R1} = V_{be} = I_{R1} R_1$$

so

$$V_{R2} = I_{R2} R_2 = I_{R1} R_2 = V_{be} \frac{R_2}{R_1} \qquad (31)$$

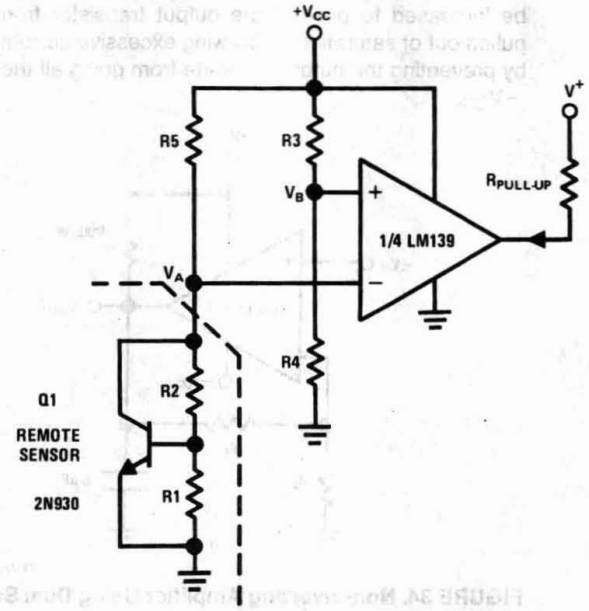
As stated previously this base-emitter voltage is strongly temperature dependent, minus 2.2 mV/°C for a silicon transistor. This temperature coefficient is also multiplied by the resistor ratio R_1/R_2.

This provides a highly linear, variable temperature coefficient reference which is ideal for use as a temperature sensor over a temperature range of approximately −65°C to +150°C. When this temperature sensor is connected as shown in *Figure 35* it can be used to indicate an alarm condition of either too high or too low a temperature excursion. Resistors R_3 and R_4 set the trip point reference voltage, V_B, with switching occuring when $V_A = V_B$. Resistor R_5 is used to bias up Q_1 at some low value of current simply to keep quiescent power dissipation to a minimum. An I_Q near 10 μA is acceptable.

Using one LM139, four separate sense points are available. The outputs of the four comparators can be used to indicate four separate alarm conditions or the outputs can be OR'ed together to indicate an alarm condition at any one of the sensors. For the circuit shown the output will go HIGH when the temperature of the sensor goes above the preset level. This could easily be inverted by simply reversing the input leads. For operation over a narrow temperature range, the resistor ratio R_2/R_1 should be large to make the alarm more sensitive to temperature variations. To vary the trip points a potentiometer can be substituted for R_3 and R_4. By the addition of a single feedback resistor to the non-inverting input to provide a slight amount of hysteresis, the sensor could function as a thermostat. For driving loads greater than 15 mA, an output current booster transistor could be used.

FOUR INDEPENDENTLY VARIABLE, TEMPERATURE COMPENSATED, REFERENCE SUPPLIES

The circuit shown in *Figure 36* provides four independently variable voltages that could be used for low current supplies for powering additional equipment or for generating the reference voltages needed in some of the previous comparator applications. If the proper Zener diode is chosen, these four voltages will have a near zero temperature coefficient. For industry standard Zeners, this will be somewhere between 5.0 and 5.4V at a Zener current of approximately 10 mA. An alternative solution is offered to reduce this 50 mW quiescent power drain. Experimental data has shown that any of National's process 21 transistors which have been selected for low reverse beta (β_R <.25) can be used



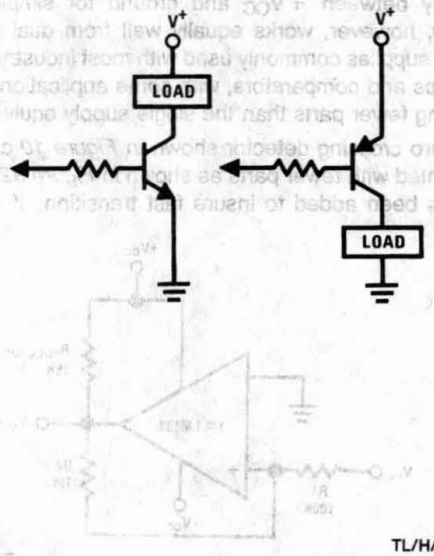


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FIGURE 35. Temperature Alarm

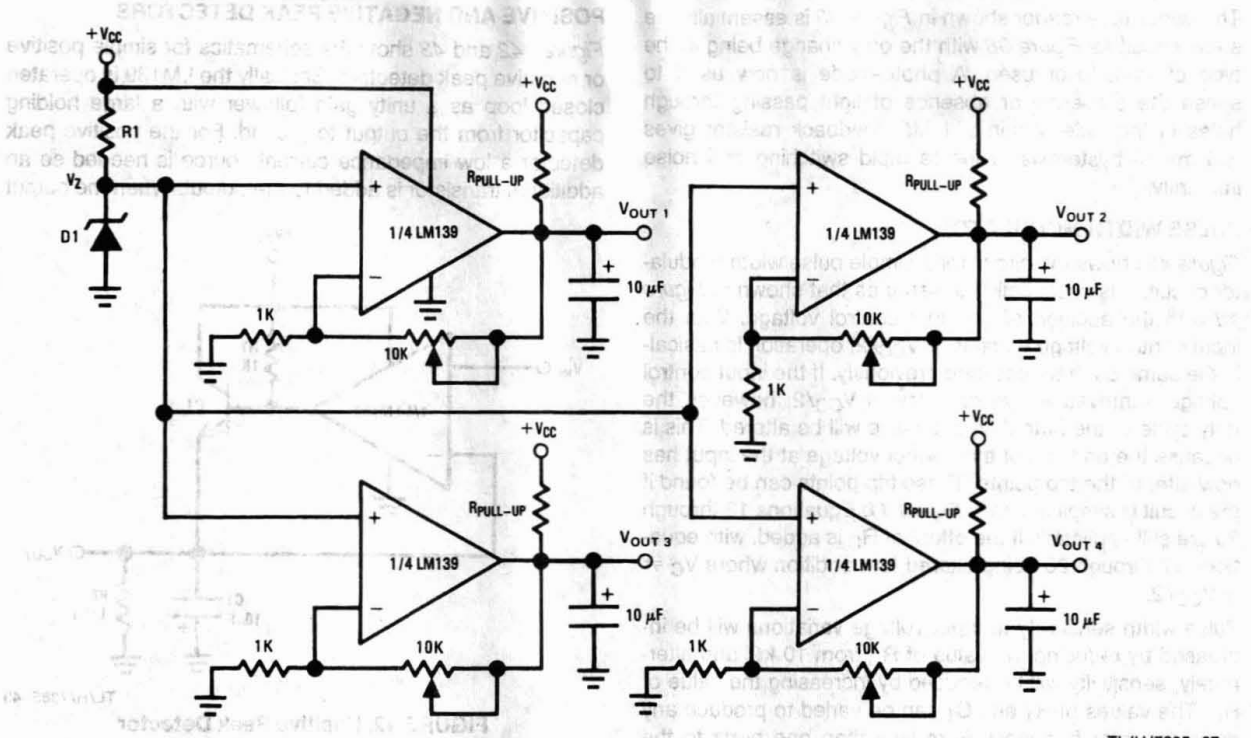

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FIGURE 36. Four Variable Reference Supplies

quite satisfactorily as a zero T.C. Zener. When connected as shown in *Figure 37*, the T.C. of the base-emitter Zener voltage is exactly cancelled by the T.C. of the forward biased base-collector junction if biased at 1.5 mA. The diode can be properly biased from any supply by adjusting R_S to set I_q equal to 1.5 mA. The outputs of any of the reference supplies can be current boosted by using the circuit shown in *Figure 30*.

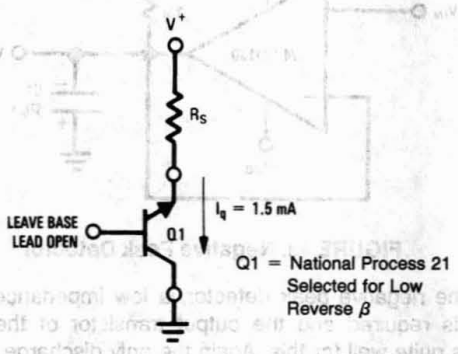

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FIGURE 37. Zero T.C. Zener

DIGITAL TAPE READER

Two circuits are presented here–a tape reader for both magnetic tape and punched paper tape. The circuit shown in *Figure 38*, the magnetic tape reader, is the same as *Figure 12* with a few resistor values changed. With a 5V supply, to make the output TTL compatible, and a 1 MΩ feedback resistor, ±5 mV of hysteresis is provided to insure fast switching and higher noise immunity. Using one LM139, four tape channels can be read simultaneously.

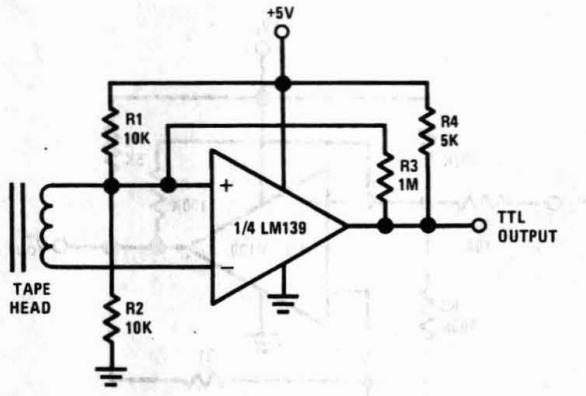

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FIGURE 38. Magnetic Tape Reader with TTL Output

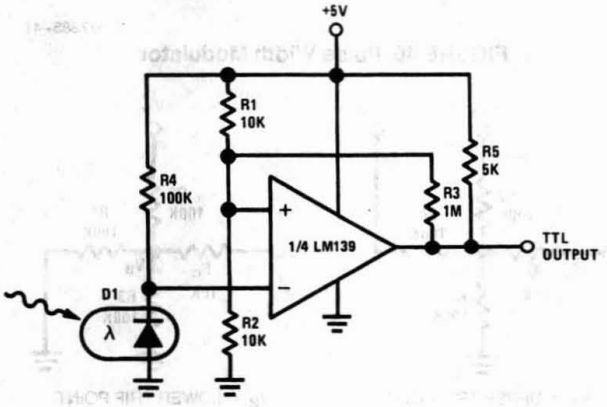

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FIGURE 39. Paper Tape Reader With TTL Output

The paper tape reader shown in *Figure 39* is essentially the same circuit as *Figure 38* with the only change being in the type of transducer used. A photo-diode is now used to sense the presence or absence of light passing through holes in the tape. Again a 1 MΩ feedback resistor gives ±5 mV of hysteresis to insure rapid switching and noise immunity.

PULSE WIDTH MODULATOR

Figure 40 shows the circuit for a simple pulse width modulator circuit. It is essentially the same as that shown in *Figure 13* with the addition of an input control voltage. With the input control voltage equal to $+V_{CC}/2$, operation is basically the same as that described previously. If the input control voltage is moved above or below $+V_{CC}/2$, however, the duty cycle of the output square wave will be altered. This is because the addition of the control voltage at the input has now altered the trip points. These trip points can be found if the circuit is simplified as in *Figure 41*. Equations 13 through 20 are still applicable if the effect of R_C is added, with equations 17 through 20 being altered for condition where $V_C \neq +V_{CC}/2$.

Pulse width sensitivity to input voltage variations will be increased by reducing the value of R_C from 10 kΩ and alternately, sensitivity will be reduced by increasing the value of R_C. The values of R_1 and C_1 can be varied to produce any desired center frequency from less than one hertz to the maximum frequency of the LM139 which will be limited by $+V_{CC}$ and the output slew rate.

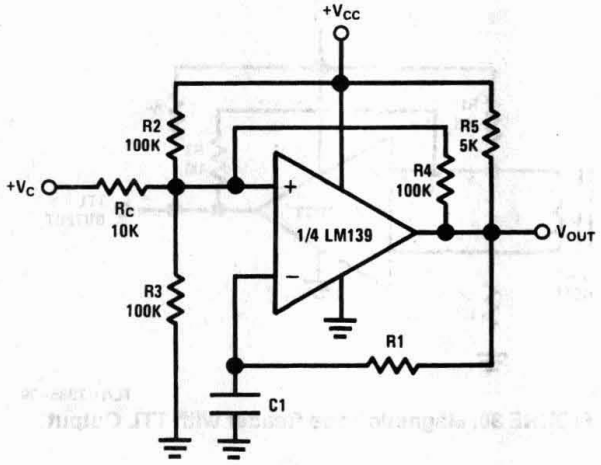

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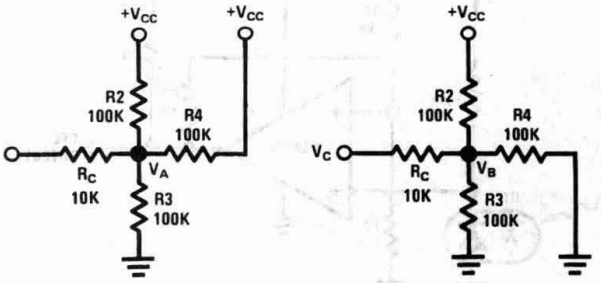
FIGURE 40. Pulse Width Modulator



V_A = UPPER TRIP POINT V_B = LOWER TRIP POINT

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FIGURE 41. Simplified Circuit For Calculating Trip Points of *Figure 40*

POSITIVE AND NEGATIVE PEAK DETECTORS

Figures 42 and *43* show the schematics for simple positive or negative peak detectors. Basically the LM139 is operated closed loop as a unity gain follower with a large holding capacitor from the output to ground. For the positive peak detector a low impedance current source is needed so an additional transistor is added to the output. When the output

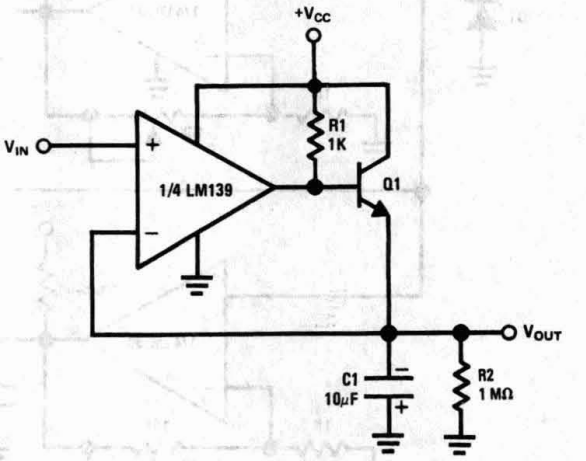

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FIGURE 42. Positive Peak Detector

of the comparator goes high, current is passed through Q_1 to charge up C_1. The only discharge path will be the 1 MΩ resistor shunting C_1 and any load that is connected to V_{OUT}. The decay time can be altered simply by changing the 1 MΩ resistor higher or lower as desired. The output should be used through a high impedance follower to avoid loading the output of the peak detector.

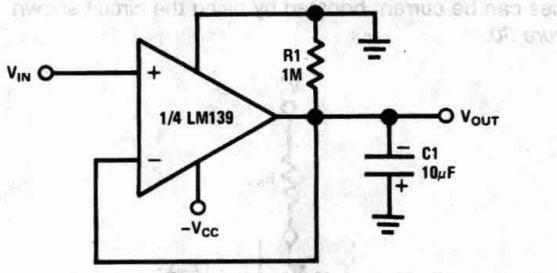

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FIGURE 43. Negative Peak Detector

For the negative peak detector, a low impedance current sink is required and the output transistor of the LM139 works quite well for this. Again the only discharge path will be the 1 MΩ resistor and any load impedance used. Decay time is changed by varying the 1 MΩ resistor.

CONCLUSION

The LM139 is an extremely versatile comparator package offering reasonably high speed while operating at power levels in the low mW region. By offering four independent comparators in one package, many logic and other functions can now be performed at substantial savings in circuit complexity, parts count, overall physical dimensions, and power consumption.

For limited temperature range application, the LM239 or LM339 may be used in place of the LM139.

It is hoped that this application note will provide the user with a guide for using the LM139 and also offer some new application ideas.

IC Preamplifier Challenges Choppers on Drift

National Semiconductor
Application Note 79

Since the introduction of monolithic IC amplifiers there has been a continual improvement in DC accuracy. Bias currents have been decreased by 5 orders of magnitude over the past 5 years. Low offset voltage drift is also necessary in a high accuracy circuits. This is evidenced by the popularity of low drift amplifier types as well as the requests for selected low-drift op amps. However, until now the chopper stabilized amplifier offered the lowest drift. A new monolithic IC preamplifier designed for use with general purpose op amps improves DC accuracy to where the drift is lower than many chopper stabilized amplifiers.

INTRODUCTION

Chopper amplifiers have long been known to offer the lowest possible DC drift. They are not without problems, however. Most chopper amps can be used only as inverting amplifiers, limiting their applications. Chopping can introduce noise and spikes into the signal. Mechanical choppers need replacement as well as being shock sensitive. Further, chopper amplifiers are designed to operate over a limited power supply, limited temperature range.

Previous low-drift op amps do not provide optimum performance either. Selected devices may only meet their specified voltage drift under restrictive conditions. For example, if a 741 device is selected without offset nulling, the addition of a offset null pot can drastically change the drift. Low drift op amps designed for offset balancing have another problem. The resistor network used in the null circuit is designed to null the drift when the offset voltage is nulled. The mechanism to achieve nulled drift depends on the difference in temperature coefficient between the internal resistors and the external null pot. Since the internal resistors have a nonlinear temperature coefficient and may vary device to device as well as between manufacturers, it can only approximately null offset drift. The problem gets worse if the external null pot has a TC other than zero.

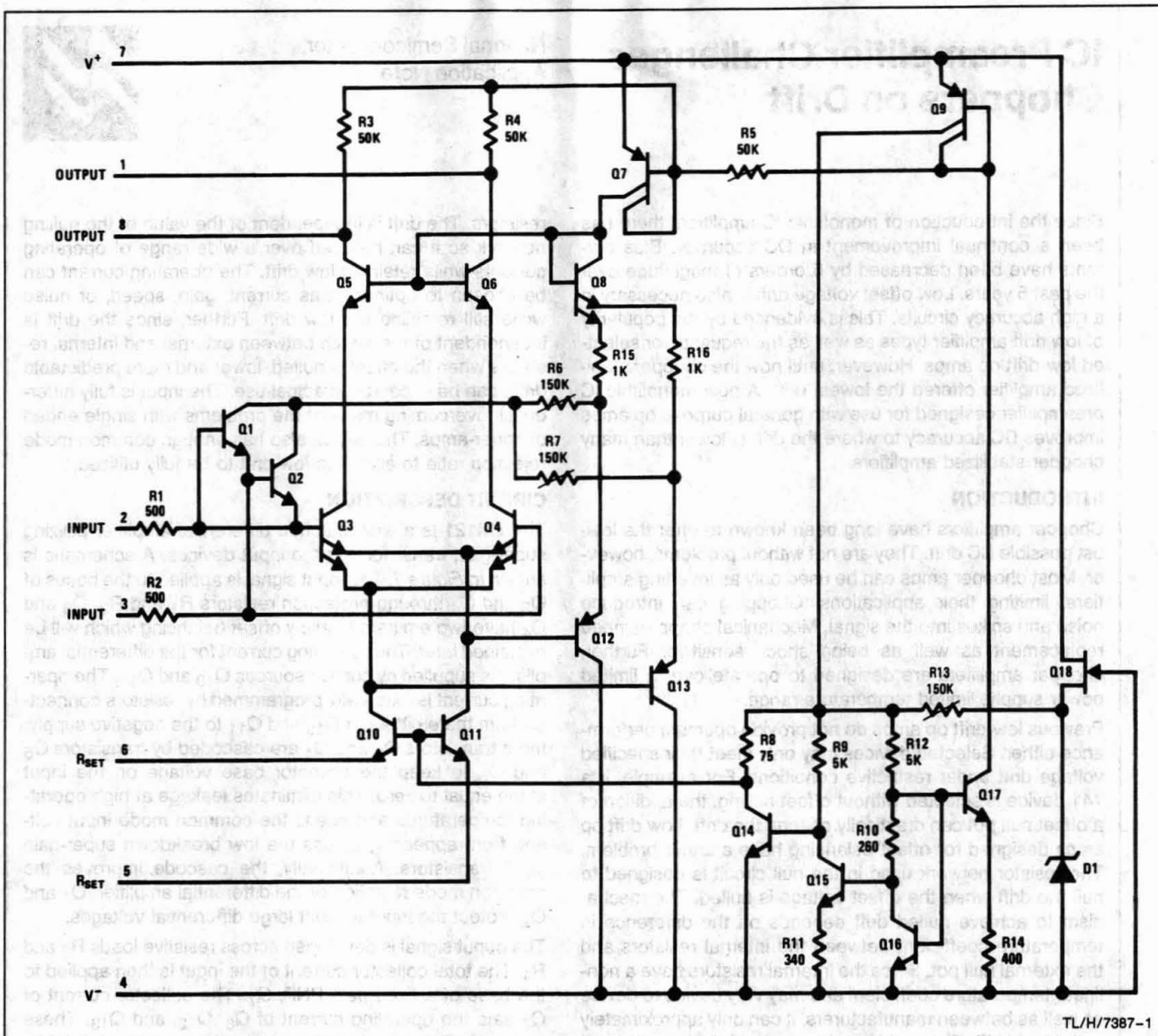
A new IC preamplifier is now available which can give drifts as low as 0.2 μV/°C. It is used with conventional op amps and eliminates the problems associated with older devices. As well as improving the DC input characteristics of the op amp, loop-gain is increased when an LM121 is used. This further improves overall accuracy since DC gain error is decreased.

The LM121 preamp is designed to give zero drift when the offset voltage is nulled to zero. The operating current of the LM121 is programmable by the value of the null network resistors. The drift is independent of the value of the nulling network so it can be used over a wide range of operating currents while retaining low drift. The operating current can be chosen to optimize bias current, gain, speed, or noise while still retaining the low drift. Further, since the drift is independent of the match between external and internal resistors when the offset is nulled, lower and more predictable drifts can be expected in actual use. The input is fully differential, overcoming many of the problems with single ended chopper-amps. The device also has enough common mode rejection ratio to allow the low drift to be fully utilized.

CIRCUIT DESCRIPTION

The LM121 is a well matched differential amplifier utilizing super-gain transistors as the input devices. A schematic is shown in *Figure 1*. The input signal is applied to the bases of Q_3 and Q_4 through protection resistors R_1 and R_2. Q_3 and Q_4 have two emitters to allow offset balancing which will be explained later. The operating current for the differential amplifier is supplied by current sources Q_{10} and Q_{11}. The operating current is externally programmed by resistors connected from the emitters of Q_{10} and Q_{11} to the negative supply. Input transistors Q_3 and Q_4 are cascoded by transistors Q_5 and Q_6 to keep the collector base voltage on the input stage equal to zero. This eliminates leakage at high operating temperatures and keeps the common mode input voltage from appearing across the low breakdown super-gain input transistors. Additionally, the cascode improves the common mode rejection of the differential amplifier. Q_1 and Q_2 protect the input against large differential voltages.

The ouput signal is developed across resistive loads R_3 and R_4. The total collector current of the input is then applied to the base of a fixed gain PNP, Q_7. The collector current of Q_7 sets the operating current of Q_8, Q_{12}, and Q_{13}. These transistors are used to set the operating voltage of the cascode, Q_5 and Q_6. By operating the cascode biasing transistors at the same operating current as the input stage, it is possible to keep collector base voltage at zero; and therefore, collector-base leakage remains low over a wide current range. Further, this minimizes the effects of V_{BE} variations and finite transistor current gain. At high operating currents the collector base voltage of the input stage is increased by about 100 mV due to the drop across R_{15} and R_{16}. This prevents the input transistors from saturating under worst case conditions of high current and high operating temperature.



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*Pin connections shown on diagram and typical applications are for TO-5 package.

FIGURE 1. Schematic Diagram of the LM121

The rest of the devices comprise the turn-on and regulator circuitry. Transistors Q_{14}, Q_{15}, and Q_{16} form a 1.2V regulator for the bases of the input stage current source. By fixing the bases of the current sources at 1.2V, their ouput current changes proportional to absolute temperature. This compensates for the temperature sensitivity of the input stage transconductance. Temperature compensating the transconductance makes the preamp more useful in some applications such as an instrumentation amplifier and minimizes bandwidth variations with temperature. The regulator is started by Q_{18} and its operating current is supplied by Q_{17} and Q_9, *Figure 2* shows the LM121 chip.

OFFSET BALANCING

The LM121 was designed to operate with an offset balancing network connected to the current source transistors. The method of balancing the offset also minimizes the drift of the preamp. Unlike earlier devices such as the LM725, the LM121 depends only upon the highly predictable emitter base voltages of transistors to achieve low drift. Devices like the LM725 depend on the match between internal resistor temperature coefficient and the external null pot as well as the input stage transistors characteristics for drift compensation.

The input stage of the LM121 is actually two differential amplifiers connected in parallel, each having a fixed offset. The offset is due to different areas for the transistor emitters. The offset for each pair is given by:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{A_1}{A_2}$$

where k is Boltzmann's constant T is absolute temperature,

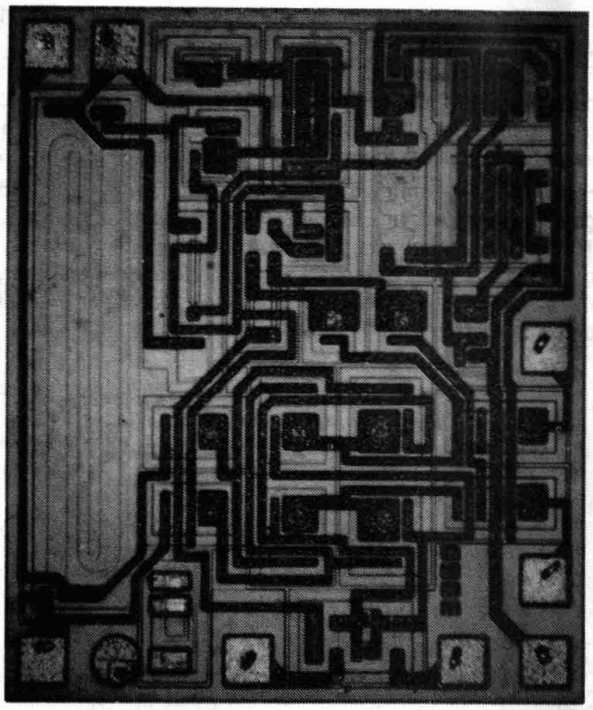

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FIGURE 2. LM121 Chip

q is the charge on an electron, and A_1 and A_2 are emitter areas. Because of the offset, each pair has a fixed drift. When the pairs are connected in parallel, if they match, the offsets and drift cancel. However, since matching is not perfect, the emitters of the pairs are not connected in parallel, but connected to independent current sources to allow offset balancing. The offset and drift effect of each pair is proportional to its operating current, so varying the ratio of the current from current sources will vary both the offset and drift. When the offset is nulled to zero, the drift is nulled to below 1 μV/°C.

The offset balancing method used in the LM121 has several advantages over conventional balancing schemes. Firstly, as mentioned earlier, it theoretically zeros the drift and offset simultaneously. Secondly, since the maximum balancing range is fixed by transistor areas, the effect of null network variations on offset voltage is minimized. Resistor shifts of one percent only cause a 30 μV shift in offset voltage on the LM121, while a one percent shift in collector resistors on a standard diff amp causes a 300 μV offset change. Finally, it allows the value of the null network to set the operating current.

ACHIEVING LOW DRIFT

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted. In many cases, the low drift of the op amp is completely swamped by external effects while the amplifier is blamed for the high drift.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Whenever dissimilar metals are joined, a thermocouple results. The voltage generated by the thermocouple is proportional to the temperature difference between the junction and the measurement end of the metal. This voltage can range between essentially zero and hundred of microvolts per degree, depending on the metals used. In any system using integrated circuits a minimum of three metals are found: copper, solder, and kovar (lead material of the IC).

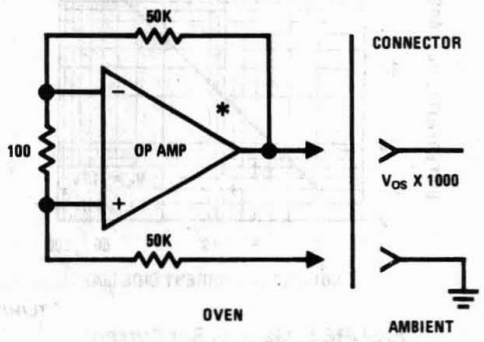
Nominally, most parts of a circuit are at the same temperature. However, a small temperature gradient can exist across even a few inches — and this is a big problem with low level signals. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally are the package-to printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

For example, a very low drift amplifier was constructed and the output monitored over a 1 minute period. During the 1 minute it appeared to have input referred offset variations of ± 5 μV. Shielding the circuit from air currents reduced this to ± 0.5 μV. The 10 μV error was due to thermal gradients across the circuit from air currents.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evenohm or managanin are best since they only generate about 2 μV/°C referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example a gain of 1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50 μV error. Most precision resistors use different material for different ranges of resistor values. It is not unexpected that resistors differing by a factor of 1000, do not track perfectly with temperature. For best results insure that the gain fixing resistors are of the same material or have tracking temperature coefficients.

Testing low drift amplifiers is also difficult. Standard drift testing techniques such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method — do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signals through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal. The circuit in *Figure 3* will yield good results if well constructed.



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*Op amp shown in *Figure 9*.

FIGURE 3. Drift Measurement Circuit

PERFORMANCE

It is somewhat difficult to specify the performance of the LM121 since it is programmable over a wide range of operating currents. Changing the operating current varies gain, bias current, and offset current — three critical parameters in a high accuracy system. However, offset voltage and drift are virtually independent of the operating current.

Typical performance at an operating current of 20 μA is shown in Table I. *Figures 4* and *5* show how the bias current, offset current, and gain change as a function of programming current. Drift is guaranteed at 1 μV/°C independent of the operating current.

TABLE I. Typical Performance at an Operating Current of 10 μA Per Side

Offset Voltage	Nulled
Bias Current	7 nA
Offset Current	0.5 nA
Offset Voltage Drift	0.3 μV/°C
Common Mode Rejection Ratio	125 dB
Supply Voltage Rejection Ratio	125 dB
Common Mode Range	±13V
Gain	20 V/V
Supply Current	0.5 mA

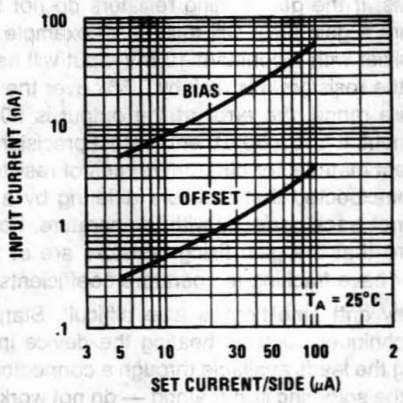

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FIGURE 4. Bias and Offset Current vs Set Current

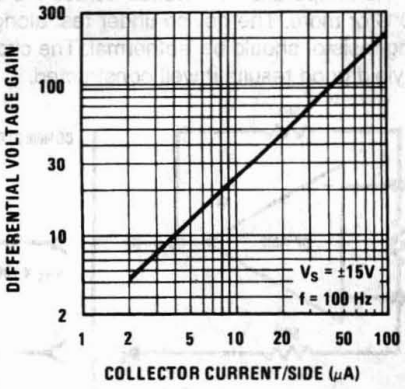

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FIGURE 5. Gain vs Set Current

Over a temperature range of −55°C to +125°C the LM121 has less than 1 μV/°C offset voltage drift when nulled. It is important that the offset voltage is accurately nulled to achieve this low drift. The drift is directly related to the offset voltage with 3.8 μV/°C drift resulting from every millivolt of offset. For example, if the offset is nulled to 100 μV, about 0.4 μV/°C will result — or twice the typically expected drift. This drift is quite predictable and could even be used to cancel the drift elsewhere in a system. *Figure 6* shows drift as a function of offset voltage. For critical applications selected devices can achieve 0.2 μV/°C.

Figures 7 and *8* show the bias current, offset current, and gain variation over a −55°C to +125°C temperature range. These performance characteristics do not tell the whole story. Since the LM121 is used with an operational amplifier, the op amp characteristics must be considered for over-all amplifier performance.

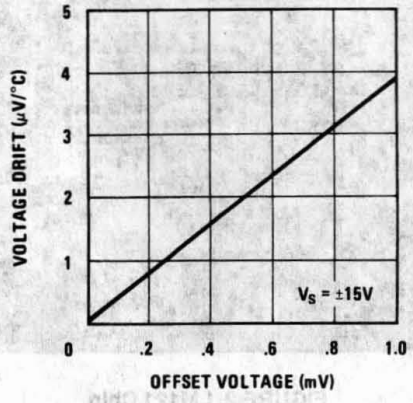

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FIGURE 6. Drift vs Offset Voltage

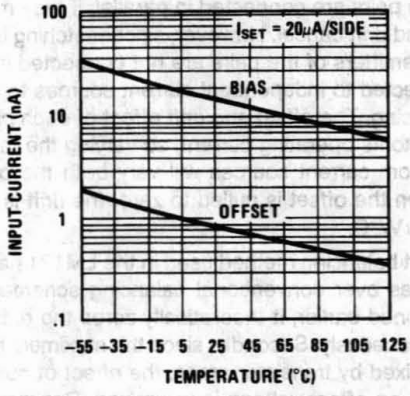

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FIGURE 7. Bias and Offset Current vs Temperature

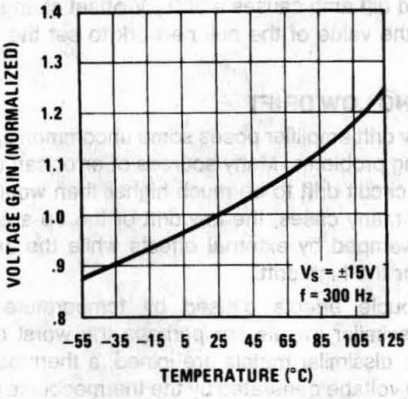

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FIGURE 8. Gain vs Temperature for the LM121

OP AMP EFFECTS

The LM121 is nominally used with a standard type of operational amplifier. The op amp functions as the second and ensuing stages of the amplifying system. When the LM121 is connected to an op amp, the two devices may be treated (and used) just as a single op amp. The inputs of the combination are the inputs of the LM121 and the output is from the op amp. Feedback, as with any op amp, is applied back to the inputs. *Figure 9* shows the general configuration of an amplifier using the LM121.

The offset voltage and drift of the op amp used have an effect on overall performance and must be considered. (The bias and offset currents of today's op amp are low enough to be ignored.) Although the exact effects of the op amp stage are difficult and tedious to calculate, a few approximations will show the sources of drift.

Op amp drift is perhaps the most important source of error. Drift of the op amp is directly reduced by the gain of the LM121. The drift referred to the input is given by:

$$\text{input drift} = \frac{\text{op amp drift}}{\text{LM121 gain}} + \text{LM121 drift.}$$

If the op amp has a drift of 10 μV/°C and the LM121 is operated at a gain of $A_V = 50$, there will be a 0.2 μV/°C component of the total drift due to the op amp. It is therefore important that the LM121 be operated at relatively high gain to minimize the effects of op amp drift. Lower gains for the LM121 will give proportionately less reduction in op amp drift. Of course, a moderately low drift op amp such as the LM108A eases the problem.

Op amp offset voltage also has an effect on total drift. For purpose of analysis assume the LM121 to be perfect with no offset or drift of its own. Then any offset seen when the LM121 is connected to an op amp is due to the op amp alone. The offset is equal to:

$$\text{offset voltage} = \frac{\text{op amp offset}}{\text{LM121 gain}}$$

or the offset is reduced by the gain of the LM121. For example, with a gain of 50 for the LM121, 2 mV of offset on the op amp appears as 40 μV of offset at the LM121 input. Unlike offset due to a mismatch in the LM121, this 40 μV of offset does not cause any drift. However, when the system is nulled so the offset at the input of the LM121 is zero, 40 μV of imbalance has been inserted into the LM121. The imbalance caused by nulling the offset induced by the op amp will cause a drift of about 0.14 μV/°C. With the system nulled the drift due to op amp will cause a drift of about 0.15 μV/°C. With the system nulled the drift due to op amp offset can be expressed as:

$$\text{drift } (\mu\text{V/°C}) = \frac{\text{op amp offset (mV)}}{\text{LM121 gain}} (3.6\ \mu\text{V/°C}).$$

In actual operation, drift due to op amp offsets will usually be better than predicted. This is because offset voltage and drift are not independent. With the LM121 there is a strong, predictable, correlation between offset and drift. Also, there is a correlation with op amps, but it is not as strong. The drift of the op amp tends to cancel the drift induced in the LM121 when the system is nulled.

In the previous example the drift due to the op amp offset was 0.15 μV/°C. If the op amp has a drift of 3.6 μV/°C per millivolt of offset (like the LM121) it will have a drift of 7.2 μV/°C. This drift is reduced by the gain of the LM121 ($A_V = 50$) to 0.14 μV/°C. This 0.14 μV/°C will cancel the 0.14 μV/°C drift due to balancing the LM121. Since op amps do not always have a strong correlation between offset and drift, the cancellation of drifts is not total. Once again, high gain for the LM121 and a low offset op amp helps achieve low drifts.

FREQUENCY COMPENSATION

The additional gain of the LM121 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. This is because the additional gain introduced by the LM121 must be rolled-off before the phase shift through the LM121 and op amp reaches 180°. The additional compensation depends on the gain of the LM121 as well as the closed loop gain of the system. Two frequency compensation techniques are shown here that will operate with any op amp that is unity gain stable.

When the closed loop gain of the op amp with the LM121 is less than the gain of the LM121 alone, more compensation is needed. The worst case situation is when there is 100% feedback — such as a voltage follower or integrator — and the gain of the LM121 is high. When high closed loop gains are used — for example $A_V = 1000$ — and only an additional gain of 100 is inserted by the LM121, the frequency compensation of the op amp will usually suffice.

The basic circuit of the LM121 in *Figure 9* shows two compensation capacitors connected to the op amp (disregarding the 30 pF frequency compensation for the op

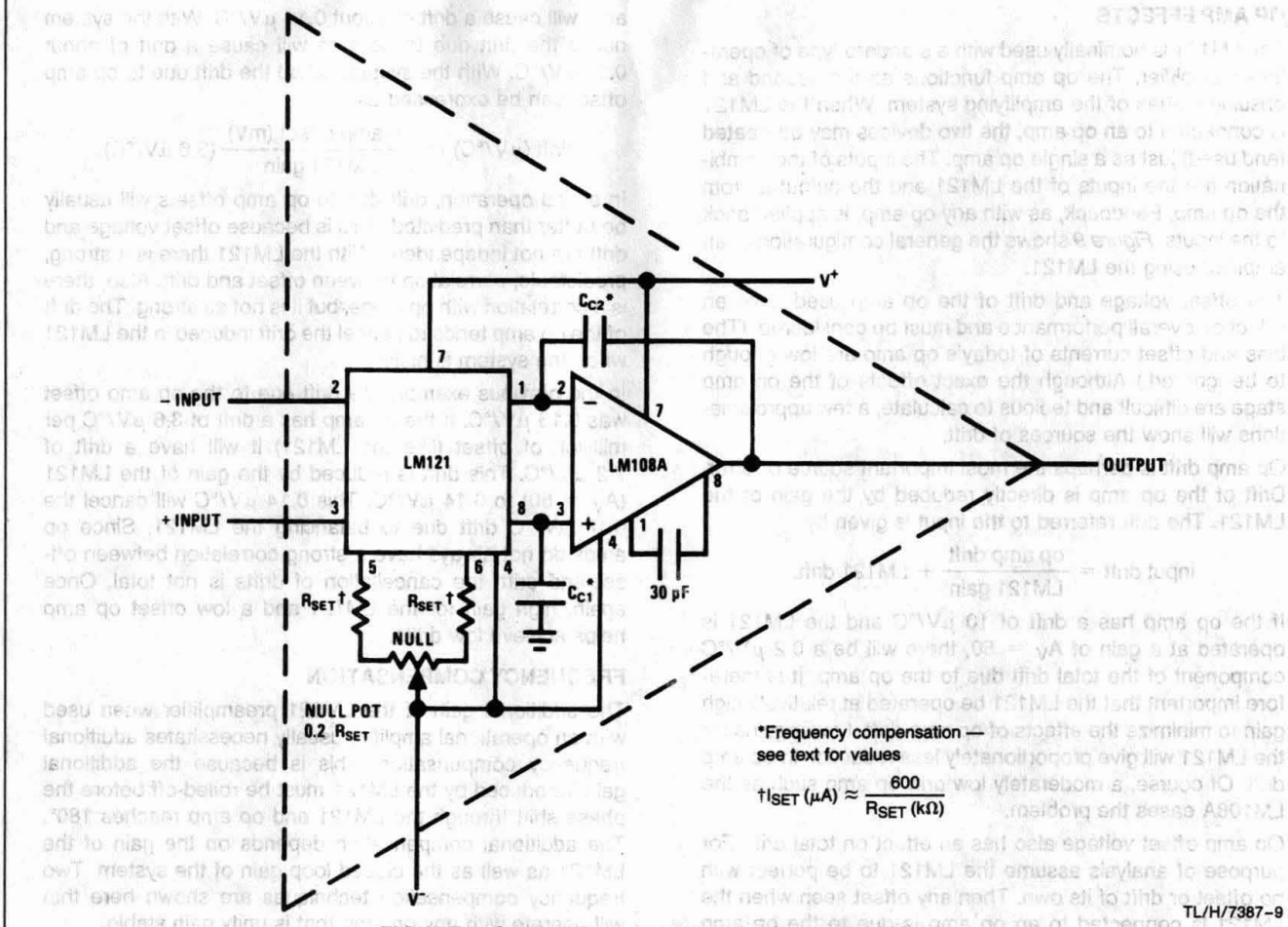

FIGURE 9. General Purpose Amplifier Using the LM121

amp alone). The capacitor from pin 6 to pin 2 around the op amp acts as an integrating capacitor to roll off the gain. Since the output of the LM121 is differential, a second capacitor is needed to roll off pin 3 of the op amp. These capacitors are C_{C1} and C_{C2} in *Figure 9*.

With capacitors equal, the circuit retains good AC power supply rejection. The approximate value of the compensation capacitors is given by:

$$C_C = \frac{8}{10^6 A_{CL} R_{SET}} \text{ farads}$$

where R_{SET} is the current set resistor from each current source and where A_{CL} is closed loop gain. Table II shows typical capacitor values.

An alternate compensation scheme was developed for applications requiring more predictable and smoother roll off. This is useful where the amplifier's gain is changed over a wide range. In this case C_{C1} is made large and connected to V^+ rather than ground. The output of the LM121 is rendered single ended by a 0.01 μF bypass capacitor to V^+. Overall frequency compensation then is achieved by an integrating capacitor around the op amp:

$$\text{Bandwidth at unity gain} \cong \frac{12}{2\pi R_{SET} C}$$

$$\text{for 0.5 MHz bandwidth } C = \frac{4}{10^6 R_{SET}}$$

TABLE II. Typical compensation capacitors for various operating currents and closed loop gains. Values given apply to LM101A, LM108, and LM741 type amplifiers.

Closed Loop Gain	Current Set Resistor				
	120 kΩ	60 kΩ	30 kΩ	12 kΩ	6 kΩ
$A_V = 1$	68 pF	130 pF	270 pF	680 pF	1300 pF
$A_V = 5$	15 pF	27 pF	50 pF	130 pF	270 pF
$A_V = 10$	10 pF	15 pF	27 pF	68 pF	130 pF
$A_V = 50$	1 pF	3 pF	5 pF	15 pF	27 pF
$A_V = 100$		1 pF	3 pF	5 pF	10 pF
$A_V = 500$			1 pF	1 pF	3 pF
$A_V = 1000$					

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz. If closed loop gain is greater than unity "C" may be decreased to:

$$C = \frac{4}{10^6 A_{CL} R_{SET}}$$

APPLICATIONS

No attempt will be made to include precision op amp applications as they are well covered in other literature. The previous sections detail frequency compensation and drift problems encountered in using very low drift op amps. The circuit shown in *Figure 9* will yield good results in almost any op amp application. However, it is important to choose the operating current properly. From the curves given it is relatively easy to see the effects of current changes. High currents increase gain and reduce op amp effects on drift. Bias and offset current also increase at high current. When the operating source resistance is relatively high, errors due to high bias and offset current can swamp offset voltage drift errors. Therefore, with high source impedances it may be advantageous to operate at lower currents.

Another important consideration is output common mode voltage. This is the voltage between the outputs of the LM121 and the positive power supply. Firstly, the output common mode voltage must be within the operating common mode range of the output op amp. At currents above 10 μA there is no problems with the LM108, LM101, and LM741 type devices. Higher currents are needed for devices with more limited common mode range, such as the LM118. As the operating current is increased, the positive common mode limit for the LM121 is decreased. This is because there is more voltage drop across the internal 50k load resistors. The output common mode voltage and positive common mode limits are about equal and given by:

$$\text{Output common mode voltage positive common mode limit} \approx V^+ - \left(0.6V + \frac{0.65 \times 50\ k\Omega}{R_{SET}}\right)$$

If it is necessary to increase the common mode output voltage (or limit), external resistors can be connected in parallel with the internal 50 kΩ resistors. This should only be done at high operating currents (80 μA) since it reduces gain and diverts part of the input stage current from the internal biasing circuitry. A reasonable value for external resistors is 50 kΩ.

The external resistors should be of high quality and low drift, such as wirewound resistors, since they will affect drift if they do not track well with temperature. A 20 ppm/°C difference in external resistor temperature coefficient will introduce an additional 0.3 μV/°C drift.

An unusually simple gain of 1000 instrumentation amplifier can be made using the LM121. The amplifier has a floating, full differential, high impedance input. Linearity is better than 1%, depending upon input signal level with maximum error at maximum input. Gain stability, as shown in *Figure 10*, is about ±2% over a −55°C to +125°C temperature range. Finally, the amplifier has very low drift and high CMRR.

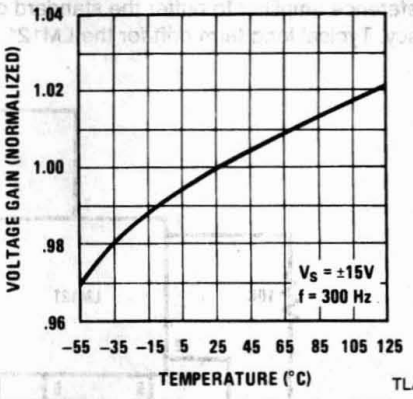

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FIGURE 10. Instrumentation Amplifier Gain vs Temperature

Figure 11 shows a schematic of the instrumentation amplifier. The LM121 is used as the input stage and operated open-loop. It converts an input voltage to a differential output current at pins 1 and 8 to drive an op amp. The op amp acts as a current to voltage converter and has a single-ended output.

Resistors R_1 and R_2 with null pot R_3 set the operating current of the LM121 and provide offset adjustment. R_4 is a fine trim to set the gain at 1000. There is very little interaction between the gain and null pots.

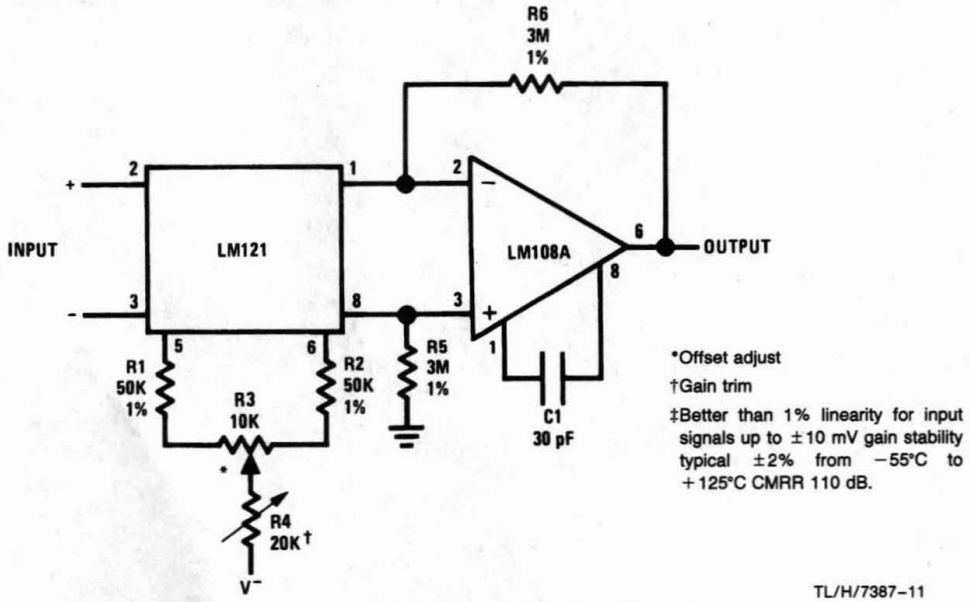

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FIGURE 11. Gain of 1000 Instrumentation Amplifier

This instrumentation amplifier is limited to a maximum input signal of ±10 mV for good linearity. At high signal levels the transfer characteristic of the LM121 becomes rapidly nonlinear, as with any differential amplifier. Therefore, it is most useful as a high gain amplifier.

Since feedback is not applied around the LM121, CMRR is not dependent on resistor matching. This eliminates the need for precisely matched resistor as with conventional instrumentation amplifiers. Although the linearity and gain stability are not as good as conventional schemes, this amplifier will find wide application where low drift and high CMRR are necessary.

A precision reference using a standard cell is shown in *Figure 12*. The low drift and low input current of the LM121A allow the reference amplifier to buffer the standard cell with high accuracy. Typical long term drift for the LM121 operating at constant temperature is less than 2 μV per 1000 hours.

To minimize temperature gradient errors, this circuit should be shielded from air currents. Good single-point wiring should also be used. When power is not applied, it is necessary to disconnect the standard cell from the input of the LM121 or it will discharge through the internal protection diodes.

CONCLUSIONS

A new preamplifier for operational amplifiers has been described. It can achieve voltage drifts as low as many chopper amplifiers without the problems associated with chopping. Operating current is programmable over a wide range so the input characteristics can be optimized for the particular application. Further, using a preamp and a conventional op amp allows more flexibility than a single low-drift op amp.

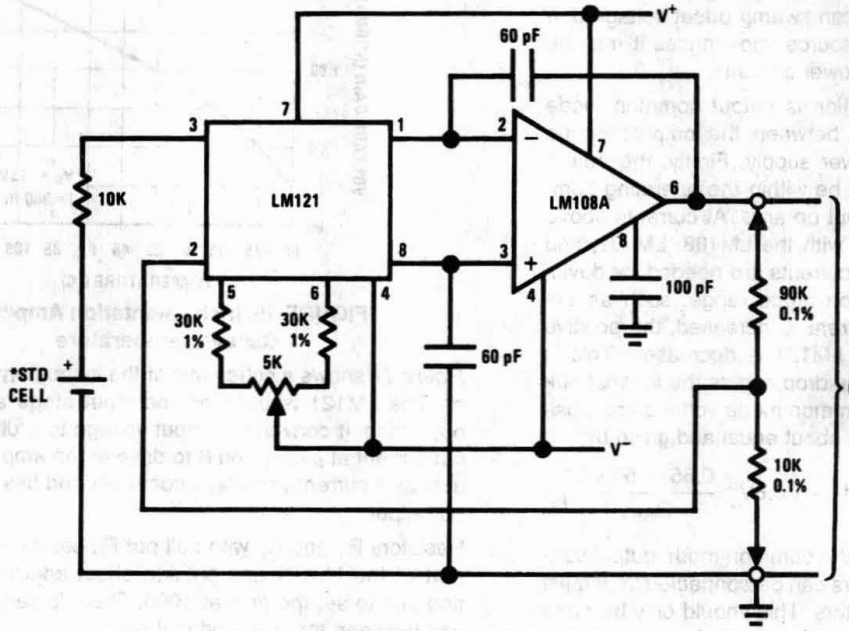

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FIGURE 12. 10V Reference

LM125 Precision Dual Tracking Regulator

National Semiconductor
Application Note 82

INTRODUCTION

The LM125 is a precision, dual, tracking, monolithic voltage regulator. It provides separate positive and negative regulated outputs, thus simplifying dual power supply designs. Operation requires few or no external components depending on the application. Internal settings provide fixed output voltages at ±15V.

Each regulator is protected from excessive internal power dissipation by a thermal shutdown circuit which turns off the regulator whenever the chip reaches a preset maximum temperature. Other features include both internal and external current limit sensing for device protection while operating with or without external current boost. For applications requiring more current than the internal current limit will allow, boosted operation is possible with the addition of a one NPN pass transistor per regulator. External resistors sense load current for controlling the limiting circuitry. Internal frequency compensation is provided on both positive and negative regulators. The internal voltage reference pins is brought out to facilitate noise filtering when desired.

CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the basic dual tracking regulator. A voltage reference establishes a fixed dc level, independent of supply or temperature variations, at the noninverting input to the negative regulator Error Amplifier. The Error Amplifier drives the Output Control Circuit which includes the high current output transistors, current limiting, and thermal shutdown circuitry.

The negative regulator output voltage is established by comparing the Voltage Reference against a fraction of the output as set by R_A and R_B. To achieve the desired tracking action of the positive regulator, a voltage established between the positive and negative regulator outputs by resistors R_C and R_D is compared to ground by the positive regulator Error Amplifier. This insures that the positive regulator output voltage will always equal the negative regulator output voltage multiplied by the unity ratio of R_C to R_D. The positive regulator Output Control Circuit is essentially the same as that in the negative regulator.

The current limit and thermal shutdown circuitry sense the output load current and die temperature respectively and

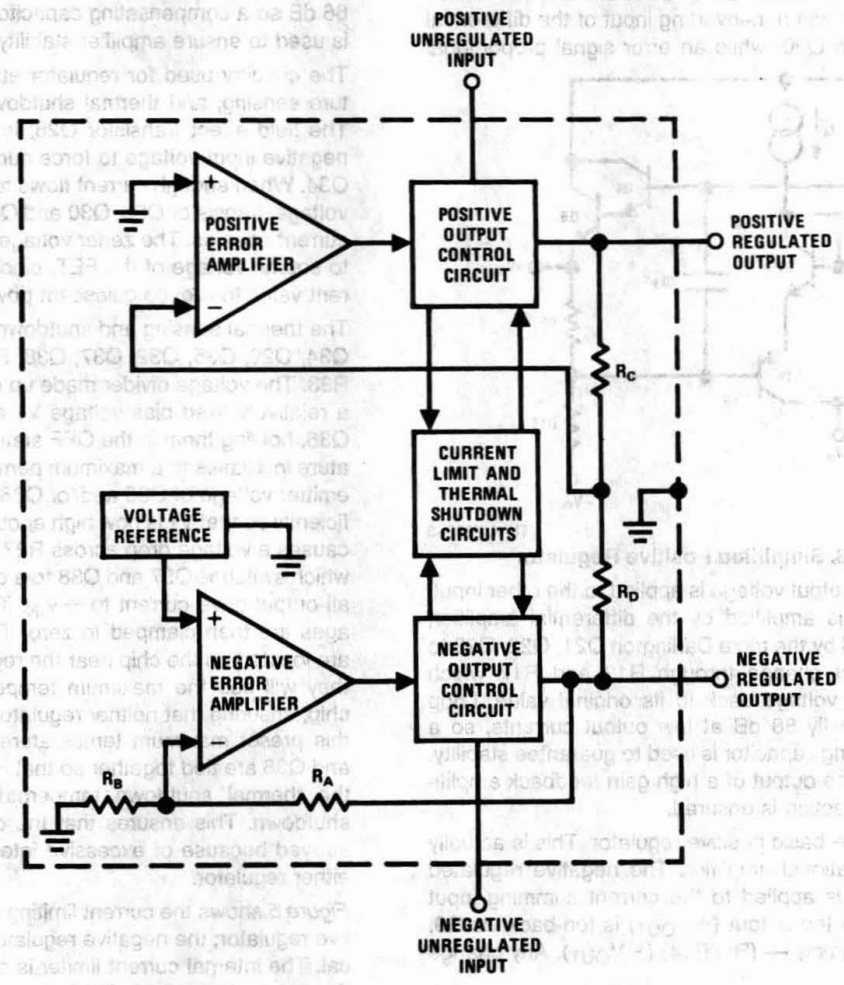

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FIGURE 1. Block Diagram for the Basic Dual Tracking Regulator

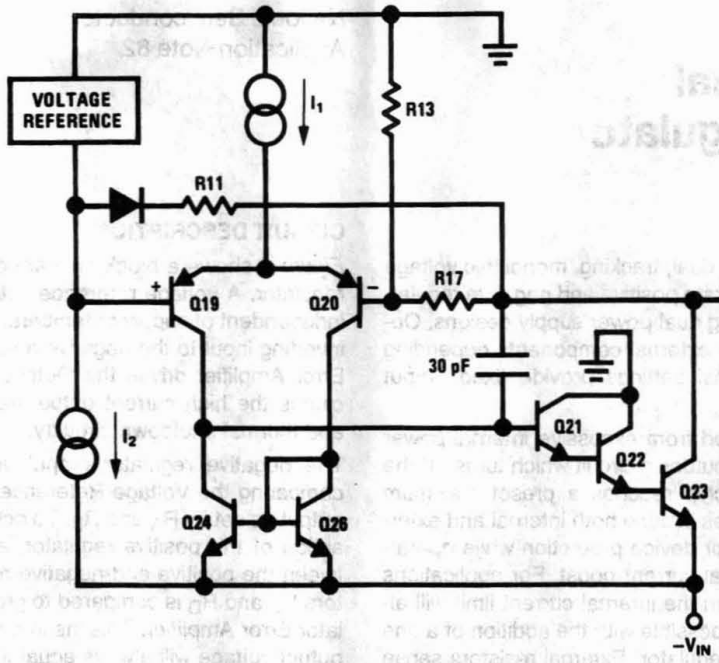

FIGURE 2. Simplified Negative Regulator

switch off all output drive capability upon reaching their predetermined limits.

Figure 2 gives a more detailed picture of the negative regulator circuitry. The temperature compensated reference voltage appears at the non-inverting input of the differential amplifier, Q19 and Q20, while an error signal proportional

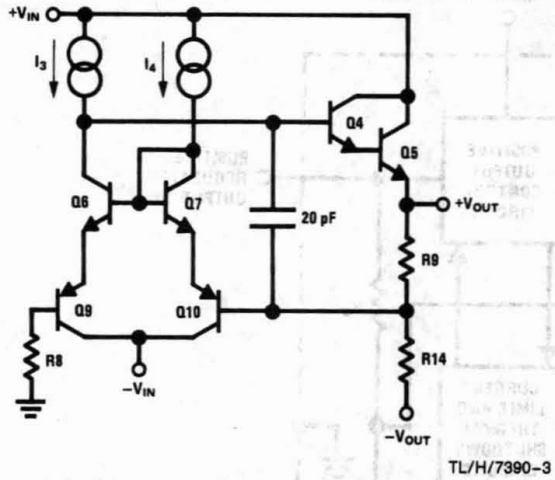

FIGURE 3. Simplified Positive Regulator

to any change in output voltage is applied to the other input. This error signal is amplified by the differential amplifier, Q19 and Q20, and by the triple Darlington Q21, Q22, Q23 to produce a current change through R13 and R17 which brings the output voltage back to its original value. Loop gain is high, typically 88 dB at low output currents, so a 30 pF compensating capacitor is used to guarantee stability. Since $-V_{OUT}$ is the output of a high gain feedback amplifier, high supply rejection is ensured.

Figure 3 shows the basic positive regulator. This is actually an inverting operational amplifier. The negative regulated voltage ($-V_{OUT}$) is applied to the current summing input through R14 while the output ($+V_{OUT}$) is fed-back via R9. Then $+V_{OUT}$ is simply — (R9/R14) ($-V_{OUT}$). Any change in the positive regulator output will create an error signal at the base of Q10 which will be amplified and sent to the voltage follower, Q4 and Q5, forcing the output voltage to track the input voltage. Here the loop gain is on the order of 66 dB so a compensating capacitor of approximately 20 pF is used to ensure amplifier stability.

The circuitry used for regulator start up, biasing, temperature sensing, and thermal shutdown is shown in *Figure 4*. The field effect transistor Q28, is initially ON allowing the negative input voltage to force current through zener diode Q34. When enough current flows to fully establish the zener voltage, transistor Q29, Q30 and Q31 turn on and bias up all current sources. The zener voltage also decreases the gate to source voltage of the FET, pinching it off to a lower current value to reduce quiescent power dissipation.

The thermal sensing and shutdown circuitry is comprised of Q34, Q29, Q35, Q32, Q37, Q38, R27, R29, R30, R31, and R33. The voltage divider made up of R29 and R30 provides a relatively fixed bias voltage V_1 at the bases of Q35 and Q36, holding them in the OFF state. When the chip temperature increases to a maximum permissible level, the base to emitter voltage of Q35 and/or Q36 will have decreased sufficiently so that V_1 is now high enough to turn them ON. This causes a voltage drop across R27 sufficient to turn on Q32 which switches Q37 and Q38 to a conducting state shunting all output drive current to $-V_{IN}$. The regulator output voltages are then clamped to zero. Transistors Q35 and Q36 are located on the chip near the regulator output devices so they will see the maximum temperatures reached on the chip, ensuring that neither regulator will ever see more than this preset maximum temperature. The collectors of Q35 and Q36 are tied together so that if either regulator reaches the thermal shutdown temperature, both regulators will shutdown. This ensures that the device can never be destroyed because of excessive internal power dissipation in either regulator.

Figure 5 shows the current limiting circuitry used in the positive regulator; the negative regulator current limiter is identical. The internal current limiter is comprised of Q8 and R5; the external current limiter is comprised of Q11 and an external resistor R_{CL}. Both operate in a similar manner. As the

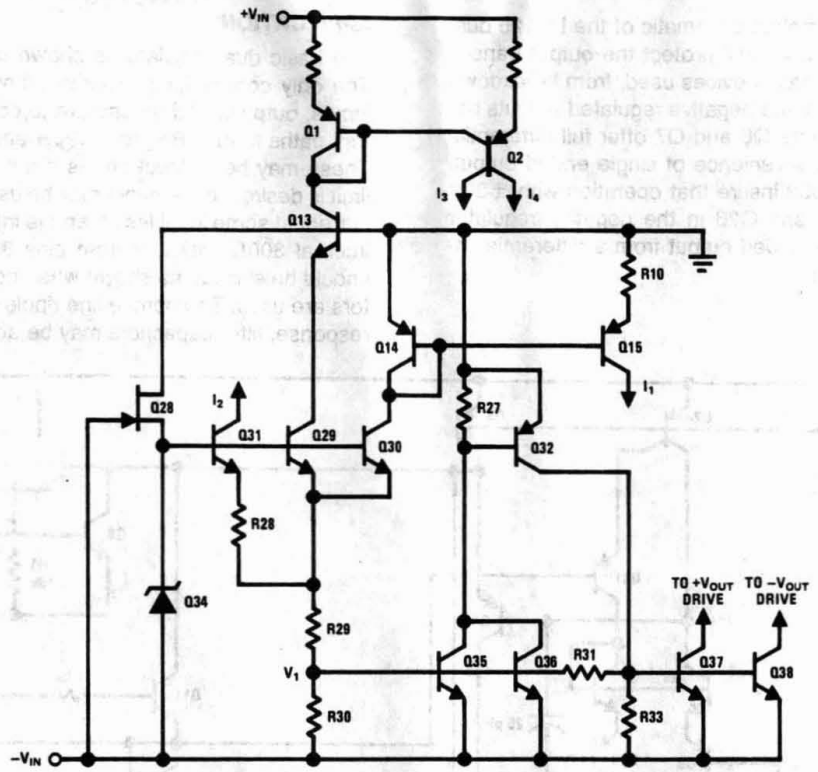

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FIGURE 4. Start-up, Biasing and Thermal Shutdown Circuitry

output current through Q5 increases, the voltage drop across resistor R5 eventually turns ON Q8 and shunts all base drive away from the output devices, Q4 and Q5. The maximum load current available with this circuit is approximately 250 mA at $T_j = 25°C$ (see *Figure 9*).

The external current limiting circuit works in a similar manner. Here the output current is sensed across the external resistor R_{CL}. When the voltage drop across R_{CL} is sufficient to turn ON transistor Q11, the output drive current is switched away from the output devices Q4 and Q5. This externally set current limit is particularly valuable when used with an external current boosting pass transistor where the current limit could be set to protect that transistor from excessive power dissipation.

The constant voltage reference circuit is shown in *Figure 6*. Zener diode Z_1 has a positive temperature coefficient of known value. V_{BE} of Q18 (negative temperature coefficient) is multiplied by the ratio of R18 and R19 and added to the positive TC of Z_1 to produce a near zero TC voltage reference. Current source I_2 is used only during start-up.

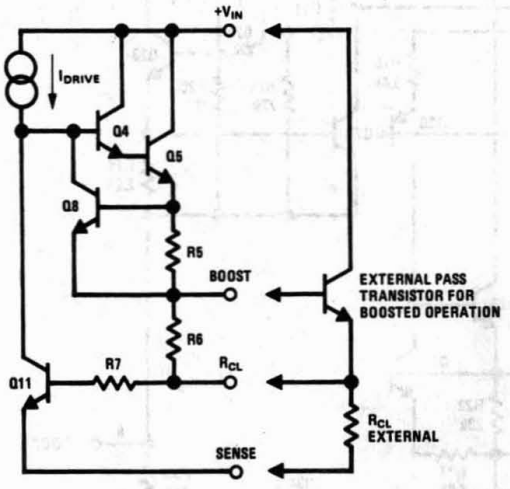

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FIGURE 5. Positive Regulator Current Limiting Circuitry

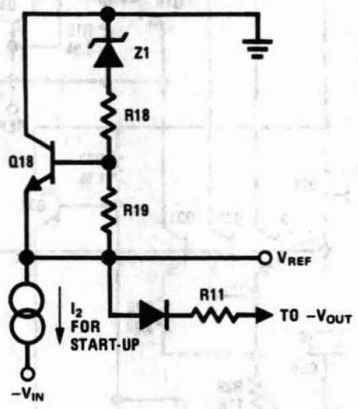

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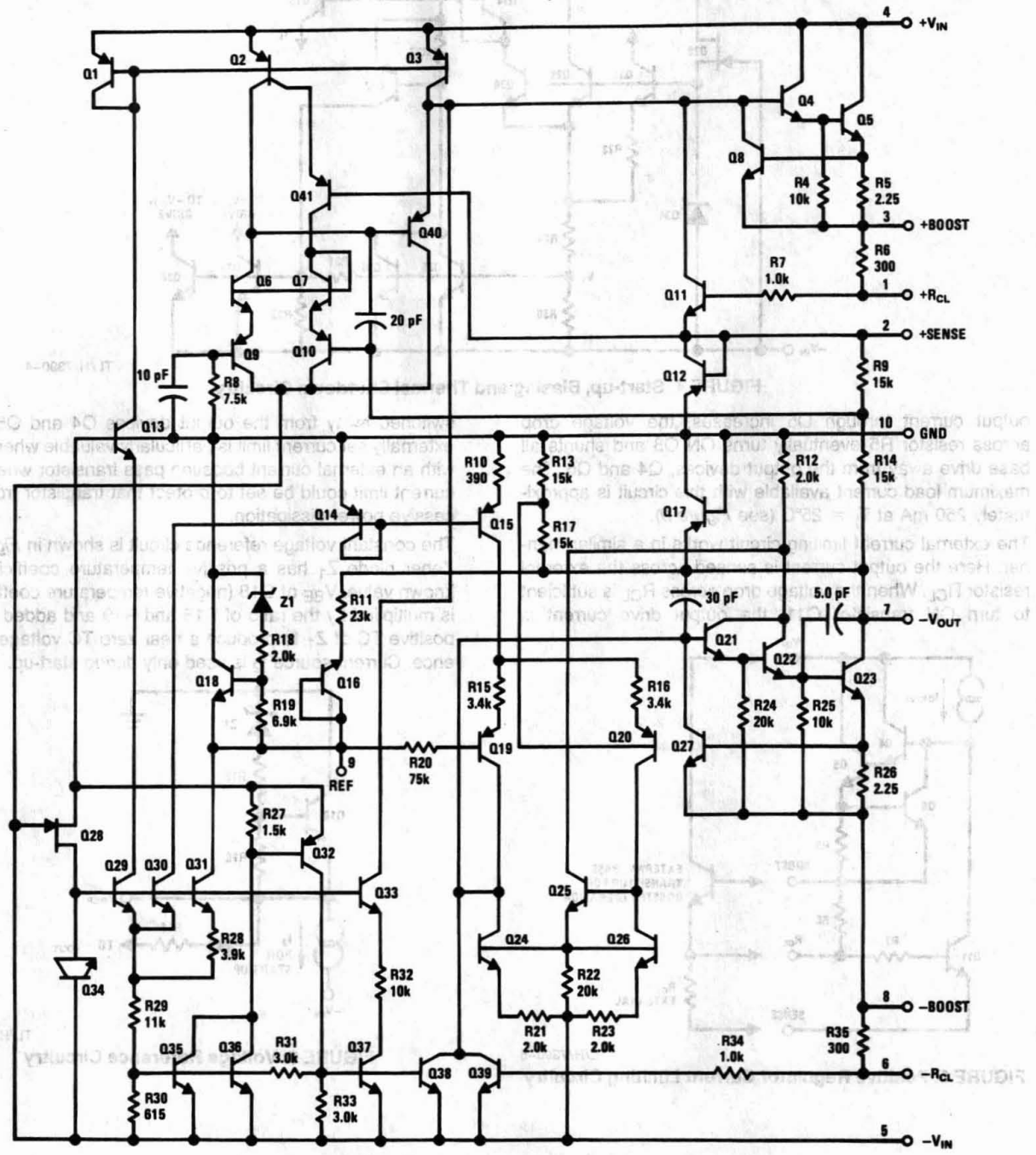
FIGURE 6. Voltage Reference Circuitry

Figure 7 shows the complete schematic of the LM125 dual regulator. Diodes Q12 and Q17 protect the output transistors, plus any external pass devices used, from breakdown in the event the positive and negative regulated outputs become shorted. Transistors Q6 and Q7 offer full differential voltage gain with the convenience of single ended output. Transistors Q13 and Q33 insure that operation with ±30V input is possible. Q24 and Q26 in the negative regulator amplifier provide single ended output from a differential input with no loss in gain.

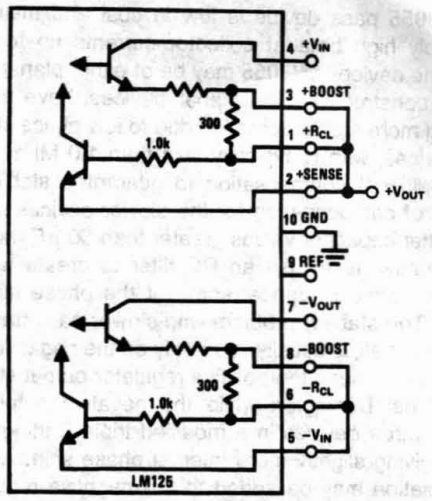
APPLICATIONS

The basic dual regulator is shown connected in *Figure 8.* The only connections required other than plus and minus inputs, outputs, and ground are to complete the output current paths from $+R_{CL}$ to $+V_{OUT}$ and from $-R_{CL}$ to $-V_{IN}$. These may be a direct shorts if the internal preset current limit is desired, or resistors may be used to set the maximum current at some level less than the internal current limit. The internal 300Ω resistors from pins 3 to 1 and pins 8 to 6 should be shorted as shown when no external pass transistors are used. To improve line ripple rejection and transient response, filter capacitors may be added to the inputs, out-



Note: Pin numbers apply to metal can package only. TL/H/7390–7

FIGURE 7. LM125



Note: Pin numbers for metal can package only. TL/H/7390–8

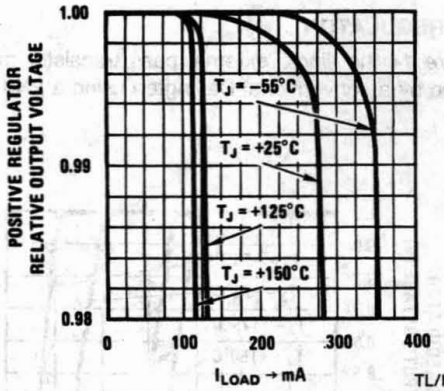
FIGURE 8. Basic Dual Regulator

puts, or both, depending on the unregulated input available. If a very low noise output voltage is desired, a capacitor may be connected from the reference voltage pin to ground. Thus shunting noise generated by the reference zener. *Figure 9* shows the internal current limiting characteristics for the basic regulator circuit of *Figure 8*.

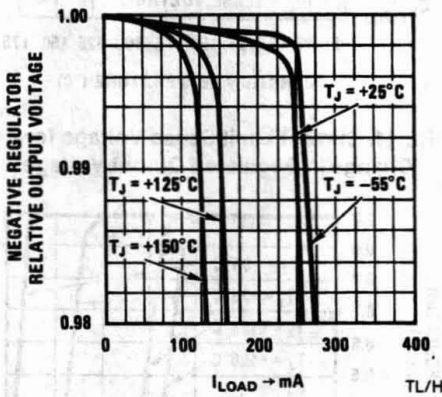
HIGH CURRENT REGULATOR

For applications requiring more supply current than can be delivered by the basic regulator, an external NPN pass transistor may be added to each regulator. This will increase the maximum output current by a factor of the external transistor beta. The circuit for current boosted operation is shown in *Figure 10*.

In the boosted mode, current limiting is often a necessary requirement to insure that the external pass device is not overheated or destroyed. Experience shows this to be the usual cause of IC regulator failure. If the regulator output is grounded the pass device may fail and short, destroying the regulator. To limit the maximum output current, a series resistor (R_{CL} in *Figure 10*) is used to sense load current. The regulator will current limit when the voltage drop across R_{CL}

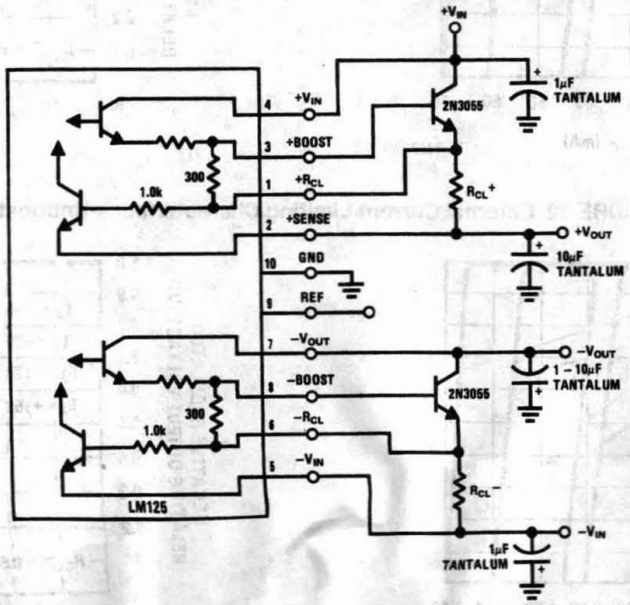


(a) TL/H/7390–9



(b) TL/H/7390–10

FIGURE 9. Internal Current Limiting Characteristics



TL/H/7390–11

FIGURE 10. Boosted High Current Regulator

equals the current limit sense voltage found in *Figure 11*. *Figure 12* shows the external current limiting characteristics unboosted and *Figure 13* shows the external current limiting characteristics in the boosted mode.

To ensure circuit stability at high currents in this configuration, it may be necessary to bypass each input with low inductance, tantalum capacitors to prevent forming resonant circuits with long input leads. A C ≥ 1 μF is recommended. The same problem can also occur at the regulator output where a C ≥ 10 μF tantalum will ensure stability and increase ripple rejection.

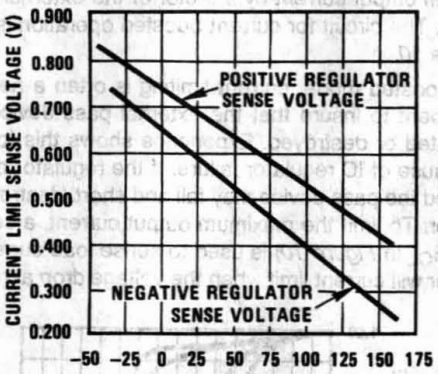


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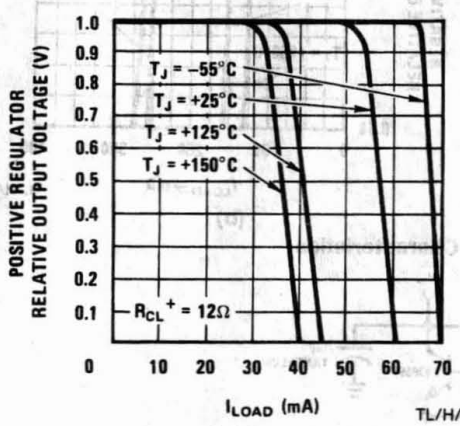
FIGURE 11. Current Limit Sense Voltage for a 0.1% Change in Regulated Output Voltage



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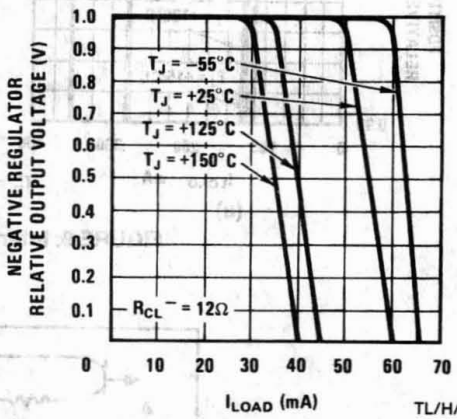
(a)



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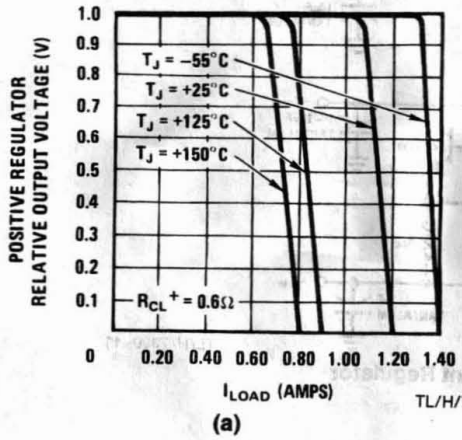
(b)

FIGURE 12. External Current Limiting Characteristics-Unboosted



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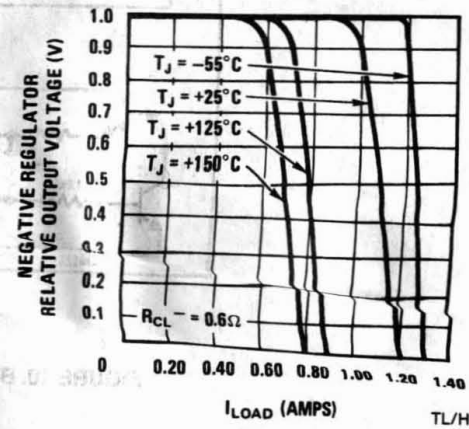
(a)



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(b)

FIGURE 13. External Current Limiting Characteristics-Boosted

The 2N3055 pass device is low in cost and maintains a reasonably high beta at collector currents up to several amps. The devices 2N3055 may be of either planar or alloy junction construction. The planar devices, have a high f_T providing more stable operation due to low phase shift. The alloy devices, with f_T typically less than 1.0 MHz, may require additional compensation to guarantee stability. The simplest of compensation for the slower devices is to use output filter capacitor values greater than 50 μF (tantalum). An alternative is to use an RC filter to create a leading phase response to cancel some of the phase lag of the devices. The stability problem with slower pass transistors, if it occurs at all, is usually seen only on the negative regulator. This is because the positive regulator output stage is a conventional Darlington while the negative output stage contains three devices in a modified triple Darlington connection giving slightly more internal phase shift. Additional compensation may be added to the negative regulator by connecting a small capacitor in the 100 pF range from the negative boost terminal to the internal reference. Since the positive regulator uses the negative regulator output for a reference, this also offers some additonal indirect compensation to the positive regulator.

7 AMP REGULATOR

In *Figure 14* the single external pass transistor has been replaced by a conventional Darlington using a 2N3715 and

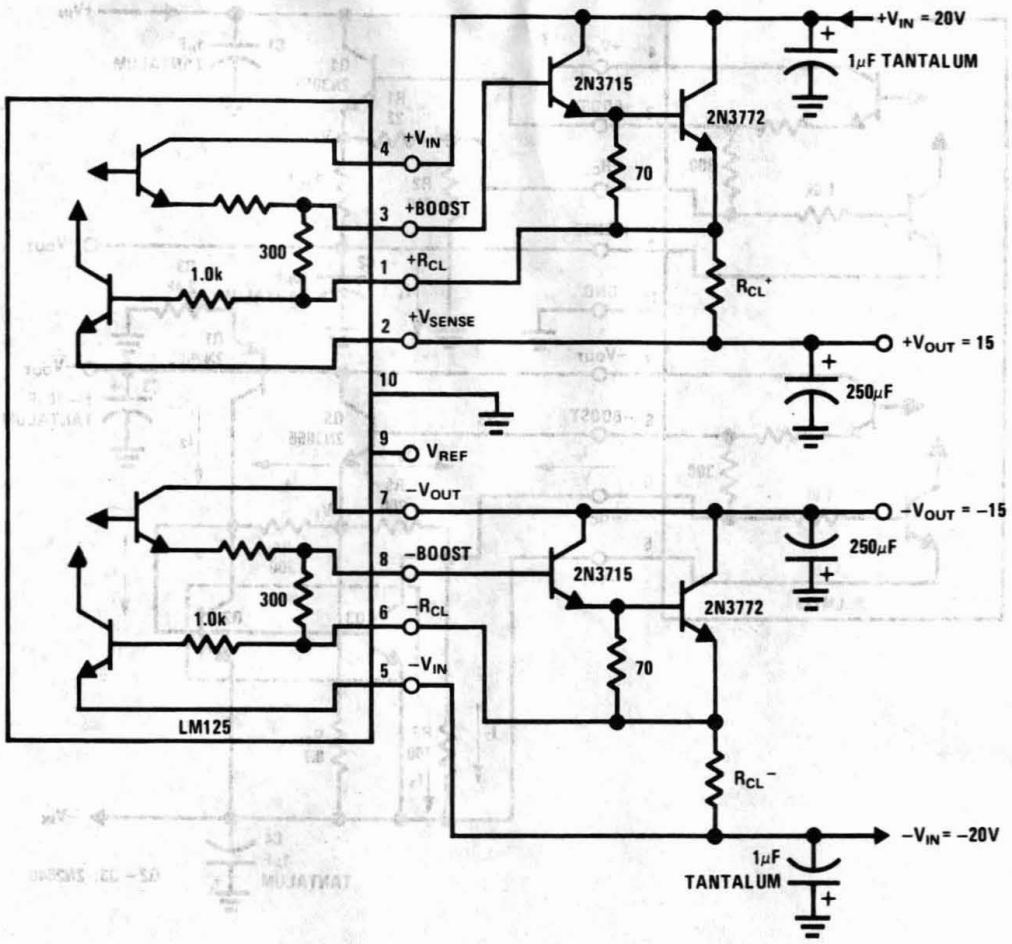

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FIGURE 14. High Current Regulator Using a Darlington Pair for Pass Elements

a 2N3772. With this configuration the output current can reach values to 10A with very good stability. The external Darlington stage increases the minimum input-output voltage differential to 4.5V. When current limit protection resistor is used, as in *Figure 14*, the maximum output current is limited by power dissipation of the 2N3772 (150W at 25°C). During normal operation this is $(V_{IN} - V_{OUT})\ I_{OUT}$ (W), but it increases to $V_{IN}\ I_{SC}$ (W) under short circuit conditions. The short circuit output current is then:

$$I_{SC} = \frac{P_{MAX}\ (T_C = 25°C)}{V_{IN}}$$

$$= \frac{150W}{20V\ (min)} = 7.5A\ max.$$

I_L could be increased to 10A or more only if $I_{SC} < I_L$. A foldback current limit circuit will accomplish this. The typical load regulation is 40 mV from no load to a full load. (T_j = 25°C, pulsed load with 20 ms t_{ON} and 250 ms t_{OFF}).

FOLDBACK CURRENT LIMITING

In many regulator applications, the normal operation power dissipation in the pass device can easily be multiplied by a factor of ten or more when the output is shorted. This may destroy the pass device, and possibly the regulator, unless the heat sink is oversized to handle this fault condition. A foldback current limiting circuit reduces short circuit output current to a fraction of the full load output current thus avoiding the need for larger heat sink. *Figure 15* shows a foldback current limiting circuit on both positive and negative regulators.

The foldback current limiting, a fraction of the output voltage must be used to oppose the voltage across the current limit sense resistor. Current limiting does not occur until the voltage across the sense resistor is higher than this opposing voltage by the amount shown in *Figure 11*. When the output is grounded, the opposing voltage is no longer present so current limiting occurs at a lower level. This is accomplished in *Figure 15* by using a programmable current source to give a constant voltage drop across R5 for the negative regulator, and by a simple resistor divider for the positive regulator. The reason for the difference between the two is that the negative regulator current limiting circuit is located between the output pass transistor and the unregulated input while the positive regulator current limiter is between the output pass transistor and the regulated output.

The operation of the positive foldback circuit is similar to that described in NSC application note AN-23. A voltage divider R1 and R2 from V_E to ground creates a fixed voltage drop across R1 opposite in polarity to the drop across $R_{CL}+$. When the load current increases to the point where the drop across $R_{CL}+$ is equal to the drop across R1 plus the current limit sense voltage given in *Figure 11*, the positive regulator will begin to current limit. As the positive output begins to drop, the voltage across R1 will also decrease so that it now requires less load current to produce the cur-

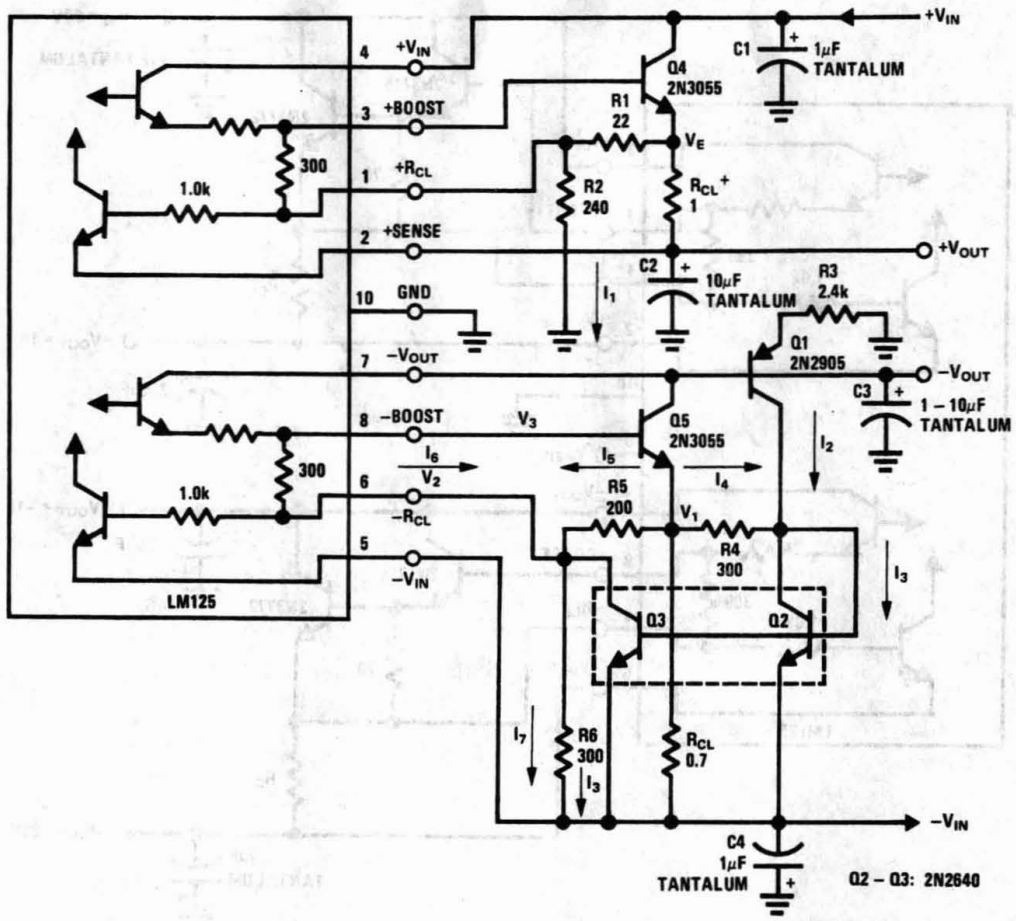

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FIGURE 15. Foldback Current Limiting Circuit

rent limit sense voltage. With the regulator output fully shorted to ground ($+V_{OUT} = 0$) the current limit will be set by the value of $+R_{CL}$ alone.

If $$\frac{I_{FB}}{I_{SC}} \leq 5$$

then the following equations can be used for calculating the positive regulator foldback current limiting resistors.

$$R_{CL}{}^{+} = \frac{V_{SENSE}}{I_{SC}} \quad (1)$$

where V_{SENSE} is from *Figure 11*.

At the maximum load current foldback point:

$$V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+} \quad (2)$$

$$V_{R1} = V_{RCL}{}^{+} - V_{SENSE} \quad (3)$$

$$V_{R1} = I_{FB}\, R_{CL}{}^{+} - V_{SENSE} \quad (4)$$

Then

$$R1 = \frac{V_{R1}}{I_1} \quad (5)$$

and

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} \quad (6)$$

The only point of caution is to ensure that the total current (I_1) through R2 is much greater than the current contribution from the internal 300Ω resistor. This can be checked by:

$$\frac{I_{FB}\, R_{CL}{}^{+}}{300} << I_1 \quad (7)$$

Note: The current from the internal 300Ω resistor is $V_{3\text{-}1}/300\Omega$, but $V_{3\text{-}1} = V_{BE} + V_{RCL} - V_{SENSE}{}^{+}$ assuming $V_{BE} \approx V_{SENSE}{}^{+}$ at the foldback point, $V_{3\text{-}1} \approx V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+}$.

Design example: 2 amp regulator LM125 positive foldback current limiting (see *Figure 15*).

Given:

$$I_{FOLDBACK} = 2.0A$$

$$I_{SHORT\text{-}CIRCUIT} = 500\ mA$$

$$V_{SENSE}\ (\text{See } \textit{Figure 11})$$

$$+V_{IN} = 25V$$

$$+V_{OUT} = 15V$$

$$\beta_{PASS\ DEVICE} = 70$$

$$\theta_{JA} = 150°C/W$$

$$T_A = 50°C$$

With a beta of 70 in the pass device and a maximum output current of 2.0A the regulator must deliver:

$$\frac{2A}{\beta} = \frac{2A}{70} = 29\ mA$$

The LM125 power dissipation will be calculated ignoring any negative output current for this example.

$$P_{LM125} = (V_{IN} - V_{OUT})\, I_{OUT}$$

$$= (25 - 15)\, 29\ mA$$

$$= 290\ mW$$

$$T_{RISE} @ \theta_{JA} = 150°C/W = 150°C \times 0.29 = 44°C$$

$$T_J = T_A + T_{RISE} = 50°C + 44°C = 94°C$$

From *Figure 11*:

$$V_{SENSE} @ (T_J = 94°C) = 520\ mW$$

From equation (1)

$$R_{CL}{}^{+} = \frac{V_{SENSE}}{I_{SC}} = \frac{520\ mV}{500\ mA} \cong 1\Omega$$

From equation (2)

$$V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+} = (2A)(1\Omega) = 2V$$

From equation (3)

$$V_{R1} = V_{RCL}{}^{+} - V_{SENSE}$$

$$V_{R1} = 2V - 520\ mV = 1.480V$$

A value for I_1 can now be found from equation (7)

$$\frac{I_{FB}\, R_{CL}{}^{+}}{300} = \frac{2A \times 1\Omega}{300\Omega} = 6.6\ mA$$

So set $I_1 = 10 \times 6.6\ mA = 66\ mA$

From equations (5) and (6)

$$R1 = \frac{V_{R1}}{I_1} = \frac{1.480V}{66\ mA} \cong 22\Omega$$

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} = \frac{15 + 0.520}{66\ mA} \cong 240\Omega$$

The foldback limiting characteristics are shown in *Figure 16* for the values calculated above at various operating temperatures.

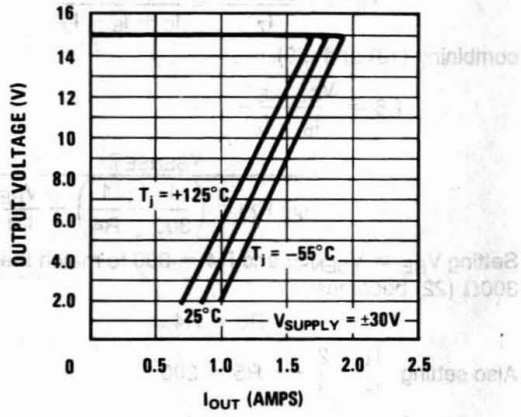

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FIGURE 16. Positive Regulator Foldback Current Limiting Characteristics

The negative regulator foldback current limiting works essentially the same way as the positive side. Q1 forces a constant current, I_2, determined by $-V_{OUT}$ and R3, through Q2. Transistors Q2 and Q3 are matched so a current identical to I_3 will flow through Q3. With the output short-circuited ($-V_{OUT} = 0$), Q1 will be OFF, setting $I_2 = 0$. The load current will be limited when V_1 increases sufficiently due to load current to make V_2 higher than $-V_{IN}$ by the current limit sense voltage.

The short circuit current is:

$$I_{SC} \cong \frac{V_{SENSE}}{R_{CL}{}^{-}} \tag{8}$$

For calculating the maximum full load current with the output still in regulation, current I_2

$$I_2 = \frac{V_{OUT} - V_{BEQ1}}{R3} \tag{9}$$

At the point of maximum load current, I_{FB}, where the regulator should start folding back:

$$V_1 = -V_{IN} + I_{FB}\, R_{CL}{}^{-} \tag{10}$$

and

$$V_2 = -V_{IN} + V_{SENSE} \tag{11}$$

The current through Q2 (and Q3) will have increased from I_2 by the amount of I_4 due to the voltage V_1 increasing above its no-load quiescent value. Since the voltage across Q2 is simply the diode drop of a base-emitter junction:

$$I_4 = \frac{[V_1 - (-V_{IN})] - V_{BE}}{R4}$$

Substituting in equation (10) gives:

$$I_4 = \frac{I_{FB}\, R_{CL}{}^{-} - V_{BE}}{R4} = \frac{I_{FB}\, R_{CL}{}^{-} - V_{BE}}{300\Omega} \tag{12}$$

The current through Q2 is now

$$I_3 = I_2 + I_4 \tag{13}$$

and the current through Q3 is:

$$I_3 = I_5 + I_6 - I_7 \tag{14}$$

The drop across R5 is found from:

$$V_1 - V_2 = (-V_{IN} + I_{FB}\, R_{CL}{}^{-}) - [V_{SENSE} + (-V_{IN})];$$

simplifying,

$$V_1 - V_2 = I_{FB}\, R_{CL}{}^{-} - V_{SENSE} \tag{15}$$

Since V_{SENSE} is the base to emitter voltage drop of the internal limiter transistor, the V_{SENSE} in equation (15) very nearly equals the V_{BE} in equation (12). Therefore the drop across R5 approximately equals the drop across R4. The current through R5, I_5, can now be determined as:

$$I_5 = \frac{I_{FB}\, R_{CL}{}^{-} - V_{SENSE}}{R5} \tag{16}$$

Summing the currents through Q3 is now possible assuming the base-emitter drop of the 2N3055 pass device can be given by $V_{BE} \approx V_{SENSE}$:

$$I_6 = \frac{V_3 - V_2}{300} \tag{17}$$

where $V_3 = V_1 + V_{BE} \approx V_1 + V_{SENSE}$

$$I_6 = \frac{V_1 + V_{SENSE} - V_2}{300}$$

Substituting in equation (15)

$$I_6 = \frac{I_{FB}\, R_{CL}{}^{-}}{300} \tag{18}$$

$$I_7 = \frac{V_2 - (-V_{IN})}{R6} = \frac{V_{SENSE}}{R6}$$

Equating equation (13) with equation (14) and inserting resistor values shown in *Figure 15*,

$$I_2 + I_4 = I_5 + I_6 - I_7$$

$$I_2 + \frac{I_{FB}\, R_{CL}^- - V_{SENSE}}{300} = I_5 + \frac{I_{FB}\, R_{CL}^-}{300} - \frac{V_{SENSE}}{300} \quad (19)$$

Canceling, we find:

$$I_2 = I_5 \quad (20)$$

This is the key to the negative foldback circuit. Current source Q1 forces current I_2 to flow through resistor R5. The voltage drop across R5 opposes the normal current limit sense voltage so that the regulator will not current limit until the drop across R_{CL}^- due to load current, equals the controlled drop across R5 plus V_{SENSE} (given in *Figure 11*). This can be written as:

$$I_{FB} = \frac{V_{SENSE} + I_2\, R5}{R_{CL}^-} \quad (21)$$

$$I_{FB} = \frac{V_{SENSE} + 200\, I_2}{R_{CL}^-}$$

A design example is now offered:

Given:

$$I_{FOLDBACK} = 2.5A$$

$$I_{SHORT\text{-}CIRCUIT} = 750\ mA$$

V_{SENSE} (See *Figure 11*)

$$-V_{IN} = 25V$$

$$-V_{OUT} = -15V$$

$$\beta_{PASS\ DEVICE} = 90$$

$$\theta_{JA} = 150°C/W$$

$$T_A = 25°C$$

The same calculations are used here to figure V_{SENSE} as with the positive regulator foldback example maximum regulator output current is calculated from:

$$I_{OUT} = \frac{2.5A}{90} = 28\ mA$$

$$P_{LM125} = (V_{IN} - V_O)\, I_{OUT} = 10V \times 28\ mA = 280\ mW$$

$$T_{RISE} = 150°C/W \times 0.28W = 42°C$$

$$T_J = T_A + T_{RISE} = 25°C + 42°C = 67°C$$

From *Figure 11*:

$$V_{SENSE} = 500\ mV$$

From equation (8):

$$R_{CL}^- = \frac{500\ mV}{750\ mA} = 0.68\Omega$$

From equation (21):

$$I_2 = \frac{I_{FB}\, R_{CL}^- - V_{SENSE}}{200\Omega} = 6.0\ mA$$

From equation (9):

$$R3 = \frac{V_{OUT} - V_{BEQ1}}{I_2}$$

$$R3 \cong \frac{14.3}{6.0\ mA} = 2.4k$$

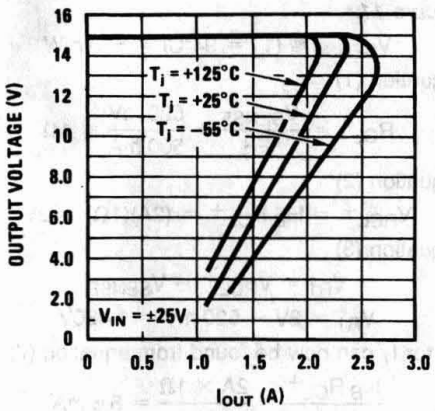

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FIGURE 17. Negative Regulator Foldback Current Limiting Characteristics

Figure 16 and *17* show the measured foldback characteristics for the values derived in the design examples. The value of R5 is set low so that the magnitude of I_5 for foldback is greater than I_4 through I_6. This reduces the foldback point sensitivity to the TC of the internal 300Ω resistor and any mismatch in the TC of Q2, Q3 or the pass device.

R6 can be computed from equation (18):

$$R6 = \frac{V_{SENSE}^-}{I_7} = \frac{V_{SENSE}^-}{I_5 + I_6 - I_3}$$

combining (13) and (20).

$$R6 = \frac{V_{SENSE}^-}{I_6 - I_4} = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left(\frac{1}{300} - \frac{1}{R4}\right) + \frac{V_{BE}}{R4}} \quad (22)$$

Setting $V_{BE} \cong V_{SENSE}$ and R4 = 300 to match the internal 300Ω (22) becomes:

$$R6 = R4$$

Also setting $\frac{I_4}{I_5} = \frac{2}{3} \rightarrow R5 = 200$

A 10 AMP REGULATOR

Figure 18 illustrates the complete schematic of a 10A regulator with foldback current limiting. The design approach is similar to that of the 2A regulator. However, in this design, the current contribution from the internal 300Ω resistor is greater due to the 2 V_{BE} drop across the Darlington pair. Expression (7) becomes:

$$\frac{I_{FB}\, R_{CL}^+ + V_{BE}}{300} << I_1\ ; \quad (23)$$

and, for the negative regulator, expression (22) becomes:

$$R6 = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left[\frac{1}{300} - \frac{1}{R4}\right] + V_{BE}\left[\frac{1}{300} + \frac{1}{R4}\right]} \quad (24)$$

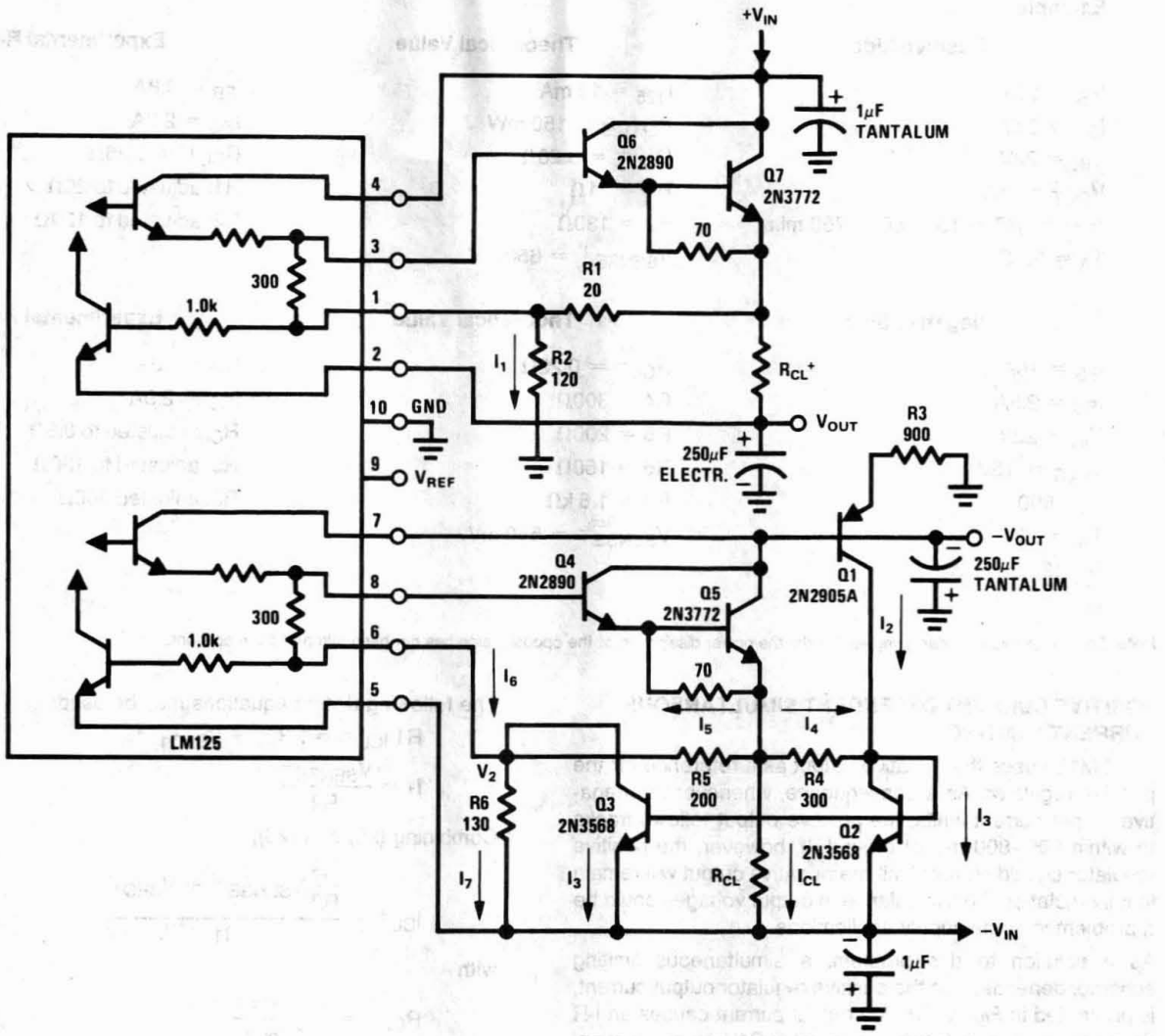

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FIGURE 18. 10A Regulator with Foldback Current Limiting

The disagreement between the theoretical and experimental values for the negative regulator is not alarming. In fact R_{CL} was based on equation (8), which is correct if for zero V_{OUT}, I_5 is zero as well. This implies:

$$V_{SENSE}\ (\text{at SC}) = \frac{V_{BEQ4} + V_{BEQ5}}{2}\ (\text{at SC})$$

which is a first order approximation.

Figure 19 illustrates the power dissipation in the external power transistor for both sides. Maximum power dissipation occurs between full load and short circuit so the heat sink for the 2N3772 must be designed accordingly, remembering that the 2N3772 must be derated according to 0.86W/°C above 25°C. This corresponds to a thermal resistance junction to case of 1.17°C/W.

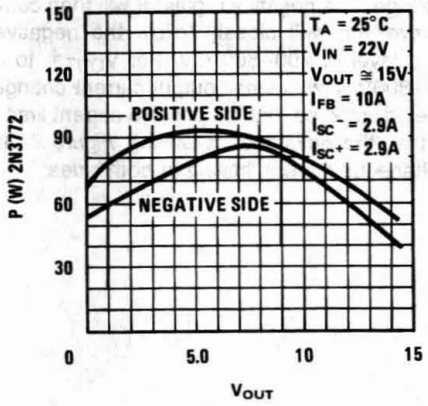

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FIGURE 19. Power Dissipation in the External Pass Transistor (Q5, Q7)

Example

Positive Side	Theoretical Value	Experimental Results
$I_{FB} = 10A$	$I_{125} = 13\ mA$	$I_{FB} = 9.8A$
$I_{SC} = 2.5A$	$P_{LM125} = 150\ mW$	$I_{SC} = 2.9A$
$V_{IN} = 22V$	$R_{CL}{}^{+} = 0.26\Omega$	$R_{CL}{}^{+} = 0.26\Omega$
$V_{OUT} = 15V$	$R1 = 21\Omega$	R1: adjusted to 20Ω
$\beta = \beta 1\ \beta 2 = 15 \times 50 = 750$ min	$R2 = 130\Omega$	R2: adjusted to 120Ω
$T_A = 25°C$	$V_{SENSE}{}^{+} = 650\ mV$	

Negative Side	Theoretical Value	Experimental Results
$I_{FB} = 10A$	$R_{CL}{}^{-} = 0.22\Omega$	$I_{FB} = 10A$
$I_{SC} = 2.5A$	$R4 = 300\Omega$	$I_{SC} = 2.9A$
$V_{IN} = 22V$	$R5 = 200\Omega$	R_{CL}: adjusted to 0.3Ω
$V_{OUT} = 15V$	$R6 = 150\Omega$	R6: adjusted to 130Ω
$\beta = 800$	$R3 = 1.6\ k\Omega$	R3: adjusted 900Ω
$T_A = 25°$	$V_{SENSE}{}^{-} = 550\ mV$	
$\frac{I_4}{I_5} = \frac{2}{3}$		

Note: For this example, in designing each side, the power dissipation of the opposite side has not been taken into the account.

POSITIVE CURRENT DEPENDENT SIMULTANEOUS CURRENT LIMITING

The LM125 uses the negative output as a reference for the positive regulator. As a consequence, whenever the negative output current limits, the positive output follows tracks to within 200–800 mV of ground. If, however, the positive regulator should current limit the negative output will remain in full regulation. This imbalance in output voltages could be a problem in some supply applications.

As a solution to this problem, a simultaneous limiting scheme, dependent on the positive regulator output current, is presented in *Figure 20*. The output current causes an I-R drop across R1 which brings transistor Q1 into conduction. As the positive load current increases I_1 increases until the voltage drop across R2 equals the negative current limit sense voltage. The negative regulator will then current limit, and positive side will closely follow the negative output down to a level of 700–800 mV. For $V_{OUT}{}^{+}$ to drop the final 700–800 mV with small output current change, $R_{CL}{}^{+}$ should be adjusted so that the positive current limit is slightly larger than the simultaneous limiting. *Figure 21* illustrates the simultaneous current limiting of both sides.

The following design equations may be used:

$$R1\ I_{CL}{}^{+} = R3\ I_1 + V_{BEQ1} \tag{25}$$

$$I_1 = \frac{V_{SENSE}{}^{-}}{R2} \tag{26}$$

Combining (25) and (26),

$$I_{CL}{}^{+} = \frac{\frac{R3}{R2} V_{SENSE}{}^{-} + V_{BEQ1}}{R1} \tag{27}$$

with

$$R_{CL}{}^{+} = \frac{V_{SENSE}{}^{+}}{1.1\ I_{CL}{}^{+}} \tag{28}$$

The negative current limit (independent of $I_{CL}{}^{+}$) can be set at any desired level.

$$I_{CL}{}^{-} = \frac{V_{SENSE}{}^{-} + V_{DIODE}}{R_{CL}{}^{-}} \tag{29}$$

Transistor Q2 turns off the negative pass transistor during simultaneous current limiting.

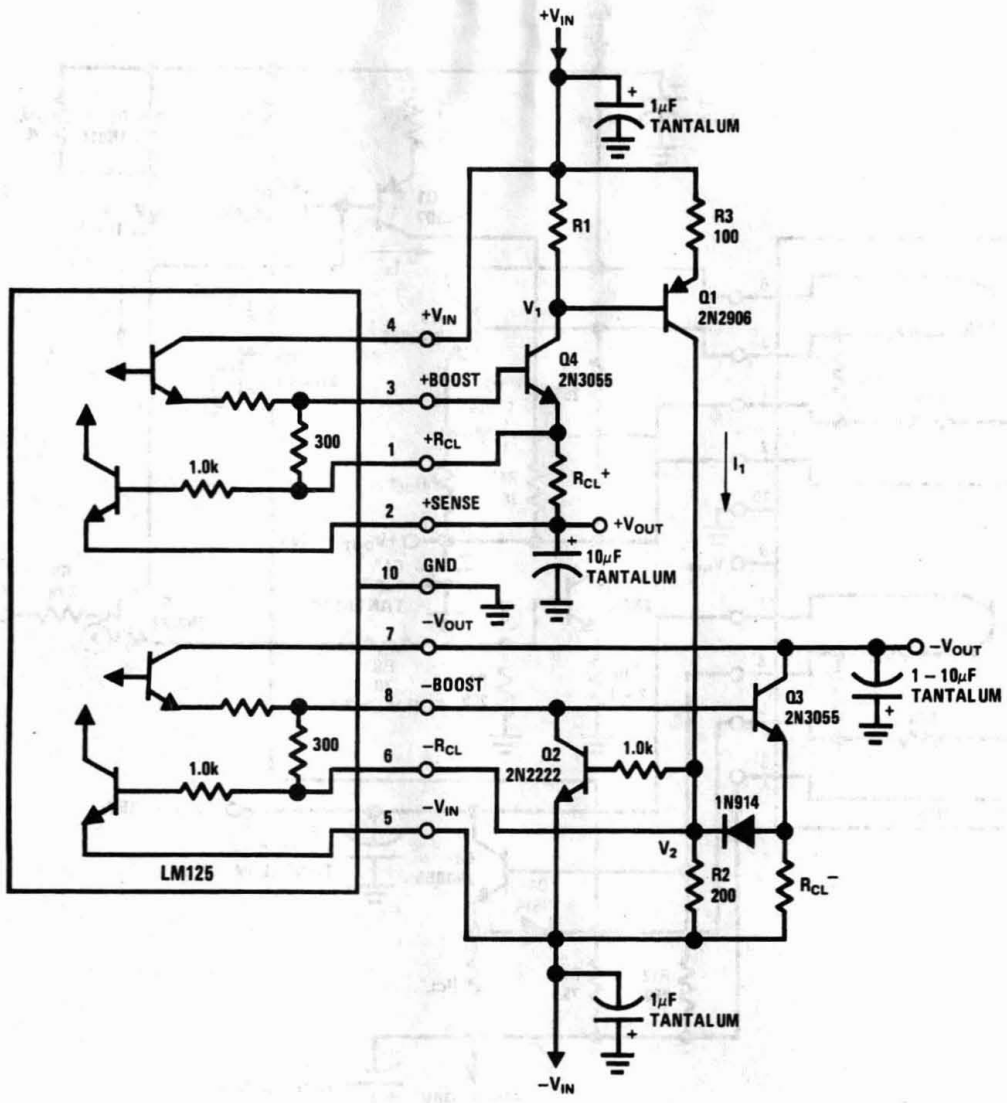

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FIGURE 20. Positive Current Dependent Simultaneous Current Limiting

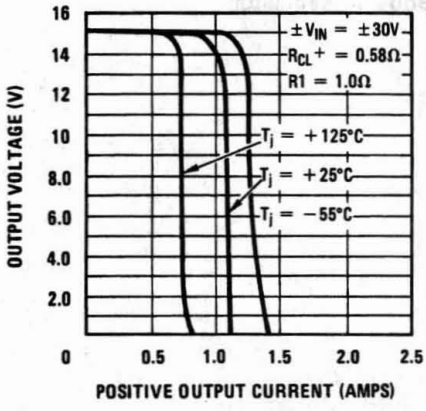

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FIGURE 21. Positive Current Dependent Simultaneous Shutdown

ELECTRONIC SHUTDOWN

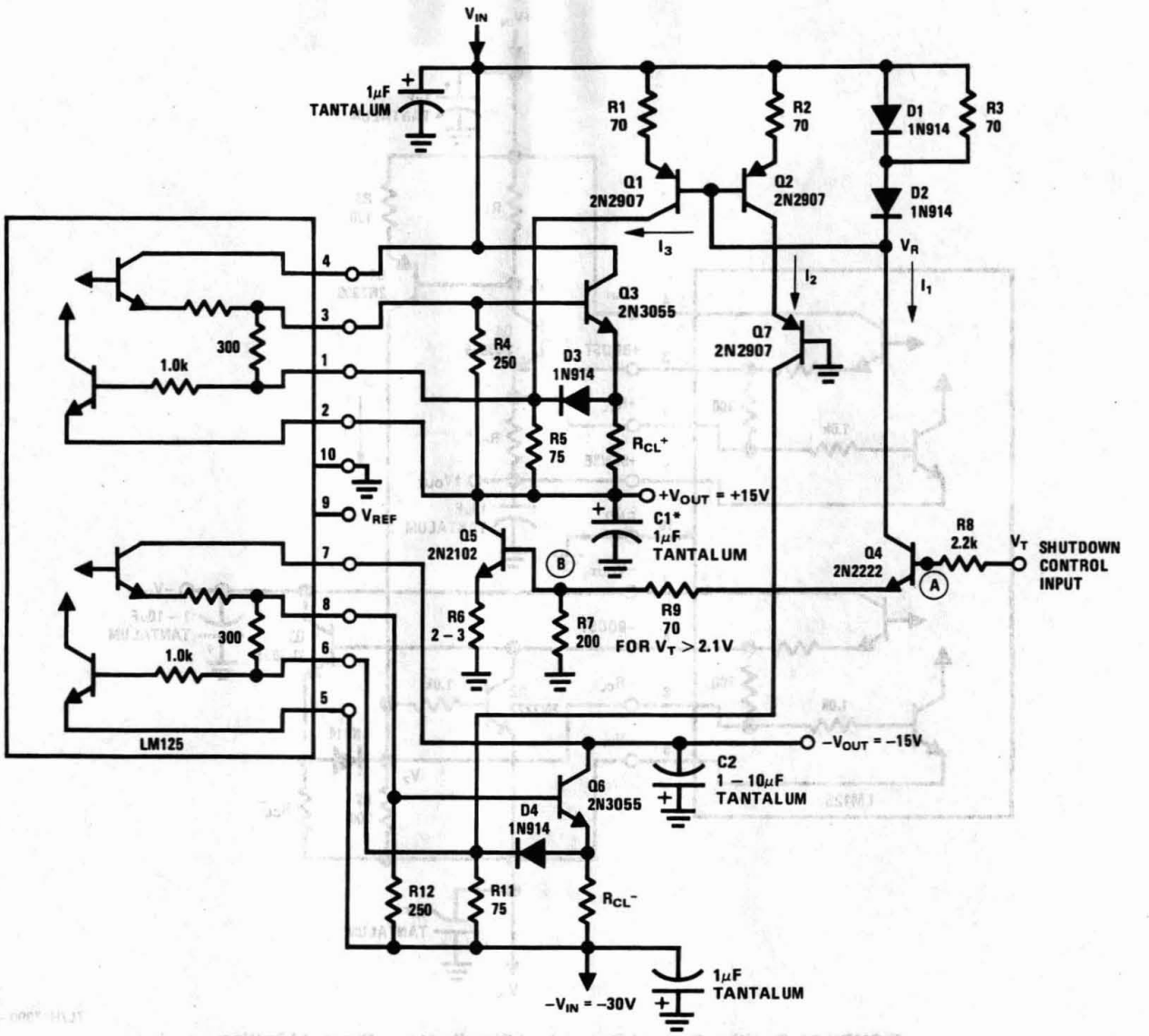
In some regulated supply applications it is desirable to shutdown the regulated outputs ($\pm V_O = 0$) without having to shutdown the unregulated inputs (which may be powering additional equipment). Various shutdown methods may be used. The simplest is to insert a relay, a saturated bipolar device, or some other type switch in series with either the regulator inputs or outputs. The switch must be able to open and close under maximum load current which, may be several amps.

As an alternate solution, the internal reference voltage of the regulator may be shorted to ground. This will force the positive and negative outputs to approximately +700 mV and +300 mV respectively. Both outputs are fully active so the full output current can still be supplied into a low impedance load. If this is unacceptable, another solution must be found.

The circuit in *Figure 22* provides complete electronic shutdown of both regulators. The shutdown control signal is TTL compatible but by adjusting R8 and R9 the regulator may be shutdown at any desired level above 2 V_{BE}, calculated as follows:

$$V_T \cong \left[\frac{R8}{R3\ \beta\ Q4} + \frac{R9}{R3}\right] V_{BE} + 2\,V_{BE} \qquad (30)$$

Positive and negative shutdown operations are similar. When a shutdown signal V_T is applied, Q4 draws current through R3 and D2 establishing a voltage V_R which starts



*For higher values of C1 increase R6 to limit the peak current through Q5 to a safe value.

TL/H/7390–25

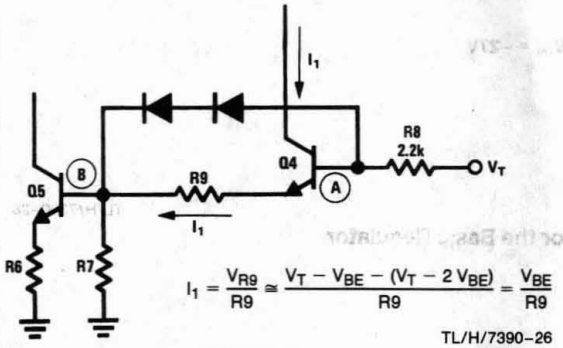
FIGURE 22. Electronic Shutdown for the Boosted Regulator

the current sources Q1 and Q2. Assuming that Q1 and Q2 are matched, and making R1 = R2 = R3, the currents I_1, I_2, I_3 are equal and both sides of the regulator shutdown simultaneously.

The current I_3 creates a drop across R5, which equals or exceeds the limit sense voltage of the positive regulator, causing it to shutdown. Since I_3 has no path to ground except through the load, a fixed load is provided by Q5, which is turned on by the variable current source Q4, C1 also discharges through Q5 and current limiting resistor R6. Resistor R4 prevents Q3 turn on during shutdown, which could otherwise occur due to the drop across R5 plus the internal 300Ω resistor. Diode D3 prevents I_3 from being shunted through R_{CL}.

C2 discharges through the load. Q7 shares the total supply voltage with Q2, thus limiting power dissipation of Q2. Another power dissipation problem may occur when the design is done for V_T = 2.0V for example, and V_T is increased above the preset threshold value. I_1 is increased and Q4 has to dissipate $(V_{IN} - 3\ V_{BE} - V_T)\ I_1$ (W). The simplest solution is to increase R8. If this is insufficient, a set of diodes may be added between nodes A and B to clamp, I_1 to a reasonable value. This is illustrated in *Figure 23*:

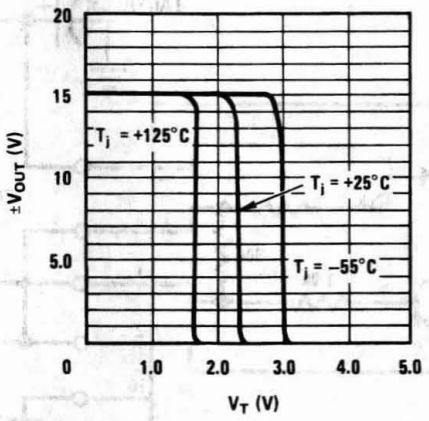
$$I_1 = \frac{V_{R9}}{R9} \cong \frac{V_T - V_{BE} - [V_T - 2\,V_{BE}]}{R9} = \frac{V_{BE}}{R9}$$



TL/H/7390–26

FIGURE 23

So I_1 is made independent of V_T and by setting a minimum value of 10 mA (R9 = 70Ω). The regulator will shutdown at any desired level above 3 V_{BE}, without overheating transistor Q4. Also using *Figure 23* the diode D1 in *Figure 22* may be omitted. The shutdown characteristics of *Figure 22* are shown in *Figure 24*.



TL/H/7390–27

FIGURE 24. Electronic Shutdown Characteristics

The normal current limiting current is set by equation (31)

$$I_{CL} = \frac{V_{SENSE} + V_{DIODE}}{R_{CL}} \qquad (31)$$

The same approach is used with the unboosted regulator shown in *Figure 25*. In this case the voltage sense resistor is the internal 300Ω one. Since output capacitors are no longer required Q3 is just used as a current sink and its emitter load has been removed.

POWER DISSIPATION

The power dissipation of the LM125 is:

$$P_d = (V_{IN}^+ - V_{OUT}^+)\, I_{OUT}^+ + (V_{IN}^- - V_{OUT}^-)\, I_{OUT}^- + V_{IN}^+ I_S^+ + V_{IN}^- I_S^-$$

where I_S is the standby current.

Ex: ±1A regulator using 2N3055 pass transistors. Assuming a β = 100, and ±25V supply,

$$P_d = 400\ \text{mW}.$$

The temperature rise for the TO-5 package will be:

$$T_{RISE} = 0.4 \times 150°C/W = 60°C$$

Therefore the maximum ambient temperature is $T_{AMAX} = T_{jMAX} - T_{RISE} = 90°C$. If the device is to operate at T_A above 90°C then the TO-5 package must have a heat sink. T_{RISE} in this case will be:

$$T_{RISE} = P_d\,(\theta_{J\text{-}C} + \theta_{C\text{-}S} + \theta_{S\text{-}A}).$$

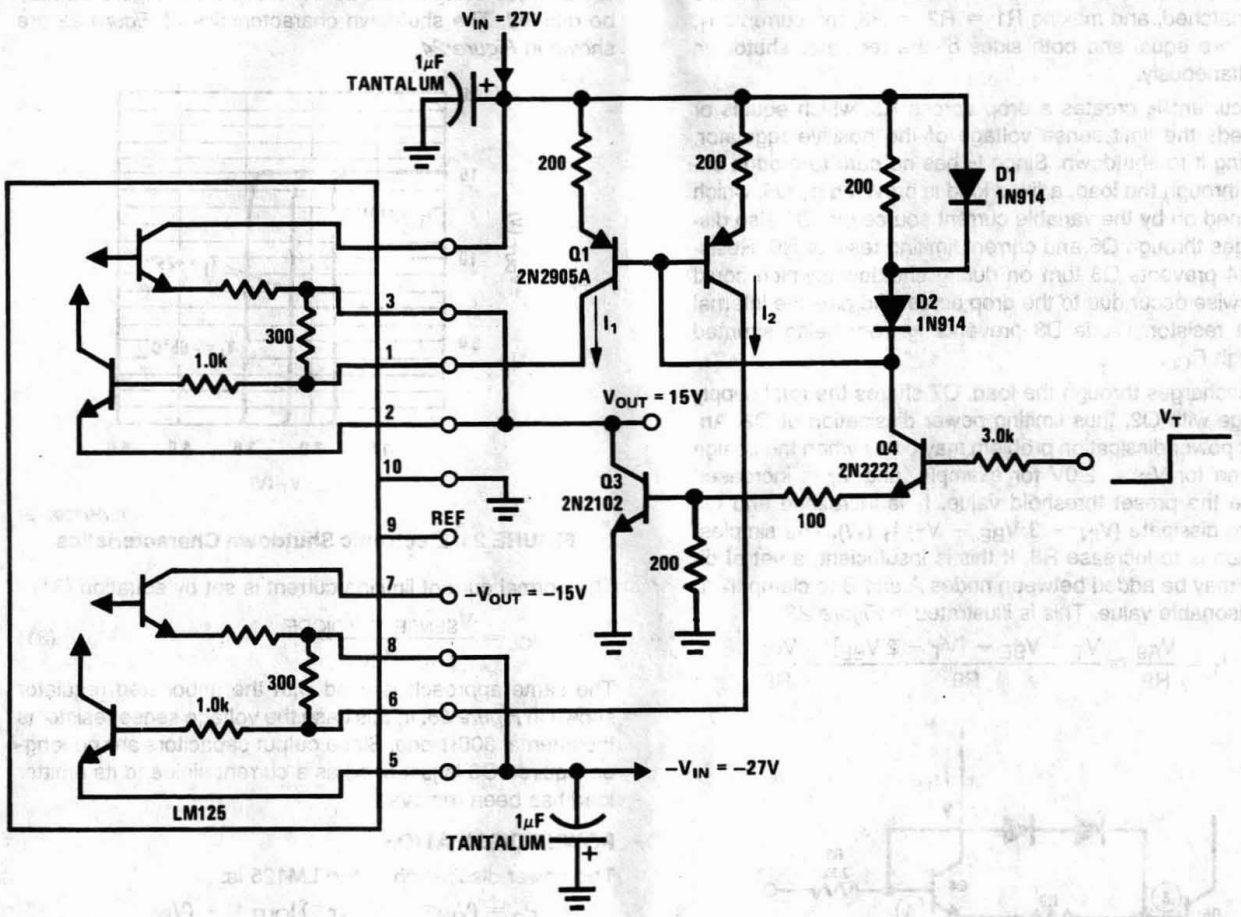


FIGURE 25. Electronic Shutdown for the Basic Regulator

Comparing the High Speed Comparators

National Semiconductor
Application Note 87
Interface
Development Group

INTRODUCTION

Several integrated circuit voltage comparators exist which were designed with high speed and complementary TTL outputs as the main objectives. The more common applications for these devices are high speed analog to digital (A to D) converters, tape and disk-file read channels, fast zero-crossing detectors, and high speed differential line receivers. This note compares the National Semiconductor devices to similar devices from other manufacturers.

The product philosophy at National was to create pin-for-pin replacement circuits that could be considered as second-sources to the other comparators, while simultaneously containing the improvements necessary to make a more optimum device for the intended usage. Optimized parameters include speed, input accuracy and impedance, supply voltage range, fanout, and reliability. The LM160/LM260/LM360 are replacement devices for the μA760, while the LM161/LM261/LM361 replace the SE/NE529. Tables I and II compare the critical parameters of the National commercial range devices to their respective counterparts.

SPEED

Throughout the universe the subject of speed must be approached with caution; the same holds true here. Speed (propagation delay time) is a function of the measurement

TABLE I. LM360/μA760C Comparison $0°C \le T_A \le +70°C$, $V^+ = +5.0V$, $V^- = -5.0V$

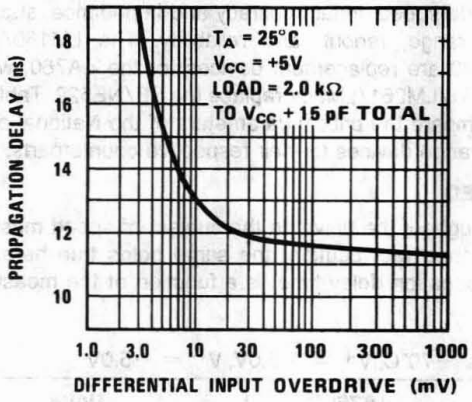
Parameter	LM360	μA760C	Units
Input Offset Voltage	5.0	6.0	mV max
Input Offset Current	3.0	7.5	μA max
Input Bias Current	20	60	μA max
Input Capacitance	4.0	8.0	pF typ
Input Impedance	17	5.0	kΩ typ @ 1 MHz 25°C
Differential Voltage Range	±5.0	±5.0	V typ
Common Mode Voltage Range	±4.0	±4.0	V typ
Gain	3.0	3.0	V/mV typ 25°
Fanout	4.0	2.0	74 Series TTL Loads
Propagation Delays:			
(1) 30 mVp-p 10 MHz Sinewave in	25	30	ns max 25°
(2) 2.0 Vp-p 10 MHz Sinewave in	20	25	ns max 25°
(3) 100 mV Step + 5.0 mV Overdrive	14	22	ns typ 25°

TABLE II. LM261/NE529 Comparison $0°C \le T_A \le +70°C$, $V^+ = +10V$, $V^- = -10V$, $V_{CC} = +5.0V$

Parameter	LM261	NE529	Units
Input Offset Voltage	3.0	10	mV max
Input Offset Current	3.0	15	μA max
Input Bias Current	20	50	μA max
Input Impedance	17	5.0	kΩ typ @ 1 MHz 25°C
Differential Voltage Range	±5.0	±5.0	V typ
Common Mode Voltage Range	±6.0	±6.0	V typ
Gain	3.0	4.0	V/mV typ 25°
Fanout	4.0	6.0	74 Series TTL Loads
Propagation Delay - 50 mV Overdrive	20	22	ns max 25°

technique. The earlier "standard" of using a 100 mV input step with 5.0 mV overdrive has given way to seemingly endless variations. To be meaningful, speed comparisons must be made with identical conditions. It is for this reason that the speed conditions specified for the National parts are the same as those of the parts replaced.

Probably the most impressive speed characteristic of the six National parts is the fact that propagation delay is essentially independent of input overdrive (*Figure 1*); a highly desirable characteristic in A to D applications. Their delay typically varies only 3 ns for overdrive variations of 5.0 mV to 500 mV, whereas the other parts have a corresponding delay variation of two to one. As can be seen in Tables I and II, the National parts have an improved maximum delay specification. Further, the 20 ns maximum delay is meaningful since it is specified with a representative load: a 2.0 kΩ resistor to +5.0V and 15 pF total load capacitance. *Figure 2* shows typical delay variation with temperature.



TL/H/7407–1

FIGURE 1. Delay vs Overdrive

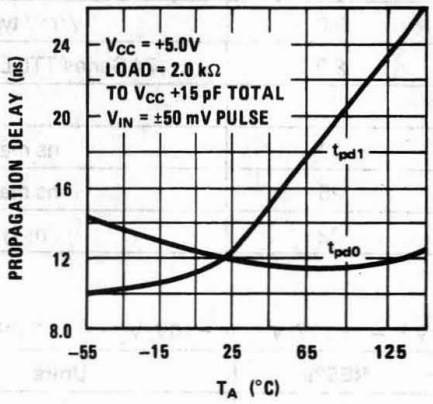


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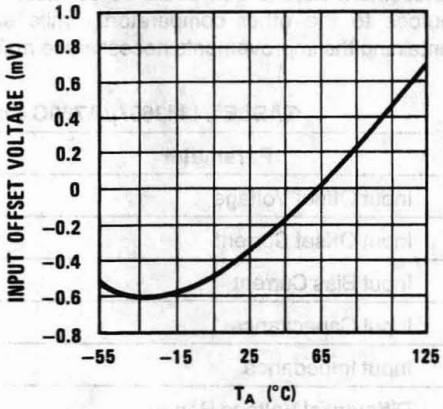
FIGURE 2. Delay vs Temperature

INPUT PARAMETERS

The A to D, level detector, and line receiver applications of these devices require good input accuracy and impedance. In all these cases the differential input voltage is relatively large, resulting in a complete switch of input bias current as the input signal traverses the reference voltage level. This effect can give rise to reduced gain and threshold inaccuracy, dependent on input source impedances and comparator input bias currents. Tables I and II show that the National parts have a substantially lower maximum bias current to ease this problem. This was done without resorting to Darlington input stages whose price is higher offset voltages and longer delay times. The lower bias currents also raise input resistance in the threshold region. Lower input capacitance and higher input resistance result in higher input impedance at high frequencies.

Even with low source impedances, input accuracy is still dependent on offset voltage. Since none of the devices under discussion has internal offset null capability, ultimate accuracy was improved by designing and specifying lower maximum offset voltage. Refer to *Figure 3* for typical offset voltage drift with temperature.

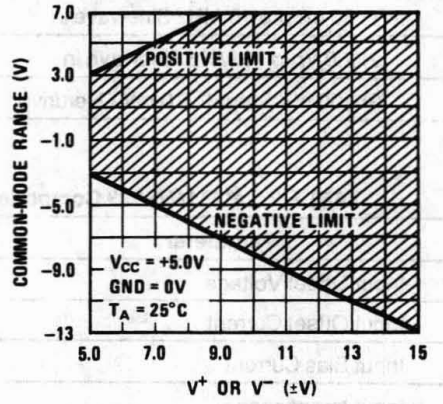


TL/H/7407–3

FIGURE 3. Offset Temperature Coefficient

OTHER PERFORMANCE AREAS

In the case of the LM160/LM260/LM360, fanout was doubled over the previous device. For the LM161/LM261/LM361, operating supply voltage range was extended to ±15V op amp supplies which are often readily available where such a comparator is used. *Figure 4* reveals the common mode range of the latter device.



TL/H/7407–4

FIGURE 4. LM161 Common Mode Range

The performance improvements previously mentioned were a result of circuit design (*Figures 5* and *6*) and device processing. Schottky clamping, which can give rise to reliability problems, was not used. Gold doping, which results in processing dependent speeds and low transistor beta, was not used. Instead a non-gold-doped process with high breakdown voltage, high beta, and high f_T ($\approx$1.5 GHz) was selected which produced remarkably consistent performance independent of normal process variation. The higher breakdown voltage allows the LM161/LM261/LM361 to operate on $\pm$15V supplies and results in lower transistor capacitance; higher beta provides lower input bias currents; and higher f_T helps reduce propagation time.

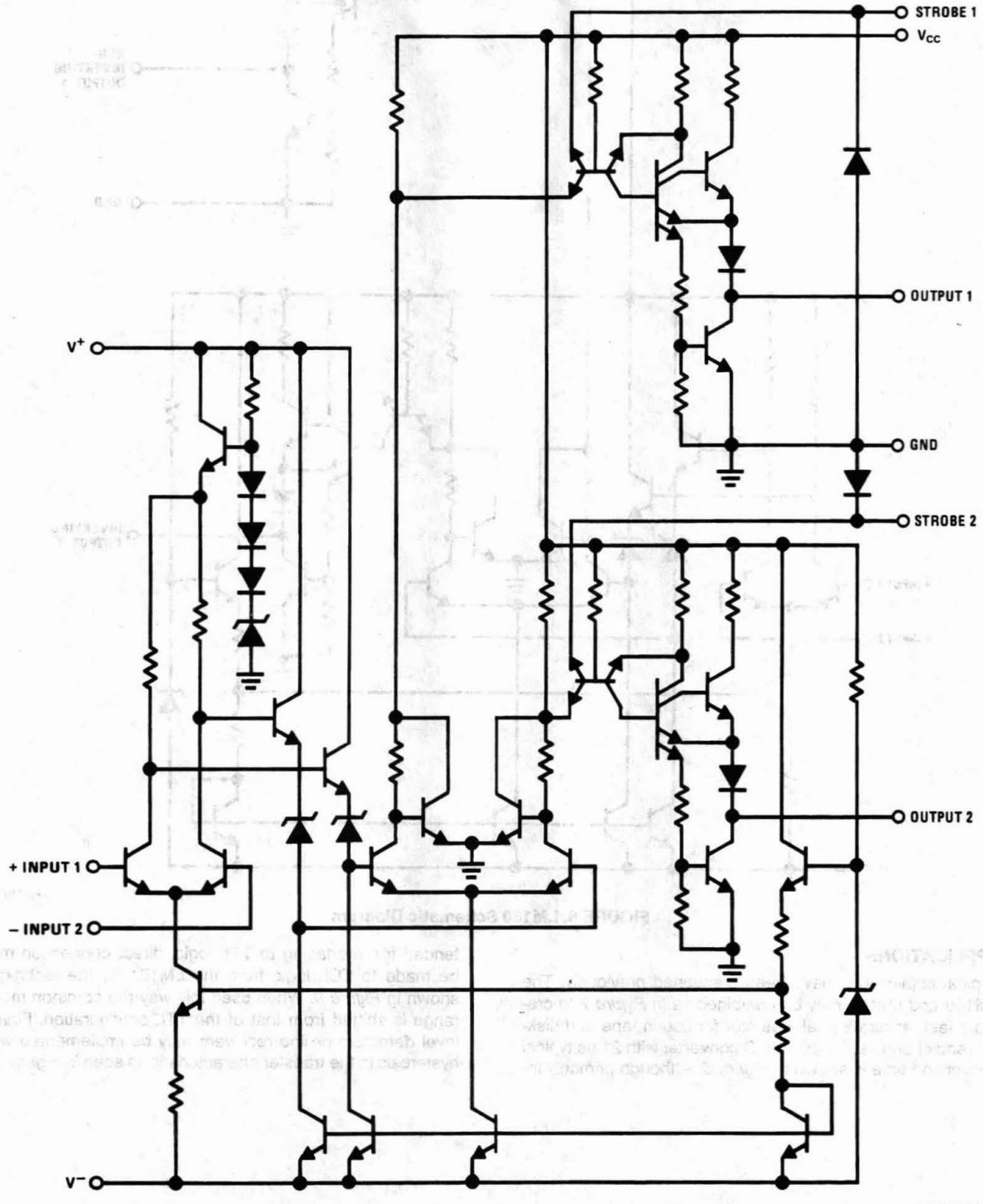


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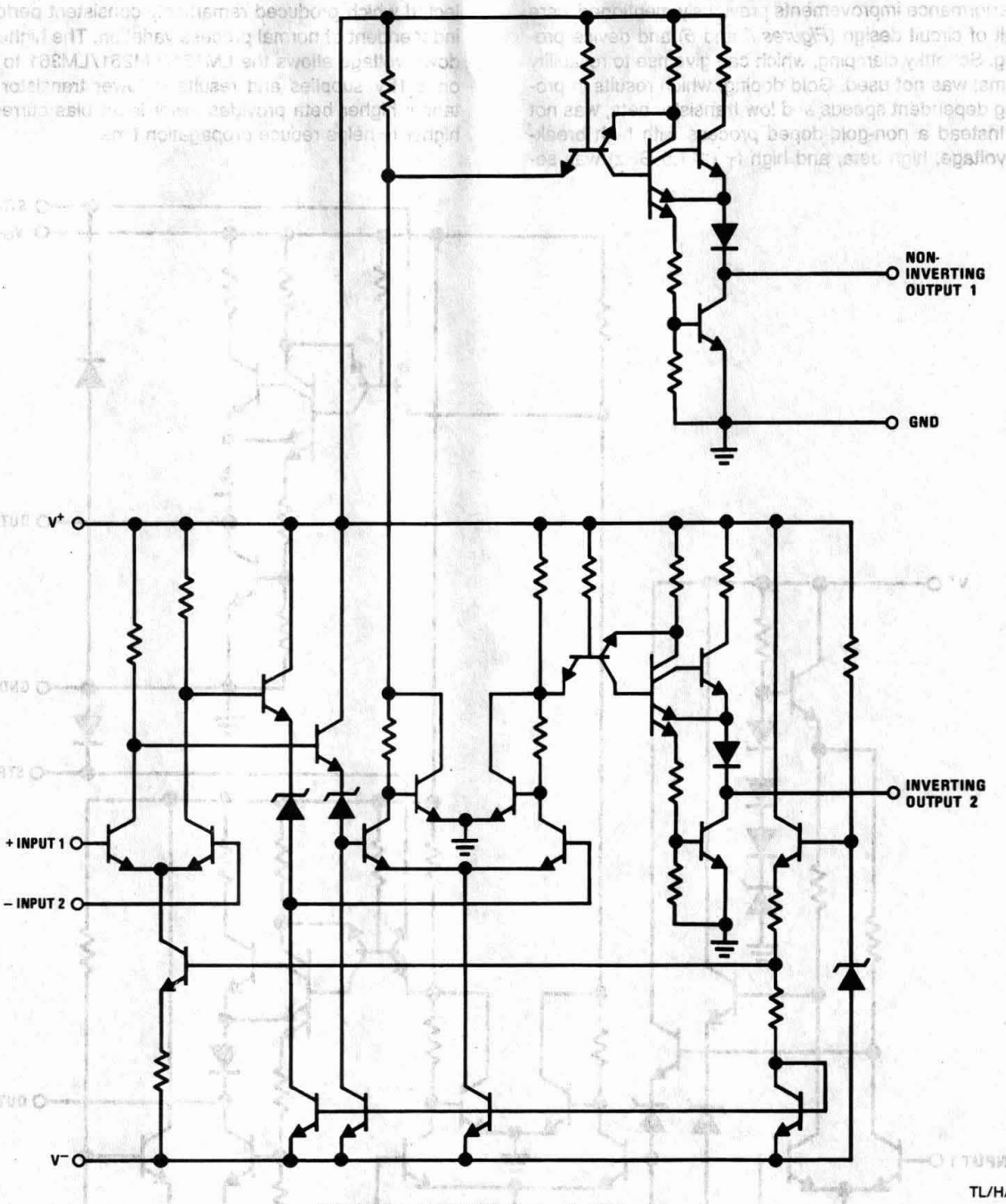
FIGURE 5. LM161 Schematic Diagram



TL/H/7407–6

FIGURE 6. LM160 Schematic Diagram

APPLICATIONS

Typical applications have been mentioned previously. The LM160 and LM161 may be combined as in *Figure 7* to create a fast, accurate peak detector for use in tape and disk-file read channels. A 3-bit A to D converter with 21 ns typical conversion time is shown in *Figure 8*. Although primarily intended for interfacing to TTL logic, direct connection may be made to ECL logic from the LM161 by the technique shown in *Figure 9*. When used this way the common mode range is shifted from that of the TTL configuration. Finally level detectors or line receivers may be implemented with hysteresis in the transfer characteristic as seen in *Figure 10*.

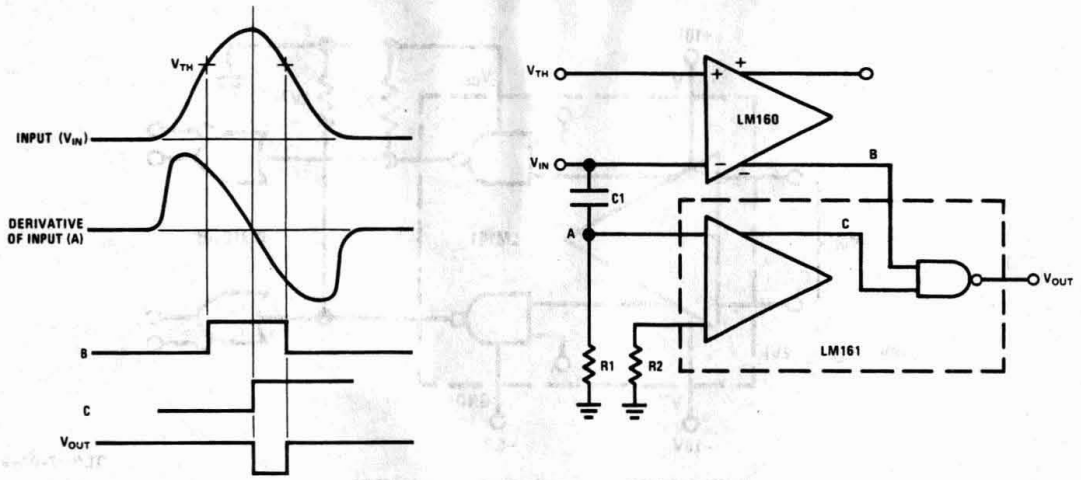


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FIGURE 7. Peak Detector

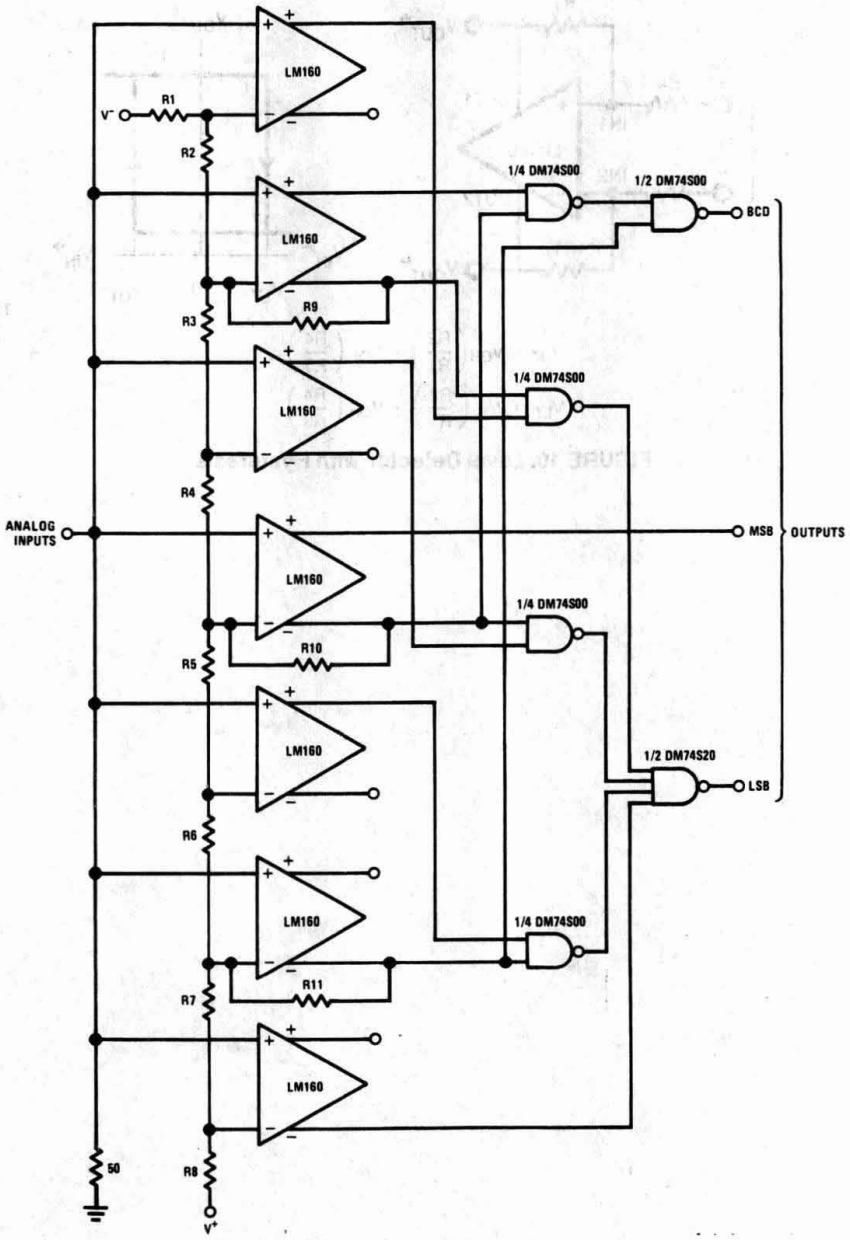

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FIGURE 8. High Speed 3-bit A to D Converter

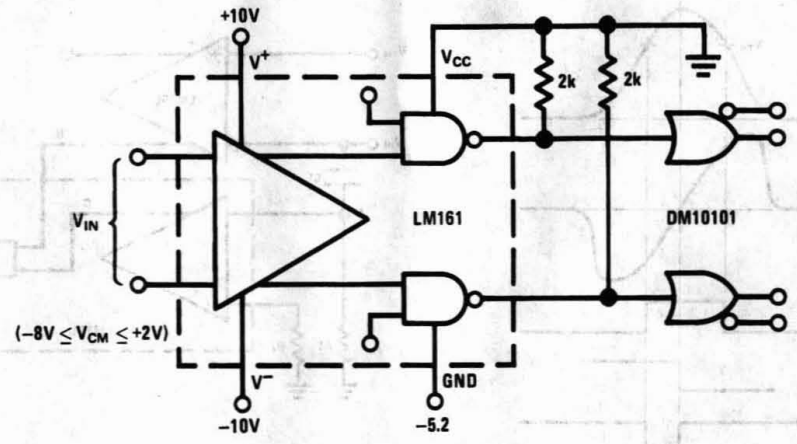

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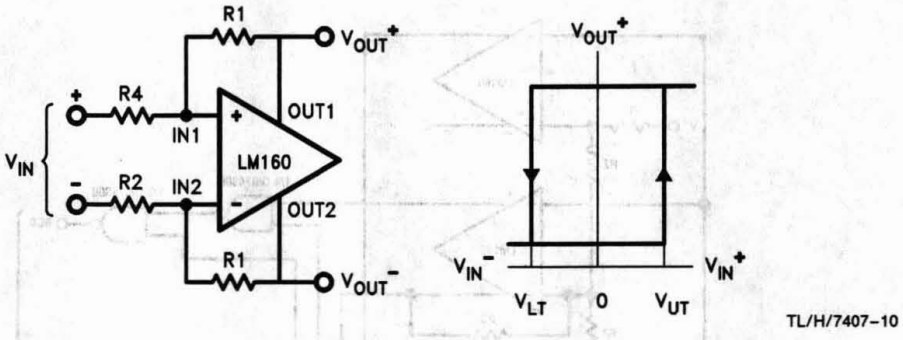
FIGURE 9. Direct Interfacing to ECL



TL/H/7407–10

$$V_{UT} = V_{OH}\left(\frac{R2}{R1}\right) - V_{OL}\left(\frac{R4}{R3}\right)$$

$$V_{LT} = V_{OL}\left(\frac{R2}{R1}\right) - V_{OH}\left(\frac{R4}{R3}\right)$$

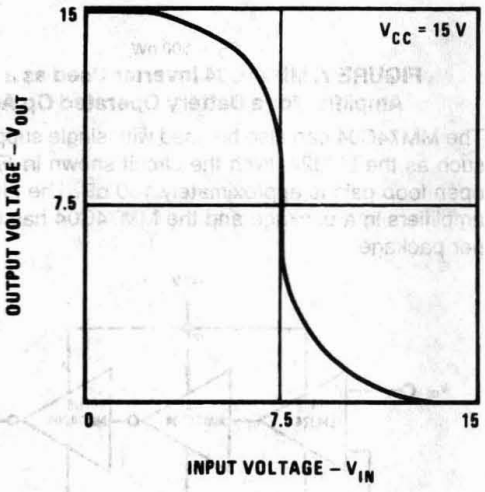
FIGURE 10. Level Detector with Hysteresis

CMOS Linear Applications

National Semiconductor
Application Note 88

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. *Figure 1* shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristics as shown in *Figure 1.*

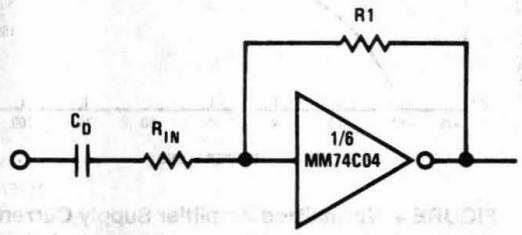


TL/F/6020–1

FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter

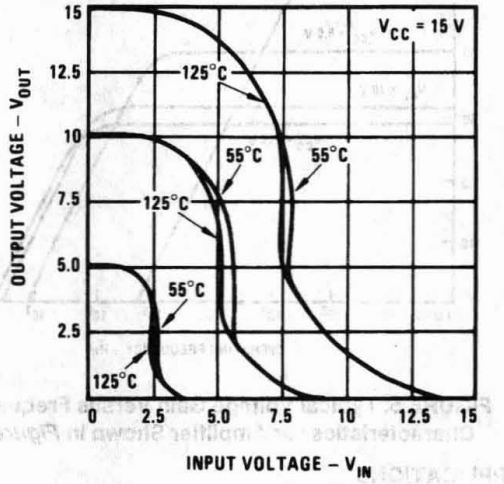
Under AC Conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. *Figure 2* shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.



TL/F/6020–2

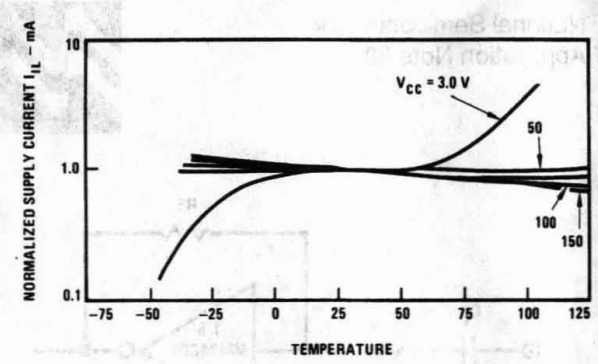
FIGURE 2. A 74CMOS Inverter Biased for Linear Mode Operation



TL/F/6020–3

FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier

Figure 3 shows typical voltage characteristics of each inverter at several values of the V_{CC}. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self-biased inverter with supply voltage is shown in *Figure 4.* When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

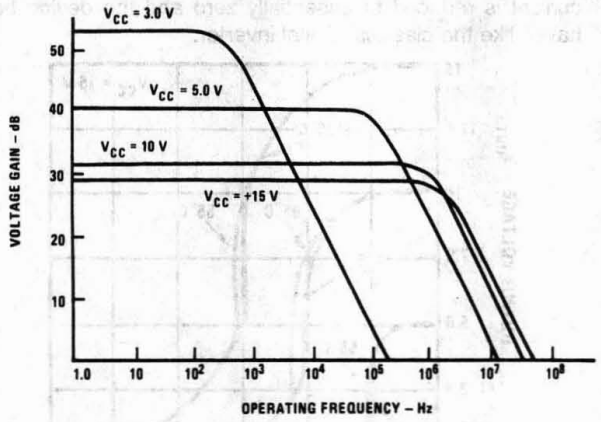


TL/F/6020–4

FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or a dual supply.



TL/F/6020–5

FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in *Figure 2*

APPLICATIONS

Cascading Amplifiers for Higher Gain

By cascading the basic amplifier block shown in *Figure 2* a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in *Figure 6*) a higher open loop gain is achieved which results in more accurate closed loop gains.

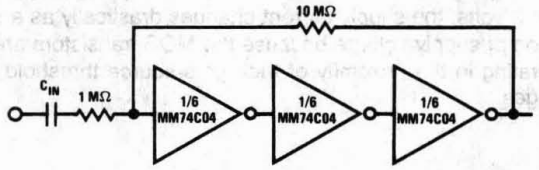


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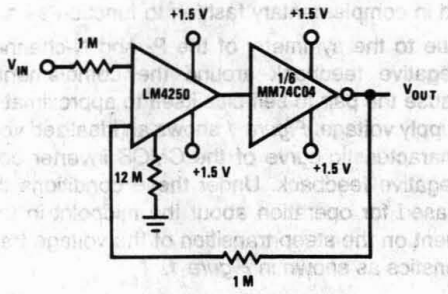
FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier

Post Amplifier for Op Amps

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in *Figure 7* is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

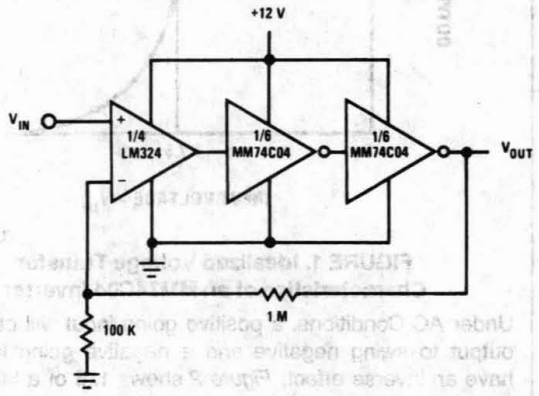


TL/F/6020–7

P_D = 500 nW

FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in *Figure 8*, the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.



TL/F/6020–8

FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA from the V_{CC} supply while the

MM74C02 will supply approximately 10 mA from the negative supply. Shown in *Figure 9* is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.

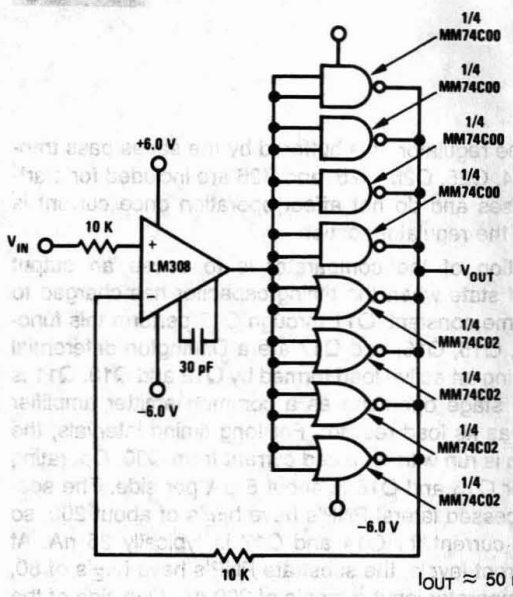


FIGURE 9. MM74C00 and MM74C02 Used as a Post Amplifier to Provide Increased Current Drive

Other Applications

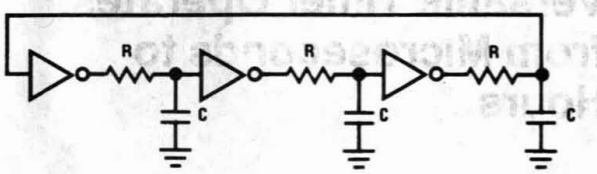
Shown in *Figure 10* is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

Conclusion

Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.

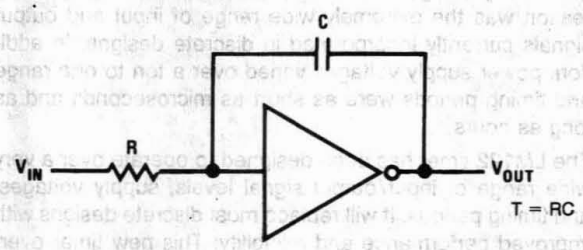
Phase Shift Oscillator Using MM74C04



$$f = \frac{1}{3.3\ RC}$$

TL/F/6020–10

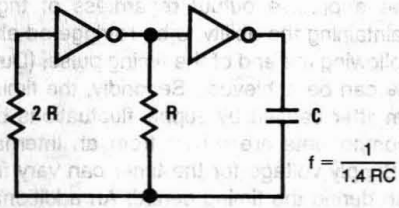
Integrator Using Any Inverting CMOS Gate



$T = RC$

TL/F/6020–11

Square Wave Oscillator



$$f = \frac{1}{1.4\ RC}$$

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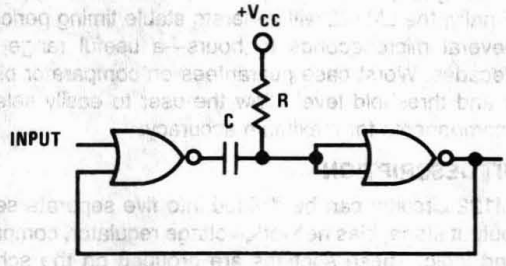
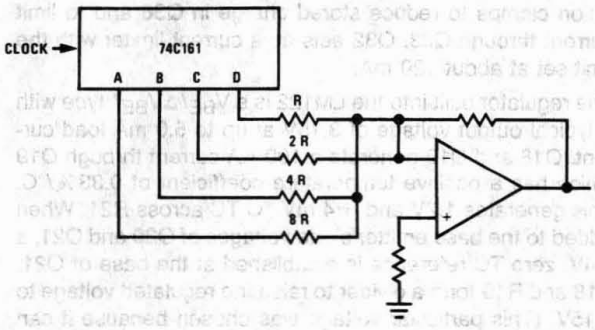
One Shot



$T = 1.4\ RC$

TL/F/6020–13

Staircase Generator



TL/F/6020–14

FIGURE 10. Variety of Circuit Ideas Using CMOS Devices

Versatile Timer Operates from Microseconds to Hours

National Semiconductor
Application Note 97

INTRODUCTION

Timing functions, until recently, have been somewhat neglected by integrated circuit manufacturers. The primary reason was the extremely wide range of input and output signals currently incorporated in discrete designs. In addition, power supply voltages varied over a ten to one range and timing periods were as short as microseconds and as long as hours.

The LM122 timer has been designed to operate over a very wide range of input/output signal levels, supply voltages, and timing periods. It will replace most discrete designs with improved performance and reliability. This new timer overcomes many of the problems incurred in discrete or early IC designs.

First, it locks out trigger signals during the timing period to guarantee a precise output regardless of trigger level—while maintaining the ability to be retriggered almost immediately following the end of the timing pulse. (Duty cycles up to 99.9% can be achieved.) Secondly, the timing period is free from jitter caused by supply fluctuations because the timing components are driven from an internal regulated source. Supply voltage for the timer can vary from 4.5V to 40V even during the timing period! An additional feature is the ±40V excursion allowed on the trigger input and the 40V/50 mA drive capability of the output transistor. These two specifications allow the LM122 to interface directly to present designs without level shift or power boosting problems. Finally, the LM122 will generate stable timing periods from several microseconds to hours—a useful range of eight decades. Worst case guarantees on comparator bias current and threshold level allow the user to easily select timing components for maximum accuracy.

CIRCUIT DESCRIPTION

The LM122 circuitry can be divided into five separate sections: output stage, bias network, voltage regulator, comparator, and logic. These sections are grouped on the schematic in *Figure 1* to simplify understanding of the timer.

The floating transistor output stage of the LM122 consists of Q32 through Q36. Q36 is the actual output transistor and is driven by emitter follower, Q33. Q34 and Q35 are antisaturation clamps to reduce stored charge in Q36 and to limit current through Q33. Q32 acts as a current limiter with the limit set at about 120 mA.

The regulator built into the LM122 is a $V_{BE}/\Delta V_{BE}$* type with a typical output voltage of 3.15V at up to 5.0 mA load current. Q18 and Q19 generate a 100 μA current through Q19 which has a positive temperature coefficient of 0.33%/°C. This generates 1.2V and +4 mV/°C TC across R21. When added to the base emitter diode voltages of Q20 and Q21, a 2.4V, zero TC reference is established at the base of Q21. R18 and R19 form a divider to raise the regulated voltage to 3.15V. (This particular voltage was chosen because it can be operated off a single 5.0V supply and because one RC time constant is exactly 2.0V out of 3.15V.) Q23 buffers Q21 from supply fluctuations and sets up the currents for the bias section of the timer. Q20 is a single stage of voltage gain for the regulator. It is buffered by the series pass transistor, Q24. Q25, Q26, R25, and R26 are included for starting purposes and do not affect operation once current is flowing in the regulator section.

*See AN-42, "On Card Regulator for Logic Circuits"

The function of the comparator is to cause an output change of state when the timing capacitor has charged to one RC time constant. Q11 through Q17 perform this function. Q14, Q15, Q16, and Q17 are a Darlington differential stage driving an active load formed by Q12 and Q13. Q11 is a second stage operating as a common emitter amplifier with R14 as its load resistor. For long timing intervals, the Darlington is run with no bleed current from Q30. Operating current for Q15 and Q16 is about 5 μA per side. The specially processed lateral PNP's have h_{FE}'s of about 200, so operating current for Q14 and Q17 is typically 25 nA. At these current levels, the substrate PNP's have h_{FE}'s of 80, giving comparator input currents of 300 pA! One side of the comparator is tied to a divider (R16 and R17) which is set at 63.2% of the reference voltage — one RC time constant. The other side is connected to the external timing resistor and capacitor.

The logic section of the LM122 performs four functions: first, it provides a latching action to make the circuitry immune to retriggering during the timing interval; second, it simulates the action of an exclusive OR gate to generate a logic reverse function; additionally, it translates the low level output from the comparator to the high level swing needed to drive the floating transistor output; and finally, it drives the discharge transistor to reset the timing capacitor. Q2 and Q3 makeup the TTL compatible trigger input to the logic section. Q3 is a lateral PNP with 60V reverse emitter-base breakdown voltage, allowing negative inputs are high as −40V without harm to the chip. R5 is an epitaxial resistor which pinches off at 30V and has a breakdown of 80V. This allows positive input voltages of up to 40V on the trigger terminal even when operating the timer from a supply voltage of only 5.0V. Typical current drawn by the trigger terminal is 40 μA at 2.0V and 600 μA at 40V. Q4 and Q6 form a latch which self-limits at about 400 μA and can be turned off by Q2. Q5 and Q7 interface the latch to the comparator so that the comparator can fire the latch at the end of the timing period. Q8, Q9, and Q10 perform the level shifting required to drive the output transistor and double as an exclusive OR gate, with the emitters of Q8 and Q9 as one input and the collectors of Q5 and Q11 as the second input. Grounding the Q8 and Q9 emitters reverses the effect of a signal appearing at the collector of Q11.

Biasing for the various circuits in the timer is generated by a string of PNP current sources consisting of Q27 through Q31. Current levels are established by the constant current source, Q23, driving diode connected Q28. The current from Q23 is 400 μA, setting the drop across the emitter resistor, R28 plus R29, at 200 mV. Q29 delivers 10 μA to the comparator and Q31 supplies a total of 100 μA to the output transistor and logic circuitry. Part of Q29's collector is returned to Q27 to avoid having to use a large value resistor for R30. Q30 is completely off when using the timer for long timing periods. Shorting the boost terminal of V+ adds

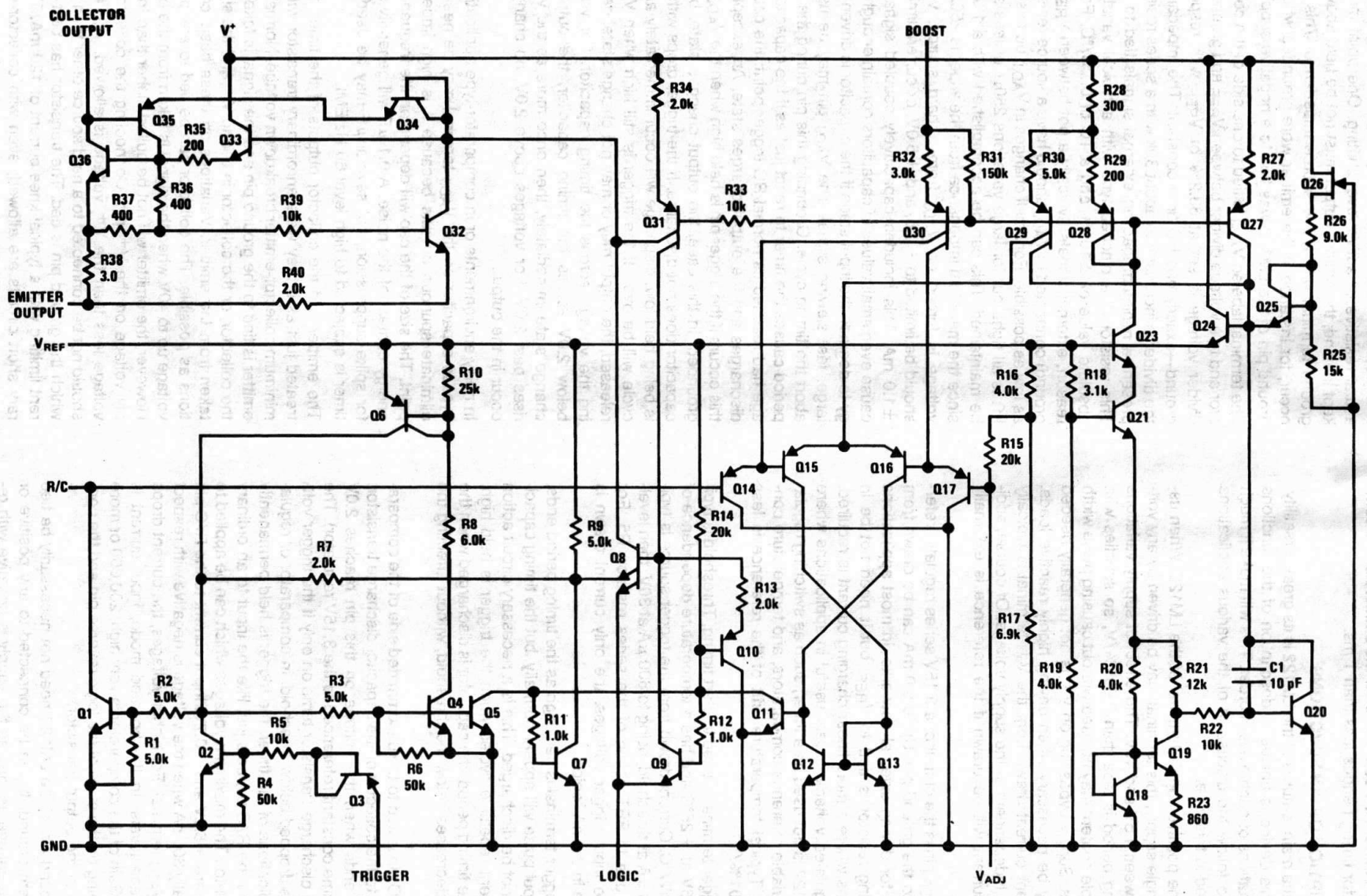


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FIGURE 1. Schematic Diagram

about 5 μA bleed current at the emitters of Q14 and Q17. This extra current is needed to slew the emitters of the comparator for timing periods less than 1 ms.

DESCRIPTION OF PIN FUNCTIONS

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

V^+ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing on V^+ is not generally needed but may be necessary when driving highly reactive loads. Quiescent current drawn from the V^+ terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The V_{REF} pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to V_{REF}, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature controllers. Typical temperature drift of the reference is less than 0.01%/°C.

The trigger terminal is used to start timing. Threshold is typically 1.6V at +25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the trigger source is typically 20 μA at threshold, rising to 600 μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region.

If the trigger terminal is held high as the timing period ends, the output pulse will appear normally, but the timing capacitor will not be discharged. This is a necessary circuit action to prevent repetitive cycles when the trigger is held high. After the timing period, the capacitor is discharged when the trigger decreases below the threshold, without affecting the output.

The R/C pin is tied to the uncommitted side of the comparator and to the collector of the capacitor discharge transistor. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). The internal discharge transistor turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the R/C pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Input current to the R/C pin is typically 300 pA when the voltage is negative with respect to the V_{ADJ} terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is 30 nA. Gain of the comparator is very high, 200,000 or more depending on the state of the logic reverse pin and the connection of the output transistor.

The ground pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the V^+ terminal. Level shifting may be necessary for the input trigger if the trigger voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the ground terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the ground pin of the LM122 was tied to a negative supply.

The terminal labeled V_{ADJ} is tied to one side of the comparator and to a voltage divider between V_{REF} and ground. The divider voltage is set at 63.2% of V_{REF} with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to V_{ADJ}. This resistor is a pinched type with a typical variation in absolute value of ±100% and a TC of 0.7%/°C. For this reason, external signals (typically a pot between V_{REF} and ground) connected to V_{ADJ} should have a source resistance as low as possible. For small changes in V_{ADJ}, up to several kΩ is all right, but for large variations 250Ω or less should be maintained. This can be accomplished with a 1.0k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on V_{ADJ} from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The V_{ADJ} pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high when the V_{ADJ} pin is grounded. In this case, the output changes state, but the capacitor does not discharge. If the trigger drops with V_{ADJ} is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when V_{ADJ} is released, the output may or may not change state, depending the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output.

In noisy environments or in comparator-type applications, a bypass capacitor on the V_{ADJ} terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1 μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The emitter and the collector outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the emitter is tied to the ground pin and the signal is taken from the collector, or the collector is tied to V^+ and the signal is taken from the emitter. Variations on these basic connections as possible. The collector can be tied to any positive voltage up to 40V when the signal is taken from the emitter. However, the emitter will not be pulled higher than the supply voltage on the V^+ pin. Connecting the collector to a voltage less than the V^+ voltage is allowed. The emitter should not be connected to a hard source other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with collector-emitter voltages up to 40V. The power time product, however, must

not exceed 15 watt•seconds for power levels above the maximum rating of the package. A short to 30V, for instance, can not be held for more than 4 seconds. These levels are based on a 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A boost pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current. For short time intervals where low input current is not needed, comparator operating current can be increased several orders of magnitude for fast operation. Shorting the boost terminal to V^+ increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5.0 μA.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used.

The "Logic" pin is used to reverse the signal appearing at the output transistor. An open or "high" condition on the logic pin programs the output transistor to be "off" during the timing period and "on" all other times. Grounding the logic pin reverses the sequence to make the transistor "on" during the timing period. Threshold for the logic is typically 150 mV with 150 μA flowing out of the terminal. If an active drive to the logic pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum V_{SAT} of 75 mV of 200 μA is required. A typical example of active drive to the logic pin is the pulse width discriminator shown in *Figure 16*.

CALCULATING WORST CASE TIMING ERROR

Timing errors for the LM122 come from the following sources:

1. Timing ratio error
2. Capacitor saturation voltage
3. Internal switching delays
4. Comparator bias current
5. External resistor and capacitor tolerance
6. Capacitor and board leakage

In general, errors 1 and 5 are the most significant, so they will be treated first.

For most applications, the major contribution to timing error from the LM122 itself is variation in timing ratio, which is the ratio of the comparator threshold voltage (typically 2.0V) to the voltage at the V_{REF} pin. A 1% error in this ratio results in a 1.8% initial timing error. Timing ratio error comes from variations in the internal divider ratio and from offset voltage in the comparator. The LM122 is specified to have a timing ratio from 0.626 to 0.638 at +25°C, giving a ±1.8% worst case contribution to initial timing period error. Over temperature, the worst case figures doubles to ±3.6%. If the initial error is trimmed out externally however, timing error drift due to timing ratio will generally be less than ±0.5% over temperature.

Adding all the contributions to timing error from the LM122 itself will usually give a figure in the 2% to 3% range at +25°C. External timing components (R_t and C_t) will normally contribute much more error than this unless selected components are used. ±5% tolerance on R_t and C_t will increase the worst case error to 12% to 13%. By trimming out initial component errors, an exact initial timing period can be obtained, but temperature drift then becomes the limiting factor. For most applications, the contributions to timing period drift due to the LM122 itself will be in the 0.005%/°C to 0.02%/°C range.

If accurate timing over temperature is required, low drift components must be used for R_t and C_t. Capacitors are available with temperature coefficients of 100 to 200 ppm/°C. Resistors, at least in the lower ranges, are available with TC's much better than this. Above 1 MΩ, however, care must be used in the selection of a low TC resistor. Units are available up to 100 MΩ with less than 100 ppm/°C drift.

Capacitor saturation voltage is the voltage still remaining on the timing capacitor after it has been reset to as near ground as the internal discharge transistor can drive it. For timing resistors 1 MΩ or greater, this remaining voltage is typically 2.5 mV. For smaller timing resistors, the capacitor saturation voltage can be calculated by the following: formula:

$$V_C \approx 2.5\ \text{mV} + \frac{(V_{REF})^* (80\Omega)}{R_t}$$

*V_{REF} = 3.15V

The effect of V_C on timing period is linear at 0.03%/mV. Temperature dependence of V_C is typically +0.2%/°C for $R_t \leq 300\ k\Omega$, rising to 0.4%/°C for $R_t = 10\ k\Omega$. This gives a typical temperature coefficient of timing error *due to* V_C of (0.002) (2.5 mV) (0.03%/mV) = 0.0015%/°C for $R_t \geq 1\ M\Omega$ and (0.004) (24 mV) (0.03%/mV) ≈ 0.003%/°C for $R_t = 10\ k\Omega$. Since most applications can use timing resistors in the range of 100 kΩ and up, error *from capacitor saturation voltage* rarely exceeds 0.15% initially, with ±0.05% variation over the full temperature range.

Internal switching delays cause errors which tend to be a fixed time rather than a percentage of the timing period. In the boosted mode this delay is typically 800 ns, and with the boost off; the delay is about 25 μs. These times can be

added directly to the calculated timing period for worst case analysis. For timing periods longer than 25 ms, the 25 μs delay gives an error of 0.1% or less. In the range of 1 or 25 ms, error due to delays is 0.1% or less for the boosted mode, rising to a maximum of 4.0% in the unboosted mode. At $\tau = 10$ μs, delay is the major contribution to timing error ($\approx$ 8%).

Comparator bias current contributes a negligible timing error for all but very long time timing periods. Error can be calculated with a simple formula:

$$\text{Error (\%)} = -50 \times R_t \times I_b \text{ (Note sign)}$$

I_b = Comparator Bias Current

R_t = Timing Resistor

For $R_t = 100$ MΩ and $I_b = 0.3$ nA (typical) a 1.5% reduction in timing period is incurred. For worst case calculations at +25°C, an I_b of 1 nA maximum is specified in the unboosted mode and 100 nA in the boosted mode. At temperatures below +25°C, these numbers still hold. At +125°C, I_b increases due to leakage to a maximum of $\pm$5 nA unboosted. For worst case calculations below +125°C, the leakage error (5 nA) can be assumed to halve for each 10°C drop below +125°C. At +95°C for instance, the leakage component of I_b would be (5 nA/8) $\approx$ 0.6 nA for a total I_b of 1.6 nA worst case. For the commercial LM322 and LM3905, worst case I_b is 2 nA at +75°C, and for the LM2905 I_b is 2 nA maximum at +85°C. For temperatures between −25°C and +85°C, the TC of I_b is typically 5 pA/°C in the unboosted mode and 100 pA/°C in the boosted mode. For a 100 MΩ R_t, this 5 pA/°C contributes −0.025%/°C to timing period drift.

$$\text{Error (\%/°C)} = (-50)(\Delta I_b/\Delta T)(R_t)$$

For worst case calculations a $\Delta I_b/\Delta T$ ($-25 \leq T_A \leq +85$°C) of 12 pA/°C may be used for the LM122/LM222 and 20 pA/°C for the LM322 and LM2905/LM3905.

External leakage paths may cause timing errors for large values of R_t and high board temperatures. Connections made to the R/C pin should be kept free of dust, moisture, and soldering flux if long time intervals are to be kept accurate. All package types have the R/C pin located between V_{REF} and the ground pin to minimize these leakages.

DESIGN HINTS

ELIMINATING TIMING CYLCE UPON INITIAL APPLICATION OF POWER

The LM122 will start a timing cycle automatically (with no trigger input) when V^+ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to V_{REF} instead of ground as shown in *Figure 2*. This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to V_{REF}. A 1.0 kΩ resistor should be included in series with the timing capacitor to limit the surge current load on V_{REF} when the capacitor is discharged.

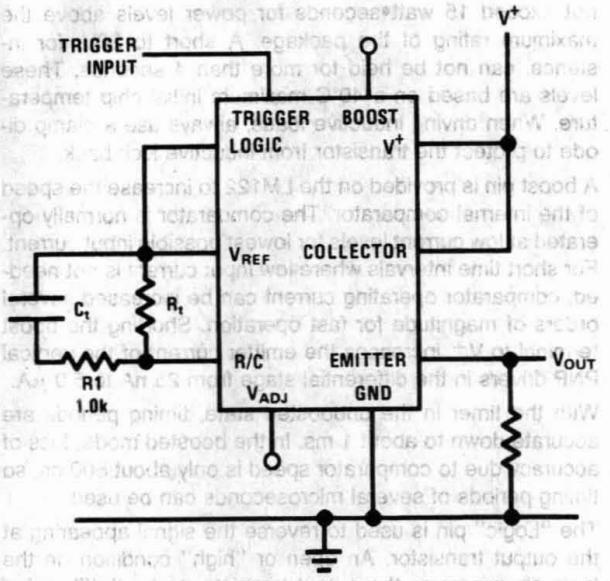

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FIGURE 2. Eliminating Initial Timing Cycle

USING ELECTROLYTIC TIMING CAPACITORS

Electrolytic capacitors are not usually recommended for timing because of their unstable capacitance and high leakage. For long timing periods (> 10 seconds) at moderate temperatures (0°C to 50°C) however, an electrolytic may be attractive because of its low cost per microfarad. Solid tantalum capacitors such as the Kemet* C series T310 (molded epoxy) or T110 (hermetic) are recommended. These units have long term stabilities of 2% to 3% and a temperature coefficient of +0.2%/°C. Selected units are available for timing use with very low leakage.

RESET TIME

The timing capacitor used with the LM122 is reset with an internal transistor which has a collector offset voltage of 2.5 mV @ 1 μA with approximately 80Ω of collector resistance. The time required to reset this capacitor determines the minimum time between timing pulses. An approximate formula for reset time is:

$$\text{Reset Time} = (80\Omega)(C_t^{\dagger})\ (5)$$

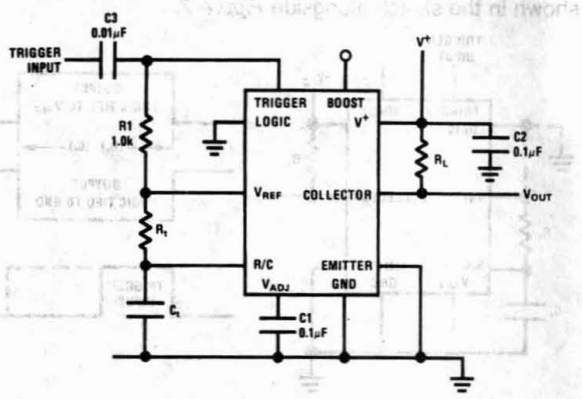
$^{\dagger}C_t$ = External timing capacitor.

NOISY ENVIRONMENTS

The LM122 is relatively insensitive to noise on supply lines and to radiated energy. In *extremely* noisy environments however, it may be necessary to configure the LM122 differently, both to eliminate false triggering and to prevent premature end of a timing period. The circuit "a" shown in *Figure 3* has been set up for maximum noise rejection. C1 bypasses the V_{ADJ} pin because of the relatively high impedance ($\cong$ 30 kΩ) of this point. Negative spikes on the V_{ADJ} pin will cause premature end of the timing period. C2 bypasses the supply for rejection of fast transients. R1 sets up the trigger pin to a "normally high" condition. This prevents extremely high electromagnetic fields from triggering the internal flip-flop during a timing period. The input trigger signal is capacitively coupled through C3. Triggering occurs on the *negative* edge of the trigger pulse as shown in the waveform sketch next to *Figure 21*.

*Manufactured by Union Carbide

If the output voltage from the LM122 can be set up to go "high" during the timing cycle, the alternate connection shown in "b" can be used. Here, the trigger is held high by D2 during the timing period. When the output goes low after the timing period is over, the circuit may be retriggered immediately via D1. R1 and C3 suppress unwanted spikes at the trigger input.



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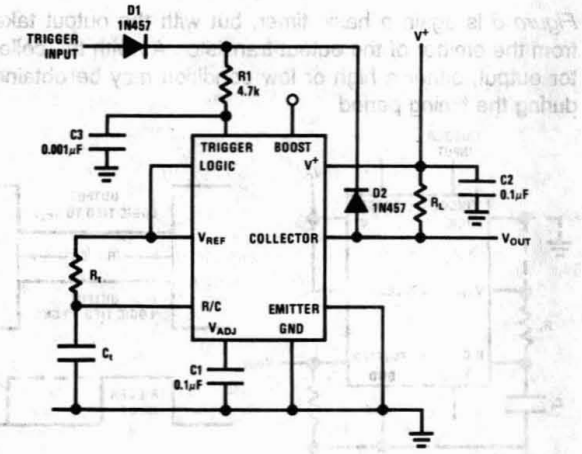
(A)



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(B)

FIGURE 3. Maximum Noise Immunity

ABORTING A TIMING CYCLE (*Figure 4*)

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground V_{ADJ}
- Raise R/C more positive than V_{ADJ}
- Wire "OR" the output

Grounding V_{ADJ} will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving V_{ADJ} to as near ground as possible. Worst case sink current is about 300 μA.

A timing cycle may be also ended by a positive pulse to a resistor ($R \leq R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to V_{ADJ} (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.

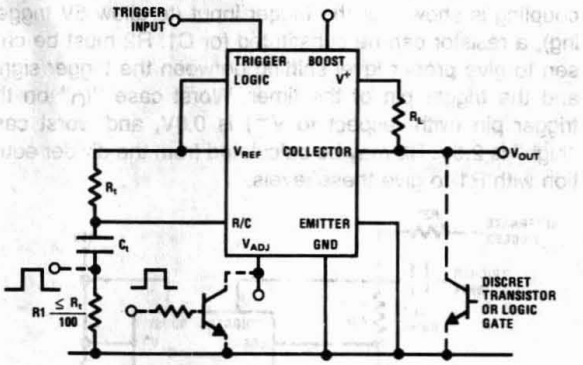

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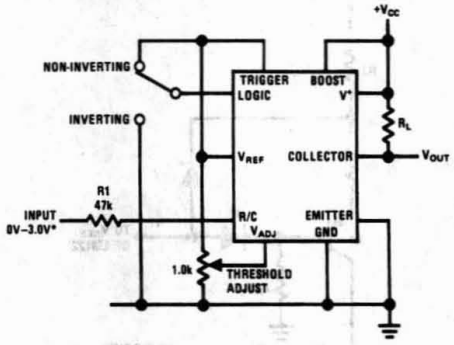
FIGURE 4. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

USING THE LM122 AS A COMPARATOR

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the V_{ADJ} terminal with a divider tied to V_{REF}. Stability of the refrence voltage is typically ±1% over a temperature range of −55°C to +125°C. Offset voltage drift in the comparator is typically 25 μV/°C in the boosted mode and 50 μV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to ±50V as shown in *Figure 5*. There is actually no limit on input voltage as long as current is limited to



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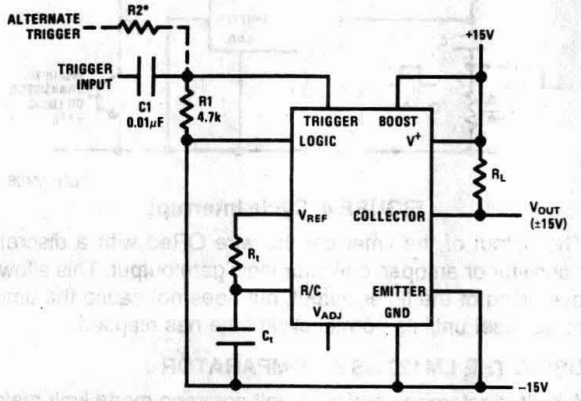
*Timer Protected Against Damage for Up to ±50V

FIGURE 5. Comparator with 0 Volts to 3.0 Volts Threshold

±1 mA. The resistor shown contributes a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply should make this comparator very useful.

USING DUAL SUPPLIES

The LM122 can be operated off dual supplies as shown in *Figure 6*. The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to V^- or be actually tied to V^- as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "I_O" on the trigger pin (with respect to V^-) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.



*Select For Proper Level Shift

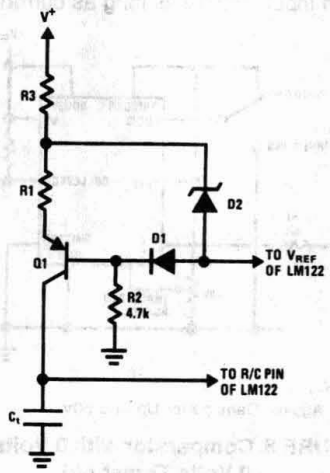
TL/H/7408–7

Emitter Terminal Or Emitter Load Must Be Tied To GND Pin Of Timer.

FIGURE 6. Operating Off Dual Supplies

LINEARIZING THE CHARGING SWEEP

In some applications (such as a linear pulse width modulator) it may be desirable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in the accompanying sketch.



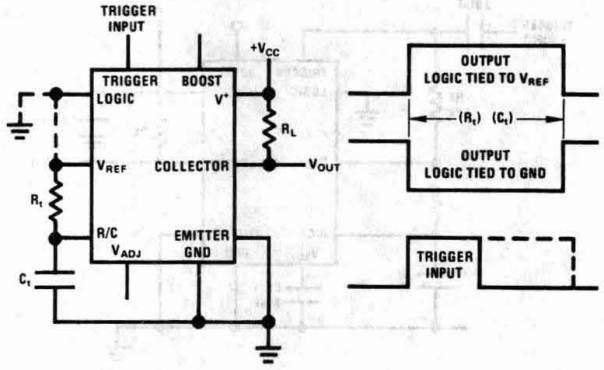
TL/H/7408–8

Q1 converts the current through R1 to a current source independent of the voltage across C_t. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the V^+ supply is stable and D1 and R2 can be omitted also if temperature stability if not critical. With D1 and R2 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

APPLICATIONS

BASIC TIMERS

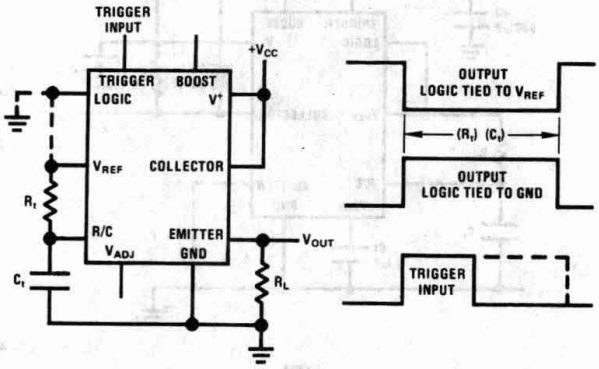
Figure 7 is a basic timer using the collector output. R_t and C_t set the time interval with R_L as the load. During the timing interval the output may be either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch alongside *Figure 7*.



TL/H/7408–9

FIGURE 7. Basic Timer-Collector Output and Timing Chart

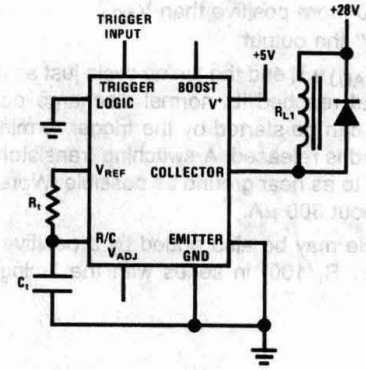
Figure 8 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.



TL/H/7408–10

FIGURE 8. Basic Timer-Emitter Output and Timing Chart

Figure 9 shows the timer interfacing 5V logic to a high voltage relay. Although the V^+ terminal could be tied to the +28V supply, this would be an unnecessary waste of power in the IC. In any case, the threshold for the trigger is 1.6V regardless of where V^+ is tied.



TL/H/7408–11

FIGURE 9. 5 Volt Logic Supply Driving 28 Volt Relay

Figure 10 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. V_{OUT} swings between +5V and ground with a minimum fanout of 5 for medium speed TTL.

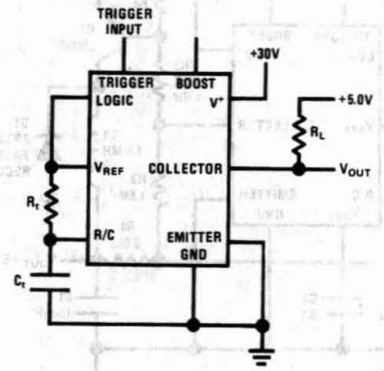


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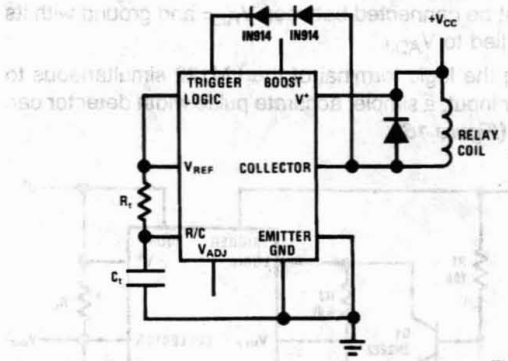
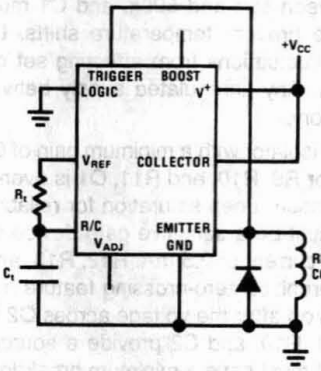
FIGURE 10. 30 Volt Supply Interfacing to 5 Volt Logic

Figure 11 is an application where the LM122 is used to simulate a thermal delay relay which prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for R_t C_t seconds after V_{CC} is applied, then closes and stays energized until V_{CC} is turned off. *Figure 12* is a similar circuit except that the relay is energized as soon as V_{CC} is applied. R_t C_t seconds later, the relay is de-energized and stays off until the V_{CC} supply is recycled.



TL/H/7408–13

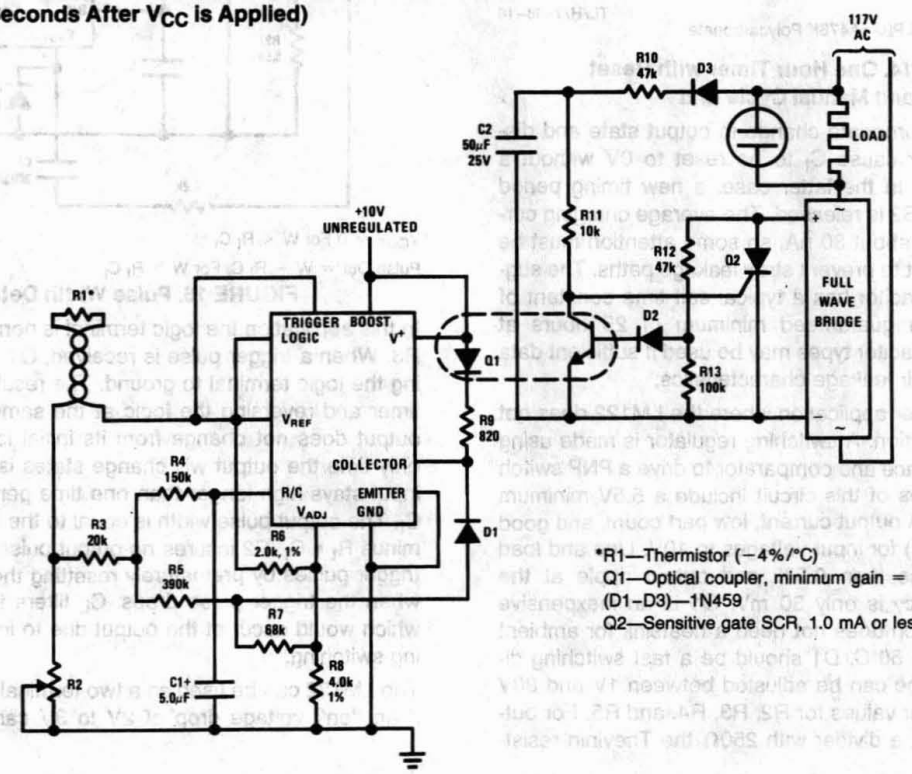
FIGURE 11. Time Out on Power Up (Relay Energized R_tC_t Seconds After V_{CC} is Applied)



TL/H/7408–14

FIGURE 12. Time Out on Power Up (Relay Energized *Until* R_tC_t Seconds After V_{CC} is Applied)

Figure 13 is a more advanced application of the LM122 as a proportioning temperature controller with optical isolation and synchronized zero crossing features. The timing function is not used. Instead the trigger terminal is held high and the LM122 is used as a high gain comparator with a built in reference. R1 is a thermistor with a −4%/°C temperature coefficient used as the sensor. R2 is used to set the temperature to be controlled by R1. R3 through R8 set up the proportioning action. R3 raises the impedance of the R1/R2 divider so that R5 sees a relatively constant impedance independent of the set point temperature. R6 and R8 reduce the V_{ADJ} impedance so that internal variations in divider impedance do not affect proportioning action. R5 and R7



*R1—Thermistor (−4%/°C)
Q1—Optical coupler, minimum gain = ½ at 1.0 mA
(D1–D3)—1N459
Q2—Sensitive gate SCR, 1.0 mA or less

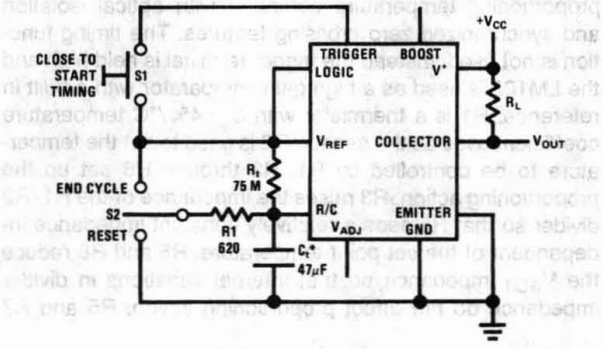
TL/H/7408–15

FIGURE 13. Proportioning Temperature Controller with Synchronized Zero-Crossing

set the actual width of the proportioning band and can be scaled as necessary to alter the width of the band. Larger resistors make the band narrower. The values shown give approximately a 1°C band. R4 and C1 determine the proportioning frequency which is about 1 Hz with the values shown. C1 or R4 can change to alter frequency, but R4 should be between 50k and 500k, and C1 must be a low leakage type to prevent temperature shifts. D1 prevents supply voltage fluctuations from affecting set point or proportioning band. Any unregulated supply between 6V and 15V is satisfactory.

Q1 is an optical isolator with a minimum gain of 0.5. With the values shown for R9, R10, and R11, Q1 is over-driven by at least 3 to 1 to insure deep saturation for reliable turn off of the SCR. Q2 must be a sensitive gate device with a worst case gate firing current of 0.5 mA. R12, R13, and D2 implement the synchronized zero-crossing feature by preventing Q1 from turning off after the voltage across Q2 has climbed above 2.5V. D3, R10, and C2 provide a source of semifiltered dc current must have a minimum breakdown of 200V.

Figure 14 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with the appropriate change in output state and discharging of C_t, or cause C_t to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released. The average charging current through R_t is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.

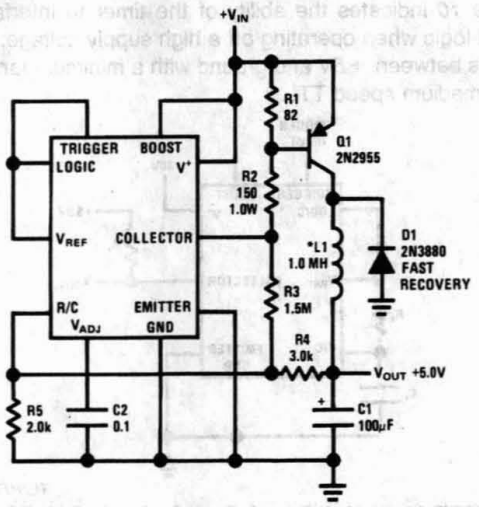


TL/H/7408–16

*Dearborn Electronics LP9A1A476K Polycarbonate

FIGURE 14. One Hour Timer with Reset and Manual Cycle End

Figure 15 is another application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP switch transistor. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω the Thevinin resistance must be connected between V_{REF} and ground with its tap point tied to V_{ADJ}.



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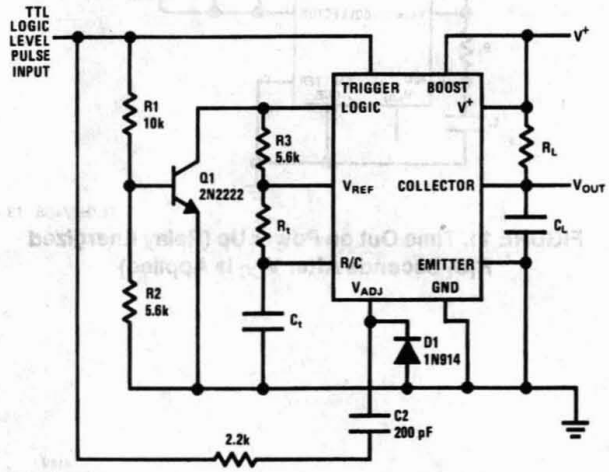
*No. 22 Wire Wound On Molybdenum Permalloy Core

FIGURE 15. 5 Volt Switching Regulator with 1.0 Amp Output and 5.5 Volt Minimum Input

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made (*Figure 16*).



*V_{OUT} = 0 For W < R_t C_t

Pulse Out = W − R_t C_t For W > R_t C_t

TL/H/7408–18

FIGURE 16. Pulse Width Detector

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by R_t and C_t. The output pulse width is equal to the input trigger width minus $R_t \bullet C_t$. C2 insures no output pulse for short (< RC) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops. C_L filters the narrow spikes which would occur at the output due to interval delays during switching.

The LM122 can be used as a two terminal time delay switch if an "on" voltage drop of 2V to 3V can be tolerated. In

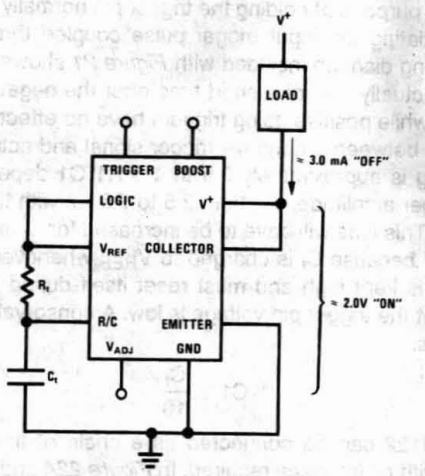


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FIGURE 17. Two-Terminal Time Delay Switch

Figure 17, the timer is used to drive a relay "on" R_t C_t seconds after application of power "off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in *Figure 18*. Pulse width is adjusted with R2 to provide initial calibration at 10 kHz. The collector of the output transistor is tied to V_{REF}, giving constant amplitude pulses equal to V_{REF} at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, (R_t) (C_t) (V_{REF}) (f). Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

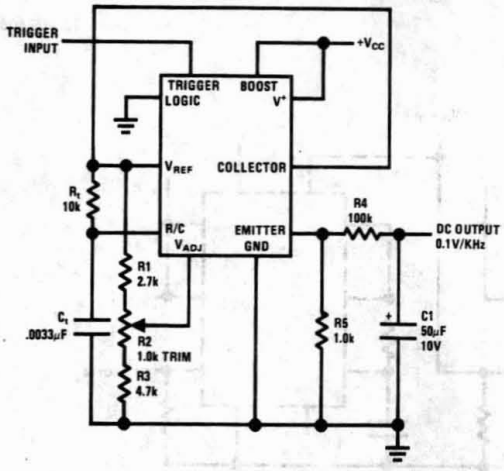

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FIGURE 18. Frequency to Voltage Converter (Tachometer) Output Independent of Supply Voltage

In some applications it is desirable to reduce supply drain to zero between timing cycles. In *Figure 19* this is accomplished by using an external PNP as a latch to drive the V+ pin of the timer.

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is

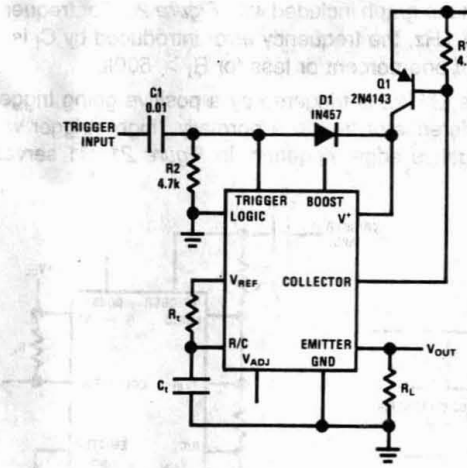

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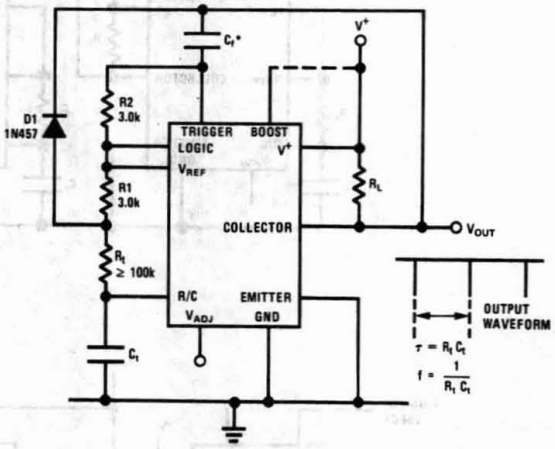
FIGURE 19. Zero Power Dissipation Between Timing Intervals

received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents coupling back into the trigger signal from the dc load created by the trigger input. If the trigger input is a short pulse, C1 and R2 may be eliminated. R_L must have a minimum value of $(V_{CC})/(2.5\ mA)$.

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capac-



*See Chart

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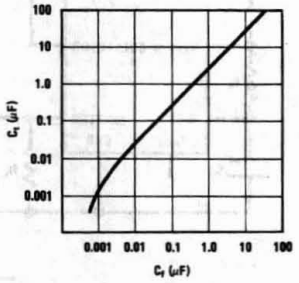

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FIGURE 20. Oscillator

itor as shown in *Figure 20*. Operating frequency is $1/(R_t\ C_t)$. The output is a narrow negative pulse whose width is approximately $2R_2\ C_f$. For optimum frequency stability, C_f should be as small as possible. The minimum value is determined by the time required to discharge C_t through the internal discharge transistor. A conservative value for C_f can be

chosen from the graph included with *Figure 20*. For frequencies below 1 kHz, the frequency error introduced by C_f is a few tenths of one percent or less for $R_t > 500k$.

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally "high" trigger will result in negative edge triggering. In *Figure 21*, R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with *Figure 21* shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual starts of timing is approximately 0.5 to 1.5 R1 C1 depending on the trigger amplitude, or about 2.5 to 7.5 μs with the values shown. This time will have to be increased for C_t larger than 0.01 μF because C_t is charged to V_{REF} whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

$$C1 \geq \frac{C_t}{10}$$

The LM122 can be connected as a chain of timers quite easily with no interface required. In *Figure 22A* and *22B*, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.

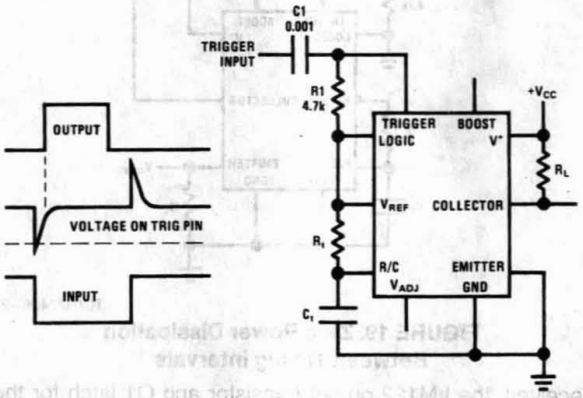

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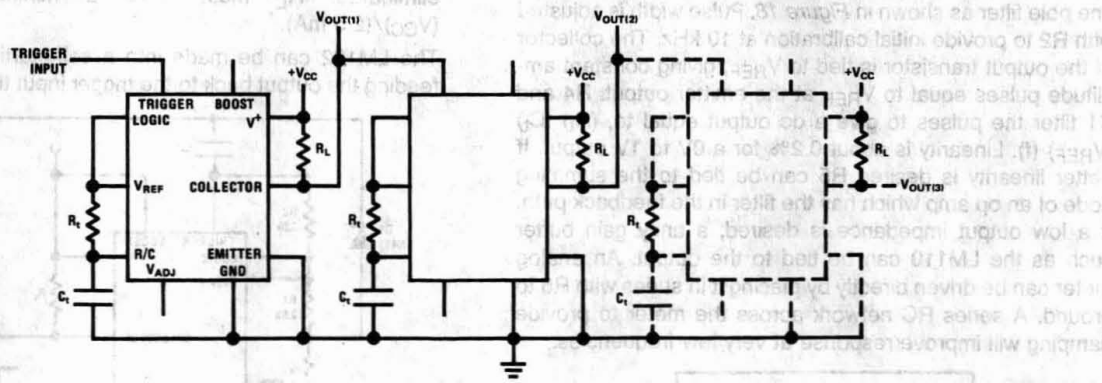
FIGURE 21. Timer Triggered by Negative Edge of Input Pulse



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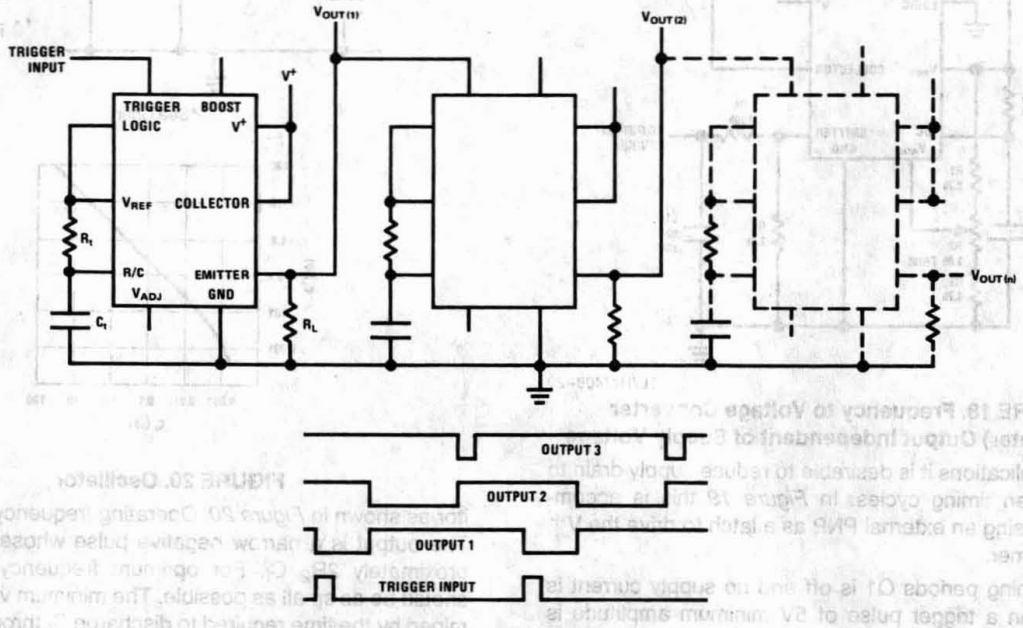
(A)



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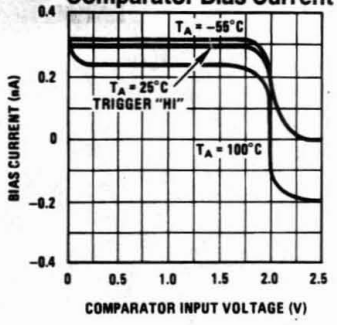
(B)

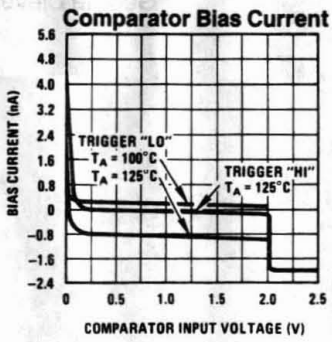
FIGURE 22. Chain of Timers

Typical Performance Characteristics

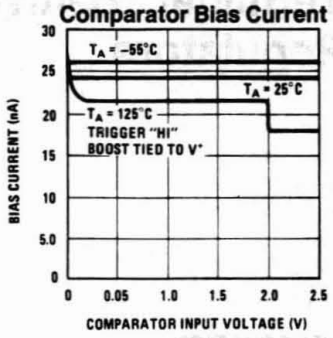
Comparator Bias Current



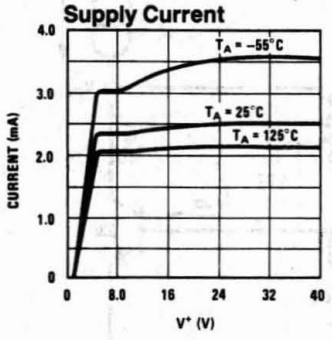
Comparator Bias Current



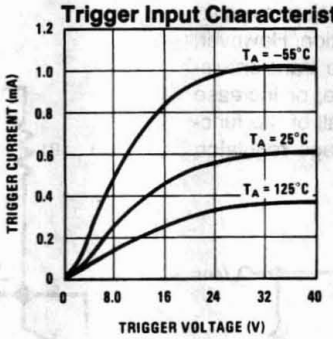
Comparator Bias Current



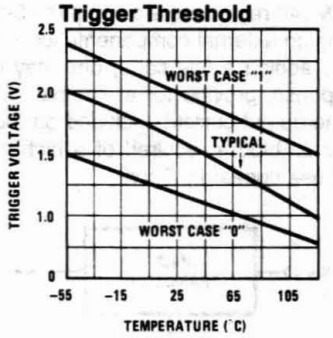
Supply Current



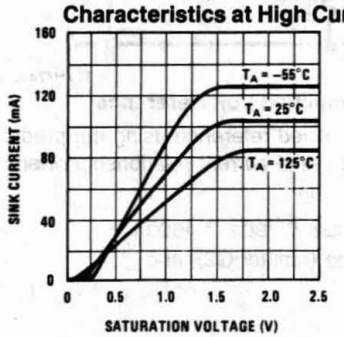
Trigger Input Characteristics



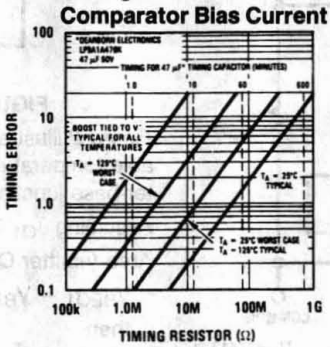
Trigger Threshold



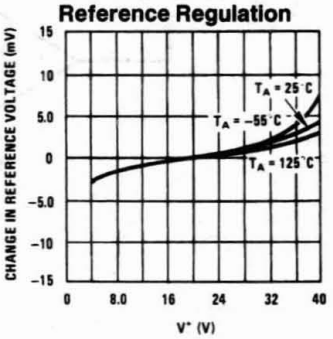
Collector Output Saturation Characteristics at High Current



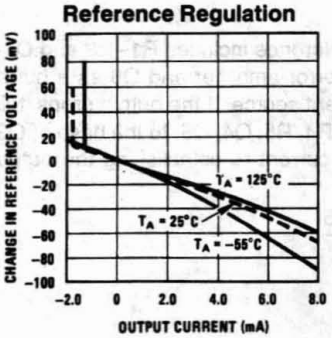
Timing Error Due to Comparator Bias Current



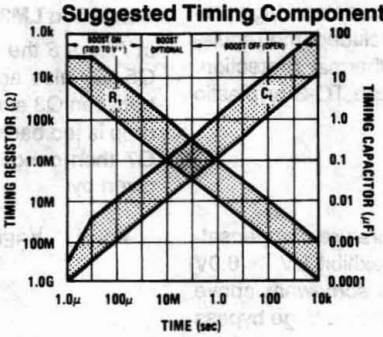
Reference Regulation



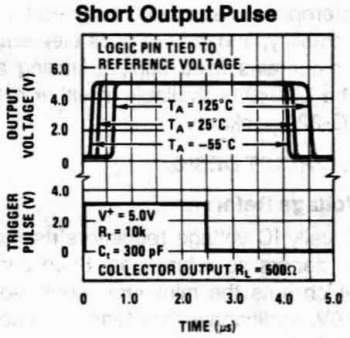
Reference Regulation



Suggested Timing Components



Short Output Pulse



TL/H/7408–27

LM340 Series Three Terminal Positive Regulators

National Semiconductor
Application Note 103
George Cleveland

INTRODUCTION

The LM340-XX are three terminal 1.0A positive voltage regulators, with preset output voltages of 5.0V or 15V. The LM340 regulators are complete 3-terminal regulators requiring no external components for normal operation. However, by adding a few parts, one may improve the transient response, provide for a variable output voltage, or increase the output current. Included on the chip are all of the functional blocks required of a high stability voltage regulator; these appear in *Figure 1*.

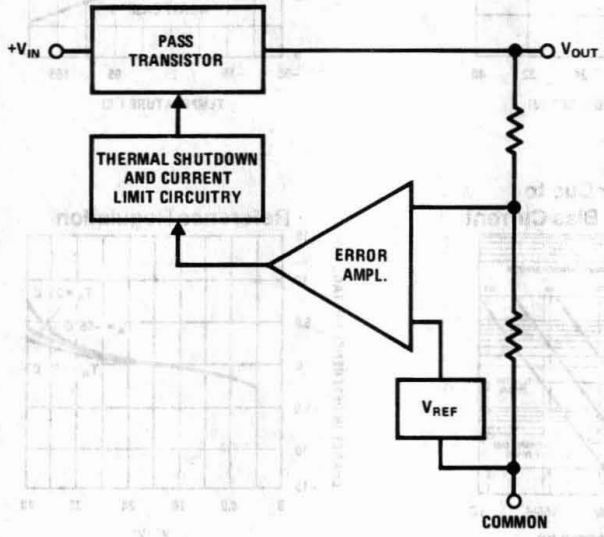


FIGURE 1. Functional Block of the LM340

The error amplifier is internally compensated; the voltage reference is especially designed for low noise and high predictability; and, as the pass element is included, the regulator contains fixed current limiting and thermal protection. The LM340 is available in either metal can TO-3 or plastic TO-220 package.

1. CIRCUIT DESIGN

Voltage Reference

Usually IC voltage regulators use temperature-compensated zeners as references. Such zeners exhibit BV > 6.0V which sets the minimum supply voltage somewhat above 6.0V. Additionally they tend to be noisy, thus a large bypass capacitor is required.

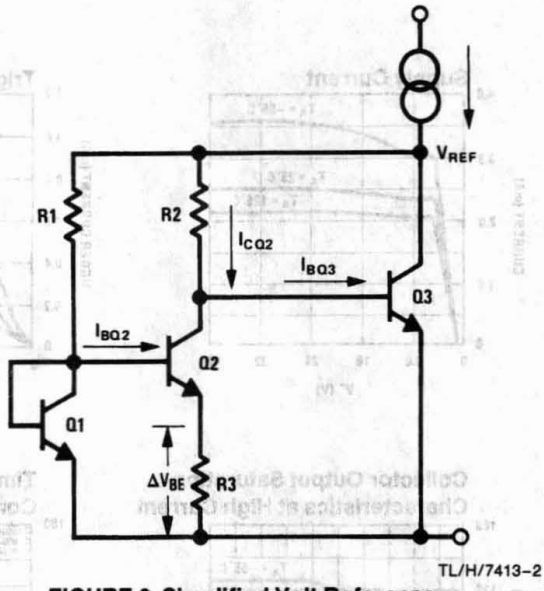


FIGURE 2. Simplified Volt Reference

Figure 2 illustrates a simplified reference using the predictable temperature, voltage, and current relationship of emitter-base junctions.

Assuming $J_{Q1} > J_{Q2}$, $I_{CQ2} \gg I_{BQ2} = I_{BQ3}$,
Area (emitter Q1) = Area (emitter Q2), and

$$V_{BEQ1} = V_{BEQ3}, \quad (1\text{-}1)$$

then

$$V_{REF} \cong \left(\frac{kT}{q} \ln \frac{R2}{R1}\right)\frac{R2}{R3} + V_{BEQ3} \quad (1\text{-}2)$$

Simplified LM340

In *Figure 3* the voltage reference includes R1–R3 and Q1–Q5. Q3 also acts as an error amplifier and Q6 as a buffer between Q3 and the current source. If the output drops, this drop is fed back, through R4, R5, Q4, Q5, to the base of Q3. Q7 then conducts more current re-establishing the output given by:

$$V_{OUT} = V_{REF}\frac{R4 + R5}{R4}$$

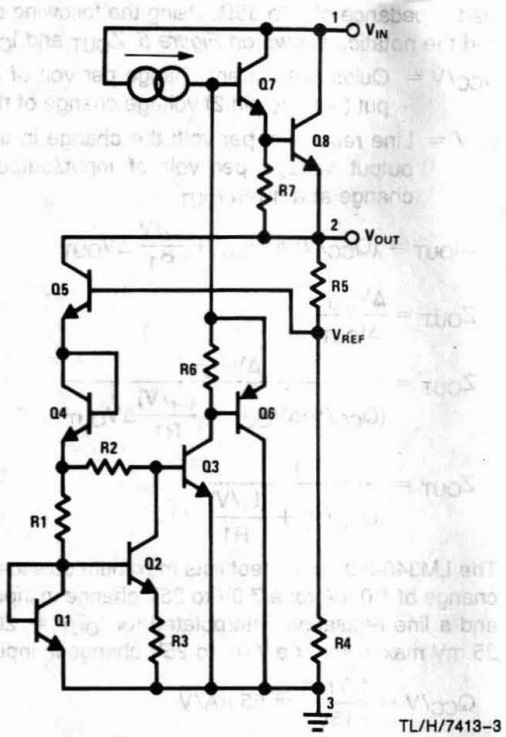


FIGURE 3. LM340 Simplified

Complete Circuit of the LM340 *(Figure 4)*

Here (J_{Q2}, J_{Q3}) > (J_{Q4}, J_{Q5}) and a positive TC ΔV_{BE} appears across R6. This is amplified by 17, (R6/R6 = 17) and is temperature compensated by the V_{BE} of Q6, Q7, Q8 to develop the reference voltage. R17 is changed to get the various fixed output voltages.

Short Circuit Protection

A) $V_{IN}-V_{OUT} < 6.0V$: There is no current through D2 and the maximum output current will be given by:

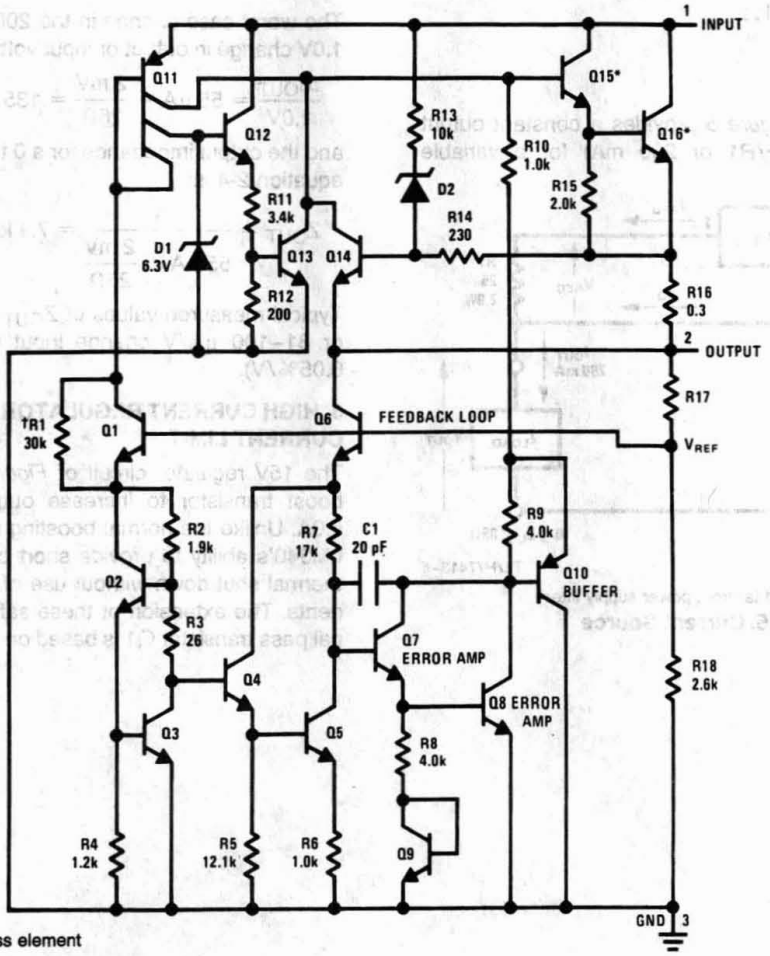
$$I_{OUT\,MAX} = \frac{V_{BEQ14}}{R16} \cong 2.2A\ (T_j = 25°C) \qquad (1\text{-}4)$$

B) $V_{IN}-V_{OUT} > 6.0V$: To keep Q16 operating within its maximum power rating the output current limit must decrease as $V_{IN}-V_{OUT}$ increases. Here D2 conducts and the drop across R16 is less than V_{BE} to turn on Q14. In this case I_{OUT} maximum is:

$$I_{OUT\,MAX} = \frac{1}{R16}\left(V_{BEQ14} - \frac{[(V_{IN} - V_{OUT}) - V_{ZD2} - V_{BEQ14}]}{R13} R14\right)$$

$$= 0.077\ [37.2 - (V_{IN} - V_{OUT})]\ (A) \qquad (1\text{-}5)$$

$$\text{at } T_j = 25°C$$



*Series pass element

†Starting up resistor

TL/H/7413–4

FIGURE 4. Complete Circuit of the LM340

Thermal Shut Down

In *Figure 4* the V_{BE} of Q13 is clamped to 0.4V. When the die temperature reaches approximately +175°C the V_{BE} to turn on Q13 is 0.4V. When Q13 turns on it removes all base drive from Q15 which turns off the regulator thus preventing a further increase in die temperature.

Power Dissipation

The maximum power dissipation of the LM340 is given by:

$$P_{D\,MAX} = (V_{IN\,MAX} - V_{OUT})\, I_{OUT\,MAX} + V_{IN\,MAX}\, I_Q \text{ (W)} \quad (1\text{-}6)$$

The maximum junction temperature (assuming that there is no thermal protection) is given by:

$$T_{jM} = \frac{36 - 13\, I_{OUT\,MAX} - (V_{IN} - V_{OUT})}{0.0855} + 25°C \quad (1\text{-}7)$$

Example:

$V_{IN\,MAX}$ = 23V, $I_{OUT\,MAX}$ = 1.0A, LM340T-15.

Equation (1-7) yields: T_{jM} = 200°C. So the T_j max of 150°C specified in the data sheet should be the limiting temperature.

From (1-6) $P_D \cong$ 8.1W. The thermal resistance of the heat sink can be estimated from:

$$\theta_{s\text{-}a} = \frac{T_{jMAX} - T_A}{P_D} - (\theta_{j\text{-}c} + \theta_{c\text{-}s}) \text{ (°C/W)} \quad (1\text{-}8)$$

The thermal resistance $\theta_{j\text{-}c}$ (junction to case) of the TO-220 package is 6°C/W, and assuming a $\theta_{c\text{-}s}$ (case to heat sink) of 0.4, equation (1-8) yields:

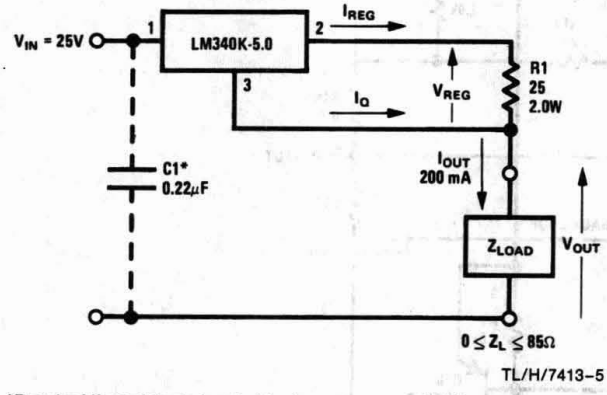
$\theta_{s\text{-}a}$ = 8.4°C/W

2. CURRENT SOURCE

The circuit shown on *Figure 5* provides a constant output current (equal to $V_{OUT}/R1$ or 200 mA) for a variable load impedance of 0 to 85Ω. Using the following definitions and the notation shown on *Figure 5*, Z_{OUT} and I_{OUT} are:

Q_{CC}/V = Quiescent current change per volt of input/output (pin 1 to pin 2) voltage change of the LM340

L_r/V = Line regulation per volt: the change in the LM340 output voltage per volt of input/output voltage change at a given I_{OUT}.



*Required if regulator is located far from power supply filter

FIGURE 5. Current Source

$$\Delta I_{OUT} = (Q_{CC}/V)\,\Delta V_{OUT} + \frac{L_r/V}{R1}\Delta V_{OUT} \quad (2\text{-}1)$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \quad (2\text{-}2)$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{(Q_{CC}/V)\Delta V_{OUT} + \frac{(L_r/V)}{R1}\Delta V_{OUT}} \quad (2\text{-}3)$$

$$Z_{OUT} = \frac{1}{(Q_{CC}/V) + \frac{(L_r/V)}{R1}} \quad (2\text{-}4)$$

The LM340-5.0 data sheet lists maximum quiescent current change of 1.0 mA for a 7.0V to 25V change in input voltage; and a line regulation (interpolated for I_{OUT} = 200 mA) of 35 mV maximum for a 7.0V to 25V change in input voltage:

$$Q_{CC}/V = \frac{1.0\text{ mA}}{15V} = 55\ \mu A/V \quad (2\text{-}5)$$

$$L_r/V = \frac{35\text{ mV}}{18V} \cong 2\text{ mV/V} \quad (2\text{-}6)$$

The worst case change in the 200 mA output current for a 1.0V change in output or input voltage using equation 2-1 is:

$$\frac{\Delta I_{OUT}}{1.0V} = 55\ \mu A + \frac{2\text{ mV}}{25\Omega} = 135\ \mu A \quad (2\text{-}7)$$

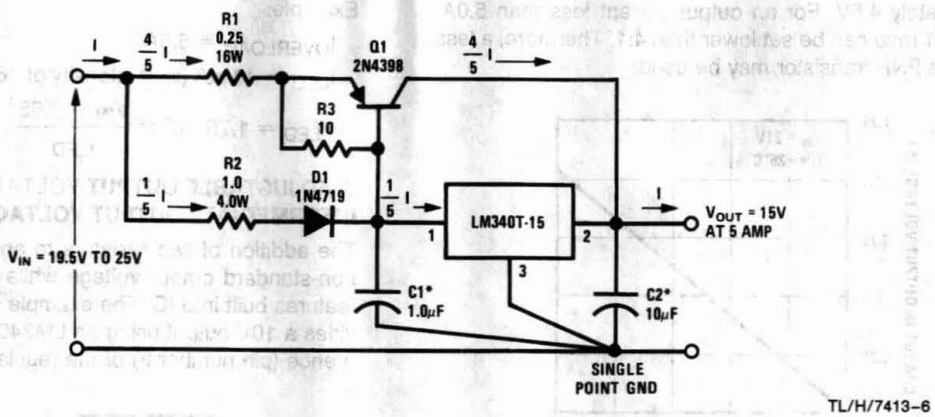
and the output impedance for a 0 to 85Ω change in Z_L using equation 2-4 is:

$$Z_{OUT} = \frac{1}{55\ \mu A + \frac{2\text{ mV}}{25\Omega}} = 7.4\ k\Omega \quad (2\text{-}8)$$

Typical measured values of Z_{OUT} varied from 10–12.3 kΩ, or 81–100 μA/V change input or output (approximately 0.05%/V).

3. HIGH CURRENT REGULATOR WITH SHORT CIRCUIT CURRENT LIMIT

The 15V regulator circuit of *Figure 6* includes an external boost transistor to increase output current capability to 5.0A. Unlike the normal boosting methods, it maintains the LM340's ability to provide short circuit current limiting and thermal shut-down without use of additional active components. The extension of these safety features to the external pass transistor Q1 is based on a current sharing scheme



*Solid tantalum

Note 1: Current sharing between the LM340 and Q1 allows the extension of short circuit current limit, safe operating area protection, and (assuming Q1's heat sink has four or more times the capacity of the LM340 head sink) thermal shutdown protection.

Note 2: $I_{SHORT\ CIRCUIT}$ is approximately 5.5 amp.

Note 3: $I_{OUT\ MAX}$ at V_{OUT} = 15V is approximately 9.5 amp.

FIGURE 6. 15V 5.0A Regulator with Short Circuit Current Limit

using R1, R2, and D1. Assuming the base-to-emitter voltage of Q1 and the voltage drop across D1 are equal, the voltage drops across R1 and R2 are equal. The currents through R1 and R2 will then be inversely proportional to their resistances. For the example shown on *Figure 6*, resistor R1 will have four times the current flow of R2. For reasonable values of Q1 beta, the current through R1 is approximately equal to the collector current of Q1; and the current through R2 is equal to the current flowing through the LM340. Therefore, under overload or short circuit conditions the protection circuitry of the LM340 will limit its own output current and, because of the R1/R2 current sharing scheme, the output current of Q1 as well. Thermal overload protection also extends Q1 when its heat sink has four or more times the capacity of the LM340 heat sink. This follows from the fact that both devices have approximately the same input/output voltage and share the load current in a ratio of four to one.

The circuit shown on *Figure 6* normally operates at up to 5.0A of output current. This means up to 1.0A of current flows through the LM340 and up to 4.0A flows through Q1. For short term overload conditions the curve of *Figure 7* shows the maximum instantaneous output current versus temperature for the boosted regulator. This curve reflects the approximately 2.0A current limit of the LM340 causing an 8.0A current limit in the pass transistor, or 10A, total.

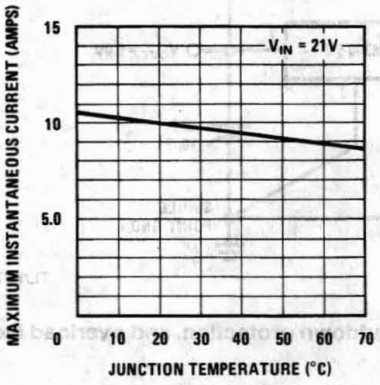


FIGURE 7. Maximum Instantaneous Current vs Junction Temperature

Under continuous short circuit conditions the LM340 will heat up and limit to a steady total state short circuit current of 4.0A to 6.0A as shown in *Figure 8*. This curve was taken using a Wakefield 680-75 heat sink (approximately 7.5°C/W) at a 25°C ambient temperature.

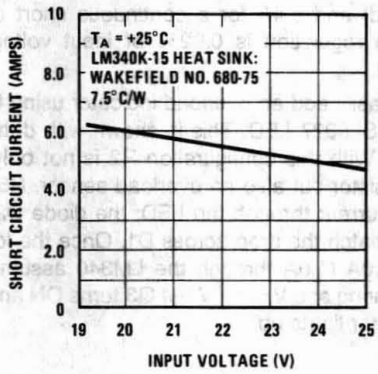
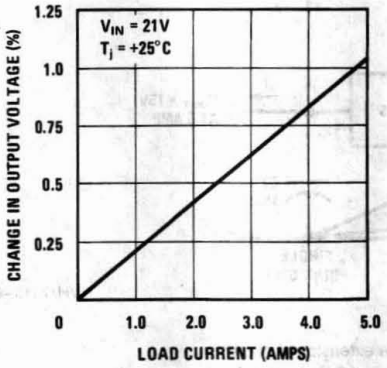


FIGURE 8. Continuous Short Circuit Current vs Input Voltage

For optimum current sharing over temperature between the LM340 and Q1, the diode D1 should be physically located close to the pass transistor on the heat sink in such a manner as to keep it at the same temperature as that of Q1. If the LM340 and Q1 are mounted on the same heat sink the LM340 should be electrically isolated from the heat sink since its case (pin 3) is at ground potential and the case of Q1 (its collector) is at the output potential of the regulator. Capacitors C1 and C2 are required to prevent oscillations and improve the output impedance respectively. Resistor R3 provides a path to unload excessive base charge from the base of Q1 when the regulator goes suddenly from full load to no load. The single point ground system shown on *Figure 6* allows the sense pins (2 and 3) of the LM340 to monitor the voltage directly at the load rather than at some point along a (possibly) resistive ground return line carrying up to 5.0A of load current. *Figure 9* shows the typical variation of load regulation versus load current for the boosted regulator. The insertion of the external pass transistor increases the input/output differential voltage from 2.0V to

approximately 4.5V. For an output current less than 5.0A, the R2/R1 ratio can be set lower than 4:1. Therefore, a less expensive PNP transistor may be used.



TL/H/7413–9

FIGURE 9. Load Regulation

4. 5.0V, 5.0A VOLTAGE REGULATOR FOR TTL

The high current 5.0V regulator for TTL shown in *Figure 10* uses a relatively inexpensive NPN pass transistor with a lower power PNP device to replace the single, higher cost, power PNP shown in *Figure 6*. This circuit provides a 5.0V output at up to 5.0A of load current with a typical load regulation of 1.8% from no load to full load. The peak instantaneous output current observed was 10.4A at a 25°C junction temperature (pulsed load with a 1.0 ms ON and a 200 ms OFF period) and 8.4A for a continuous short circuit. The typical line regulation is 0.02% of input voltage change (I_{OUT} = 0).

One can easily add an overload indicator using the National's new NSL5027 LED. This is shown with dotted lines in *Figure 10*. With this configuration R2 is not only a current sharing resistor but also an overload sensor. R5 will determine the current through the LED; the diode D2 has been added to match the drop across D1. Once the load current exceeds 5.0A (1.0A through the LM340 assuming perfect current sharing and $V_{D1} = V_{D2}$) Q3 turns ON and the overload indicator lights up.

Example:

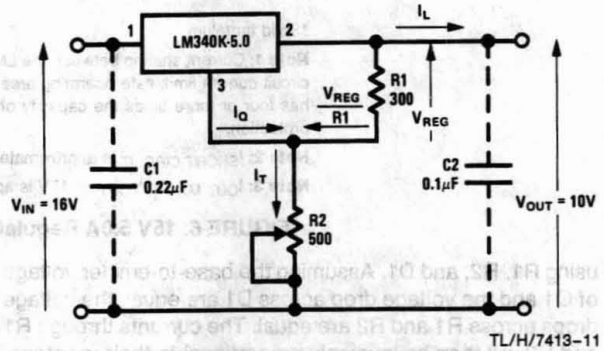
$I_{OVERLOAD}$ = 5.0A

I_{LED} = 40 mA (light intensity of 16 mcd)

$$V_{LED} = 1.75,\ R5 \cong \frac{V_{IN} - 2.65}{I_{LED}} \qquad (4\text{-}1)$$

5. ADJUSTABLE OUTPUT VOLTAGE REGULATOR FOR INTERMEDIATE OUTPUT VOLTAGES

The addition of two resistors to an LM340 circuit allows a non-standard output voltage while maintaining the limiting features built into IC. The example shown in *Figure 11* provides a 10V output using an LM340K-5.0 by raising the reference (pin number 3) of the regulator by 5.0V.

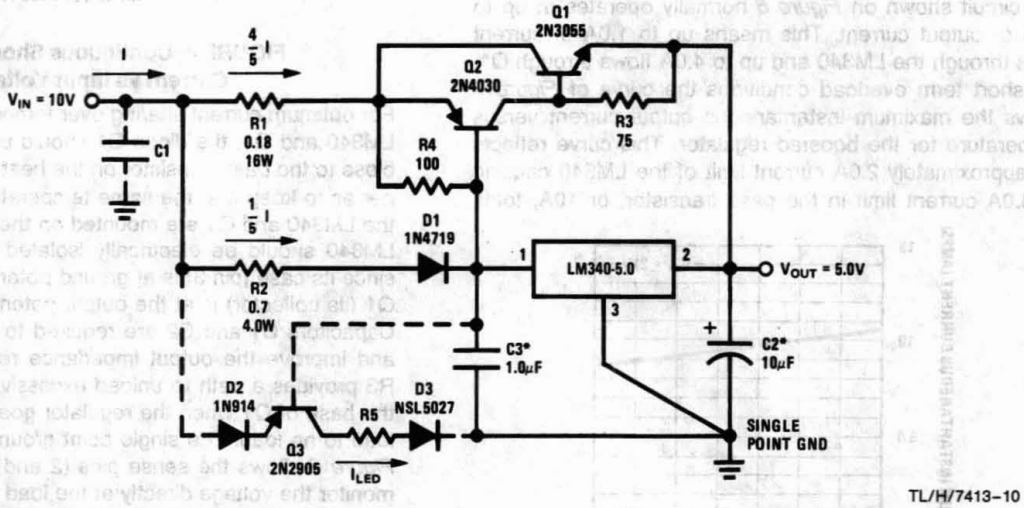


TL/H/7413–11

FIGURE 11. 10V Regulator

The 5.0V pedestal results from the sum of regulator quiescent current I_Q and a current equal to $V_{REG}/R1$, flowing through potenteniometer R2 to ground. R2 is made adjustable to compensate for differences in I_Q and V_{REG} output. The circuit is practical because the change in I_Q due to line voltage and load current changes is quite small.

The line regulation for the boosted regulator is the sum of the LM340 line regulation, its effects on the current through



TL/H/7413–10

*Solid tantalum

FIGURE 10. 5.0V, 5.0A Regulator for TTL (with short circuit, thermal shutdown protection, and overload indicator)

R2, and the effects of ΔI_Q in response to input voltage changes. The change in output voltage is:

$$\Delta V_{OUT} = (L_r/V)\,\Delta V_{IN} + \frac{(L_r/V)\,\Delta V_{IN}\,R2}{R1} + (Q_{CC}/V)\,\Delta V_{IN}\,R2 \quad (5\text{-}1)$$

giving a total line regulation of:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = (L_r/V)\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/V)\,R2 \quad (5\text{-}2)$$

The LM340-5.0 data sheet lists $\Delta V_{OUT} < 50$ mV and $\Delta I_Q < 1.0$ mA for $\Delta V_{IN} = 18V$ at $I_{OUT} = 500$ mA. This is:

$$L_r/V = \frac{50\text{ mV}}{18V} \approx 3\text{ mV/V} \quad (5\text{-}3)$$

$$Q_{CC}/V = \frac{1.0\text{ mA}}{18V} = 55\ \mu\text{A/V} \quad (5\text{-}4)$$

The worst case at line regulation for the circuit of *Figure 11* calculated by equation 5-2, $I_{OUT} = 500$ mA and R2 = 310Ω is:

$$\frac{\Delta V_{OUT}}{1.0V} = 3\text{ mV/V}\left(1 + \frac{310\Omega}{300\Omega}\right) + (55\ \mu\text{A/V})\,310\Omega \quad (5\text{-}5)$$

$$\frac{\Delta V_{OUT}}{1.0V} = 6\text{ mV/V} + 17\text{ mV/V} = 23\text{ mV/V} \quad (5\text{-}6)$$

This represents a worst case line regulation value of 0.23%/V.

The load regulation is the sum of the LM340 voltage regulation, its effect on the current through R2, and the effect of ΔI_Q in response to changes in load current. Using the following definitions and the notation shown on *Figure 11* ΔV_{OUT} is:

Z_{OUT} = Regulator output impedance: the change in output voltage per amp of load current change.

Z_{340} = LM340 output impedance

Q_{CC}/A = Quiescent current change per amp of load current change

$$\Delta V_{OUT} = (Z_{340})\,\Delta I_L + \frac{(Z_{340})}{R1}\,\Delta I_L\,R2 + (Q_{CC}/A)\,\Delta I_L\,R2 \quad (5\text{-}7)$$

and the total output impedance is:

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_L} = Z_{340}\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/A)\,R2 \quad (5\text{-}8)$$

The LM340-5.0 data sheet gives a maximum load regulation $L_r = 50$ mV and $\Delta I_Q = 1.0$ mA for a 1.0A load change.

$$Z_{340} = \frac{50\text{ mV}}{1.0A} = 0.05\Omega \quad (5\text{-}9)$$

$$Q_{CC}/A = \frac{1\text{ mA}}{1.0A} = 100\ \mu\text{A/A} \quad (5\text{-}10)$$

This gives a worst case dc output impedance (ac output impedance being a function of C2) for the 10V regulator using equation 5-8 of:

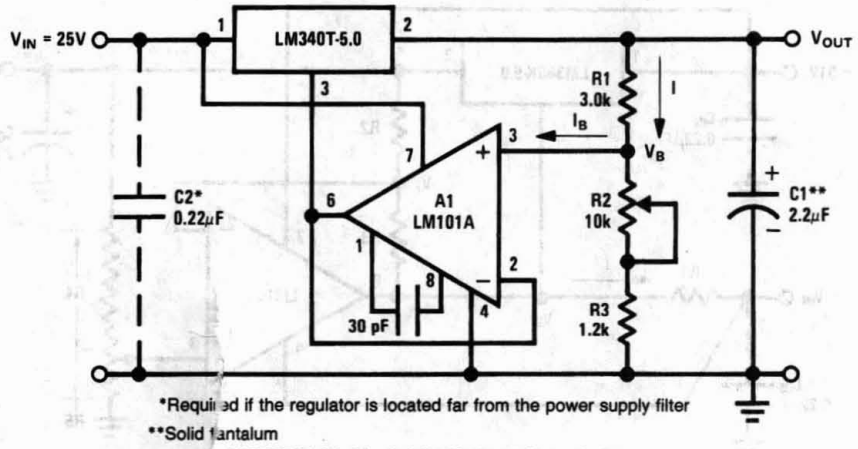
$$Z_{OUT} = 0.05\Omega\left(1 + \frac{310\Omega}{300\Omega}\right) + (100\ \mu\text{A/A})\,310\Omega \quad (5\text{-}11)$$

$$Z_{OUT} = 0.10\Omega + 0.031\Omega = 0.13\Omega$$

or a worst case change of approximately 1.5% for a 1.0A load change. Typical measured values are about one-third of the worst case value.

6. VARIABLE OUTPUT REGULATOR

In *Figure 12* the ground terminal of the regulator is "lifted" by an amount equal to the voltage applied to the non-inverting input of the operational amplifier LM101A. The output



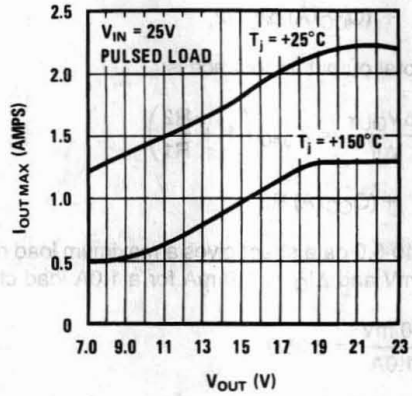
*Required if the regulator is located far from the power supply filter

**Solid tantalum

TL/H/7413–12

FIGURE 12. Variable Output Regulator

voltage of the regulator is therefore raised to a level set by the value of the resistive divider R1, R2, R3 and limited by the input voltage. With the resistor values shown in *Figure 12*, the output voltage is variable from 7.0V to 23V and the maximum output current (pulsed load) varies from 1.2A to 2.0A (T_j = 25°C) as shown in *Figure 13*.



TL/H/7413–13

FIGURE 13. Maximum Output Current

Since the LM101A is operated with a single supply (the negative supply pin is grounded). The common mode voltage V_B must be at least at a 2.0 V_{BE} + V_{SAT} above ground. R3 has been added to insure this when R2 = 0. Furthermore the bias current I_B of the operational amplifier should be negligible compared to the current flowing through the resistive divider.

Example:

V_{IN} = 25V

$V_{OUT\ MIN}$ = 5 + V_B, (R2 = 0),
V_B = R3 (I − I_B) = 2.0V
R1 = 2.5 R3

$V_{OUT\ MAX}$ = V_{IN} − dropout volt.
(R2 = $R2_{MAX}$)
$R2_{MAX}$ = 3.3 R1

So setting R3, the values of R1 and R2 can be determined.

If the LM324 is used instead of the LM101A, R3 can be omitted since its common mode voltage range includes the ground, and then the output will be adjustable from 5 to a certain upper value defined by the parameters of the system.

The circuit exhibits the short-circuit protection and thermal shutdown properties of the LM340 over the full output range.

The load regulation can be predicted as:

$$\Delta V_{OUT} = \frac{R1 + R2 + R3}{R1} \Delta V_{340} \qquad (6\text{-}1)$$

where ΔV_{340} is the load regulation of the device given in the data sheet. To insure that the regulator will start up under full load a reverse biased small signal germanium diode, 1N91, can be added between pins 2 and 3.

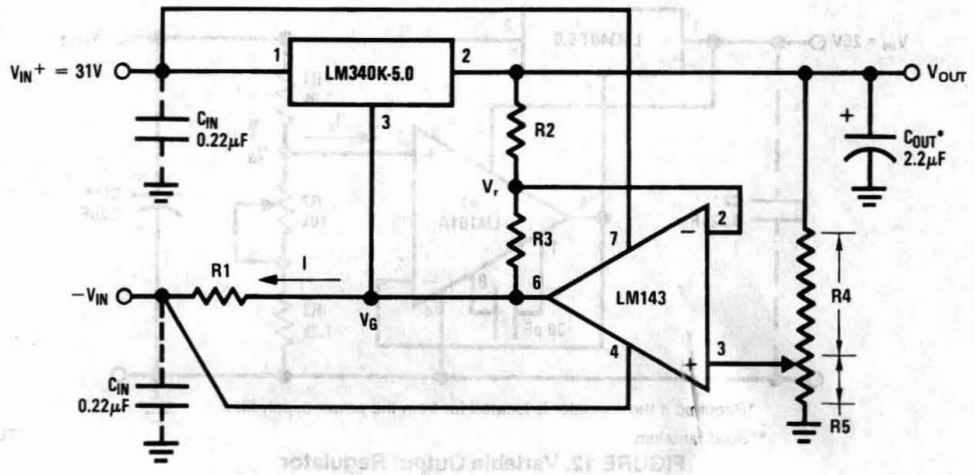
7. VARIABLE OUTPUT REGULATOR 0.5V–29V

When a negative supply is available an approach equivalent to that outlined in section 6 may be used to lower the minimum output voltage of the regulator below the nominal voltage that of the LM340 regulator device. In *Figure 14* the voltage V_G at the ground pin of the regulator is determined by the drop across R1 and the gain of the amplifier. The current I may be determined by the following relation:

$$I = \frac{V_{340}}{R1} \frac{R2\,R5 - R3\,R4}{R4\,(R2 + R3)} + \frac{V_{IN}^-}{R1} \qquad (7\text{-}1)$$

or if R2 + R3 = R4 + R5 = R

$$I = \frac{V_{340}\,R2}{R1\,R4} + \frac{1}{R1}(V_{IN}^- - V_{340}) \qquad (7\text{-}2)$$



TL/H/7413–14

*Solid tantalum

FIGURE 14. Variable Output Voltage 0.5V − 30V

considering that the output is given by:

$$V_{OUT} = V_G + V_{340} \quad (7\text{-}3)$$

and

$$V_G = R1\ I - V_{IN}^- \quad (7\text{-}4)$$

combining 7-2, 7-3, 7-4 an expression for the output voltage is:

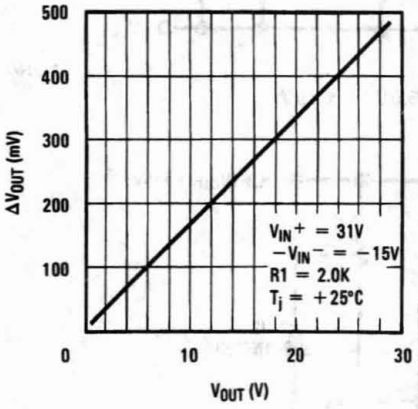
$$V_{OUT} = V_{340}\frac{R2}{R4} \quad (7\text{-}5)$$

Notice that the output voltage is inversely proportional to R4 so the output voltage may be adjusted very accurately for low values. A minimum output of 0.5V has been set. This implies that

$$\frac{R2}{R4} = 0.1\frac{R3}{R4} = 0.9\frac{R3}{R2} = 9 \quad (7\text{-}6)$$

An absolute zero output voltage will require R4 = ∞ or R2 = 0, neither being practical in this circuit. The maximum output voltage as shown in *Figure 14* is 30V if the high voltage operational amplifier LM143 is used. If only low values of V_{OUT} are sought, then an LM101 may be used. R1 can be computed from:

$$R1 = \frac{V_{IN}^-}{I_{Q340}} \quad (7\text{-}7)$$



TL/H/7413–15

FIGURE 15. Typical Load Regulation for a 0.5V−30V Regulator (ΔI_{OUT} = 1.0A)

Figure 15 illustrates the load regulation as a function of the output voltage.

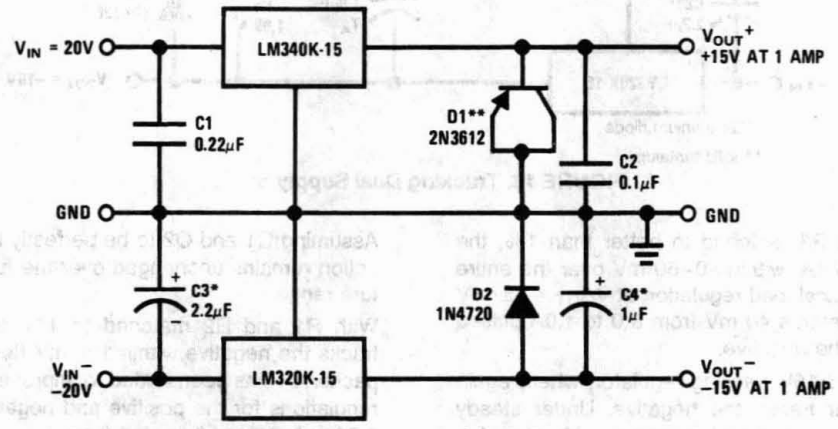
8. DUAL POWER SUPPLY

The plus and minus regulators shown in *Figure 16* will exhibit line and load regulations consistent with their specifications as individual regulators. In fact, operation will be entirely normal until the problem of common loads occurs. A 30Ω load from the +15V output to the −15V output (representing a 0.5A starting load for the LM340K-15 if the LM320K-15 is already started) would allow start up of the LM340 in most cases. To insure LM340 startup over the full temperature range into a worst case 1.0A current sink load the germanium power "diode" D1 has been added to the circuit. Since the forward voltage drop of the germanium diode D1 is less than that of the silicon substrate diode of the LM340 the external diode will take any fault current and allow the LM340 to start up even into a negative voltage load. D1 and silicon diode D2 also protect the regulator outputs from inadvertant shorts between outputs and to ground. For shorts between outputs the voltage difference between either input and the opposite regulator output should not exceed the maximum rating of the device.

The example shown in *Figure 16* is a symmetrical ±15V supply for linear circuits. The same principle applies to nonsymmetrical supplies such as a +5.0V and −12V regulator for applications such as registers.

9. TRACKING DUAL REGULATORS

In *Figure 17*, a fraction of the negative output voltage "lifts" the ground pins of the negative LM320K-15 voltage regulator and the LM340K-15 through a voltage follower and an inverter respectively. The dual operational amplifier LM1558 is used for this application and since its supply voltage may go as high as ±22V the regulator outputs may be set between 5.0V and 20V. Because of the tighter output tolerance and the better drift of the LM320, the positive regulator is made to track the negative. The best tracking action is achieved by matching the gain of both operational amplifiers, that is, the resistors R2 and R3 must be matched as closely as possible.



TL/H/7413–16

*Solid tantalum

**Germanium diode (using a PNP germanium transistor with the collector shorted to the emitter)

Note: C1 and C2 required if regulators are located far from power supply filter.

FIGURE 16. Dual Power Supply

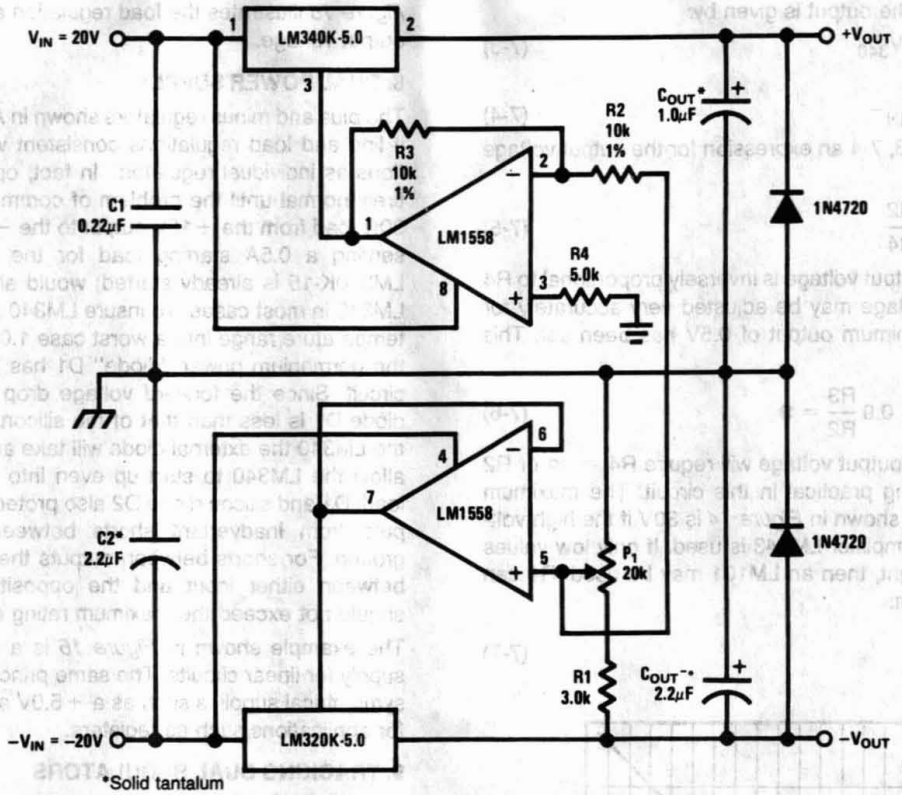


FIGURE 17. Tracking Dual Supply ±5.0V − ±18V

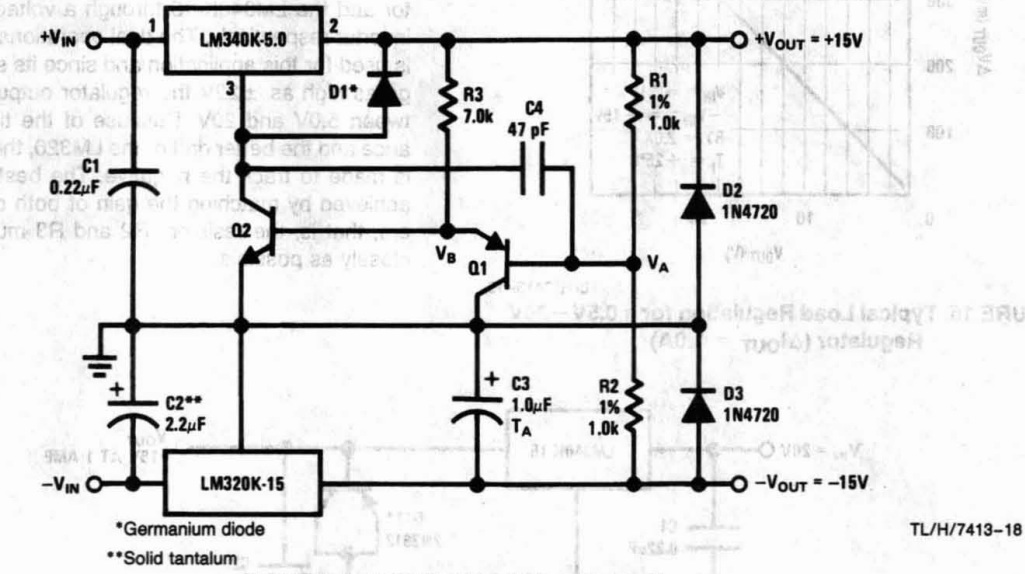


FIGURE 18. Tracking Dual Supply ±15V

Indeed, with R2 and R3 matched to better than 1%, the LM340 tracks the LM320 within 40–50 mV over the entire output range. The typical load regulation at V_{OUT} = ±15V for the positive regulator is 40 mV from a 0 to 1.0A pulsed load and 80 mV for the negative.

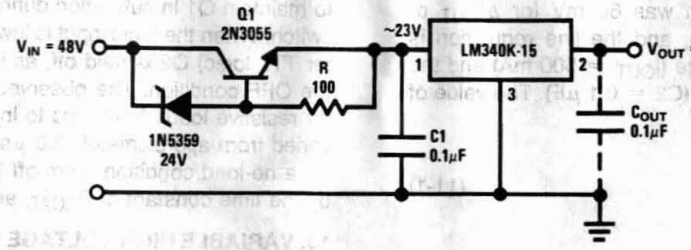
Figure 18 illustrates ±15V tracking regulator, where again the positive regulator tracks the negative. Under steady state conditions V_A is at a virtual ground and V_B at a V_{BE} above ground. Q2 then conducts the quiescent current of the LM340. If $-V_{OUT}$ becomes more negative the collector base junction of Q1 is forward biased thus lowering V_B and raising the collector voltage of Q2. As a result $+V_{OUT}$ rises and the voltage V_A again reaches ground potential.

Assuming Q1 and Q2 to be perfectly matched, the tracking action remains unchanged over the full operating temperature range.

With R1 and R2 matched to 1%, the positive regulator tracks the negative within 100 mV (less than 1%). The capacitor C4 has been added to improve stability. Typical load regulations for the positive and negative sides from a 0 to 1.0A pulsed load (t_{ON} = 1.0 ms, t_{OFF} = 200 ms) are 10 mV and 45 mV respectively.

10. HIGH INPUT VOLTAGE

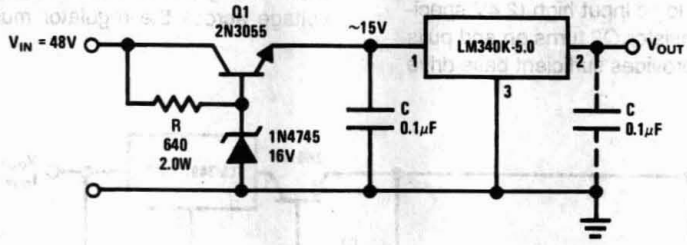
The input voltage of the LM340 must be kept within the limits specified in the data sheet. If the device is operated



TL/H/7413–19

*Heat sink Q1 and LM340

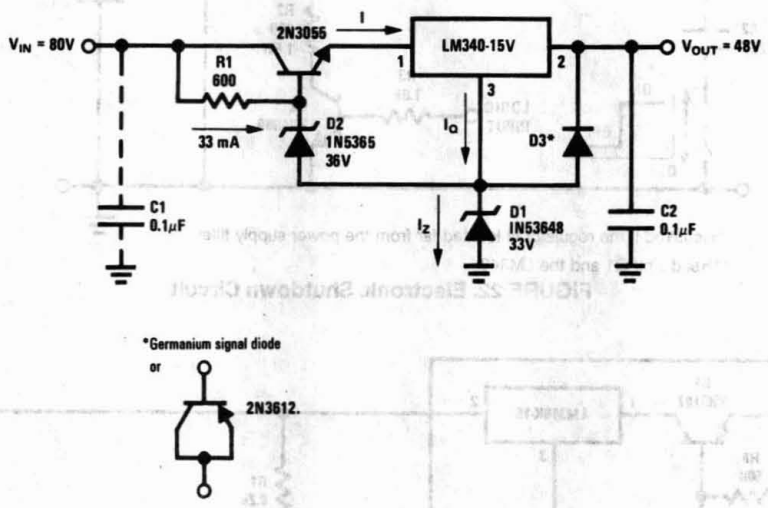
FIGURE 19. High Input Voltage



TL/H/7413–20

*Heat sink Q1 and LM340

FIGURE 20. High Input Voltage



TL/H/7413–21

FIGURE 21. High Voltage Regulator

above the absolute maximum input voltage rating, two failure modes may occur. With the output shorted to ground, the series pass transistor Q16 (see *Figure 4*) will go to avalanche breakdown; or, even with the output not grounded, the transistor Q1 may fail since it is operated with a collector-emitter voltage approximately 4.0V below the input.

If the only available supply runs at a voltage higher than the maximum specified, one of the simplest ways to protect the regulator is to connect a zener diode in series with the input of the device to level shift the input voltage. The drawback to this approach is obvious. The zener must dissipate ($V_{SUPPLY} - V_{IN\ MAX}$ LM340). (I_{OUTMAX}) which may be several watts. Another way to overcome the over voltage problem is illustrated in *Figure 19* where an inexpensive, NPN-zener-resistor, combination may be considered as an equivalent to the power zener. The typical load regulation of this circuit is 40 mV from 0 to 1.0A pulsed load (T_j = 25°C) and the line regulation is 2.0 mV for 1.0V variation in the input voltage (I_{OUT} = 0). A similar alternate approach is shown in *Figure 20*.

With an optional output capacitor the measured noise of the circuit was 700 μVp-p.

11. HIGH VOLTAGE REGULATOR

In previous sections the principle of "lifting the ground terminal" of the LM340, using a resistor divider or an operational amplifier, has been illustrated. One can also raise the output voltage by using a zener diode connected to the ground pin as illustrated in the *Figure 21* to obtain an output level increased by the breakdown voltage of the zener. Since the input voltage of the regulator has been allowed to go as high as 80V a level shifting transistor-zener (D2)—resistor combination has been added to keep the voltage across the LM340 under permissible values. The disadvantage of the system is the increased output noise and output voltage drift due to the added diodes.

Indeed it can be seen that, from no load to full load conditions, the ΔI_Z will be approximately the current through R1 (≅ 35 mA) and therefore the degraded regulation caused by D1 will be V_Z (at 35 mA + I_Q) − V_Z (at I_Q).

The measured load regulation was 60 mV for ΔI_{OUT} of 5.0 mA to 1.0A (pulsed load), and the line regulation is 0.01%V of input voltage change (I_{OUT} = 500 mA) and the typical output noise 2.0 mVp-p (C2 = 0.1 μF). The value of R1 is calculated as:

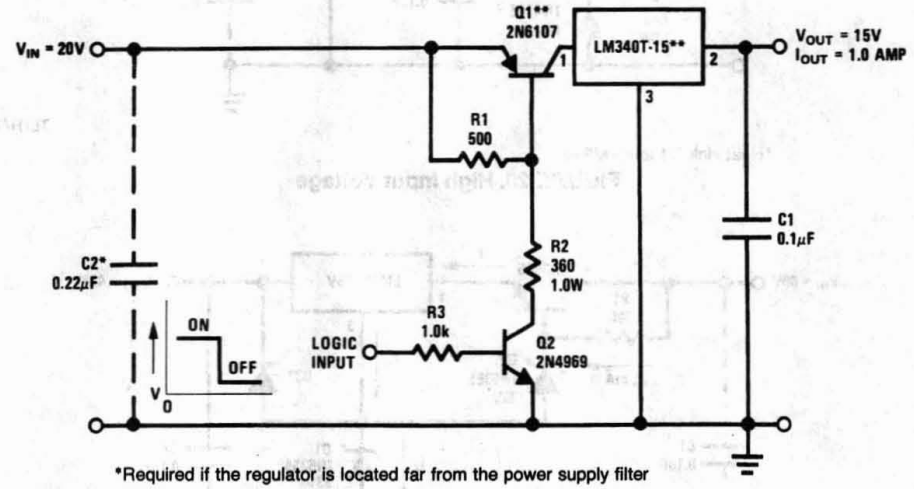
$$R1 \cong \beta\left[\frac{V_{IN} - (V_{Z1} + V_{Z2})}{I \text{ full load}}\right] \qquad (11\text{-}1)$$

12. ELECTRONIC SHUTDOWN

Figure 22 shows a practical method of shutting down the LM340 under the control of a TTL or DTL logic gate. The pass transistor Q1 operates either as a saturated transistor or as an open switch. With the logic input high (2.4V specified minimum for TTL logic) transistor Q2 turns on and pulls 50 mA down through R2. This provides sufficient base drive to maintain Q1 in saturation during the ON condition of the switch. When the logic input is low (0.4V specified maximum for TTL logic) Q2 is held off, as is Q1; and the switch is in the OFF condition. The observed turn-on time was 7.0 μs for resistive loads from 15Ω to infinity and the turn-off time varied from approximately 3.0 μs for a 15Ω load to 3.0 ms for a no-load condition. Turn-off time is controlled primarily by the time constant of R_{LOAD} and C1.

13. VARIABLE HIGH VOLTAGE REGULATOR WITH OVERVOLTAGE SHUTDOWN

A high voltage variable-output regulator may be constructed using the LM340 after the idea illustrated in section 7 and drawn in *Figure 23*. The principal inconvenience is that the voltage across the regulator must be limited to maximum

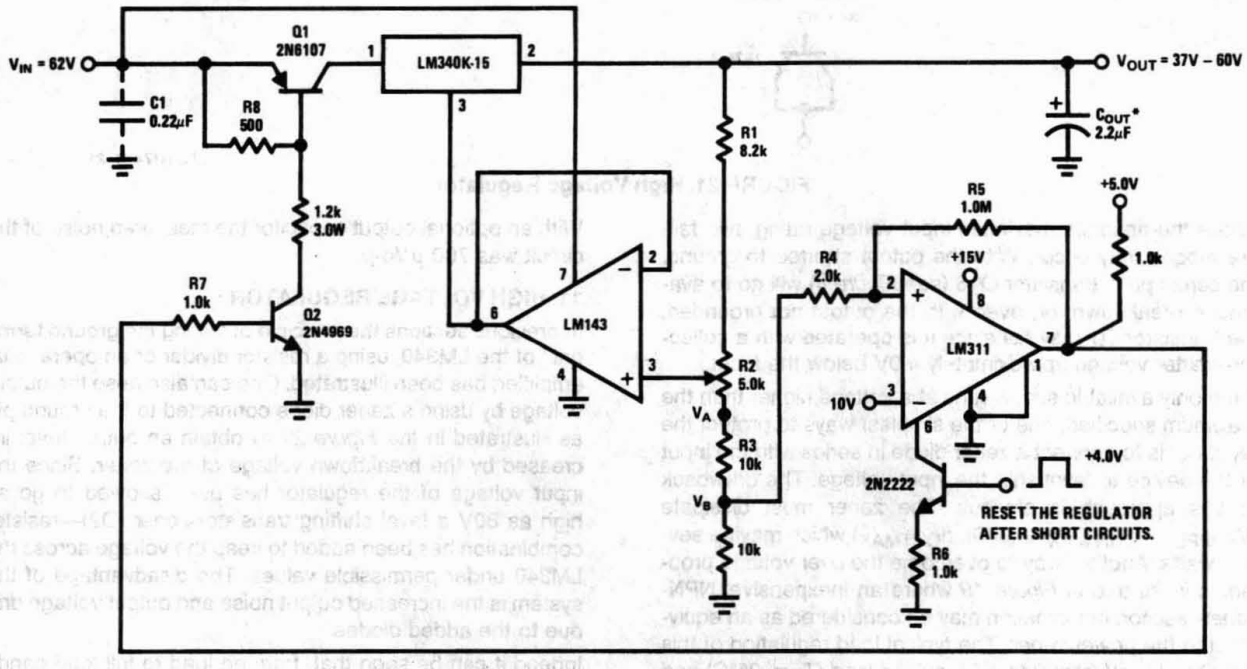


*Required if the regulator is located far from the power supply filter

**Head sink Q1 and the LM340

TL/H/7413–22

FIGURE 22. Electronic Shutdown Circuit



*Solid tantalum

TL/H/7413–23

FIGURE 23. Variable High Voltage Regulator with Shortcircuit and Overvoltage Protection

rating of the device, the higher the applied input voltage the higher must be lifted the ground pin of the LM340. Therefore the range of the variable output is limited by the supply voltage limit of the operational amplifier and the maximum voltage allowed across the regulator. An estimation of this range is given by:

$$V_{OUT\ MAX} - V_{OUT\ MIN} = V_{SUPPLY\ MAX340} - V_{NOMINAL340} - 2.0V \quad (13\text{-}1)$$

Examples:

LM340-15: $V_{OUTMAX} - V_{OUTMIN} = 35 - 15 - 2 = 18V$

Figure 23 illustrates the above considerations. Even though the LM340 is by itself short circuit protected, when the output drops, also V_A drops and the voltage difference across the device increases. If it exceeds 35V the pass transistor internal to the regulator will breakdown, as explained in section 11. To remedy this, an over-voltage shutdown is included in the circuit. When the output drops the comparator switches low, pulls down the base Q2 thus opening the switch Q1, and shutting down the LM340. Once the short circuit has been removed the LM311 must be activated through the strobe to switch high and close Q1, which will start the regulator again. The additional voltages required to operate the comparator may be taken from the 62V since the LM311 has a certain ripple rejection and the reference voltage (pin 3) may have a superimposed small ac signal. The typical load regulation can be computed from equation 6-1.

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1. AN-42: *"IC Provides on Card Regulation for Logic Circuits."*

2. Carl T. Nelson: *"Power distribution and regulation can be simple, cheap and rugged."* EDN, February 20, 1973.

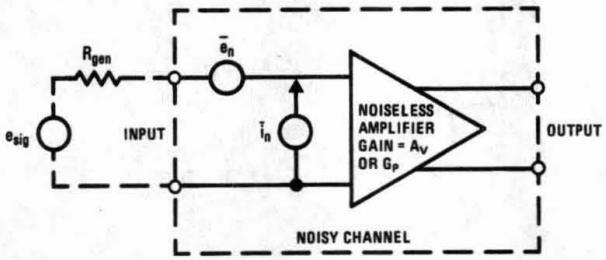
Noise Specs Confusing?

National Semiconductor
Application Note 104

It's really all very simple—once you understand it. Then, here's the inside story on noise for those of us who haven't been designing low noise amplifiers for ten years.

You hear all sorts of terms like signal-to-noise ratio, noise figure, noise factor, noise voltage, noise current, noise power, noise spectral density, noise per root Hertz, broadband noise, spot noise, shot noise, flicker noise, excess noise, I/F noise, fluctuation noise, thermal noise, white noise, pink noise, popcorn noise, bipolar spike noise, low noise, no noise, and loud noise. No wonder not everyone understands noise specifications.

In a case like noise, it is probably best to sort it all out from the beginning. So, in the beginning, there was noise; and then there was signal. The whole idea is to have the noise very small compared to the signal; or, conversely, we desire a high signal-to-noise ratio S/N. Now it happens that S/N is related to noise figure NF, noise factor F, noise power, noise voltage $\bar{e}_n$, and noise current $\bar{i}_n$. To simplify matters, it also happens that any noisy channel or amplifier can be completely specified for noise in terms of two noise generators $\bar{e}_n$ and $\bar{i}_n$ as shown in *Figure 1.*



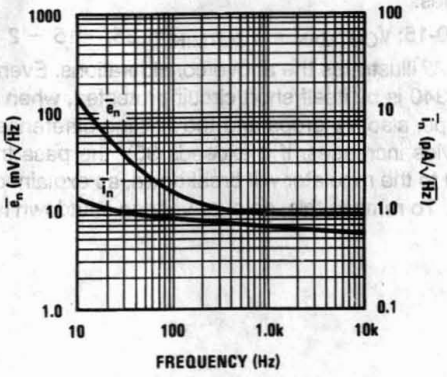
TL/H/7414–1

FIGURE 1. Noise Characterization of Amplifier

All we really need to understand are NF, $\bar{e}_n$, and $\bar{i}_n$. So here is a rundown on these three.

NOISE VOLTAGE, $\bar{e}_n$, or more properly, EQUIVALENT SHORT-CIRCUIT INPUT RMS NOISE VOLTAGE is simply that noise voltage which would appear to originate at the input of the noiseless amplifier if the input terminals were shorted. It is expressed in nanovolts per root Hertz $nV/\sqrt{Hz}$ at a specified frequency, or in microvolts in a given frequency band. It is determined or measured by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristic is used in measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$ if data is to be expressed per unit bandwidth or per root Hertz. The level of $\bar{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in *Figure 2.* This increase is 1/f NOISE.

NOISE CURRENT, $\bar{i}_n$, or more properly, EQUIVALENT OPEN-CIRCUIT RMS NOISE CURRENT is that noise which



TL/H/7414–2

FIGURE 2. Noise Voltage and Current for an Op Amp

occurs apparently at the input of the noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz $pA/\sqrt{Hz}$ at a specified frequency or in nanoamps in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional noise voltage which is $\bar{i}_n \times R_{in}$ (or X_{cin}). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\bar{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the input, there is only $\bar{e}_n$ and $\bar{i}_n X_{cin}$. The $\bar{i}_n$ is measured with a bandpass filter and converted to $pA\sqrt{Hz}$ if appropriate; typically it increases at lower frequencies for op amps and bipolar transistors, but increases at higher frequencies for field-effect transistors.

NOISE FIGURE, NF is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \text{ Log} \frac{(S/N)_{in}}{(S/N)_{out}} \quad (1)$$

where: S and N are power or (voltage)^2 levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of R_{gen} and any X_{gen} as well as frequency must be known to properly express NF in meaningful terms. This is because the amplifier $\bar{i}_n \times Z_{gen}$ as well as R_{gen} itself produces input noise. The signal source in *Figure 1* contains some noise. However e_{sig} is generally considered to be noise free and input noise is present as the THERMAL NOISE of the resistive component of the signal generator impedance R_{gen}. This thermal noise is WHITE in nature as it contains constant NOISE POWER DENSITY per unit bandwidth. It is easily seen from Equation 2 that the $\overline{e_n^2}$ has the units V^2/Hz and that $(\bar{e}_n)$ has the units $V/\sqrt{Hz}$

$$\overline{e_{R^2}} = 4kTRB \quad (2)$$

where: T is the temperature in °K

R is resistor value in Ω

B is bandwidth in Hz

k is Boltzman's constant

RELATION BETWEEN $\bar{e}_n$, $\bar{i}_n$, NF

Now we can examine the relationship between $\bar{e}_n$ and $\bar{i}_n$ at the amplifier input. When the signal source is connected, the $\bar{e}_n$ appears in series with the e_{sig} and $\bar{e}_R$. The $\bar{i}_n$ flows through R_{gen} thus producing another noise voltage of value $\bar{i}_n \times R_{gen}$. This noise voltage is clearly dependent upon the value of R_{gen}. All of these noise voltages add at the input in rms fashion; that is, as the square root of the sum of the squares. Thus, neglecting possible correlation between $\bar{e}_n$ and $\bar{i}_n$, the total input noise is

$$\overline{e_N^2} = \overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2 \qquad (3)$$

Further examination of the NF equation shows the relationship of $\bar{e}_N$, $\bar{i}_n$, and NF.

$$NF = 10 \log \frac{S_{in} \times N_{out}}{S_{out} \times N_{in}}$$

$$= 10 \log \frac{S_{in}\, G_p\, \overline{e_N^2}}{S_{in}\, G_p\, \overline{e_R^2}}$$

where: G_p = power gain

$$= 10 \log \frac{\overline{e_N^2}}{\overline{e_R^2}}$$

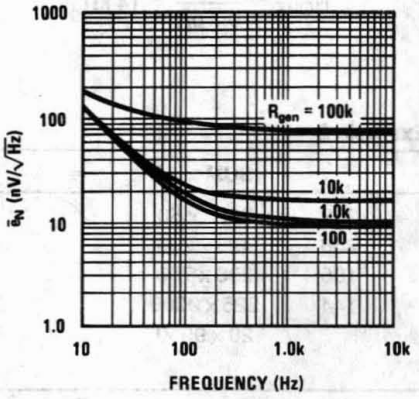
$$= 10 \log \frac{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2}{\overline{e_R^2}}$$

$$NF = 10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2}\, R_{gen}^2}{\overline{e_R^2}}\right) \qquad (4)$$

Thus, for small R_{gen}, noise voltage dominates; and for large R_{gen}, noise current becomes important. A clear advantage accrues to FET input amplifiers, especially at high values of R_{gen}, as the FET has essentially zero $\bar{i}_n$. Note, that for an NF value to have meaning, it must be accompanied by a value for R_{gen} as well as frequency.

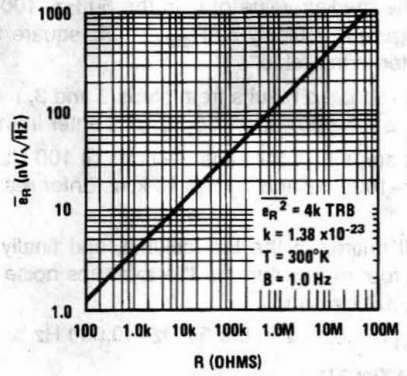
CALCULATING TOTAL NOISE, $\bar{e}_N$

We can generate a plot of $\bar{e}_N$ for various values of R_{gen} if noise voltage and current are known vs frequency. Such a graph is shown in *Figure 3* drawn from *Figure 2*. To make this plot, the thermal noise $\bar{e}_R$ of the input resistance must be calculated from Equation 2 or taken from the graph of *Figure 4*. Remember that each term in Equation 3 must be squared prior to addition, so the data from *Figure 4* and from *Figure 2* is squared. A sample of this calculation follows:



TL/H/7414–3

FIGURE 3. Total Noise for the Op Amp of *Figure 2*



TL/H/7414–4

FIGURE 4. Thermal Noise of Resistor

Example 1: Determine total equivalent input noise per unit bandwidth for an amplifier operating at 1 kHz from a source resistance of 10 kΩ. Use the data from *Figures 2* and *4*.

1. Read $\bar{e}_R$ from *Figure 4* at 10 kΩ; the value is 12.7 nV/√Hz.
2. Read $\bar{e}_n$ from *Figure 2* at 1 kHz; the value is 9.5 nV/√Hz.
3. Read $\bar{i}_n$ from *Figure 2* at 1 kHz; the value is 0.68 pA/√Hz. Multiply by 10 kΩ to obtain 6.8 nV/√Hz.
4. Square each term individually, and enter into Equation 3.

$$\bar{e}_N = \sqrt{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2}$$

$$= \sqrt{9.5^2 + 12^2 + 6.8^2} \qquad = \sqrt{279}$$

$$\bar{e}_N = 17.4 \text{ nV}/\sqrt{\text{Hz}}$$

This is total rms noise at the input in one Hertz bandwidth at 1 kHz. If total noise in a given bandwidth is desired, one must integrate the noise over a bandwidth as specified. This is most easily done in a noise measurement set-up, but may be approximated as follows:

1. If the frequency range of interest is in the flat band; i.e., between 1 kHz and 10 kHz in *Figure 2*, it is simply a matter of multiplying $\bar{e}_N$ by the square root of the bandwidth. Then, in the 1 kHz–10 kHz band, total noise is

$$\bar{e}_N = 17.4\sqrt{9000}$$

$$= 1.65\ \mu V$$

2. If the frequency band of interest is not in the flat band of *Figure 2*, one must break the band into sections, calculating average noise in each section, squaring, multiplying by section bandwidth, summing all sections, and finally taking square root of the sum as follows:

$$\bar{e}_N = \sqrt{\overline{e_R^2} B + \sum_1^i (\overline{e_n^2} + \overline{i_n^2}\, R_{gen}^2)_i\, B_i} \qquad (5)$$

where: i is the total number of sub-blocks.

For most purposes a sub-block may be one or two octaves. Example 2 details such a calculation.

Example 2: Determine the rms noise level in the frequency band 50 Hz to 10 kHz for the amplifier of *Figure 2* operating from R_{gen} = 2k.

1. Read $\bar{e}_R$ from *Figure 4* at 2k, square the value, and multiply by the entire bandwidth. Easiest way is to construct a table as shown on the next page.
2. Read the median value of $\bar{e}_n$ in a relatively small frequency band, say 50 Hz–100 Hz, from *Figure 2*, square it and enter into the table.

3. Read the median value of $\bar{i}_n$ in the 50 Hz–100 Hz band from *Figure 2*, multiply by R_{gen} = 2k, square the result and enter in the table.
4. Sum the squared results from steps 2 and 3, multiply the sum by Δf = 100–50 = 50 Hz, and enter in the table.
5. Repeat steps 2–4 for band sections of 100 Hz–300 Hz, 300 Hz–1000 Hz and 1 kHz–10 kHz. Enter results in the table.
6. Sum all entires in the last column, and finally take the square root of this sum for the total rms noise in the 50 Hz–10,000 Hz band.
7. Total $\bar{e}_n$ is 1.62 μV in the 50 Hz–10,000 Hz band.

CALCULATING S/N and NF

Signal-to-noise ratio can be easily calculated from known signal levels once total rms noise in the band is determined. Example 3 shows this rather simple calculation from Equation 6 for the data of Example 2.

$$S/N = 20 \log \frac{e_{sig}}{\bar{e}_N} \quad (6)$$

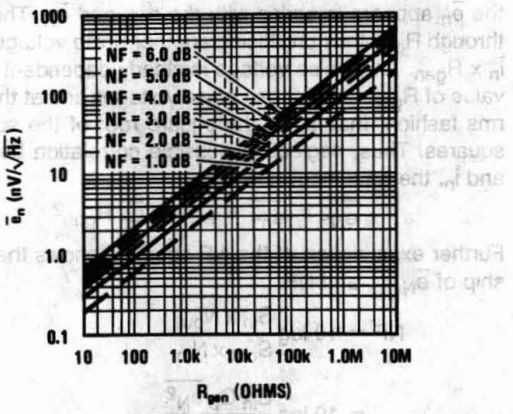
Example 3: Determine S/N for an rms e_{sig} = 4 mV at the input to the amplifier operated in Example 2.

1. RMS signal is e_{sig} = 4 mV
2. RMS noise from Example 2 is 1.62 μV
3. Calculate S/N from Equation 6

$$S/N = 20 \log \frac{4\ mV}{1.62\ \mu V}$$

$$= 20 \log (2.47 \times 10^3)$$
$$= 20 (\log 10^3 + \log 2.47)$$
$$= 20 (3 + 0.393)$$
$$S/N = 68\ dB$$

It is also possible to plot NF vs frequency at various R_{gen} for any given plot of $\bar{e}_n$ and $\bar{i}_n$. However there is no specific all-purpose conversion plot relating NF, $\bar{e}_n$, $\bar{i}_n$, R_{gen} and f. If either $\bar{e}_n$ or $\bar{i}_n$ is neglected, a reference chart can be constructed. *Figure 5* is such a plot when only $\bar{e}_n$ is considered. It is useful for most op amps when R_{gen} is less than about 200Ω and for FETs at any R_{gen} (because there is no significant $\bar{i}_n$ for FETs), however actual NF for op amps with R_{gen} > 200Ω is higher than indicated on the chart. The graph of *Figure 5* can be used to find spot NF if $\bar{e}_n$ and R_{gen} are known, or to find $\bar{e}_n$ if NF and R_{gen} are known. It can also be used to find max R_{gen} allowed for a given max NF when $\bar{e}_n$ is known. In any case, values are only valid if $\bar{i}_n$ is negligible and at the specific frequency of interest for NF and $\bar{e}_n$, and for 1 Hz bandwidth. If bandwidth increases, the plot is valid so long as $\bar{e}_n$ is multiplied by $\sqrt{B}$.



TL/H/7414–5

FIGURE 5. Spot NF vs R_{gen} when Considering *Only* $\bar{e}_n$ and $\bar{e}_R$ (not valid when $\bar{i}_n$ R_{gen} is significant)

THE NOISE FIGURE MYTH

Noise figure is easy to calculate because the signal level need not be specified (note that e_{sig} drops out of Equation 4). Because NF is so easy to handle in calculations, many designers tend to lose sight of the fact that signal-to-noise ratio $(S/N)_{out}$ is what is important in the final analysis, be it an audio, video, or digital data system. One can, in fact, choose a high R_{gen} to reduce NF to near zero if $\bar{i}_n$ is very small. In this case $\bar{e}_R$ is the major source of noise, overshadowing $\bar{e}_n$ completely. The result is very low NF, but very low S/N as well because of very high noise. Don't be fooled into believing that low NF means low noise *per se*!

Another term is worth considering, that is optimum source resistance R_{OPT}. This is a value of R_{gen} which produces the lowest NF in a given system. It is calculated as

$$R_{OPT} = \frac{\bar{e}_n}{\bar{i}_n} \quad (7)$$

This has been arrived at by differentiating Equation 4 with respect to R_{gen} and equating it to zero (see Appendix). *Note that this does not mean lowest noise.*

For example, using *Figure 2* to calculate R_{OPT} at say 600 Hz,

$$R_{OPT} = \frac{10\ nV}{0.7\ pA} = 14\ k\Omega$$

TABLE I. Noise Calculations for Example 2

B (Hz)	Δf (Hz)	$\bar{e}_n^2$ (nV/Hz)	+ $\bar{i}_n^2 R_{gen}^2$			SUM x Δf	=	(nV²)
50–100	50	$(20)^2 = 400$	$(8.7 \times 2.0k)^2$	=	302	702* x 50		35,000
100–300	200	$(13)^2 = 169$	$(8 \times 2.0k)^2$	=	256	425 x 200		85,000
300–1000	700	$(10)^2 = 100$	$(7 \times 2.0k)^2$	=	196	296 x 700		207,000
1.0k–10k	9000	$(9)^2 = 81$	$(6 \times 2.0k)^2$	=	144	225 x 9000		2,020,000
50–10,000	9950	$\bar{e}_R^2 = (5.3)^2 = 28$				28 x 9950		279,000

Total $\bar{e}_N = \sqrt{2{,}626{,}000} = 1620\ nV = 1.62\ \mu V$

*The units are as follows: $(20\ nV/\sqrt{Hz})^2 = 400\ (nV)^2/Hz$

$(8.7\ pA/\sqrt{Hz} \times 2.0\ k\Omega)^2 = (17.4\ nA/\sqrt{Hz})^2 = 302\ (nV)^2/Hz$

Sum = 702 $(nV)^2$/Hz x 50 Hz = 35,000 $(nV)^2$

Then note in *Figure 3*, that $\bar{e}_N$ is in the neighborhood of 20 nV/$\sqrt{Hz}$ for R_{gen} of 14k, while $\bar{e}_N$ = 10 nV/$\sqrt{Hz}$ for R_{gen} = 0–100Ω. STOP! Do not pass GO. Do not be fooled. Using $R_{gen} = R_{OPT}$ does not guarantee lowest noise UNLESS $e_{sig}^2 = kR_{gen}$ as in the case of transformer coupling. When $e_{sig}^2 > kR_{gen}$, as is the case where signal level is proportional to R_{gen} ($e_{sig} = kR_{gen}$), it makes sense to use the highest practical value of R_{gen}. When $e_{sig}^2 < kR_{gen}$, it makes sense to use a value of $R_{gen} < R_{OPT}$. These conclusions are verified in the Appendix.

This all means that it does not make sense to tamper with the R_{gen} of existing signal sources in an attempt to make $R_{gen} = R_{OPT}$. Especially, do not add series resistance to a source for this purpose. It does make sense to adjust R_{gen} in transformer coupled circuits by manipulating turns ratio or to design R_{gen} of a magnetic pick-up to operate with preamps where R_{OPT} is known. It does make sense to increase the design resistance of signal sources to match or exceed R_{OPT} so long as the signal voltage increases with R_{gen} in at least the ratio $e_{sig}^2 \propto R_{gen}$. It does not necessarily make sense to select an amplifier with R_{OPT} to match R_{gen} because one amplifier operating at $R_{gen} = R_{OPT}$ may produce lower S/N than another (quieter) amplifier operating with $R_{gen} \neq R_{OPT}$.

With some amplifiers it is possible to adjust R_{OPT} over a limited range by adjusting the first stage operating current (the National LM121 and LM381 for example). With these, one might increase operating current, varying R_{OPT}, to find a condition of minimum S/N. Increasing input stage current decreases R_{OPT} as $\bar{e}_n$ is decreased and $\bar{i}_n$ is simultaneously increased.

Let us consider one additional case of a fairly complex nature just as a practical example which will point up some factors often overlooked.

Example 4: Determine the S/N *apparent to the ear* of the amplifier of *Figure 2* operating over 50-12,800 Hz when driven by a phonograph cartridge exhibiting R_{gen} = 1350Ω, L_{gen} = 0.5H, and average e_{sig} = 4.0 mVrms. The cartridge is to be loaded by 47k as in *Figure 6*. This is equivalent to using a Shure V15, Type 3 for average level recorded music.

1. Choose sectional bandwidths of 1 octave each, these are listed in the following table.
2. Read $\bar{e}_n$ from *Figure 2* as average for each octave and enter in the table.
3. Read $\bar{i}_n$ from *Figure 2* as average for each octave and enter in the table.
4. Read $\bar{e}_R$ for the R_{gen} = 1350Ω from *Figure 4* and enter in the table.
5. Determine the values of Z_{gen} at the midpoint of each octave and enter in the table.
6. Determine the amount of $\bar{e}_R$ which reaches the amplifier input; this is

$$\bar{e}_R \frac{R1}{R1 + Z_{gen}}$$

7. Read the noise contribution $\bar{e}_{47k}$ of R1 = 47k from *Figure 4*.
8. Determine the amount of $\bar{e}_{47K}$ which reaches the amplifier input; this is

$$\bar{e}_{47k} \frac{Z_{gen}}{R1 + Z_{gen}}$$

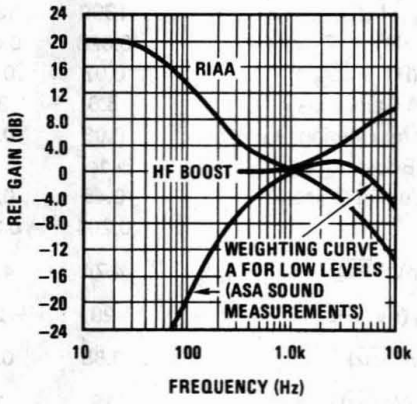


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FIGURE 7. Relative Gain for RIAA, ASA Weighting A, and H-F Boost Curves

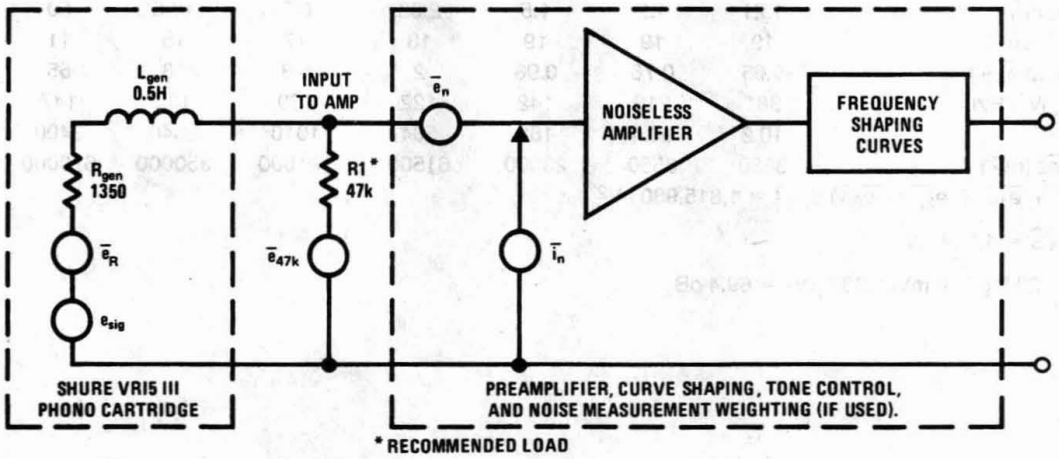

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FIGURE 6. Phono Preamp Noise Sources

9. Determine the effective noise contributed by $\bar{i}_n$ flowing through the parallel combination of R1 and Z_{gen}. This is
$$\bar{i}_n \frac{Z_{gen}\,R1}{Z_{gen} + R1}$$
10. Square all noise voltage values resulting from steps 2, 6, 8 and 9; and sum the squares.
11. Determine the relative gain at the midpoint of each octave from the RIAA playback response curve of *Figure 7*.
12. Determine the relative gain at these same midpoints from the A weighted response curve of *Figure 7* for sound level meters (this roughly accounts for variations in human hearing).
13. Assume a tone control high frequency boost of 10 dB at 10 kHz from *Figure 7*. Again determine relative response of octave midpoints.
14. Multiply all relative gain values of steps 11-13 and square the result.
15. Multiply the sum of the squared values from step 10 by the resultant relative gain of step 14 and by the bandwidth in each octave.
16. Sum all the values resultant from step 15, and find the square root of the sum. This is the total audible rms noise apparent in the band.
17. Divide e_{sig} = 4 mV by the total noise to find S/N = 69.4 dB.

STEPS FOR EXAMPLE

1	Frequency Band (Hz)	50–100	100–200	200–400	400–800	800–1600	1.6–3.2k	3.2–6.4k	6.4–12.8k
	Bandwidth, B (Hz)	50	100	200	400	800	1600	3200	6400
	Bandcenter, f (Hz)	75	150	300	600	1200	2400	4800	9600
5	Z_{gen} at f (Ω)	1355	1425	1665	2400	4220	8100	16k	32k
	Z_{gen} R1 (Ω)	1300	1360	1600	2270	3900	6900	11.9k	19k
	$Z_{gen}/R1 + Z_{gen})$	0.028	0.030	0.034	0.485	0.082	0.145	0.255	0.400
	$R1/(R1 + Z_{gen})$	0.97	0.97	0.97	0.95	0.92	0.86	0.74	0.60
11	RIAA Gain, A_{RIAA}	5.6	3.1	2.0	1.4	1	0.7	0.45	0.316
12	Corr for Hearing, A_A	0.08	0.18	0.45	0.80	1	1.26	1	0.5
13	H-F Boost, A_{boost}	1	1	1	1	1.12	1.46	2.3	3.1
14	Product of Gains, A	0.45	0.55	0.9	1.12	1.12	1.28	1.03	0.49
	A^2	0.204	0.304	0.81	1.26	1.26	1.65	1.06	0.241
4	$\bar{e}_R$ (nV/√Hz)	4.74	4.74	4.74	4.74	4.74	4.74	4.74	4.74
7	$\bar{e}_{47k}$ (nV/√Hz)	29	29	29	29	29	29	29	29
3	$\bar{i}_n$ (pA/√Hz)	0.85	0.80	0.77	0.72	0.65	0.62	0.60	0.60
2	$\bar{e}_n$ (nV/√Hz)	19	14	11	10	9.5	9	9	9
9	$\bar{e}_1 = \bar{i}_n (Z_{gen}\,R1)$	1.1	1.09	1.23	1.63	2.55	4.3	7.1	11.4
6	$\bar{e}_2 = \bar{e}_R\,R1/(R1 + Z_{gen})$	4.35	4.35	4.35	4.25	4.15	3.86	3.33	2.7
8	$\bar{e}_3 = \bar{e}_{47k}\,Z_{gen}/(R1 + Z_{gen})$	0.81	0.87	0.98	1.4	2.4	4.2	7.4	11.6
10	$\overline{e_n^2}$	360	195	121	100	90	81	81	81
	$\overline{e_1^2}$ (from $\bar{i}_n$)	1.21	1.2	1.5	2.65	6.5	18.5	50	150
	$\overline{e_2^2}$ (from $\bar{e}_R$)	19	19	19	18	17	15	11	7.2
	$\overline{e_3^2}$ (from $\bar{e}_{47k}$)	0.65	0.76	0.96	2	5.8	18	55	135
	$\Sigma\overline{e_n^2}$ (nV²/Hz)	381	216	142	122	120	133	147	373
15	BA^2 (Hz)	10.2	30.4	162	504	1010	2640	3400	1550
	$BA^2\Sigma\overline{e^2}$ (nV²)	3880	6550	23000	61500	121000	350000	670000	580000

16 $\Sigma(\overline{e_{n_i}^2} + \overline{e_{1_i}^2} + \overline{e_{2_i}^2} + \overline{e_{3_i}^2})\,B_iA_i^2 = 1{,}815{,}930\ nV^2$

$\bar{e}_N = \sqrt{\Sigma} = 1.337\ \mu V$

17 $S/N = 20 \log (4.0\ mV/1.337\ \mu V) = 69.4\ dB$

Note the significant contributions of $\bar{i}_n$ and the 47k resistor, especially at high frequencies. Note also that there will be a difference between calculated noise and that noise measured on broadband meters because of the A curve employed in the example. If it were not for the A curve attenuation at low frequencies, the $\bar{e}_n$ would add a very important contribution below 200 Hz. This would be due to the RIAA boost at low frequency. As it stands, 97% of the 1.35 μV would occur in the 800–12.8 kHz band alone, principally because of the high frequency boost and the A measurement curve. If the measurement were made without either the high frequency boost or the A curve, the $\bar{e}_n$ would be 1.25 μV. In this case, 76% of the total noise would arise in the 50 Hz–400 Hz band alone. If the A curve were used, but the high-frequency boost were deleted, $\bar{e}_n$ would be 0.91 μV; and 94% would arise in the 800–12,800 Hz band alone.

The three different methods of measuring would only produce a difference of +3.5 dB in overall S/N, however the prime sources of the largest part of the noise and the frequency character of the noise can vary greatly with the test or measurement conditions. It is, then, quite important to know the method of measurement in order to know which individual noise sources in *Figure 6* must be reduced in order to significantly improve S/N.

CONCLUSIONS

The main points in selecting low noise preamplifiers are:

1. Don't pad the signal source; live with the existing R_{gen}.
2. Select on the basis of low values of $\bar{e}_n$ and especially $\bar{i}_n$ if R_{gen} is over about a thousand Ω.
3. Don't select on the basis of NF or R_{OPT} in most cases. NF specs are all right so long as you know precisely how to use them and so long as they are valid over the frequency band for the R_{gen} or Z_{gen} with which you must work.
4. Be sure to (root) sum all the noise sources $\bar{e}_n$, $\bar{i}_n$ and $\bar{e}_R$ in your system over appropriate bandwidth.
5. The higher frequencies are often the most important unless there is low frequency boost or high frequency attenuation in the system.
6. Don't forget the filtering effect of the human ear in audio systems. Know the eventual frequency emphasis or filtering to be employed.

APPENDIX I

Derivation of R_{OPT}:

$$NF = 10 \log \frac{\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}$$

$$10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}\right)$$

$$\frac{\delta NF}{\delta R} = \frac{0.435}{(4\ kTRB)^2} \frac{4\ kTRB\ (2R\ \overline{i_n^2}) - (\overline{e_n^2} + \overline{i_n^2} R^2) 4\ kTB}{1 + (\overline{e_n^2} + \overline{i_n^2} R^2)/4\ kTRB}$$

where: $R = R_{gen}$

Set this = 0, and

$$4\ kTRB(2R\ \overline{i_n^2}) = 4\ kTB\ (\overline{e_n^2} + \overline{i_n^2} R^2)$$

$$2\ \overline{i_n^2} R^2 = \overline{e_n^2} + \overline{i_n^2} R^2$$

$$\overline{i_n^2} R^2 = \overline{e_n^2}$$

$$R^2 = \overline{e_n^2}/\overline{i_n^2}$$

$$R_{OPT} = \frac{\bar{e}_n}{\bar{i}_n}$$

APPENDIX II

Selecting R_{gen} for highest S/N.

$$S/N = \frac{e_{sig}^2}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2)}$$

For S/N to increase with R,

$$\frac{\delta S/N}{\delta R} > 0$$

$$\frac{\delta S/N}{\delta R} = \frac{2e_{sig}\ (\delta e_{sig}/\delta R)\ (\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2) - e_{sig}^2\ (4\ kT + 2\ \overline{i_n^2} R)}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2)^2}$$

APPENDIX II (Continued)

If we set > 0, then

$$2\,(\delta e_{sig}/\delta\,R)\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2) > e_{sig}\,(4\,kT + 2\,\overline{i_n{}^2}\,R)$$

For $e_{sig} = k_1\sqrt{R}$, $\delta e_{sig}/\delta R = \dfrac{k_1}{2\sqrt{R}}$

$$(2\,k_1/2\sqrt{R})\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R2) > k_1\sqrt{R}\,(4\,kT + 2\,\overline{i_n{}^2}\,R)$$

$$\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2 > 4\,kTR + 2\,\overline{i_n{}^2}\,R^2$$

$$\overline{e_n{}^2} > \overline{i_n{}^2}\,R^2$$

$$R < \overline{e}_n/\overline{i}_n$$

Therefore S/N increases with R_{gen} so long as $R_{gen} \leq R_{OPT}$

For $e_{sig} = k_1\,R$, $\delta e_{sig}/\delta R = k_1$

$$2\,k_1\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2) > k_1 R\,(4\,kT + 2\,\overline{i_n{}^2}\,R)$$

$$2\,\overline{e_R{}^2} + 2\,\overline{e_n{}^2} + 2\,\overline{i_n{}^2}\,R^2 > 4\,kTR + 2\,\overline{i_n{}^2}\,R^2$$

$$\overline{e_R{}^2} + 2\,\overline{e_n{}^2} > 0$$

Then S/N increases with R_{gen} for any amplifier.

For any $e_{sig} < k_1\sqrt{R}$, an optimum R_{gen} may be determined. Take, for example, $e_{sig} = k_1\,R^{0.4}$, $\delta e_{sig}/\delta R = 0.4k_1\,R^{-0.6}$.

$$(0.8\,k_1/R^{0.6})\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2) > k_1\,R^{0.4}\,(4\,kT + 2\,\overline{i_n{}^2}\,R)$$

$$0.8\,\overline{e_R{}^2} + 0.8\,\overline{e_n{}^2} + 0.8\,\overline{i_n{}^2}\,R^2 > 4\,kTR + 2\,\overline{i_n{}^2}\,R^2$$

$$0.8\,\overline{e_n{}^2} > 0.2\,\overline{e_R{}^2} + 1.2\,\overline{i_n{}^2}\,R^2$$

Then S/N increases with R_{gen} until

$$0.25\,\overline{e_R{}^2} + 1.5\,\overline{i_n{}^2}\,R^2 = \overline{e_n{}^2}$$

Fast IC Power Transistor with Thermal Protection

National Semiconductor
Application Note 110

INTRODUCTION

Overload protection is perhaps most necessary in power circuitry. This is shown by recent trends in power transistor technology. Safe-area, voltage and current handling capability have been increased to limits far in excess of package power dissipation. In RF transistors, devices are now available and able to withstand badly mismatched loads without destruction. However, for anyone working with power transistors, they are still easily destroyed.

Since power circuitry, in many cases, drives other low level circuitry—such as a voltage regulator—protection is doubly important. Overloads that cause power transistor failure can result in the destruction of the entire circuit. This is because the common failure mode for power transistors is a short from collector to emitter—applying full voltage to the load. In the case of a voltage regulator, the raw supply voltage would be applied to the low level circuitry.

A new monolithic power transistor provides virtually absolute protection against any type of overload. Included on the chip are current limiting, safe area protection and thermal limiting. Current limiting controls the peak current through the chip to a safe level below the fuzing current of the aluminum metalization. At high collector to emitter voltage the safe area limiting reduces the peak current to further protect the power transistor. If, under prolonged overload, power dissipation causes chip temperature to rise toward destructive levels, thermal limiting turns off the device keeping the devices at a safe temperature. The inclusion of thermal limiting, a feature not easily available in discrete circuitry makes this device especially attractive in applications where normal protective schemes are ineffective.

The device's high gain and fast response further reduce requirements of surrounding circuitry. As well as being used in linear applications, the IC can interface transistor-transistor logic or complementary-MOS logic to power loads without external devices. In fact, the input-current requirement of 3 microamperes is small enough for one CMOS gate to drive over 400 LM195's.

Besides high dc current gain, the IC has low input capacitance so it can be easily driven from high impedance sources—even at high frequencies. In a standard TO-3 power package, the monolithic structure ties the emitter, rather than the collector, to the case effectively boot-strapping the base-to-package capacitance. Additionally, connecting the emitter to the package is especially convenient for grounded emitter circuits.

The device is fully protected against any overload condition when it is used below the maximum voltage rating. The current-limiting circuitry restricts the power dissipation to 35 watts, 1.8 amperes are available at collector-to-emitter voltage of 17V decreasing to about 0.8 amperes at 40V. In reality, however, like standard transistors, power dissipation in actual use is limited by the size of the external heat sink.

Switching time is fast also. At 40V 25 Ohm load can be switched on or off in a relatively fast 500 ns. The internal planar double diffused monolithic transistors have an f_t of 200 MHz to 400 MHz. The limiting factor on overall speed is the protective and biasing circuitry around the output transistors. An important performance point is that no more than the normal 3 μA base current is needed for fast switching.

To the designer, the LM195 acts like an ordinary power transistor, and its operation is almost identical to that of a standard power device. However, it provides almost absolute protection against any type of overload. And, since it is manufactured with standard seven-mask IC technology, the device is produceable in large quantities at reasonable cost.

CIRCUIT DESIGN

Besides the protective features, the monolithic power transistor should function as closely to a discrete transistor as possible. Of course, due to the circuitry on the chip, there will be some differences.

Figure 1 shows a simplified schematic of the power transistor. A power NPN Darlington is driven by an input PNP. The PNP and output NPN's are biased by internal current source I_1. The composite three transistors yield a total current gain in excess of 10^6 making it easy to drive the power transistors from high impedance sources. Unlike normal power transistors, the base current is negative, flowing out of the PNP. However, in most cases this is not a problem.

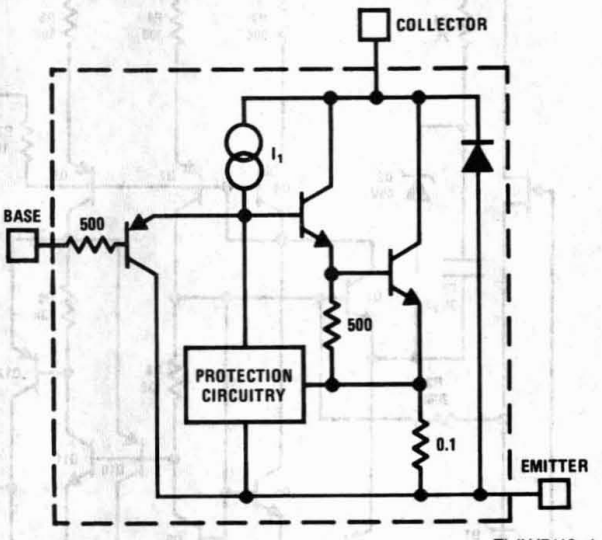

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FIGURE 1. Simplified Circuit of the LM195

The input PNP transistor is made with standard IC processing and has a reverse base-emitter breakdown voltage in excess of 40V. This allows the power transistor to be driven from a stiff voltage source without damage due to excessive base current. At input voltages in excess of about 1V the input PNP becomes reverse biased and no current is drawn from the base lead. In fact it is possible for the base of the monolithic transistor to be driven with up to 40V even though the collector to emitter voltage is low. Further, the input PNP isolates the base drive from the protective circuitry insuring that even with high base drive the device will be protected. When the device is turned off current I_1 is shunted from the base of the NPN transistor by the PNP and appears at the emitter terminal. This sets the minimum load current to about 2 mA, not a severe restriction for a power transistor. Because of the PNP and I_1, the power transistor turns "on" rather than "off" if the base is opened; however, most power circuits already include a base-emitter resistor to absorb leakage currents in present power transistors.

A schematic of the LM195 is shown in *Figure 2*. The circuitry is biased by four current sources comprised of Q4, Q7, Q8 and Q9. The operating current is set by Q5 and Q6 and is relatively independent of supply voltage. FET Q1 and R2 insure reliable starting of the bias circuitry while D1 clamps the output of the FET limiting the starting current at high supply voltage.

The output transistors Q19 and Q20 are driven from input PNP Q14. Current limiting independent of temperature changes is provided by Q21, Q16, and Q15. At high collector to emitter voltages the current limit decreases due to the voltage across R21 from D3, D4 and R20. The double emitter structure used on Q21 allows the power limiting to more closely approximate constant power curve rather than a straight line decrease in output current as input voltage increases.

Transistor Q13 thermally limits the device by removing the base drive at high temperature. The actual temperature sensing is done by Q11 and Q12 with Q10 regulating the voltage across the sensors so thermal limit temperature remains independent of supply. As temperature increases, the collector current of Q11 increases while the V_{BE} of Q12 decreases. At about 170°C the Q12 turns on Q13 removing the base drive from the output transistors. Finally, C1, Q2 and Q3 boost operating currents during switching to obtain faster response time and Q17 and Q18 compensate for h_{fe} variations in the power devices.

PERFORMANCE

The new power transistor is packaged in a standard TO-3 transistor package making it compatible with standard power transistors. An added advantage of the monolithic structure is that the emitter is tied to the case rather than the collector. This allows the device to be connected directly to ground in collector output applications.

A photomicrograph of the LM195 is shown in *Figure 3*. More than half of the die area is needed for the output power transistor (Q20). Actually, the power transistor is many individual small transistors connected in parallel with a common collector. Partitioning the power device into small discrete areas improves power handling over a single large device. Firstly, the power device has ten base sections spread across the chip. Between the base diffusion are N+ collector contacts. Each section has its own emitter ballasting resistor to insure current sharing between sections. One of these resistors is used to sense the output current for current limiting.

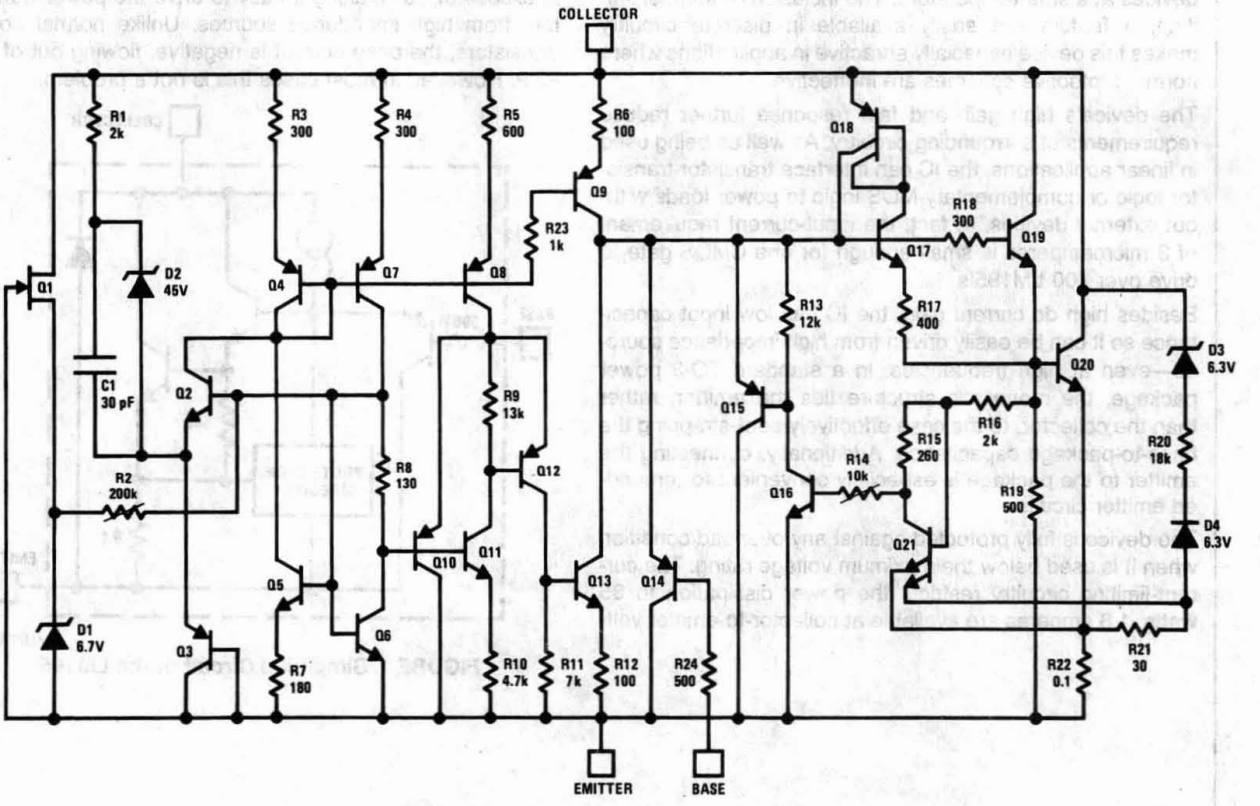

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FIGURE 2. Schematic Diagram of the LM195

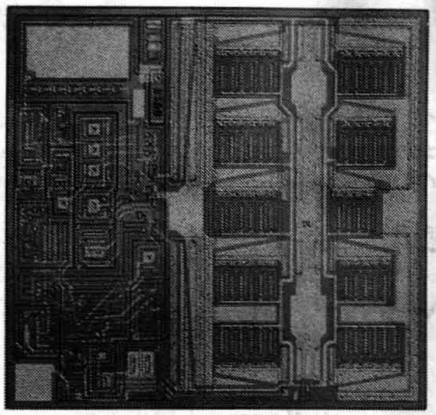

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FIGURE 3. LM195 Chip

TABLE I. Typical Performance

Collector to Emitter Voltage	42V
Base to Emitter Voltage (max.)	42V
Peak Collector Current (internally limited)	1.8 amps
Reverse Base Emitter Voltage	20V
Base to Emitter Voltage (I_C = 1.0 amp)	0.9V
Base Current	3 μA
Saturation Voltage	2V
Switching Time (turn on or turn off)	500 ns
Power Dissipation (internally limited)	35 watts
Thermal Limit Temperature	165°C
Maximum Operating Temperature	150°C
Thermal Resistance (Junction to Case)	2.3°C/W

A detail of one of the base sections is shown in *Figure 4*. An interdigitated structure is used with alternating base contacts and emitter stripes. Integrated into each emitter is an individual emitter ballasting resistor to insure equal current sharing between emitters in each section. Aluminum metalization runs the length of the emitter stripe to prevent lateral voltage drop from debiasing a section of the stripe at high operating currents. All current in the stripe flows out through the small ballasting resistor where it is summed with the currents from the other stripes in the section. The partitioning in conjunction with the emitter resistor gives a power transistor with large safe-area and good power handling capability.

APPLICATIONS

With the full protection and high gain offered by this monolithic power transistor, circuit design is considerably simplified. The inclusion of thermal limiting, not normally available in discrete design allows the use of smaller heat sinks than with conventional protection circuitry. Further, circuits where protection of the power device is difficult—if not impossible—now cause no problems.

For example, with only current limiting, the power transistor heat sink must be designed to dissipate worst case overload power dissipation at maximum ambient temperature. When the power transistor is thermally limited, only normal power need be dissipated by the heat sink. During overload, the device is allowed to heat up and thermally limit, drastically reducing the size of the heat sink needed.

Switching circuits such as lamp drivers, solenoid drivers or switching regulators do not dissipate much power during normal operation and usually no heat sink is necessary. However, during overload, the full supply voltage times the maximum output current must be dissipated. Without a large heat sink standard power transistors are quickly destroyed.

Using this new device is easier than standard power transistors but a few precautions should be observed. About the only way the device can be destroyed is excessive collector to emitter voltage or improper power supply polarity. Sometimes when used as an emitter follower, low level high frequency oscillations can occur. These are easily cured inserting a 5k-10k resistor in series with the base lead. The resistor will eliminate the oscillation without effecting speed or performance. Good power supply bypassing should also be used since this is a high frequency device.

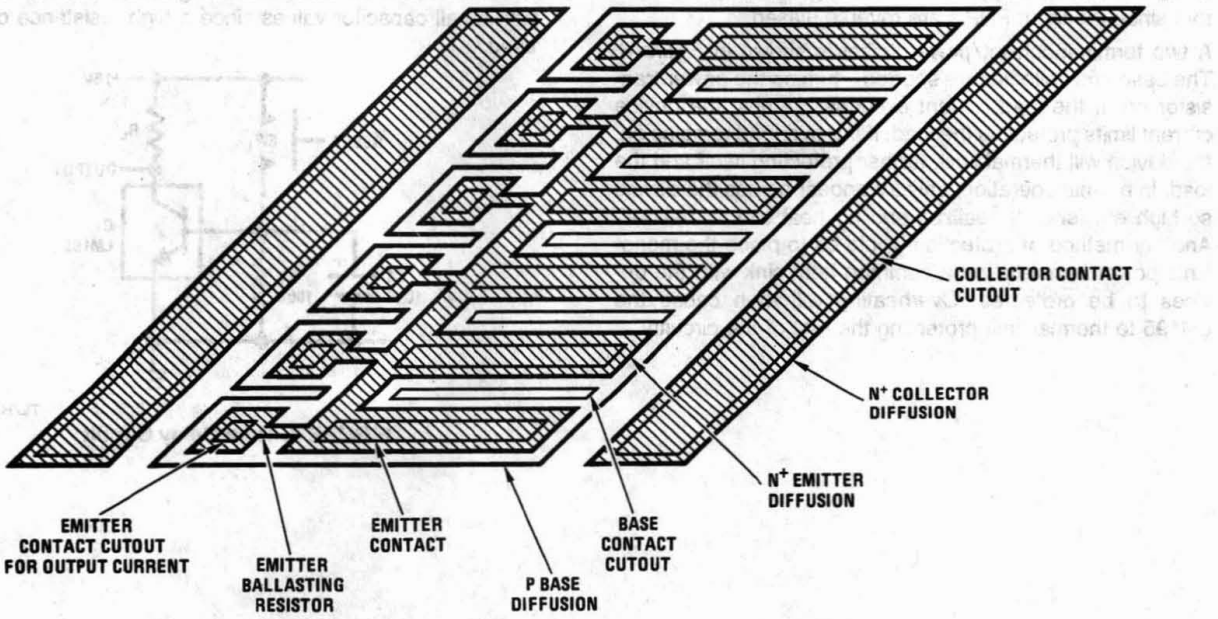

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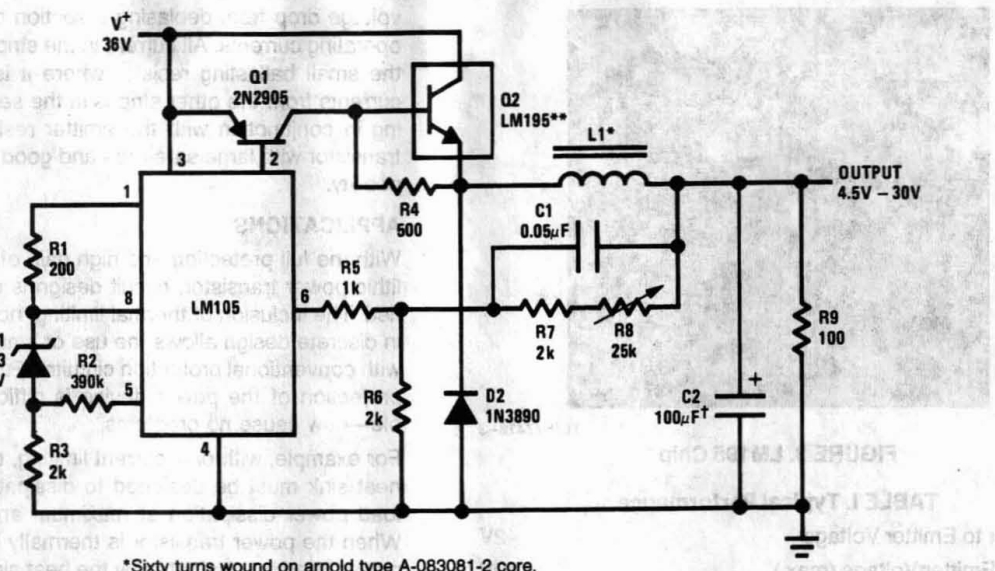
FIGURE 4. Detailed Structure of one Section of the Power Transistor



*Sixty turns wound on arnold type A-083081-2 core.

**Four devices in parallel.

†Solid tantalum.

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FIGURE 5. 6 Amp Variable Output Switching Regulator

Figure 5 shows a 6 amp, variable output switching regulator for general purpose applications. An LM105 positive regulator is used as the amplifier-reference for the switching regulator. Positive feedback to induce switching is obtained from the LM105 at pin 1 through an LM103 diode. The positive feedback is applied to the internal amplifier at pin 5 and is independent of supply voltage. This forces the LM105 to drive the pass devices either "on" or "off," rather than linearly controlling their conduction. Negative feedback, delayed by L1 and the output capacitor, C2, causes the regulator to switch with the duty cycle automatically adjusting to provide a constant output. Four LM195's are used in parallel to obtain a 6 amp output since each device can only supply about 2 amps. Note that no ballasting resistors are needed for current sharing. When Q1 turns "on" all bases are pulled up to V^+ and no base current flows in the LM195 transistors since the input PNP's are reverse biased.

A two terminal current/power limiter is shown in *Figure 6*. The base and collector are shorted—turning the power transistor on. If the load current exceeds 2 amps, the device current limits protecting the load. If the overload remains on, the device will thermal limit, further protecting itself and the load. In normal operation, only 2V appear across the device so high efficiency is realized and no heat sink is needed. Another method of protection would be to place the monolithic power transistor on a common heat sink with the devices to be protected. Overheating will then cause the LM195 to thermal limit protecting the rest of the circuitry.

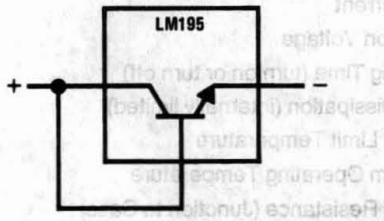

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FIGURE 6. Two Terminal Current Limiter

The low base current make this power device suitable for many unique applications. *Figure 7* shows a time delay circuit. Upon application of power or S1 closing, the load is energized. Capacitor C1 slowly charges toward V^- through R1. When the voltage across R1 decreases below about 0.8 volts the load is de-energized. Long delays can be obtained with small capacitor values since a high resistance can be used.

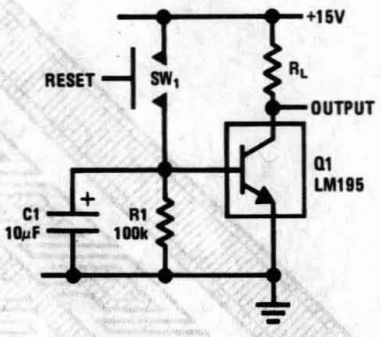

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FIGURE 7. Time Delay Circuit

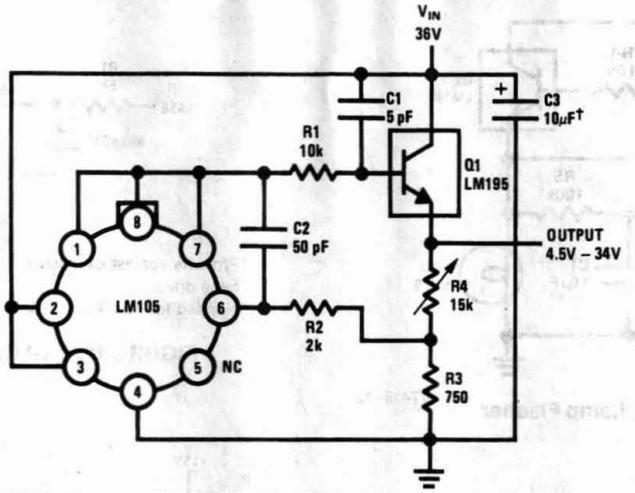

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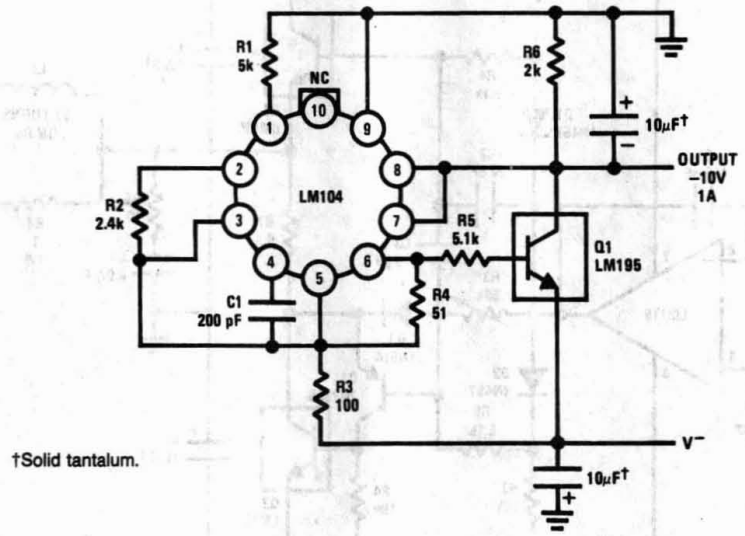
FIGURE 8. 1 Amp Positive Voltage Regulator



†Solid tantalum.

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FIGURE 9. 1 Amp Negative Regulator

Figures 8 and *9* show how the LM195 can be used with standard IC's to make positive or negative voltage regulators. Since the current gain of the LM195 is so high, both regulators have better than 2 mV load regulation. They are both fully overload protected and will operate with only 2V input-to-output voltage differential.

An optically isolated power transistor is shown in *Figure 10*. D1 and D2 are almost any standard optical isolator. With no drive, R1 absorbs the base current of Q1 holding it off. When power is applied to the LED, D2 allows current to flow from the collector to base. Less than 20 μA from the diode is needed to turn the LM195 fully on.

An alternate connection for better ac response is to return the cathode of D2 to separate positive supply rather than the collector of Q1, as shown in *Figure 11*, eliminating the added collector to base capacitance of the diode. With this circuit a 40V 1 amp load can be switched in 500 ns. Of course, any photosensitive diode can be used instead of the opto-isolator to make a light activated switch.

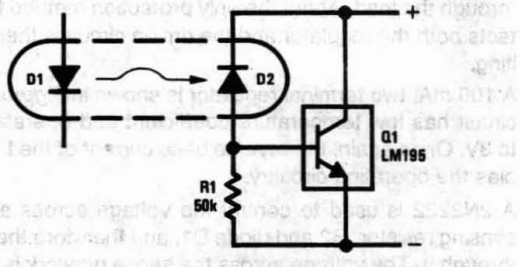

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FIGURE 10. Optically Isolated Power Transistor

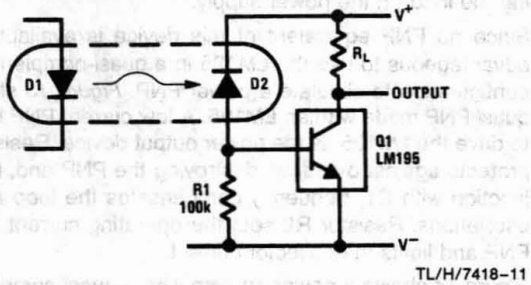

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FIGURE 11. Fast Optically Isolated Switch

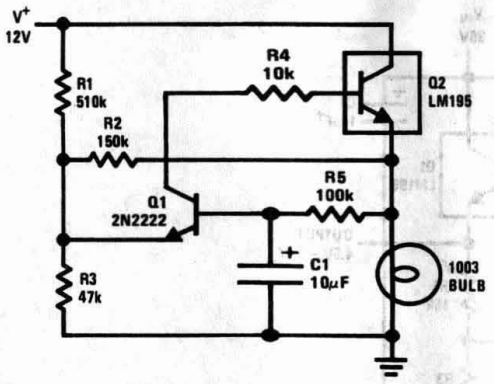

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FIGURE 12. 1 Amp Lamp Flasher

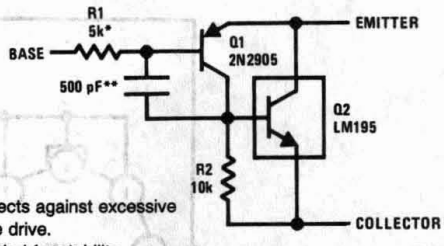

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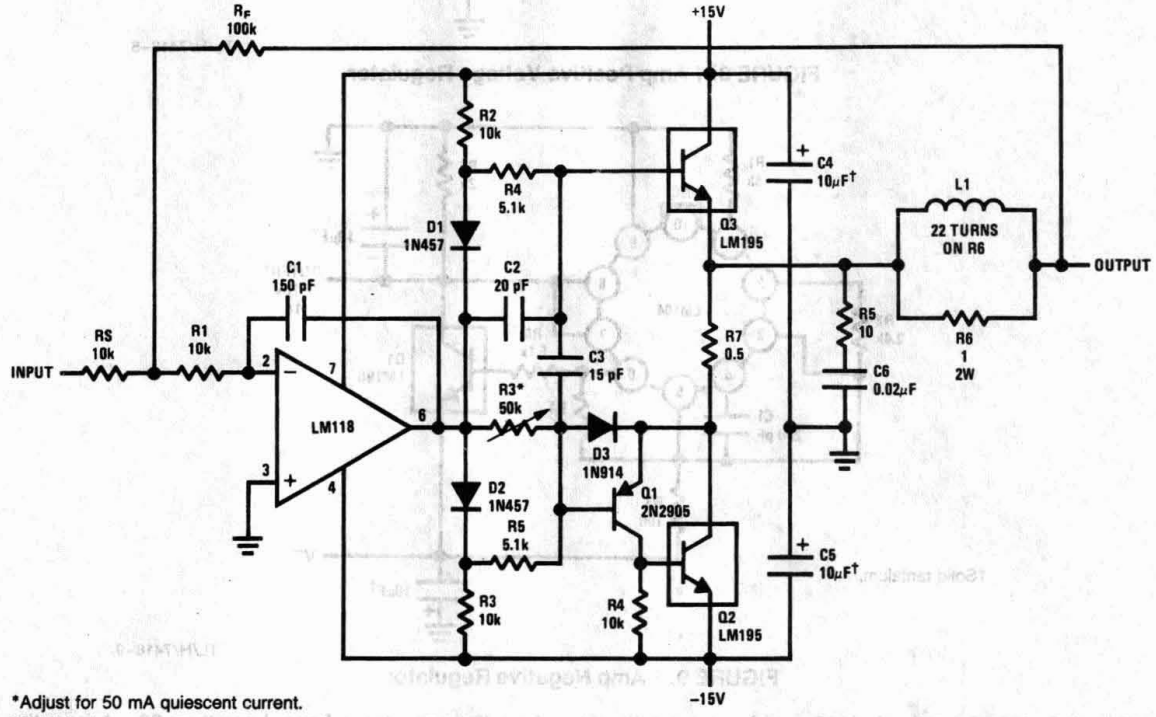
FIGURE 13. PNP Configuration for LM195



*Adjust for 50 mA quiescent current.
†Solid tantalum.

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FIGURE 14. Power Op Amp

A power lamp flasher is shown in *Figure 12*. It is designed to flash a 12V bulb at about a once-per second rate. The reverse base current of Q2 provides biasing for Q1 eliminating the need for a resistor. Typically, a cold bulb can draw 8 times its normal operating current. Since the LM195 is current limited, high peak currents to the bulb are not experienced during turn-on. This prolongs bulb life as well as easing the load on the power supply.

Since no PNP equivalent of this device is available, it is advantageous to use the LM195 in a quasi-complementary configuration to simulate a power PNP. *Figure 13* shows a quasi PNP made with an LM195. A low current PNP is used to drive the LM195 as the power output device. Resistor R1 protects against overdrive destroying the PNP and, in conjunction with C1, frequency compensates the loop against oscillations. Resistor R2 sets the operating current for the PNP and limits the collector current.

Figure 14 shows a power op amp with a quasi-complementary power output stage. Q1 and Q2 form the equivalent of a power PNP. The circuit is simply an op amp with a power output stage. As shown, the circuit is stable for almost any load. Better bandwidth can be obtained by decreasing C1 to 15 pF (to obtain 150 kHz full output response), but capacitive loads can cause oscillation. If due to layout, the quasi-complimentary loop oscillates, collector to base capacitance on Q1 will stabilize it. A simpler power op amp for up to 300 Hz operation is shown in *Figure 15*.

One of the more difficult circuit types to protect is a current regulator. Since the current is already fixed, normal protection doesn't work. Circuits to limit the voltage across the current regulator may allow excessive current to flow through the load. About the only protection method that protects both the regulator and the driven circuit is thermal limiting.

A 100 mA, two terminal regulator is shown in *Figure 16*. The circuit has low temperature coefficient and operates down to 3V. Once again, the reverse base current of the LM195 to bias the operating circuitry.

A 2N2222 is used to control the voltage across a current sensing resistor, R2 and diode D1, and therefore the current through it. The voltage across the sense network is the V_{BE} of the 2N2222 plus 1.2V from the LM113. In the sense network R2 sets the current while D1 compensates for the V_{BE} of the transistor. Resistor R1 sets the current through the LM113 to 0.6 mA.

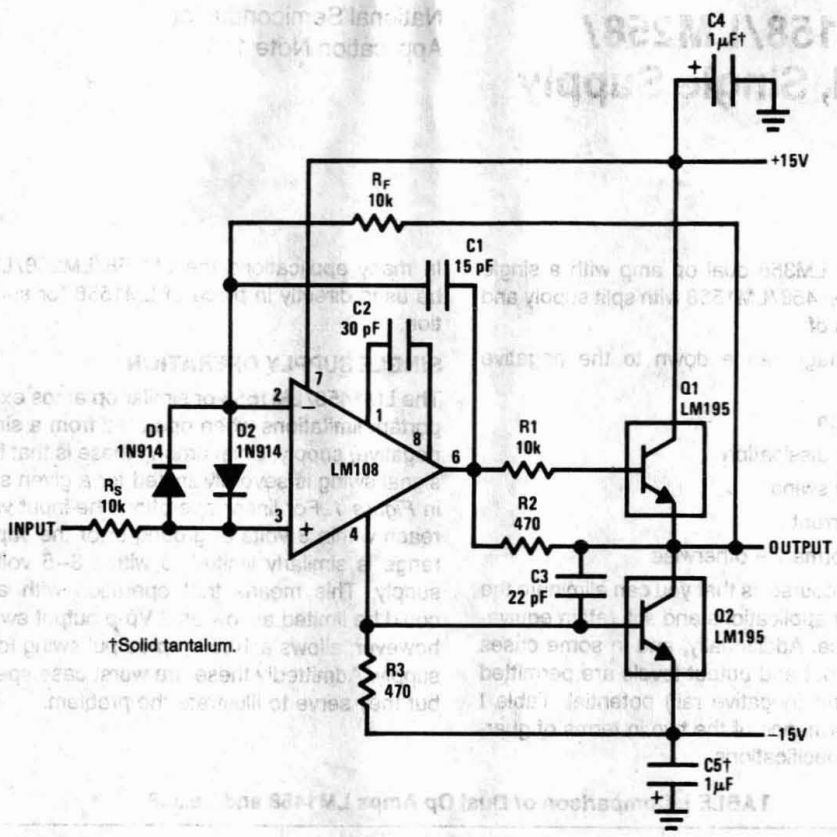


FIGURE 15. 1 Amp Voltage Follower

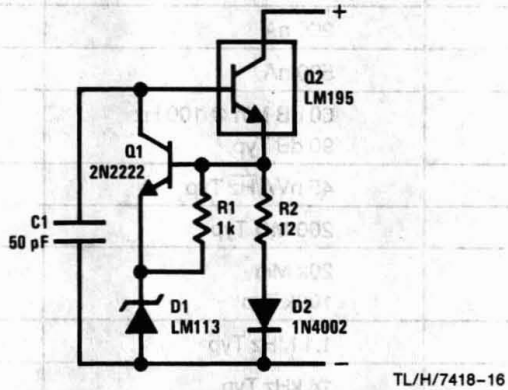


FIGURE 16. Two Terminal 100 mA Current Regulator

CONCLUSIONS

A new IC power transistor has been developed that significantly improves power circuitry reliability. The device is virtually impossible to destroy through abuse. Further it has high gain and fast response. It is manufactured with standard seven mask IC technology making it produceable in large quantities at reasonable prices. Finally, in addition to the protection features, it has high gain simplifying surrounding circuitry.

Use the LM158/LM258/ LM358 Dual, Single Supply Op Amp

National Semiconductor
Application Note 116

INTRODUCTION

Use the LM158/LM258/LM358 dual op amp with a single supply in place of the LM1458/LM1558 with split supply and reap the profits in terms of:

a. Input and output voltage range down to the negative (ground) rail

b. Single supply operation

c. Lower standby power dissipation

d. Higher output voltage swing

e. Lower input offset current

f. Generally similar performance otherwise

The main advantage, of course, is that you can eliminate the negative supply in many applications and still retain equivalent op amp performance. Additionally, and in some cases more importantly, the input and output levels are permitted to swing down to ground (negative rail) potential. Table I shows the relative performance of the two in terms of guaranteed and/or typical specifications.

In many applications the LM158/LM258/LM358 can also be used directly in place of LM1558 for split supply operation.

SINGLE SUPPLY OPERATION

The LM1458/LM1558 or similar op amps exhibit several important limitations when operated from a single positive (or negative) supply. Chief among these is that input and output signal swing is severely limited for a given supply as shown in *Figure 1*. For linear operation, the input voltage must not reach within 3 volts of ground or of the supply, and output range is similarly limited to within 3–5 volts of ground or supply. This means that operation with a +12V supply could be limited as low as 2 Vp-p output swing. The LM358 however, allows a 10.5 Vp-p output swing for the same 12V supply. Admittedly these are worst case specification limits, but they serve to illustrate the problem.

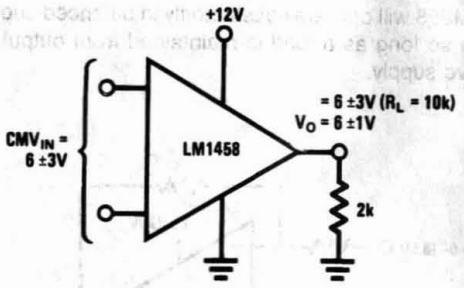
TABLE I. Comparison of Dual Op Amps LM1458 and LM358

Characteristic	LM1458	LM358
V_{IO}	6 mV Max	7 mV Max
CM V_I	24 Vp-p*	0–28.5V*
I_{IO}	200 nA	50 nA
I_{OB}	500 nA	−500 nA
CMRR	60 dB Min @ 100 Hz 90 dB Typ	85 dB Typ @ DC
$\bar{e}_n$ @ 1 kHz, R_{GEN} 10 kΩ	45 nV/$\sqrt{Hz}$ Typ	40 nV/$\sqrt{Hz}$ Typ**
Z_{IN}	200 MΩ Typ	Typ 100 MΩ
A_{VOL}	20k Min 100k Typ	100k Typ
f_c	1.1 MHz Typ	1 MHz Typ**
P_{BW}	14 kHz Typ	11 kHz Typ**
dV_o/dt	0.8V/μs Typ	0.5V/μs Typ**
V_o @ R_L = 10k/2k	24/20 Vp-p*	28.5 Vp-p
I_{SC}	20 mA Typ	Source 20 mA Min (40 Typ) Sink 10 mA Min (20 Typ)
PSRR @ DC	37 dB Min 90 dB Typ	100 dB Typ
I_D (R_L = ∞)	8 mA Max	2 mA Max

‡From laboratory measurement

*Based on V_S = 30V on LM358 only, or V_S = ±15V

**From data sheet typical curves



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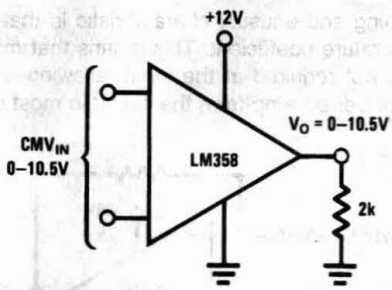

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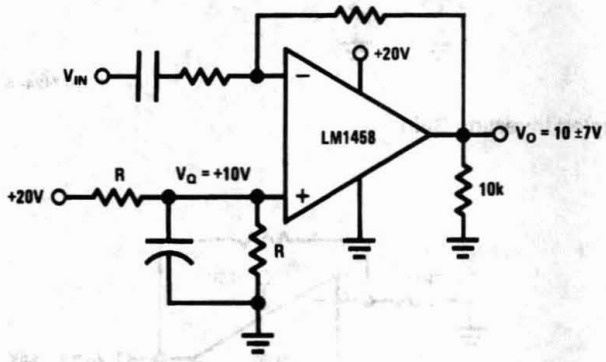
FIGURE 1. Worst Case Signal Levels with + 12V Supply



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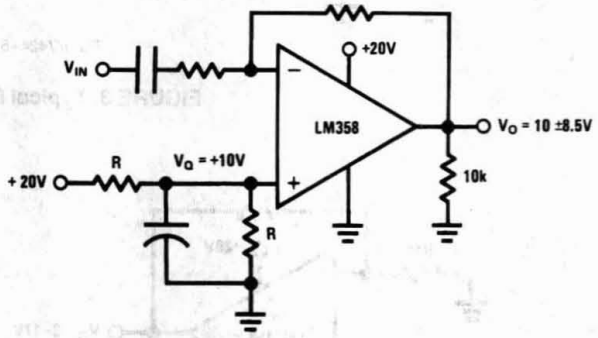

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FIGURE 2. Operating with AC Signals

AC GAIN

For AC signals the input can be capacitor coupled. The input common mode and quiescent output voltages are fixed at one-half the supply voltage by a resistive divider at the non-inverting input as shown in *Figure 2*. This quiescent output could be set at a lower voltage to minimize power dissipation in the LM358, if desired, so long as $V_Q \geq V_{IN}$ pk. For the LM1458 the quiescent output must be higher, $V_Q \geq 3V + V_{IN}$ pk thus, for small signals, power dissipation is much greater with the LM1458. Example: Required $V_O = V_Q \pm 1V$ pk into 2k, V_{SUPPLY} = as required. Find quiescent dissipation in load and amplifier for LM1458 and LM358.

LM358	LM1458
$V_Q = +1V$	$V_Q = 4V$
$V_{SUPPLY} = +3.5V$	$V_{SUPPLY} = 8V$
$P_{LOAD} = \frac{E_L^2}{R_L} = \frac{1}{2k} = 0.5$ mW	$P_{LOAD} = \frac{4^2}{2k} = 8$ mW
$P_D = V_S I_S^* + (V_S - V_Q) I_L$	$P_D = P_D^* + (V_S - V_Q)\, I_L$
$= 3.5V \times 0.7$ mA $+ (3.5-1)\frac{1V}{2k}$	$= 22$ mW $+ (8-4)\frac{4V}{2k}$
$P_D = 2.45 + 1.25 = 3.7$ mW	$P_D = 22 + 8 = 30$ mW
$P_{TOTAL} = 3.7 + 0.5 = 4.2$ mW	$P_{TOTAL} = 30 + 8 = 38$ mW
*From typical characteristics	*From typical characteristics

The LM1458 requires over twice the supply voltage and nearly 10 times the supply power of the LM358 in this application.

INVERTING DC GAIN

Connections and biasing for DC inverting gain are essentially the same as for the AC coupled case. Note, of course, that the output cannot swing negative when operated from a single positive supply. *Figure 3* shows the connections and signal limitations.

NON-INVERTING DC GAIN

The non-inverting gain connection does not require the V_Q biasing as before; the inverting input can be returned to ground in the usual manner for gains greater than unity, (see *Figure 4*). A tremendous advantage of the LM358 in this connection is that input signals and output may extend all the way to ground; therefore DC signals in the low-millivolt range can be handled. The LM1458 still requires that V_{IN} = 3–17V. Therefore maximum gain is limited to $A_V = (V_O - 3)/3$, or A_V max = 5.4 for a 20V supply.

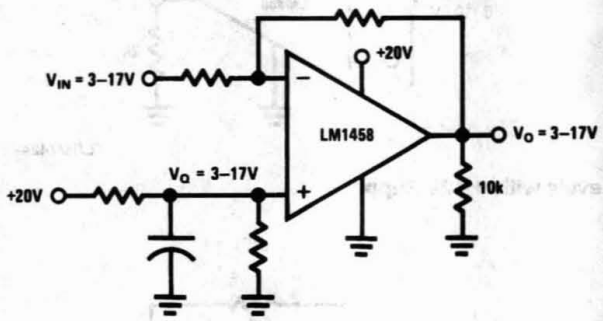
There is no similar limitation for the LM358.

ZERO T.C. INPUT BIAS CURRENT

An interesting and unusual characteristic is that I_{IN} has a zero temperature coefficient. This means that matched resistance is not required at the input, allowing omission of one resistor per op amp from the circuit in most cases.

BALANCED SUPPLY OPERATION

The LM358 will operate satisfactorily in balanced supply operation so long as a load is maintained from output to the negative supply.



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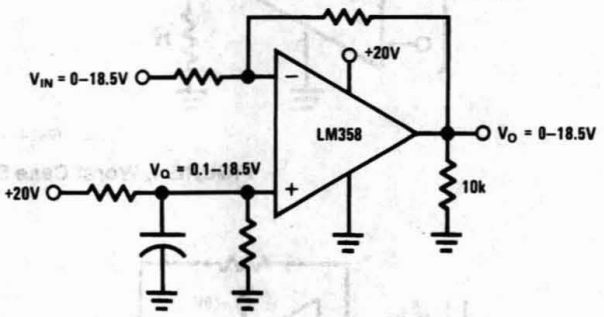

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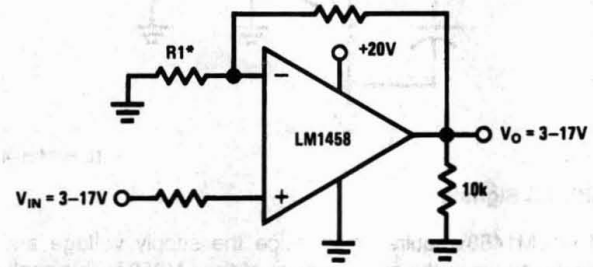
FIGURE 3. Typical DC Coupled Inverting Gain



*R1 = ∞ for A_V = +1
$A_V \leq 5.4$ for 20V Supply

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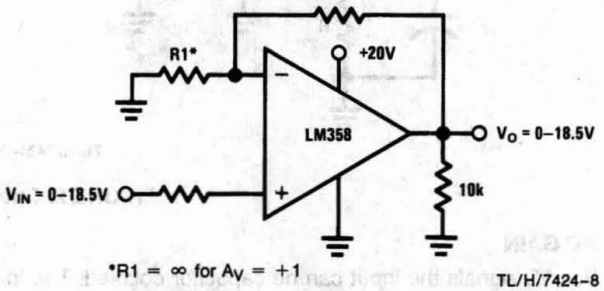

*R1 = ∞ for A_V = +1
A_V not limited

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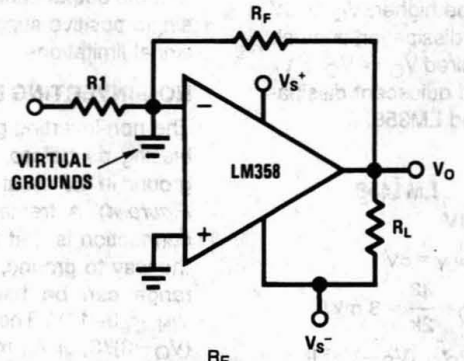
FIGURE 4. Typical DC Coupled Non-Inverting Gain



Crossover (distortion) occurs at $V_O = V_S^- \frac{R_F}{R_L + R_F}$

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FIGURE 5. Split Supply Operation of LM358

The output load to negative supply forces the amplifier to source some minimum current at all times, thus eliminating crossover distortion. Crossover distortion without this load would be more severe than that expected with the normal op amp. Since the single supply design took notice of this normal load connection to ground, a class AB output stage was not included. Where ground referenced feedback resistors are used as in *Figure 5*, the required load to the negative supply depends upon the peak negative output signal level desired without exhibiting crossover distortion. R_L to the negative rail should be chosen small enough that the voltage divider formed by R_F and R_L will permit V_o to swing negative to the desired point according to the equation:

$$R_L = R_F \frac{V_S^- - V_o}{V_o}.$$

R_L could also be returned to the positive supply with the advantage that V_o max would never exceed ($V_S^+ - 1.5V$). Then with $\pm 15V$ supplies $R_{L\ MIN}$ would be 0.12 R_F. The disadvantage would be that the LM358 can source twice as much current as it can sink, therefore R_L to negative supply can be one-half the value of R_L to positive supply.

The need for single or split supply is based on system requirements which may be other than op amp oriented. However if the only need for balanced supplies is to simplify the biasing of op amps, there are many systems which can find a cost effective benefit in operating LM358's from single supplies rather than standard op amps from balanced supplies. Of the usual op amp circuits, Table II shows those few which have limited function with single supply operation. Most are based on the premise that to operate from a single supply, a reference V_Q at about one-half the supply be available for bias or (zero) signal reference. The basic circuits are those listed in AN-20.

TABLE II. Conventional Op Amp Circuits Suitable for Single Supply Operation

Application	Limitations
AC Coupled amp‡	V_Q*
Inverting amp	V_Q
Non-inverting amp	OK*
Unity gain buffer	OK
Summing amp	V_Q
Difference amp	V_Q
Differentiator	V_Q
Integrator	V_Q
LP Filter	V_Q
I-V Connector	V_Q
PE Cell Amp	OK
I Source	$I_{O\ MIN} = \frac{1.5}{R1}$
I sink	OK
Volt Ref	OK
FW Rectifier	V_Q or modified circuit
Sine wave osc	V_Q
Triangle generator	V_Q
Threshold detector	OK
Tracking, regulator PS	Not practical
Programmable PS	OK
Peak Detector	OK to $V_{IN} = 0$

‡See AN20 for conventional circuits

*V_Q denotes need for a reference voltage, usually at about $\frac{V_S}{2}$

OK means no reference voltage required

LM143 Monolithic High Voltage Operational Amplifier Applications

National Semiconductor
Application Note 127

INTRODUCTION

The LM143 is a general purpose, high voltage operational amplifier featuring ±40V maximum supply voltage operation, output swing to ±37V, ±38V input common-mode range, input overvoltage protection up to ±40V and slew rate greater than 2V/μs*. Offset null capability plus low input bias and offset currents (8 nA and 1 nA respectively) minimize errors in both high and low source impedance applications. Due to isothermal symmetry of the chip layout, gain is constant for loads ≥ 2 kΩ at output levels to ±37V. Because of these features, the LM143 offers advantages not found in other general purpose op amps. The LM143 may, in fact, be used as an improved performance, plug-in replacement for the LM741 in most applications.

This paper describes the operation of the LM143 and presents applications which take advantage of its unique, high voltage capabilities. Obviously, other applications exist where the low input current and high slew rate of the LM143 are useful. (See AN-29 on the LM108.) Application tips are included in the appendix to guide the user toward reliable, trouble-free operation.

CIRCUIT DESCRIPTION

A simplified schematic of the LM143, shown in *Figure 1*, illustrates the basic circuit operation. The super-β input transistors[1], Q1 and Q2, are used as emitter followers to achieve low input bias currents. Although these devices exhibit β = 2000–5000, they inherently have a low collector-base breakdown voltage of about 4V. Therefore, active voltage clamps Q3 and Q4 protect Q1 and Q2 under all input conditions including common-mode and differential overvoltage. Other NPNs in the circuit are representative of those found in standard IC op amps ($\beta \approx 200$, LV_{CEO} = 50–70V).

The input stage differential amplifier Q7 and Q8 with large base width exhibit LV_{CEO} = 90V to 110V and high BV_{EBO} so readily withstand input overvoltages. The total input stage collector current (I_1 = 80 μA) is made higher than in most op amps to improve slew rate. Emitter degeneration resistors, R10 and R11, reduce transconductance[2] to limit small signal bandwidth at 1 MHz for a phase margin of 75°. Q16 and Q17 function as active collector loads for Q7 and Q8 and provide differential to single-ended current conversion with full differential gain.

One of the highest breakdown voltages available in standard planar NPN processing is the collector-base, BV_{CBO} which is typically 90V to 120V. To make use of this high voltage capability in the active region, the second stage consists of a cascode (common emitter-common base pair) connection of Q21 and Q23. The internal voltage bias V_{B1}, shunts avalanche-induced leakage current away from the base of Q21, avoiding β multiplication as found in the LV_{CEO} mode. Q23 and emitter follower Q22 are internally biased at a low voltage so the BV_{CEO} mode is impossible. Frequency compensation is achieved with an internal, high voltage capacitor, C_C.

* An externally compensated version of the LM143, the LM144, offers even higher slew rate in most applications. The LM144 is pin-for-pin compatible with the LM101A.

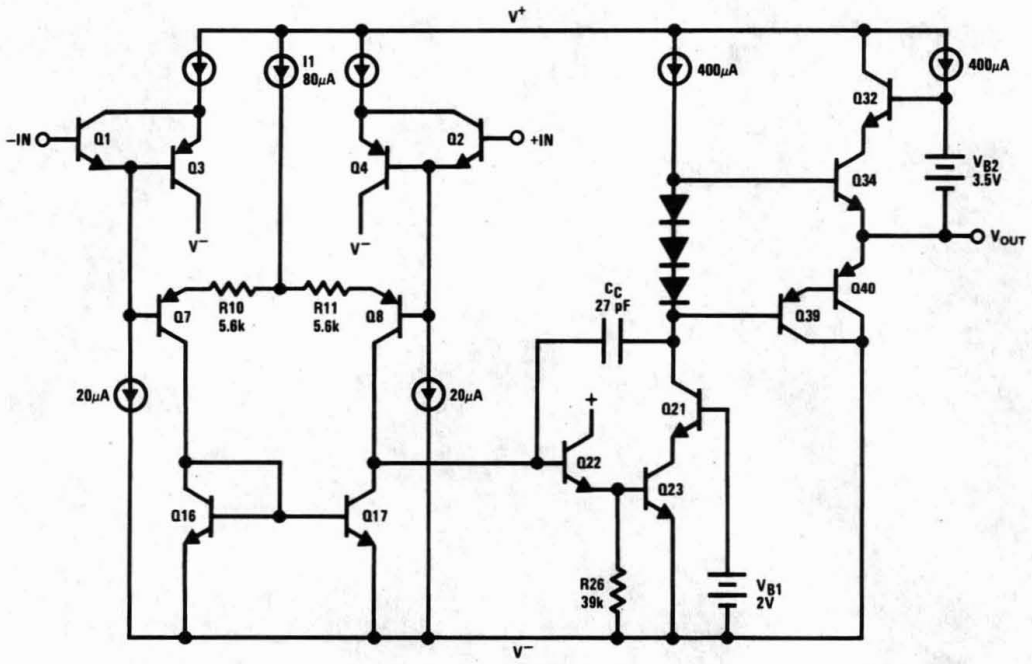

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FIGURE 1. LM143 Simplified Schematic

The second stage drives a complementary class AB output stage. A cascode connection of Q32 and Q34 is again employed for high breakdown voltage. The associated voltage bias, V_{B2}, is internally derived. A Darlington PNP pair, Q39 and Q40 with BV_{CEO} = 100V, provides the active pull-down.

HIGH VOLTAGE APPLICATIONS

The following applications make use of the high voltage capabilities of the LM143. As with most general purpose op amps, the power supplies should be adequately bypassed to ground with 0.1 μF capacitors.

130 Vp-p Drive to a Floating Load

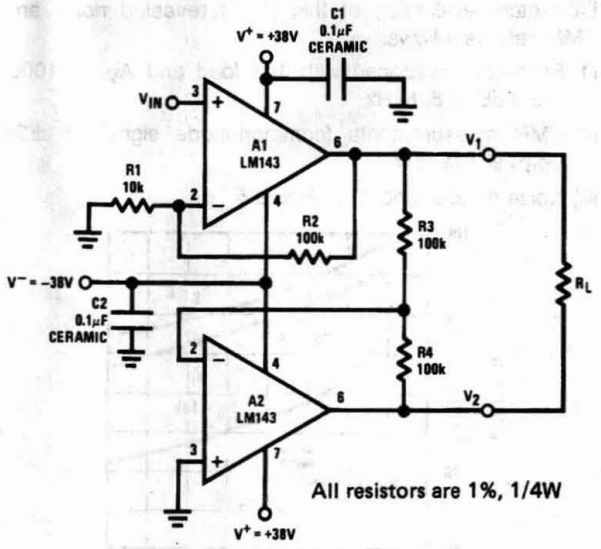
A circuit diagram using two LM143's to drive up to 130V peak-to-peak is given in *Figure 2*.

A non-inverting voltage amplifier, with a gain of A_V = 1 + (R2/R1), is followed by a unity gain inverter. The load is applied across the outputs of A1 and A2. Therefore, V_{OUT} = V1 − V2 = V1 − (−V1) = 2V1. If V1 = 65 Vp-p, then 2V1 = 130 Vp-p.

The above circuit was breadboarded and the results are as follows:

i) Maximum output voltage: 138 Vp-p unclipped into 10 kΩ load

ii) Slew rate: 6V/μs



TL/H/7432–2

FIGURE 2. 130V Drive Across a Floating Load

±34V Common-Mode Range Instrumentation Amplifier

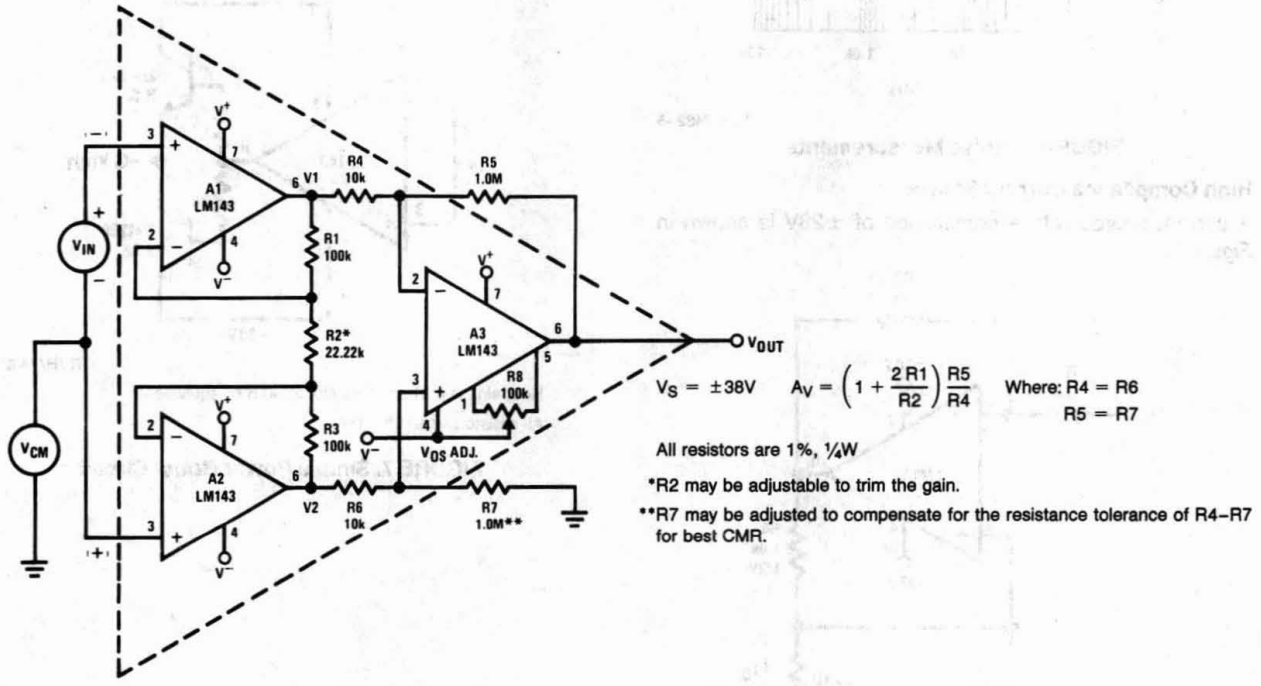
An instrumentation amplifier with ±34V common-mode range, high input impedance and a gain of X1000 is shown in *Figure 3*.

For a differential input signal, V_{IN}, A1 and A2 act as non-inverting amplifiers of gain A_{V1} = 1 + (2R1/R2), where R1 = R3. However, the gain is unity for common-mode signals since voltages V1 and V2 are in phase, and no current flow is developed through R1, R2 and R3. The second stage is simply an op amp connected as a simple differential amplifier of gain, A_{V2} = (R5/R4), where R5 = R7 and R4 = R6. The total gain of the instrumentation amplifier is

$$A_V = \left(1 + \frac{2\,R1}{R2}\right)\left(\frac{R5}{R4}\right) = \left(1 + \frac{2 \times 100k}{22.22k}\right)\left(\frac{1.0M}{10k}\right)$$

$$= 1000$$

R7 may be adjusted to take up the resistance tolerances of R4, R5 and R6 for best common-mode rejection (CMR). Also, R2 may be made adjustable to vary the gain of the instrumentation amplifier without degrading the CMR.



V_S = ±38V $A_V = \left(1 + \frac{2\,R1}{R2}\right)\frac{R5}{R4}$ Where: R4 = R6, R5 = R7

All resistors are 1%, ¼W

*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4–R7 for best CMR.

TL/H/7432–3

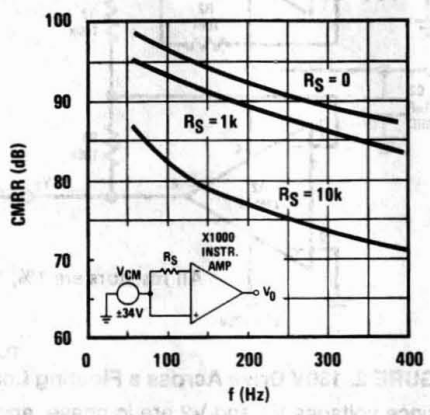
FIGURE 3. Wide Common-Mode Range Instrumentation Amplifier

Laboratory evaluation of this circuit revealed noise and CMR data as follows:

i) Frequency response with 10k load and A_V = 1000: −3.0 dB at 8.9 kHz

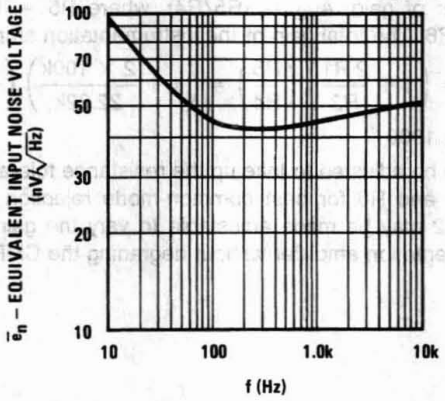
ii) CMR measurements (common-mode signal of ±34 Vp-p) in *Figure 4*

iii) Noise measurements in *Figure 5*



TL/H/7432-4

FIGURE 4. Common-Mode Rejection Measurements

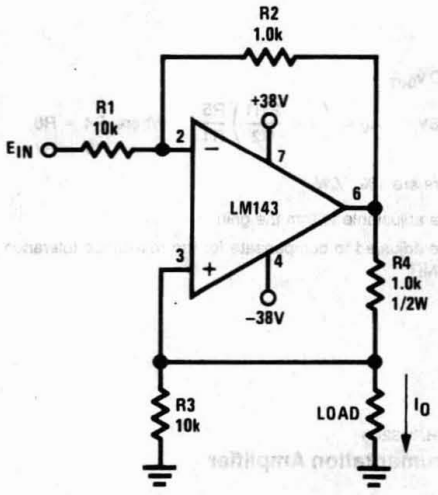


TL/H/7432-5

FIGURE 5. Noise Measurements

High Compliance Current Source

A current source with a compliance of ±28V is shown in *Figure 6*.



TL/H/7432-6

All resistors 1% metal film, ¼W unless otherwise specified.

FIGURE 6. High-Compliance Current Source

The non-inverting input of the op amp senses the current through R4 to establish an output current, I_O proportional to the input voltage. The expression for I_O is

$$I_O = -\frac{E_{IN}\,R2}{R1\,R4} = -\frac{0.1\text{ mA}}{V}E_{IN}.$$

R3 keeps the circuit stable under any value of load resistance. Measured circuit performance is as follows:

I_{OMAX} = ±3.5 mA at E_{IN} = ±35V

R_{OUT} = 2 MΩ at I_{OUT} = ±2.0 mA

CURRENT BOOSTED APPLICATIONS

Because of the high voltage capability of the LM143, some thought must be given for the selection of the minimum load resistance. At an ambient temperature of 25°C, the LM143 can dissipate 680 mW. Worst case dissipation arises when the load resistance R_L is connected to one supply and V_O = 0. Then the amplifier sources I_O = (38V/R_L) with 38V internal voltage drop. During this condition,

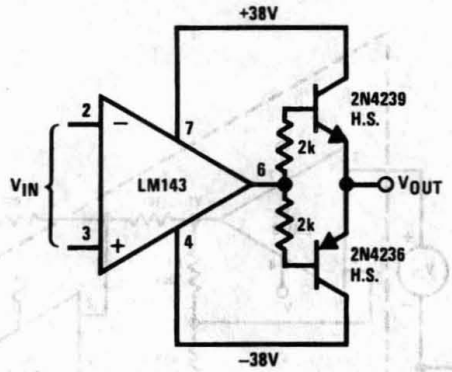
$$P_{MAX} = 680\text{ mW} = \frac{E_L{}^2}{R_L} = \frac{(38V)^2}{R_L}$$

$$\text{or } R_L = \frac{1444V^2}{680\text{ mW}} \approx 2.1\text{ k}\Omega$$

Hence, load resistances less than 2k will cause excessive power dissipation.

Simple Power Boost Circuit

For loads less than 2 kΩ, a power boost circuit should be added. The simple booster shown in *Figure 7* has the advantage of minimal parts count, but crossover distortion is noticeable and there is no short circuit protection; hence, either the LM143 or the boost transistors may fail under short circuit conditions.



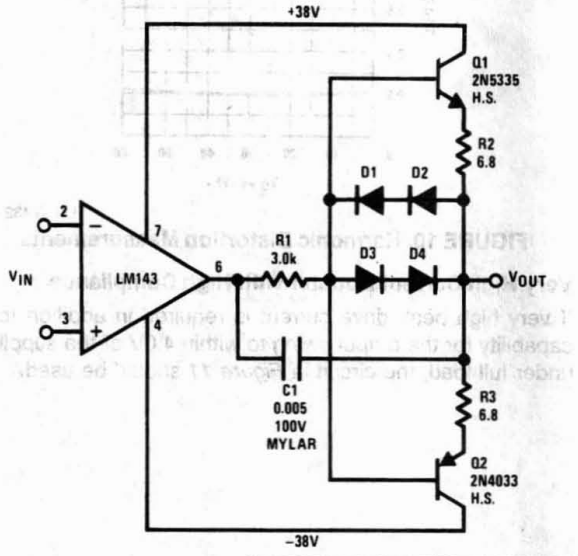
TL/H/7432-7

Heat sink is a Thermalloy No. 2230-5 or equivalent.
All resistors are 10%, 1W.

FIGURE 7. Simple Power Boost Circuit

100 mA Current Boost Circuit

With the addition of 4 diodes, a resistor and a capacitor, the booster circuit can be short circuit protected at 100 mA as shown in *Figure 8*.



TL/H/7432–8

Heat sink is a Thermalloy No. 2230-5 or equivalent.

All diodes are 1N914.

All resistors are ½W, 10%.

FIGURE 8. 100 mA Current Boost Circuit

R1 protects the LM143 by limiting the maximum drive current to (38V/3.0k) ≅ 12.5 mA, thereby keeping safely within the device dissipation limit of 680 mW. D1—D4 in conjuction with R2 and R3 protect the output transistors Q1 and Q2 by shunting the output drive current if the voltage drop across R2 or R3 exceeds 0.7V.

Breadboard Data:

i) Frequency Response: Limited by LM143 frequency response and slew rate.

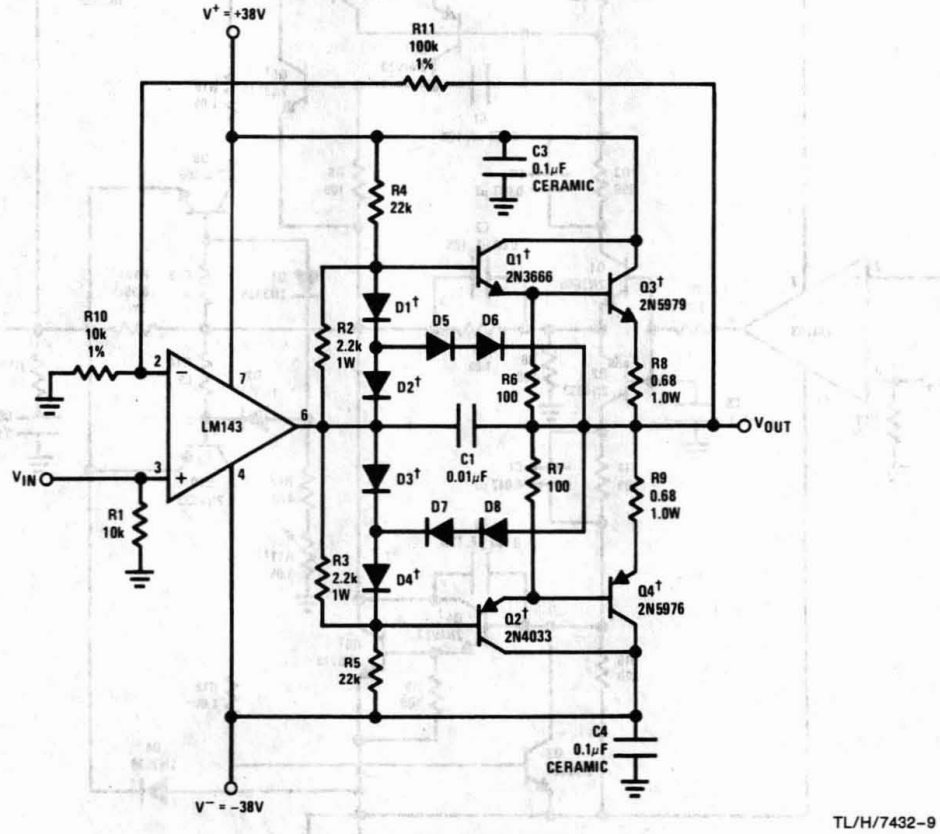
ii) Step response for unity gain, voltage follower configuration: Less than 10% overshoot for 1.0V step with 0.01 μF capacitive load, 50% overshoot with 0.47 μF capacitive load. The circuit is unconditionally stable for capacitive loads.

iii) Output Voltage: ±33 Vp-p into 400Ω load

1.0 Amp Class AB Current Booster

If crossover distortion is objectionable and currents of up to 1.0A are needed, the circuit in *Figure 9* should be used.

The output of the LM143 drives a class AB complementary output stage. The quiescent current for the output stage is set by the current flow through R4, R5 and diodes D1–D4. The diodes D1–D4 are on a common heat sink with the output transistors Q3 and Q4 so that the voltage drops across the diodes and base-emitter junctions of the output



TL/H/7432–9

†Put on common heat sink, Thermalloy 6006B or equivalent.

All diodes are 1N3193.

All resistors are 10%, ¼W except as noted.

FIGURE 9. 1 Amp Class AB Current Booster with Short Circuit Protection

transistors will track with temperature. Normally, R4 and R5 supply the current drive for the output Darlingtons, Q1, Q3 and Q2, Q4, but if additional drive is needed, the LM143 supplies the remainder through R2 and R3. For short circuited load, the drive current is bypassed around the output transistors through D1, D5 and D6 during the positive half cycle and through D4, D7 and D8 during the negative half cycle. Drive current bypassing, or output current limiting, occurs whenever R8 or R9 sees more than one diode drop (≅ 0.7V). An expression for the maximum output current is

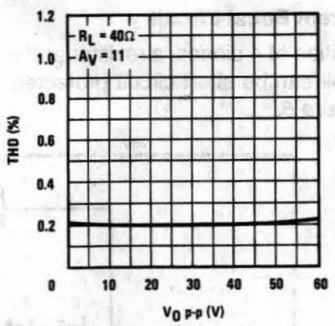
$$I_{MAX} \cong \frac{0.7V}{0.68\Omega}$$

$$I_{MAX} \cong 1.0A.$$

Capacitor C1 stabilizes the circuit under most feedback and load conditions and C3 and C4 bypass the power supply. Measured performance is as follows:

i) Maximum output voltage with $R_L = 40\Omega$: +29.6V, −28V with $V_S = \pm 38\ V_{DC}$.

ii) Harmonic distortion measurements of *Figure 10* were measured with a closed loop gain of 10.

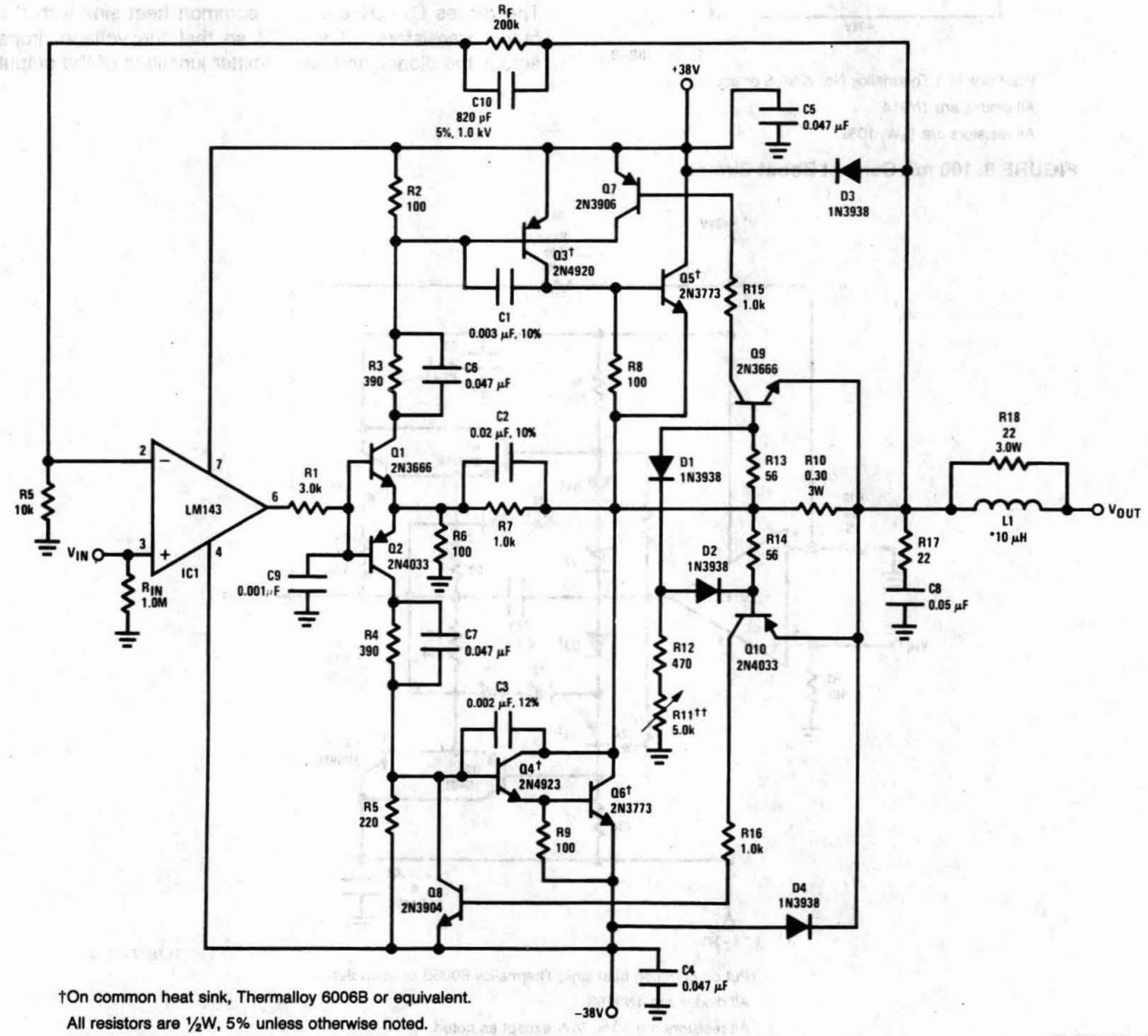


TL/H/7432–10

FIGURE 10. Harmonic Distortion Measurements

Very High Current Booster with High Compliance

If very high peak drive current is required in addition to a capability for the output swing to within 4.0V of the supplies under full load, the circuit in *Figure 11* should be used.



†On common heat sink, Thermalloy 6006B or equivalent.

All resistors are ½W, 5% unless otherwise noted.

All capacitors are 20%, 100V, ceramic disc unless otherwise noted.

††Output current limit adjust.

TL/H/7432–11

FIGURE 11. Very High Current Booster with High Compliance

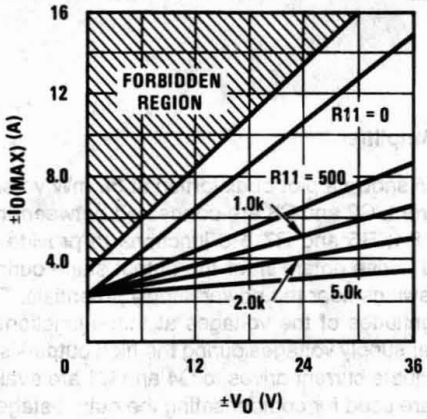
Excluding the LM143, the current booster has three stages. The first stage is made up of Q1 and Q2 which level shifts and boosts the current output of the LM143 to about 100 mA. Q3 and Q4 further boost the output of Q1 and Q2 to about 1.0A. Q5 and Q6 then have adequate drive to source and sink at least 10A. There is no quiescent current path when the output voltage is zero since Q1 and Q2 are biased off.

The short circuit protection circuit is made up of Q7 and Q9 on the positive side and Q8 and Q10 on the negative side. Q9 or Q10 turns on as soon as $V_{BE} \cong 0.7V$ appears across R10 when the output terminal is shorted to ground. Then Q7 or Q8 bypass the drive to the output devices, Q5 and Q6. Since R10 is 0.3Ω, current limiting under short circuited output occurs at 2.3A and is relatively independent of the current limit adjustment resistor, R11. An expression for the maximum output current, $I_{OUT\ MAX}$, with V_{OUT} and R11 as variables is

$$|I_{OUTMAX}| \cong \frac{\frac{(|V_{OUT}| - V_{D1})\,R13}{R11 + R12 + R13} + V_{BE9}}{R10}$$

$$\cong \frac{\frac{(|V_{OUT}| - 0.7)\,56\Omega}{R11 + 526\Omega} + 0.7V}{0.3\Omega}$$

The equation is valid for both output polarities. The plot in *Figure 12* superimposes the above equation on the maximum operating area curve for the 2N3773 and illustrates the safe area protection feature.



TL/H/7432–12

FIGURE 12. Maximum Output Current as a Function of R11 and V_{OUT}

The diodes, D1 and D2, are in the circuit to keep the base-emitter junctions of Q9 and Q10 from being reversed biased during the opposite polarity output voltage swings. C1, C2, C3, C6, C7 and C9 are judiciously inserted in the circuit to prevent oscillation. R17, R18, C8 and L1 are used in the circuit to maintain stability under all load conditions. Diodes D3 and D4 provide protection for inductive loads.

All measurements taken with a 4Ω load and ±38V supplies unless otherwise stated:

i) Maximum power out: 144 Wrms

ii) Frequency response:
   a) −3.0 dB at 10 kHz at full power
   b) −3.0 dB at 11.5 kHz at 10 Vp-p out

iii) Maximum output voltage: ±34V

iv) Maximum capacitive load: 10 μF with 10% overshoot for a small signal step response

v) DC deadband: 20 μV

vi) Quiescent current: 12.7 mA (positive supply), 2.1 mA (negative supply)

vii) Input impedance: 1 MΩ

viii) Voltage gain: 21

HIGH POWER APPLICATIONS

90 Wrms Audio Power Amplifier

A circuit diagram of an audio power amplifier which is capable of 90 Wrms into a 4Ω speaker or 70 Wrms into an 8Ω speaker is given in *Figure 13*. The circuit features safe area, short circuit and overload protection, harmonic distortion less than 0.1% at 1.0 kHz, and an all NPN output stage.

The output of the LM143 drives a quasi-complementary output stage made up of Q1, Q2, Q3 and Q4. This quasi-complementary circuit, which makes possible an all NPN output, was chosen over the complementary output circuit due to the lack of low cost high voltage power PNP transistors.

Safe area current limiting occurs whenever the output current is

$$|I_{OUTMAX}| = \frac{\frac{(|V_{OUT}| - V_{D3})\,R11}{R11 + R13} + V_{BE5}}{R12}$$

where R11 = R15 = 330Ω,

R13 = R14 = 3.9k,

R12 = R16 = 0.25Ω and

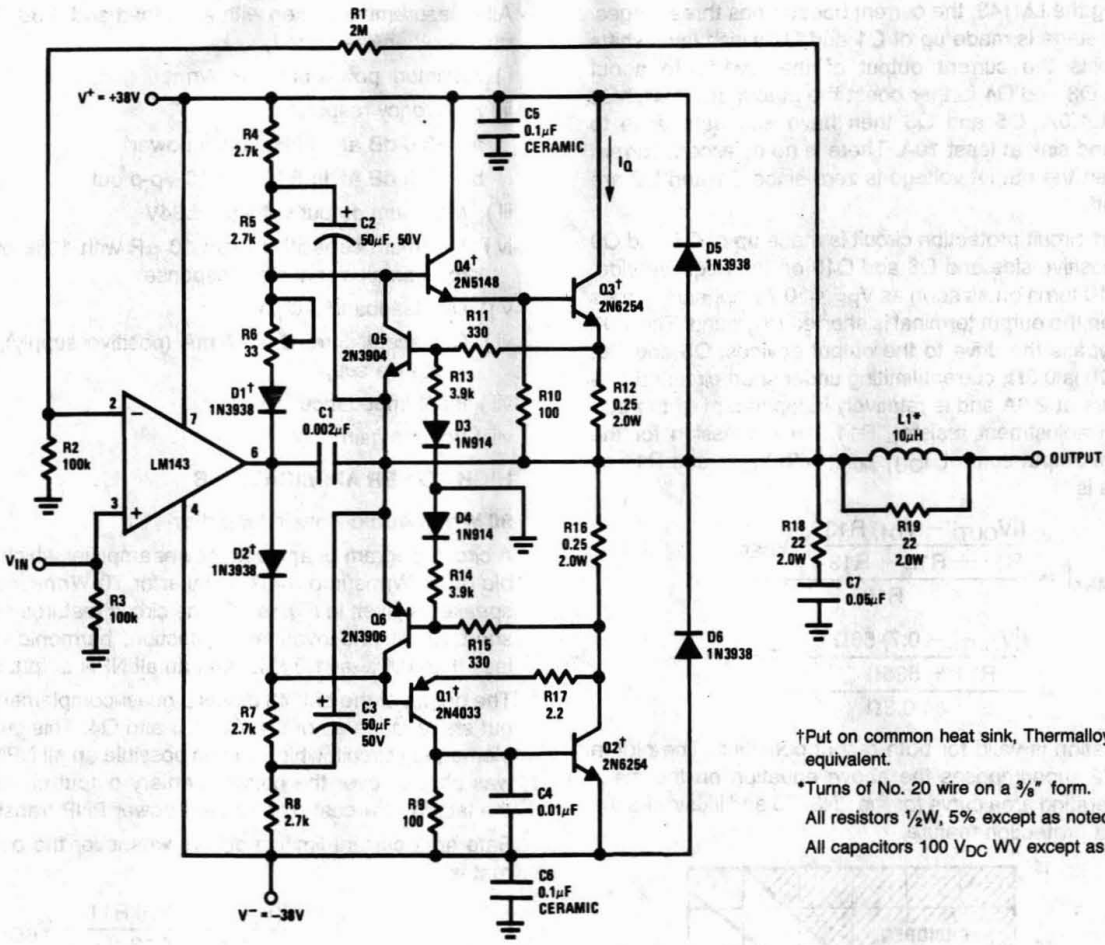
$V_{BE5} \cong V_{BE6} \cong V_{D3} \cong V_{D4} \cong 0.7V$.

If the output is shorted, the above equation simplifies to

$$I_{OUTMAX} = \frac{V_{BE5}}{R12} \cong \frac{0.7V}{0.25\Omega} = 2.8A$$

If the output voltage is 30V,

$$I_{OUTMAX} = \frac{\frac{(30V - 0.7V)\,330}{4.23k} + 0.7V}{0.25\Omega} \cong \frac{2.3 + 0.7V}{0.25} = 12A$$



†Put on common heat sink, Thermalloy 6006B or equivalent.

*Turns of No. 20 wire on a ⅜" form.

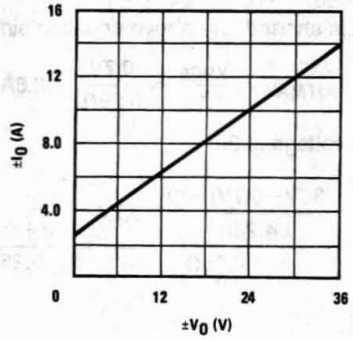
All resistors ½W, 5% except as noted.

All capacitors 100 V_{DC} WV except as noted.

TL/H/7432–13

FIGURE 13. 90W Audio Power Amplifier

The maximum output current, $I_{O(MAX)}$, versus V_O is plotted in *Figure 14*. D4 and D3 are in the circuit to keep Q5 off during the negative half of the output voltage cycle and Q6 off during the positive half cycle.

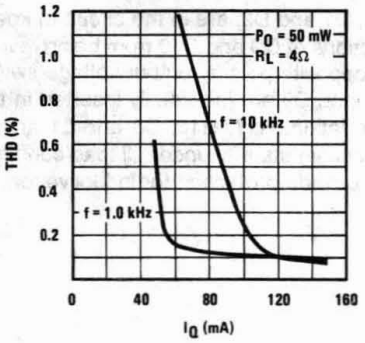


TL/H/7432–14

FIGURE 14. Output Current Limiting as a Function of Output Voltage

The output stage is biased into class AB operation by using the resistor string R4, R5, R7 and R8 to set the voltage drops across R6, D1 and D2, which then determine the quiescent current through the output transistors. These diodes are thermally coupled to the output devices to track their base-emitter junction voltages with temperature. Low distortion at low power levels is achieved by adjusting R6 to set the quiescent current through Q3 and Q2 to about 100 mA.

Figure 15 shows a plot of distortion at 50 mW versus quiescent current. C2 and C3 are connected between the output and the R4, R5 and R7, R8 junctions to provide a "bootstrapped" drive potential for the output stage during output voltage swings near the power supply potentials. The absolute magnitudes of the voltages at these junctions exceed the power supply voltages during the high outputs swings so that adequate current drives to Q4 and Q1 are available. C1 and C4 are used for compensating the output stage. C5 and C6 are used for power supply bypassing. R18, C7, R19 and L1 are included in the circuit to keep the amplifier stable under all load conditions. D5 and D6 provide protection for inductive loads.



TL/H/7432–15

FIGURE 15. Quiescent Current vs Distortion

The input impedance of the audio amplifier is simply the value of R3. To keep the output offset voltages to a minimum, R3 ≅ R1 ‖ R2. The voltage gain is

$$A_V = 1 + \frac{R1}{R2} = 1 + \frac{2.0M}{100k} = 21$$

The following data was taken with $V_S = \pm 38V$:

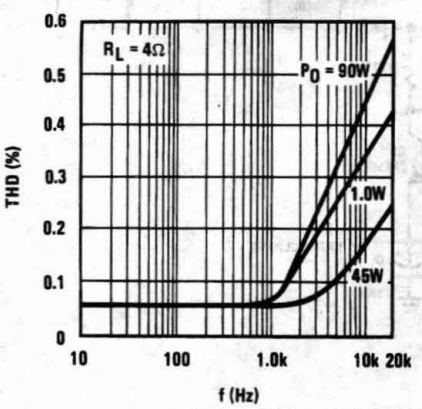
i) Maximum power output before visible clipping:
   a) 90 Wrms at 1.0 kHz into 4Ω load
   b) 70 Wrms at 1.0 kHz into 8Ω load

ii) Distortion measurement: distortion versus frequency and power is plotted in *Figures 16* and *17*.

iii) Maximum capacitive load: 20 μF

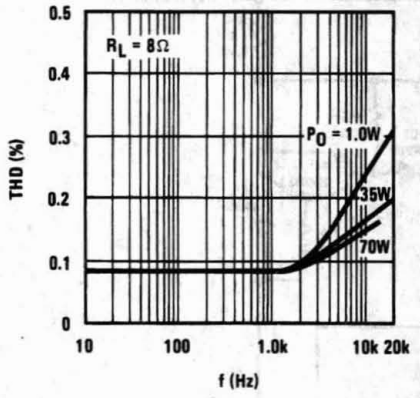
iv) Output noise, 10 Hz to 20 kHz: 100 μVrms

v) Frequency response:
   a) Small signal (1.0 Vrms into 4.0Ω): −3.0 dB at 40 kHz
   b) Power (90W into 4Ω): −3.0 dB at 29 kHz
   c) Power (70W into 8Ω): −3.0 dB at 30 kHz



TL/H/7432–16

FIGURE 16. Distortion vs Frequency, $R_L = 4\Omega$



TL/H/7432–17

FIGURE 17. Distortion vs Frequency, $R_L = 8\Omega$

POWER SUPPLY CIRCUITS

The ability of the LM143 to withstand up to 80V can be exploited fully in the design of regulated power supplies. The circuits to be described use a zener reference voltage, an IC voltage amplifier, and a discrete power transistor pass element. If care is taken to keep the voltage drop across the pass element within 40V, standard three terminal voltage regulators such as the LM340, LM120, etc. may be used as pass elements and significantly decrease parts count and circuit complexity. Circuits using this approach are given in the LM340 application note (see AN-103).

A Tracking ±65V Supply with 500 mA Output

A tracking power supply circuit can be made by modifying the circuit for the 130 Vp-p driver circuit. The modified circuit is given in *Figure 18*.

A 2N4275 is used as a stable zener voltage reference of about 6.5V. Its output is amplified from one to about 10 times by the circuitry associated with IC1. The output of IC1 is applied through R10 to the Darlington connected transistors, Q2 and Q3. The feedback resistor, R5, one end of which is connected to the V^+ output node, is made variable so that the V^+ output voltage will vary from 6.5V to about +65V. The V^+ output is applied to a unity gain inverting power amplifier to generate the V^- output voltage. The output circuit of the unity gain inverter uses a composite PNP, Q4 and Q5, to provide the current boost.

Since the input terminals of A2 are at ground potential, the positive supply lead cannot be grounded; instead, it is connected to the output of a 4.7V zener diode, D8, to keep within the input common-mode range.

C1, C3 and C4 are used for decreasing the power supply noise. C2 is used in bypassing most of the noise generated by the reference voltage and C5 and C6 are used to reduce the voltage output noise. Short circuit protection is provided by D1, D2, D3, R10 and R14 on the positive side and by D4, D5, R11 and R15 on the negative side. The short circuit protection circuit is the same as the one used in the 1.0A current booster circuit.

The short circuit current is given by

$$I_{MAX} \cong \frac{V_{BE}}{R14} \cong \frac{V_{BE}}{R15}$$

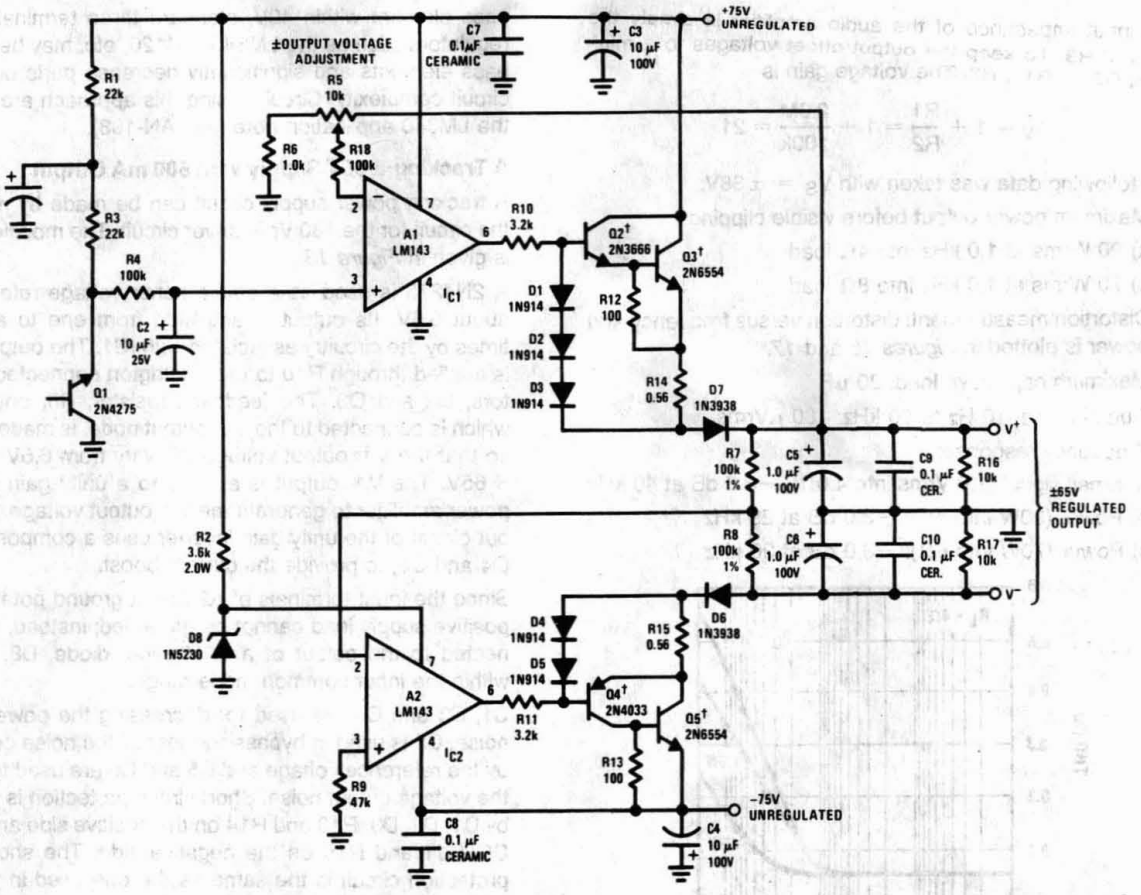
$$\cong \frac{0.7}{0.56} = 1.25A$$

where V_{BE} = voltage drop across a diode.

±65V, 1.0A Power Supply with Continuously Variable Output Current and Voltage

If a continuously variable output current as well as output voltage supply is needed, a power supply circuit given in *Figure 19* will do the job. It has an output range from 7.1V to 65V with an adjustable output current range of 0 to 1.0A.

Basically, the power supply circuit is a non-ideal voltage source in series with a non-ideal current source. A reference voltage of approximately 6.5V is obtained by zenering the base-emitter junction of the 2N4275. The positive temperature coefficient of the zenering voltage is compensated by the negative temperature coefficient of the forward biased base-collector junction. The output of the voltage reference goes to the variable gain power amplifier made up of IC2, Q6, Q7 and their associated components and to a reference current source made up of Q2, D1 and components around them. The variable gain power amplifier multiplies the reference voltage from one to ten times due to the variable feedback resistor, R17. since the maximum current output of IC2 is at most 20 mA, the Darlington connected Q6 and Q7 are used to boost the available output current to 500 mA.

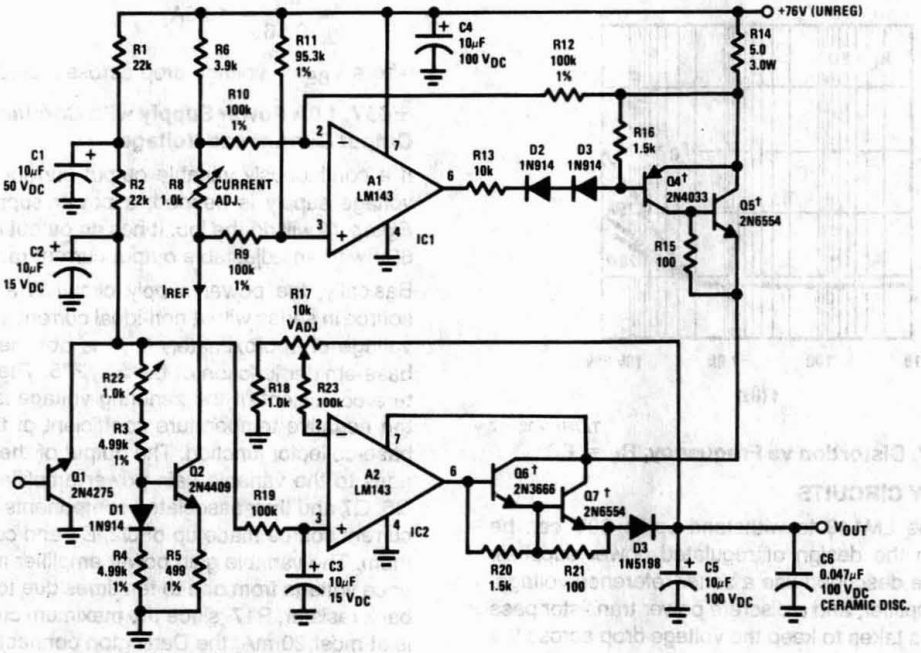


†Put on common heat sink, Thermalloy 6006B or equivalent.

All resistors are ½W, 5%, except as noted.

TL/H/7432–18

FIGURE 18. Tracking 65V, 1A Power Supply with Short Circuit Protection



†Put on common heat sink, Thermalloy 6006B or equivalent.

All resistors ½W, 10% unless otherwise noted.

All capacitors 20%.

TL/H/7432–19

FIGURE 19. 1A, 65V Power Supply with Variable Current Limit

Breadboard Data for the Tracking 65V Power Supply

$V_{IN} = \pm 75V$, $I_{OUT} = \pm 500$ mA, $T_j = 25°C$, $T_A = 25°C$, $V_{OUT} = \pm 40V$, unless otherwise specified.

Parameter	Conditions	Measured Data	
		$+V_{OUT}$	$-V_{OUT}$
Load Regulation	$0 \le I_{OUT} \le 500$ mA	0.5 mV	1.0 mV
Line Regulation	$\lvert\pm 50V\rvert \le V_{IN} \le \lvert\pm 80V\rvert$ $I_{OUT} = \pm 100$ mA $I_{OUT} = \pm 500$ mA	 175 mV 169 mV	 176 mV 173 mV
Quiescent Current	$I_{OUT} = 0$	Pos. Supply 28.22 mA	Neg. Supply 6.55 mA
Output Noise Voltage*	10 Hz ≤ f ≤ 100 kHz	0.125 mV	0.135 mV
Ripple Rejection	$I_{OUT} = \pm 20$ mA, f = 120 Hz	−72.5 dB	−63.4 dB
Output Voltage Drift*		3.38 mV/°C	3.43 mV/°C

*The output noise and drift are due primarily to the zener reference.

Measured Performance of the 1A, 65V Power Supply

$V_{IN} = +76V$, $I_{OUT} = 500$ mA, $T_j = 25°C$, $V_{OUT} = +40V$ unless otherwise specified

Parameter	Conditions	Measured Data
Load Regulation	$0 \le I_{OUT} \le 500$ mA (Pulsed Load)	5.0 mV
Line Regulation	$46V \le V_{IN} \le 76V$ $I_{OUT} = 100$ mA $I_{OUT} = 500$ mA (dc Loads)	 297 mV 286 mV
Maximum Output Voltage	dc Load	68.6V
Quiescent Current		21.4 mA
Output Noise Voltage*	10 Hz ≤ f ≤ 100 kHz	0.280 mV
Ripple Rejection	$I_{OUT} = 20$ mA f = 120 Hz $\Delta V_S = 3.0$ Vp-p $\Delta V_O = 6.0$ mVp-p	66.6 dB
Loads are Pulsed Loads	200 μs Pulse Every 200 ms	

*The output noise is due primarily to zener reference

The power current source is an op amp used as a differential amplifier which senses the voltage drop across R8 and maintains this same voltage across R14. Hence, the maximum output current is

$$I_{OUT} = \frac{R8}{R14} \times I_{REF} \le \frac{1.0k}{5.0\Omega} \times 5.0\text{ mA} = 1.0A.$$

Since the output load under most conditions will not demand what the power current source can deliver, Q4 and Q5 will remain in saturation during normal operation. When Q4 and Q5 are pulled out of saturation, the output load voltage will drop until the load current just equals what is available from the power current source. Because the positive supply terminal of IC2 is tied to the collectors of Q4 and Q5, IC2 will supply just enough current drive to Q6 and Q7 to keep itself on. Hence, a current limiting resistor is unnecessary for IC2. A 10k current limiting resistor, R13, is present since the total unregulated power supply voltage is available for IC1. R6 is used to stay within the input common-mode voltage range of IC1.

I_{REF} is derived from the 6.5V reference source, Q1, by using Q2 in a current source configuration. R22 is made adjustable so that I_{REF} can be set for 5.0 mA.

CONCLUSION

The LM143 is a high performance operational amplifier suited for applications requiring supply voltages up to ±40V. The LM143 is especially useful in power supply circuits where the unregulated voltages are as high as ±40V and in amplifier circuits where output voltages greater than ±30V peak are needed. The LM143 is internally compensated and is pin-for-pin compatible with the LM741. Compared with the LM741, the LM143 exhibits an order of magnitude lower input bias currents, better than five times the slew rate and twice the output voltage swing.

APPENDIX

Toward the goal of trouble-free applications, this appendix details some of the more subtle features of the LM143 and reviews application hints pertinent both to op amps in general and the LM143 in particular. The complete schematic of the LM143 is shown in *Figure 20*.

The circuit starts drawing supply current, at supply voltages of ±4V, when current is provided to a 7.5V zener diode D5 by the collector FET Q41. The gate-channel junction of Q41 exhibits 100V breakdown as source and drain are lightly doped NPN collector and substrate material. The collector current of Q18 biases current sources Q25 through Q30 and sets the supply current at nearly zero TC.

Q19 furnishes a bias voltage, 5V above the negative supply, for the collectors of Q15, Q20 and Q22. The low impedance 2V reference (V_{B1} in *Figure 1*) for the base of Q21 appears at the emitter of Q20 and has the correct TC to insure that Q23 never saturates. Should this occur, the low resistance of Q23 would cause premature LV_{CEO} breakdown of Q21.

The input transistors, Q1 and Q2, are biased by Q13 and Q14 which have a breakdown voltage essentially equal to BV_{CBO} by virtue of the high emitter impedance, R18 and R19, relative to the low dynamic impedance of D4. In a similar way, Q18 and Q19 stand off essentially the full supply voltage. These devices have a high output impedance caused by series feedback and so hold the supply current nearly constant to prevent excessive power dissipation at high supply voltages.

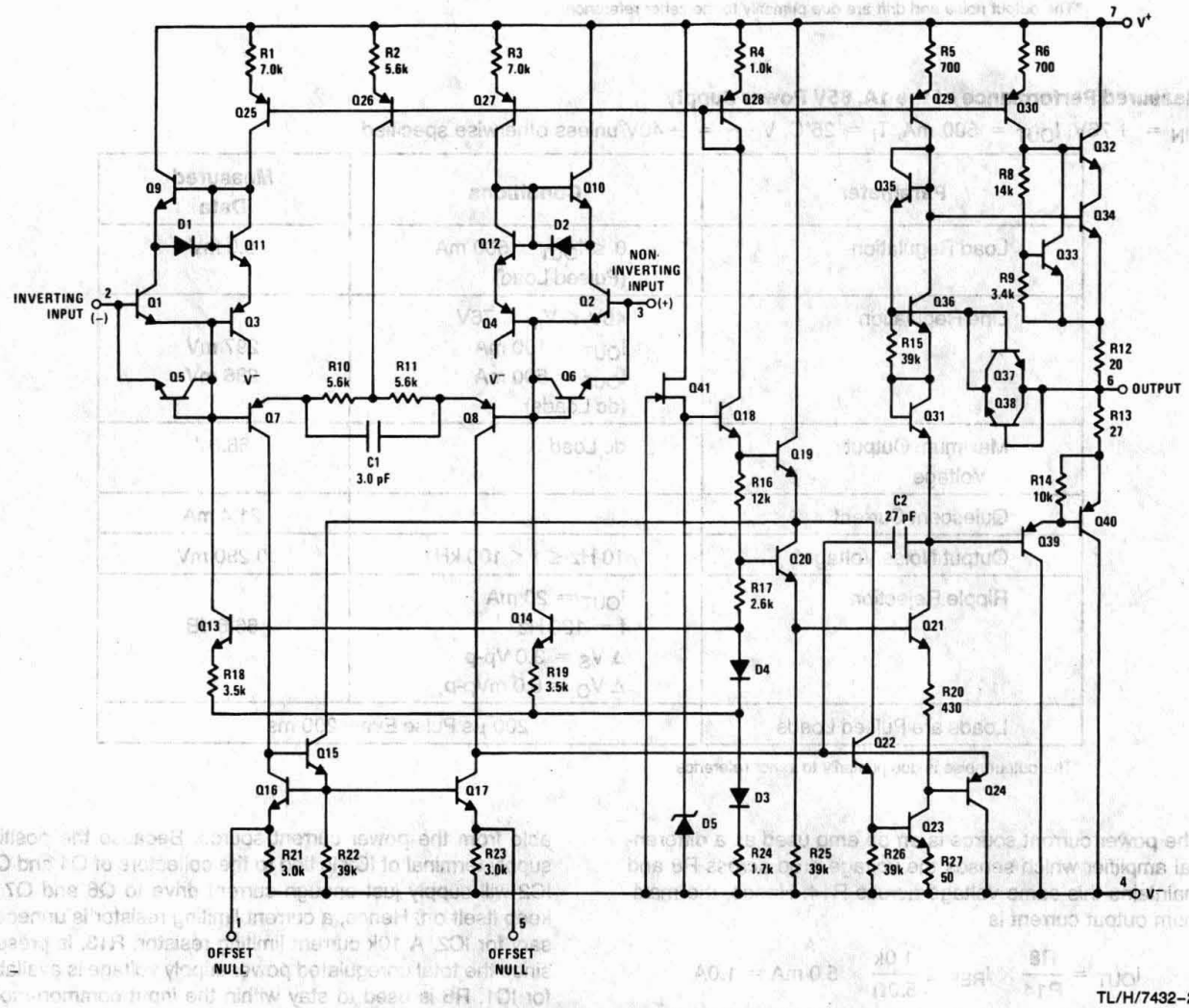


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FIGURE 20. Complete Schematic of the LM143

While the simple voltage clamping scheme, Q3 and Q4 in *Figure 1*, is adequate, it is prone to oscillation when built with high β PNPs. The more elaborate scheme of *Figure 20* prevents instability. This clamping method is similar to that used in the LM108, but allows large differential inputs to exist with complete input overvoltage protection. Q9 and Q10, which withstand the high input common-mode voltage, have a BV_{CBO}-type breakdown due to the low impedance diodes seen from the base leads and the high impedance of Q1 and Q2 (enhanced by 100% series feedback) in the emitter leads. Input overvoltage protection also holds up under high-level transient input voltages.

With a large negative-going step input, as could occur in the unity-gain voltage follower configuration, diode-connected Q6 turns "ON", protecting the emitter-base junction of Q2 from zener breakdown and subsequent long-term β degradation. At the same time, stray capacitance at the collector of Q2 is discharged by D2 through Q4 and Q12. This holds Q10 in a true BV_{CBO} mode (emitter open-circuited) and clamps the voltage across Q2 to 3 V_{BE}.

With a large positive-going step input, stray capacitance at the collectors of Q2 and Q12 is charged by the forward-biased collector junction of Q2. As before, with D2 conducting, Q10 is again in the BV_{CBO} breakdown mode. Since the inverting input can be subject to the same transients, Q1 is afforded the same protection.

Distributed capacitance associated with R10 and R11, together with the collector-base capacitance of Q26, cause a high frequency transmission pole (the "tail" pole[2]) which can degrade phase margin. This is avoided by adding a small lead capacitor, C1, which provides an alternative low-impedance signal path, thus bypassing the tail pole.

The offset null resistors, R21 and R23, are made larger than that strictly necessary to null the offset voltage. This reduces the transconductance of Q17 and, therefore, the noise gain of the active loads into R10 and R11. By this simple expedient, broadband input noise voltage is substantially reduced.

The voltage reference for the output stage (V_{B2} in *Figure 1*) is realized by actively simulating a 4-diode stack. The voltage across Q33, given by (1 + R8/R9) V_{BE}, is about 3.5V. Biased at 400 μA from Q30, the circuit presents a low impedance, less than 50Ω, to the base of Q32. Since the TC of the reference is negative, Q34 is designed to always remain out of saturation under worst-case conditions of high temperature and high output current. This avoids potential destructive breakdown of Q32.

Current limiting for Q32 and Q34 is provided by diode-connected Q37 and resistor R12. When the voltage drop across R12 turns on Q37, it removes base drive from Q34. In a similar fashion, current limiting in the negative direction is initiated when the voltage drop across R13 causes Q38 to conduct. This current is limited in Q21 by R20 to about 1 mA. When this occurs, base drive is removed from Q39.

Although output short circuits to ground or either supply can be sustained indefinitely at supply voltages lower than $\pm$22V, short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of their maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. As with all IC op amps, voltage reversal between the power supplies will almost always result in a destroyed unit.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertently contact voltages equal to those across the power supplies.

REFERENCES

1. R. J. Widlar, "Super Gain Transistors for ICs", National Semiconductor TP-11, March 1969.
2. J. E. Solomon, "The Monolithic Op Amp: A Tutorial Study", IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974.

FM Remote Speaker System

National Semiconductor
Application Note 146

INTRODUCTION

A high quality, noise free, wireless FM transmitter/receiver may be made using the LM566 VCO and LM565 PLL Detector. The LM566 VCO is used to convert the program material into FM format, which is then transformer coupled to standard power lines. At the receiver end the material is detected from the power lines and demodulated by the LM565.

The important difference between this carrier system and others is its excellent quality and freedom from noise. Whereas the ordinary wireless intercom uses an AM carrier and exhibits a poor signal-to-noise ratio (S/N), the system described here uses an FM carrier for inherent freedom from noise and a PLL detection system for additional noise rejection.

The complete system is suitable for high-quality transmission of speech or music, and will operate from any AC outlet anywhere on a one-acre homesite. Frequency response is 20–20,000 Hz and THD is under ½% for speech and music program material.

Transmission distance along a power line is at least adequate to include all outlets in and around a suburban home and yard. Whereas many carrier systems operate satisfactorily only when transmitter and receiver are plugged into the same side of the 120–240/V power service line, this system operates equally well with the receiver on either side of the line.

The transmitter is plugged into the AC line at a radio or stereo system source. The signal for the transmitter is ideally taken from the MONITOR or TAPE OUT connectors provided on component system Hi-Fi receivers. If these outputs are not available, the signal could be taken from the main or extra speaker terminals, although the remote volume would then be under control of the local gain control. The carrier system receiver need only be plugged into the AC line at the remote listening location. The design includes a 2.5W power amplifier to drive a speaker directly.

TRANSMITTER

Two input terminals are provided so that both LEFT and RIGHT signals of a stereo set may be combined for mono transmission to a single remote speaker if desired.

The input signal level is adjustable by R_1 to prevent overmodulation of the carrier. Adding C_2 across each input resistor R_7 and R_8 improves the frequency response to 20 kHz as shown in *Figure 5*. Although casual listening does not demand such performance, it could be desired in some circumstances.

The VCO free-running frequency, or carrier frequency f_c, determined by R_4 and C_4 is set at 200 kHz which is high enough to be effectively coupled to the AC line. VCO sensitivity under the selected bias conditions with $V_S = 12V$ is about $\pm 0.66\ f_c/V$. For minimum distortion, the deviation should be limited to ±10%; thus maximum input at pin #5 of the VCO is ±0.15V peak. A reduction due to the summing network brings the required input to about 0.2V rms for ±10% modulation of f_c, based on nominal output levels from stereo receivers. Input potentiometer R_1 is provided to set the required level. The output at pin #3 of the LM566, being a frequency modulated square wave of approximately 6V pk-pk amplitude, is amplified by a single transistor Q_1 and coupled to the AC line via the tuned transformer T_1. Because T_1 is tuned to f_c, it appears as a high impedance collector load, so Q_1 need not have additional current limiting. The collector signal may be as much as 40–50V pk-pk. Coupling capacitor C_8 isolates the transfomer from the line at 60 Hz.

A Voltage regulator provides necessary supply rejection for the VCO. The power transformer is sized for peak secondary voltage somewhat below the regulator breakdown voltage spec (35V) with a 125V line.

RECEIVER

The receiver amplifies, limits, and demodulates the received FM signal in the presence of line transient interference sometimes as high as several hundred volts peak. In addition, it provides audio mute in the absence of carrier and 2.5W output to a speaker.

The carrier signal is capacitively coupled from the line to the tuned transformer T_1. Loaded Q of the secondary tank T_1C_2 is decreased by shunt resistor R_1 to enable acceptance of the ±10% modulated carrier, and to prevent excessive tank circuit ringing on noise spikes. The secondary of T_1 is tapped to match the base input impedance of Q_{1A}. Recovered carrier at the secondary of T_1 may be anywhere from 0.2 to 45V p-p; the base of Q_{1A} may see pk-to-pk signal levels of from 12 mV to 2.6V.

Q_{1A}–Q_{1D} operates as a two-stage limiter amplifier whose output is a symmetrical square wave of about 7V pk-pk with rise and fall times of 100 ns.

The output of the limiting amplifier is applied directly to the mute peak detector, but is reduced to 1V pk–pk for driving the PLL detector.

The PLL detector operates as a narrow band tracking filter which tracks the input signal and provides a low-distortion demodulated audio output with high S/N. The oscillator within the PLL is set to free-run at or near the carrier frequency of 200 kHz. The free-run frequency is $f_o \approx 1/(3.7\ R_{16}C_{13})$. Since the PLL will lock to a carrier near its free-run frequency, an adjustment of R_{16} is not strictly necessary; R_{16} could be fixed at 4700 or 5100Ω. Actually, the PLL with the indicated value of C_{11} can lock on a carrier within about ±40 kHz of its center frequency. However, rejection of impulse noise in difficult circumstances can be maximized by carefully adjusting f_o to the carrier frequency f_c. Adding

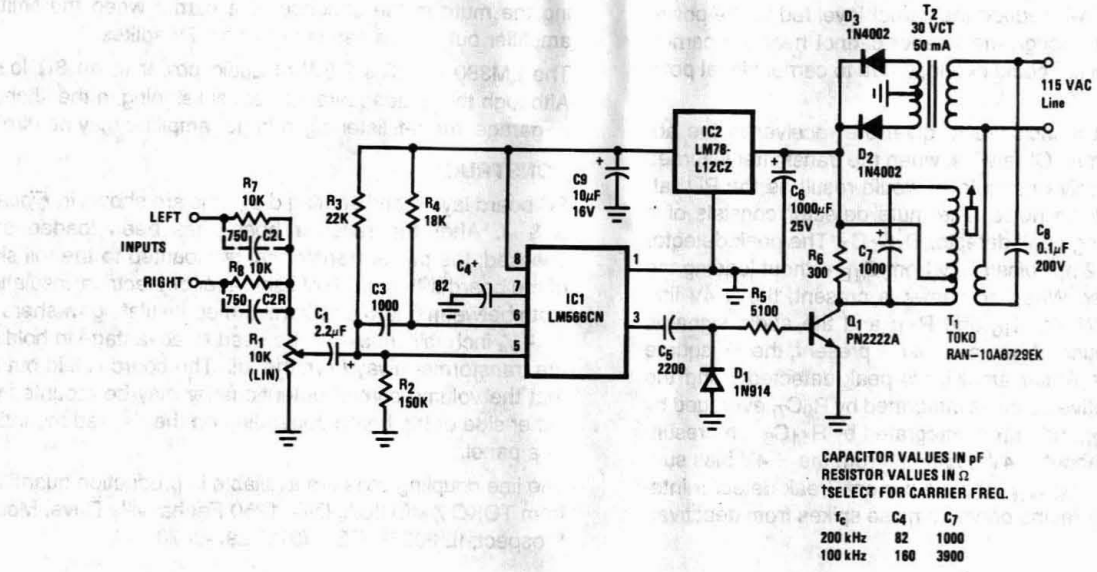

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FIGURE 1. Carrier System Transmitter

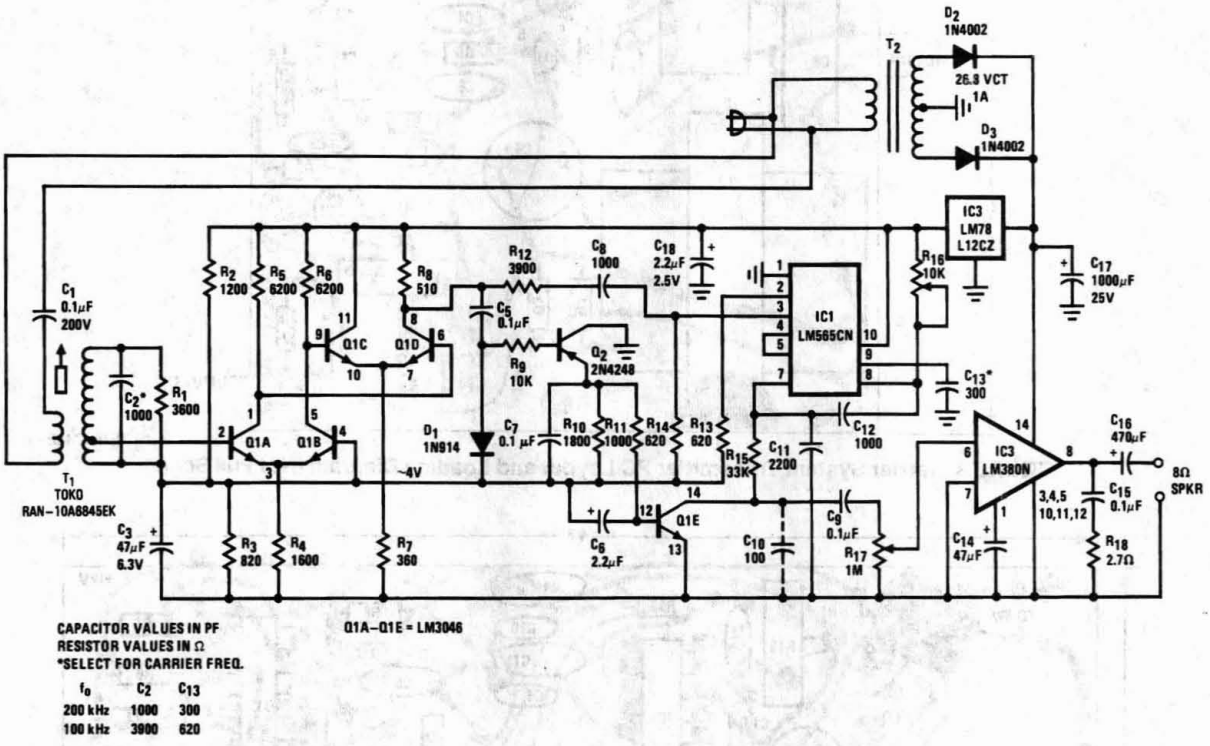

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FIGURE 2. Carrier System Receiver

C_{10} = 100 pF will reduce the carrier level fed to the power amplifier. Even though the listener cannot hear the carrier, the audio amplifier could overload due to carrier signal power.

A mute circuit is included to quiet the receiver in the absence of a carrier. Otherwise, when the transmitter is turned OFF, an excessive noise level would result as the PLL attempts to lock on noise. The mute detector consists of a voltage doubling peak detector $D_1Q_2C_7$. The peak detector shunts the 1–2 mA bias away from Q_{1E} without loading the limiter amplifier. When no carrier is present, the +4V line biases Q_{1E} ON via R_{10} and R_{11}; and the audio signal is shorted to ground. When a carrier is present, the 7V square wave from the limiter amplifier is peak detected*, and the resultant negative output is integrated by R_9C_7, averaged by R_{10} across C_7, and further integrated by $R_{11}C_6$. The resultant output of about −4V subtracts from the +4V bias supply, thus depriving Q_{1E} of base current. Peak detector integration and averaging prevents noise spikes from deactivating the mute in the absence of a carrier when the limiter amplifier output is a series of narrow 7V spikes.

The LM380 supplies 2.5W of audio power to an 8Ω load. Although this is adequate for casual listening in the kitchen or garage, for hi-fi listening, a larger amplifier may be direct.

CONSTRUCTION

PC board layout and stuffing diagrams are shown in *Figures 3 & 4*. After the receiver board has been loaded and checked, the power transformer is mounted to the foil side of the board with a piece of fish-paper or electrical insulating cloth between board and transformer. Insulating washers of 1/16–1/4 inch thickness can be used to advantage in holding the transformer away from the foil. The board is laid out so that the volume control potentiometer may be mounted on either side of the board depending on the desired mounting to a panel.

The line coupling coils are available in production quantities from TOKO AMERICA, INC. 1250 Feehanville Drive, Mount Prospect, IL 60056. TEL: (312) 297-0070

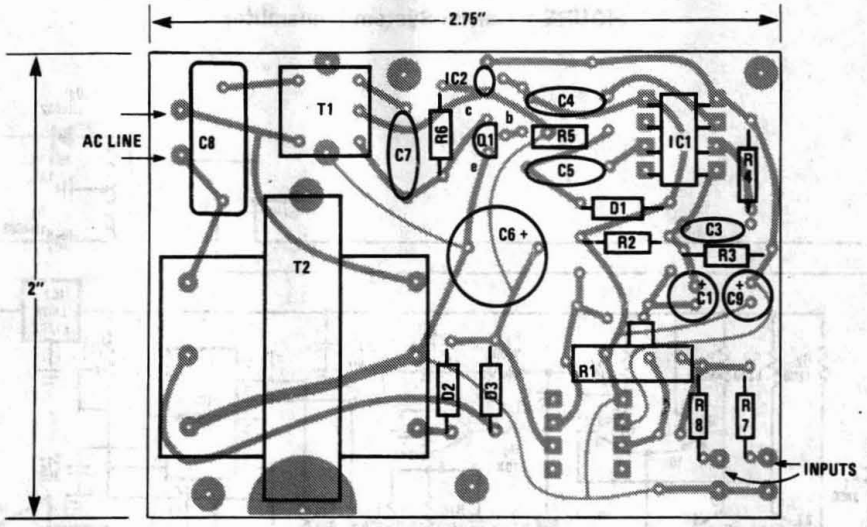

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FIGURE 3. Carrier System Transmitter PC Layout and Loading Diagram (Not Full Scale)

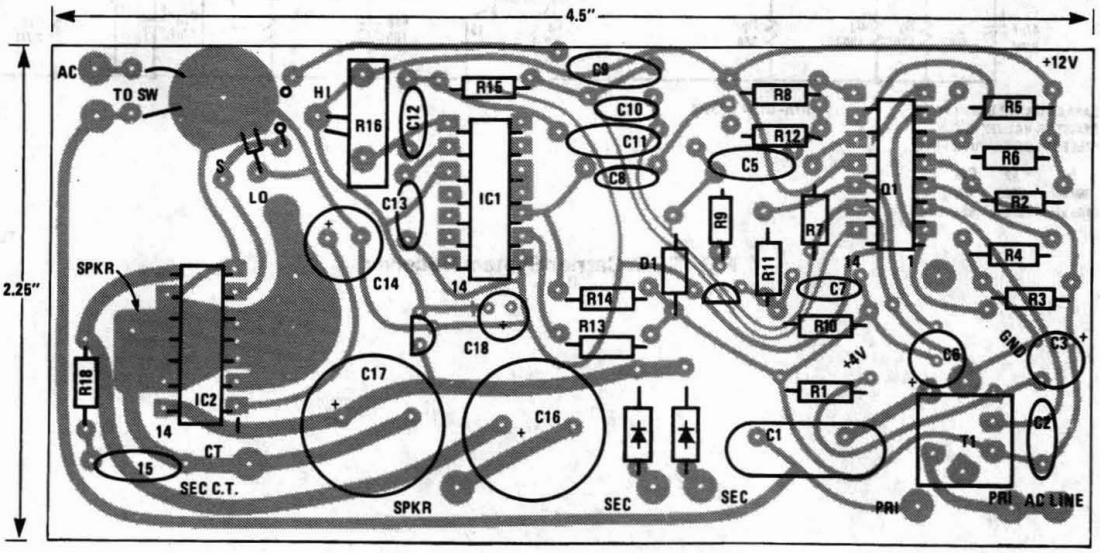

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FIGURE 4. Carrier System Receiver PC Layout and Loading Diagram (Not Full Scale)

ADJUSTMENT

Adjustments are few and extremely simple. Transmitter carrier frequency f_c is fixed near 200 kHz by R_4 and C_4; the exact frequency is unimportant. T_1 for both transmitter and receiver are tuned for maximum coupling to and from the AC line. Plug in both receiver and transmitter; no carrier modulation is necessary. Insure that both units are operative. Observe or measure with an AC VTVM the waveform at T_1 secondary in the receiver. Tune T_1 of the transmitter for maximum observed signal amplitude. Then tune T_1 of the receiver for a further maximum. Repeat on the transmitter, then the receiver. Tuning is now complete for the line coupling transformers and should not have to be repeated for either. If the receiver is located some distance from the transmitter in use, or on the opposite side of the 110–220V service line, a re-adjustment of the receiver T_1 may be made to maximize rejection of SCR dimmer noise. The receiver PLL free-running frequency is adjusted by R_{16}. Set R_{16} near the center of its range. Rotate slowly in either direction until the PLL loses lock (evidenced by a sharp increase in noise and a distorted output). Note the position and then repeat, rotating in the other direction. Note the new position and then center R_{16} between the two noted positions. A fine adjustment may be made for minimum noise with an SCR dimmer in operation. The final adjustment is for modulation amplitude at the transmitter. Connect the audio signal to the transmitter input and adjust the input potentiometer R_1 for a signal maximum of about 0.1V rms at the input to the LM566. Adjustment is now complete for both transmitter and receiver and need not be repeated.

A STEREO SYSTEM

If full stereo or the two rear channels of a quadraphonic system are to be transmitted, both transmitter and receiver must be duplicated with differing carriers. Omit R_8 and include R_7 & C_2 on the transmitter if desired. Carriers could be set to 100 and 200 kHz for the two channels. Actually, they need only be set a distance of 40 kHz apart.

PERFORMANCE

Overall S/N is about 65 dB. Distortion is below about ¼% at low frequencies, and in actual program material it should not exceed ½% as very little signal power occurs in music above about 1 kHz.

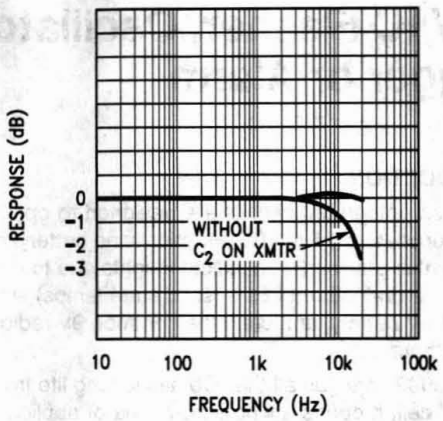

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FIGURE 5. Overall System Performance Transmitter Input to Input of Receiver Power Amplifier

The 2.5W audio amplifier provides an adequate sound level for casual listening. The LM380 has a fixed gain of 50. Therefore for a 2.5W max output, the input must be 89 mV. This is slightly less than the ±10% deviation level so we are within design requirements. Average program level would run a good 10 dB below this level at 28 mV input.

Noise rejection is more than adequate to suppress line noise due to fluorescent lamps and normal line transients. Appliance motors on the same side of the 110–220V line may produce some noise. Even SCR dimmers produce only a background of impulse noise depending upon the relative location of receiver and SCR. Otherwise, performance is noise-free anywhere in the home. Satisfactory operation was observed in a factory building so long as transmitter and receiver were connected to the same phase of the three-phase service line.

APPLICATIONS

Additional applications other than home music systems are possible. Intercoms are one possibility, with a separate transmitter and receiver located at each station. A microphone can serve as the source material and the system can act as a monitor for a nursery room. Background music may be added to existing buildings without the expense of running new wiring.

1.3V IC Flasher, Oscillator, Trigger or Alarm

National Semiconductor
Application Note 154

INTRODUCTION

Most linear integrated circuits are designed to operate with power supplies of 4.5 to 40V. Practically no battery/portable equipment is provided with indicator lights due to unacceptable power drain. Even LEDs (solid state lamps) won't light from a 1.5V battery, and drain the common 9V radio battery in a few hours.

The LM3909 changes all this. Obtaining long life from a single 1.5V cell, it opens a whole new area of applications for linear integrated circuits. Sufficient voltage for flashing a light emitting diode is generated with cell voltage down to 1.1V. In such low duty cycle applications batteries will last for months to years of continuous operation. Such flasher circuits then become practical for marking location of flashlights, emergency equipment, and boat mooring floats in the dark.

The LM3909 is simple in design, easy to use, and includes extra resistors to minimize external circuitry and the size of the completed flasher or oscillator.

CIRCUIT OPERATION

The circuit below in *Figure A* is the LM3909 connected as the simplest type of oscillator. Ignoring the capacitor for a moment, and assuming 1.5V on pin 5, current will flow in the 3k and 6k timing resistors through the emitter of Q_1. This current will be amplified by about 3 by Q_2 and passed to the base of Q_3. Q_3 will then conduct, pulling down on the base of Q_4 and hence the base of Q_1. This is a negative feedback since it will reduce timing resistor current and current to the power transistor's base until a balance is reached. This will occur with the collector of Q_3 at about 0.5V, the base of Q_4 at about 1V, and a very small voltage from pin 8 to ground. The difference between these two voltages is the base-emitter drop of Q_1 and 2/3 the base-emitter drop of Q_4 as set by the high resistance divider from its base to emitter.

Note that negative feedback *voltage* is attenuated by at least 2 due to the divider of two 400Ω resistors. Now considering the capacitor, its positive feedback is initially unity. Therefore the DC bias condition and the temporary excess positive feedback conditions are met and the circuit must oscillate.

The waveform at pin 8 of the above oscillator is shown below. The waveform at pin 2, the power transistor collector, is almost a rectangle. It extends from a saturation voltage of 0.1V or less to within about 0.1V of the supply voltage. The "on" period of course coincides with the negative pulses at pin 8. Other circuit voltages can easily be inferred from the two waveforms in *Figure B*.

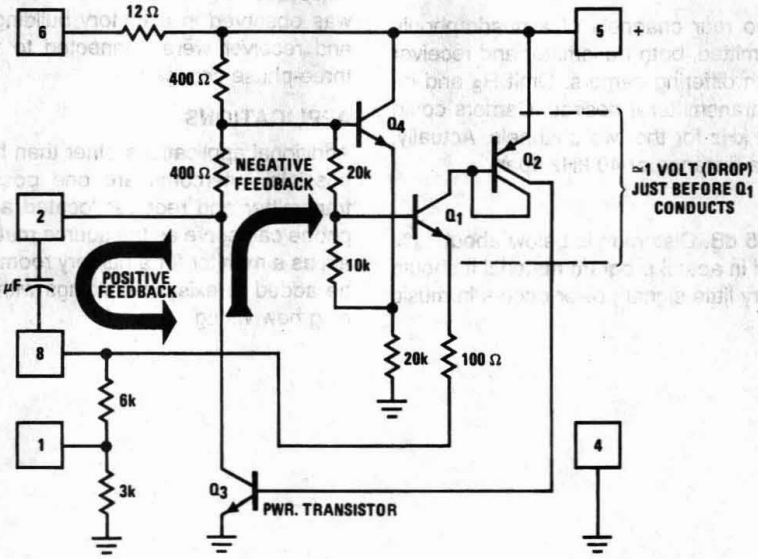

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FIGURE A

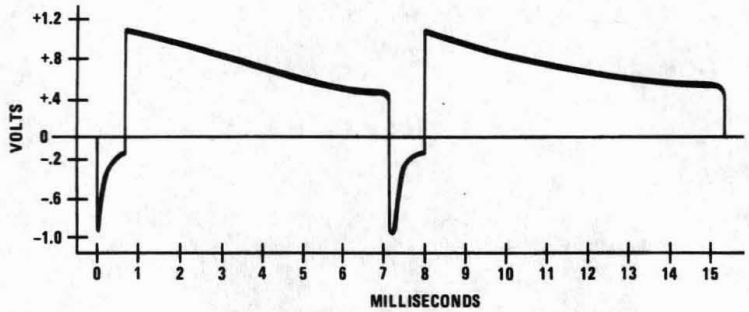

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FIGURE B

The simplicity of LED and incandescent pilot lamp flashers is illustrated below in *Figure 1.* In the LED flasher, the LM3909 uses the single capacitor for both timing and voltage boosting.

The LM3909, although designed as a LED flasher, is ideal for other applications such as high current, trigger pulse for SCRs and "Triacs." The frequency of oscillation adjusts from under 1 Hz to hundreds of kHz. Waveshape can be set from pulses a few μs wide to approximately a square wave. Thus the LM3909 can perform as a sound effects generator, an audible alarm, or audible continuity checker. Finally it can be a radio (detector/amplifier), low power one-way intercom, two-way telegraph set, or part of a "mini-strobe" light flashing up to 7 times per second.

Operating with only a 1.5V battery as a supply gives the LM3909 several rather unique characteristics. First, *no* known connection can cause immediate destruction of the IC. Its internal feedback loop insures self-starting of properly loaded oscillator circuits. Experimenters can safely explore the possibilities of the LM3909 as an AC amplifier, one-shot, latch circuit, resistance limit detector, multi-tone oscillator, heat detector, or high frequency oscillator.

With the accent on the practical, a brief circuit description will be given followed by circuits in the following application areas:

Flasher & Indicator Applications

Audio & Oscillator Applications

Trigger & Other Applications

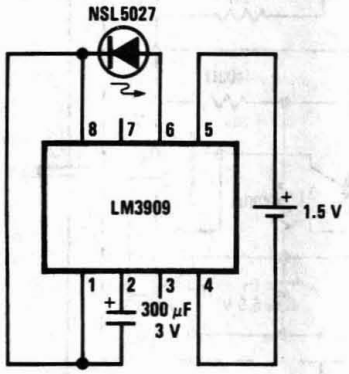
For those who want to modify or design their own circuits using the LM3909, application hints will be covered near the end of this note.

CIRCUIT DESCRIPTION

The circuit of *Figure 2* again shows the typical 1.5V LED flasher, but with the internal circuitry of the IC illustrated.

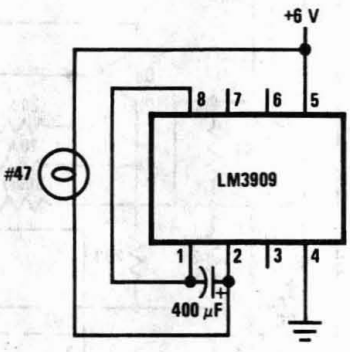
The flasher achieves minimum power usage in two ways. Operated as above, the LED receives current only about 1% of the time. The rest of the time, all transistors but Q_4 are off. The 20k resistor from Q_4's emitter to supply-common draws only about 50 μA. The 300 μF capacitor is charged through the two 400Ω resistors connected to pin 5 and through the 3k resistor connected to pin 1 of the circuit.

1.5V Flasher



Note: Nominal Flash Rate: 1 Hz.

Incandescent Bulb Flasher



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Note: Flash Rate: 1.5 Hz.

FIGURE 1. Two Simple Flashers

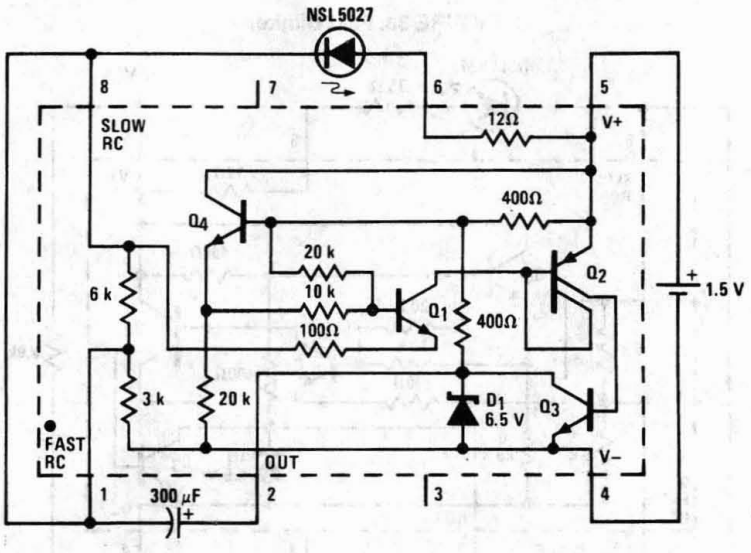

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FIGURE 2. Circuit Operation

Transistors Q_1 through Q_3 remain off until the capacitor becomes charged to about 1V. This voltage is determined by the junction drop of Q_4, its base-emitter voltage divider, and the junction drop of Q_1. When voltage at pin 1 becomes a volt more negative than that at pin 5 (supply positive terminal) Q_1 begins to conduct. This then turns on Q_2 and Q_3.

The LM3909 then supplies a pulse of high current to the LED. Current amplification of Q_2 and Q_3 is between 200 and 1000. Q_3 can handle over 100 mA and rapidly pulls pin 2 close to supply common (pin 4). Since the capacitor is charged, its other terminal at pin 1 goes *below* the supply common. The voltage at the LED is then higher than battery voltage, and the 12Ω resistor between pins 5 and 6 limits the LED current.

Many of the other oscillator circuits work in a similar fashion. If voltage boost is not needed (with or without current limiting) loads can be hooked between pins 2 and 6 or pins 2 and 5.

APPLICATIONS: FLASHER & INDICATOR

Differing uses and supply voltages will require adjustment of flashing rates. Often it is convenient to leave the capacitor the same value to minimize its size, or to fix the pulse energy to the LED. First, the internal RC resistors can be used to obtain 3k, 6k, or 9k by hooking to or shorting the appropriate pins. Further adjustment methods are shown in the two parts of *Figure 3* below.

In *Figure 3a*, it can be seen that the internal RC resistors are shunted by an external 1k between pins 8 and 4. This will give a little over 3 times the flashing rate of the typical 1.5V flasher of *Figure 1*.

The 3.9k resistor in *Figure 3b* connected from pin 1 to the 6V supply raises voltage at the bottom of the 6k RC resistor. Charging current through that resistor is greatly reduced, bringing flashing rate down to about that of the 1.5V circuit (1 Hz). As will be explained later, this biasing method also insures starting of oscillation even under unfavorable conditions.

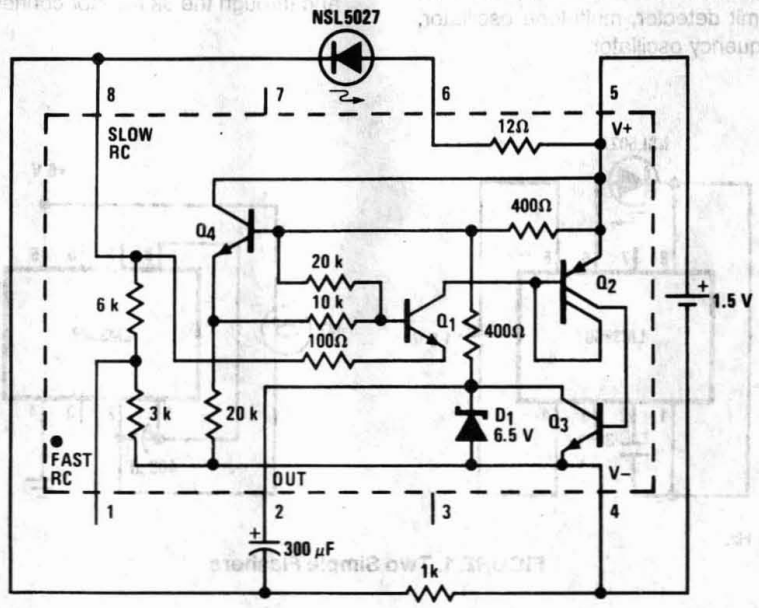

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FIGURE 3a. Fast Blinker

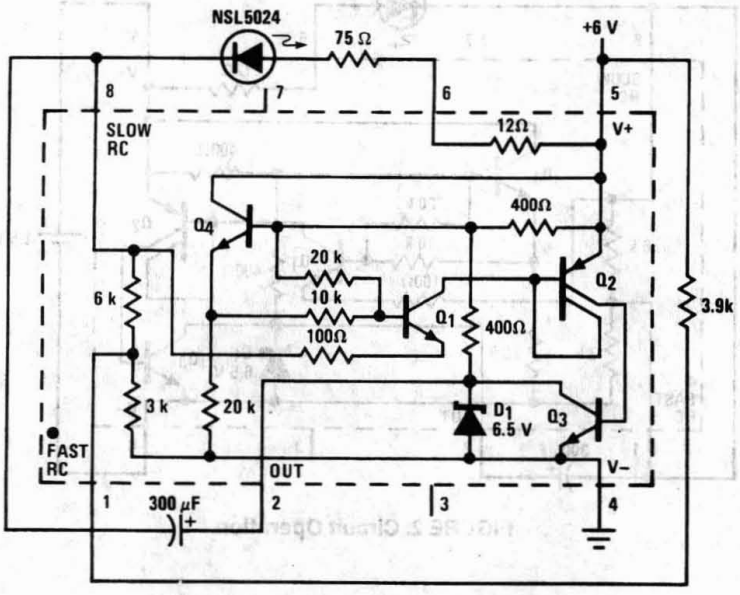

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FIGURE 3b. 6 Volt Flasher

Two precautions are taken for circuit reliability. The added 75Ω series resistor for the LED keeps current peaks within safe limits for the diode and IC. Also, in operation above a 3V supply, the electrolytic capacitor sees momentary voltage reversals. It should be rated for periodic reversals of 1.5V.

A continuously appearing indicator light can also be powered from a single 1.5V cell as shown in *Figure 4.* Duty cycle and frequency of the current pulses to the LED are increased until the average energy supplied provides sufficient light. At frequencies above 2 kHz, even the fastest movement of the light source or the observer's head will not produce significant flicker.

Since this indicator powering circuit uses the smallest capacitor that will reliably provide full output voltage, its operating frequency is well above the 2 kHz point. The indicator is not, however, intended as a long life system, since battery drain is about 12 mA.

High frequency operation requires addition of *two* external resistors, typically of the same value. One, of course, shunts the high internal timing resistors. If only this one were used, the capacitor charging current would have to pass through the two 400Ω resistors internally connected between pin 5 and the collector of Q3. Oscillation at a slower rate and lower duty cycle than desired would occur, and oscillation might cease altogether before the battery was fully discharged. The second 68Ω resistor shunting the two 400Ω resistors eliminates these problems.

The circuit in *Figure 5* is a relaxation type oscillator flashing 2 LEDs sequentially. With a 12 VDC supply, repetition rate is 2.5 Hz. C_2, the timing and storage capacitor, alternately charges through the upper LED and is discharged through the other by the IC's power transistor, Q_3.

If a red/green flasher is desired, the green LED should have its anode or plus lead toward pin 5 (like the lower LED). A shorter but higher voltage pulse is available in this position.

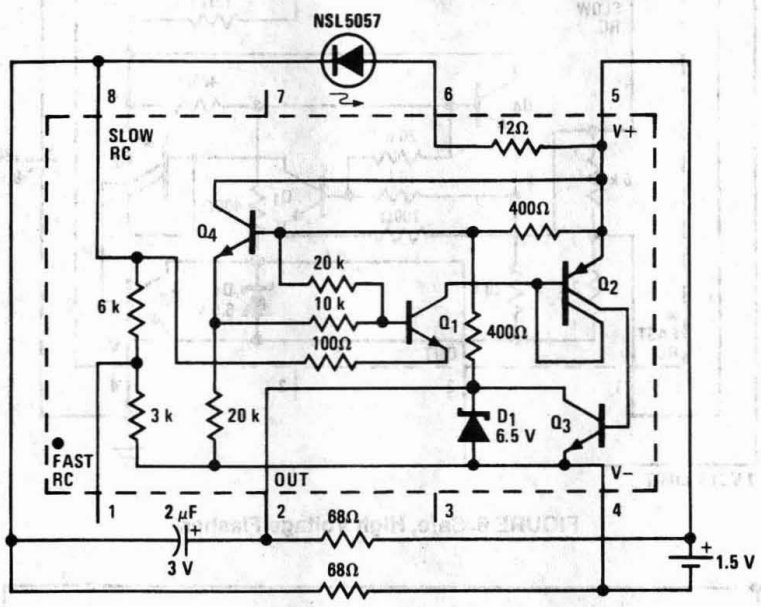

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FIGURE 4. "Continuous" 1.5V Indicator

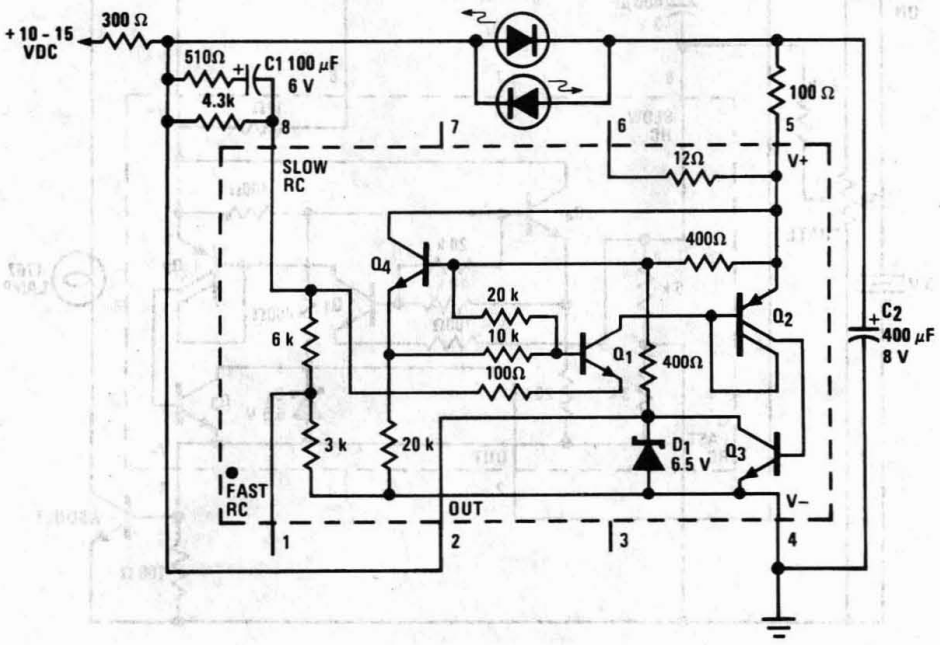

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FIGURE 5. Alternating Flasher

Indication or monitoring of a high voltage power supply at a remote location can be done much more safely than with neon lamps. If the dropping resistor (43k as in *Figure 6*) is located at the source end, all other voltages on the line, the IC, and the LED will be limited to less than 7V, above ground.

The timing capacitor is charged through the dropping resistor and the two 400Ω collector loads between pins 2 and 5 of the IC. When capacitor voltage reaches about 5V, there is enough voltage across the 1k resistor (to pin 8) to turn on Q_1, and hence trigger on the whole IC to discharge the capacitor through the LED.

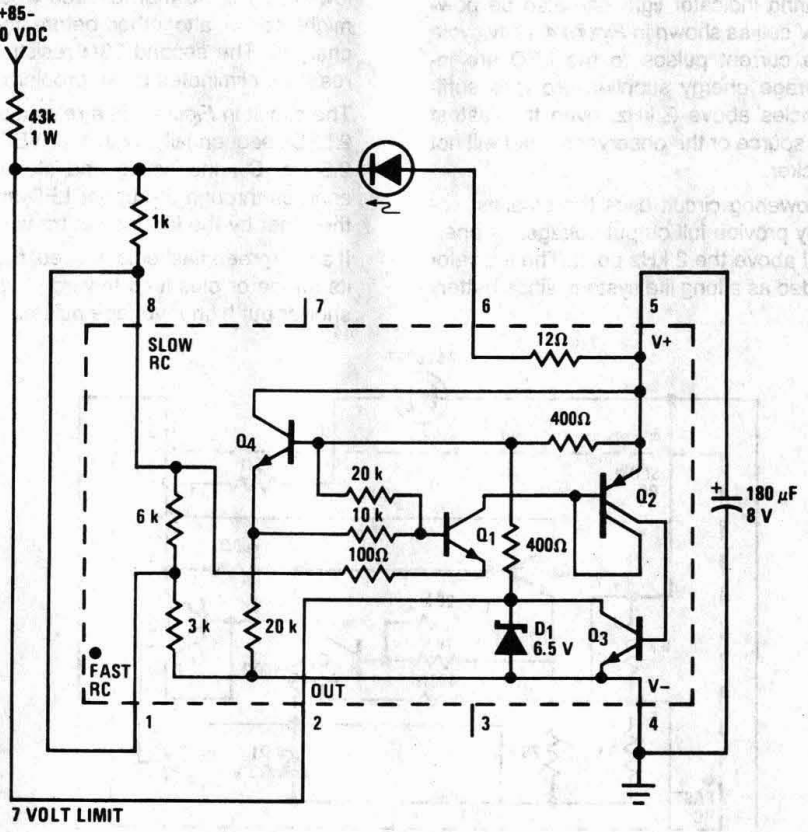

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FIGURE 6. Safe, High Voltage Flasher

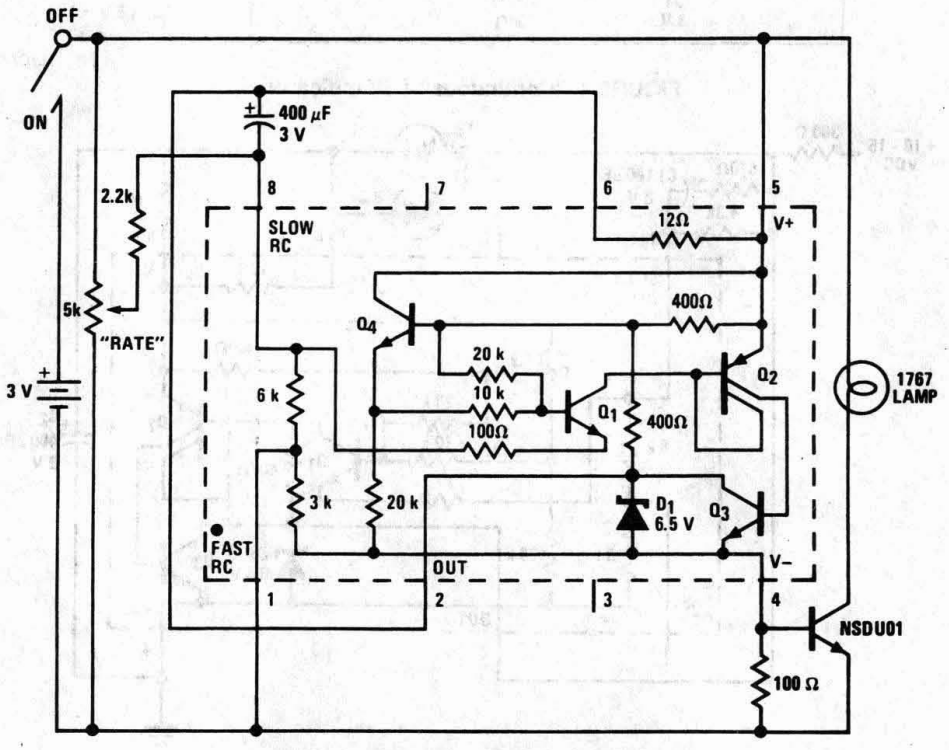

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FIGURE 7. "Mini-Strobe" Variable Flasher

There are many other LED applications and variations of circuits. A chart outlining operation of the circuit of *Figure 6* at various voltages appears on the LM3909 data sheet. Also shown are circuits for adjusting the flash rate, flashing 4 LEDs in parallel, and details for building a blinking locator light into an ordinary flashlight.

Incandescent bulbs can also be flashed, as already illustrated in *Figure 1.* However, most such bulbs draw more than the 150 mA that the LM3909 can switch. The two following circuits therefore use an added power transistor rated at 1A or more. In each circuit, an NPN transistor is used, so the power transistor's base drive is obtained from the common or ground pin of the flasher IC.

The 3V "mini-strobe" of *Figure 7* may be used as a variable rate warning light or for advertising or special effects. The rate control is so wide range that it adjusts from no flashes at all to continuously on. Chosen for rapid response, the miniature 1767 lamp can be flashed several times a second.

A "mini-strobe" circuit was tested in a Lantern Flashlight with a large reflector. In a dark room, the flashes were almost fast enough to stop a person's motion. As a toy, the fast setting can mimic the strobes at rock concerts or the flicker of old-time movies.

Figure 8 below shows a higher power application such as would use an automotive storage battery for power. It provides about a 1 Hz flash rate and powers a lamp drawing a nominal 600 mA.

A particular advantage of this circuit is that it has only 2 external wires and thus may be hooked up in either of the two ways shown below in *Figure 9.* Further, no circuit failure can cause a battery drain greater than that of the bulb itself, continuously lit.

In the circuit of *Figure 8*, the 3300 μF capacitor performs a number of other functions. It makes the LM3909 immune to supply spikes, and provides the means of limiting the IC's supply voltage. Since the LM3909 can only operate with

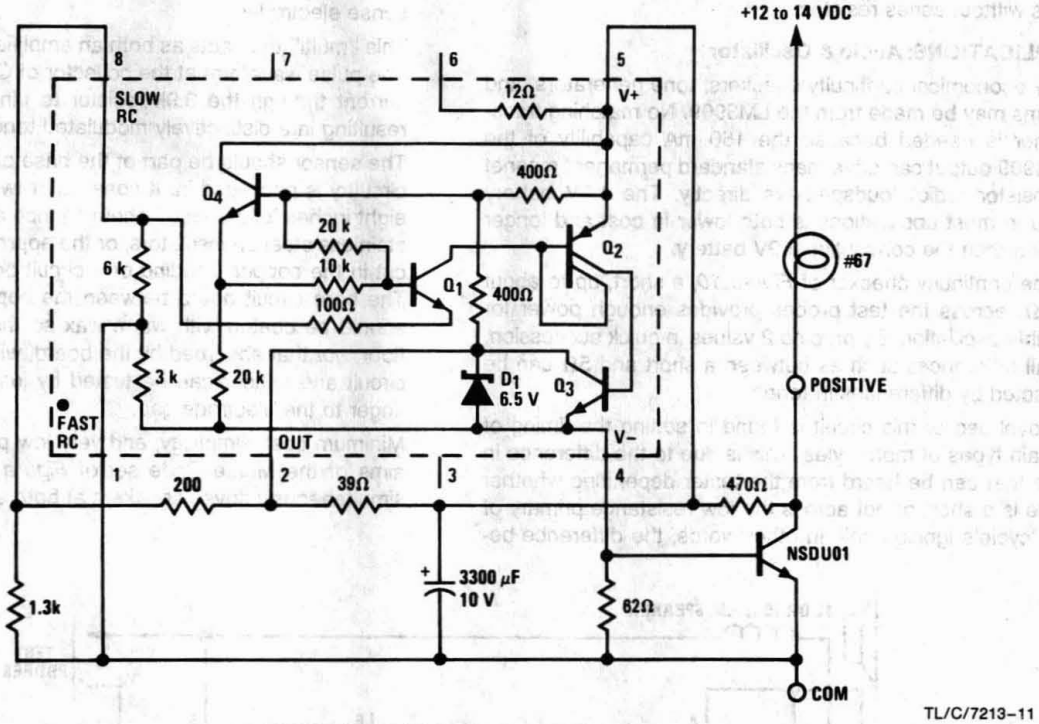

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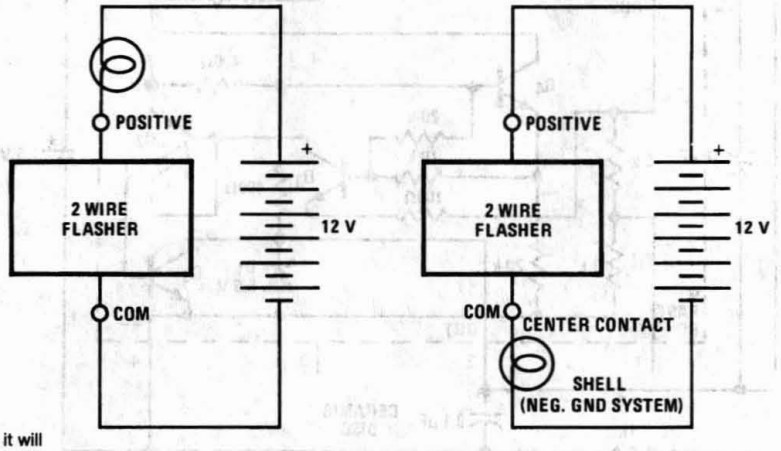
FIGURE 8. 12 Volt Flasher (2 Wire)



TL/C/7213–12

Note: If flasher case insulated, it will operate in positive or negative ground systems.

FIGURE 9. 2 Wire Flasher Usage

7.5V or less on pin 5 (in this circuit) the 200Ω/1.3k divider attached to pin 8 of the IC causes it to turn fully on at 7V or less on pin 5. Then the LM3909 discharges the timing capacitor (its own supply voltage) to 4V or less, whereupon it turns off. The capacitor discharge current comes out of pin 4 of the IC, turning on the NSD U01 transistor. It is the large size of the timing capacitor that allows it to *store* all the needed energy for turning on the power transistor. This in turn permits the whole flasher circuit to operate as a 2 wire device.

Many other flasher possibilities exist. LED flash rate can be varied from 0 to 20 Hz, or a number of LEDs may be flashed in parallel. With a 3V supply, yellow and green LEDs may be flashed. A 6V incandescent "emergency lantern" can be made and its PR-13 bulb may be made to give continuous light or flash by switch selection. This is a more reliable, longer lived system than a lantern with a second thermal flasher bulb. The NSL4944 Current Regulated LED makes possible flashing many LEDs in parallel or with high voltages without series resistors.

APPLICATIONS: Audio & Oscillator

Very economical continuity checkers, tone generators, and alarms may be made from the LM3909. No matching transformer is needed because the 150 mA capability of the LM3909 output can drive many standard permanent magnet (transistor radio) loudspeakers directly. The 1.5V battery used in most applications is both lower in cost and longer lasting than the conventional 9V battery.

In the continuity checker of *Figure 10*, a short, up to about 100Ω, across the test probes provides enough power for audible oscillation. By probing 2 values in quick succession, small differences such as between a short and 5Ω can be detected by differences in tone.

A novel use of this circuit is found in setting the timing of certain types of motorcyles. This is due to the difference in tone that can be heard from the tester depending whether there is a short or not across the low resistance primary of the 'cycle's ignition coil. In other words, the difference between a 1Ω resistor and a 1Ω inductor can be heard. Quick checks for shorts and opens in transformers and motors can therefore be made.

Darkrooms, laundry rooms, laboratories, and cellar workshops can often suffer damage from spills or water seepage ruining lumber, chemicals, fertilizer, bags of dry concrete, etc. The circuit of *Figure 11* is safe on potentially damp floors since there is no connection to the power line. Further, its standby battery drain of 100 μA yields a battery life close to (or, according to some experiments, exceeding) shelf life.

Without moisture, multivibrator transistor Q_a is completely off, and its collector load (6.2k) provides enough current to hold pin 8 of the LM3909 above 0.75V where it cannot oscillate. When the sense electrodes pass about 0.25 μA, due to moisture, Q_a starts turning on, and since Q_b is already partially biased on, positive feedback now occurs. Q_a and Q_b are now an astable multivibrator which starts at about 1 Hz and oscillates faster as more leakage passes across the sense electrodes.

This "multi" then acts as both an amplifier and a modulator. The pulse waveform at the collector of Q_a varies the timing current through the 3.9k resistor to pin 8 of the LM3909 resulting in a distinctively modulated tone output.

The sensor should be part of the base of the box the alarm circuitry is packaged in. It consists of two electrodes six or eight inches long spaced about ⅛ inch apart. Two strips of stainless steel on insulators, or the appropriate zig-zag path cut in the copper cladding of a circuit board will work well. The bare circuit board between the copper sensing areas should be coated with warm wax so that moisture on the floor, *not* that absorbed by the board, will be detected. The circuit and sensor can be tested by just touching a damp finger to the electrode gap.

Minimum cost, simplicity, and very low power drain are the aims of the Morse Code set of *Figure 12.* One oscillator simultaneously drives speakers at both sending and receiv-

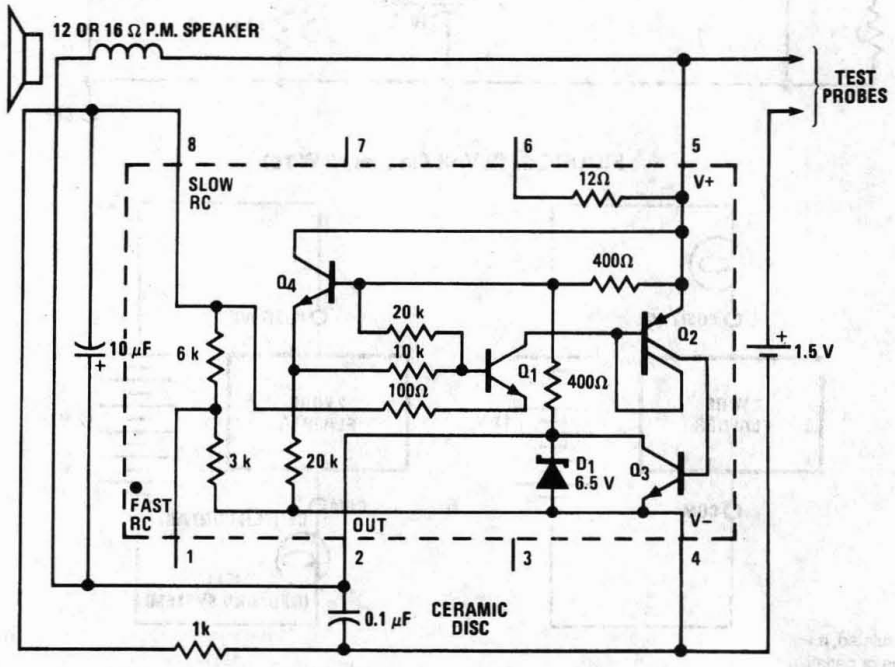


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FIGURE 10. "Buzz Box" Continuity and Coil Checker

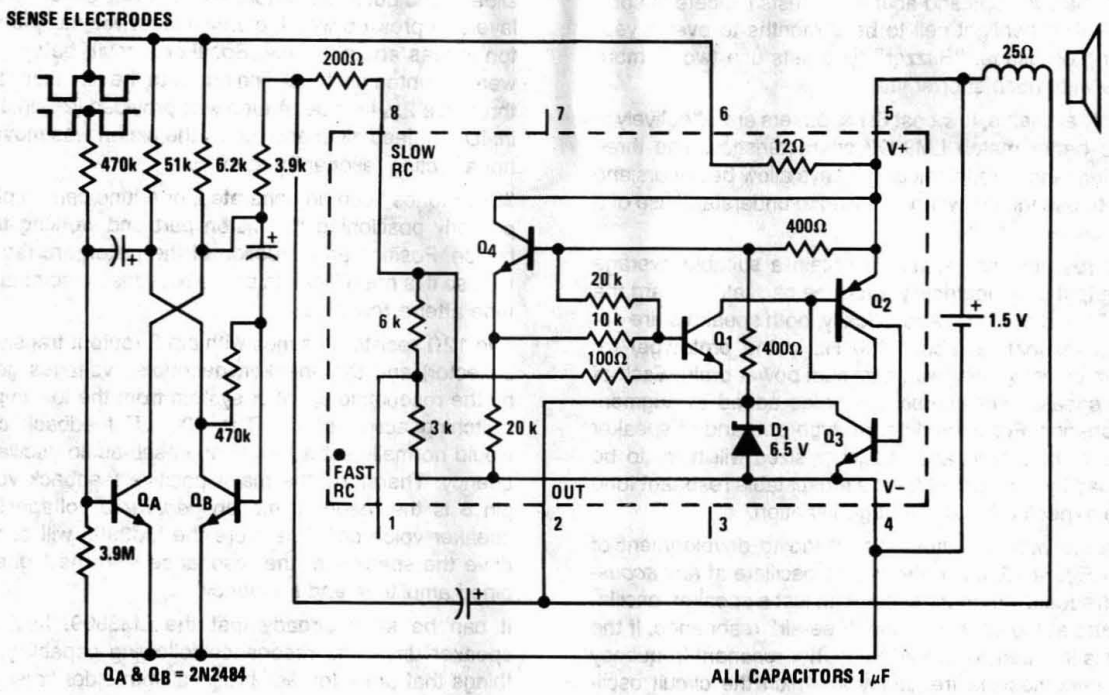

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FIGURE 11. Water Seepage Alarm

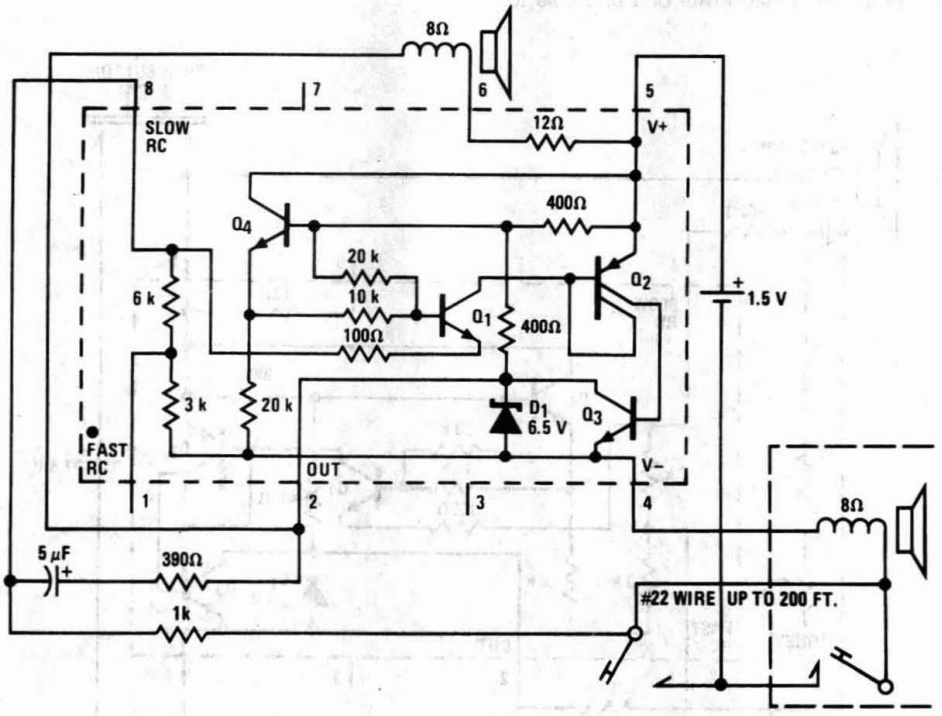

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FIGURE 12. Morse Code Set

ing ends. Calculations and actual use tests indicate life of a single alkaline penlight cell to be 3 months to over a year depending on usage. "Buzzer" type sets use two or more batteries with much shorter life.

Commonly available, low cost 8Ω speakers are effectively in series to better match LM3909 characteristics. The three wire system and parallel telegraph keys allow beginners and children to use the set without having to understand use of a "send-receive" switch.

The two resistors are added to obtain a suitable average power output and electrically force the oscillator toward the desired 50% duty cycle. Acoustically, both speakers are operated at resonance (about 400 Hz in the prototype) for maximum pleasing tone with minimum power drain. Each of the two speaker enclosures has holes added to augment this resonance. For each different type or brand of speaker and size of box, hole and capacitor sizes will have to be determined by experiment for the most stable resonant tone over the expected battery voltage variation.

Experiments with the above circuit led to development of circuit in *Figure 13*. It is optimized to oscillate at any *acoustic* load frequency of resonance! With just a speaker, oscillation occurs at the speaker cone "free-air" resonance. If the speaker is in an enclosure with a higher resonant frequency . . . this becomes the frequency at which the circuit oscillates.

An educational audio demonstration device, or simply an enjoyable toy, has been fabricated as follows. A roughly cubical box of about 64 in.^{3} was made with one end able to slide in and out like a piston. The box was stiffened with thin layers of pressed wood, etc. Minimum volume with the piston in was about 10 in.^{3}. Speaker, circuit, battery, and all were mounted on the sliding end with the speaker facing out through a 2¼ in. hole. A tube was provided (2½ in. long, 5/16 in. ID) to bleed air in and out as the piston was moved while not affecting resonant frequency.

"Slide tones" can be generated, or a tune can be played by properly positioning the piston part and working the push button. Position and direction of the piston are rather intuitive, so it is not difficult to play a reasonable semblance of a tune after a few tries.

The 12Ω resistor in series with pin 2 (output transistor Q_3's collector) and the speaker, decouples voltages generated by the resonating speaker system from the low impedance switching action of Q_3. The 100 μF feedback capacitor would normally set a low or even sub-audio oscillation frequency. Therefore, the major positive feedback voltage to pin 8 is the resonant motion *generated* voltage from the speaker voice coil. Therefore the LM3909 will continue to drive the speaker at the resonance with the highest combined amplitude and frequency.

It can be seen already that the LM3909, having direct speaker drive and resonance following capability, can do things that are a lot less practical with older timer and unijunction circuitry. Two final "sound effect" type of circuits are illustrated in *Figure 14*.

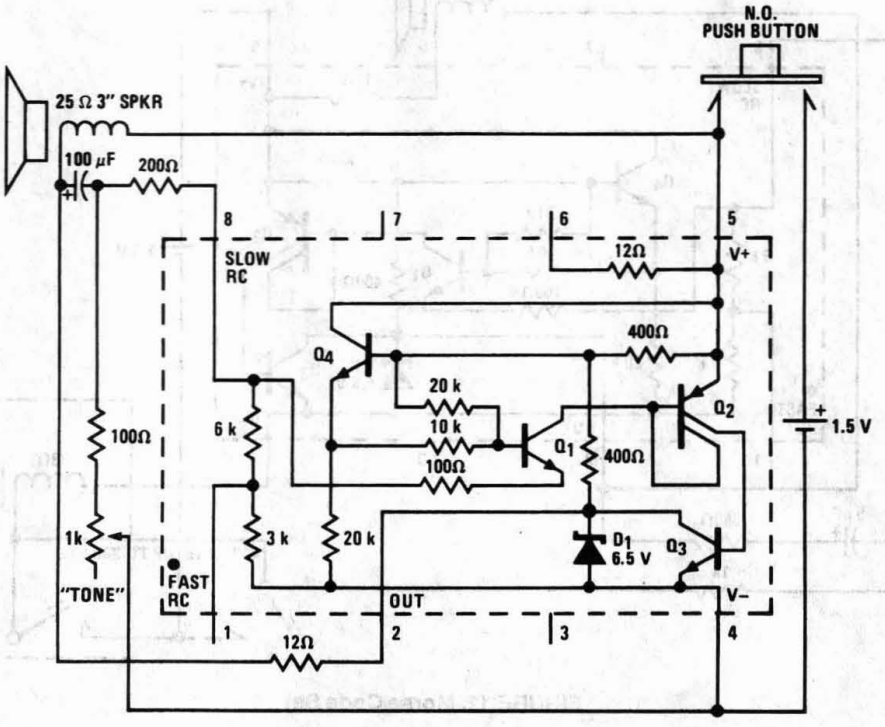

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FIGURE 13. Electronic "Trombone"

The siren of *Figure 14a* produces a rapidly rising wail upon pressing the button, and a slower "coasting down" upon release. If it is desirable to have the tone stop sometime after the button is released, an 18k resistor may be placed between pins 8 and 6 of the IC. The sound is then much like that of a motor driven siren.

In this circuit, the oscillation must not be influenced by acoustic resonances. The 1 μF capacitor and 200Ω resistor determine a pulse to the speaker that is wider than that for flashing LEDs, but much narrower than is used in the tuned systems of *Figures 12* and *13*. The repetition rate of speaker pulses is determined by the 2.7k resistor, and the charge on the 500 μF capacitor. Discharging this capacitor with the pushbutton increases current in the 2.7k resistor causing a rapid upshift in tone.

The "whooper" of *Figure 14b* sounds somewhat like the electronic sirens used on city police cars, ambulances, and airport "crash wagons." The rapid modulation makes the tone seem louder for the same amount of power input.

The tone generator is the same as in the previous siren. Instead of a pushbutton, a rapidly rising and falling modulating voltage is generated by a second LM3909 and its associated 400 μF capacitor. The 2N1304 transistor is used as a low voltage (germanium) diode. This transistor along with the large feedback resistor (5.1k to pin 8) forces the ramp generator LM3909 into an unusual mode of operation hav-

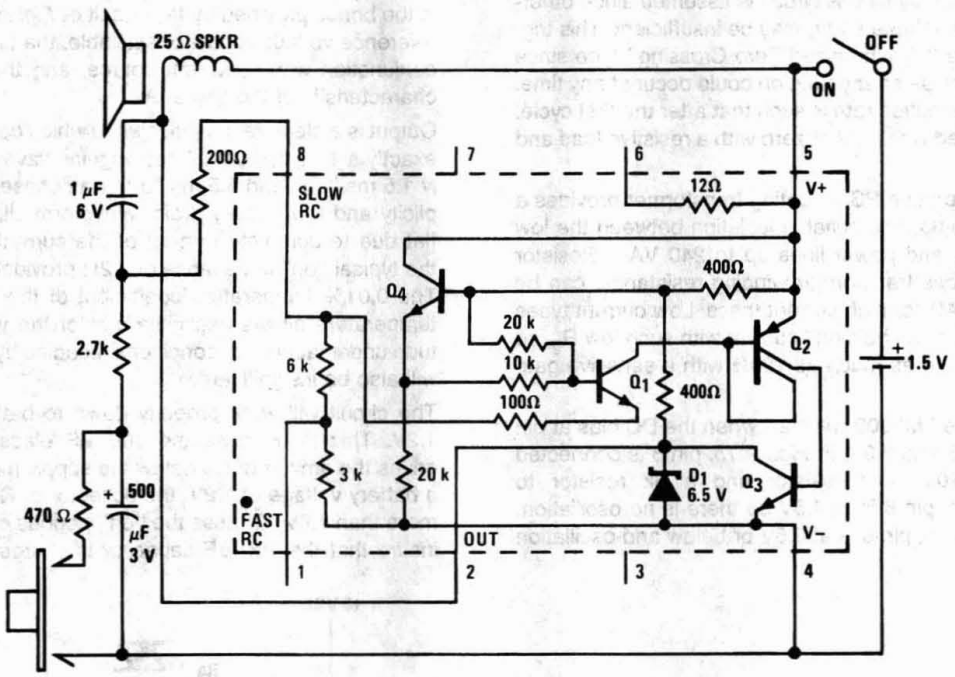

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FIGURE 14a. Fire Siren

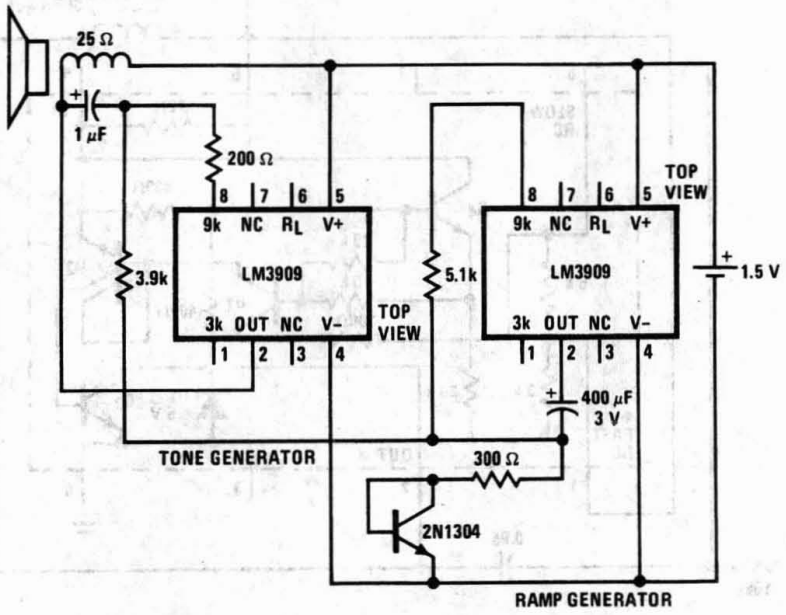

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FIGURE 14b. Whooper Siren

ing longer "on" periods than "off" periods. This raises the average tone of the tone generator and makes the modulations seem more even.

APPLICATIONS: Trigger & Other

With its high pulse current capability, the LM3909 is a good pulse-transformer driver. Further, it uses fewer parts and operates more successfully from low voltage supplies than do the equivalent unijunction circuits. The "Triac" trigger of *Figure 15* operates from a 5V logic supply and provides gate trigger pulses of up to 200 mA.

With no gate input, or a TTL logic high input, the LM3909 is biased off since pin 1 is tied to V+. With a logic low at the gate in, the IC provides 10 μs pulses at about a 7 kC rate. A TTL gate loaded only by this circuit is assumed since otherwise worst-case voltage swing may be insufficient. This trigger is not of the "Synchronized Zero Crossing" type since the first trigger pulse after gating on could occur at any time. However, the repetition rate is such that after the first cycle, a triac is triggered within 8V of zero with a resistive load and a 115 VAC line.

The standard Sprague PC mounting transformer provides a 2:1 current step-up, and suitable isolation between the low voltage circuitry and power lines up to 240 VAC. Resistor R_g, which includes transformer winding resistance, can be as little as 3 or 4Ω for high current triacs. Low current types may need excessive "holding" current with such low R_g, so it may be raised to as much as 100Ω with a sensitive gate triac.

Oscillation of the LM3909 will start when the DC bias at pin 8 is between 1.6 and 3.9V. In *Figure 15,* pin 8 is connected between the 10k input resistor and a 6k resistor to 5V. With 3.8V in, pin 8 is at 4.5V so there is no oscillation. With 1V, or less, in, pin 8 is at 3.5V or below and oscillation occurs. From this example, it can be seen that other input resistors or bias dividers can be calculated to gate the LM3909 triac trigger from other logic levels.

A useful electronic lab device is a precision square wave generator/calibrator. If the output is held at a few tenths percent of 1V, peak-to-peak, it is useful in calibrating oscilloscopes and adjusting 'scope probes. Many lower cost or battery-portable oscilloscopes do not have this feature built in. Also it is useful in checking gain and transient response of various amplifiers including "hi-fi" power amplifiers.

Battery powered equipment is free from both the inconvenience of a line cord, and from some of the noise and hum effects of equipment attached to the power line. Operation for over five hundred hours from a single flashlight "D" cell is the bonus provided by the circuit of *Figure 16.* The lowest reference voltage regulator available, the LM113, is used in conjunction with a current source, and the voltage boost characteristic of the LM3909.

Output is a clean rectangular wave which can be adjusted to exactly a 1V amplitude. A rectangular wave of approximately 1.5 ms "on" and 5.5 ms "off" was chosen for circuit simplicity and low battery drain. Waveform clipping is virtually flat due to complete turn-off of the current switch Q_2 and the typical "on" impedance of 0.2Ω provided by the LM113. The 0.01% temperature coefficient of the LM113 at room temperature allows negligible drift of the waveform amplitude under laboratory conditions. Loading by a 'scope probe will also be insignificant.

The circuit will work properly down to battery voltages of 1.2V. This is because the 100 μF electrolytic capacitor drives the emitter of Q_2 below the supply minus terminal. At a battery voltage of 1.2V, the collector of Q_2 can still swing more than 1.6V. Q_1 uses the "off" periods of the LM3909 to insure that the 100 μF capacitor is charged to almost the

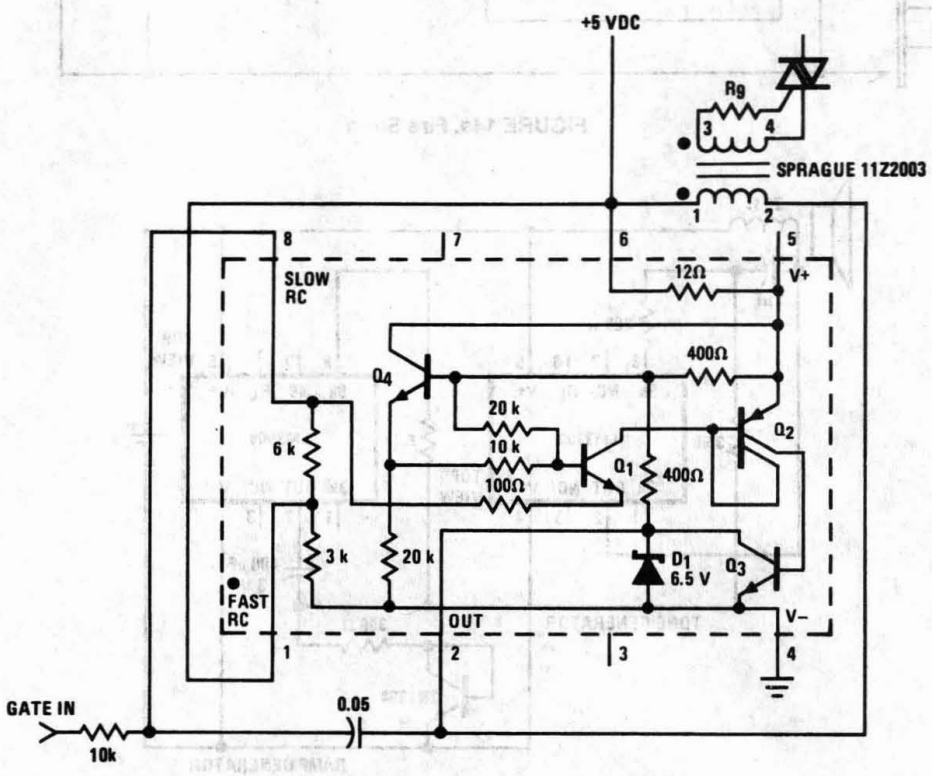

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FIGURE 15. Triac Trigger

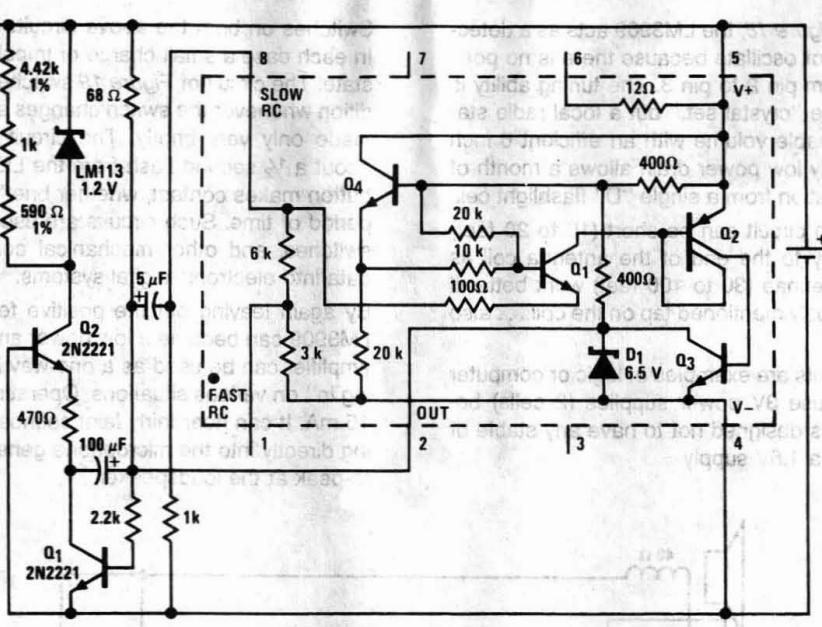

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FIGURE 16. 'Scope Calibrator

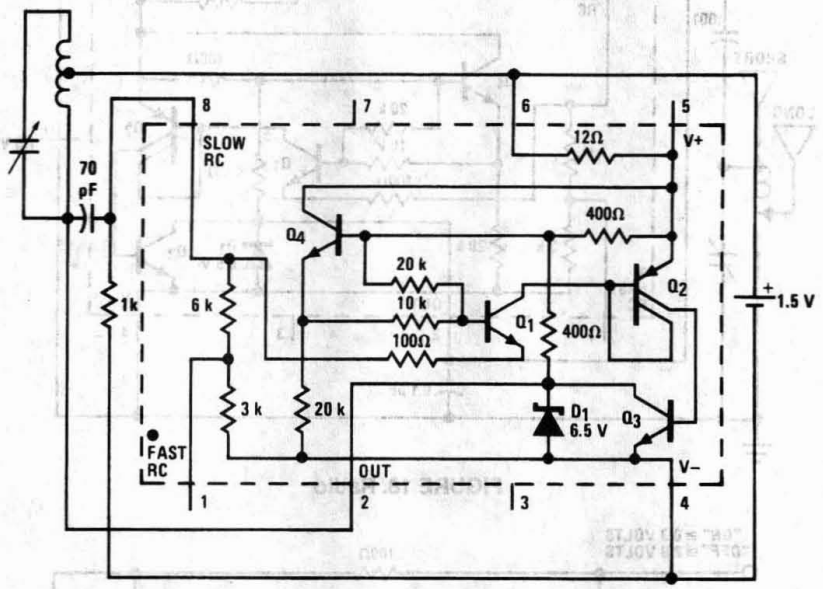

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FIGURE 17. R.F. Oscillator

entire battery voltage. Thus when the LM3909 turns on and pin 2 drives almost to the minus supply voltage, the negative side of the capacitor is driven 0.9 to 1.2V below this terminal. Low battery voltage cannot lead to an undetected error in the 1V squarewave. This is because the waveform becomes distorted rather than just decreasing in amplitude as battery voltage becomes too low.

Taking advantage of the versatility and the indestructability of the LM3909 by a 1.5V battery, the IC can become an ideal teaching means, or experimental device for the young electronic hobbyist. As well as the circuits already presented, the LM3909 can be made to work as amplifier, radio, and even logic type circuits. The ideas of negative and positive feedback can be presented. The circuits presented in *Figures 17* through *21* are intended as illustrations or demonstrations of circuitry concepts such as would be used in an experimenter's kit. They are not meant to be used as parts of finished commercial products with specific performance specifications. In other words, working circuits have been breadboarded, but no measurements of performance such as frequency range and distortion have been attempted.

Both tuned circuits of *Figures 17* and *18* use standard AM radio ferrite antenna coils (loopsticks) with a tap 40% of the turns up from one end. The oscillator works up to 800 kHz or so, and the radio tunes the regular AM broadcast band. Both also use standard (360 pF) AM radio tuning capacitors.

The oscillator has the normal capacitive positive feedback used with LM3909 circuits, but with frequency determined by the tuned circuit loading the output circuit. Detailed operating descriptions of these experimenter's circuits will not be attempted in order to keep down the length of this note. Near the end, a discussion of the IC's general theory of operation will be given, which should help in understanding the individual circuits.

In the radio circuit of *Figure 18,* the LM3909 acts as a detector amplifier. It does not oscillate because there is no positive feedback path from pin 2 to pin 8. The tuning ability is only as good as simple "crystal set," but a local radio station can provide listenable volume with an efficient 6 inch loudspeaker. Extremely low power drain allows a month of continuous radio operation from a single "D" flashlight cell.

Antennae for the radio circuit can be short (10 to 20 feet) and connected directly to the end of the antenna coil as illustrated. Longer antennae (30 to 100 feet) work better if attached to the previously mentioned tap on the coil . . . also illustrated.

The following two circuits are examples of logic or computer type functions. They use 3V power supplies (2 cells) because the LM3909 was designed not to have any stable or "latching" states with a 1.5V supply.

Switches on both the above circuits are momentary types. In each case a small charge or impulse affects the circuit's state. The circuit of *Figure 19* switches to and *holds* its condition whenever the switch changes sides, even if contact is made only very briefly. The circuit of *Figure 20* delivers about a ½ second flash from the LED every time its pushbutton makes contact, whether briefly or for a much longer period of time. Such circuits are used with keyboards, limit switches, and other mechanical contacts that must feed data into electronic digital systems.

By again leaving out the positive feedback capacitor, the LM3909 can become a low power amplifier. This little audio amplifier can be used as a one-way intercom or for "listening in" on various situations. Operating current is only 12 to 15 mA. It can hear fairly faint sounds, and someone speaking directly into the microphone generates a full 1.4V peak-to-peak at the loudspeaker.

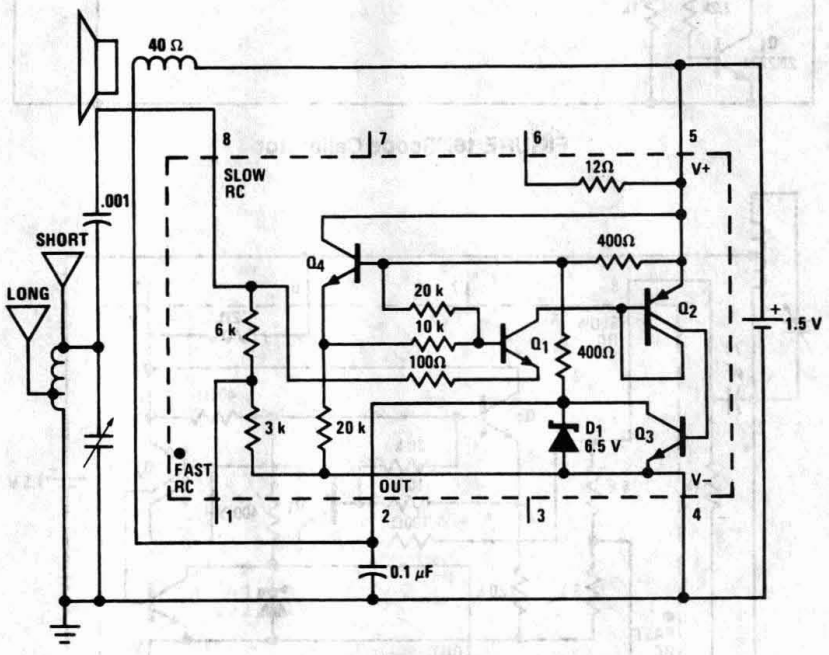

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FIGURE 18. Radio

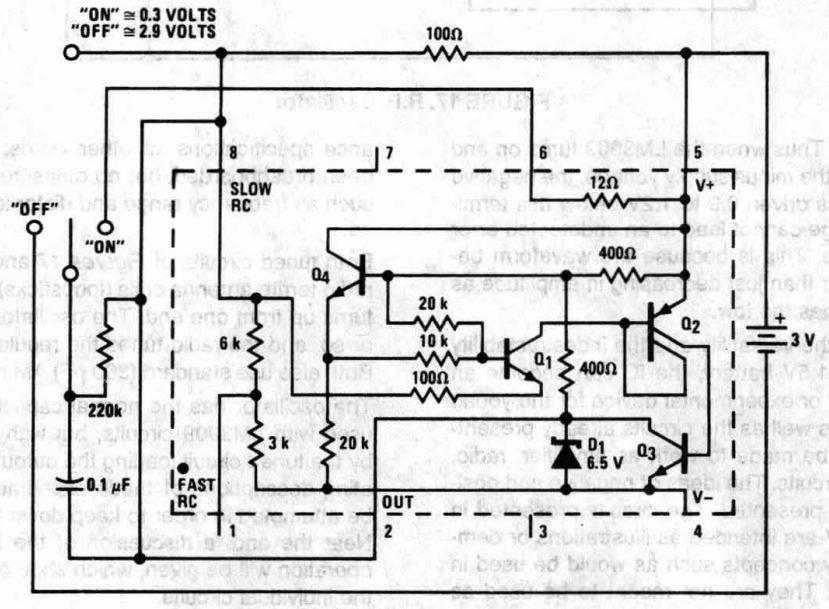

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FIGURE 19. Latch Circuit

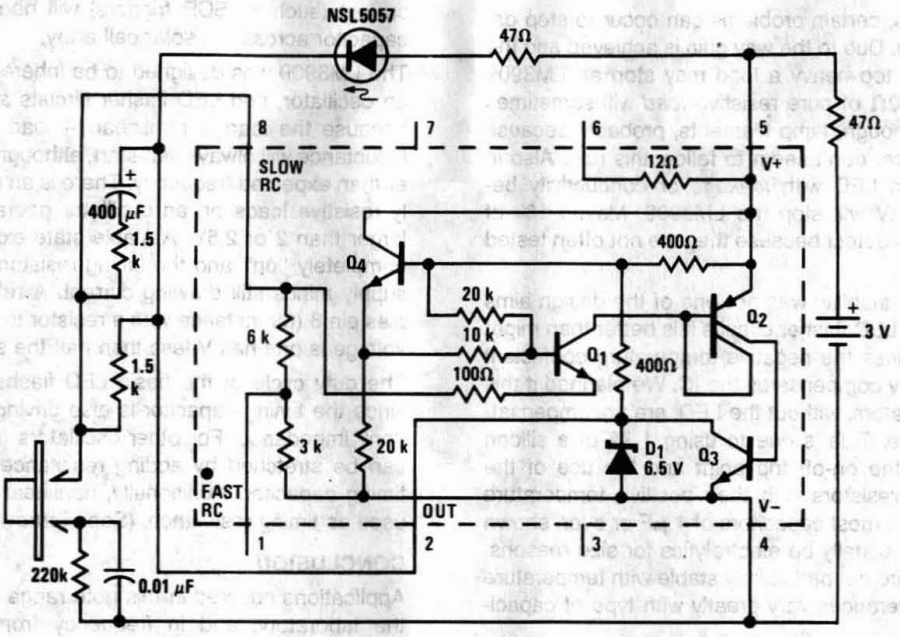

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FIGURE 20. Indicating One-Shot

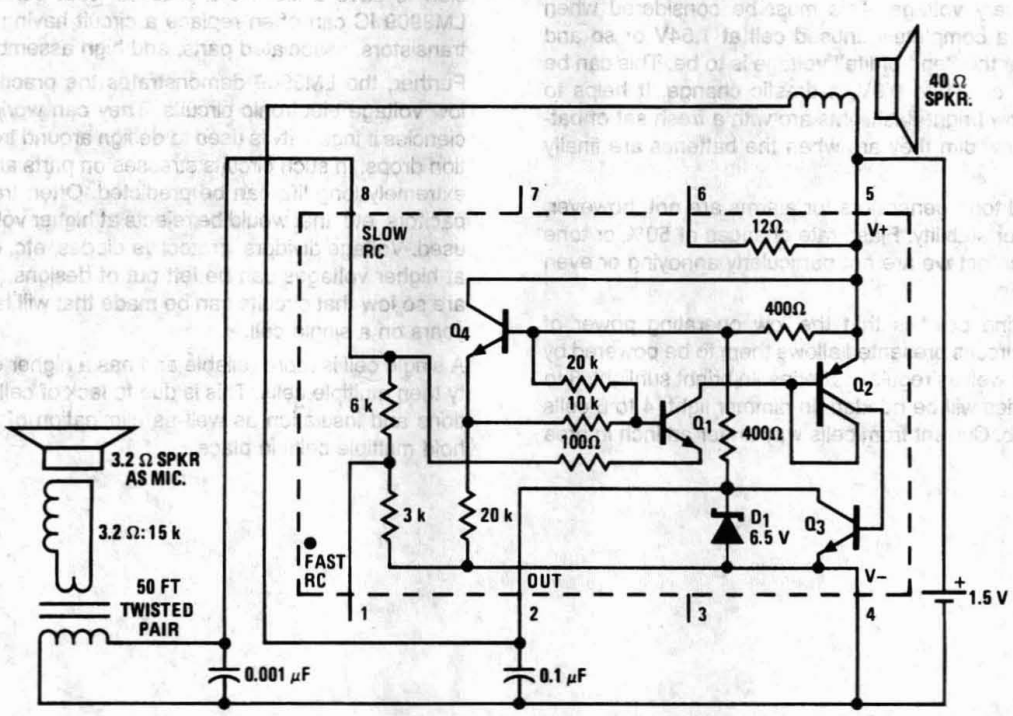

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FIGURE 21. Mini-Power Amplifier

APPLICATION HINTS

With 1.5V supplies, certain problems can occur to stop oscillation or flashing. Due to the way gain is achieved and the type of feedback, too heavy a load may stop an LM3909 from oscillating. 20Ω of pure resistive *load* will sometimes do it. Strangely enough, lamp filaments, probably because of some inductance, don't seem to follow this rule. Also in flasher circuits, an LED with *leakage* or conductivity between 0.9 and 1.2V will stop the LM3909. Maybe 1% of LEDs will have this defect because they are not often tested for it.

Greater frequency stability was not one of the design aims of the LM3909. In LED flasher circuits it is better than might be expected because the negative temperature coefficient of the LED partially compensates the IC. We planned it this way. Simple oscillators, without the LED, are uncompensated for temperature. This is due to using 1 ⅔ of a silicon junction drop as the on-off trip point and the use of the integrated timing resistors with their positive temperature coefficient. Further, most capacitors of 1 μF or over, shown in the circuits, will usually be electrolytics for size reasons. These, however, are not particularly stable with temperature and their initial tolerances vary greatly with type of capacitor.

In most of the oscillator circuits, frequency is also proportional to battery voltage. This must be considered when starting with a completely unused cell at 1.54V or so and deciding what the "end-of-life" voltage is to be. This can be in the range of 1.1 to 0.9V, a drastic change. It helps to remember how bright flashlights are with a fresh set of batteries, and how dim they are when the batteries are finally changed.

Flashers and tone generators for alarms are not, however, demanding for stability. Flash rate changes of 50% or tone shifts of ½ an octave are not particularly annoying or even too noticeable.

One interesting point is that the low operating power of most of the circuits presented allows them to be powered by *solar cells* as well as regular batteries. In bright sunlight, 3 to 4 cells in series will be needed. In dimmer light, 4 to 6 cells will do the job. Current from cells way under an inch in area generally will be sufficient, but circuits drawing a high pulse current (such as SCR triggers) will need a surge storage capacitor across the solar cell array.

The LM3909 was designed to be inherently self-starting as an oscillator, and LED flasher circuits *are*, at any voltage, because the load is nonlinear. A load with sufficient self inductance will always self-start, although possibly at a higher than expected frequency. There is an exception for largely resistive loads on an oscillator operating with a supply larger than 2 or 2.5V. A stable state exists with Q_3 turned completely "on" and the timing resistors from pin 8 to the supply minus still drawing current. A reliable solution is to bias pin 8 (for instance with a resistor to V+) so that its DC voltage is one half V less than half the supply voltage.

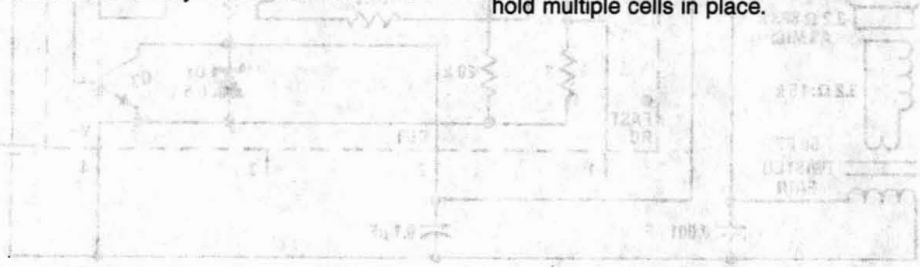
The duty cycle of the basic LED flasher is inherently low since the timing capacitor is also driving the very low LED "on" impedance. For other oscillators the "on" duty cycle can be stretched by adding resistance in series with the timing capacitor. Additionally, nonlinear resistance can be used as timing resistance. (See *Figure 14b*)

CONCLUSION

Applications covered in this note range in use from toys to the laboratory, and in frequency from DC to RF. The LM3909 can be used to amuse, teach, or even upon occasion to save a life. As a practical cost consideration the LM3909 IC can often replace a circuit having a number of transistors, associated parts, and high assembly cost.

Further, the LM3909 demonstrates the practicality of very low voltage electronic circuits. They can work at high efficiencies if ingenuity is used to design around transistor junction drops. In such circuits stresses on parts are so low that extremely long life can be predicted. Often transistors, capacitors, etc. that would be rejects at higher voltages can be used. Voltage dividers, protective diodes, etc. often needed at higher voltages can be left out of designs. Power drains are so low that circuits can be made that will last months to years on a single cell.

A single cell is more reliable and has a higher energy density then multiple cells. This is due to lack of cell interconnections and insulation as well as elimination of packaging to hold multiple cells in place.



Specifying A/D and D/A Converters

National Semiconductor
Application Note 156

The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you ensure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

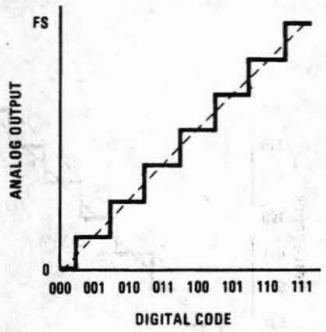
This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

MEANING OF PERFORMANCE SPECS

Resolution describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in 2^n. The least significant increment is then 2^{-n}, or one least significant bit (LSB). In contrast, the most significant bit (MSB) carries a weight of 2^{-1}. Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in 2^{12} (1 part in 4096) or 0.0244% of full scale. A converter with 10V full scale could resolve a 2.44mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0244% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

Accuracy is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than $\pm 1/2$ LSB or ± 1 part in 2^{12+1} ($\pm 0.0122\%$ of full scale) due to finite resolution. This would be the case in *Figure 1* if there were no errors. Actually, $\pm 0.0122\%$ FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ± 1 LSB accurate, this is equivalent to $\pm 0.0245\%$ or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately.



TL/H/5612–1

FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy

Quantizing Error is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset ½ LSB at zero scale as shown in *Figure 2*, exhibits only ±½ LSB maximum output error. If not offset, the error will be $\frac{-1}{+0}$ LSB as shown in *Figure 3*. For example, a perfect 12-bit ADC will show a ±½ LSB error of ±0.0122% while the quantizing error of an 8-bit ADC is ±½ part in 2^8 or ±0.195% of full scale. Quantizing error is not strictly applicable to a DAC; the equivalent effect is more properly a resolution error.

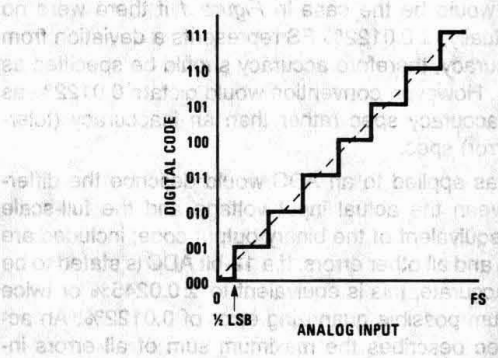
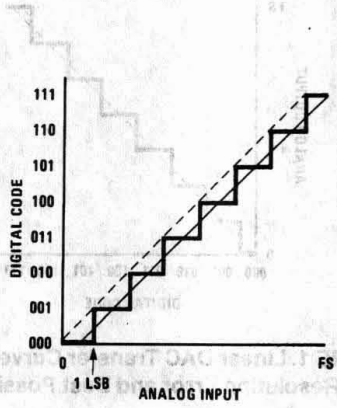


FIGURE 2. ADC Transfer Curve, ½ LSB Offset at Zero



TL/H/5612–2

FIGURE 3. ADC Transfer Curve, No Offset

Scale Error (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See *Figure 4*.) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient**.) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of *Figure 7*, a scale adjustment at ¾ scale could improve the overall ± accuracy compared to an adjustment at full scale.

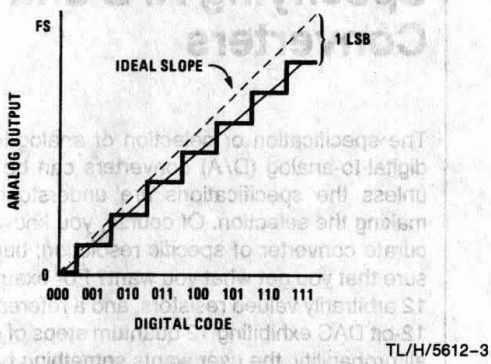


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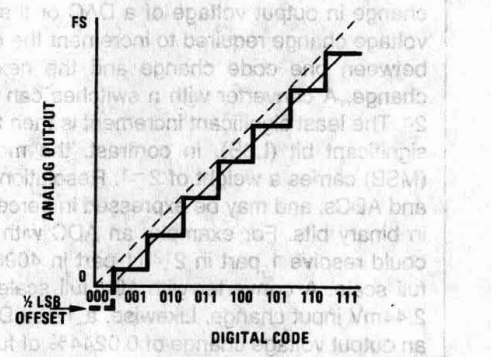
FIGURE 4. Linear, 1 LSB Scale Error

Gain Error is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

Offset Error (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See *Figure 5*.) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.



TL/H/5612–4

FIGURE 5. DAC Transfer Curve, ½ LSB Offset at Zero

Hysteresis Error in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches ½ LSB.

Linearity, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specification of ± ½ LSB

linearity implies error in addition to the inherent ±½ LSB quantizing or resolution error. In reference to *Figure 2*, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than ±½ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ±1 LSB (½ LSB resolution error plus ½ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A ±½ LSB linearity spec guarantees monotonicity (see below) and ≤±1 LSB differential non-linearity (see below). In the example of *Figure 6*, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond ±½ LSB will allow for a non-monotonic transfer curve. *Figure 7* shows a typical non-linear curve; non-linearity is 1¼ LSB yet the curve is smooth and monotonic.

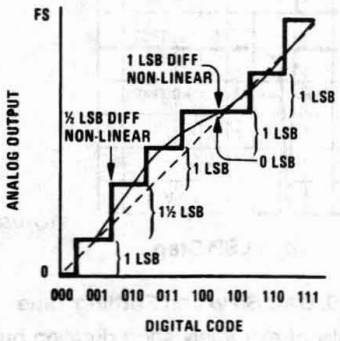
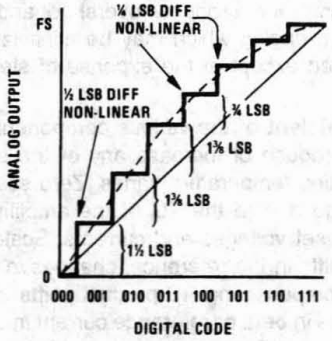


FIGURE 6. ±½ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)



TL/H/5612–5

FIGURE 7. 1¼ LSB Non-Linear, ½ LSB Differential Non-Linearity

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

Differential Non-Linearity indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit ½ LSB differential non-linearity (see *Figures 6* and *7*). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. *Figure 6* shows a curve with a ±½ LSB linearity and ±1 LSB differential non-linearity while *Figure 7* shows a curve with +1¼ LSB linearity and ±½ LSB differential non-linearity. In many user applications, the curve of *Figure 7* would be preferred over that of *Figure 6* because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in *Figure 8* where the linearity spec is ±1 LSB and the differential linearity spec is ±2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in *Figure 8*. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2.6-bit converter?). The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter. Differential non-linearity can always be as much as twice the non-linearity, but no more.

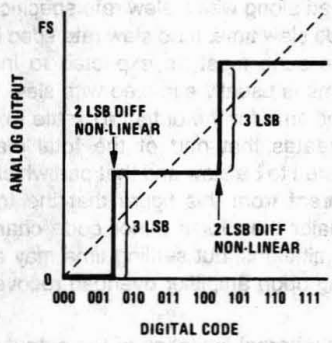


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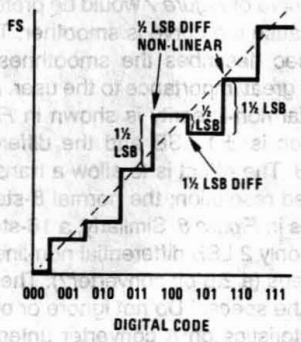
FIGURE 8. ±1 LSB Linear, ±2 LSB Differential Non-Linear

Monotonicity. A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed ±½ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage is some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A ±½ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than ±½ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with ±½ bit linearity to 10 bits (not ±½ LSB) will be monotonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.



TL/H/5612–7

FIGURE 9. Non-Monotonic (Must be > ±½ LSB Non-Linear)

Settling Time is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±½ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. *Figure 10* delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

Slew Rate is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/μs. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in *Figure 10*.

Overshoot and Glitches occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These

TL/H/5612–8

FIGURE 10. DAC Slew and Settling Time

glitches are normally of extremely short duration but could be of ½ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.

Temperature Coefficient of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

Long-Term Drift, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

Supply Rejection relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C.

Conversion Rate is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

Clock Rate is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

Input Impedance of an ADC describes the load placed on the analog source.

Output Drive Capability describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

CODES

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

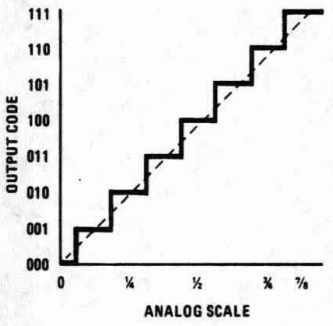
Natural Binary (or simply Binary) is the usual 2^n code with 2, 4, 8, 16, . . . , 2^n progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal. Zero scale is then all "zeros" while full scale is all "ones."

Complementary Binary (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

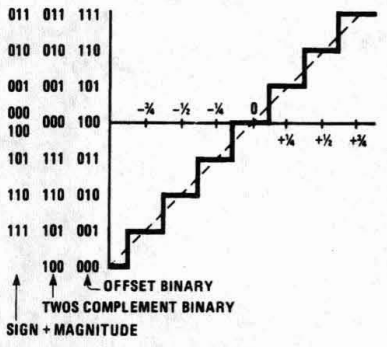
Binary Coded Decimal (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

Offset Binary is a natural binary code except that it is offset (usually ½ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in *Figure 11.*

Two's Complement Binary is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number −8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for ± representation in 4 bits so not a valid code in the ± scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in *Figure 11.* Note that the offset binary representation of the ± scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.



(a) Zero to + Full-Scale



TL/H/5612–9

(b) ± Full-Scale

FIGURE 11. ADC Codes

Sign Plus Magnitude coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in *Figure 11*. Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

CONTROL

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

Start Conversion (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

End of Conversion (EOC) is a digital signal from an ADC which informs the external system that the digital output data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

Clock signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

CONCLUSION

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

IC Voltage Reference has 1 ppm per Degree Drift

National Semiconductor
Application Note 161

A new linear IC now provides the ultimate in highly stable voltage references. Now, a new monolithic IC the LM199, out-performs zeners and can provide a 6.9V reference with a temperature drift of less than 1 ppm/° and excellent long term stability. This new IC, uses a unique subsurface zener to achieve low noise and a highly stable breakdown. Included is an on-chip temperature stabilizer which holds the chip temperature at 90°C, eliminating the effects of ambient temperature changes on reference voltage.

The planar monolithic IC offers superior performance compared to conventional reference diodes. For example, active circuitry buffers the reverse current to the zener giving a dynamic impedance of 0.5Ω and allows the LM199 to operate over a 0.5 mA to 10 mA current range with no change in performance. The low dynamic impedance, coupled with low operating current significantly simplifies the current drive circuitry needed for operation. Since the temperature coefficient is independent of operating current, usually a resistor is all that is needed.

Previously, the task of providing a stable, low temperature coefficient reference voltage was left to a discrete zener diode. However, these diodes often presented significant problems. For example, ordinary zeners can show many millivolts change if there is a temperature gradient across the package due to the zener and temperature compensation diode not being at the same temperature. A 1°C difference may cause a 2 mV shift in reference voltage. Because the on-chip temperature stabilizer maintains constant die temperature, the IC reference is free of voltage shifts due to temperature gradients. Further, the temperature stabilizer, as well as eliminating drift, allows exceptionally fast warm-up over conventional diodes. Also, the LM199 is insensitive to stress on the leads—another source of error with ordinary glass diodes. Finally, the LM199 shows virtually no hysteresis in reference voltage when subject to temperature cycling over a wide temperature range. Temperature cycling the LM199 between 25°C, 150°C and back to 25°C causes less than 50 μV change in reference voltage. Standard reference diodes exhibit shifts of 1 mV to 5 mV under the same conditions.

SUB SURFACE ZENER IMPROVES STABILITY

Previously, breakdown references made in monolithic IC's usually used the emitter-base junction of an NPN transistor as a zener diode. Unfortunately, this junction breaks down at the surface of the silicon and is therefore susceptible to surface effects. The breakdown is noisy, and cannot give long-term stabilities much better than about 0.3%. Further, a surface zener is especially sensitive to contamination in the oxide or charge on the surface of the oxide which can cause short-term instability or turn-on drift.

The new zener moves the breakdown below the surface of the silicon into the bulk yielding a zener that is stable with time and exhibits very low noise. Because the new zener is made with well-controlled diffusions in a planar structure, it is extremely reproducible with an initial 2% tolerance on breakdown voltage.

A cut-away view of the new zener is shown in *Figure 1.* First a small deep P^+ diffusion is made into the surface of the silicon. This is then covered by the standard base diffusion. The N^+ emitter diffusion is then made completely covering the P^+ diffusion. The diode then breaks down where the dopant concentration is greatest, that is, between the P^+ and N^+. Since the P^+ is completely covered by N^+ the breakdown is below the surface and at about 6.3V. One connection to the diode is to the N^+ and the other is to the P base diffusion. The current flows laterally through the base to the P^+ or cathode of the zener. Surface breakdown does not occur since the base P to N^+ breakdown voltage is greater than the breakdown of the buried device. The buried zener has been in volume production since 1973 as the reference in the LX5600 temperature transducer.

CIRCUIT DESCRIPTION

The block diagram of the LM199 is shown in *Figure 2.* Two electrically independent circuits are included on the same chip—a temperature stabilizer and a floating active zener. The only electrical connection between the two circuits

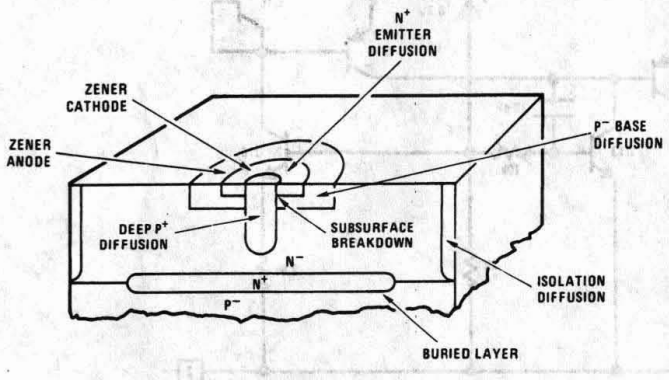
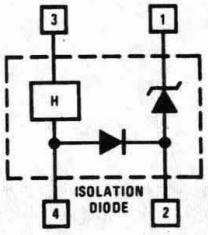


FIGURE 1. Subsurface Zener Construction



TL/H/5613–1

FIGURE 2. Functional Block Diagram

is the isolation diode inherent in any junction-isolated integrated circuit. The zener may be used with or without the temperature stabilizer powered. The only operating restriction is that the isolation diode must never become forward biased and the zener must not be biased above the 40V breakdown of the isolation diode.

The actual circuit is shown in *Figure 3.* The temperature stabilizer is composed of Q1 through Q9. FET Q9 provides current to zener D2 and Q8. Current through Q8 turns a loop consisting of D1, Q5, Q6, Q7, R1 and R2. About 5V is applied to the top of R1 from the base of Q7. This causes 400 μA to flow through the divider R1, R2. Transistor Q7 has a controlled gain of 0.3 giving Q7 a total emitter current of about 500 μA. This flows through the emitter of Q6 and drives another controlled gain PNP transistor Q5. The gain of Q5 is about 0.4 so D1 is driven with about 200 μA. Once current flows through Q5, Q8 is reverse biased and the loop is self-sustaining. This circuitry ensures start-up.

The resistor divider applies 400 mV to the base of Q4 while Q7 supplies 120 μA to its collector. At temperatures below the stabilization point, 400 mV is insufficient to cause Q4 to conduct. Thus, all the collector current from Q7 is provided as base drive to a Darlington composed of Q1 and Q2. The Darlington is connected across the supply and initially draws 140 mA (set by current limit transistor Q3). As the chip heats, the turn on voltage for Q4 decreases and Q4 starts to conduct. At about 90°C the current through Q4 appreciably increases and less drive is applied to Q1 and Q2. Power dissipation decreases to whatever is necessary to hold the chip at the stabilization temperature. In this manner, the chip temperature is regulated to better than 2°C for a 100°C temperature range.

The zener section is relatively straight-forward. A buried zener D3 breaks down biasing the base of transistor Q13. Transistor Q13 drives two buffers Q12 and Q11. External current changes through the circuit are fully absorbed by the buffer transistors rather than D3. Current through D3 is held constant at 250 μA by a 2k resistor across the emitter base of Q13 while the emitter-base voltage of Q13 nominally temperature compensates the reference voltage.

The other components, Q14, Q15 and Q16 set the operating current of Q13. Frequency compensation is accomplished with two junction capacitors.

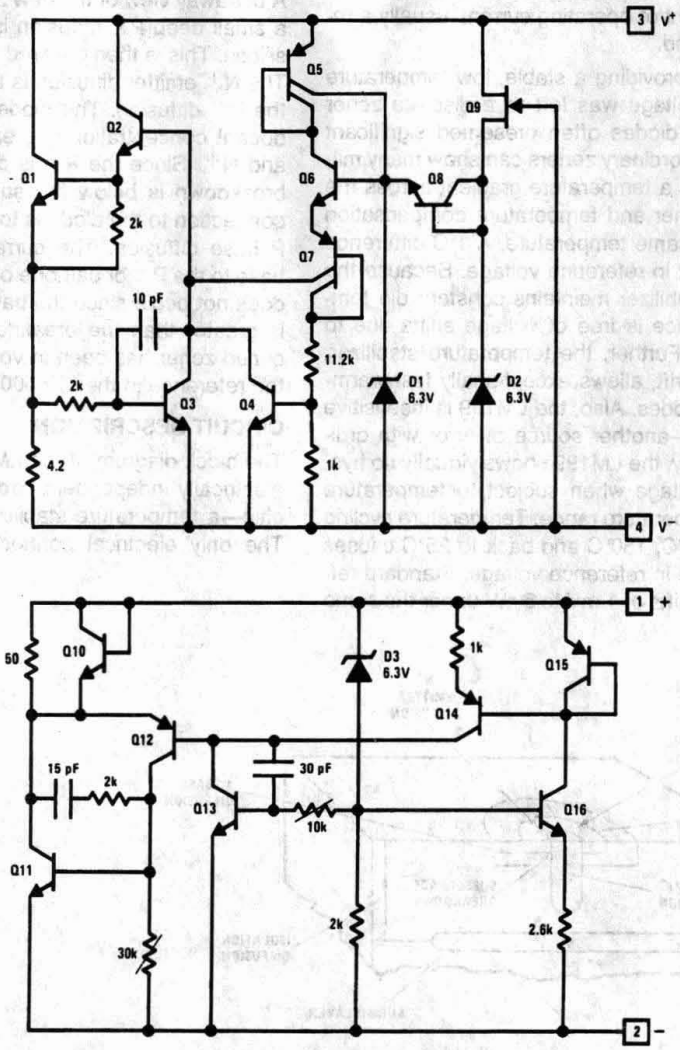


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FIGURE 3. Schematic Diagram of LM199 Precision Reference

PERFORMANCE

A polysulfone thermal shield, shown in *Figure 4,* is supplied with the LM199 to minimize power dissipation and improve temperature regulation. Using a thermal shield as well as the small, high thermal resistance TO-46 package allows operation at low power levels without the problems of special IC packages with built-in thermal isolation. Since the LM199 is made on a standard IC assembly line with standard assembly techniques, cost is significantly lower than if special techniques were used. For temperature stabilization only 300 mW are required at 25°C and 660 mW at −55°C.

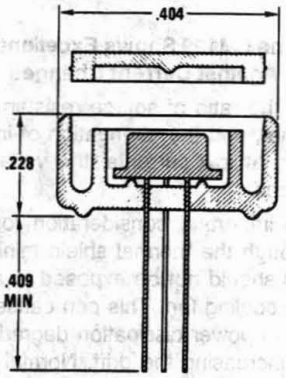

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FIGURE 4. Polysulfone Thermal Shield

Temperature stabilizing the device at 90°C virtually eliminates temperature drift at ambient temperatures less than 90°C. The reference is nominally temperature compensated and the thermal regulator further decreases the temperature drift. Drift is typically only 0.3 ppm/°C. Stabilizing the temperature at 90°C rather than 125°C significantly reduces power dissipation but still provides very low drift over a major portion of the operating temperature range. Above 90°C ambient, the temperature coefficient is only 15 ppm/°C.

A low drift reference would be virtually useless without equivalent performance in long term stability and low noise. The subsurface breakdown technology yields both of these. Wideband and low frequency noise are both exceptionally low. Wideband noise is shown in *Figure 5* and low frequency noise is shown over a 10 minute period in the photograph of *Figure 6.* Peak to peak noise over a 0.01 Hz to 1 Hz bandwidth is only about 0.7 μV.

Long term stability is perhaps one of the most difficult measurements to make. However, conditions for long-term stability measurements on the LM199 are considerably more realistic than for commercially available certified zeners. Standard zeners are measured in ±0.05°C temperature controlled both at an operating current of 7.5 mA ±0.05 μA. Further, the standard devices must have stress-free contacts on the leads and the test must not be interrupted during the measurement interval. In contrast, the LM199 is measured in still air of 25°C to 28°C at a reverse current of 1 mA ±0.5%. This is more typical of actual operating conditions in instruments.

When a group of 10 devices were monitored for long-term stability, the variations all correlated, which indicates changes in the measurement system (limitation of 20 ppm) rather than the LM199.

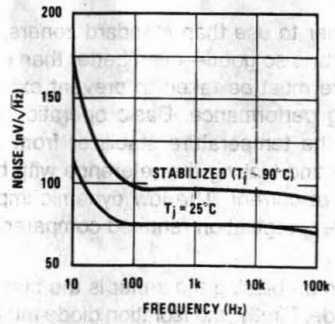

FIGURE 5. Wideband Noise of the LM199 Reference

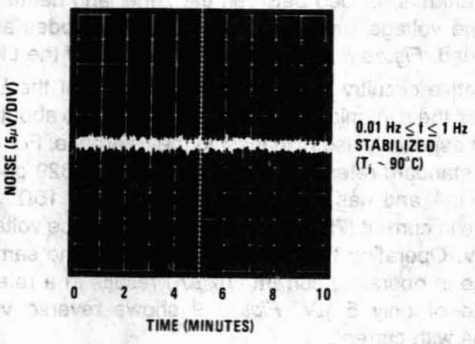

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FIGURE 6. Low Frequency Noise Voltage

Because the planar structure does not exhibit hysteresis with temperature cycling, long-term stability is not impaired if the device is switched on and off.

The temperature stabilizer heats the small thermal mass of the LM199 to 90°C very quickly. Warm-up time at 25°C and −55°C is shown in *Figure 7.* This fast warm-up is significantly less than the several minutes needed by ordinary diodes to reach equilibrium. Typical specifications are shown in Table I.

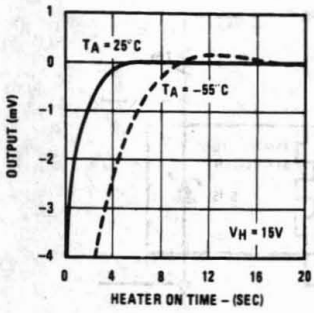

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FIGURE 7. Fast Warmup Time of the LM199

Table I. Typical Specifications for the LM199

Reverse Breakdown Voltage	6.95V
Operating Current	0.5 mA to 10 mA
Temperature Coefficient	0.3 ppm/°C
Dynamic Impedance	0.5Ω
RMS Noise (10 Hz to 10 kHz)	7μV
Long-Term Stability	≤20 ppm
Temperature Stabilizer Operating Voltage	9V to 40V
Temperature Stabilizer Power Dissipation (25°C)	300 mW
Warm-up Time	3 Seconds

APPLICATIONS

The LM199 is easier to use than standard zeners, but the temperature stability is so good—even better than precision resistors—that care must be taken to prevent external circuitry from limiting performance. Basic operation only requires energizing the temperature stabilizer from a 9V to 40V power source and biasing the reference with between 0.5 mA to 10 mA of current. The low dynamic impedance minimizes the current regulation required compared to ordinary zeners.

The only restriction on biasing the zener is the bias applied to the isolation diode. Firstly, the isolation diode must not be forward biased. This restricts the voltage at either terminal of the zener to a voltage equal to or greater than the V^-.

A dc return is needed between the zener and heater to insure the voltage limitation on the isolation diodes are not exceeded. *Figure 8* shows the basic biasing of the LM199.

The active circuitry in the reference section of the LM199 reduces the dynamic impedance of the zener to about 0.5Ω. This is especially useful in biasing the reference. For example, a standard reference diode such as a 1N829 operates at 7.5 mA and has a dynamic impedance of 15Ω. A 1% change in current (75 μA) changes the reference voltage by 1.1 mV. Operating the LM199 at 1 mA with the same 1% change in operating current (10 μA) results in a reference change of only 5 μV. *Figure 9* shows reverse voltage change with current.

Biasing current for the reference can by anywhere from 0.5 mA to 10 mA with little change in performance. This wide current range allows direct replacement of most zener types with no other circuit changes besides the temperature stabilizer connection. Since the dynamic impedance is constant with current changes regulation is better than discrete zeners. For optimum regulation, lower operating currents are

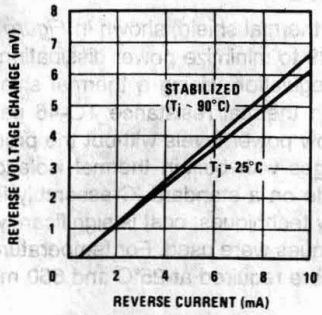

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FIGURE 9. The LM199 Shows Excellent Regulation Against Current Changes

preferred since the ratio of source resistance to zener impedance is higher, and the attenuation of input changes is greater. Further, at low currents, the voltage drop in the wiring is minimized.

Mounting is an important consideration for optimum performance. Although the thermal shield minimizes the heat low, the LM199 should not be exposed to a direct air flow such as from a cooling fan. This can cause as much as a 100% increase in power dissipation degrading the thermal regulation and increasing the drift. Normal conviction currents do not degrade performance.

Printed circuit board layout is also important. Firstly, four wire sensing should be used to eliminate ohmic drops in pc traces. Although the voltage drops are small the temperature coefficient of the voltage developed along a copper trace can add significantly to the drift. For example, a trace with 1Ω resistance and 2 mA current flow will develop 2 mV drop. The TC of copper is 0.004%/°C so the 2 mV drop will change at 8 μV/°C, this is an additional 1 ppm drift error. Of course, the effects of voltage drops in the printed circuit traces are eliminated with 4-wire operation. The heater current also should not be allowed to flow through the voltage reference traces. Over a −55°C to +125°C temperature

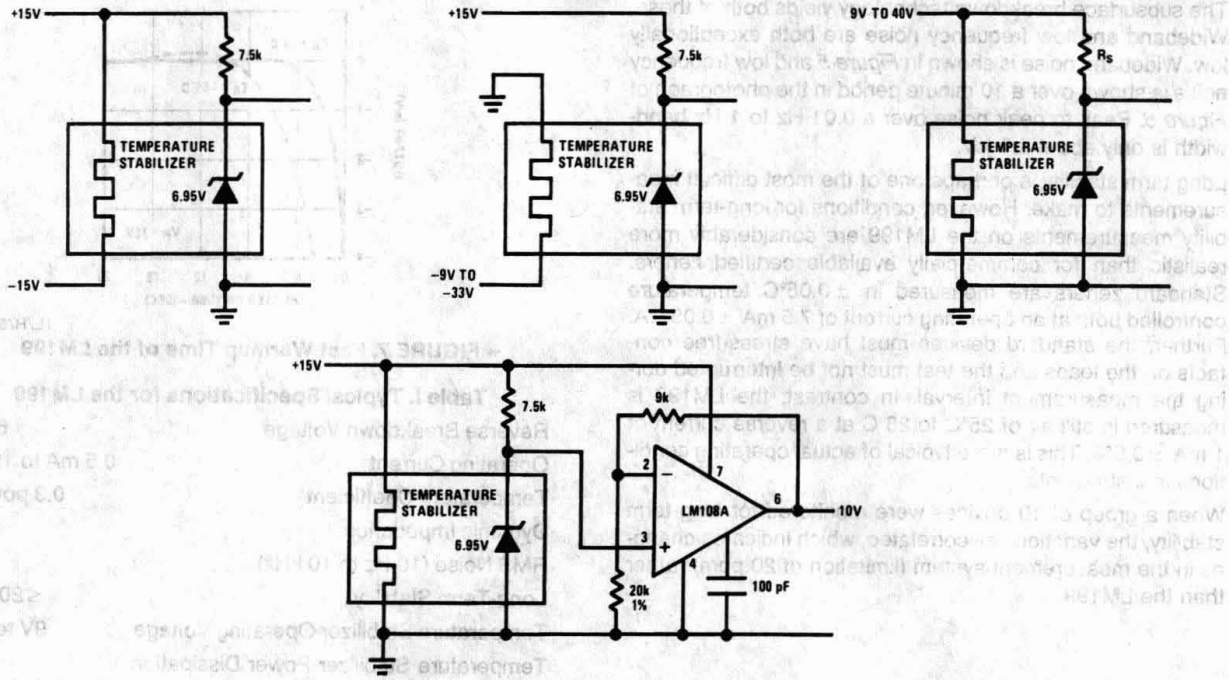

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FIGURE 8. Basic Biasing of the LM199

range the heater current will change from about 1 mA to over 40 mA. These magnitudes of current flowing reference leads or reference ground can cause huge errors compared to the drift of the LM199.

Thermocouple effects can also use errors. The kovar leads from the LM199 package from a thermocouple with copper printed circuit board traces. Since the package of the 199 is heated, there is a heat flow along the leads of the LM199 package. If the leads terminate into unequal sizes of copper on the p.c. board greater heat will be absorbed by the larger copper trace and a temperature difference will develop. A temperature *difference* of 1°C between the two leads of the reference will generate about 30 μA. Therefore, the copper traces to the zener should be equal in size. This will generally keep the errors due to thermocouple effects under about 15 μV.

The LM199 should be mounted flush on the p.c. board with a minimum of space between the thermal shield and the boards. This minimizes air flow across the kovar leads on the board surface which also can cause thermocouple voltages. Air currents across the leads usually appear as ultra-low frequency noise of about 10 μV to 20 μV amplitude.

It is usually necessary to scale and buffer the output of any reference to some calibrated voltage. *Figure 10* shows a simple buffered reference with a 10V output. The reference is applied to the non-inverting input of the LM108A. An RC rolloff can be inserted in series with the input to the LM108A to roll-off the high frequency noise. The zener heater and op amp are all powered from a single 15V supply. About 1% regulation on the input supply is adequate contributing less than 10 μV of error to the output. Feedback resistors around the LM308 scale the output to 10V.

Although the absolute values of the resistors are not extremely important, tracking of temperature coefficients is vital. The 1 ppm/°C drift of the LM199 is easily exceeded by the temperature coefficient of most resistors. Tracking to better than 1 ppm is also not easy to obtain. Wirewound types made of Evenohm or Mangamin are good and also have low thermoelectric effects. Film types such as Vishay resistors are also good. Most potentiometers do not track fixed resistors so it is a good idea to minimize the adjustment range and therefore minimize their effects on the output TC. Overall temperature coefficient of the circuit shown in *Figure 10* is worst case 3 ppm/°C. About 1 ppm is due to the reference, 1 ppm due to the resistors and 1 ppm due to the op amp.

Figure 11 shows a standard cell replacement with a 1.01V output. A LM321 and LM308 are used to minimize op amp drift to less than 1 μV/°C. Note the adjustment connection which minimizes the TC effects of the pot. Set-up for this circuit requires nulling the offset of the op amp first and then adjusting for proper output voltage.

The drift of the LM321 is very predictable and can be used to eliminate overall drift of the system. The drift changes at 3.6 μV/°C per millivolt of offset so 1 mV to 2 mV of offset can be introduced to minimize the overall TC.

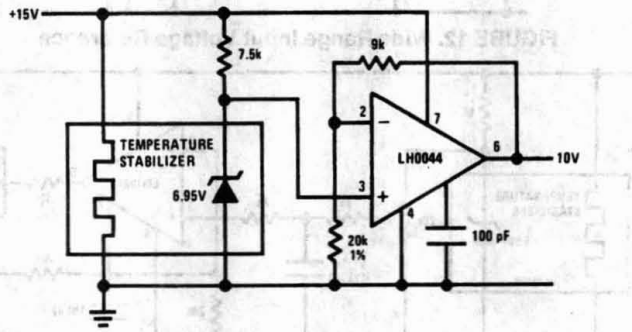

FIGURE 10. Buffered 10V Reference

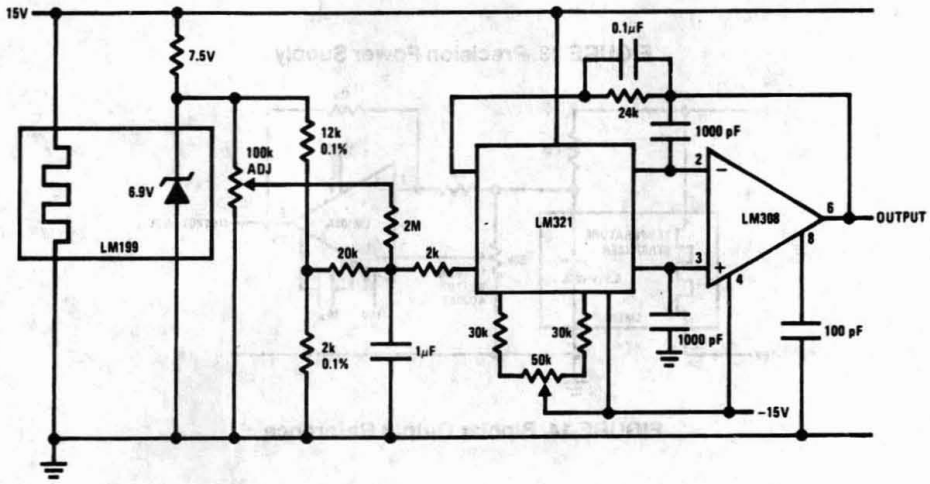

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FIGURE 11. Standard Cell Replacement

For circuits with a wide input voltage range, the reference can be powered from the output of the buffer as is shown in *Figure 12.* The op amp supplies regulated voltage to the resistor biasing the reference minimizing changes due to input variation. There is some change due to variation of the temperature stabilizer voltage so extremely wide range operation is not recommended for highest precision. An additional resistor (shown 80 kΩ) is added to the unregulated input to insure the circuit starts up properly at the application of power.

A precision power supply is shown in *Figure 13.* The output of the op amp is buffered by an IC power transistor the LM395. The LM395 operates as an NPN power device but requires only 5 μA base current. Full overload protection inherent in the LM395 includes current limit, safe-area protection, and thermal limit.

A reference which can supply either a positive or a negative continuously variable output is shown in *Figure 14.* The reference is biased from the ±15 input supplies as was shown earlier. A ten-turn pot will adjust the output from $+V_Z$ to $-V_Z$ continuously. For negative output the op amp operates as an inverter while for positive outputs it operates as a non-inverting connection.

Op amp choice is important for this circuit. A low drift device such as the LM108A or a LM108-LM121 combination will provide excellent performance. The pot should be a precision wire wound 10 turn type. It should be noted that the output of this circuit is not linear.

CONCLUSIONS

A new monolithic reference which exceeds the performance of conventional zeners has been developed. In fact, the LM199 performance is limited more by external components than by reference drift itself. Further, many of the problems associated with conventional zeners such as hysteresis, stress sensitivity and temperature gradient sensitivity have also been eliminated. Finally, long-term stability and noise are equal of the drift performance of the new device.

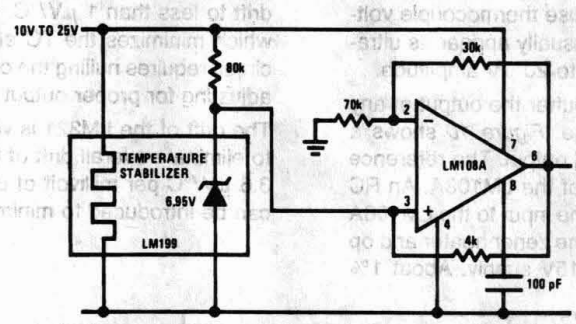

FIGURE 12. Wide Range Input Voltage Reference

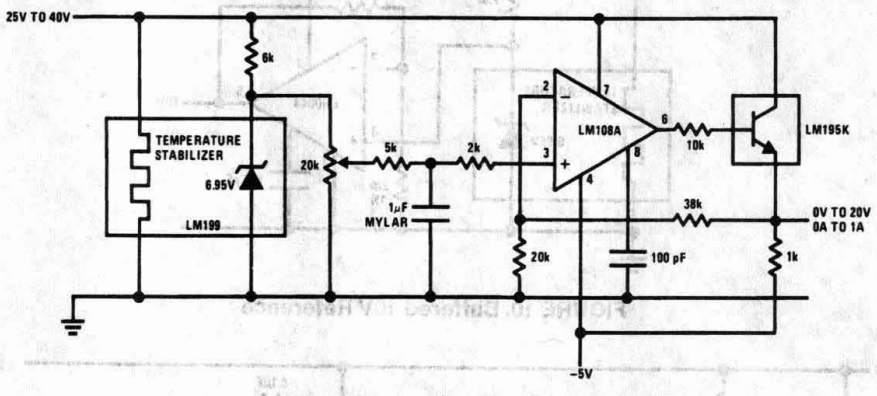

FIGURE 13. Precision Power Supply

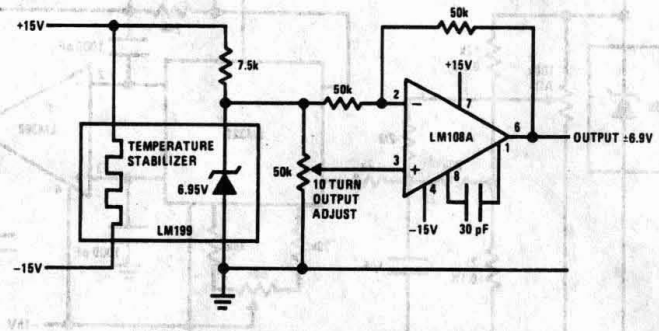

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FIGURE 14. Bipolar Output Reference

LM2907 Tachometer/Speed Switch Building Block Applications

National Semiconductor
Application Note 162

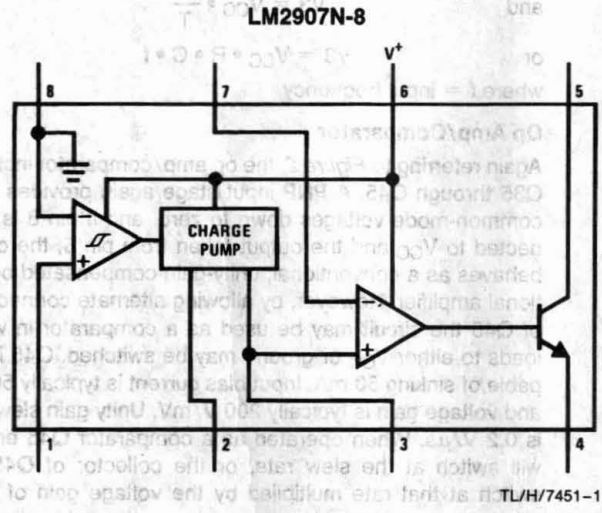
INTRODUCTION

Frequency to voltage converters are available in a number of forms from a number of sources, but invariably require significant additional components before they can be put to use in a given situation. The LM2907, LM2917 series of devices was developed to overcome these objections. Both input and output interface circuitry is included on chip so that a minimum number of additional components is required to complete the function. In keeping with the systems building block concept, these devices provide an output voltage which is proportional to input frequency and provide zero output at zero frequency. In addition, the input may be referred to ground. The devices are designed to operate from a single supply voltage, which makes them particularly suitable for battery operation.

PART 1—GENERAL OPERATION PRINCIPLES

Circuit Description

Referring to *Figure 1,* the family of devices all include three basic components: an input amplifier with built-in hysteresis; a charge pump frequency to voltage converter; and a versatile op amp/comparator with an uncommitted output transistor. LM2917 incorporates an active zener regulator on-chip. LM2907 deletes this option. Both versions are obtainable in 14-pin and in 8-pin dual-in-line molded packages, and to special order in other packages.



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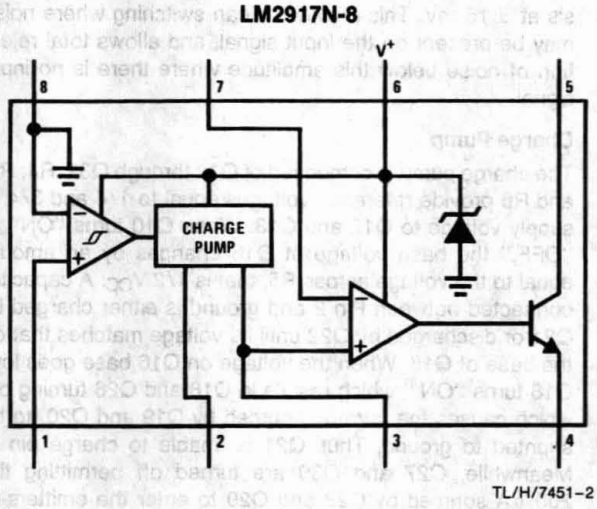

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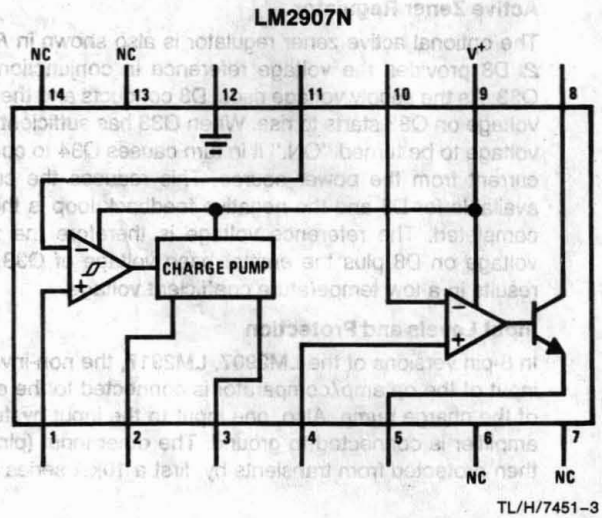

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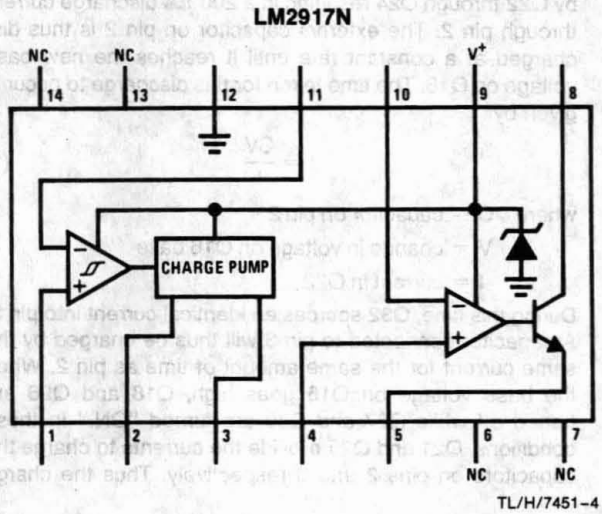

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FIGURE 1. Block Diagrams

Input Hysteresis Amplifier

The equivalent schematic diagram is shown in *Figure 2.* Q1 through Q11 comprise the input hysteresis amplifier. Q1 through Q4 comprise an input differential amplifier which, by virtue of PNP level shifting, enables the circuit to operate with signals referenced to ground. Q7, Q8, D4, and D5 comprise an active load with positive feedback. This load behaves as a bi-stable flip-flop which may be set or reset depending upon the currents supplied from Q2 and Q3. Consider the situation where Q2 and Q3 are conducting equally, i.e. the input differential voltage is zero. Assuming Q7 to be conducting, it will be noted that the current from Q3 will be drawn by Q7 and Q8 will be in the "OFF" state. This allows the current from Q2 to drive Q7 in parallel with D4 and a small resistor. D4 and Q7 are identical geometry devices, so that the resistor causes Q7 to be biased at a higher level than D4. Thus Q7 will be able to conduct more current than Q3 provides. In order to reverse the state of Q7 and Q8, it will be necessary to reduce the current from Q2 below that provided by Q3 by an amount which is established by R1. It can be shown that this requires a differential input to Q1 and Q4, of approximately 15mV. Since the circuit is symmetrical, the threshold voltage to reverse the state is 15 mV in the other direction. Thus the input amplifier has built-in hysteresis at ±15 mV. This provides clean switching where noise may be present on the input signal, and allows total rejection of noise below this amplitude where there is no input signal.

Charge Pump

The charge pump is composed of Q12 through Q32. R4, R5, and R6 provide reference voltages equal to 1/4 and 3/4 of supply voltage to Q12 and Q13. When Q10 turns "ON" or "OFF," the base voltage at Q16 changes by an amount equal to the voltage across R5, that is $1/2\ V_{CC}$. A capacitor connected between Pin 2 and ground is either charged by Q21 or discharged by Q22 until its voltage matches that on the base of Q16. When the voltage on Q16 base goes low, Q16 turns "ON," which results in Q18 and Q26 turning on, which causes the current, sourced by Q19 and Q20, to be shunted to ground. Thus Q21 is unable to charge pin 2. Meanwhile, Q27 and Q30 are turned off permitting the 200 μA sourced by Q28 and Q29 to enter the emitters of Q31 and Q32 respectively. The current from Q31 is mirrored by Q22 through Q24 resulting in a 200 μA discharge current through pin 2. The external capacitor on pin 2 is thus discharged at a constant rate until it reaches the new base voltage on Q16. The time taken for this discharge to occur is given by:

$$t = \frac{CV}{I} \qquad (1)$$

where C = capacitor on pin 2
V = change in voltage on Q16 base
I = current in Q22

During this time, Q32 sources an identical current into pin 3. A capacitor connected to pin 3 will thus be charged by the same current for the same amount of time as pin 2. When the base voltage on Q16 goes high, Q18 and Q26 are turned off while Q27 and Q30 are turned "ON." In these conditions, Q21 and Q25 provide the currents to charge the capacitors on pins 2 and 3 respectively. Thus the charge required to return the capacitor on pin 2 to the high level voltage is duplicated and used to charge the capacitor connected to pin 3. Thus in one cycle of input the capacitor on pin 3 gets charged twice with a charge of CV.

Thus the total charge pumped into the capacitor on pin 3 per cycle is:

$$Q = 2\,CV \qquad (2)$$

Now, since $V = V_{CC}/2$

then $$Q = CV_{CC} \qquad (3)$$

A resistor connected between pin 3 and ground causes a discharge of the capacitor on pin 3, where the total charge drained per cycle of input signal is equal to:

$$Q1 = \frac{V3 \bullet T}{R}$$

where V3 = the average voltage on pin 3
T = period of input signal
R = resistor connected to pin 3

In equilibrium Q = Q1

$$\text{i.e., } CV_{CC} = \frac{V3 \bullet T}{R} \qquad (4)$$

and $$V3 = V_{CC} \bullet \frac{RC}{T} \qquad (5)$$

or $$V3 = V_{CC} \bullet R \bullet C \bullet f \qquad (6)$$

where f = input frequency

Op Amp/Comparator

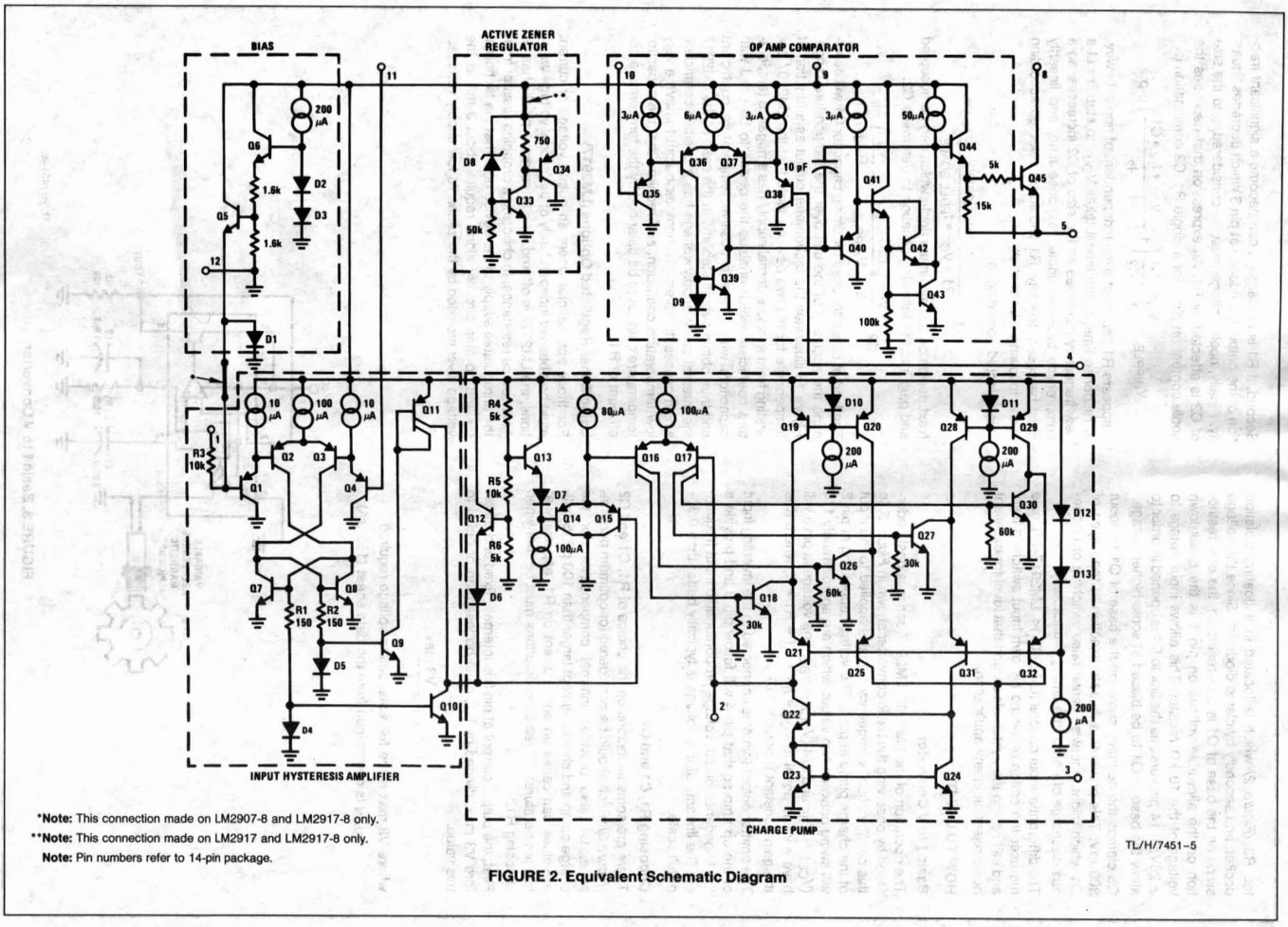
Again referring to *Figure 2,* the op amp/comparator includes Q35 through Q45. A PNP input stage again provides input common-mode voltages down to zero, and if pin 8 is connected to V_{CC} and the output taken from pin 5, the circuit behaves as a conventional, unity-gain-compensated operational amplifier. However, by allowing alternate connections of Q45 the circuit may be used as a comparator in which loads to either V_{CC} or ground may be switched. Q45 is capable of sinking 50 mA. Input bias current is typically 50 nA, and voltage gain is typically 200 V/mV. Unity gain slew rate is 0.2 V/μs. When operated as a comparator Q45 emitter will switch at the slew rate, or the collector of Q45 will switch at that rate multiplied by the voltage gain of Q45, which is user selectable.

Active Zener Regulator

The optional active zener regulator is also shown in *Figure 2.* D8 provides the voltage reference in conjunction with Q33. As the supply voltage rises, D8 conducts and the base voltage on Q33 starts to rise. When Q33 has sufficient base voltage to be turned "ON," it in turn causes Q34 to conduct current from the power source. This reduces the current available for D8 and the negative feedback loop is thereby completed. The reference voltage is therefore the zener voltage on D8 plus the emitter base voltage of Q33. This results in a low temperature coefficient voltage.

Input Levels and Protection

In 8-pin versions of the LM2907, LM2917, the non-inverting input of the op amp/comparator is connected to the output of the charge pump. Also, one input to the input hysteresis amplifier is connected to ground. The other input (pin 1) is then protected from transients by, first a 10kΩ series resis-



*Note: This connection made on LM2907-8 and LM2917-8 only.

**Note: This connection made on LM2917 and LM2917-8 only.

Note: Pin numbers refer to 14-pin package.

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FIGURE 2. Equivalent Schematic Diagram

tor, R3 *(Figure 2)* which is located in a floating isolation pocket, and secondly by clamp diode D1. Since the voltage swing on the base of Q1 is thus restricted, the only restriction on the allowable voltage on pin 1 is the breakdown voltage of the 10 kΩ resistor. This allows input swings to ±28V. In 14-pin versions the link to D1 is opened in order to allow the base of Q1 to be biased at some higher voltage.

Q5 clamps the negative swing on the base of Q1 to about 300 mV. This prevents substrate injection in the region of Q1 which might otherwise cause false switching or erroneous discharge of one of the timing capacitors.

The differential input options (LM2907-14, LM2917-14), give the user the option of setting his own input switching level and still having the hysteresis around that level for excellent noise rejection in any application.

HOW TO USE IT

Basic f to V Converter

The operation of the LM2907, LM2917 series is best understood by observing the basic converter shown in *Figure 3.* In this configuration, a frequency signal is applied to the input of the charge pump at pin 1. The voltage appearing at pin 2 will swing between two values which are approximately 1/4 (V_{CC}) − V_{BE} and 3/4 (V_{CC}) − V_{BE}. The voltage at pin 3 will have a value equal to $V_{CC} \bullet f_{IN} \bullet C1 \bullet R1 \bullet K$, where K is the gain constant (normally 1.0).

The emitter output (pin 4) is connected to the inverting input of the op amp so that pin 4 will follow pin 3 and provide a low impedance output voltage proportional to input frequency. The linearity of this voltage is typically better than 0.3% of full scale.

Choosing R1, C1 and C2

There are some limitations on the choice of R1, C1 and C2 *(Figure 3)* which should be considered for optimum performance. C1 also provides internal compensation for the charge pump and should be kept larger than 100 pF. Smaller values can cause an error current on R1, especially at low temperatures. Three considerations must be met when choosing R1.

First, the output current at pin 3 is internally fixed and therefore V3 max, divided by R1, must be less than or equal to this value.

$$\therefore R1 \geq \frac{V3\ max}{I_{3MIN}}$$

where V3 max is the full scale output voltage required

I_{3MIN} is determined from the data sheet (150 μA)

Second, if R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Finally, ripple voltage must be considered, and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1, C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \bullet \frac{C1}{C2}\left(1 - \frac{V_{CC} \bullet f_{IN} \bullet C1}{I_2}\right) \text{p-p}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new frequency increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be cosen carefully. R1 should be selected according to the following relationship:

C is selected according to:

$$C1 = \frac{\text{V3 Full Scale}}{R1 \bullet V_{CC} \bullet f_{\text{FULL SCALE}}}$$

Next decide on the maximum ripple which can be accepted and plug into the following equation to determine C2:

$$C2 = \frac{V_{CC}}{2} \bullet \frac{C1}{V_{RIPPLE}}\left(1 - \frac{V_3}{R_1 I_2}\right)$$

The kind of capacitor used for timing capacitor C1 will determine the accuracy of the unit over the temperature range. *Figure 15* illustrates the tachometer output as a function of temperature for the two devices. Note that the LM2907 operating from a fixed external supply has a negative temperature coefficient which enables the device to be used with capacitors which have a positive temperature coefficient and thus obtain overall stabililty. In the case of the LM2917 the internal zener supply voltage has a positive coefficient which causes the overall tachometer output to have a very low temperature coefficient and requires that the capacitor temperature coefficient be balanced by the temperature coefficient of R1.

Using Zener Regulated Options (LM2917)

For those applications where an output voltage or current must be obtained independently of the supply voltage variations, the LM2917 is offered. The reference typically has an 11Ω source resistance. In choosing a dropping resistor from the unregulated supply to the device note that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages,

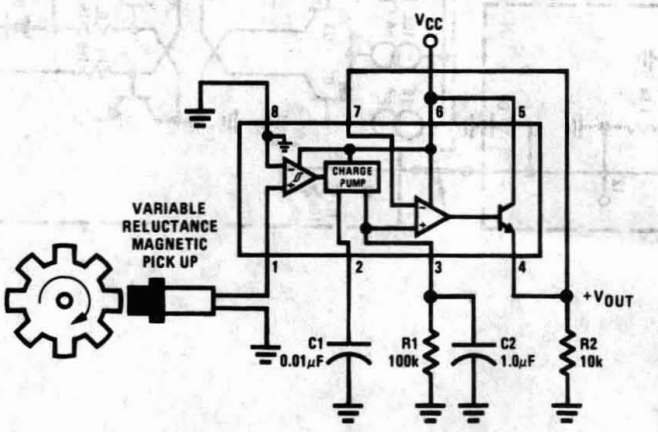

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FIGURE 3. Basic f to V Converter

there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9V to 16V, a resistance of 470Ω will minimize these zener voltage variations to 160 mV. If the resistor goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation. Take care also that the power dissipation of the IC is not exceeded at higher supply voltages. *Figure 4* shows suitable dropping resistor values.

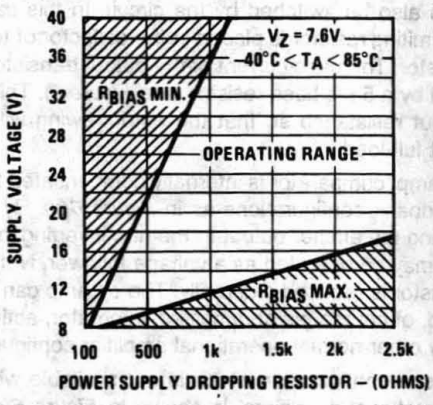

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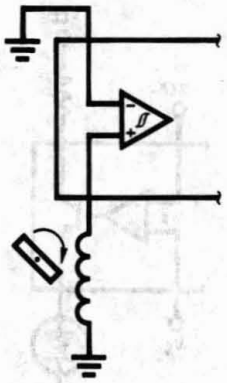
FIGURE 4. Zener Regular Bias Resistor Range

Input Interface Circuits

The ground referenced input capability of the LM2907-8 allows direct coupling to transformer inputs, or variable reluctance pickups. *Figure 5(a)* illustrates this connection. In many cases, the frequency signal must be obtained from another circuit whose output may not go below ground. This may be remedied by using ac coupling to the input of the LM2907 as illustrated in *Figure 5(b).* This approach is very suitable for use with phototransistors for optical pickups. Noisy signal sources may be coupled as shown in *Figure 5(c).* The signal is bandpass filtered. This can be used, for example, for tachometers operating from breakerpoints on a conventional Kettering ignition system. Remember that the minimum input signal required by the LM2907 is only 30 mVp-p, but this signal must be able to swing at least 15 mV on either side of the inverting input. The maximum signal which can be applied to the LM2907 input, is ±28V. The input bias current is a typically 100 nA. A path to ground must be provided for this current through the source or by other means as illustrated. With 14-pin package versions of LM2907, LM2917, it is possible to bias the inverting input to the tachometer as illustrated in *Figure 5(d).* This enables the circuit to operate with input signals that do not go to ground, but are referenced at higher voltages. Alternatively, this method increases the noise immunity where large signal



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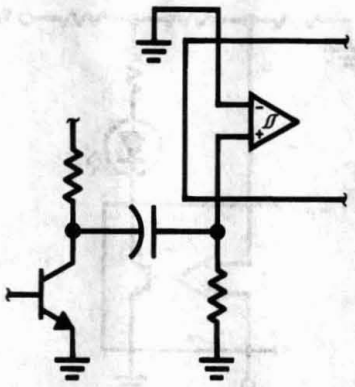
(a) Ground Referenced Inputs



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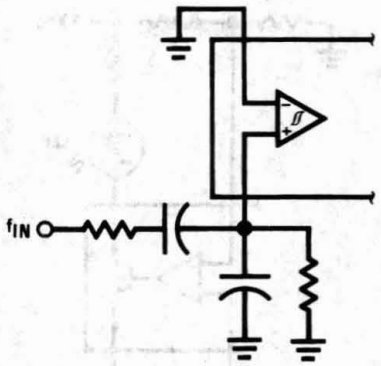
(b) AC Coupled Input



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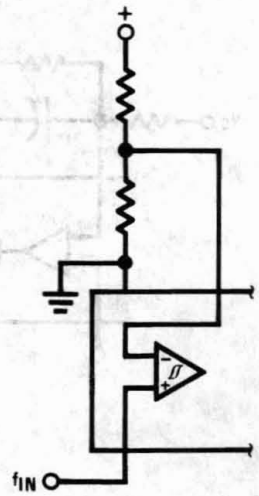
(c) Bandpass Filtered Input Reduces Noise



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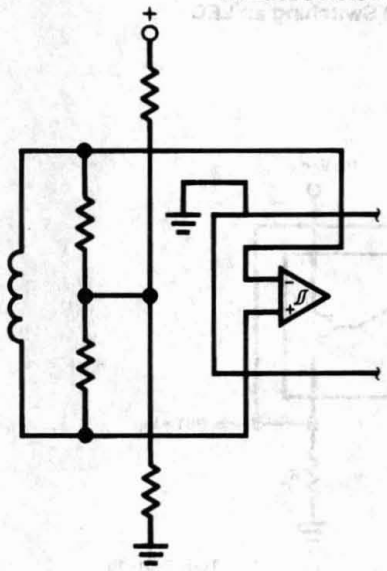
(d) Above Ground Sensing



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(e) High Common-Mode Rejection Input Circuit

FIGURE 5. Tachometer Input Configurations

levels are available but large noise signals on ground are also present. To take full advantage of the common-mode rejection of the input differential stage, a balanced bias configuration must be provided. One such circuit is illustrated in *Figure 5(e).* With this arrangement, the effective common-mode rejection may be virtually infinite, owing to the input hysteresis.

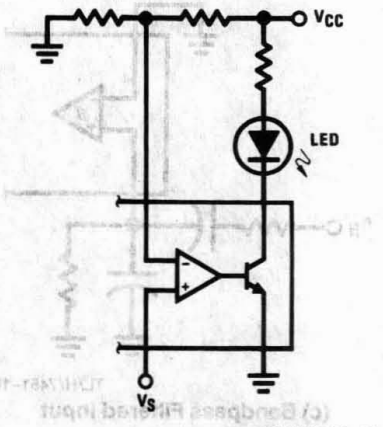
Output Configurations

LM2907, LM2917 series devices incorporate an unusually flexible op amp/comparator device on-chip for interfacing with a wide variety of loads. This flexibility results from the availability of both the collector and emitter of the output transistor which is capable of driving up to 50 mA of load current. When the non-inverting input is higher than the inverting input, this output transistor is turned "ON". It may be used to drive loads to either the positive or the negative supply with the emitter or collector respectively connected to the other supply. For example, *Figure 6(a),* a simple speed switch can be constructed in which the speed signal derived from the frequency to voltage converter is compared to a reference derived simply by a resistive divider from the power supply. When the speed signal exceeds the reference, the output transistor turns on the light emitting diode in the load. A small current limiting resistor should be placed in series with the output to protect the LED and the output transistor.

This circuit has no hysteresis in it, i.e., the turn "ON" and turn "OFF" speed voltages are essentially equal. In cases where speed may be fluctuating at a high rate and a flashing LED would be objectionable, it is possible to incorporate hysteresis so that the switch-on speed is above the switch-off speed by a controlled amount. Such a configuration is illustrated in *Figure 6(b). Figure 6(c)* shows how a grounded load can also be switched by the circuit. In this case, the current limiting resistor is placed in the collector of the power transistor. The base current of the output transistor (Q45) is limited by a 5 kΩ base resistor (see *Figure 2*). This raises the output resistance so that the output swing will be reduced at full load.

The op amp/comparator is internally compensated for unity gain feedback configurations as in *Figure 6(d).* By directly connecting the emitter output to the non-inverting input, the op amp may be operated as a voltage follower. Note that a load resistor is required externally. The op amp can also be operated, of course, as an amplifier, integrator, active filter, or in any other normal operational amplifier configuration.

One unique configuration which is not available with standard operational amplifiers, is shown in *Figure 6(e).* Here the collector of the output transistor is used to drive a load



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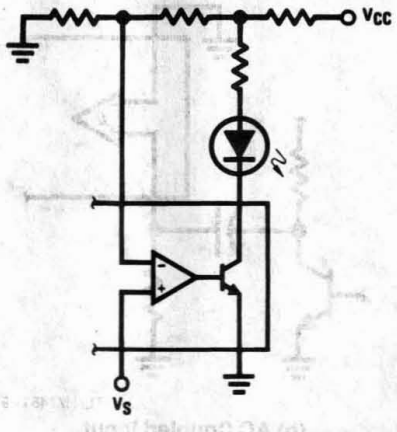
(a) Switching an LED



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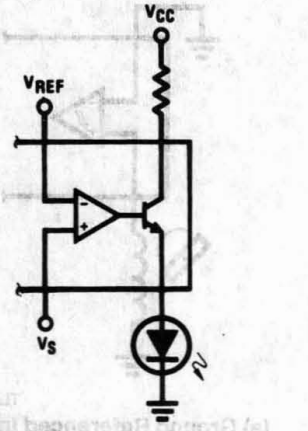
(b) Adding Hysteresis to LED Switch



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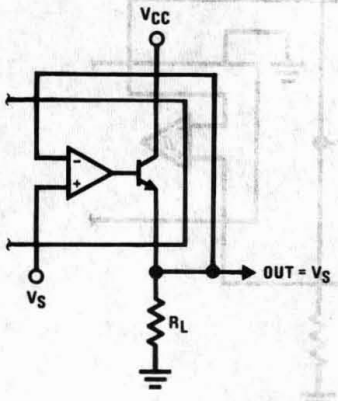
(c) Switching a Grounded Load



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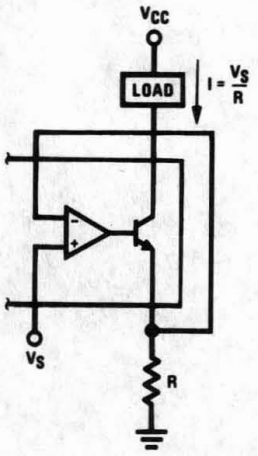
(d) Voltage Follower



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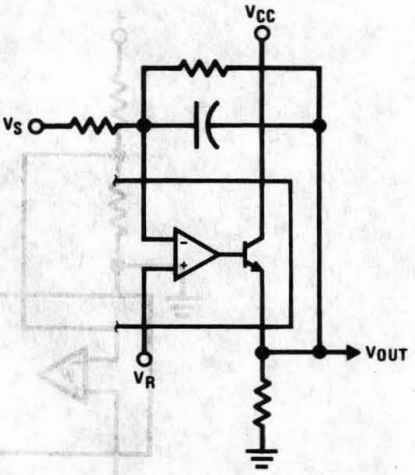
(e) Voltage to Current Converter



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(f) Integrator

FIGURE 6. Output Configurations

with a current which is proportional to the input voltage. In other words, the circuit is operating as a voltage to current converter. This is ideal for driving remote signal sensors and moving coil galvanometers. *Figure 6(f)* shows how an active integrator can be used to provide an output which falls with increasing speed.

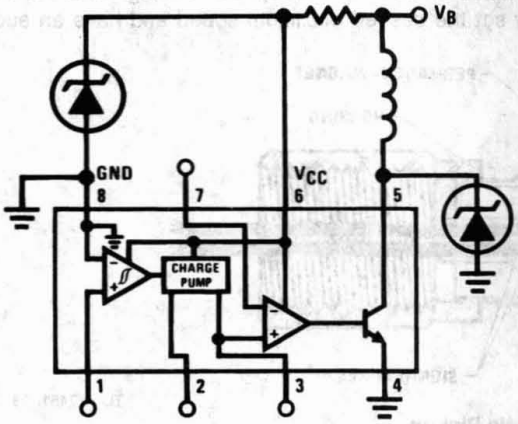
These are the basic configurations obtainable with the op amp/comparator. Further combinations can be seen in the applications shown in Part II of this application note.

Transient Protection

Many application areas use unregulated power supplies which tend to expose the electronics to potentially damaging transients on the power supply line. This is particularly true in the case of automotive applications where two such transients are common.[1] First is the load dump transient. This occurs when a dead battery is being charged at a high current and the battery cable comes loose, so that the current in the alternator inductance produces a positive transient on the line in the order of 60V to 120V. The second transient is called field decay. This occurs when the ignition is turned "OFF" and the energy stored in the field winding of the alternator causes a negative 75V transient on the ignition line.

Figure 7 illustrates methods for protecting against these and other transients. *Figure 7(a)* shows a typical situation in which the power supply to the LM2907 can be provided through a dropping resistor and regulated by an external zener diode Z1, but the output drive is required to operate from the full available supply voltage. In this case, a separate protection zener Z2 must be provided if the voltage on the power line is expected to exceed the maximum rated voltage of the LM2907.

In *Figure 7(b)* and *Figure 7(c),* the output transistor is required only to drive a simple resistive load and no secondary protection circuits are required. (Note that the dropping resistor to the zener also has to supply current to the output circuit). With the foregoing circuits, reverse supply protection is supplied by the forward biased zener diode. This device should be a low forward resistance unit in order to limit the maximum reverse voltage applied to the integrated circuit. Excessive reverse voltage on the IC can cause high currents to be conducted by the substrate diodes with consequent danger of permanent damage. Up to 1V negative can generally be tolerated. Versions with internal zeners may be self-protecting depending on the size of dropping resistor used. In applications where large negative voltage



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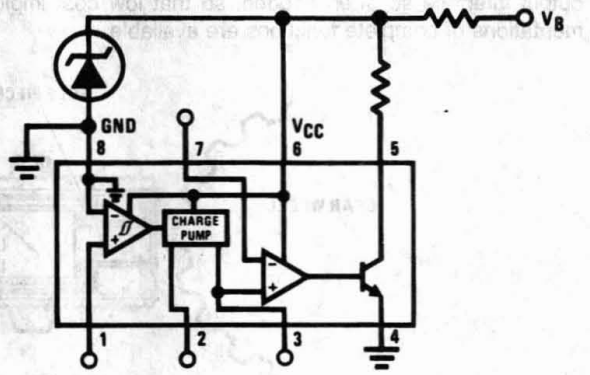
(a)



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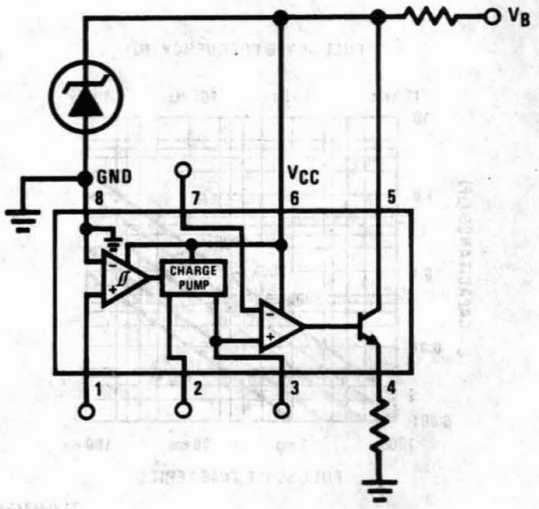
(b)



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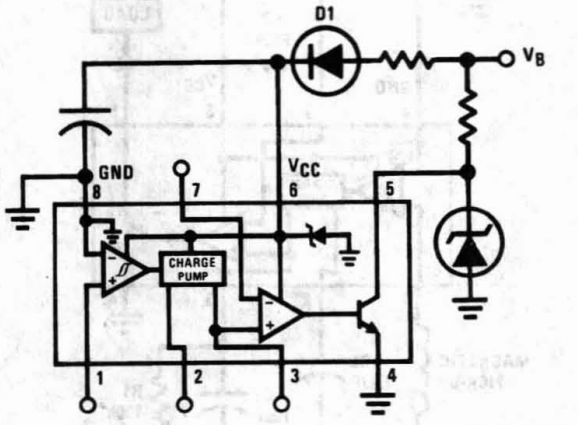
(c)



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(d)

FIGURE 7. Transient Protection Schemes

transients may be anticipated, a blocking diode may be connected in the power supply line to the IC as illustrated in *Figure 7(d).* During these negative transients, the diode D1 will be reverse biased and prevent reverse currents flowing in the IC. If these transients are short and the capacitor C1 is large enough, then the power to the IC can be sustained. This is useful to prevent change of state or change of charge in in systems connected to it.

Temperature Ranges and Packaging Considerations

The LM2907, LM2917 series devices are specified for operation over the temperature range −40°C to +85°C.

The devices are normally packaged in molded epoxy, dual-in-line packages. Other temperature ranges and other packages are availabe to special order. For reliability requirements beyond those of normal commercial application where the cost of military qualification is not bearable, other programs are available such as B+.

PART II—APPLICATIONS

INTRODUCTION

The LM 2907, LM2917 series devices were designed not only to perform the basic frequency to voltage function required in many systems, but also to provide the input and output interface so often needed, so that low cost implementations of complete functions are available.

The concept of building blocks requires that a function be performed in the same way as it can be mathematically defined. In other words, a frequency to voltage converter will provide an output voltage proportional to frequency which is independent of the input voltage or other input parameters, except the frequency. In the same way, the output voltage will be zero when the input frequency is zero. These features are built into the LM2907.

Applications for the device range from simple speed switch for anti-pollution control device functions in automobiles, to motor speed controls in industrial applications. The applications circuits which follow are designed to illustrate some of the capabilities of the LM2907. In most cases, alternative input or output configurations can be mixed and matched at will and other variations can be determined from the description in Part I of this application note. For complete specifications, refer to the data sheet.

Speed Switches

Perhaps the most natural application of the LM2907 is in interfacing with magnetic pickups, such as the one illustrated in *Figure 8* to perform speed switching functions. As an example, New York taxies are required to change the intensity of the warning horn above and below 45 mph. Other examples include an over-speed warning, where a driver may set the desired maximum speed and have an audible

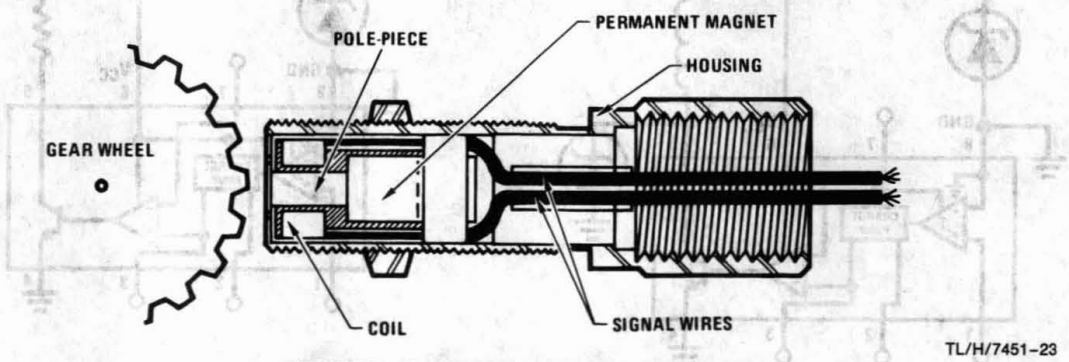

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FIGURE 8. Typical Magnetic Pickup

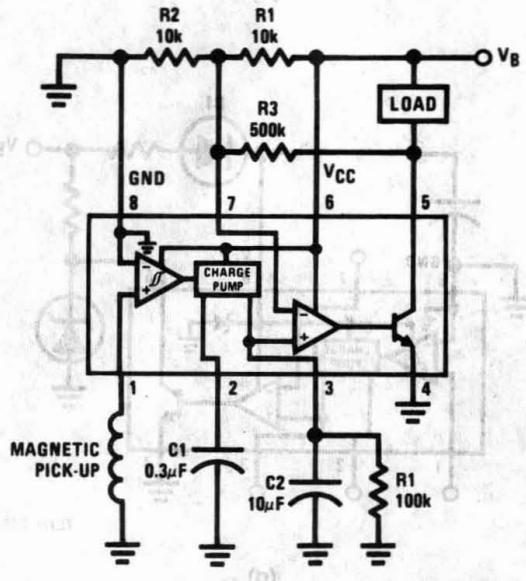

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FIGURE 9. Simple Speed Switch Load is Energized

$$\text{when } f_{IN} > \frac{1}{2C1R1}$$

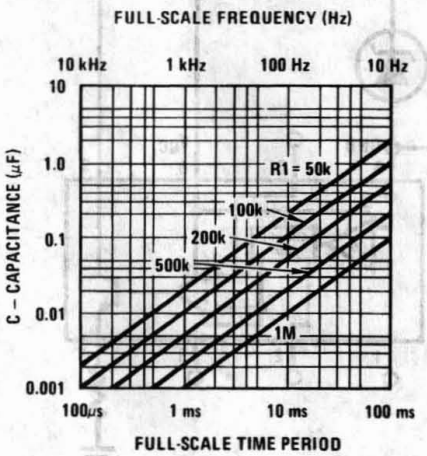

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FIGURE 10. RC Selection Chart

or visual warning of speeds in excess of that level. Many anti-pollution devices included on several recent automobile models have included a speed switch to disable the vacuum advance function until a certain speed is attained[2]. A circuit which will perform these kind of functions is shown in *Figure 9.* A typical magnetic pickup for automotive applications will provide a thousand pulses per mile so that at 60 mph the incoming frequency will be 16.6 Hz. If the reference level on the comparator is set by two equal resistors R1 and R2 then the desired value of C1 and R1 can be determined from the simple relationship:

$$\frac{V_{CC}}{2} = V_{CC} \bullet C1 \bullet R1 \bullet f.$$

or $C1R1f = 0.5$

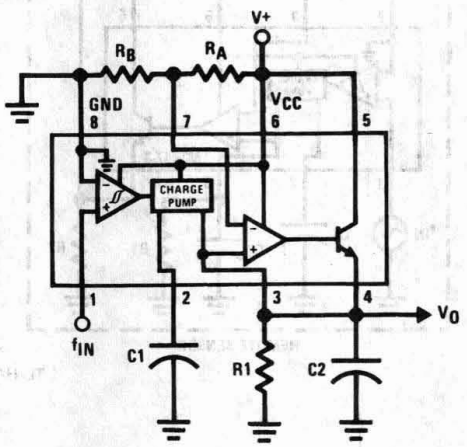
and hence $C1R1 = 0.03$

From the RC selection chart in *Figure 10* we can choose suitable values for R1 and C1. Examples are 100 kΩ and 0.3 μF. The circuit will then switch at approximately 60 mph with the stated input frequency relationship to speed. To determine the ripple voltage refer back to the equation for ripple voltage (under "Choosing R1, C1 and C2"). From this we can determine that there will be about 10 mV of ripple at the switching level. To prevent this from causing chattering of the load a certain amount of hysteresis is added by including R3. This will provide typically 1% of supply as a hysteresis or 1.2 mph in the example. Note that since the reference to the comparator is a function of supply voltage as is the output from the charge pump there is no need to regulate the power supply. The frequency at which switching occurs is independent of supply voltage.

In some industrial applications it is useful to have an indication of past speed excesses, for example in notifying the need for checking of bearings. The LM2907 can be made to latch until the power supply is turned "OFF" in the case where the frequency exceeds a certain limit, by simply connecting the output transistor emitter back to the non-inverting input of the comparator as shown in *Figure 11.* It can also serve to shut off a tape recorder or editing machine at the end of a rewind cycle. When the speed suddenly increases, the device will sense the condition and shut down the motor.

Analog Displays

The LM2907, LM2917 series devices are particularly useful for analog display of frequency inputs. In situations where the display device is a moving coil instrument the advantages of the uncommitted output transistor can be realized by providing a current drive to the meter. This avoids temperature tracking problems with the varying meter resistance and enables high resistance instruments to be driven accurately with relatively large voltages as illustrated in *Figure 12.* The LM2917 version is employed here to provide a regulated current to the instrument. The onboard 7.6V zener is compatible with car and boat batteries and enables the moving coil instrument to employ the full battery voltage for its deflection. This enables high torque meters to be used. This is particularly useful in high vibration environments such as boats and motorcycles. In the case of boats, the most common speed pickup for the knot meter employs a rotating propeller driving a magnetic pickup device. Meteorologists employ a large number of anemometers for measuring wind velocities and these are frequently coupled by a magnetic pickup. In examples like these, where there is frequently a large distance between the display device and the sensor, the configuration of *Figure 13* can be usefully employed to cut down on the number of wires needed. Here the output current is conducted along the supply line so that a local current sensing device in the supply line can be used to get a direct reading of the frequency at the remote location where the electronics may also be situated. The small zero speed offset due to the device quiescent current may be compensated by offsetting the zero on the display device. This also permits one display device to be shared between several inputs.



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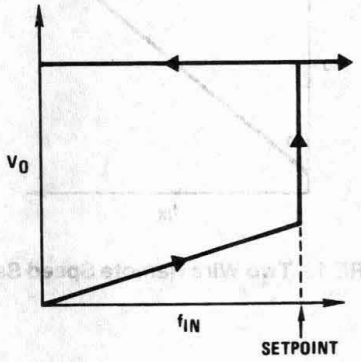

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$$V_O = F_{IN}V + R1\,C1$$

$$SETPOINT = V + \frac{RB}{RD + RA}$$

Latchup occurs when

$$F_{IN} = \frac{RB}{RA + RB}\,\frac{1}{R1\,C1}$$

Independent of V + !

FIGURE 11. Overspeed Latch

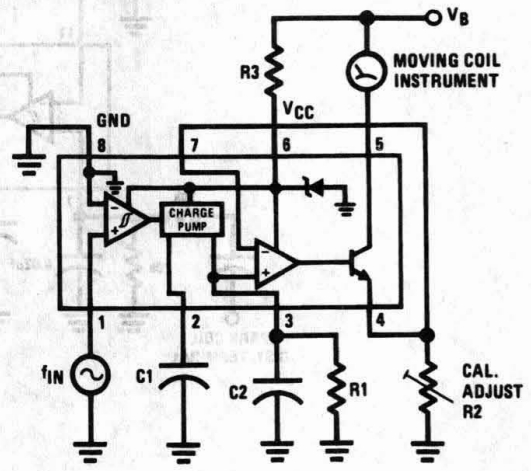

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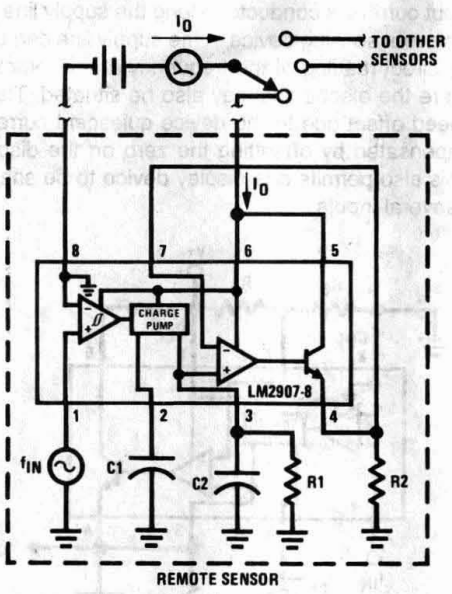
FIGURE 12. Analog Display of Frequency



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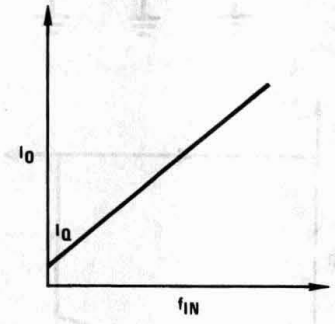

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FIGURE 13. Two Wire Remote Speed Sensor

Automotive Tachometer

Not all inputs are derived from variable reluctance magnetic pickups; for example, in spark ignition engines the tachometer is generally driven from the spark coil. An interface circuit for this situation is shown in *Figure 14.* This tachometer can be set up for any number of cylinders by linking the appropriate timing resistor as illustrated. A 500Ω trim resistor can be used to set up final calibration. A protection circuit composed of a 10Ω resistor and a zener diode is also shown as a safety precaution against the transients which are to be found in automobiles.

Motor Speed Controls

DC motors with or without brushes can be purchased with ac tachometer outputs already provided by the manufacturer[3]. With these motors in combination with the

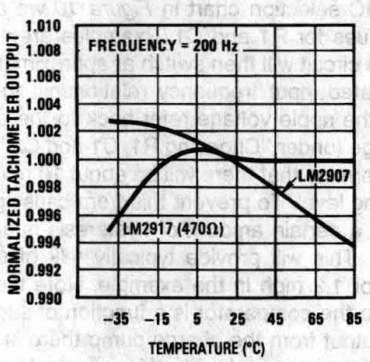

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FIGURE 15. Normalized Tachometer Output vs. Temperature

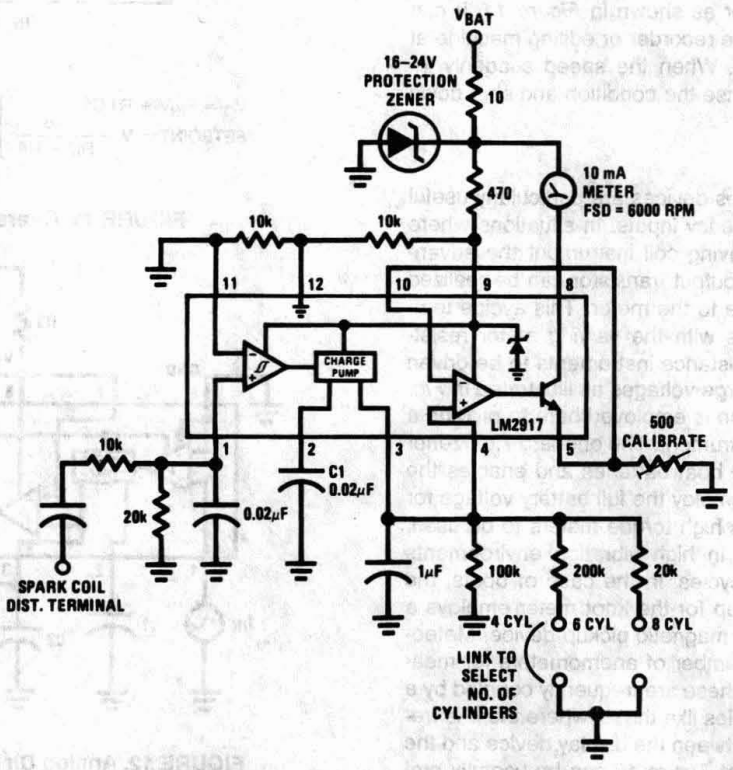

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FIGURE 14. Gasoline Engine Tachometer

LM2907, a very low cost speed control can be constructed. In *Figure 16* the most simple version is illustrated where the tachometer drives the non-inverting input of the comparator up towards the preset reference level. When that level is reached, the output is turned off and the power is removed from the motor. As the motor slows down, the voltage from the charge pump output falls and power is restored. Thus speed is maintained by operating the motor in a switching mode. Hysteresis can be provided to control the rate of switching. An alternative approach which gives proportional control is shown in *Figure 17.* Here the charge pump integrator is shown in a feedback connection around the operational amplifier. The output voltage for zero speed is equal to the reference voltage set up on the potentiometer on the non-inverting input. As speed increases, the charge pump puts charge into capacitor C2 and causes the output V_{OUT} to fall in proportion to speed. The output current of the op amp transistor is used to provide an analog drive to the motor. Thus as the motor speed approaches the reference level, the current is proportionately reduced to the motor so that the motor gradually comes up to speed and is maintained without operating the motor in a switching mode. This is particularly useful in situations where the electrical noise generated by the switching mode operation is objectionable. This circuit has one primary disadvantage in that it has poor load regulation. A third configuration is shown in *Figure 18.* This employs an LM2907-8 acting as a shunt mode regulator. It also features an LED to indicate when the device is in regulation.

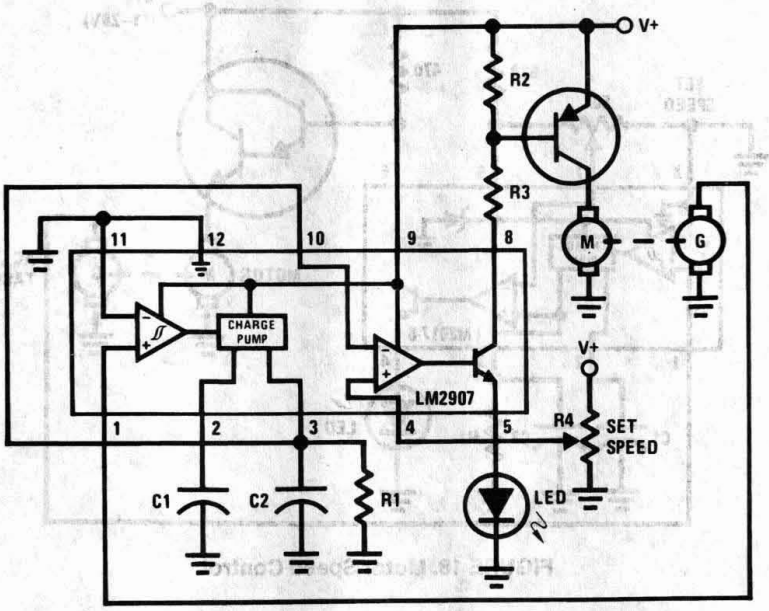

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FIGURE 16. Motor Speed Control

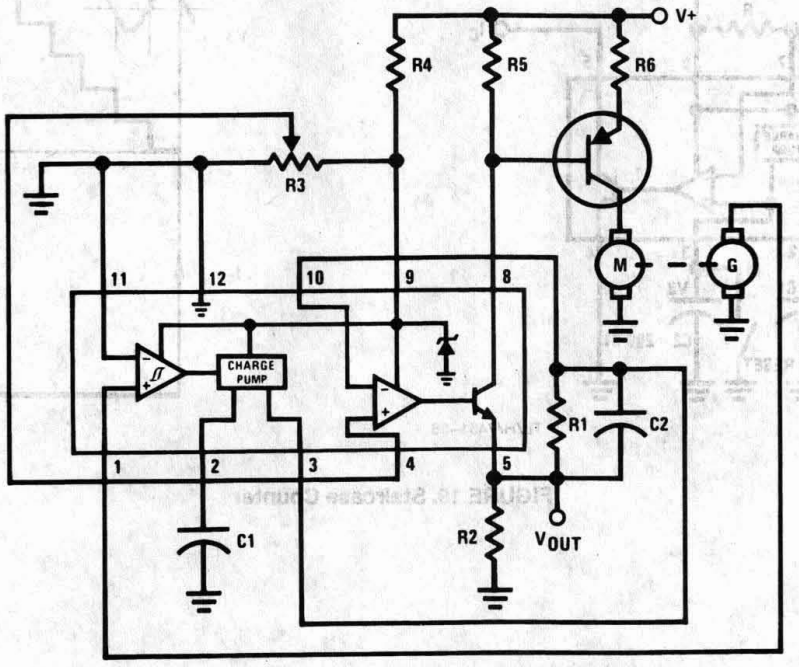

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FIGURE 17. Motor Speed Control with Proportional Drive

Position Sensing

In addition to their use to complete tachometer feedback loops, used in position transducer circuits, the LM2907, LM2917 devices can also be used as position transducers. For example, the timing resistor can be removed from pin 3 so that the output current produces a staircase instead of a fixed dc level. If the magnetic pickup senses passing notches or items, a staircase signal is generated which can then be compared with a reference to initiate a switching action when a specified count is reached. For example, *Figure 19* shows a circuit which will count up a hundred input pulses and then switch on the output stage. Examples of this application can be found in automated packaging operations or in line printers.

The output of the tachometer is proportional to the product of supply voltage, input frequency, a capacitor and a resistor. Any one of these may be used as the input variable or they may be used in combination to produce multiplication. An example of a capacitive transducer is illustrated in *Figure 20,* where a fixed input frequency is employed either from the 60 Hz line as a convenient source or from a stable oscillator. The capacitor is a variable element mechanically coupled to the system whose position is to be sensed. The output is proportional to the capacitance value, which can be arranged to have any desired relationship to the mechanical input by suitable shaping of the capacitor electrodes.

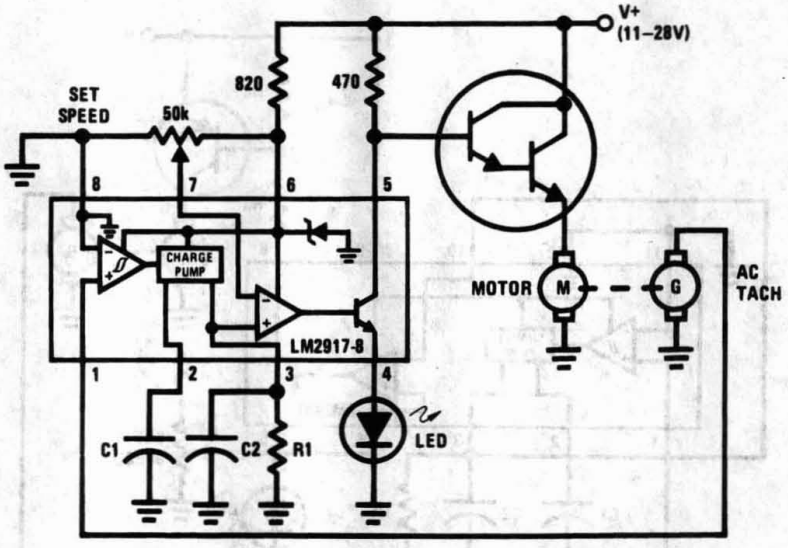

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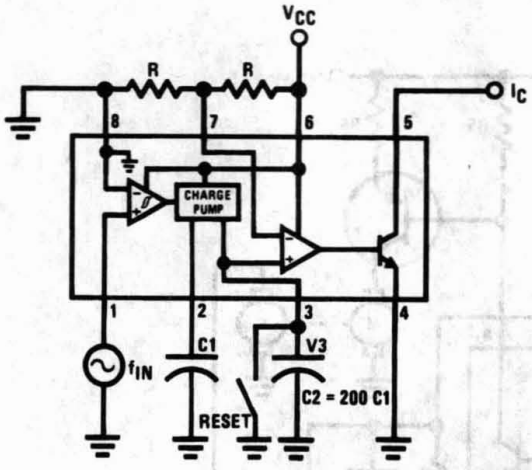
FIGURE 18. Motor Speed Control



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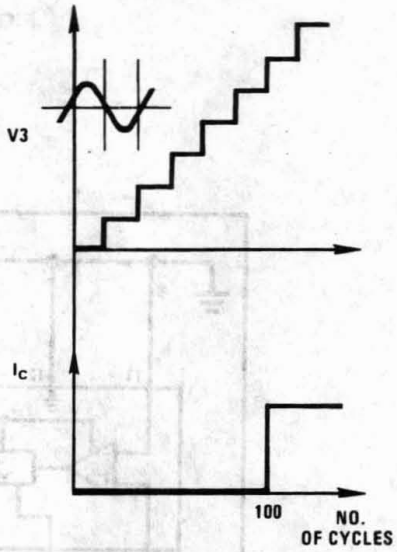

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FIGURE 19. Staircase Counter

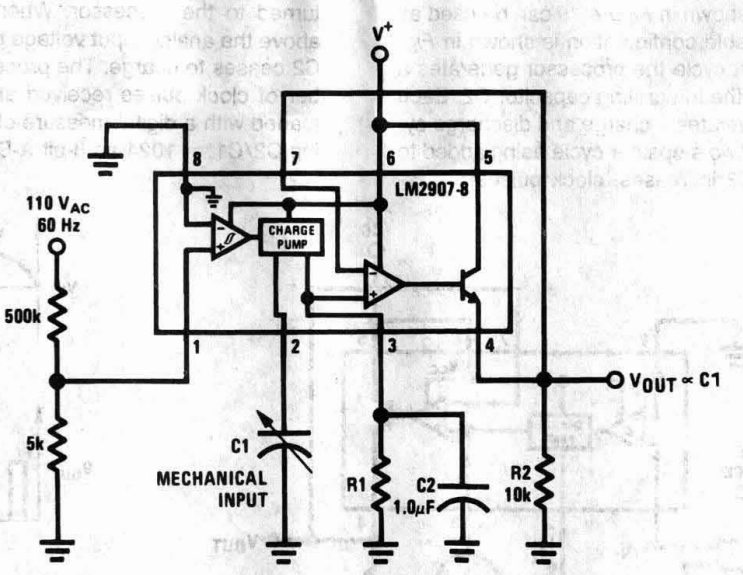

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FIGURE 20. Capacitive Transducer

Analog Systems Building Block

The LM2907, LM2917 series characterize systems building block applications by the feature that the output from the device is proportional only to externally programmed inputs. Any or all of these inputs may be controlled inputs to provide the desired output. For example, in *Figure 20* the capacitance transducer can be operated as a multiplier. In flow measurement indicators, the input frequency can be a variable depending on the flow rate, such as a signal generated from a paddle wheel, propeller or vortex sensor[4]. The capacitor can be an indication of orifice size or aperture size, such as in a throttle body. The product of these two will indicate volume flow. A thermistor could be added to R1 to convert the volume flow to mass flow. So a combination of these inputs, including control voltage on the supply, can be used to provide complex multiplicative analog functions with independent control of the variables.

Phase-locked loops (PLL) are popular today now that low cost monolithic implementations are available off the shelf. One of their limitations is the narrow capture range and hold-in range. The LM2907 can be employed as a PLL helper. The configuration is shown in *Figure 21.* The LM2907 here serves the function of a frequency-to-voltage converter which puts the VCO initially at approximately the right frequency to match the input frequency. The phase detector is then used to close the gap between VCO and input frequency by exerting a control on the summing point. In this way, given proper tracking between the frequency-to-voltage converter and the VCO, (which is a voltage-to-frequency converter), a wide-range phase loop can be developed.

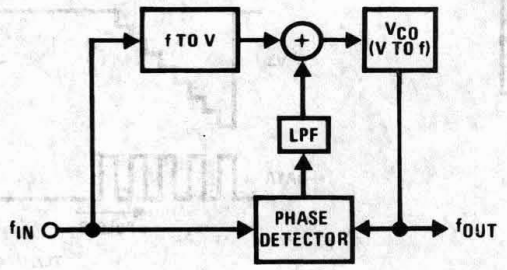

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FIGURE 21. Phase-Locked Loop Helper Added f to V Greatly Increases Capture and Hold Range

The linearity of voltage controlled oscillators can be improved by employing the LM2907 as a feedback control element converting the frequency back to voltage and comparing with the input voltage. This can often be a lower cost solution to linearizing the VCO than by working directly on the VCO itself in the open loop mode. The arrangement is illustrated in *Figure 22.*

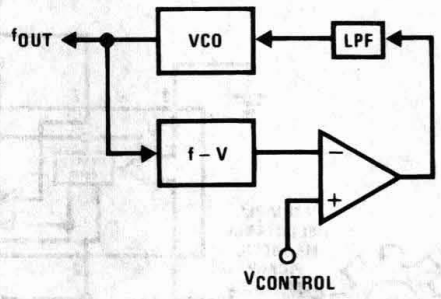

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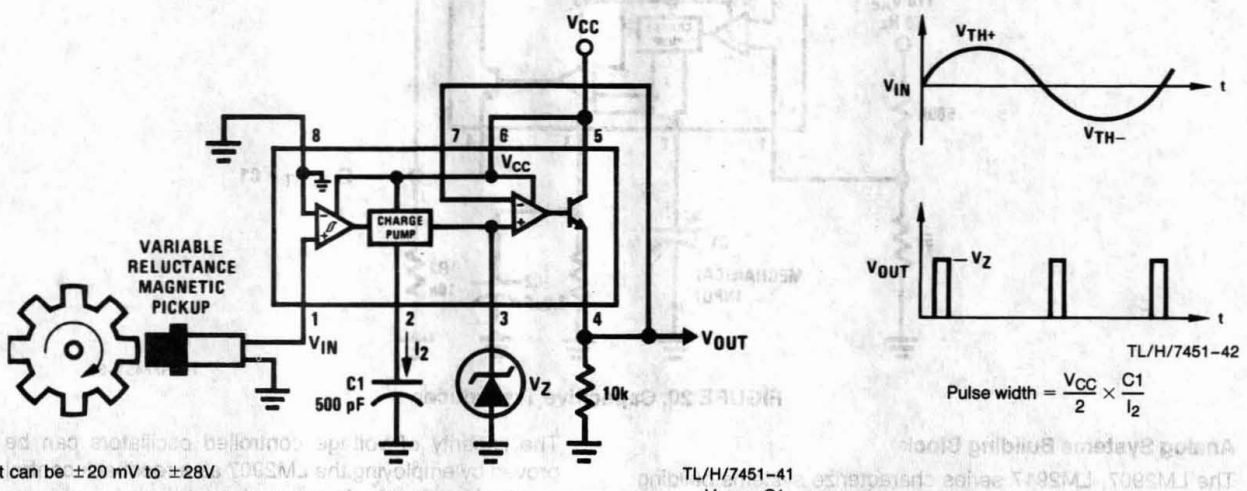
FIGURE 22. Feedback Controlled VCO

Digital Interface

A growing proportion of the complex control systems today are being controlled by microprocessors and other digital devices. Frequently they require inputs to indicate position or time from some mechanical input. The LM2907 can be used to provide zero crossing datum to a digital system using the circuits illustrated in *Figure 23.* At each zero crossing of the input signal the charge pump changes the state of capacitor C1 and provides a one-shot pulse into the zener diode at pin 3. The width of this pulse is controlled by the internal current of pin 2 and the size of capacitor C1 as well as by the supply voltage. Since a pulse is generated by each zero crossing of the input signal we call this a "two-shot" instead of a "one-shot" device and this can be used for doubling the frequency that is presented to the microprocessor control system. If frequency doubling is not required and a square wave output is preferred, the circuit of *Figure 24* can be employed. In this case, the output swing is the same as the swing on pin 2 which is a swing of half supply voltage starting at 1 V_{BE} below one quarter of supply and going to 1 V_{BE} below three-quarters of supply. This can be increased up to the full output swing capability by reducing or removing the negative feedback around the op amp.

The staircase generator shown in *Figure 19* can be used as an A-D converter. A suitable configuration is shown in *Figure 25.* To start a convert cycle the processor generates a reset pulse to discharge the integrating capacitor C2. Each complete clock cycle generates a charge and discharge cycle on C1. This results in two steps per cycle being added to C2. As the voltage on C2 increases, clock pulses are returned to the processor. When the voltage on C2 steps above the analog input voltage the data line is clamped and C2 ceases to charge. The processor, by counting the number of clock pulses received after the reset pulse, is thus loaded with a digital measure of the input voltage. By making C2/C1 = 1024 an 8-bit A-D is obtained.



Input can be ±20 mV to ±28V

Output frequency equal twice input frequency.

$$\text{Pulse width} = \frac{V_{CC}}{2} \times \frac{C1}{I_2}$$

$$\text{Pulse height} = V_{ZENER}$$

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FIGURE 23. "Two-Shot" Zero Crossing Detector

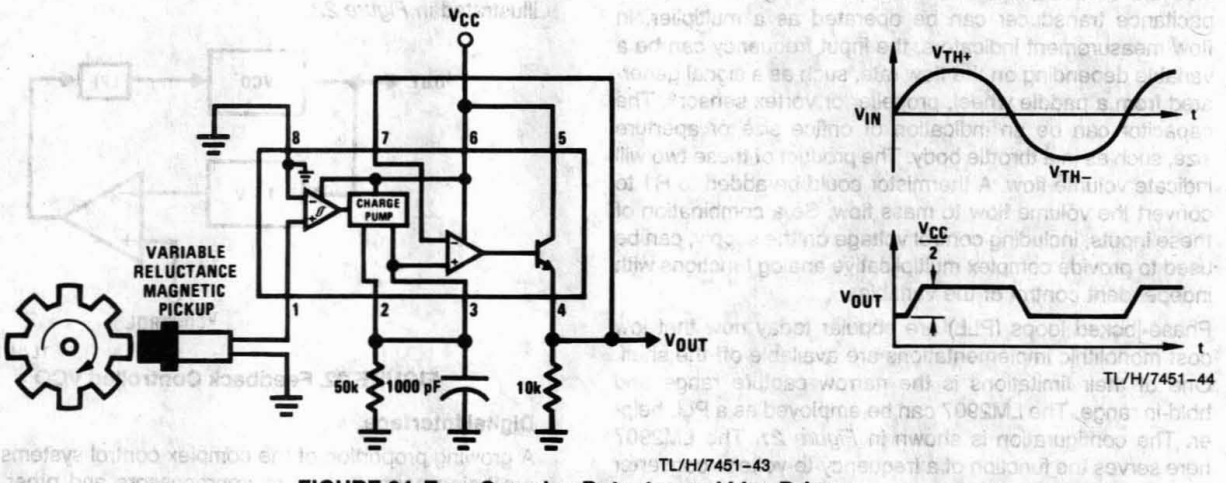


FIGURE 24. Zero Crossing Detector and Line Drivers

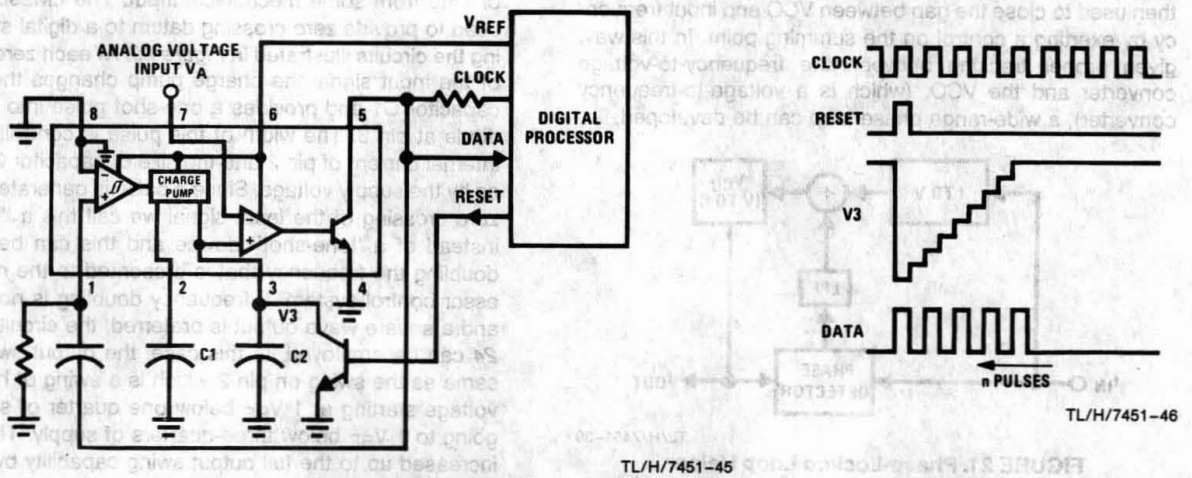
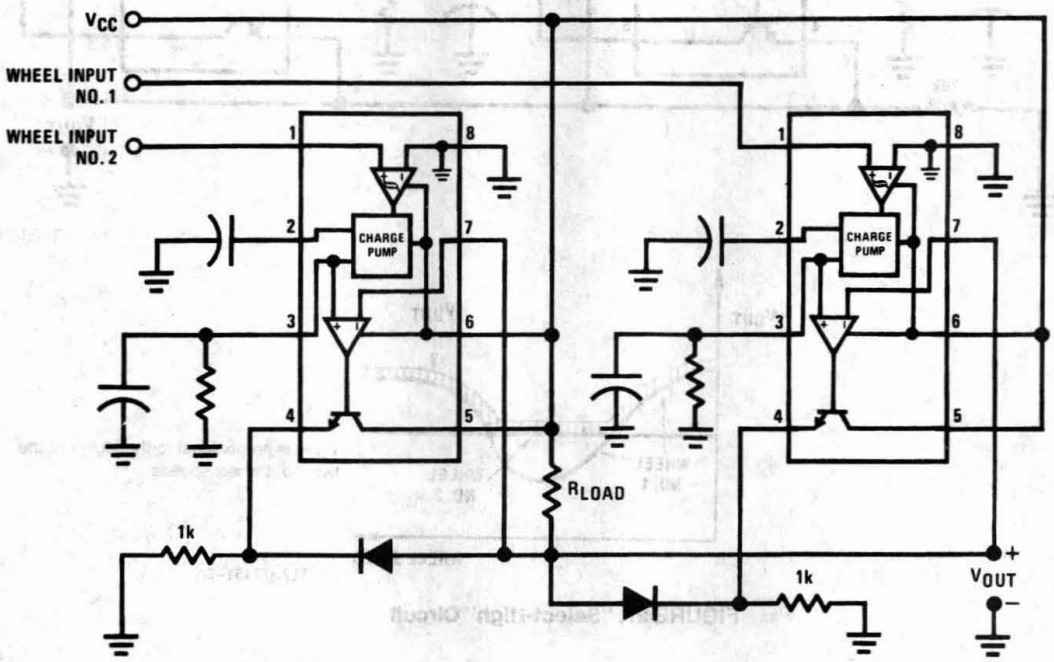


FIGURE 25. A-D Converter

Anti-Skid Circuit Functions

Motor Vehicle Standards 121 place certain stopping requirements on heavy vehicles which require the use of electronic anti-skid control devices.[5] These devices generally use variable reluctance magnetic pickup sensors on the wheels to provide inputs to a control module. One of the questions which the systems designer must answer is whether to use the average from each of the two wheels on a given axle or to use the lower of the two speeds or to use the higher of the two speeds. Each of the three functions can be generated by a single pair of LM2907-8 as illustrated in *Figures 26–28.* In *Figure 26* the input frequency from each wheel sensor is converted to a voltage in the normal manner. The op amp/comparator is connected with negative feedback with a diode in the loop so that the amplifier can only pull down on the load and not pull up. In this way, the outputs from the two devices can be joined together and the output will be the lower of the two input speeds. In *Figure 27* the output emitter of the onboard op amp provides the pullup required to provide a select-high situation where the output is equal to the higher of two speeds. The select average circuit in *Figure 28* saves components by allowing the two charge pumps to operate into a single RC network. One of the amplifiers is needed then to buffer the output and provide a low impedance output which is the average of the two input frequencies. The second amplifier is available for other applications.



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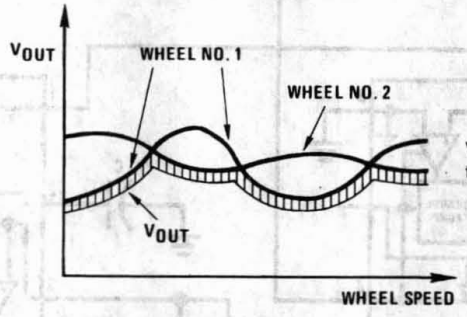

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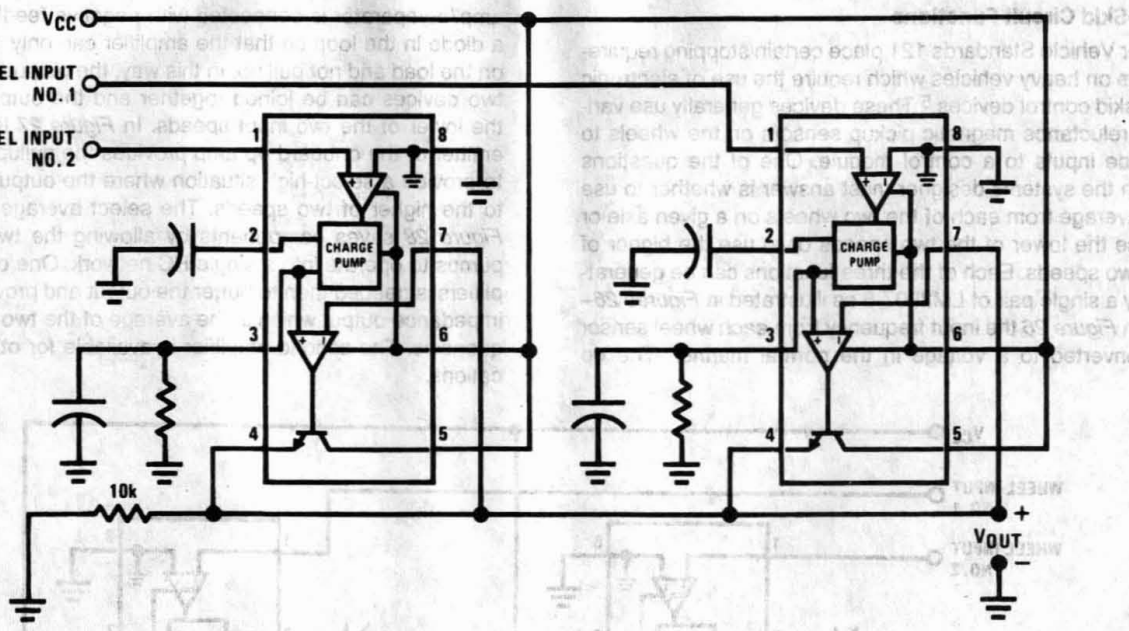
FIGURE 26. "Select-Low" Circuit



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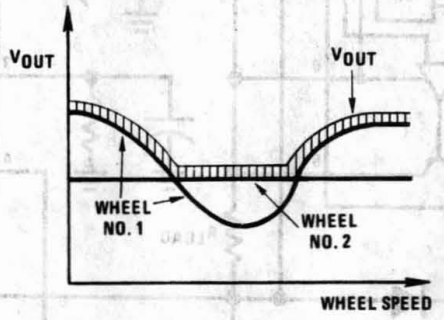

VOUT is proportional to the higher of the two input wheel speeds

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FIGURE 27. "Select-High" Circuit

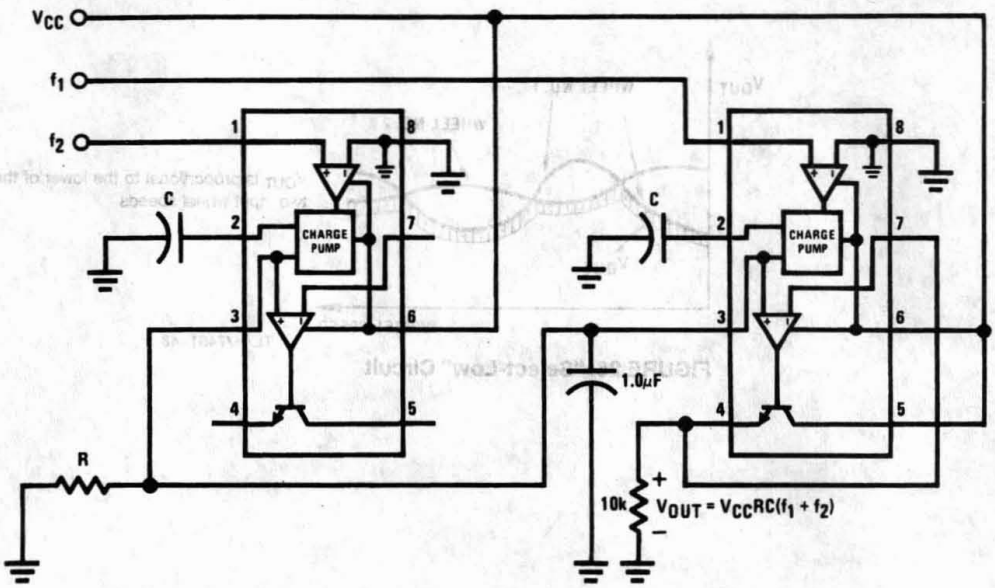

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FIGURE 28. "Select-Average" Circuit

Transmission and Clutch Control Functions

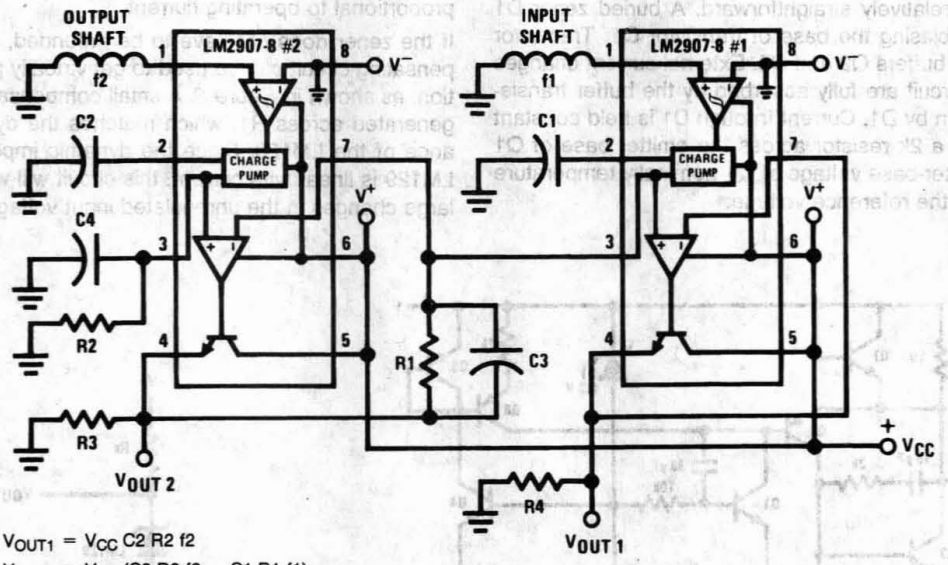
Electric clutches can be added to automotive transmissions to eliminate the 6% slip which typically occurs during cruise and which results in a 6% loss in fuel economy. These devices could be operated by a pair of LM2907's as illustrated in *Figure 29.* Magnetic pickups are connected to input and output shafts of the transmission respectively and provide frequency inputs f_1 and f_2 to the circuit. Frequency, f_2, being the output shaft speed, is also a measure of vehicle road speed. Thus the LM2907-8 No. 2 provides a voltage proportional to road speed at pin 3. This is buffered by the op amp in LM2907-8 No. 1 to provide a speed output V_{OUT1} on pin 4. The input shaft provides charge pulses at the rate of $2f_1$ into the inverting node of op amp 2. This node has the integrating network R1, C3 going back to the output of the op amp so that the charge pulses are integrated and provide an inverted output voltage proportional to the input speed. Thus the output V_{OUT2} is proportional to the difference between the two input frequencies. With these two signals—the road speed and the difference between road speed and input shaft speed—it is possible to develop a number of control functions including the electronic clutch and a complete electronic transmission control. (In the configuration shown, it is not possible for V_{OUT2} to go below zero so that there is a limitation to the output swing in this direction. This may be overcome by returning R3 to a negative bias supply instead of to ground.)

CONCLUSION

The applications presented in this note indicate that the LM2907, LM2917 series devices offer a wide variety of uses ranging from very simple low cost frequency to voltage conversion to complex systems building blocks. It is hoped that the ideas contained here have given suggestions which may help provide new solutions to old problems. Additional applications ideas are included in the data sheet, which should be referred to for all specifications and characteristics.

REFERENCES

1. Sociey of Automotive Engineers: Preliminary Recommended Environmental Practices for Electronic Equipment Design. October 1974.
2. See for example: Pollution Control Installers Handbook—California Bureau of Automotive Repair No. BAR H-001 § 5.5.4 NOX control systems.
3. TRW Globe Motors, 2275 Stanley Avenue, Dayton, Ohio 45404.
4. S.A.E. Paper #760018 Air Flow Measurement for Engine Control—Robert D. Joy.
5. Code of Federal Regulations. Title 49 Transportation; Chapter V—National Highway Traffic Safety Administration, Dept. of Transportation; Part 571—Federal Motor Vehicle Safety Standards; Standard No. 121.



$V_{OUT1} = V_{CC}\ C2\ R2\ f2$

$V_{OUT2} = V_{CC}\ (C2\ R2\ f2 - C1\ R1\ f1)$

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FIGURE 29. Transmission or Clutch Control Functions

IC Zener Eases Reference Design

National Semiconductor
Application Note 173

DESCRIPTION

A new IC zener with low dynamic impedance and wide operating current range significantly simplifies reference or regulator circuit design. The low dynamic impedance provides better regulation against operating current changes, easing the requirements of the biasing supply. Further, the temperature coefficient is independent of operating current, so that the LM129 can be used at any convenient current level. Other characteristics such as temperature coefficient, noise and long term stability are equal to or better than good quality discrete zeners.

The LM129 uses a new subsurface breakdown IC zener combined with a buffer circuit to lower dynamic impedance. The new subsurface zener has low noise and excellent long term stability since the breakdown is in the bulk of the silicon. Circuitry around the zener supplies internal biasing currents and buffers external current changes from the zener. The overall breakdown is about 6.9V with devices selected for temperature coefficients.

The zener is relatively straightforward. A buried zener D1 breaks down biasing the base of transistor Q1. Transistor Q1 drives two buffers Q2 and Q3. External current changes through the circuit are fully absorbed by the buffer transistors rather than by D1. Current through D1 is held constant at 250 μA by a 2k resistor across the emitter base of Q1 while the emitter-base voltage of Q1 nominally temperature compensates the reference voltage.

The other components, Q4, Q5 and Q6, set the operating current of Q1. Frequency compensation is accomplished with two junction capacitors.

All that is needed for biasing in most applications is a resistor as shown in *Figure 2*. Biasing current can be anywhere from 0.6 mA to 15 mA with little change in performance. Optimally, however, the biasing current should be as low as possible for the best regulation. The dynamic impedance of the LM129 is about 1 Ω and is independent of current. Therefore, the regulation of the LM129 against voltage changes is 1/Rs.

Lower currents or higher Rs give better regulation. For example, with a 15V supply and 1 mA operating current, the reference change for a 10% change in the 15V supply is 180 μV. If the LM129 is run at 5 mA, the change is 900 μV or 5 times worse. By comparison, a standard IN821 zener will change about 17 mV. All discrete zeners have about the same regulation since their dynamic impedance is inversely proportional to operating current.

If the zener does not have to be grounded, a bridge compensating circuit can be used to get virtually perfect regulation, as shown in *Figure 3*. A small compensating voltage is generated across R1, which matches the dynamic impedance of the LM129. Since the dynamic impedance of the LM129 is linear with current, this circuit will work even with large changes in the unregulated input voltage.

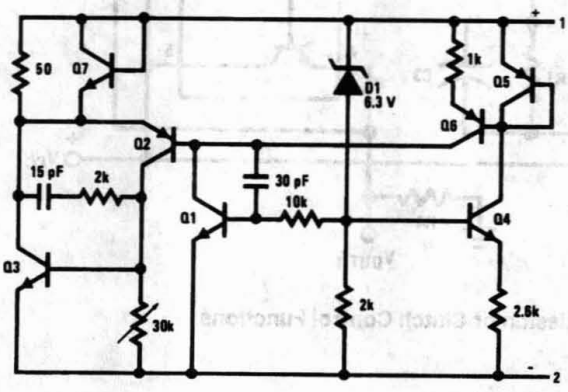

FIGURE 1. IC Reference Zener

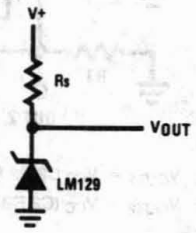

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FIGURE 2. Basic Biasing

Other output voltages are easily obtained with the simple op-amp circuit shown in *Figure 4*. A simple non-inverting amplifier is used to boost and buffer the zener to 10V. The reference is run directly from the input power rather than the output of the op-amp. When the zener is powered from the op-amp, special starting circuitry is sometimes necessary to insure the output comes up in the right polarity. For outputs lower than the breakdown of the LM129 a divider can be connected across the zener to drive the op-amp.

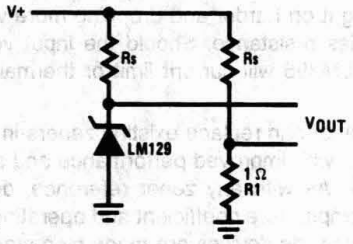

FIGURE 3. Bridge Compensation for Line Changes

An AC square wave or bipolarity output reference can easily be made with an op-amp and FET switch as shown in *Figure 5*. When Q1 is "ON", the LM108 functions as a normal inverting op-amp with a gain of −1 and an output of −6.9V. With Q1 "OFF" the op-amp acts as a giving 6.9 V at the output. Some non-symmetry will occur from loading change on the LM129 in the different states and mismatch of R1 and R2. Trimming either R1 or R2 can make the output exactly symmetrical around ground.

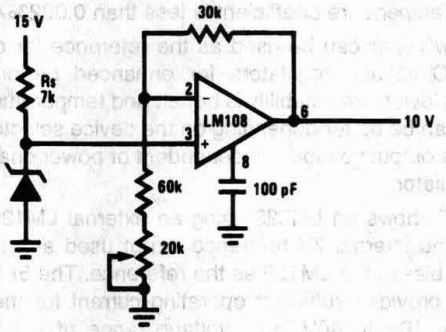

FIGURE 4. 10 Volt Buffered Output Reference

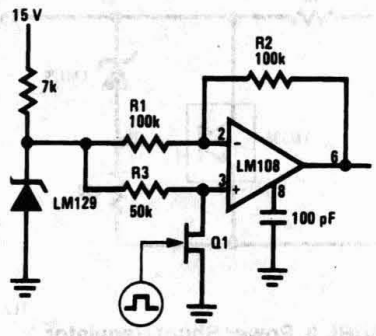

FIGURE 5. Bipolar Output Reference

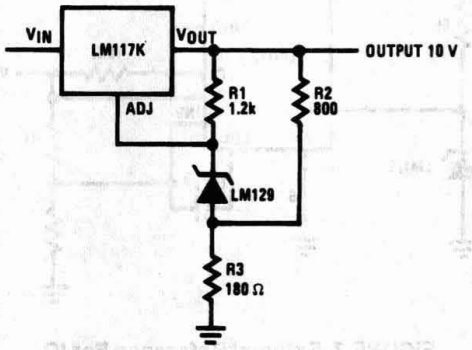

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FIGURE 6. High Stability 10 V Regulator

By combining the LM129 with an LM117 three-terminal regulator a high stability power regulator can be made. This is shown in *Figure 6*. Resistor R1 biases the LM129 at about 1 mA from the 1.25V reference in the LM117. The voltage of the LM129 is added to the 1.25V of the LM117 to make a total reference voltage of 8.1V. The output voltage is then set at 10V by R2 and R3. Since the internal reference of the LM117 contributes only about 20% of the total reference voltage, regulation and drift are essentially those of the external zener. The regulator has 0.2% load and line regulation and if a low drift zener such as the LM129A is used overall temperature coefficient is less than 0.002%/°C.

The new zener can be used as the reference for conventional IC voltage regulators for enhanced performance. Noise is lower, time stability is better, and temperature coefficient can be better depending on the device selected. Further, the output voltage is independent of power changes in the regulator.

Figure 7 shows an LM723 using an external LM129 reference. The internal 7V reference is not used and a single resistor biases the LM129 as the reference. The 5k resistor chosen provides sufficient operating current for the zener over the 10V to 40V input voltage range of the LM723. Since the dynamic impedance of the LM129 is so low, the reference regulation against line changes is only 0.02%/V. This is small compared to the regulation of 0.1%/V for the LM723; however, the resistor can be replaced by a 1 mA to 5 mA FET used as a constant current source for improved regulation. When the FET is used reference regulation is easily 0.001%/V. Output voltage is set in the standard manner except that for low output voltages sufficient current must be run through the zener to power the voltage divider supplying the reference to the LM723.

An overload protected power shunt regulator is shown in *Figure 8*. The output voltage is about 7.8V — the 7V breakdown of the LM129 plus the 0.8V emitter-base voltage of the LM395. The LM395 is an IC, 1.5 A power transistor with complete overload protection on the chip. Included on the chip are current limiting and thermal limiting, making the device virtually blowout-proof. Further, the base current is only 5 μA, making it easy to drive as a shunt regulator. As the input voltage rises, more drive is applied to the base of the LM395, turning it on harder and dropping more voltage across the series resistance. Should the input voltage rise too high, the LM395 will current limit or thermal limit, protecting itself.

The new IC zener can replace existing zeners in just about any application with improved performance and simpler external circuitry. As with any zener reference, devices are selected for temperature coefficient and operating temperature range. Since the devices are made by a standard integrated circuit process, cost is low and good reproducibility is obtained in volume production.

Finally, since the device is actually an IC, it is packaged in a rugged TO-46 metal can package or a 3-lead plastic transistor package.

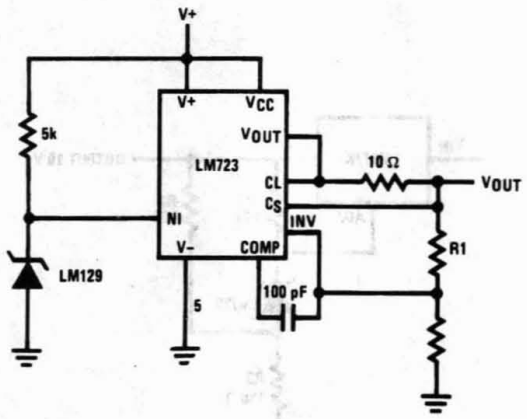
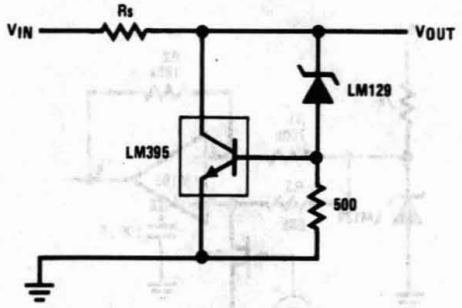


FIGURE 7. External Reference For IC



TL/H/5614–3

FIGURE 8. Power Shunt Regulator

Applications for an Adjustable IC Power Regulator

National Semiconductor
Application Note 178

A new 3-terminal adjustable IC power regulator solves many of the problems associated with older, fixed regulators. The LM117, a 1.5A IC regulator is adjustable from 1.2V to 40V with only 2 external resistors. Further, improvements are made in performance over older regulators. Load and line regulation are a factor of 10 better than previous regulators. Input voltage range is increased to 40V and output characteristics are fully specified for load of 1.5A. Reliability is improved by new overload protection circuitry as well as *100% burn-in* of all parts. The table below summarizes the typical performance of the LM117.

TABLE I

Output Voltage Range	1.25V–40V
Line Regulation	0.01%/V
Load Regulation I_L = 1.5A	0.1%
Reference Voltage	1.25V
Adjustment Pin Currrent	50 μA
Minimum Load Current (Quiescent Current)	3.5 mA
Temperature Stability	0.01%/°C
Current Limit	2.2A
Ripple Rejection	80 dB

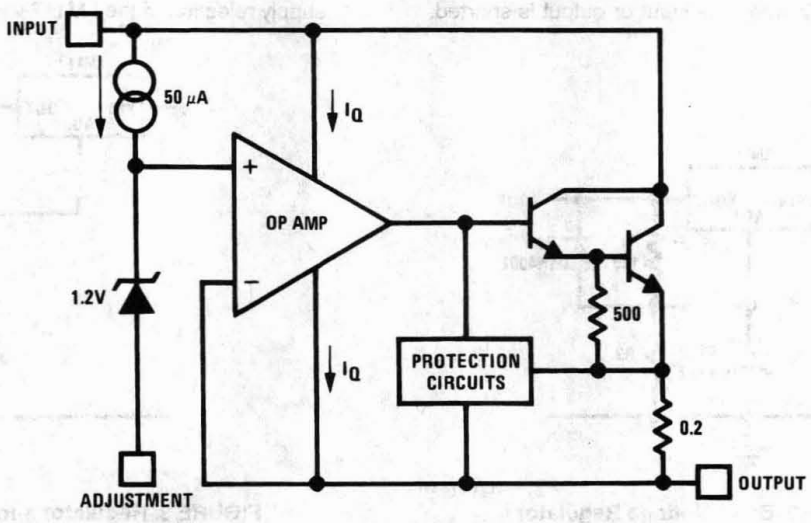
The overload protection circuitry on the LM117 includes current limiting, safe-area protection for the internal power transistor and thermal limiting. The current limit is set at 2.2A and, unlike presently available positive regulators, remains relatively constant with temperature. Over a −55°C to +150°C temperature range, the current limit only shifts about 10%.

At high input-to-output voltage differentials the safe-area protection decreases the current limit. With the LM117, full output current is available to 15V differential and, even at 40V, about 400 mA is available. With some regulators, the output will shut completely off when the input-to-output differential goes above 30V, possibly causing start-up problems. Finally, the thermal limiting is always active and will protect the device even if the adjustment terminal should become accidentally disconnected.

Since the LM117 is a floating voltage regulator, it sees only the input-to-output voltage differential. This is of benefit, especially at high output voltage. For example, a 30V regulator nominally operating with a 38V input can have 70V input transient before the 40V input-to-output rating of the LM117 is exceeded.

BASIC OPERATION

The operation of how a 3-terminal regulator is adjusted can be easily understood by referring to *Figure 1*, which shows a functional circuit. An op amp, connected as a unity gain buffer, drives a power Darlington. The op amp and biasing circuitry for the regulator is arranged so that all the quiescent current is delivered to the regulator output (rather than ground) eliminating the need for a separate ground terminal. Further, all the circuitry is designed to operate over the 2V to 40V input-to-output differential of the regulator.



TL/H/7334–1

FIGURE 1. Functional Schematic of the LM117

A 1.2V reference voltage appears inserted between the non-inverting input of the op amp and the adjustment terminal. About 50 μA is needed to bias the reference and this current comes out of the adjustment terminal. In operation, the output of the regulator is the voltage of the adjustment terminal plus 1.2V. If the adjustment terminal is grounded, the device acts as a 1.2V regulator. For higher output voltages, a divider R1 and R2 is connected from the output to ground as is shown in *Figure 2*. The 1.2V reference across resistor R1 forces 10 mA of current to flow. This 10 mA then flows through R2, increasing the voltage at the adjustment terminal and therefore the output voltage. The output voltage is given by:

$$V_{OUT} = 1.2V \times \left(1 + \frac{R2}{R1}\right) + 50\ \mu A\ R2$$

The 50 μA biasing current is small compared to 5 mA and causes only a small error in actual output voltages. Further, it is extremely well regulated against line voltage or load current changes so that it contributes virtually no error to dynamic regulation. Of course, programming currents other than 10 mA can be used depending upon the application.

Since the regulator is floating, all the quiescent current must be absorbed by the load. With too light of a load, regulation is impaired. Usually, a 5 mA programming current is sufficient; however, worst case minimum load for commercial grade parts requires a minimum load of 10 mA. The minimum load current can be compared to the quiescent current of standard regulators.

APPLICATIONS

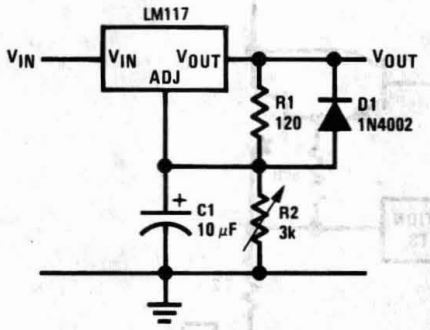
An adjustable lab regulator using the LM117 is shown in *Figure 2* and has a 1.2V to 25V output range. A 10 mA program current is set by R1 while the output voltage is set by R2. Capacitor C1 is optional to improve ripple rejection so that 80 dB is obtained at any output voltage. The diode, although not necessary in this circuit since the output is limited to 25V, is needed with outputs over 25V to protect against the capacitors discharging through low current nodes in the LM117 when the input or output is shorted.

The programming current is constant and can be used to bias other circuitry, while the regulator is used as the power supply for the system. In *Figure 3*, the LM117 is used as a 15V regulator while the programming current powers an LM127 zener reference. The LM129 is an IC zener with less than 1Ω dynamic impedance and can operate over a range of 0.5 mA to 15 mA with virtually no change in performance.

Another example of using the programming current is shown in *Figure 4* where the output setting resistor is tapped to provide multiple output voltage to op amp buffers. An additional transistor is included as part of the overload protection. When any of the outputs are shorted, the op amp will current limit and a voltage will be developed across its inputs. This will turn "ON" the transistor and pull down the adjustment terminal of the LM117, causing all outputs to decrease, minimizing possible damage to the rest of the circuitry.

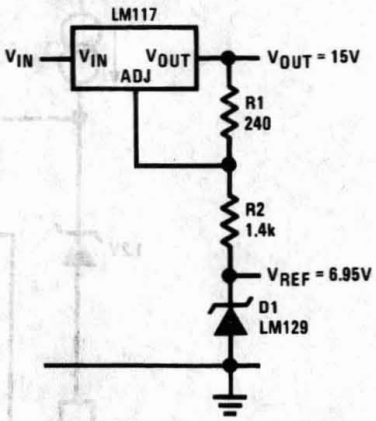
Ordinary 3-terminal regulators are not especially attractive for use as precision current regulators. Firstly, the quiescent current can be as high as 10 mA, giving at least 1% error at 1A output currents, and more error at lower currents. Secondly, at least 7V is needed to operate the device. With the LM117, the only error current is 50 μA from the adjustment terminal, and only 4.2V is needed for operation at 1.5A or 3.2V at 0.5A. A simple 2-terminal current regulator is shown in *Figure 5* and is usable anywhere from 10 mA to 1.5A.

Figure 6 shows an adjustable current regulator in conjunction with the voltage regulator from *Figure 2* to make constant voltage/constant current lab-type supply. Current sensing is done across R1, a 1Ω resistor, while R2 sets the current limit point. When the wiper of R2 is connected, the 1Ω sense resistor current is regulated at 1.2A. As R2 is adjusted, a portion of the 1.2V reference of the LM117 is cancelled by the drop across the pot, decreasing the current limit point. At low output currents, current regulation is degraded since the voltage across the 1Ω sensing resistor becomes quite low. For example, with 50 mA output current, only 50 mV is dropped across the sense resistor and the supply rejection of the LM117 will limit the current regulation



TL/H/7334–2

FIGURE 2. Basic Voltage Regulator

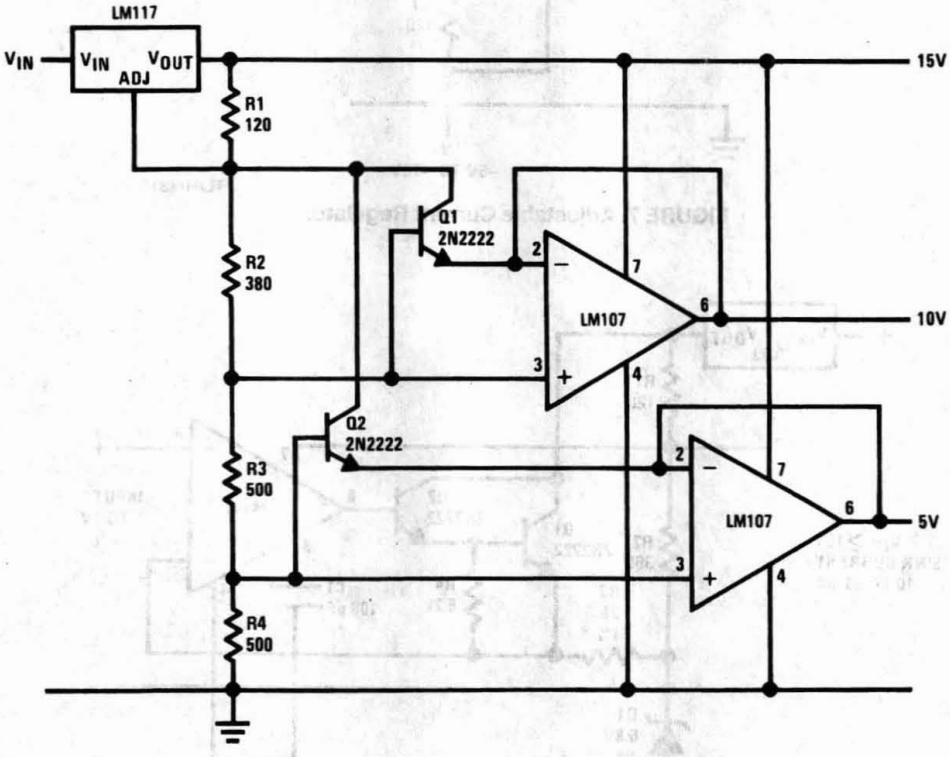


TL/H/7334–3

FIGURE 3. Regulator and Voltage Reference

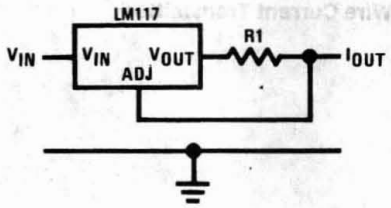
to about 3% for a 40V change across the device. An alternate current regulator is shown in *Figure 7* using an additional LM117 to provide the reference, rather than an LM113 diode. Both current regulators need a negative supply to operate down to ground.

Figure 8 shows a 2-wire current transmitter with 10 mA to 50 mA output current for a 1V input. An LM117 is biased as a 10 mA current source to set the minimum current and provide operating current for the control circuitry. Operating off the 10 mA is an LM108 and an LM129 zener. The zener provides a common-mode voltage for operation of the LM108 as well as a 6.9V reference, if needed. Input signals are impressed across R3, and the curent through R3 is delivered to the output of the regulator by Q1 and Q2. For a 25Ω resistor, this gives a 40 mA current change for a 1V input. This circuit can be used in 4 mA to 20 mA applications, but the LM117 must be selected for low quiescent current. Minimum operating voltage is about 12V.



TL/H/7334–4

FIGURE 4. Regulator with Multiple Outputs

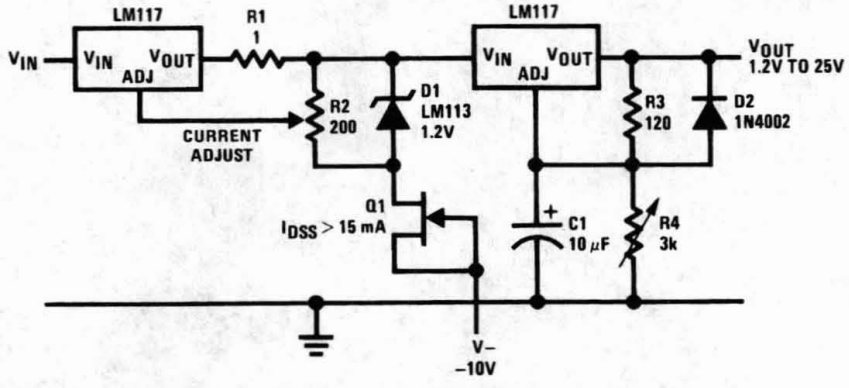


$$I_{OUT} = \frac{1.25V}{R1}$$

$10\ mA \leq I_{OUT} \leq 1.5A$

TL/H/7334–5

FIGURE 5. 2-Terminal Current Regulator



TL/H/7334–6

FIGURE 6. Adjustable Regulator. Constant Voltage/Constant Current, 10 mA to 1.2A

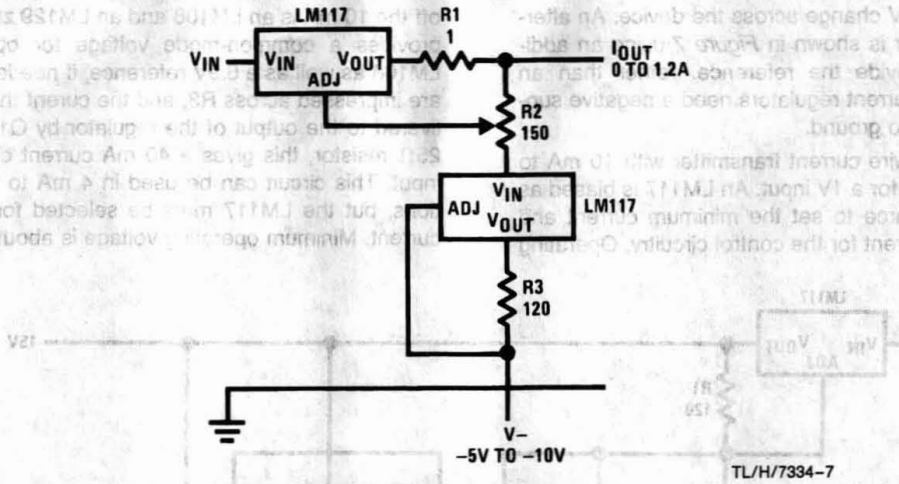


FIGURE 7. Adjustable Current Regulator

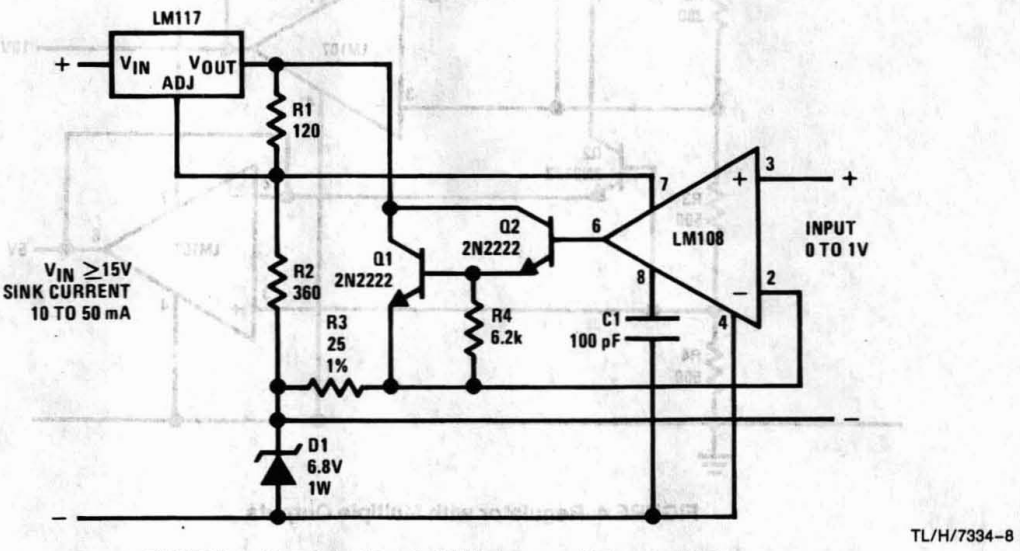


FIGURE 8. 10 mA to 50 mA 2-Wire Current Transmitter

3-Terminal Regulator is Adjustable

National Semiconductor
Application Note 181

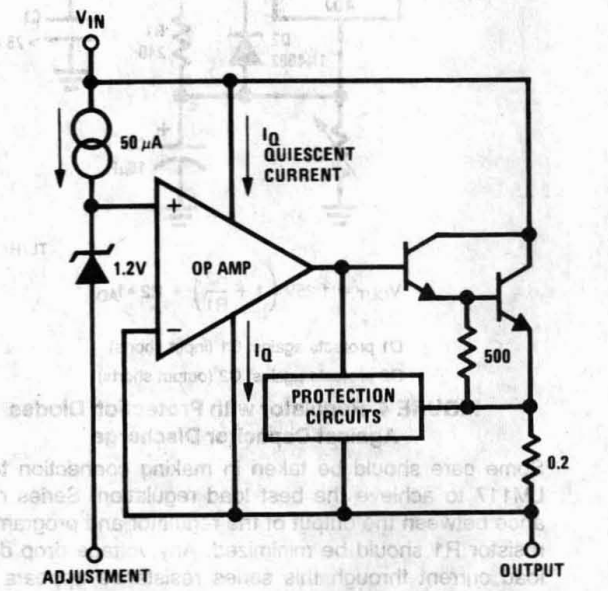
INTRODUCTION

Until now, all of the 3-terminal power IC voltage regulators have a fixed output voltage. In spite of this limitation, their ease of use, low cost, and full on-chip overload protection have generated wide acceptance. Now, with the introduction of the LM117, it is possible to use a single regulator for any output voltage from 1.2V to 37V at 1.5A. Selecting close-tolerance output voltage parts or designing discrete regulators for particular applications is no longer necessary since the output voltage can be adjusted. Further, only one regulator type need be stocked for a wide range of applications. Additionally, an adjustable regulator is more versatile, lending itself to many applications not suitable for fixed output devices.

In addition to adjustability, the new regulator features performance a factor of 10 better than fixed output regulators. Line regulation is 0.01%/V and load regulation is only 0.1%. It is packaged in standard TO-3 transistor packages so that heat sinking is easily accomplished with standard heat sinks. Besides higher performance, overload protection circuitry is improved, increasing reliability.

ADJUSTABLE REGULATOR CIRCUIT

The adjustment of a 3-terminal regulator can be easily understood by referring to *Figure 1*, which shows a functional circuit. An op amp, connected as a unity gain buffer, drives a power Darlington. The op amp and biasing circuitry for the regulator are arranged so that all the quiescent current is delivered to the regulator output (rather than ground) eliminating the need for a separate ground terminal. Further, all the circuitry is designed to operate over the 2V to 40V input to output differential of the regulator.



TL/H/1532–1

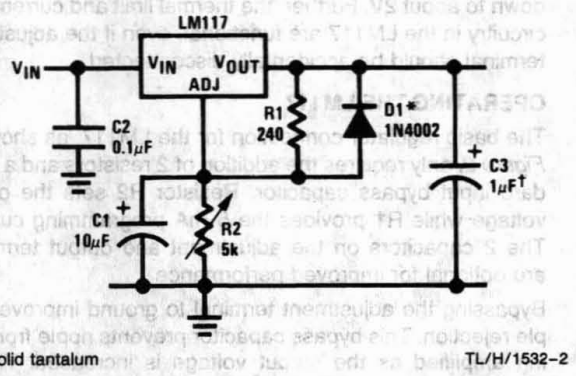
FIGURE 1. Functional Schematic of the LM117

A 1.2V reference voltage appears inserted between the non-inverting input of the op amp and the adjustment terminal. About 50 μA is needed to bias the reference and this current comes out of the adjustment terminal. In operation, the output of the regulator is the voltage of the adjustment terminal plus 1.2V. If the adjustment terminal is grounded, the device acts as a 1.2V regulator. For higher output voltages, a divider R1 and R2 is connected from the output to ground as is shown in *Figure 2*. The 1.2V reference across resistor R1 forces 5 mA of current to flow. This 5 mA then flows through R2, increasing the voltage at the adjustment terminal and therefore the output voltage. The output voltage is given by:

$$V_{OUT} = 1.2V\left(1 + \frac{R2}{R1}\right) + 50\ \mu A\ R2$$

The 50 μA biasing current is small compared to 5 mA and causes only a small error in actual output voltages. Further, it is extremely well regulated against line voltage or load current changes so that is contributes virtually no error to dynamic regulation. Of course, programming currents other than 5 mA can be used depending upon the application.

Since the regulator is floating, all the quiescent current must be absorbed by the load. With too light of a load, regulation is impaired. Usually the 5 mA programming current is sufficient; however, worst case minimum load for commercial grade parts requires a minimum load of 10 mA. The minimum load current can be compared to the quiescent current of standard regulators.



† Solid tantalum

*Discharges C1 if output is shorted to ground

TL/H/1532–2

FIGURE 2. Adjustable Regulator with Improved Ripple Rejection

OVERLOAD PROTECTION CIRCUITRY

An important advancement in the LM117 is improved current limit circuitry. Current limit is set internally at about 2.2A and the current limit remains constant with temperature. Older devices such as the LM309 or LM7800 regulators use the turn-on of an emitter-base junction of a transistor to set the current limit. This causes current limit to typically change by a factor of 2 over a −55°C to +150°C temperature range. Further, to insure adequate output current at 150°C the current limit is relatively high at 25°C, which can cause problems by overloading the input supply.

Also included is safe-area protection for the pass transistor to decrease the current limit as input-to-output voltage differential increases. The safe area protection circuit in the LM117 allows full output current at 15V differential and does not allow the current limit to drop to zero at high input-to-output differential voltages, thus preventing start up problems with high input voltages. *Figure 3* compares the current limit of the LM117 to an LM340 regulator.

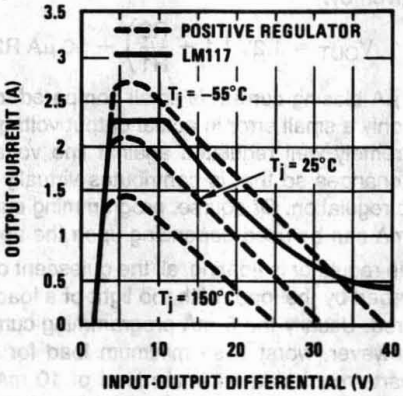


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FIGURE 3. Comparison of LM117 Current Limit with Older Positive Regulator

Thermal overload protection, included on the chip, turns the regulator OFF when the chip temperature exceeds about 170°C, preventing destruction due to excessive heating. Previously, the thermal limit circuitry required about 7V to operate. The LM117 has a new design that is operative down to about 2V. Further, the thermal limit and current limit circuitry in the LM117 are functional, even if the adjustment terminal should be accidentally disconnected.

OPERATING THE LM117

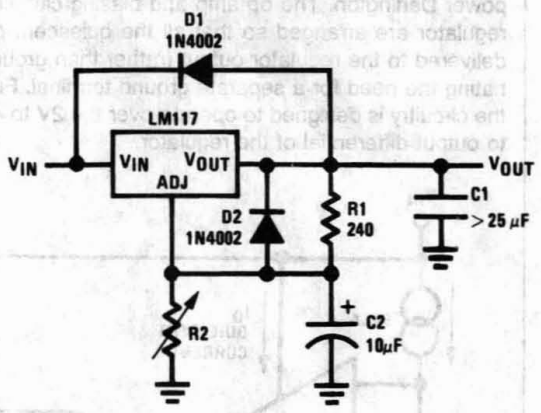
The basic regulator connection for the LM117, as shown in *Figure 2*, only requires the addition of 2 resistors and a standard input bypass capacitor. Resistor R2 sets the output voltage while R1 provides the 5 mA programming current. The 2 capacitors on the adjustment and output terminals are optional for improved performance.

Bypassing the adjustment terminal to ground improves ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor, 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at 120 Hz. If a bypass capacitor is used, it is sometimes necessary to include protection diodes as discussed later, to prevent the capacitor from discharging through internal low current paths in the LM117 and damaging the device.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability. When external capacitors are used with any IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain a 20A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal (C2) can discharge through a low current junction. Discharge occurs when either the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V and less than 10 μF capacitance. *Figure 4* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



TL/H/1532–4

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \bullet I_{ADJ}$$

D1 protects against C1 (input shorts)

D2 protects against C2 (output shorts)

FIGURE 4. Regulator with Protection Diodes Against Capacitor Discharge

Some care should be taken in making connection to the LM117 to achieve the best load regulation. Series resistance between the output of the regulator and programming resistor R1 should be minimized. Any voltage drop due to load current through this series resistance appears as a change in the reference voltage and degrades regulation. If possible, 2 wires should be connected to the output—1 for load current and 1 for resistor R1. The ground of R2 can

be returned near the ground of the load to provide remote sensing and improve load regulation.

APPLICATIONS

Figure 5 shows a 0V to 25V general purpose lab supply. Operation of the LM317 down to 0V output requires the addition of a negative supply so that the adjustment terminal can be driven to −1.2V. An LM329 6.9V reference is used to provide a regulated −1.2V reference to the bottom of adjustment pot R2. The LM329 is an IC zener which has exceptionally low dynamic impedance so the negative supply need not be well regulated. Note that a 10 mA programming current is used since lab supplies are often used with no-load, and the LM317 requires a worst-case minimum load of 10 mA.

The 1.2V minimum output of the LM117 makes it easy to design power supplies with electrical shut-down. At 1.2V, most circuits draw only a small fraction of their normal operating current. In *Figure 6* a TTL input signal causes Q1 to ground the adjustment terminal decreasing the output to 1.2V. If true zero output is desired, the adjustment can be driven to −1.2V; however, this does require a separate negative supply.

When fixed output voltage regulators are used as on-card regulator for multiple cards, the normal output voltage tolerance of ±5% between regulators can cause as much as 10% difference in operating voltage between cards. This can cause operating speed differences in digital circuitry, interfacing problems or decrease noise margins.

Figure 7 shows a method of adjusting multiple on-card regulators so that all outputs track within ±100 mV. The adjustment terminals of all devices are tied together and a single divider is used to set the outputs. Programming current is set at 10 mA to minimize the effects of the 50 μA biasing current of the regulators and should further be increased if many LM117's are used. Diodes connected across each regulator insure that all outputs will decrease if 1 regulator is shorted.

Two terminal current regulators can be made with fixed-output regulators; however, their high output voltage and high quiescent current limit their accuracy. With the LM117 as shown in *Figure 8*, a high performance current source useful from 10 mA to 1.5A can be made. Current regulation is typically 0.01%/V even at low currents since the quiescent current does not cause an error. Minimum operating voltage is less than 4V, so it is also useful as an in-line adjustable current limiter for protection of other circuitry.

Low cost adjustable switching regulators can be made using an LM317 as the control element. *Figure 9* shows the simplest configuration. A power PNP is used as the switch driving an L-C filter. Positive feedback for hysteresis is applied to the LM317 through R6. When the PNP switches, a small square wave is generated across R5. This is level shifted and applied to the adjustment terminal of the regulator by R4 and C2, causing it to switch ON or OFF. Negative

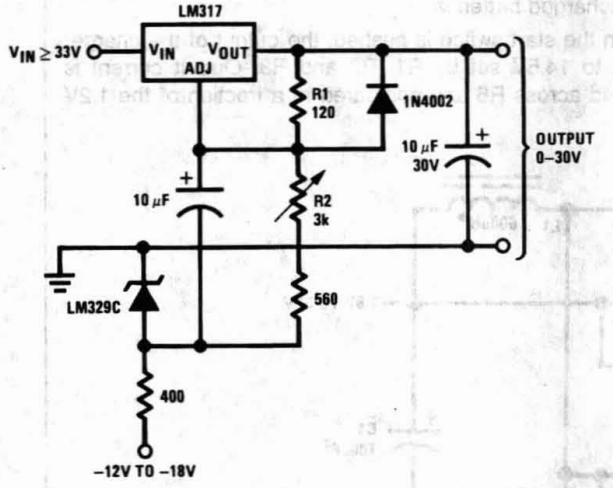


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FIGURE 5. General Purpose 0–30V Power Supply

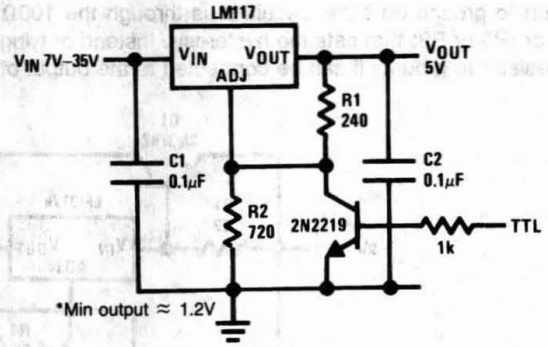

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FIGURE 6. 5V Logic Regulator with Electronic Shutdown*

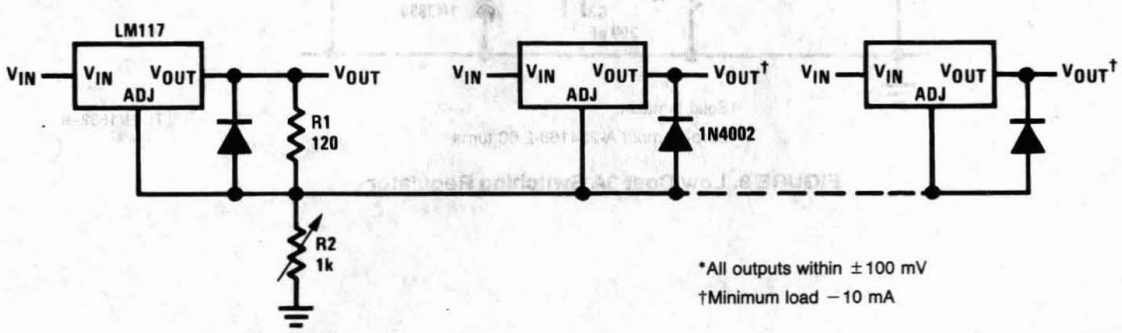

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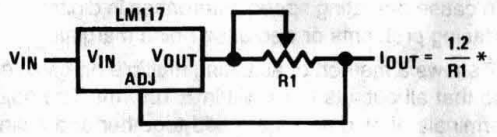
FIGURE 7. Adjusting Multiple On-Card Regulators with Single Control*



TL/H/1532–8

*0.8Ω ≤ R1 ≤ 120Ω

FIGURE 8. Precision Current Limiter

feedback is taken from the output through R3, making the circuit oscillate. Capacitor C3 acts as a speed-up, increasing switching speed, while R2 limits the peak drive current to Q1.

The circuit in *Figure 9* provides no protection for Q1 in case of an overload. A blow-out proof switching regulator is shown in *Figure 10*. The PNP transistor has been replaced by a PNP-NPN combination with LM395's used as the NPN transistors. The LM395 is an IC which acts as an NPN transistor with overload protection. Included on the LM395 is current limiting, safe-area protection and thermal overload protection making the device virtually immune to any type of overload.

Efficiency for the regulators ranges from 65% to 85%, depending on output voltage. At low output voltages, fixed power losses are a greater percentage of the total output power so efficiency is lowest. Operating frequency is about 30 kHz and ripple is about 150 mV, depending upon input voltage. Load regulation is about 50 mV and line regulation about 1% for a 10V input change.

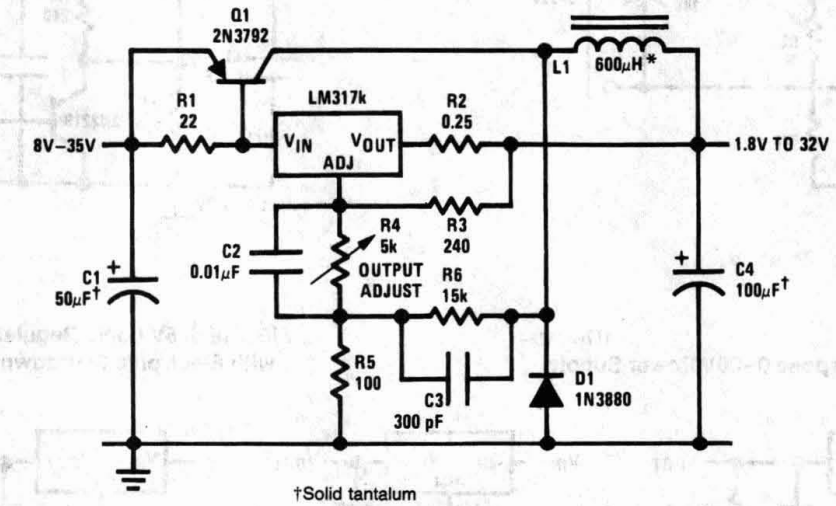
One of the more unique applications for these switching regulators is as a tracking pre-regulator. The only DC connection to ground on either regulator is through the 100Ω resistor (R5 or R8) that sets the hysteresis. Instead of tying this resistor to ground, it can be connected to the output of a linear regulator so that the switching regulator maintains a constant input-to-output differential on the linear regulator. The switching regulator would typically be set to hold the input voltage to the linear regulator about 3V higher than the output.

Battery charging is another application uniquely suited for the LM117. Since battery voltage is dependent on electrochemical reactions, the charger must be designed specifically for the battery type and number of cells. Ni-Cads are easily charged with the constant current sources shown previously. For float chargers on lead-acid type batteries all that is necessary is to set the output of the LM117 at the float voltage and connect it to the battery. An adjustable regulator is mandatory since, for long battery life the float voltage must be precisely controlled. The output voltage temperature coefficient can be matched to the battery by inserting diodes in series with the adjustment resistor for the regulator and coupling the diodes to the battery.

A high performance charger for gelled electrolite lead-acid batteries is shown in *Figure 11*. This charger is designed to quickly recharge a battery and shut off at full charge.

Initially, the charging current is limited to 2A by the internal current limit of the LM117. As the battery voltage rises, current to the battery decreases and when the current has decreased to 150 mA, the charger switches to a lower float voltage preventing overcharge. With a discharged battery, the start switch is not needed since the charger will start by itself; however, it is included to allow topping off even slightly discharged batteries.

When the start switch is pushed, the output of the charger goes to 14.5V set by R1, R2 and R3. Output current is sensed across R6 and compared to a fraction of the 1.2V



†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/1532–9

FIGURE 9. Low Cost 3A Switching Regulator

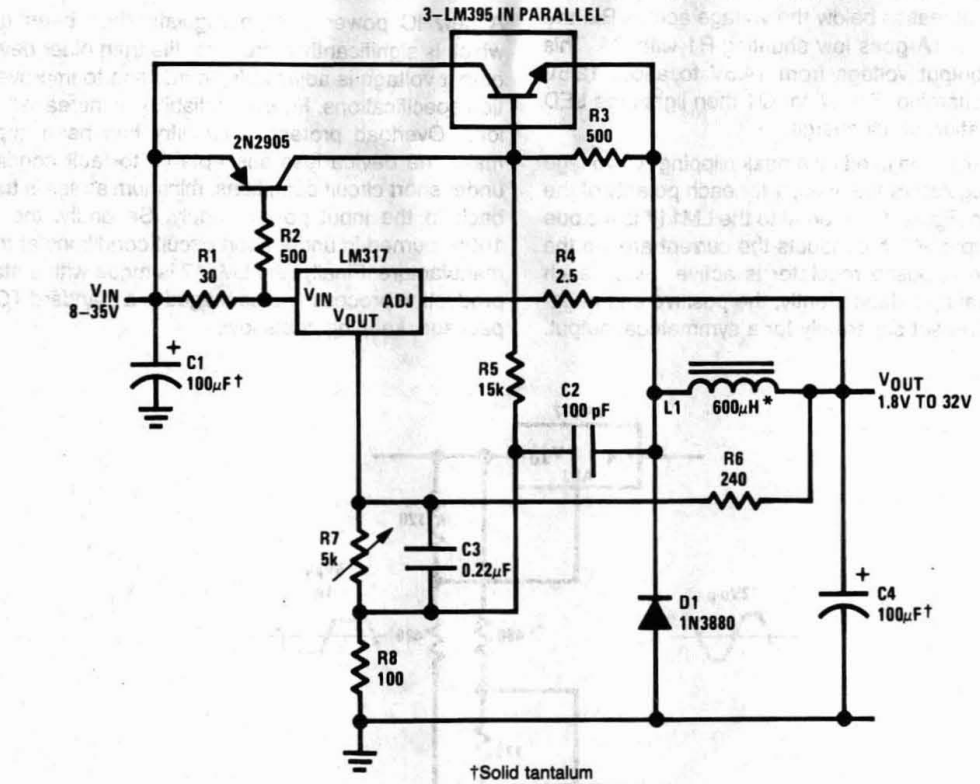


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FIGURE 10. 4A Switching Regulator with Overload Protection

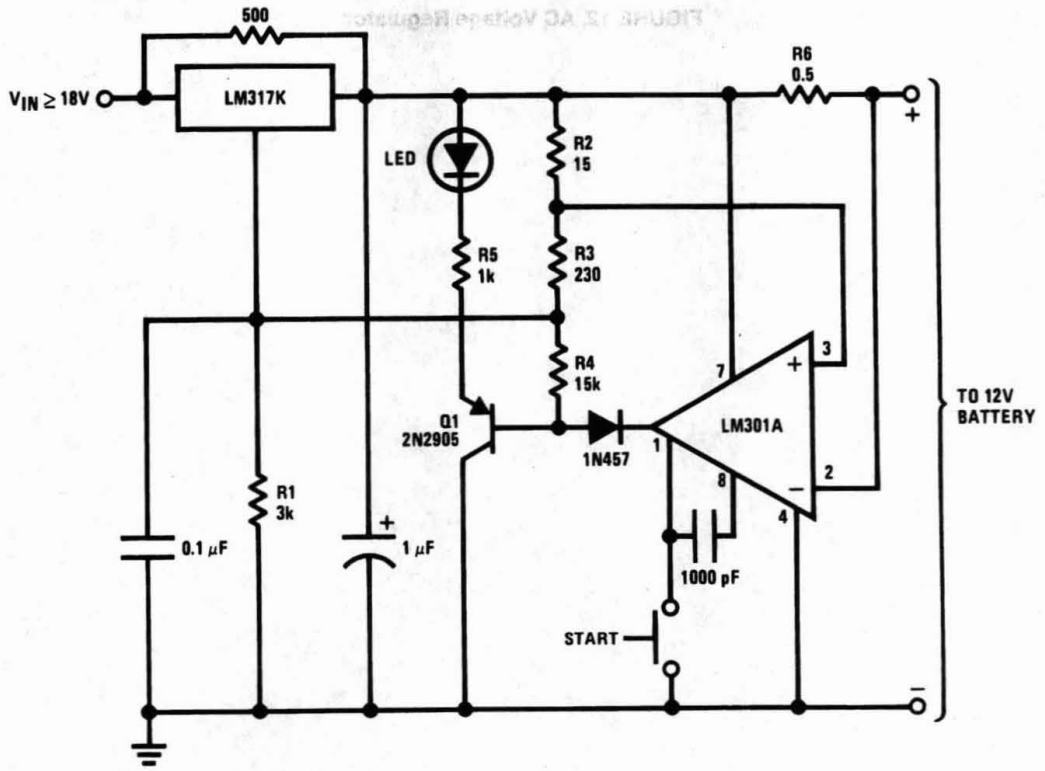

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FIGURE 11. 12V Battery Charger

reference (across R2) by an LM301A op amp. As the voltage across R6 decreases below the voltage across R2, the output of the LM101A goes low shunting R1 with R4. This decreases the output voltage from 14.5V to about 12.5V terminating the charging. Transistor Q1 then lights the LED as a visual indication of full charge.

The LM117 can even be used as a peak clipping AC voltage regulator. Two regulators are used, 1 for each polarity of the input as shown in *Figure 12*. Internal to the LM117 is a diode from input-to-output which conducts the current around the device when the opposite regulator is active. Since each regulator is operating independently, the positive and negative peaks must be set separately for a symmetrical output.

CONCLUSIONS

A new IC power voltage regulator has been developed which is significantly more versatile than older devices. The output voltage is adjustable, in addition to improved regulation specifications. Further, reliability is increased in 2 fashions. Overload protection circuitry has been improved to make the device less susceptable to fault conditions and under short circuit conditions, minimum stress is transmitted back to the input power supply. Secondly, the device is 100% burned-in under short circuit conditions at the time of manufacture. Finally, the LM117 is made with a standard IC production process and packaged in a standard TO-3 power package, keeping costs low.

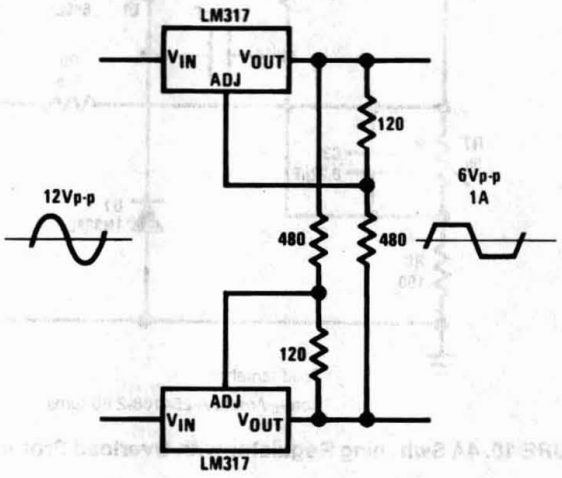

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FIGURE 12. AC Voltage Regulator

Improving Power Supply Reliability with IC Power Regulators

National Semiconductor
Application Note 182

Three-terminal IC power regulators include on-chip overload protection against virtually any normal fault condition. Current limiting protects against short circuits fusing the aluminum interconnects on the chip. Safe-area protection decreases the available output current at high input voltages to insure that the internal power transistor operates within its safe area. Finally, thermal overload protection turns off the regulator at chip temperatures of about 170°C, preventing destruction due to excessive heating. Even though the IC is fully protected against normal overloads, careful design must be used to insure reliable operation in the system.

SHORT CIRCUITS CAN OVERLOAD THE INPUT

The IC is protected against short circuits, but the value of the on-chip current limit can overload the input rectifiers or transformer. The on-chip current limit is usually set by the manufacturer so that with worst-case production variations and operating temperature the device will still provide rated output current. Older types of regulators, such as the LM309, LM340 or LM7800 can have current limits of 3 times their rated output current.

The current limit circuitry in these devices uses the turn-on voltage of an emitter-base junction of a transistor to set the current limit. The temperature coefficient of this junction combined with the temperature coefficient of the internal resistors gives the current limit a −0.5%/°C temperature coefficient. Since devices must operate and provide rated current at 150°C, the 25°C current limit is 120% higher than typical. Production variations will add another ±20% to initial current limit tolerance so a typical 1A part may have a 3A current limit at 25°C. This magnitude of overload current can blow the input transformer or rectifiers if not considered in the initial design—even though it does not damage the IC.

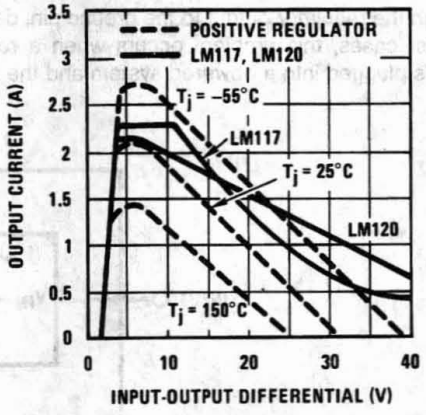
One way around this problem (other than fuses) is by the use of minimum size heat sinks. The heat sink is designed for only normal operation. Under overload conditions, the device (and heat sink) are allowed to heat up to the thermal shut-down temperature. When the device shuts down, loading on the input is reduced.

Newer regulators have improved current limiting circuitry. Devices like the LM117 adjustable regulator, LM123, 3A, 5V logic regulator or the LM120 negative regulators have a relatively temperature-stable current limit. Typically these devices hold the current limit within ±10% over the full −55°C to +150°C operating range. A device rated for 1.5A output will typically have a 2.2A current limit, greatly easing the problem of input overloads.

Many of the older IC regulators can oscillate when in current limit. This does not hurt the regulator and is mostly dependent upon input bypassing capacitors. Since there is a large variability between regulator types and manufacturers, there is no single solution to eliminating oscillations. Generally, if oscillations cause other circuit problems, either a solid tantalum input capacitor or a solid tantalum in series with 5Ω to 10Ω will cure the problem. If one doesn't work, try the other.

Start-up problems can occur from the current limit circuitry too. At high input-ouput differentials, the current limit is decreased by the safe-area protection. In most regulators the decrease is linear, and at input-output voltages of about 30V the output current can decrease to zero. Normally this causes no problem since, when the regulator is initially powered, the output increases as the input increases. If such a regulator is running with, for example, 30V input and 15V output and the output is momentarily shorted, the input-output differential increases to 30V and available output current is zero. Then the output of the regulator stays at zero even if the short is removed. Of course, if the input is turned OFF, then ON, the regulator will come up to operating voltage again. The LM117 is the only regulator which is designed with a new safe-area protection circuit so output current does not decrease to zero, even at 40V differential.

This type of start-up problem is particularly load dependent. Loads to a separate negative supply or constant-current devices are among the worst. Another, usually overlooked, load is pilot lights. Incandescent bulbs draw 8 times as much current when cold as when operating. This severely adds to the load on a regulator, and may prevent turn-on. About the only solutions are to use an LM117 type device, or bypass the regulator with a resistor from input to output to supply some start-up current to the load. Resistor bypassing will not degrade regulation if, under worst-case conditions of maximum input voltage and minimum load current, the regulator is still delivering output current rather than absorbing current from the resistor. *Figure 1* shows the output current of several different regulators as a function of output voltage and temperature.



TL/H/7458–1

FIGURE 1. Comparison of LM117 Current Limit with Older Positive Regulator

When a positive regulator (except for the LM117) is loaded to a negative supply, the problem of start-up can be doubly bad. First, there is the problem of the safe-area protection as mentioned earlier. Secondly, the internal circuitry cannot supply much output current when the output pin is driven more negative than the ground pin of the regulator. Even with low input voltages, some positive regulators will not start when loaded by 50 mA to a negative supply. Clamping the output to ground with a germanium or Schottky diode usually solves this problem. Negative regulators, because of different internal circuitry, do not suffer from this problem.

DIODES PROTECT AGAINST CAPACITOR DISCHARGE

It is well recognized that improper connections to a 3-terminal regulator will cause its destruction. Wrong polarity inputs or driving current into the output (such as a short between a 5V and 15V supply) can force high currents through small area junctions in the IC, destroying them. However, improper polarities can be applied accidently under many normal operating conditions, and the transient condition is often gone before it is recognized.

Perhaps the most likely sources of transients are external capacitors used with regulators. *Figure 2* shows the discharge path for different capacitors used with a positive regulator. Input capacitance, C1, will not cause a problem under any conditions. Capacitance on the ground pin (or adjustment pin is the case of the LM117) can discharge through 2 paths which have low current junctions.

If the output is shorted, C2 will discharge through the ground pin, possibly damaging the regulator. A reverse-biased diode, D2, diverts the current around the regulator, protecting it. If the input is shorted, C3 can discharge through the output pin, again damaging the regulator. Diode D1 protects against C3, preventing damage. Also, with both D1 and D2 in the circuit, when the input is shorted, C2 is discharged through both diodes, rather than the ground pin.

In general, these protective diodes are a good idea on all positive regulators. At higher output voltages, they become more important since the energy stored in the capacitors is larger. With negative regulators and the LM117, there is an inernal diode in parallel with D1 from output-to-input, eliminating the need for an external diode if the output capacitor is less than 25 μF.

Another transient condition which has been shown to cause problems is momentary loss of the ground connection. This charges the output capacitor to the unregulated input voltage minus a 1—2V drop across the regulator. If the ground is then connected, the output capacitor, C3, discharges through the regulator output to the ground pin, destroying it. In most cases, this problem occurs when a regulator (or card) is plugged into a powered system and the input pin is connected before the ground. Control of the connector configuration, such as using 2 ground pins to insure ground is connected first, is the best way of preventing this problem. Electrical protection is cumbersome. About the only way to protect the regulator electrically is to make D2 a power zener 1V to 2V above the regulator voltage and include 10Ω to 50Ω in the ground lead to limit the current.

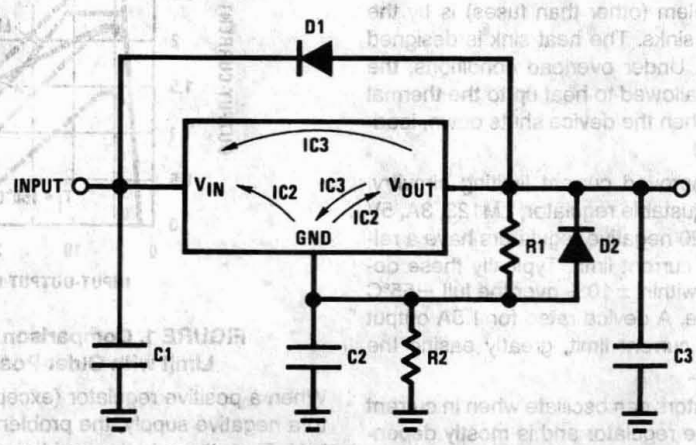
LOW OPERATING TEMPERATURE INCREASES LIFE

Like any semiconductor circuit, lower operating temperature improves reliability. Operating life decreases at high junction temperatures. Although many regulators are rated to meet specifications at 150°C, it is not a good idea to design for continuous operation at that temperature. A reasonable maximum operating temperature would be 100°C for epoxy packaged devices and 125°C for hermetically sealed (TO-3) devices. Of course, the lower the better, and decreasing the above temperatures by 25°C for normal operation is still reasonable.

Another benefit of lowered operating temperatures is improved power cycle life for low cost soft soldered packages. Many of today's power devices (transistors included) are assembled using a TO-220 or TO-3 aluminum soft solder system. With temperature excursions, the solder work-hardens and with enough cycles the solder will utlimately fail. The larger the temperature change, the sooner failure will occur. Failures can start at about 5000 cycles with a 100°C temperature excursion. This necessitates, for example, either a large heat sink or a regulator assembled with a hard solder, such as steel packages, for equipment that is continuously cycled ON and OFF.

THERMAL LIMITING GIVES ABSOLUTE PROTECTION

Without thermal overload protection, the other protection circuitry will only protect against short term overloads. With thermal limiting, a regulator is not destroyed by long time short circuits, overloads at high temperatures or inadequate heat sinking. In fact, this overload protection makes the IC regulator tolerant of virtually any abuse, with the possible exception of high-voltage transients, which are usually filtered by the capacitors in most power supplies.



TL/H/7458–2

FIGURE 2. Positive Regulator with Diode Protection Against Transient Capacitor Discharge

One problem with thermal limiting is testing. With a 3-terminal regulator, short-circuit protection and safe-area protection are easily measured electrically. For thermal limiting to operate properly, the electrical circuitry on the IC must function and the IC chip must be well die-attached to the package so there are no hot spots. About the only way to insure that thermal limiting works is to power the regulator, short the output, and let it cook. If the regulator still works after 5 minutes (or more) the thermal limit has protected the regulator.

This type of testing is time consuming and expensive for the manufacturer so it is not always done. Some regulators, such as the LM117, LM137, LM120 and LM123, do receive an electrical burn-in in thermal shutdown as part of their testing. This insures that the thermal limiting works as well as reducing infant mortality. If it is probable that a power supply will have overloads which cause the IC to thermally limit, testing the regulator is in order.

References for A/D Converters

National Semiconductor
Application Note 184

Interfacing between digital and analog signals is becoming increasingly important with the proliferation of digital signal processing. System accuracy is often limited by the accuracy of the converter and a limitation of the converter is the voltage reference. Design can be difficult if the reference is external.

The accuracy of any converter is limited by the temperature drift or long term drift of the voltage reference, even if conversion linearity is perfect. Assuming that the voltage reference is allowed to add 1/2 least significant bit error (LSB) to the converter, it is surprising how good the reference must be when even small temperature excursions are considered. When temperature changes are large, the reference design is a major problem. Table I shows the reference requirements for different converters while Table II shows how the same problems exist with digital panel meters.

The voltage reference circuitry is required to do several functions to maintain a stable output. First, input power supply changes must be rejected by the reference circuitry. Secondly, the zener used in the reference must be biased properly, while other parts of circuitry scale the typical zener voltage and provides a low impedance output. Finally, the reference circuitry must reject ambient temperature changes so that the temperature drift of the reference circuitry plus the drift of the zener does not exceed the desired drift limit.

While zener temperature coefficient is obviously critical to reference performance, other sources of drift can easily add as much error as zener — even in voltage references with modest performance of 20 ppm/°C temperature drift. Zener drift and op amp drift add directly to the drift error, while resistor error is only a function of how well the scaling resistors track. Resistors which have a high TC can be used if they track.

For a 10V output with a 6.9V zener, the drift contribution of resistor mistracking is about 0.4 since the gain is 1.4. The range of temperature coefficient errors for different components used to make a 10V reference from a 6.9V zener are shown in Table III. Another potential source of error, input supply variations, are negligible if the input is 1% regulated, and the resistor feeding the zener is stable to 1%.

Less frequently specified sources of error in voltage reference zeners are hysteresis and stress sensitivity. Stress on either a zener-diode junction or the series-temperature-compensating junction will cause voltage shifts. The axial leads on discrete devices can transmit stress from outside the package to the junction, causing 1 mV to 5 mV shifts.

Temperature cycling is the discrete zener can also induce non-reversible changes in zener voltage. If a zener is heated from 25°C to 100°C and then back to 25°C, the zener voltage may not return to its original value. This is because the temperature cycle has permanently changed the stress in the die, changing the voltage. This effect can be as high as 5 mV in some diodes and may be cumulative with many temperature cycles. The new planar IC zeners, such as the LM199 (temperature stabilized) or the LM129 are insensitive to stress and show only about 50 μV of hysteresis for a 150°C temperature cycle since the package does not stress the silicon chip.

DESIGNING THE REFERENCE

If moderate temperature performance such as 20 ppm/°C is all that is needed, 2 different approaches can be used in the reference design. In the first, the temperature drift error is split equally between the zener and the amplifier or scaling resistors. This requires a moderately low drift zener and op amp with 10 ppm resistors.

TABLE I. Maximum Allowable Reference Drift for 1/2 Least Significant Bits Error of Binary Coded Converter

TEMP CHANGE	BITS					
	6	8	10	12	14	
25°C	310	80	20	5	1.25	ppm/°C
50°C	160	40	10	2.5	0.6	ppm/°C
100°C	80	20	5	1.2	0.3	ppm/°C
125°C	63	16	3	1	0.2	ppm/°C

TABLE II. Maximum Allowable Reference Drift for 1/2 Digit Error of Digital Meters

TEMP CHANGE	DIGITS								
	2	2½	3	3½	4	4½	5	5½	
25°C	200	100	20	10	2	1	0.2	0.1	ppm/°C
5°C			100	50	10	5	1	0.5	ppm/°C

*0.01%/°C = 100 ppm/°C, 0.001%/°C = 10 ppm/°C, 0.0001%/°C = 1 ppm/°C

TABLE III. Drift Error Contribution From Reference Components for a 10V Reference

DEVICE	ERROR	10V OUTPUT DRIFT
Zener	**Zener Drift**	
LM199A	0.5 ppm/°C	0.5 ppm/°C
LM199, LM399A	1 ppm/°C	1 ppm/°C
LM399	2 ppm/°C	2 ppm/°C
1N829, LM3999	5 ppm/°C	5 ppm/°C
LM129, 1N823A, 1N827A, LM329A	10–50 ppm/°C	10–50 ppm/°C
LM329, 1N821, 1N825	20–100 ppm/°C	20–100 ppm°C
Op Amp	**Offset Voltage Drift**	
LM725, LH0044, LM121	1 μV/°C	0.15 ppm/°C
LM108A, LM208A, LM308A	5 μV/°C	0.7 ppm/°C
LM741, LM101A	15 μV/°C	2 ppm/°C
LM741C, LM301A, LM308	30 μV/°C	4 ppm/°C
Resistors	**Resistance Ratio Drift**	
1% (RN55D)	50–100 ppm	20–40 ppm/°C
0.1% (Wirewound)	5–10	2–4 ppm
Tracking 1 ppm Film or Wirewound	—	0.4 ppm/°C

The second approach uses a very low drift zener and allows the buffer amplifier or scaling resistor to cause most of the drift error. This type of design is now made economical by the availability of low cost temperature stabilized IC zeners with virtually no TC. Further, the temperature coefficient of this reference is easily upgraded, if necessary. The 2 reference circuits are shown in *Figure 1a and Figure 1b.*

In *Figure 1a,* an LM308 op amp is used to increase the typical zener output to 10V while adding a worst-case drift of 4 ppm/°C to the 10 ppm/°C of the zener. Resistors R3 and R4 should track to better than 10 ppm bringing the total error so far to 18 ppm. Since the output must be adjusted to eliminate the initial zener tolerance, a pot, R5 and R2 have been added. The loading on the pot by R2 is small, and there is no tracking requirement between the pot and R2. It is necessary for R2 to track R3 and R4 within 50 ppm.

In *Figure 1b,* a low drift reference and op amp are used to give a total drift, exclusive of resistors of 3 ppm/°C. Now the resistor tracking requirement is relaxed to about 50 ppm, allowing ordinary 1% resistors to be used. The circuit in *Figure 1b* is modified easily for applications requiring 3 ppm/°C to 5 ppm/°C overall drift by tightening the tracking of the resistors. For more accurate applications, the Kelvin sensing for both output and ground should be used. For even lower drifts, substituting a 1 μV/°C op amp, 1 ppm tracking resistors and an LM199A zener, overall drifts of 1 ppm/°C can be achieved. In both of the circuits, it is important to remember that the tracking of resistors can, at worst-case, be twice temperature drift of either resistance.

In both circuits, the zener is biased by a single resistor from the supply, rather than from the reference output. This eliminates possible start-up problems and, because of the 1Ω dynamic impedance of the IC zeners, only adds about

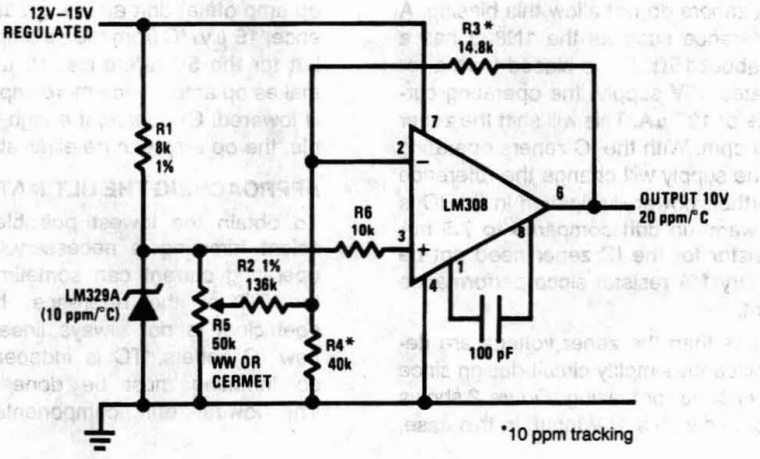


FIGURE 1a. 10V, 20 ppm Reference Using a Low Cost Zener and Low Drift Resistors

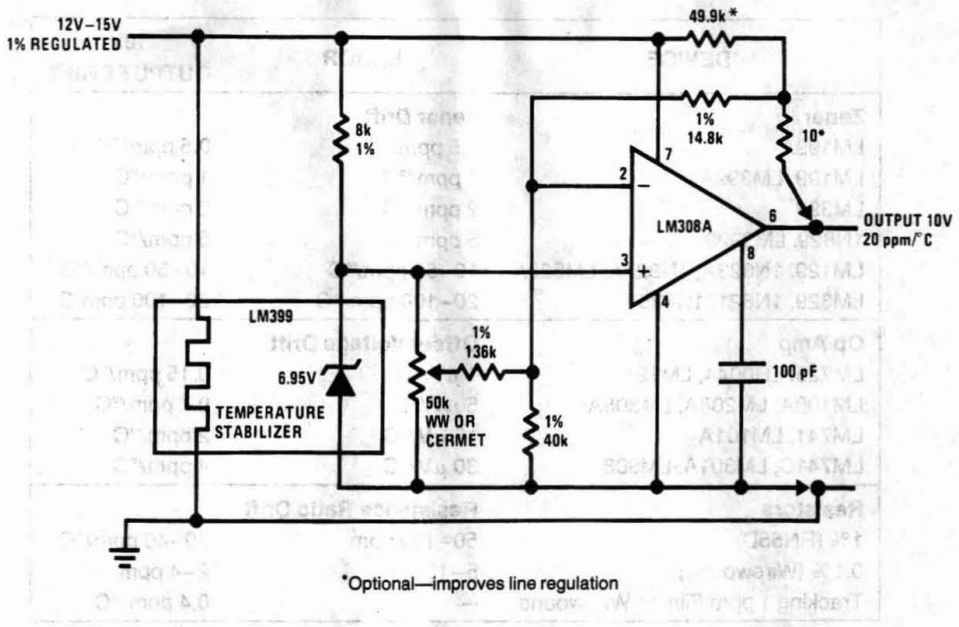


FIGURE 1b. 10V Reference has Low Drift Reference and Standard 1% Resistors. Kelvin Sensing is Shown with Compensation for Line Changes.

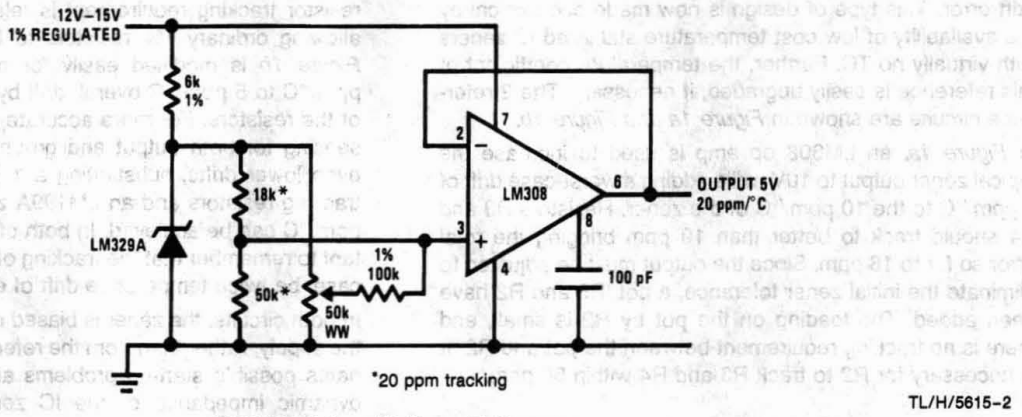


FIGURE 2. Low Voltage Reference

20 μV of error. Compensation for input changes is shown in *Figure 1b.* Conventional zeners do not allow this biasing. A conventional 5 ppm reference such as the 1N829 has a dynamic impedance of about 15Ω. If it is biased from a resistor from a 1% regulated 15V supply, the operating current can change by 1.7% or 127 μA. This will shift the zener voltage by 1.9 mV or 60 ppm. With the IC zeners operating at 1 mA, a 1% shift in the supply will change the reference by 20 μV or 3 ppm. Further, power dissipation in the IC is only 7 mW, giving low warm-up drift compared to 7.5 mA zeners. The biasing resistor for the IC zener need not be any better than an ordinary 1% resistor since performance is independent of current.

When output voltages less than the zener voltage are desired, the IC zeners significantly simplify circuit design since no auxiliary regulator is needed for biasing. *Figure 2* shows a 5V reference circuit for use with a 15V input. In this case, zener drift contributes proportionally to the output drift while op amp offset drift adds a greater rate. With the 10V reference, 15 μV/°C from the op amp contributed 2 ppm/°C drift, but for the 5V reference, 15 μV/°C adds 3 ppm/°C. This makes op amp choice more important as the output voltage is lowered. Of course, if a high output impedance is tolerable, the op amp can be eliminated.

APPROACHING THE ULTIMATE DRIFT

To obtain the lowest possible drifts, temperature coefficient trimming is necessary. With discrete zeners, the operating current can sometimes be trimmed to change the TC of the reference; however, the temperature coefficient is not always linear or predictable. With the new IC zeners, TC is independent of operating current so trimming must be done elsewhere in the circuit. The lowest drift components should be used since

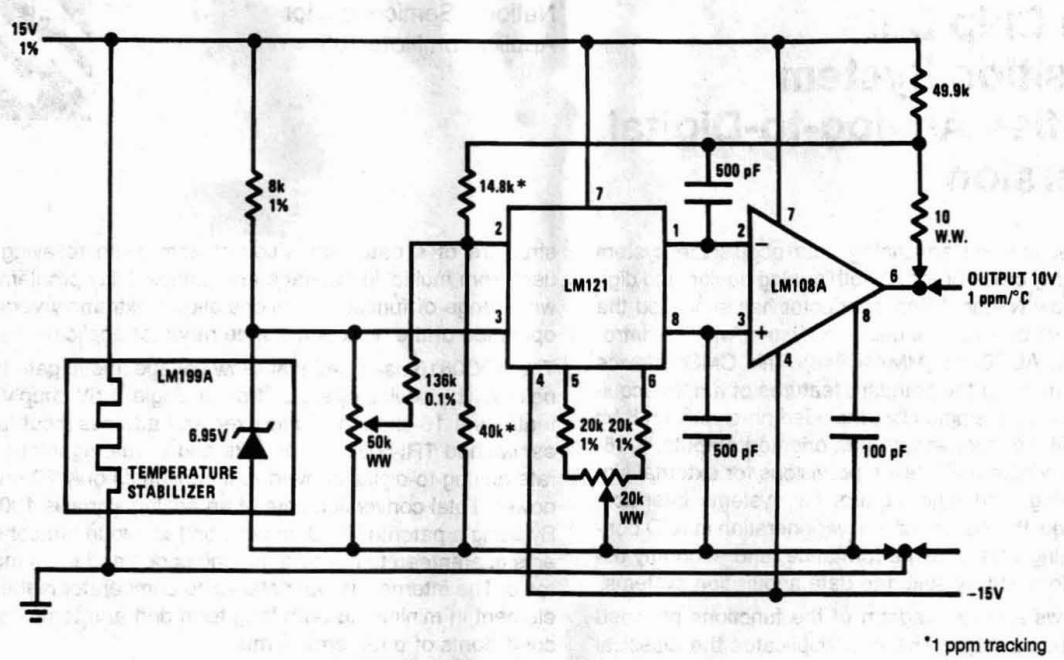


FIGURE 3. Ultra Low Drift Reference

trimming can only remove a linear component of drift. High TC devices can have a highly non-linear drift, making trimming difficult.

Figure 3 shows a circuit suitable for trimming. An LM199A reference with 0.5 ppm/°C drift is used with a 121/108 op amp. Resistors should be 1 ppm tracking to give overall untrimmed drifts of about 0.9 ppm. The 121/108 is a low drift amplifier combination where drift is predictably proportional to offset voltage. An offset can be set for the 108/121 combination to cancel the measured drift with 1 pass calibration.

Trimming procedure is as follows: the zener is disconnected and the input of the op amp grounded. Then the offset of the op amp is nulled out to zero. Reconnecting the zener, the output is adjusted to precisely 10V. A temperature run is made and the drift noted. The op amp will drift 3.6 μV/°C for every 1 mV of offset, so for every 5 μV/°C drift at the output, the offset of the op amp is adjusted 1 mV (1.4 mV measured at the output) in the opposite direction. The output is readjusted to 10V and the drift checked.

Although this trimming scheme was chosen since only a single adjustment is usually required, compensation is not always perfect. Hysteresis effects can appear in resistors or op amps as well as zeners. Best results can be obtained by cycling the circuit to temperature a few times before taking data to relieve assembly stresses on the components. Also, oven testing can sometimes cause thermal gradients across circuits, giving 50 μV to 100 μV of error. However, with careful layout and trimming, overall reference drifts of 0.1 ppm/°C to 0.2 ppm/°C can be achieved.

There are 2 other possible problem areas to be considered before final layout. Good single point grounding is important. Traces on a PC board can easily have 0.1Ω and only 10 mA will cause a 1 mV shift. Also, since these references are close to high-speed digital circuitry, shielding may be necessary to prevent pick-up at the inputs of the op amp. Transient response to pick-up or rapid loading changes can sometimes be improved by a large capacitor. (1 μF—10 μF) directly on the op amp output; but this will depend on the stability of the op amp.

Single Chip Data Acquisition System Simplifies Analog-to-Digital Conversion

National Semiconductor
Application Note 193

Until recently, building an analog data acquisition system required a hardy cross-breed of both analog design and digital design. Now National Semiconductor has simplified the design problem of a data acquisition system with the introduction of the ADC0816 (MM74C948). This CMOS device incorporates many of the standard features of a data acquisition system onto a single chip. Included on-chip is an 8-bit analog-to-digital converter with bus oriented outputs, a 16-channel expandable multiplexer, provisions for external signal conditioning, and logic control for systems interface. This chip marks the advent of a new generation in A/D converters, bringing versatility, performance, and economy using a technology ideally suited to data acquisition systems.

Figure 1 shows a block diagram of the functions provided within a single package. The chip duplicates the classical structure of a data acquisition system while relieving the user from multichip interface and compatibility problems. A wide range of functional options allows extremely versatile operation of the device in a wide range of applications.

The ADC0816 uses National's low voltage, metal gate technology. The device operates from a single +5V supply and features a 16-channel multiplexer with address input latches, latched TRI-STATE® outputs and a true eight-bit-accurate analog-to-digital converter. It consumes only 20 mW of power. Total conversion time of an analog signal is 100 μs. By using a patented A/D conversion technique the converter is guaranteed to have no missing codes and to be monotonic. The internal chopper stabilized comparator is the key element in minimizing both long term drift and temperature coefficients of other error terms.

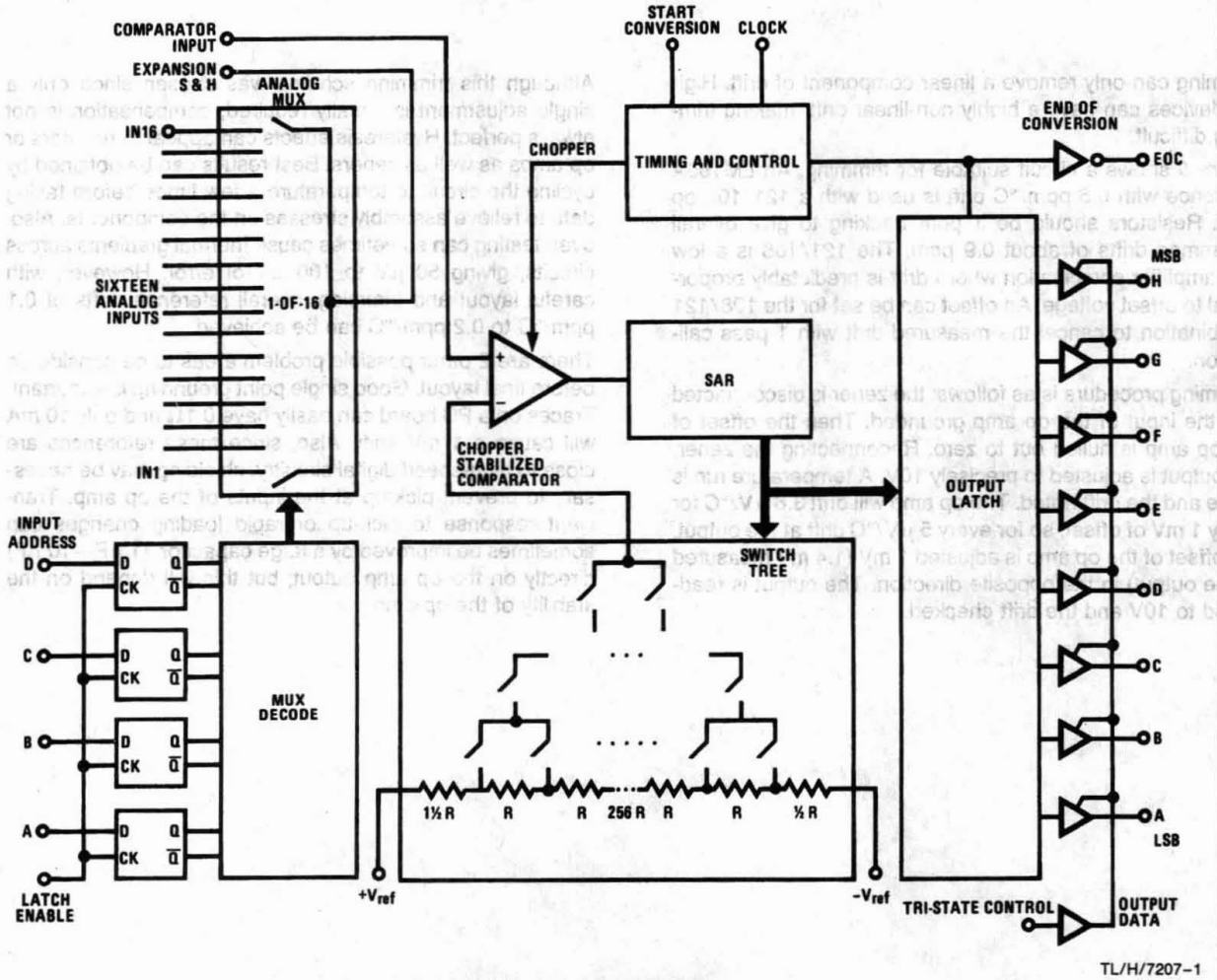


FIGURE 1. ADC0816/MM74C948 Block Diagram

Figure 2 shows a typical application employing the ADC0816 for use in a microprocessor-based environmental control system. In this system the microprocessor can select a channel, monitor a particular sensor reading, convert that signal to a digital word, and make a system decision based upon that input. Many other areas of process control, machine control, or multi-input analog system can utilize this basic configuration.

THE CONVERTER

The heart of this single-chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into three major sections: the 256R ladder network, the successive approximation register, and the comparator.

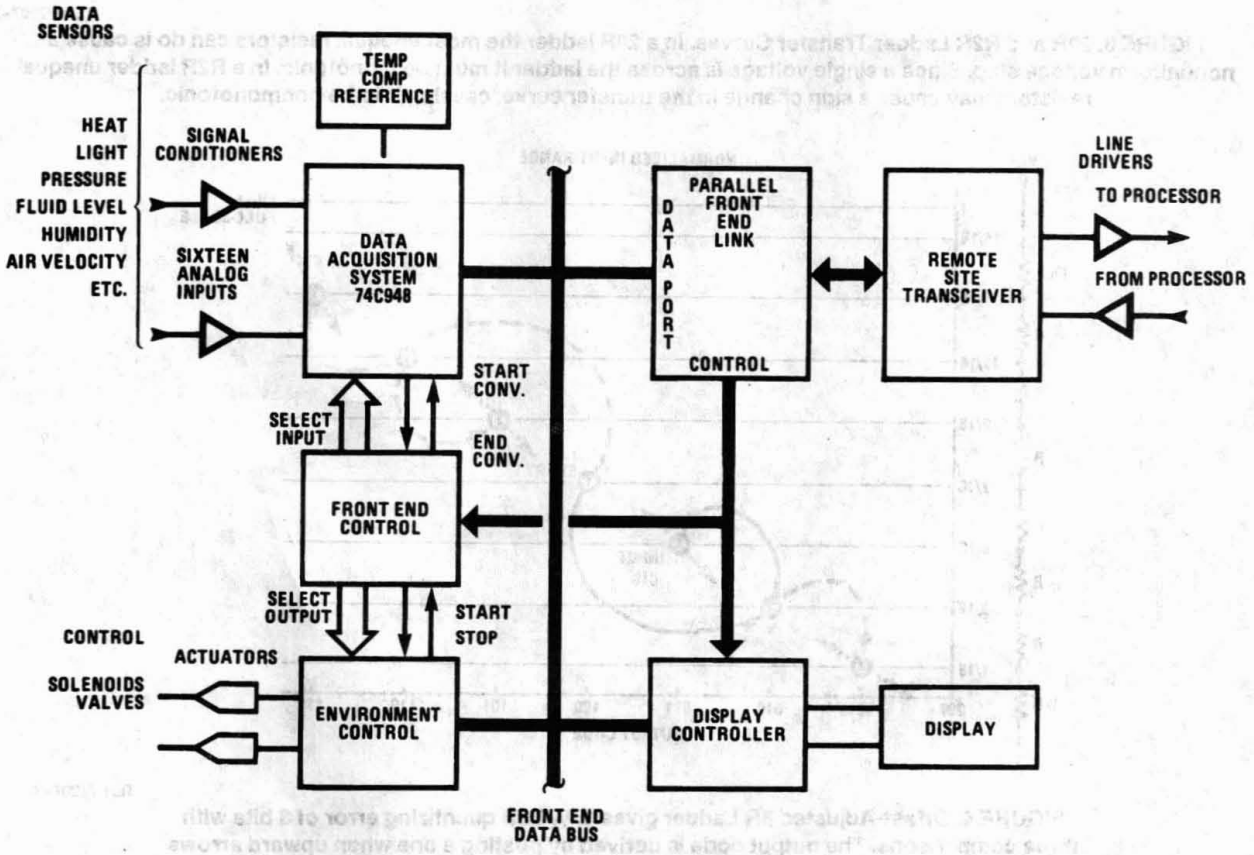
The 256R ladder network approach was chosen over the conventional R/2R ladder because of its inherent monotonicity. Monotonicity is particularly important in closed-loop feedback control systems. A non-monotonic relationship can cause oscillations that could be catastrophic. Additionally, the 256R network does not cause load variations on the reference voltage.

Figure 3 shows a comparison of the output characteristic for the two approaches with a variation in the ladder resistance. In the 256R approach with unequal or shorted resistors the slope of the output transfer function cannot be different from the slope of the analog input. For the R/2R ladder network, mismatches in the resistor values can cause the slope of the output digital code to be different from the analog input signal.

The bottom resistor and the top resistor of the ladder network in *Figure 4* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs eight iterations to approximate the input voltage. For any SAR-type converter, n iterations are required for an n-bit converter. *Figure 4* shows a typical example of a 3-bit converter with an input voltage of 1/4 full-scale. Since the initial approximation at 7/16 of full-scale is too high, a zero is posted for the most significant bit (MSB). The second approximation is too low, therefore a one is posted for the second bit. The final approximation is determined to be too high, so a zero is posted for the least significant bit (LSB). In the ADC0816/MM74C948 the approximation technique is extended to eight bits using the 256R network.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the respectability of the device. A chopper stabilized comparator provides the most effective method of satisfying all the converter requirements.



TL/H/7207–2

FIGURE 2. Remote Environmental Control System

The chopper stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long-term drift, and input offset errors.

The design of this A/D converter has been optimized by incorporating the most desirable aspects of several conversion techniques. The ADC0816 offers high speed, high accuracy, low temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control.

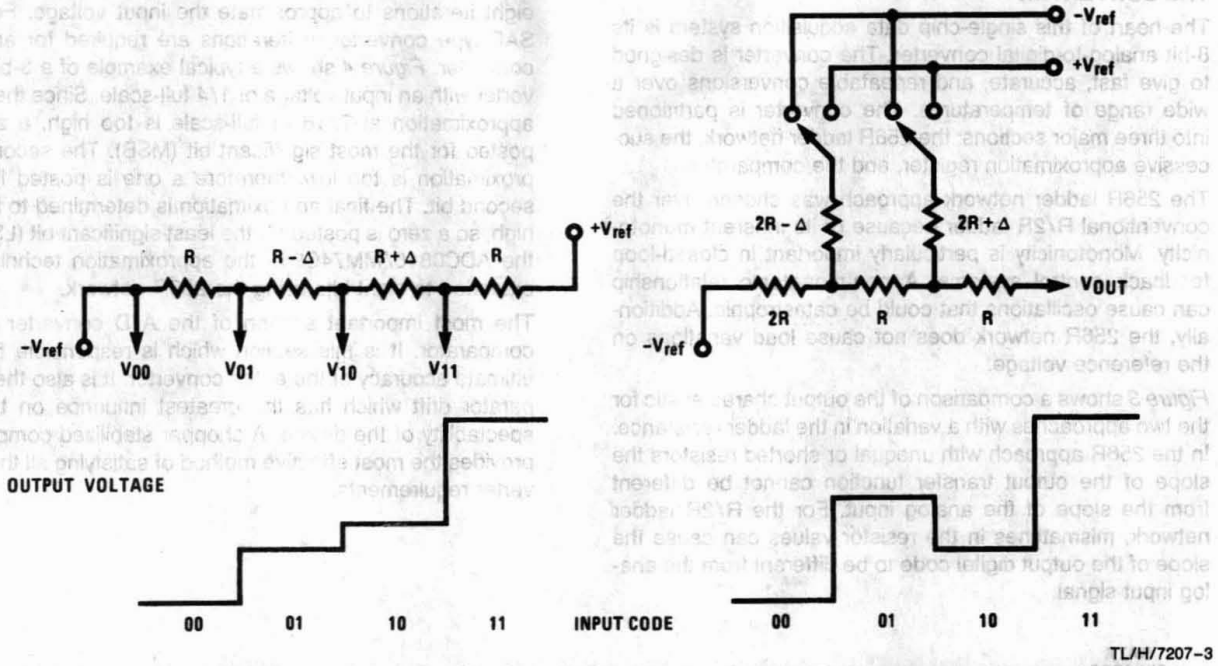


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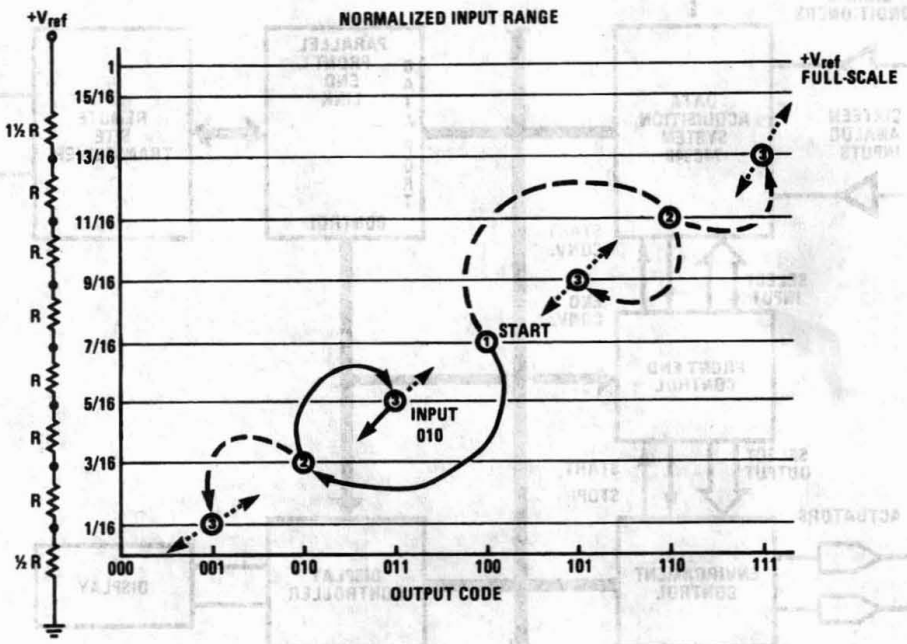
FIGURE 3. 2ⁿR and R2R Ladder Transfer Curves. In a 2ⁿR ladder the most unequal resistors can do is cause a nonuniform voltage step. Since a single voltage is across the ladder it must be monotonic. In a R2R ladder unequal resistors may cause a sign change in the transfer curve, causing it to be nonmonotonic.



TL/H/7207–4

FIGURE 4. Offset-Adjusted 8R Ladder gives ±½ LSB quantizing error of 3 bits with three comparisons. The output code is derived by posting a one when upward arrows are followed and a zero when downward arrows are followed to the input voltage.

CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor Systems

National Semiconductor
Application Note 200

SUMMARY

This paper describes techniques for interfacing National Semiconductor's new ADC3511 and ADC3711 microprocessor compatible analog-to-digital converter chips to 8080A microprocessor systems. The hardware interface and the software interrupt service routine will be described for single and multiple A/D converter data acquisition systems.

INTRODUCTION

The recent introduction of monolithic digital voltmeter chips has encouraged designers to consider their use as analog-to-digital converters in data acquisition systems. While the high accuracy afforded at low cost was attractive, certain difficulties in applying these devices in digital systems were encountered. Most of these difficulties were due to the DVM chip's output structure being oriented towards driving 7-segment displays with internally generated digit scanning rates. National Semiconductor has recently introduced a family of monolithic CMOS A/D converters—2 of these devices are directed towards LED display DPM and DVM applications (ADD3501 3 ½-digit DPM and ADD3701 3 ¾-digit DPM) while the other 2 (ADC3511 3 ½-digit A/D and ADC3711 3 ¾-digit A/D) have addressable BCD outputs. These last 2 devices allow easy interface to microprocessor and calculator-oriented (COPS) systems.

Single or multiple channel monitoring of physical variables can be achieved with high accuracy despite the lack of complexity and low overall cost.

A/D CONVERSION

All A/D converters in this family operate from a single 5V supply and convert inputs from 0 to ±2V. The converters use a pulse-width modulation technique which requires no precision components and exhibits low offset, low drift, high linearity and no rollover error. An additional advantage is that the voltage reference is of the same polarity as the supply.

Two resolutions are offered: the 3 ½-digit types divide the input into 2,000 counts plus sign, while the 3 ¾-digit types provide 4,000 counts plus sign which is roughly equivalent to the resolution of a 12-bit plus sign binary converter. The 3 ½-digit converters require 200 ms per conversion; 3 ¾-digit types require 400 ms.

The converters handle negative inputs by internally switching the inputs and forcing the sign bit low. While this technique allows conversion of positive and negative inputs with only a single supply, the supply must be isolated from the inputs. Without an isolated supply, only positive voltages may be converted.

The basic converter is shown in *Figure 1*. The actual conversion technique is described in Appendix A.

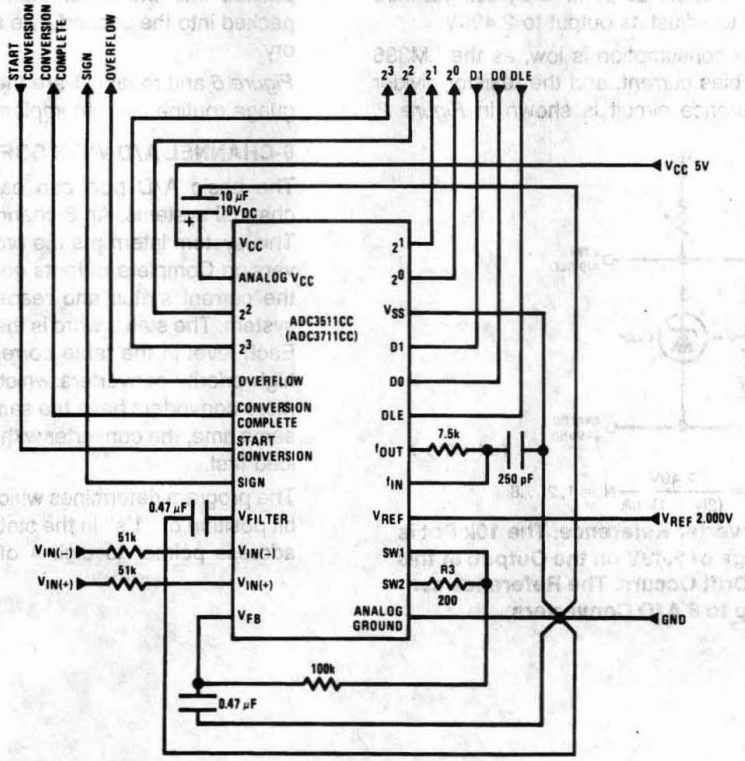


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FIGURE 1. Basic A/D Converter

BCD OUTPUT DESCRIPTION

The ADC3511 and ADC3711 present the output data in BCD form on a single 4-line output port, plus a separate sign output. The desired digit is selected by a 2-bit address which is latched by a high level at the Digit Latch Enable input (DLE); a low level at DLE allows flow thru operation. Since the output is BCD, it is compatible with many standard instruments and can easily be converted into binary by the processor if this format should be desired. Overrange inputs are indicated by a hexidecimal "EEEE" plus an Overflow output.

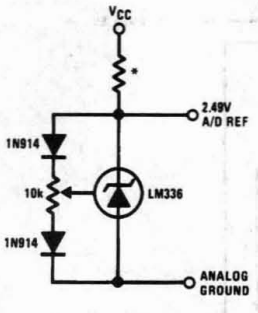
A new conversion is begun by a positive pulse or high level at the Start Conversion (SC) input. The analog section of the converter continuously tracks the analog input. The Start Conversion command controls only the transfer of new data to the output latches, consequently the delay from the SC pulse to the Conversion Complete (CC) signal may vary from several milliseconds to several hundred milliseconds. In interrupt driven systems the delay is no problem, since the processor does not execute delay instructions while waiting for the data. However, if in-line or program I/O is used where the program waits for the data to be ready, the maximum delay between SC and CC must be programmed into the wait routine. This type of I/O is therefore not as efficient as interrupt I/O.

The CC output goes low immediately after the SC pulse. At the end of a conversion, CC goes high and remains high until a new conversion is initiated. Continuous conversion operation is obtained by tying the SC input to V_{CC}.

REFERENCE VOLTAGE

The 2.000V reference is derived from the LM336, a recently announced monolithic reference which provides 2.5V with low drift at low cost. This active reference is adjusted for minimum thermal drift of about 20 ppm/°C by using a third terminal on the device to adjust its output to 2.490V.

Total reference current consumption is low, as the LM336 requires only 1 mA of bias current, and the resistor divider about 2 mA. The reference circuit is shown in *Figure 2*.



TL/H/5616–2

$$*R = \frac{2.49V}{(2N + 1)\ mA} \quad N = 1, 2 \ldots 8$$

FIGURE 2. A/D Converter Reference. The 10k Pot is Adjusted to a Voltage of 2.49V on the Output; at this Voltage Minimum Drift Occurs. The Reference can Supply up to 8 A/D Converters.

One reference can be used for many A/D's. The values of the upper series resistor R1 depends on the number of converters used.

A SINGLE CHANNEL CONVERTER

A complete A/D port is seen in *Figures 3* and *4*. *Figure 3* shows a Dual Polarity converter and *Figure 4* a Positive Only Polarity converter. Each port contains an A/D converter, TRI-STATE® bus driver, and 2 gates to control I/O. This A/D port is easily used in single or multi-channel systems. In multichannel systems a converter is used on every channel allowing digital multiplexing of the outputs.

Data from the A/D converter in a single channel system is easily processed using an OUT command to start a conversion and IN commands to read the data after the microprocessor has been interrupted by a Conversion Complete.

As seen in *Figure 5*, a single channel A/D port uses a 6-bit bus comparator to decode its assigned peripheral address from the lower address bits of the 8080A address bus.

When an interrupt is received, the present status of the processor is stored on the stack memory by a series of push commands. The interrupt is serviced by reading digit 4 (MSD) into the processor and checking the overflow bit. If the overflow bit is high, the converter input has exceeded its range and an error signal is generated, indicating that scaling must be done to attenuate the input signal. If the OFL is low, the sign bit is then checked to determine the polarity of the conversion. If the sign bit is low, a "1" is added to the MSB of digit 4. Since this bit would normally be low, (maximum converter range allows MSB $\leq$ 3 or 0011) a "1" in this position is used to denote a negative input voltage. The 4 bits of digit 4 which now include the sign are shifted into the upper half of the first byte and the 4 bits of digit 3 are packed into the lower half. Similarly, digits 2 and 1 are packed into the second byte and both bytes stored in memory.

Figure 6 and routine 1 are the flow chart and assembly language routine used to implement this action.

8-CHANNEL A/D WITH SOFTWARE PRIORITY

The basic A/D port can easily be expanded to multiple channel systems. An 8-channel system is seen in *Figure 7*. This system interrupts the processor when one of the Conversion Complete outputs goes high. The processor saves the current status and reads the status word of the A/D system. The status word is then compared to a priority table. Each level in the table corresponds to a priority level with high priority converters which are first in the table. If 2 or more converters have the same priority and are ready at the same time, the converter with the highest number gets serviced first.

The program determines which service routine to use by the bit position of "1's" in the status word. The routine loads the address pointer to digit 4 of the selected converter. The

program then calls a subroutine which goes through the process of checking overflow, sign and packs 4 BCD digits into 2 bytes. These 2 bytes are then stored in a table in the memory directly above the converter addresses. After a channel is serviced, the original processor status is restored and the interrupt enabled. If additional channels need service, they immediately interrupt so the new status word is then read and a new priority established.

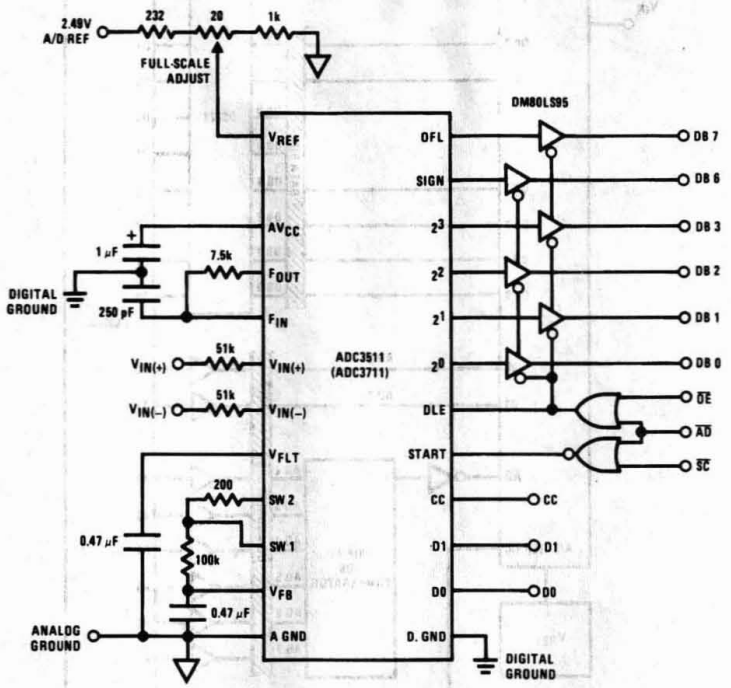


FIGURE 3. Dual Polarity A/D Requires that Inputs are Isolated from the Supply. Input Range Is ± 1.999V.

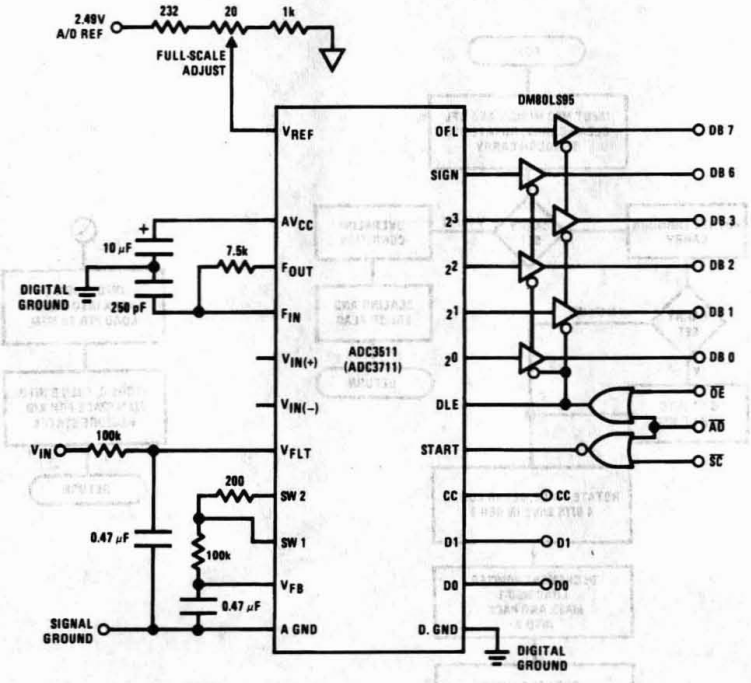


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FIGURE 4. Positive Polarity A/D Operating from 5V Supply. Input Range Is + 1.999V.

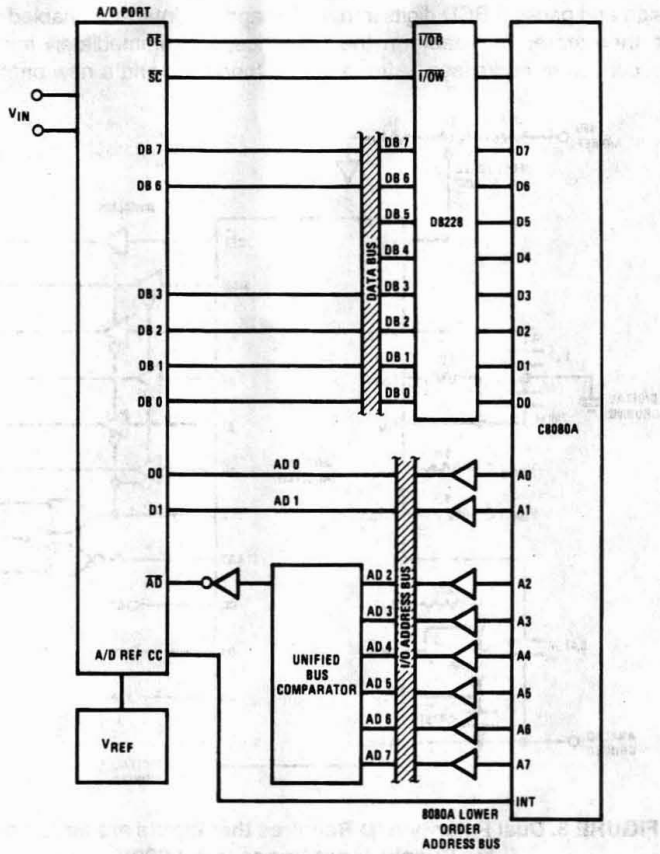
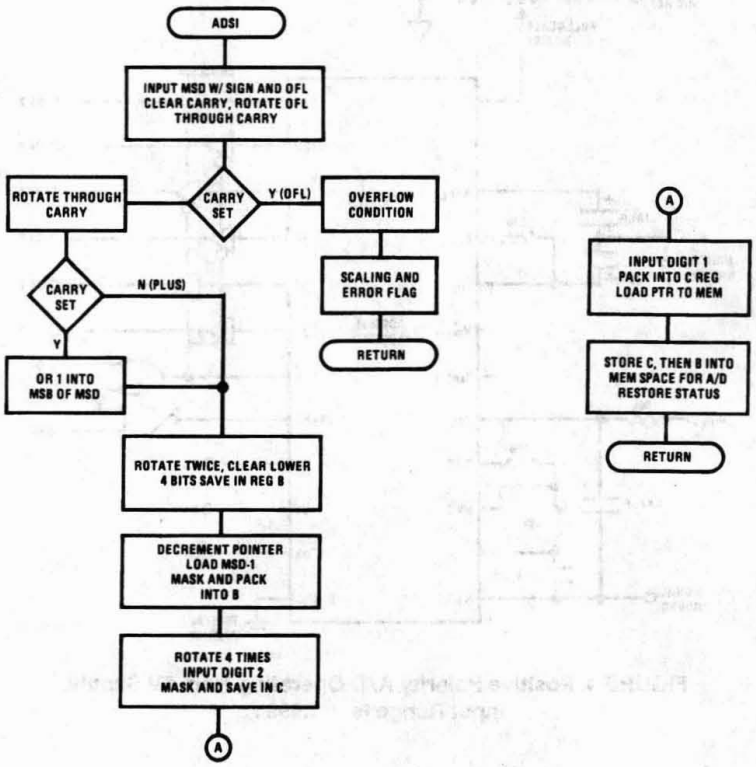


FIGURE 5. Single Channel A/D Interface with Peripheral Mapped I/O


ADSI
INPUT MSD W/ SIGN AND OFL CLEAR CARRY, ROTATE OFL THROUGH CARRY
ROTATE THROUGH CARRY
CARRY SET
Y (OFL)
OVERFLOW CONDITION
SCALING AND ERROR FLAG
RETURN
CARRY SET
N (PLUS)
Y
OR 1 INTO MSB OF MSD
ROTATE TWICE, CLEAR LOWER 4 BITS SAVE IN REG B
DECREMENT POINTER LOAD MSD-1 MASK AND PACK INTO B
ROTATE 4 TIMES INPUT DIGIT 2 MASK AND SAVE IN C
A
A
INPUT DIGIT 1 PACK INTO C REG LOAD PTR TO MEM
STORE C, THEN B INTO MEM SPACE FOR A/D RESTORE STATUS
RETURN

TL/H/5616–4

FIGURE 6. Flow Chart for Single Channel A/D Converter

Routine 1. Single Channel Interrupt Service Routine

LABEL	OPCODE	OPERAND	COMMENT
ADIS:	PUSH	PSW	; A/D interrupt service
	PUSH	H	; save
	PUSH	B	; current status
	IN	ADD 4	; input A/D digit 4
	IN	ADD 4	; delay
	ORA		; reset carry
	RAL		; rotate OFL thru carry
	JC	OFL	; overflow condition
	RAL		; rotate sign thru carry
	JC	PLUS	; positive input
	ORI	20H	; OR 1 into MSB, neg input
PLUS:	RAL		; shift
	RAL		; into position
	ANI	FO	; mask lower bits
	MOV	BA	; save in B
	IN	ADD 3	; input digit 3
	IN	ADD 3	; delay
	ANI	OF	; mask higher bits
	OR	B	; pack into B
	MOV	B, A	; save in B
	IN	ADD 2	; input digit 2
	IN	ADD 2	; delay
	RAL		; rotate
	RAL		; into
	RAL		; upper
	RAL		; 4 bits
	ANI	FO	; mask lower bits
	MOV	C, A	; save in C
	IN	ADD 1	; in digit 1
	IN	ADD 1	; delay
	ANI	OF	; mask upper bits
	OR	C	; pack
	MOV	C, A	; save in C
	LXI	H, ADMS	; load ptr to A/D ; Mem, space
	MOV	M, C	; save C in memory
	INX	H	; point next
	MOV	M, B	; save B in memory
	OUT	ADD 1	; start new conversion
	POP	B	; restore
	POP	H	; previous
	POP	PSW	; status
	EI		; enable interrupts
	RET		; return to main program

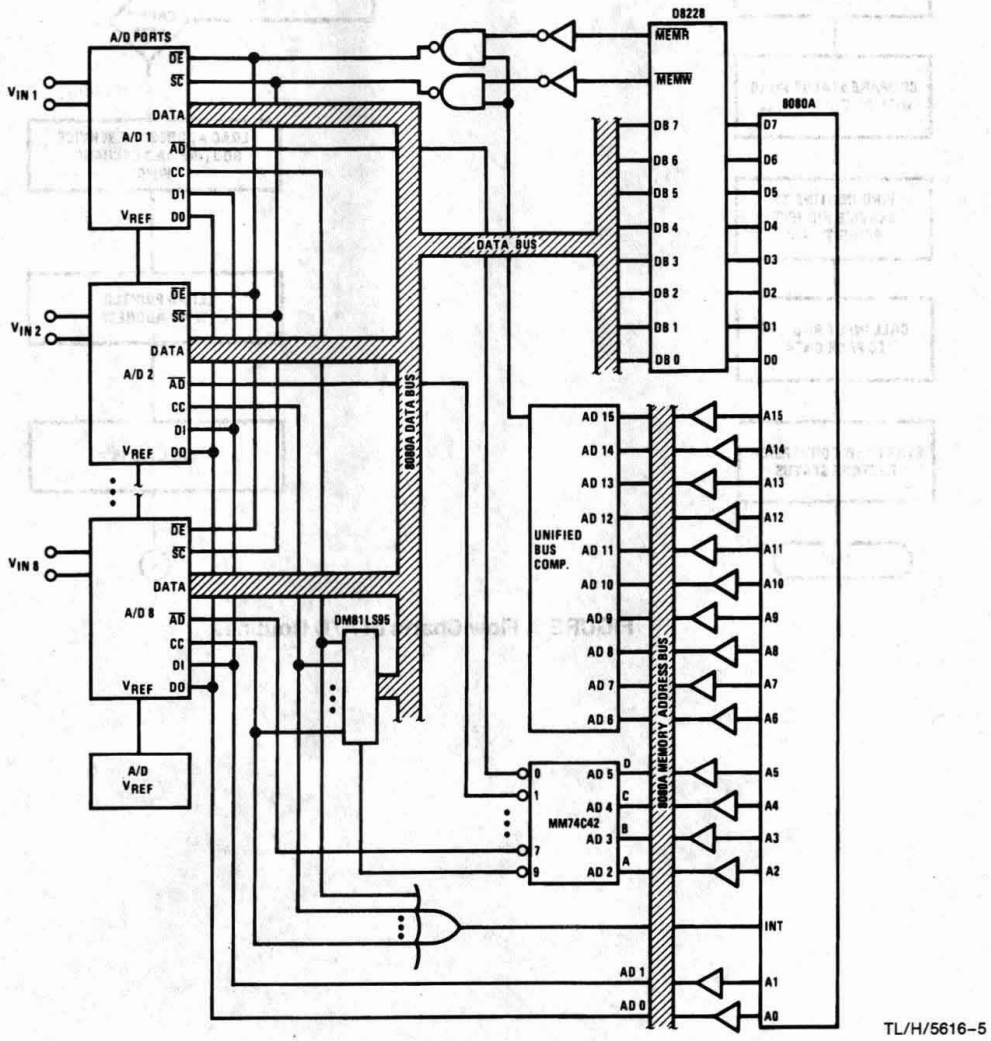
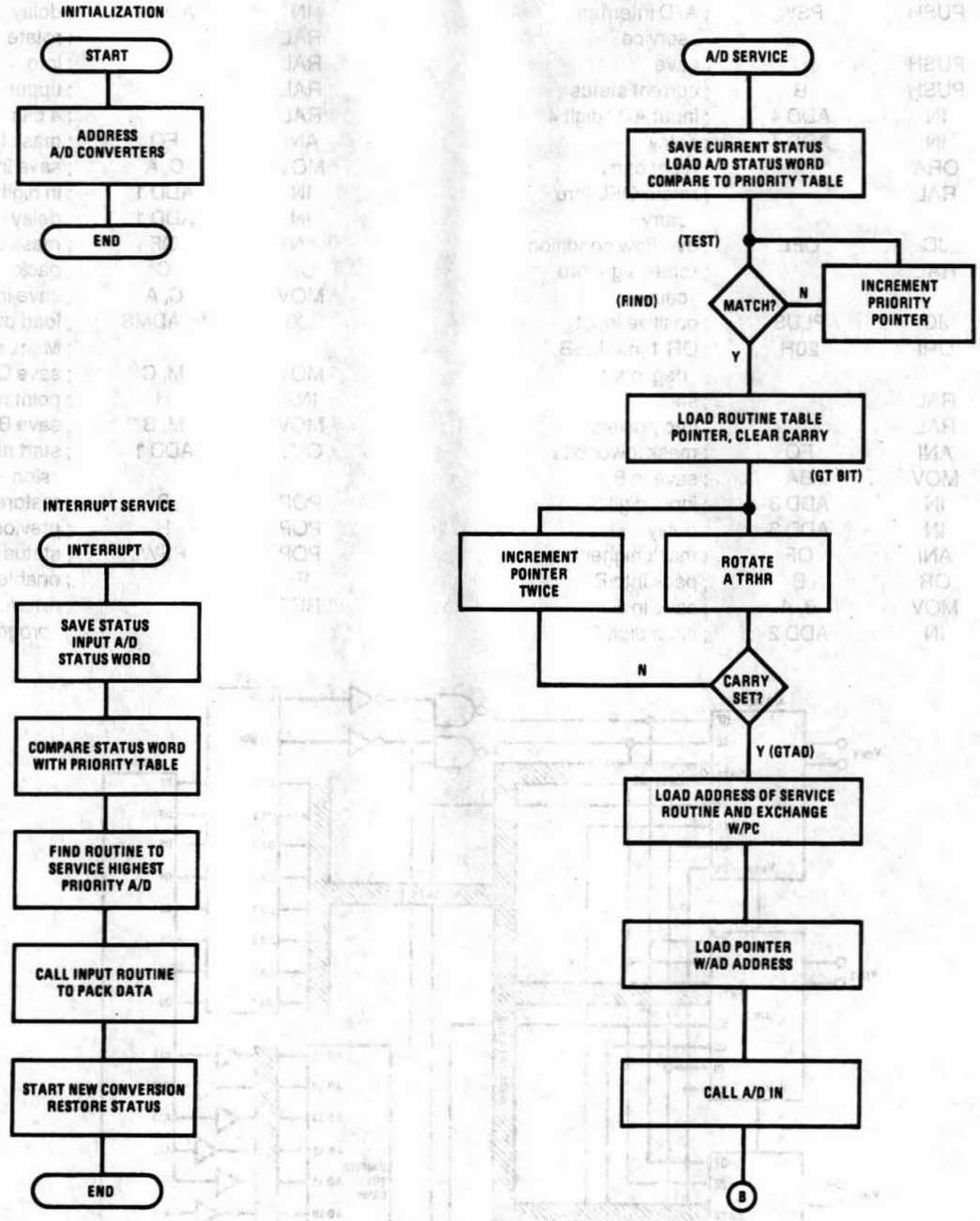
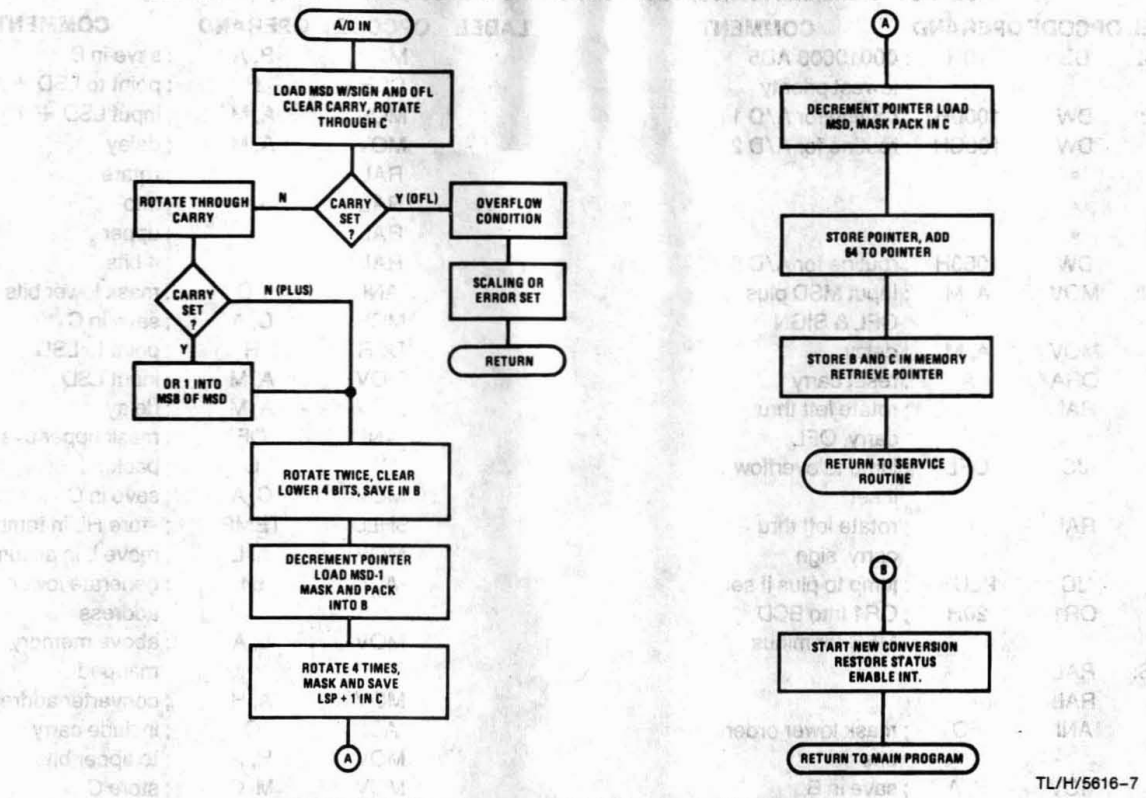


FIGURE 7. 8-Channel A/D System with Maskable Priority Interrupt Using Memory Mapped I/O



TL/H/5616–6

FIGURE 8. Flow Charts of A/D Routines


A/D IN
LOAD MSD W/SIGN AND OFL CLEAR CARRY, ROTATE THROUGH C
ROTATE THROUGH CARRY
N
CARRY SET ?
Y (OFL)
OVERFLOW CONDITION
SCALING OR ERROR SET
RETURN
CARRY SET ?
N (PLUS)
Y
OR 1 INTO MSB OF MSD
ROTATE TWICE, CLEAR LOWER 4 BITS, SAVE IN B
DECREMENT POINTER LOAD MSD-1 MASK AND PACK INTO B
ROTATE 4 TIMES, MASK AND SAVE LSP + 1 IN C
A
A
DECREMENT POINTER LOAD MSD, MASK PACK IN C
STORE POINTER, ADD 64 TO POINTER
STORE B AND C IN MEMORY RETRIEVE POINTER
RETURN TO SERVICE ROUTINE
B
START NEW CONVERSION RESTORE STATUS ENABLE INT.
RETURN TO MAIN PROGRAM

TL/H/5616–7

FIGURE 8. Flow Charts of A/D Routines (Continued)

Routine 2. 8-Channel Interrupt Service Routine with Software Priority

```
LABEL   OPCODE   OPERAND    COMMENT
IAD:    PUSH     PSW        ; interrupt from A/D
        PUSH     H          ; save H & L on stack
        PUSH     B          ; save B & C on stack
        PUSH     D          ; save D & E on stack
        LXI      H, ADWD    ; pickup A/D status word
        MOV      6, M       ; move word into B
        LXI      H, PRTBL   ; pickup priority tbl pointer
TEST:   MOV      A, B       ; place status word in accum.
        ANA      M          ; mask with priority table
        JNZ      FIND       ; match jump to Find
        INX      H          ; point to lower priority
        JMP      TEST       ; try again
FIND:   LXI      H, RTBL    ; pickup routine tbl pointer
        ORA      A          ; reset carry
GTBIT:  RAR                 ; rotate thru carry
        JC       GTAD       ; bit was found
        INX      H          ; point to
        INX      H          ; next routine
        JMP      GTBIT      ; try again
GTAD:   MOV      E, M       ; move first byte into E
        INX      H          ; point to next byte
        MOV      D, M       ; move second byte into D
        XCGH                ; exchange DE, HL
        PCHL                ; jump to input routine
INAD1:  LXI      H, AD1     ; pickup pointer to A/D 1
        CALL     ADIN       ; call common input routine
        MOV      M, A       ; start new conversion
        JMP      DONE       ; all done
INAD2:  LXI      H, AD2     ; pickup pointer to A/D 2
        CALL     ADIN       ; call input routine
        MOV      M, A       ; start new conversion
        JMP      DONE       ; all done
        •
        •
        •
DONE:   POP      D          ; restore D
        POP      B          ; restore B
        POP      H          ; restore H
        POP      PSW        ; restore PSW
        EI                  ; enable interrupts
        RET                 ; return to main program
PRTBL:  DB       04H        ; 0000C100 AD3 highest priority
        DB       03H        ; 0000011 AD2 & AD1 next priority
```

Routine 2. 8-channel Interrupt Service Routine with Software Priority (Continued)

```
LABEL  OPCODE  OPERAND   COMMENT
PRTBL:   DB      10H     ; 00010000 AD5
                           lowest priority
RTBL:    DW      1000H   ; routine for A/D 1
         DW      100CH   ; routine for A/D 2
         •
         •
         •
         DW      1060H   ; routine for A/D 8
ADIN:    MOV     A, M    ; Input MSD plus
                           OFL & SIGN
         MOV     A, M    ; delay
         ORA     A       ; reset carry
         RAL             ; rotate left thru
                           carry, OFL
         JC      OFL     ; jump to overflow
                           if set
         RAL             ; rotate left thru
                           carry, sign
         JC      PLUS    ; jump to plus if set
         OR1     20H     ; OR1 into BCD,
                           MSB for minus
PLUS:    RAL
         RAL
         ANI     FO      ; mask lower order
                           bits
         MOV     B, A    ; save in B
         DCR     H       ; point to MSD-1
         MOV     A, M    ; input MSD-1
         MOV     A, M    ; delay
         ANI     OF      ; mask higher 4 bits
         OR      B       ; pack MSD and MSD-1
         MOV     B, A    ; save in B
         DCR     H       ; point to LSD + 1
         MOV     A, M    ; input LSD + 1
         MOV     A, M    ; delay
         RAL             ; rotate
         RAL             ; into
         RAL             ; upper
         RAL             ; 4 bits
         ANI     FO      ; mask lower bits
         MOV     C, A    ; save in C
         DCR     H       ; point to LSD
         MOV     A, M    ; input LSD
         MOV     A, M    ; delay
         ANI     OF      ; mask upper bits
         OR      C       ; pack
         MOV     C, A    ; save in C
         SHLD    TEMP    ; store HL in temp
         MOV     A, L    ; move L in accum.
         ACI     64      ; generate lower
                           address
         MOV     L, A    ; above memory
                           mapped
         MOV     A, H    ; converter addresses
         ACI     O       ; include carry
         MOV     H, A    ; to upper bits
         MOV     M, C    ; store C
         INX     H       ; then
         MOV     M, B    ; store B
         LHLD    TEMP    ; retrieve HL
         RET             ; return
```

ADJUSTMENT AND TESTING

Adjustment and testing of a single channel A/D is done by monitoring the memory space where the interrupt routine stores the data word. The microprocessor is forced to loop around a section of program with interrupts enabled. As the input voltage of the converter is changed, this data word should also change as the converter updates it. A precision voltage reference is connected to the input of the A/D and incremental voltage steps are applied. The A/D data word should also change according to the voltage steps.

At full-scale input voltage, the data word should be at its maximum value. If not, check the full-scale adjust on the A/D by adjusting it so the OFL bit goes high when the input is exactly 2.000V.

Multichannel systems are more difficult to check. Start by individually checking the full-scale adjustments so the converters overflow at 2.000V. Check the software priority routine by forcing all status bits of the status word high. This corresponds to all converters being ready at the same time, a very unlikely worst-case condition. The microprocessor should respond by outputting the address of all 4 digits of the A/D port with the highest priority along with the $\overline{\text{memR}}$ strobes, then with a $\overline{\text{memW}}$ strobe to start a new conversion. The next highest priority converter should then receive its addresses and $\overline{\text{memR}}$ strobes and so on down the line.

Once the priority routine has been debugged, each data word is monitored as the input to its converter is adjusted. Since a common input routine is used, once 1 channel operates, all the other channels should also.

Debugging may most easily be done by single stepping through the program at these critical areas. No timing problems should be encountered since the A/D port appears to be a standard peripheral or memory. In the ADC3511 and ADC3711 the desired output is merely addressed the same as a memory location.

The memory requirements of the interface depends, of course, on the complexity of the system. The single channel converter requires approximately 60 bytes of program storage plus 2 bytes for data storage and 4 peripheral addresses.

The multichannel system requires about 40 bytes for the priority routine and 10 bytes of program for each converter routine. The common input routine requires about 50 bytes of program and is used by all the converter routines in the form of a subroutine.

Memory mapped I/O causes 64 memory locations to be used to input an 8-channel system. The data space is located directly above the address space for the converters and 16 memory locations are used to store the data for 8 converters.

CONCLUSION

The ADC3511 and ADC3711 microprocessor compatible A/D converters eliminate the difficulties previously encountered in applying DPM chips to microprocessor systems. The low parts count and low cost per channel make distributed or remote A/D conversion practical for a variety of data acquisition applications.

APPENDIX A

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure A1*. The output of SW 1 is either at V_{REF} or 0V, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high, then V_{OUT} will equal $_{REF}$ (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge, the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V, the comparator output will switch high. On the rising edge of the next clock, the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW 1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The low pass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

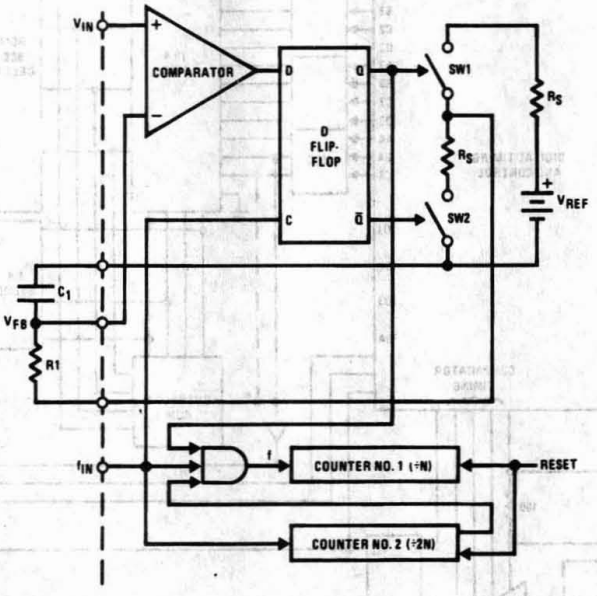
$$f = \text{(duty cycle)} \times (f_{IN})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{count} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.

For the ADC3711 N = 4000.



TL/H/5616–8

$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE A1. Analog Loop Schematic Pulse Modulation A/D Converter

Electrical Characteristics

ADC3511CC, ADC3711CC 4.75 ≤ V_{CC} ≤ 5.25V; −40°C ≤ T_A +85°C, f=5 conv./sec (ADC3511CC): 2.5 conv./sec (ADC3711CC); unless otherwise specified.

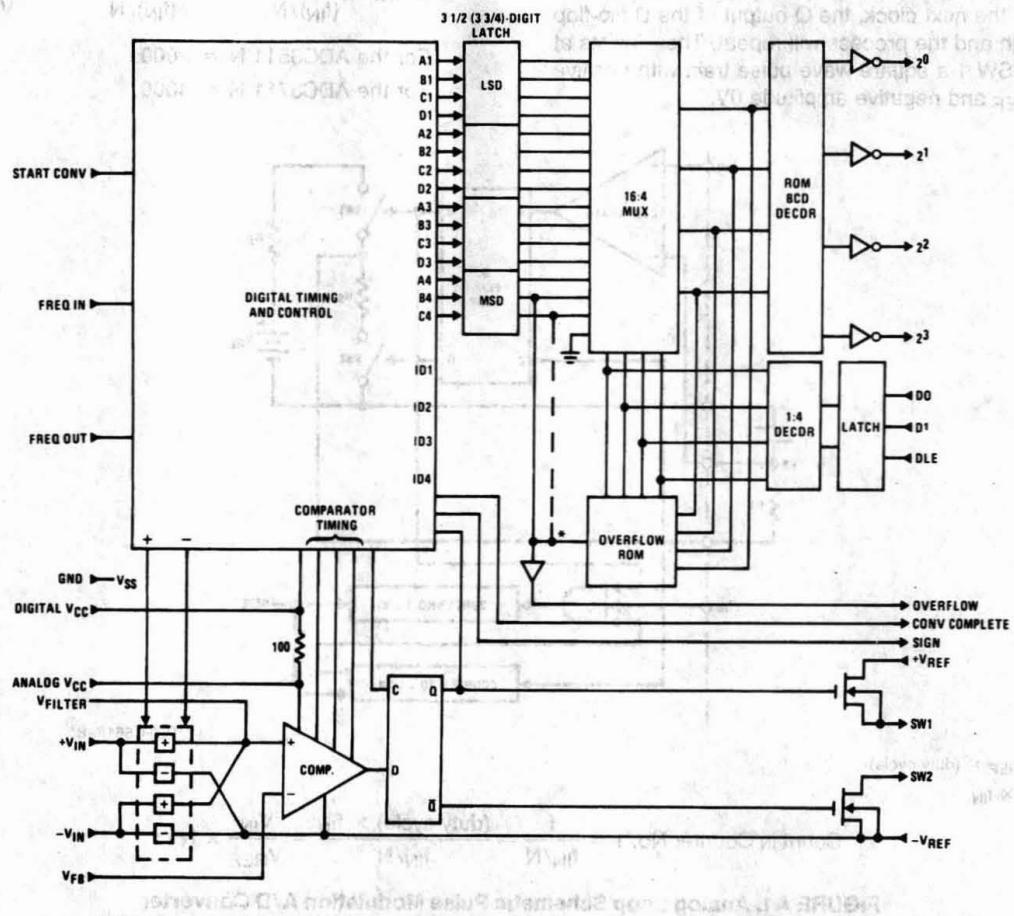
Parameter		Conditions	Min	Typ (Note 2)	Max	Units
	Non-Linearity	(Note 3) V_{IN} = 0−2V Full-Scale V_{IN} = 0−200 mV Full-Scale	−0.05	+0.025	0.05	% of Full-Scale
	Organization Error		−1		0	Counts
	Offset Error	V_{IN} = 0V, (Note 4)	−0.5	1.0	3.0	mV
	Rollover Error		−0		0	Counts
V_{IN}+, V_{IN}−	Analog Input Current	T_A=25°C	−5	1	5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore, 0.025% of full-scale = ½ counts and 0.05% of full-scale = 1 count. For the ADC3711CCL: full-scale = 3999 counts; therefore, 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 counts.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.



TL/H/5616–9

FIGURE A2. ADC3511 3½-Digit A/D (*ADC3711 3 ¾-Digit A/D) Block Diagram

A Digital Multimeter Using the ADD3501

National Semiconductor
Application Note 202

INTRODUCTION

National Semiconductor's ADD3501 is a monolithic CMOS IC designed for use as a 3 ½-digit digital voltmeter. The IC makes use of a pulse-modulation analog-to-digital conversion scheme that operates from a 2V reference voltage, functions with inputs between 0V and ±1.999V and operates from a single supply.

The conversion rate is set by an external resistor/capacitor combination, which controls the frequency of an on-chip oscillator. The ADD3501 directly drives 7-segment multiplexed LED displays, aided only by segment resistors and external digit buffers. The ADD3501 blanks the most significant digit whenever the MSD is zero; and, during overrange conditions, the display will read either +OFL or −OFL (depending on the polarity of the input.)

These characteristics make the ADD3501 suitable for use in low-cost instrumentation. An example of such use is the inexpensive, accurate, digital multimeter (DMM) presented here—an instrument that measures AC and DC voltages and currents, and resistance.

CIRCUIT DESCRIPTION

Figure 1 shows the circuit diagram of the ADD3501-based DMM, and Table I summarizes its measurement capabilities. Since the accuracy of the ADD3501 is ±0.05%, the DMM's performance is mainly determined by the choice of discrete components.

Supporting the ADD3501 is a DS75492 digit driver, an NSB5388 LED display, and an LM340 regulator for the V_{CC} supply. A 2V reference voltage—derived from the LM336 reference-diode circuitry—permits the 3 ½-digit system a 1 mV/LSD resolution (i.e., the ADD3501's full-scale count of 1999 or 1999 mV).

DC Voltage Measurement. The DMM's user places the (+) and (−) probes across the voltage to be measured, and sets the voltage range switch as necessary. This switch scales the input voltage, dividing it down so that the maximum voltage across the ADD3501's V_{IN} and V_{IN}—pins is limited to 2V full-scale on each input range. The ADD3501 performs an A/D conversion, and displays the value of the DMM's input voltage. The instrument's input impedance is at least 10 MΩ on all DC voltage ranges. Except for the 2V range, the DMM's survival voltage—the maximum safe DC input—is in excess of 1 kV. On the 2V range, the maximum allowable input is 700V.

AC Voltage Measurement. Switching the DMM to its AC VOLTS mode brings the circuit of *Figure 2* into function. This circuit operates as an averaging filter to generate a DC output proportional to the value of the rectified AC input; this value, in turn, is "tapped down" by R5 to a level equivalent to the input's rms value, which is the value displayed by the DMM.

Op amp A3 is simply a voltage follower that lowers the input-attenuator's source impedance to a value suitable to drive into A4. This impedance conversion helps eliminate some of the possible offset-voltage problems (the A4 input-offset-current source impedance IR drop, for example) and noise susceptibility problems as well. C1 blocks the DC offset voltage generated by A3.

A4 and A5 comprise the actual AC-to-DC converter; to see how it works refer again to *Figure 2*, and consider first its operation on the negative portion of an AC input signal. At the output of A4 are 2 diodes, D1 and D2, which act as switches. For a negative input to A4's inverting input, D1 turns on and clamps A4's output to 0.7V, while D2 opens, disconnecting A4's output from A5's summing point (the inverting input). A5 now operates as a simple inverter: R2 is its input resistor, R5 its feedback resistor, and its output is positive.

Now consider what happens during the positive portion of an AC input. A4's output swings negative, opening D1 and closing D2, and the op amp operates as an inverting unity-gain amplifier. Its input resistor is R1, its feedback resistor is R3, and its output now connects to A5's summing point through R4. D2 does not affect A4's accuracy because the diode is inside the feedback loop.

A positive input to A4 causes it to pull a current from A5's summing point through R4 and D2; the positive input also causes a current to be supplied to the A5 summing point through R2. Because A4 is a unity-gain inverter, the voltage drops across R2 and R4 are equal, but opposite in sign. Since the value of R2 is double that of R4, the net input current at A5's summing point is equal to, but opposite, the current through R2. A5 now operates as a summing inverter, and yields—again—a positive output. (R6 functions simply to reduce output errors due to input offset currents.)

Thus, the positive and negative portions of the DMM's AC voltage input both yield positive DC outputs from A5. With C2 connected across R5 as shown, the circuit becomes an averaging filter. As already mentioned, the tap on R5 is set so that the circuit's DC output is equivalent to the rms value of the DMM's AC voltage input, which is the value converted and displayed by the ADD3501

DC Current Measurement. To make a DC current measurement, the user inserts the DMM's probes in series with the circuit current to be measured and selects a suitable scale. On any scale range, the DMM loads the measured circuit with a 2V drop for a full-scale input.* The ADD3501 simply converts and displays the voltage drop developed across the DMM's current-sensing resistor.

*This drop may be reduced to 200 mV; refer to the last section of this application note.

TECHNICAL SPECIFICATIONS

DC VOLTS	< ±1% ACCURACY
RANGES	2V, 20V, 200V, 2 kV
INPUT IMPEDANCE	2V RANGE, > 10MΩ 20V TO 2 kV RANGE, 10MΩ
AC RMS VOLTS	< ±1% ACCURACY
RANGES	2V, 20V, 200V, 2 kV (40 TO 5 kHz SINEWAVE)
DC AMPS	< ±1% ACCURACY
RANGES	200 μA, 2mA, 20 mA, 200 mA, 2A
AC RMS AMPS	< ±1% ACCURACY
RANGES	200 μA, 2 mA, 20 mA, 200 mA, 2 A
OHMS	< ±1% ACCURACY
RANGES	200 Ω, 2 kΩ, 20 kΩ, 200 kΩ, 2 MΩ

Note 1: All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.

Note 2: All resistors are ¼ watt unless otherwise specified.

Note 3: All capacitors are ±10%.

Note 4: All op amps have a 0.1 μF capacitor connected across the V+ and V− supplies.

Note 5: All diodes are 1N914.

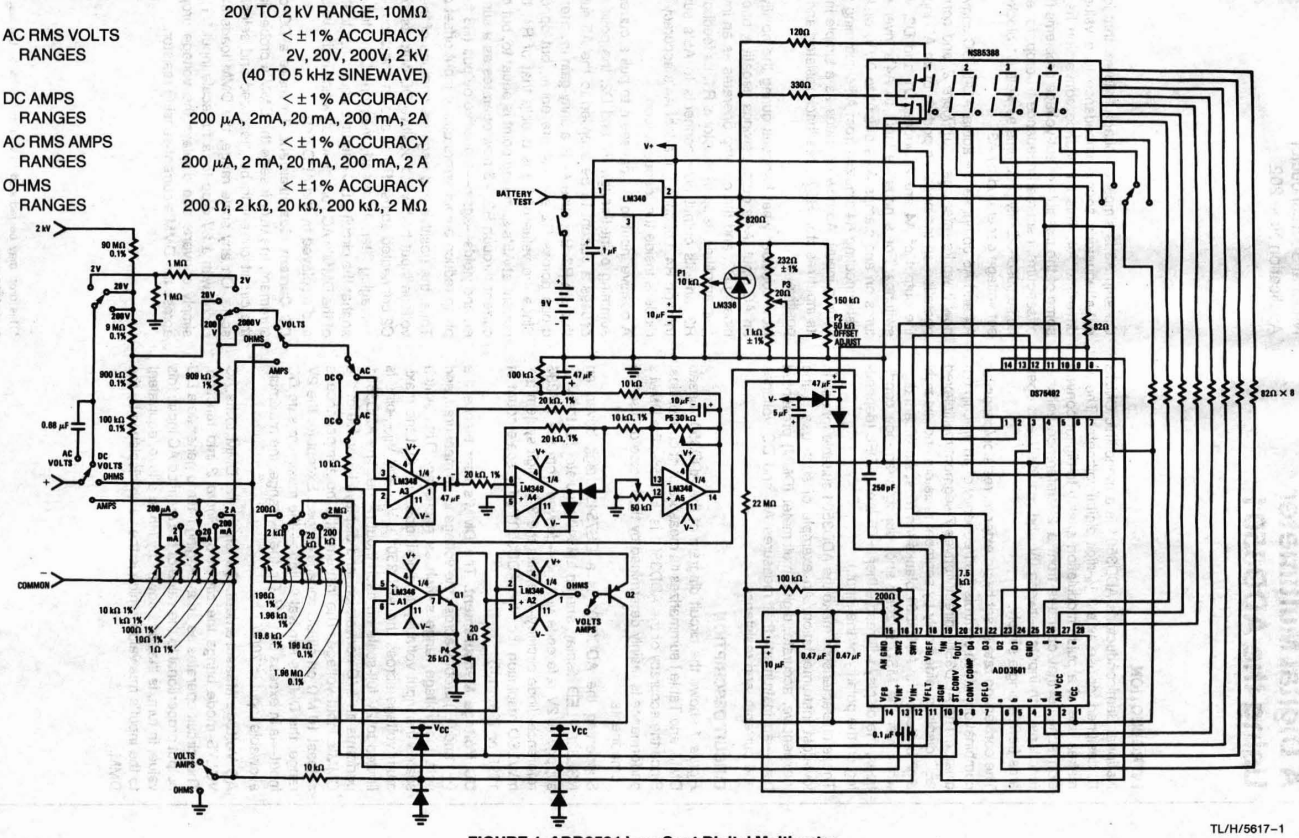


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FIGURE 1. ADD3501 Low Cost Digital Multimeter

AC Current Measurement. AC current measurements are made in a way similar to DC current measurements. The DMM is switched to its AMPS and AC settings. The in-circuit current is again measured by a drop across the DMM's current-sensing resistor, but now the AC voltage developed across this resistor is processed by A3, A4, and A5—exactly as described for AC voltage measurements—before being transferred to the ADD3501. Again, the DMM displays an rms value appropriate for the AC signal current being measured.

Resistance Measurement. This DMM measures resistance in the same way as do most multimeter: it measures the voltage drop developed across the unknown resistance by forcing a known, constant-current through it. Suitable scale calibration translates the voltage drop to a resistance value.

The resistance measurement requires the generation of a constant-current source that is independent of changes in V_{CC}, using the 2V, ground-referred reference voltage. The circuit of *Figure 3* accomplishes this.

In *Figure 3*, A1 establishes a constant-current sink by forcing node A to V_{REF}, the voltage level at A1's non-inverting input. With node A held constant at V_{REF} (2.000V), current through R2 is also fixed—since Q1's collector current is determined by the αI_E product—thus establishing V1 as

$$V1 = V_{CC} - \alpha(V_{REF}/R1)R2 \qquad (1)$$

Note that V_{REF} is derived from the LM336—a precision voltage source. Equation (1) shows, then, that (all else remaining constant) V1 varies directly with changes in V_{CC}; i.e., V1 tracks V_{CC}. The A1/Q1 pair thus establishes a voltage across R2 that floats, independent of changes in the ground-referenced potentials (V_{CC} and V_{REF}) that define it.

Now look at the A2/Q2 circuitry. The closed-loop operation of A2 tries to maintain a zero differential voltage between its input terminals. A2's non-inverting input is held at V1; thus, A2's inverting input is driven to V1. The current through R_L (Q2's emitter current) is therefore $(V_{CC} - V1)R_L$. Since V1 tracks V_{CC}, then $(V_{CC} - V1)$ - the voltage drop across R_L—is constant, thus producing I_{SOURCE} (*Figure 3*)—the constant source current needed for the resistance measurement.

Note, that varying R_X will not affect I_{SOURCE} so long as the voltage drop across R_X is less than $(V1 - V_{BE2})$. Should V_{RX} exceed $(V1 - V_{BE2})$, Q2 would saturate, invalidating the measurement. The ADD3501 eliminates this worry, however, because as soon as the drop across R_X equals or exceeds the 2V full-scale input voltage the ADD3501 will display an OFL condition.

Finally, SW1 (*Figure 3*) is required as part of the VOLTS/AMPS/OHMS mode selection circuitry; in the VOLTS/AMPS position it prevents Q2's base-emitter junction pulling the V− supply to ground through A2.

TABLE I. DMM PERFORMANCE

Measurement Mode	Range 0.2	2	2	200	2000	Frequency Response	Accuracy	Overrange Display
DC Volts	—	V	V	V	V	—	≤ 1% F.S.	± OFLO
AC Volts	—	V_{RMS}	V_{RMS}	V_{RMS}	V_{RMS}	40 Hz to 5 kHz	≤ 1% F.S.	+ OFLO
DC Amps	mA	mA	mA	mA	mA		≤ 1% F.S.	± OFLO
AC Amps	mA_{RMS}	mA_{RMS}	mA_{RMS}	mA_{RMS}	mA_{RMS}	40 Hz to 5 kHz	≤ 1% F.S.	+ OFLO
Ohms	kΩ	kΩ	kΩ	kΩ	kΩ	—	≤ 1% F.S.	+ OFLO

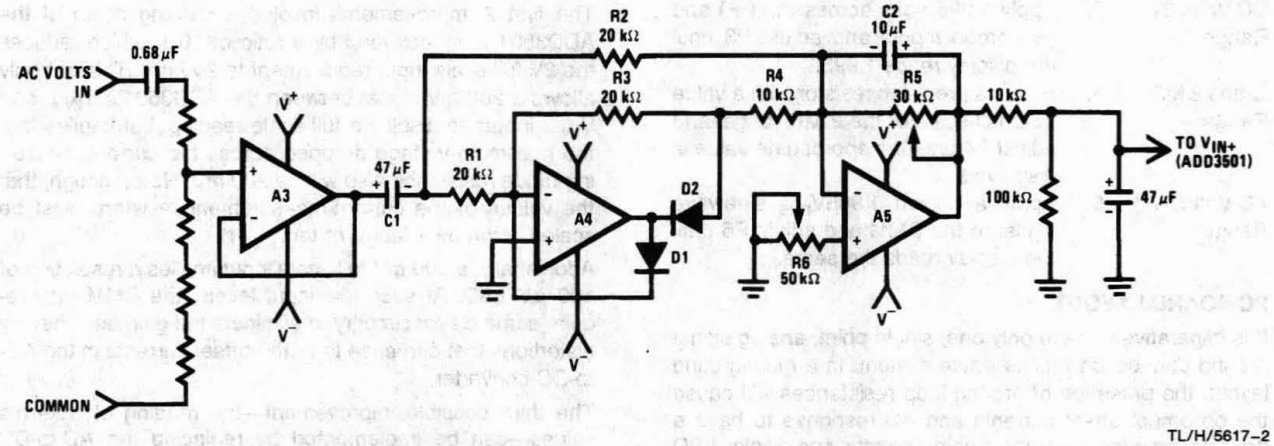

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FIGURE 2. AC/DC Converter

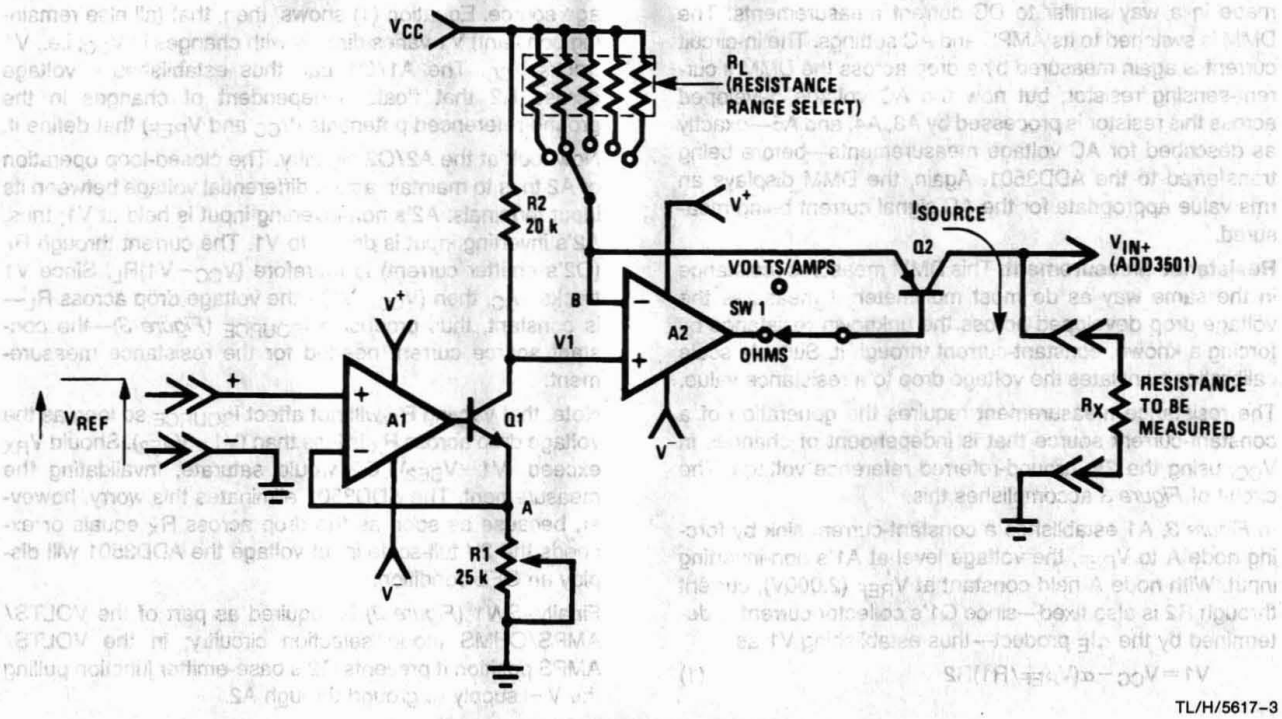

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FIGURE 3. Constant-Current Source

CALIBRATION

Calibrate the DMM according to the following sequence of operations:

1. Adjust P1 until the cathode voltage of the reference diode, LM336, equals 2.49V. This reduces the diode's temperature coefficient to its minimum value.

DC Volts 2V Range

2. Short the (+) and (−) probe inputs of the ADD3501 and adjust P2 until the display reads 0000.

DC Volts 2V Range

3. Apply 1.995 volts across the (+) and (−) probe inputs and adjust P3 until the display reads 1.995.

Ohms 2 MΩ Range

4. Select a precision resistor with a value near full-scale or the 2 MΩ range, and adjust P4 until the appropriate value is displayed.

AC Volts 2V Range

5. Apply a known $1.995V_{rms}$ sinewave signal to the DMM and adjust P5 until the display reads the same.

PC BOARD LAYOUT

It is imperative to have only one, single-point, analog signal ground connection for the entire system. In a multi-ground layout, the presence of ground-loop resistances will cause the op amps' offset currents and AC response to have a devastating effect on system gain, linearity, and display LSD flicker. Similar precautions must also be taken in the layout of the analog and high-switching-current (digital) paths of the ADD3501.

A FINAL NOTE

The digital multimeter described in this note was developed with the goals of accuracy and low cost. For the high-end DMM market segments, however, improvements to the basic circuit of *Figure 1* are possible in the following areas:

1. Expand the VOLTS mode to include a 200 mV full-scale range;
2. Decrease the full-scale current-measurement loading voltage from 2V to 200 mV; and,
3. Provide a true-rms measurement capability.
4. Increase resolution by substituting the ADD3701—3 ¾-digit DVM chip—which is interchangeable and provides a maximum display count of 3.999.

The first 2 improvements involve a dividing down of the ADD3501 feedback loop by a ratio of 10:1, which reduces the 2V full-scale input requirement to 200 mV. This not only allows a 200 mV signal between the ADD3501's V_{IN+} and V_{IN-} inputs to display a full-scale reading, but implies that the maximum voltage dropped across the current-measuring-mode resistance also will be 200 mV. Note, though, that the values of the current-measurement resistors must be scaled down by a factor of ten.

Additionally, a 200 mV full-scale input implies a resolution of 100 μV/LSD. At such low input levels, the DMM may require some clever circuitry to eliminate the gain and linearity distortions that can arise from the offset currents in the AC-to-DC converter.

The third possible improvement—the reading of true-rms values—can be implemented by replacing the AC-to-DC converter of *Figure 2* with National's LH0091, a true-rms-to-DC converter, and appropriate interface circuitry.

REFERENCES:

1. ADD3501 Data Sheet.
2. LH0091 Data Sheet.
3. LM336 Data Sheet.
4. Application Note AN-20.
5. ADD3701 Data Sheet.

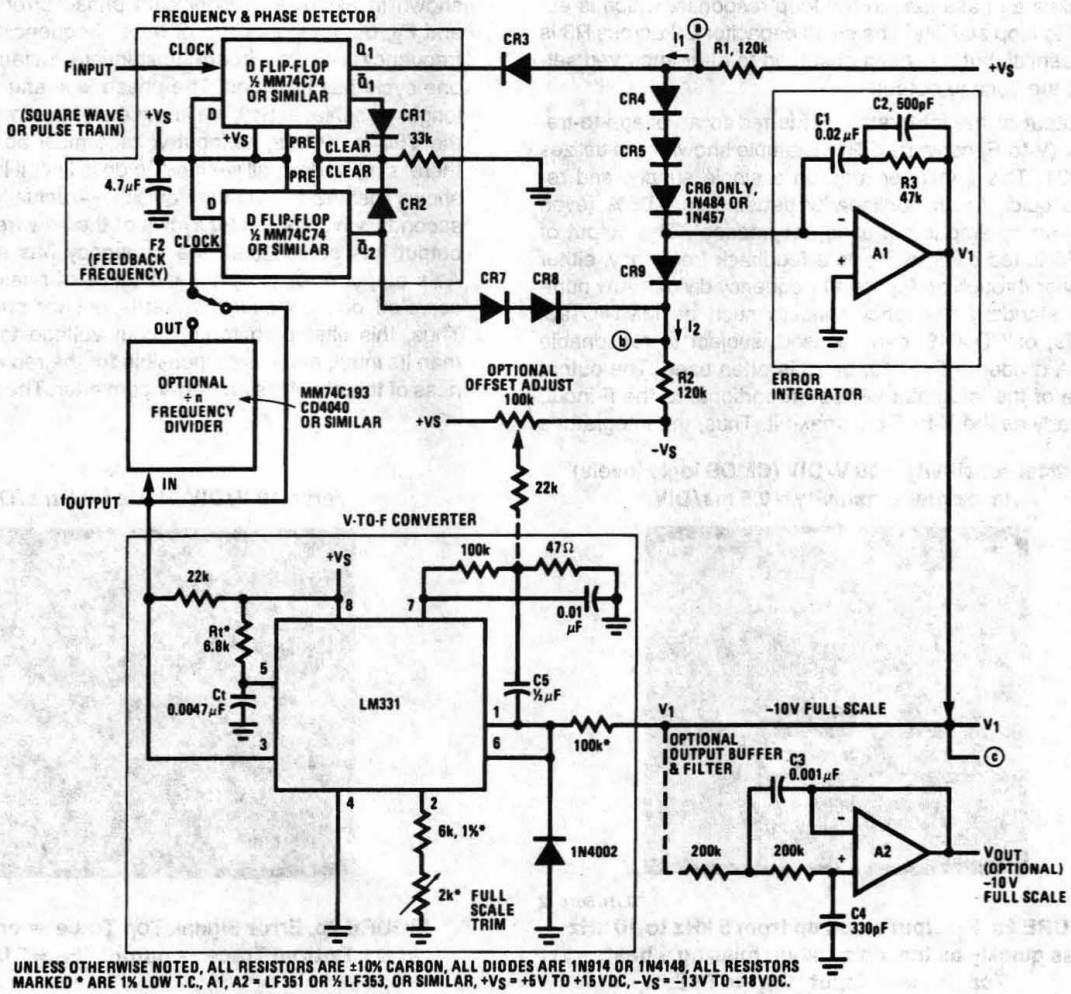
New Phase-Locked-Loops Have Advantages as Frequency to Voltage Converters (and more)

National Semiconductor
Application Note 210
Robert Pease

A phase-locked-loop (PLL) is a servo system, or, in other words, a feedback loop that operates with frequencies and phases. PLL's are well known to be quite useful (powerful, in fact) in communications systems, where they can pluck tiny signals out of large noises. Here, however, we will discuss a new kind of PLL which cannot work with low-level signals immersed in noise, but has a new set of advantages, instead. It does require a clean noise-free input frequency such as a square wave or pulse train.

This PLL can operate over a wide frequency range, not just 1 or 2 octaves but over 1 or 2 or 3 decades. It naturally provides a voltage output which responds quickly to frequency changes, yet does not have any inherent ripple. Thus, it can be used as a frequency-to-voltage (F-to-V) converter which does not have any of the classical limitations or compromises of (large ripple) vs (slow response), which most F-to-V converters have.[1] The linearity of this F-to-V converter will be as good as the linearity of the V-to-F converter used, and this linearity can easily be better than 0.01%. Other advantages will be apparent as we study the circuit further.

The basic circuit shown in *Figure 1* has all the functional blocks of a standard PLL. The frequency and phase detection do not consist of a quadrature detector, but of a standard dual-D flip-flop. When the frequency input is larger than F_2, Q1 will be forced high a majority of the time, and provide a positive error signal (via CR3, 4, 5, and 6) to the integrator.



UNLESS OTHERWISE NOTED, ALL RESISTORS ARE ±10% CARBON, ALL DIODES ARE 1N914 OR 1N4148, ALL RESISTORS MARKED * ARE 1% LOW T.C., A1, A2 = LF351 OR ½ LF353, OR SIMILAR, $+V_S$ = +5V TO +15VDC, $-V_S$ = -13V TO -18VDC.

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FIGURE 1. Basic Wide-Range Phase-Locked Loop

1. Appendix C, "V/F Converter ICs Handle Frequency-to-Voltage Needs," National Semiconductor Linear Applications book.

If F input and F_2 are the same, but the rising edges of F input lead the rising edges of F_2, the duty cycle of Q1 = HI will be proportional to the phase error. Thus, the error signal fed to the integrator will decrease to nearly zero, when the loop has achieved phase-lock, and the phase error between F_{IN} and F_2 is zero. Actually, in this condition, Q1 will put out 30 nanosecond positive pulses, at the same time that Q2 puts out 30 nanosecond negative pulses, and the net effect as seen by the integrator is zero net charge. The 30 nanosecond pulses at Q1 and Q2 enable both flip-flops to be CLEARED, and prepared for the next cycle. This phase-detector action is substantially the same as that of an MC4044 Phase-Detector, but the MM74C74 is cheaper and uses less power. It is fast enough for frequencies below 1 MHz. (At higher frequencies, a DM74S74 can be used similarly, with very low delays.)

The error integrator takes in the current from R1 or R2, as gated by the Q1 and $\overline{Q2}$ outputs of the flip-flop. For example, when F_{IN} is higher, and Q1 is HIGH, I_1 will flow through CR4, 5, and 6 and cause the integrator's output to go more negative. This is the direction to make the V-to-F converter run faster, and bring F_2 up to F input. Note that A1 does not merely integrate this current in C1 (a mistake which many amateur PLL designers make). The resistor R3 in series with C1 makes a phase *lead* in the loop response, which is essential to loop stability. The small capacitor C2 across R3 is not essential, but has been observed to offer improved settling at the voltage output.

The output of the integrator, V1, is fed to a voltage-to-frequency (V-to-F) converter. The example shown here utilizes a LM331. This converter runs on a single supply, and responds quickly with nonlinearity better than 0.05% (even though an op-amp is not used nor needed). The output of the VFC is fed back to F_2, as a feedback frequency, either directly or through an (optional) frequency divider. Any number of standard frequency dividers such as MM74C193, CD4029, or CD4018, can be used, subject to reasonable limits. A divider of 2, 3, 10, or 16 is often used. The output voltage of the integrator will be proportional to the F input, as linearly as the V-to-F can make it. Thus, the integrator's output voltage V1 can be used as the output of an ultralinear F-to-V converter. However during the brief pulses when the flip-flop is CLEARing itself, there will be small glitches found on the output of A1. The RMS value of this noise may be very small, typically 0.5 to 5mV, but the peak amplitude, sometimes 10 to 100mV, can be annoying in some systems. And, no additional filtering can be added in the main loop's path, for any further delay in the route to the VFC would cause loop instability. Instead, the output may be obtained from a separate filter and buffer which operates on a branch path. A2 provides a simple 2-pole active filter (as discussed in Reference 1) which cuts the steady-state ripple and noise down below 1mV peak-to-peak an excellent level for such a quick F-to-V (as we shall see).

What is not obvious about A2 is that its output can settle (within a specified error-band such as ±10 millivolts from the final DC value) earlier and more quickly than A1's output. The waveforms in *Figure 2* show F_{IN} stepping up instantly from 5 kHz to 10 kHz; it also shows F_2 stepping up very quickly. The error signal at Q1 is also shown. The critical waveforms are shown in *Figure 3*, the outputs of A1 and A2. While A1 puts out large spikes (caused by I1 flowing through R3), these large spikes cause the V-to-F converter to jump from 5 kHz to 10 KHz without any delay. There is, as shown in Figure 2, a significant phase error between F_{IN} and F_2, but an inspection of these frequencies shows that frequency lock has been substantially instantaneous. Not one cycle has been lost The phase lock and settling takes longer to achieve. Still, we know that if the frequency out of the VFC is 10 kHz, its input voltage must be −10 VDC. If there is noise on it, all we have to do is filter it in A2. Figure 3 shows that A2 settles very quickly — actually, in 2.0 milliseconds, which is just 20 cycles of the new frequency. A2's output has settled (i.e., the frequency has settled). while A1's output error (which is indicative of phase error being servo'ed out) continues to settle out for another 12 ms. Thus, this filter permits its output voltage to settle faster than its input, and it is responsible for the remarkable quickness of this circuit as an F-to-V converter. The waveforms of

Vertical sensitivity = 10 V/DIV (CMOS logic levels)
Horizontal sensitivity = 0.5 ms/DIV

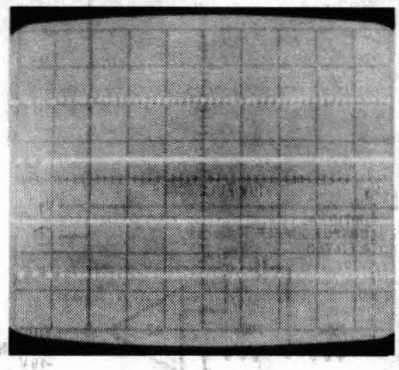

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FIGURE 2a. F output steps up from 5 kHz to 10 kHz as quickly as the input, never missing a beat.
Top Trace = input "F_{IN}" to PLL.
Bottom Trace = output "F_{OUT}" from PLL.

Vert = 10 V/DIV, Horiz = 0.5 ms/DIV

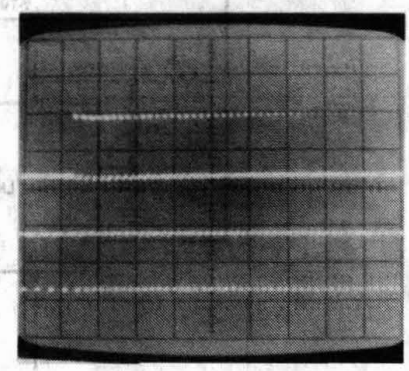

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FIGURE 2b. Error Signal. Top Trace = error signal at Q1. Bottom Trace = output "F_{OUT}" from PLL.

Figure 3 can be compared to the response (shown in *Figure 4)* of a conventional F-to-V converter. The upper trace is the output of a conventional FVC after a 4-pole filter[2], and the lower trace is the output of the circuit of *Figure 1*. The phase-locked-loop F-to-V converter is quicker yet quieter.

2. AN-207, V-to-F and F-to-V Converter Applications.

Vert = 2 V/DIV, Horiz = 2 ms/DIV

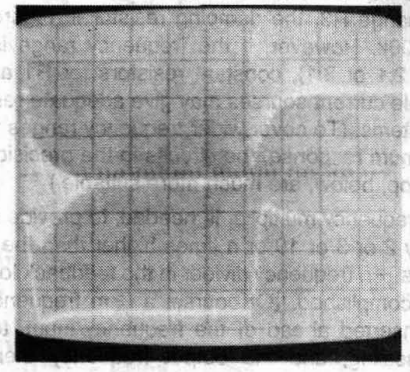

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FIGURE 3a. Settling waveforms, as F_{IN} goes from 5 kHz to 10 kHz and back again, using circuit of *Figure 1*. Top Trace = output of integrator (V1). Bottom Trace = output of filter (V_{OUT}).

Vert = 2 V/DIV, Horiz = 0.5 ms/DIV

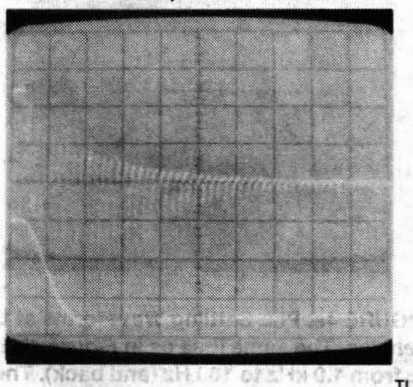

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FIGURE 3b. PLL Settling Waveforms. The same waveform as in *Figure 3a*, but time base is expanded to 0.5 ms/DIV to show fine detail of settling.

Vert = 2 V/DIV, Horiz = 20 ms/DIV

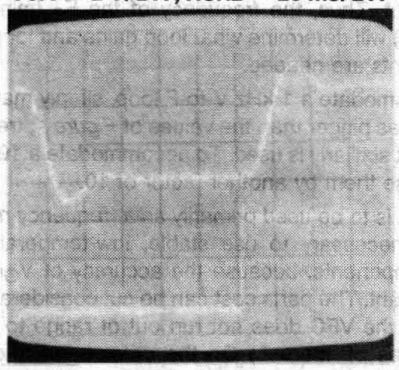

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FIGURE 4a. FVC Response vs PLL Response. The PLL can settle rather more quickly than a conventional F-to-V converter. Top Trace = conventional F-to-V converter with 4-pole active filter, responding to a 5 kHz to 10 kHz step. Bottom Trace = PLL FVC, with the same input, circuit of *Figure 1*.

Vert = 2 V/DIV, Horiz = 20 ms/DIV

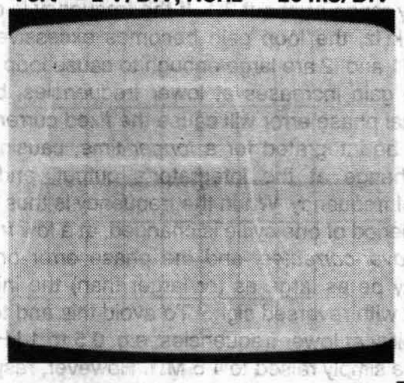

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FIGURE 4b. FVC Step Response. FIGURE 4b. This waveform is similar to that in *Figure 4a* but the frequency change covers a 10:1 ratio, from 10 kHz to 1 kHz and back to 10 kHz. For this waveform, the adaptive current sources of *Figure 5* connect to *Figure 1* (whereas for *Figure 4a* R1 = R2 = 120k).

Vert = 2 V/DIV, Horiz = 5 ms/DIV

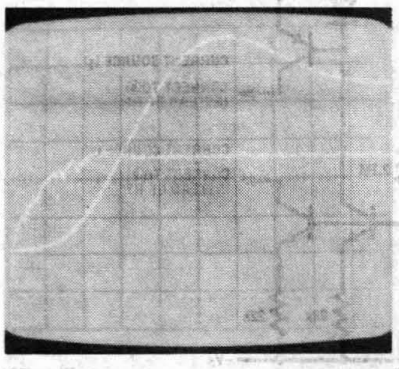

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FIGURE 4c. FVC Response. The same as *Figure 4b*, but time base expanded to 5 ms/DIV, to show detail of rise time. Top Trace = conventional FVC. Bottom Trace = PLL FVC.

Vert = 2 V/DIV, Horiz = 5 ms/DIV

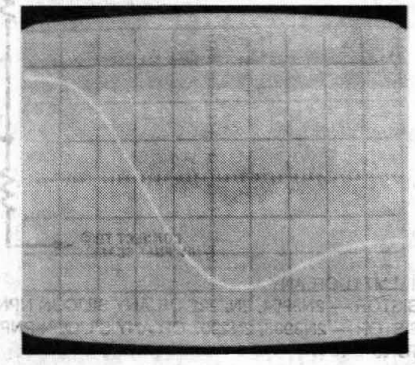

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FIGURE 4d. FVC Response The same as *Figure 4b*, but expanded to 5 ms/DIV to show details of fall time. Top Trace = conventional FVC. Bottom Trace = PLL FVC.

Vert = 0.2 V/DIV/, Horiz = 50 ms/DIV

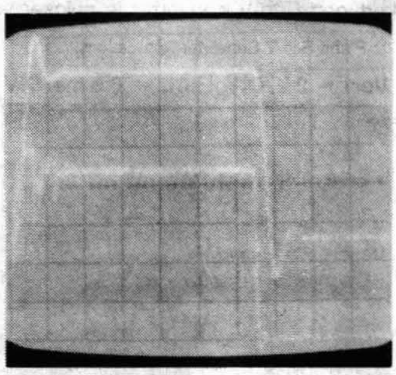

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FIGURE 4e. PLL Settling Waveforms at Low Frequencies. The same idea as in *Figure 4b*, but 10 × slower, from 1.0 kHz to 100 Hz (and back). The settling to 1 kHz is still distinctly faster for the PLL, but at 100 Hz, it is a bit slower. Still, the PLL is faster than the FVC at all speeds from 200 Hz to 10 kHz.

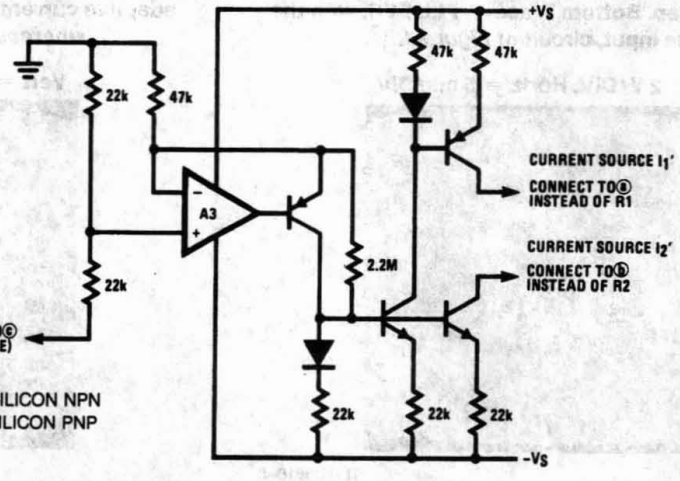
So far we have shown a PLL which operates nicely over a frequency range of about 3:1. If the frequency is decreased below 3 kHz, the loop gain becomes excessive, and the currents I1 and I2 are large enough to cause loop instability. The loop gain increases at lower frequencies, because a given initial phase error will cause the fixed current from R1 or R2 to be integrated for a *longer* time, causing a *larger* output change at the integrator's output, and a *larger* change of frequency. When the frequency is thus corrected, and the period of one cycle is changed, at a low frequency it may be *over-corrected,* and the phase error on the next cycle may be as large as (or larger than) the initial phase error, but with reversed sign.[3] To avoid this and to maintain loop stability at lower frequencies, e.g. 0.5 to 1 kHz, R1 and R2 can be simply raised to 1.5 MΩ. However, response to a step will be proportionally slower. To achieve a wide frequency range (20:1), and optimum quickness at all frequencies, it is necessary to servo I1 and I2 to be *proportional to the frequency.* Fortunately, as V1 is normally proportional to F, it is easy to generate current sources I1' and I2' which are proportional to F. The circuit of *Figure 5* can be connected to the basic PLL, instead of R1 and R2, and provides good, quick loop stability over a 30:1 frequency range, from 330 Hz to 10 kHz. For best results over a 30:1 frequency range, change R3, the damping resistor in Figure 1, from 47k to 100k. However, if the frequency range is smaller (such as 2:1 or 3:1), constant resistors for R1 and R2 or very simple current sources may give adequate response in many systems. (To cover wider frequency ranges than 30.1 with optimum response, the circuits in the precision phase-locked-loop, below, are much more suitable.)

Often a frequency multiplier is needed, to provide an output frequency 2 or 3 or 10 or n times higher than the input. By inserting a ÷n frequency divider in the feedback loop, this is easily accomplished. [Of course, a ÷m frequency divider can be inserted ahead of the frequency input, to provide correct scaling, and the output frequency then will be $F_{IN}(n/m)$.]

To obtain good loop stability in a frequency multiplier with n = 2, remember that a 20 kHz V-to-F converter followed by a ÷2 circuit has exactly the same loop response and stability needs as a 10 kHz V-to-F converter, because it *is* a 10 kHz V-to-F converter, even though it provides a useful 20 kHz output. Thus, the frequency of the F_2 (minimum and maximum) will determine what loop gains and loop damping components are needed.

To accommodate a 1 kHz V-to-F loop, simply make C1 and C2 10 times bigger than the values of *Figure 1*; treat C3, C4, C5 and Ct similarly is used. To accommodate a 100 Hz V-to-F, increase them by another factor of 10.

If the PLL is to be used primarily as a frequency multiplier, it may be necessary to use stable, low-temperature-coefficient components, because the accuracy of V_{OUT} will not be important. The parts cost can be cut considerably. (Make sure that the VFC does not run out of range to handle all frequencies of interest.) On the other hand, the damping components will be chosen quite a bit differently if slow, stable jitter-free response is needed or if quick response is required. The circuits shown are just a starting place, to start optimizing your own circuit.



A3 — LF351, LM741 OR ANY
NPN TRANSISTOR — 2N3904, 2N2222 OR ANY SILICON NPN
PNP TRANSISTOR — 2N3906, 2N2907 OR ANY SILICON PNP
ALL RESISTORS ±10%
ALL DIODES 1N914 OR 1N4148 OR SIMILAR

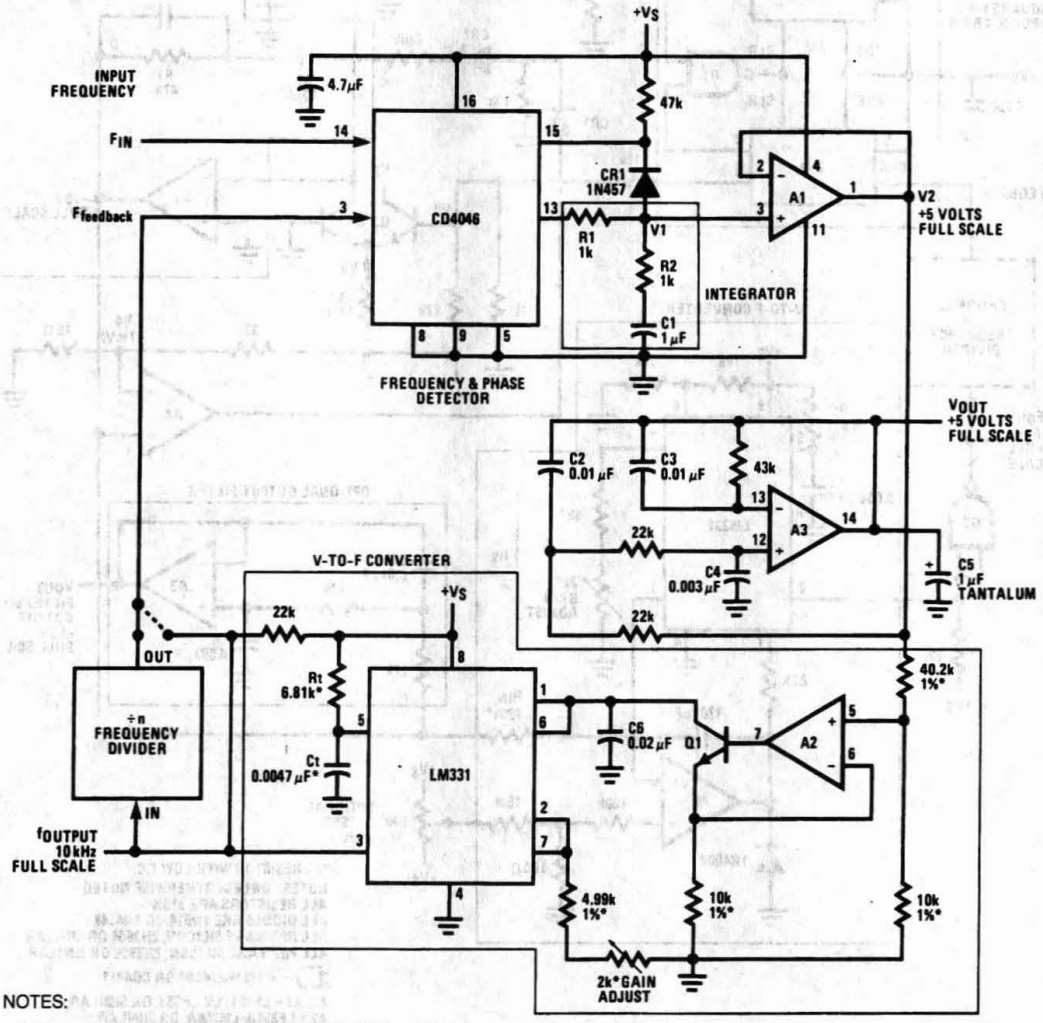
TL/H/5618–11

FIGURE 5. Proportional Current Source for Basic PLL

3. Optimize phase-lock loops to meet your needs or determine why you can't. Andrzej B. Przedpelski, *Electronic Design,* September 13, 1978.

A Single-Supply PLL

The single-supply PLL is shown in *Figure 6* as an example of a simple circuit which is effective when battery operation or single-supply operation is necessary. This circuit will function accurately over a 10:1 frequency range from 1 kHz to 10 kHz, but will not respond as quickly as the basic PLL of *Figure 1*. The reason is the use of the CD4046 frequency detector. When an F_{IN} edge occurs ahead of a F feedback pulse, pin 13 of the CD4046 pulls up on C1 via R1 = 1 kΩ. This current cannot be controlled or manipulated over as wide a range as "I1" in *Figure 1*. As a consequence, the response of this PLL is never as smooth nor fast-settling as the basic PLL, but it is still better behaved than most F-to-V converters. As with the basic PLL, the detector feeds a current to be integrated in C1 (and R2 provides the necessary "lead"). A1 acts simply as a buffer for the R1, C1 integrator. A3, optional, can provide a nicely filtered output. And A2 servos Q1, drawing a current out of C6 which is proportional to V2. Here the LM331 acts as a current-to-frequency converter, and F output is precisely proportional to the collector current of Q1. As with the basic circuit, this PLL can be used as a quick and/or quiet F-to-V converter, or as a frequency multiplier. One of the most important uses of an F-to-V is to demodulate the frequency of a V-to-F converter, which may be situated at a high common-mode voltage, isolated by photoisolators, or to recover a telemetered signal. An F-to-V converter of this sort can provide good bandwidth for demodulating such a signal.



NOTES:
— Q1 = 2N3565 OR 2N3904 HIGH BETA NPN
— A1, A2, A3 = ¼ LM324
— ON CD4046, PINS 1, 2, 4, 6, 7, 10, 11, 12 ARE NO CONNECTION
— USE STABLE, LOW-T.C. PARTS FOR COMPONENTS MARKED*
—+V_S = +7 TO +15 VDC

TL/H/5618–12

FIGURE 6. Single Supply Phase Locked Loop

The precision PLL in *Figure 7* acts very much the same as the basic PLL, with refinements in various places.

- The flip-flops in the detector have a gate G1 to CLEAR them, for quicker response.
- The currents which A1 integrates are steered through Q1, Q2 and Q3, Q4 because transistors are quicker then diodes, yet have much lower leakage.
- The V-to-F converter uses A2 as an op-amp integrator, to get better than 0.01% nonlinearity (max).
- G2 is recommended as an inverter, to invert the signal on the LM331's pin 3, avoid a delay, and improve loop stability. (However, we never found any *real* improvement in loop stability, despite theories that insist it must be there. Comments are invited.)

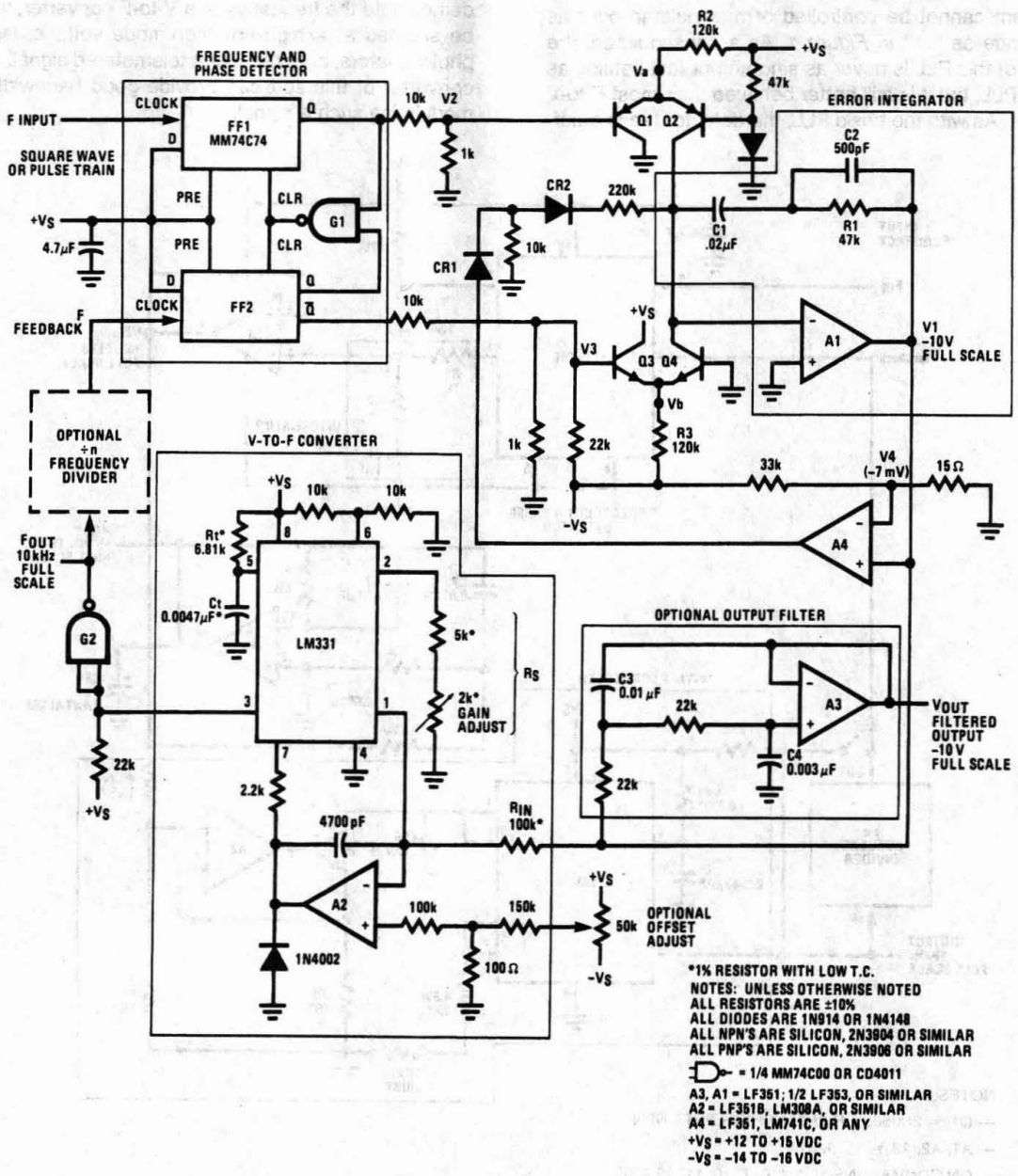


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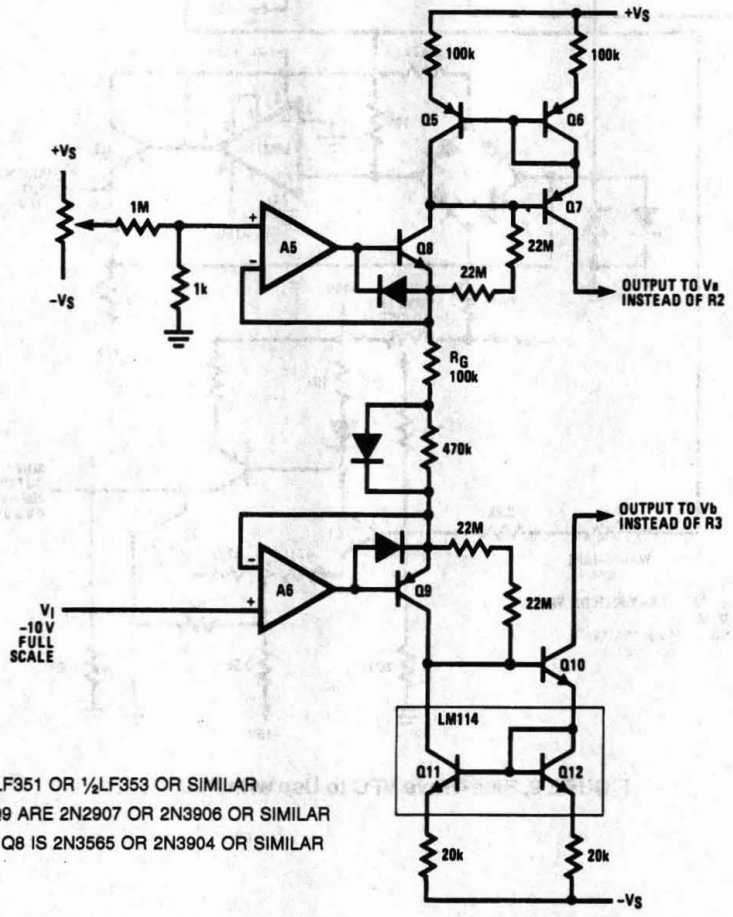
FIGURE 7. Precision PLL

- A4 is included as an (optional) limiter, to prevent V1 from ever going positive. This will facilitate quick startup and recovery from overdrive conditions.

Also, in *Figure 8*, the wide-range current pump for the precision PLL is a "semiprecision" circuit, and provides an output current proportional to −V1, give or take 10 or 15%, over a 3-decade range. The 22 MΩ resistors prevent the current from shutting off in case −V becomes positive (probably unnecessary if A4 is used). For best results over a full 3-decade range (11 kHz to 9 Hz), do use A4, delete the four 22 MΩ resistors, and insert the (diode parallel to the 470 kΩ) in series with the R_G as shown. This will give good stability at all frequencies (although stability cannot be extended below 1/1500 of full scale without extra efforts).

This PLL has been widely used in testing of VFCs, as it can force the LM331 to run at a crystal-controlled frequency (established as the F input), and the output voltage at V_{OUT} is promptly measured by a 6-digit (1 ppm nonlinearity, max) digital voltmeter, with much greater speed and precision than can be obtained by forcing a voltage and trying to read a frequency. While at 10 kHz, the advantages are clearcut; at 50 Hz it is even more obvious. Measuring a 50 Hz signal with ±0.01 Hz resolution cannot be done (even with the most powerful computing counter-timer) as accurately, quickly, and conveniently as the PLL's voltage output settles.



A5, A6, ARE LF351 OR ½LF353 OR SIMILAR
Q5, Q6, Q7, Q9 ARE 2N2907 OR 2N3906 OR SIMILAR
Q8, Q10 ARE Q8 IS 2N3565 OR 2N3904 OR SIMILAR

TL/H/5618–14

FIGURE 8. Wide Range Current Pumps for Precision PLL of *Figure 7*

One final application of this PLL is as a wide-range sine generator. The VFC in *Figure 9* puts out an adequate sine-shaped output, but does not have good V-to-F linearity, and its frequency stability is not much better than 0.2%. An LM331 makes an excellent linear stable V-to-F converter, with a pulse output; but it can not make sines. But it can command, via a PLL, to force the sine VFC to run at the correct frequency. Simply connect the sine VFC of *Figure 9* into one of the PLLs, instead of the LM331 VFC circuit. Then use a precise linear low-drift VFC based on the LM331 to establish the F_{IN} to the PLL. If the voltage needed by the sine VFC to put out a given frequency drifts a little, that is okay, as the integrator will servo and make up the error. The use of a controlled sine-wave generator in a test system was the first of many applications for a wide-range phase-locked-loop.

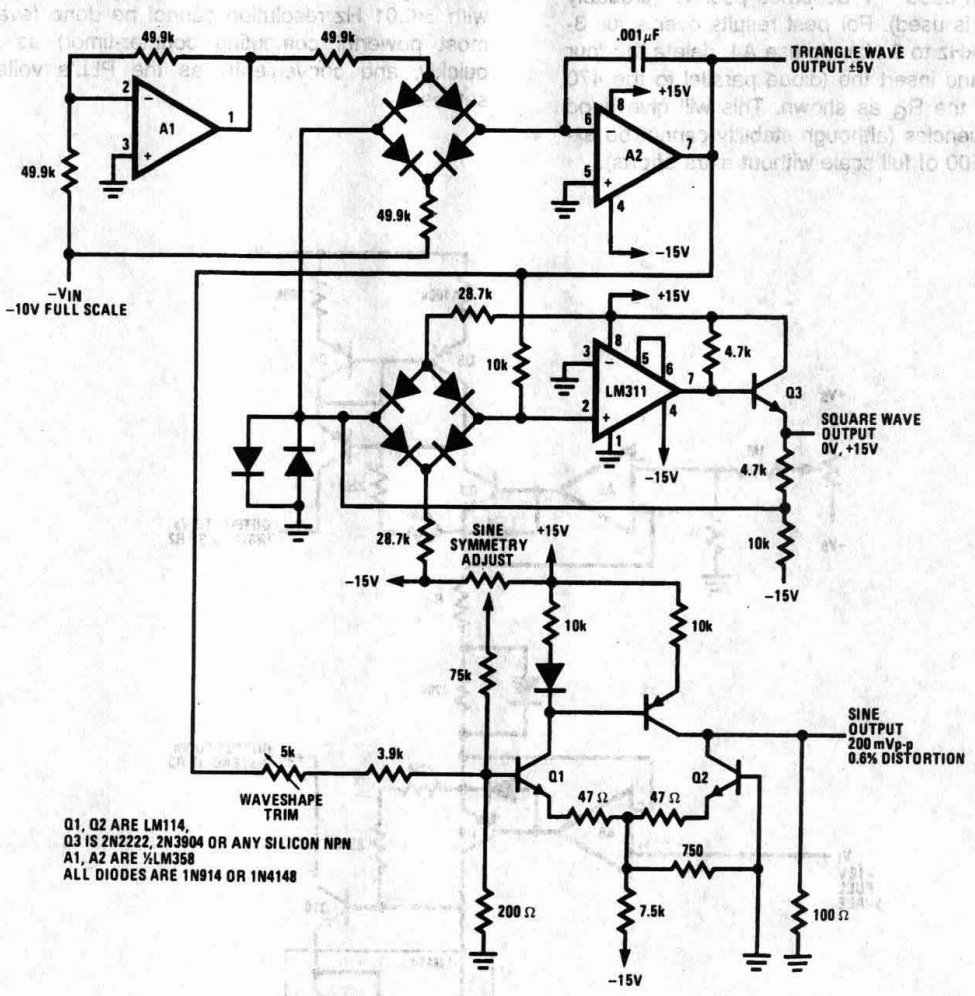


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FIGURE 9. Sine-Wave VFC to Use with PLL

New Op Amp Ideas

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Abstract: *An op amp and voltage reference capable of single supply operation down to 1.1V is introduced. Performance is uncompromised and compares favorably with standard, state-of-the-art devices. In a departure from conventional approaches, the circuit can operate in a floating mode, powered by residual voltages, independent of fixed supplies. A brief description of the IC design is given, but emphasis is on applications. Examples are given for a variety of remote comparators and two-wire transmitters for analog signals. Regulator designs with outputs ranging from a fraction of a volt to several hundred volts are discussed. In general, greater precision is possible than with existing ICs. Designs for portable instruments are also looked into. These applications serve to emphasize the flexibility of the new part and can only be considered a starting point for new designs.*

introduction

Integrated circuit operational amplifiers have reached a certain maturity in that there no longer seems to be a pressing demand for better performance. Devices are available at low cost for all but the most exacting needs. Of course, there is always room for improvement, but even substantial changes in specifications cannot be expected to cause much excitement.

A new approach to op amp design and application has been taken here. First, the amplifier has been equipped to function in a floating mode, independent of fixed supplies. This, however, in no way restricts conventional operation. Second, it has been combined with a voltage reference, since these two functions are often interlocked in equipment design. Third, the minimum operating voltage has been reduced to nearly one volt. It will be seen that these features open broad new areas of application.

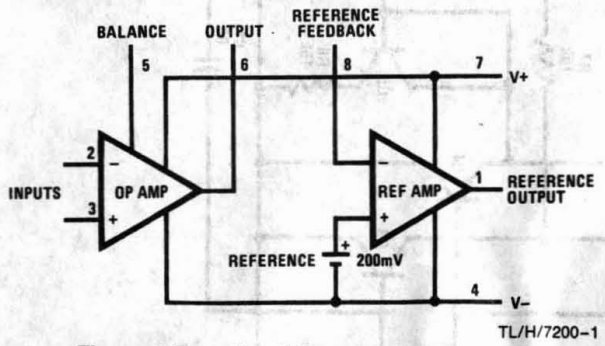

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Figure 1. Functional diagram of the new IC

A functional diagram of the new device is shown in *Figure 1*. Even though a voltage reference and a reference amplifier have been added, it can still be supplied in an eight-pin TO-5 or mini-DIP. The pin connections for the op amp are the same as the industry standards. And offset balancing that tends to minimize drift has been provided. Both the op amp and the reference amplifier are internally compensated for unity-gain feedback.

Table I shows that, except for bias current, the general specifications are much as good as the popular LM108. But the new circuit has a common mode range that includes V^- and the output swings within 50 mV of the supplies with 50 μA load, or within 0.4V with 20 mA load. These parameters are specified in Table I as the conditions under which gain and common-mode rejection are measured. Table II indicates that the reference compares favorably with the better ICs on the market today.

TABLE I. Typical Performance of the Operational Amplifier at 25°C

Parameter	Conditions	Value
Input Offset Voltage		0.3 mV
Offset Voltage Drift	$-55°C \le T_A \le 125°C$	2 μV/°C
Input Offset Current		0.25 nA
Offset Current Drift	$-55°C \le T_A \le 125°C$	2 pA/°C
Input Bias Current		10 nA
Bias Current Drift	$-55°C \le T_A \le 125°C$	40 pA/°C
Common-Mode Rejection	$V^- \le V_{CM} \le V^+ - .85V$	102 dB
Supply-Voltage Rejection	$1.2V \le V_S \le 40V$	96 dB
Unloaded Voltage Gain	$V_S = \pm 20V$, $V_O = \pm 19.95V$, $I_O \le 50\ \mu A$	400V/mV
Loaded Voltage Gain	$V_S = \pm 20V$, $V_O = \pm 19.6V$, $R_L = 980\Omega$	130V/mV
Unity-Gain Bandwidth	$1.2V \le V_S \le 40V$	0.3 MHz
Slew Rate	$1.2V \le V_S \le 40V$	0.15V/μs

TABLE II. Typical Performance of the Reference at 25°C

Parameter	Conditions	Value
Line Regulation	$1.2V \le V_S \le 40V$	0.001%/V
Load Regulation	$0 \le I_O \le 1$ mA	0.01%
Feedback Sense Voltage		200 mV
Temperature Drift	$-55°C \le T_A \le 125°C$	0.002%/°C
Feedback Bias Current		20 nA
Amplifier Gain	$0.2V \le V_O \le 35V$	75V/mV
Total Supply Current	$12.V \le V_S \le 40V$	270 μA

Since worst-case internal dissipation can easily exceed 1W under overload conditions, thermal overload protection is included. Thus at higher ambient temperatures, this circuit is better protected than conventional op amps with lesser output capabilities.

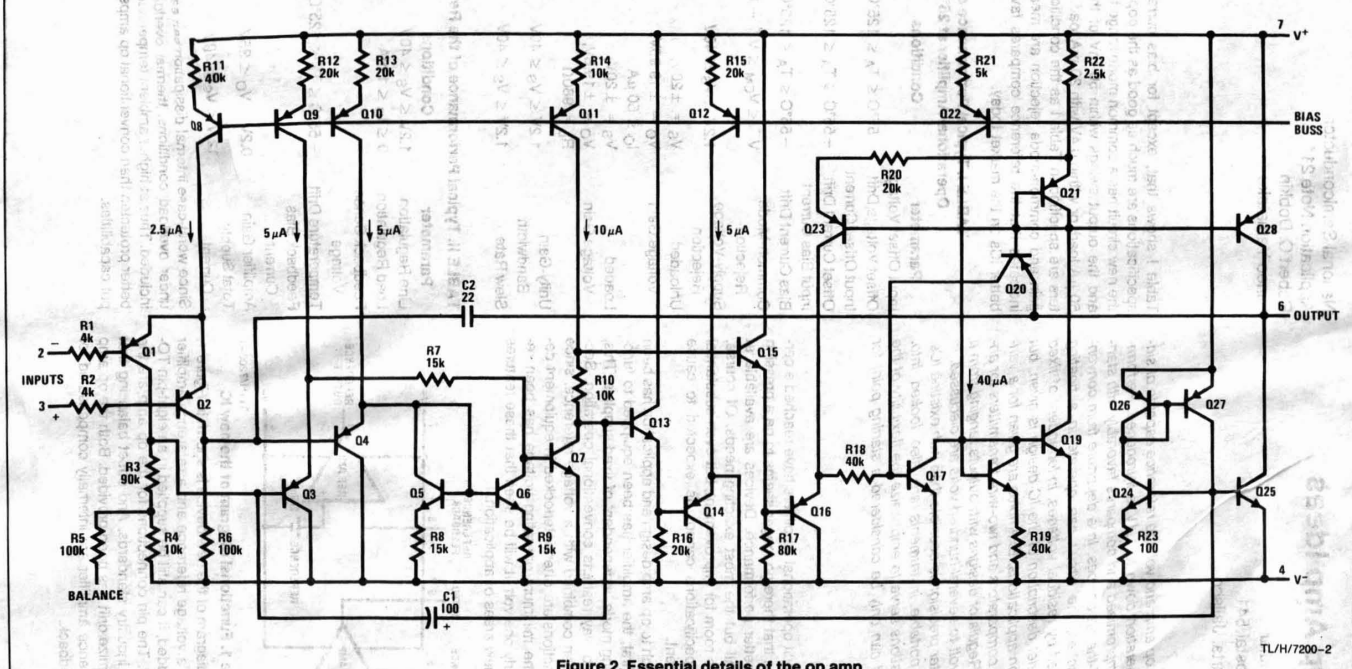

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Figure 2. Essential details of the op amp

Figures 2 and *5* are simplified schematics of the op amp, the reference and the internal current regulator. A complete circuit description is a subject in itself and is covered in detail elsewhere [1]. However, a brief run through the circuit is in order to give some understanding of the details that affect application.

the op amp

Referring to *Figure 2*, lateral PNPs are used for the op amp input because this was the only reasonable way to get V^- included in the common-mode range while meeting the minimum-voltage requirement. These transistors typically have $h_{FE} > 100$ at $I_C = 1\ \mu A$ and appear to match better than their NPN counterparts. Current gain is less affected by temperature, resulting in a fairly flat bias current over temperature (*Figure 3*). At elevated temperature the sharp decrease in bias current for $V_{CM} > V^-$ is caused by the same substrate leakage that affects bi-FET op amps.

Protective resistors have been included in the input leads so that current does not become excessive when the inputs are forced below the negative supply, forward biasing the base tubs of the lateral PNPs.

Offset nulling is accomplished by connecting the balance terminal to a variable voltage derived from the reference output, as shown in *Figure 4*. Both the input stage collector voltage and the reference are well regulated and have a low temperature drift. The resistance of the adjustment potentiometer can be made very much lower than the resistance looking back into the balance pin. Therefore, no matching of temperature coefficients is required and offset nulling will tend to produce a minimum-drift condition.

With 200 mV on the balance control, the balance range is asymmetrical. Standard parts are trimmed to bring them into the −1 mV to 8 mV adjustment range. Null sensitivity can be reduced for low-offset premium parts by adding a resistor on the top end of R1.

Proceeding through the circuit, the input stage is buffered by vertical PNP followers, Q3 and Q4. From here, the differential signal is converted to single ended and fed to the base of the second stage amplifier, Q7.

This configuration is not inherently balanced in that the emitter-base voltage of the PNP transistors is required to match that of the NPNs. The final design includes circuitry to correct for the expected variations.

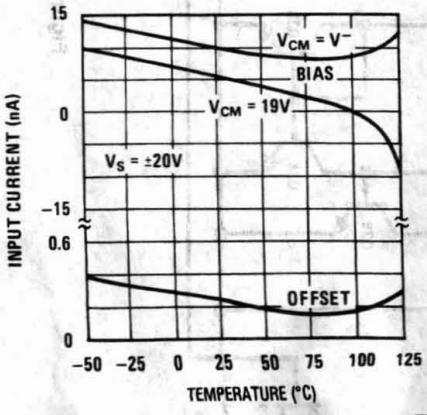

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Figure 3. *Variation of input current with temperature*

From the collector of Q7, the signal splits, driving separate halves of the complementary class-B output stage. The NPN output transistor, Q25, is driven through Q13 and Q14.

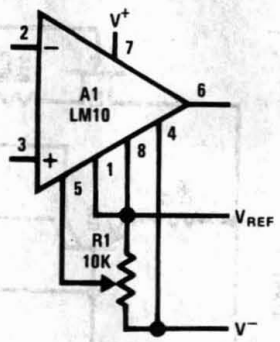

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Figure 4. Op amp offset adjustment

This complementary emitter follower arrangement provides the necessary current gain without requiring the extra bias voltage of the Darlington connection.

Base drive for the NPN output transistor is initially supplied by Q12, but a boost circuit has also been added to increase the available drive as a function of load current. This is accomplished by Q24 in conjunction with a current inverter.

Drive for the PNP half of the output is somewhat more complicated. Again, a compound buffer, Q15 and Q16, is used, although to maintain circuit balance rather than for current gain. The signal proceeds through two inverters, Q17 and Q19, to obtain the correct phase relationship and DC level shift before it is fed to the PNP output transistor, Q28.

This path has three common-emitter stages and, potentially, much higher gain than the NPN side. The gain is equalized, however, by the shunting action of Q18–R19 and Q21–R22 as well as negative feedback through Q23.

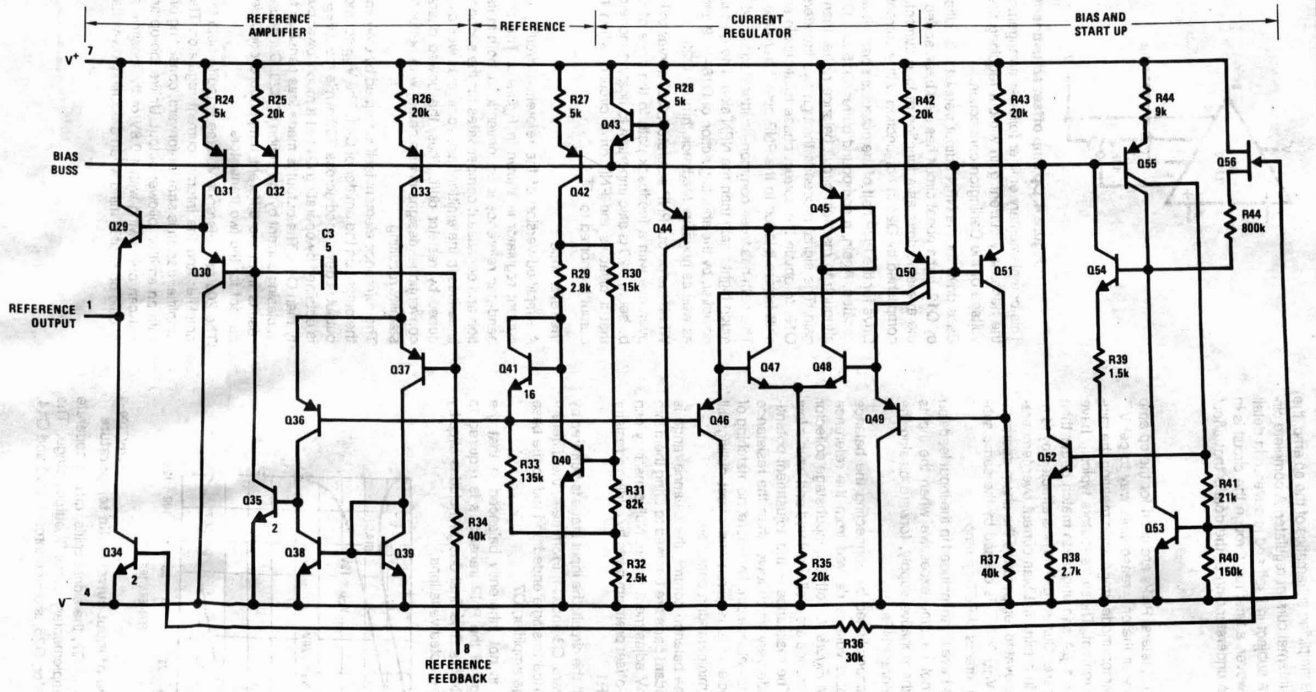
When the output PNP saturates, Q20 serves to limit its base overdrive with a feedback path to the base of Q17. As will be seen, Q20 is also important to floating-mode operation in that it disables the PNP drive circuitry when the op-amp output is shorted to V^+.

the reference

A simplified version of the reference circuitry and internal current regulator is shown in *Figure 5*. The design of the band-gap reference is unconventional both in its configuration and because it compensates for the second-order nonlinearities in the emitter-base voltage as well as those introduced by resistor drift. Thus, the bowed characteristic of conventional designs is eliminated, with better temperature stability resulting.

The reference element iself is formed by Q40 and Q41, with the output on the emitter of Q41. The V_{BE} component of the output is developed across R30, while the ΔV_{BE} component is obtained by operating Q41 at a much lower current density than Q40. The output is made less sensitive to variations in biasing current by the action of R29. Curvature correction results from the different temperature coefficients of bias current for the two transistors.

The 200 mV reference voltage is fed to both the reference amplifier and the internal current regulator. The reference amplifier design is straight-forward, consisting of two stages with an emitter follower output. Unlike the op amp, the output can only swing within 0.8V of the positive supply. This should be kept in mind when designing low-voltage circuitry.



TL/H/7200–5

Figure 5. Simplified schematic of the reference and internal current regulator

A minimal sink current (~20 μA) is supplied by Q34. And since the reference is not included in the thermal protection control loop, conventional current limit is included on the final circuit to limit maximum output current to about 3 mA.

The current regulator is also relatively uncomplicated. A control loop drives the current source bias bus so that the output of one current source (Q51) is proportional to the reference voltage. The remaining current sources are slaved into regulation by virtue of matching.

The remaining circuitry generates a trickle current for start-up and biases internal circuitry.

An analysis of the complete circuit would serve only to bring into focus a multitude of detail such as second-order DC compensation terms, minor-loop frequency stabilization, clamps, overload protection, etc. Although necessary, these particulars tend to obscure the principles being put forward. So, having gained some insight into circuit operation, it is appropriate to proceed to some of the novel applications made possible with this new IC.

floating comparators

The light-level detector in *Figure 6* illustrates floating-mode operation of the IC. Shorting the op-amp outut to V^+ disables the PNP half of the class-B output stage, as mentioned earlier. Thus, with a positive input signal, neither half of the output conducts and the current between the supply terminals is equal to the quiescent supply current. With negative input signals, the NPN portion of the output begins to turn on, reaching the short circuit current for a few hundred microvolts overdrive. This is shown in *Figure 7*.

Figure 7 also shows the terminal characteristics for the case where the output is shorted to V^- so that only the PNP side can be activated. This mode of operation has not been so thoroughly investigated, but it gives a slightly lower ON voltage at moderate currents and the gain is generally higher below 70°C. With ON currents less than about 1 mA, the terminal voltage drops low enough to disrupt the internal regulators and the reference, producing some hysteresis. Further, there is a tendency to oscillate over about a 50 μV range of input voltage in the linear region of comparator operation.

The above is not intended to preclude operation with the output connected to V^-, if there is a good reason for doing so. It is meant only to draw attention to the problems that might be encountered.

In *Figure 6*, the internal reference supplies the bias that determines the transition threshold. At crossover, the voltage across the photodiode is equal to the offset voltage of the op amp, so leakage is negligible. The circuit can directly drive such loads as logic circuits or silicon controlled rectifiers. The IC can be located remotely with the sensor, with the output transmitted along a twisted-pair line. Alternatively, a common ground can be used if there is sufficient noise immunity; and the signal can be transmitted on a single line.

It should be remembered that this particular design is fully compensated as a feedback amplifier. As such it is not particularly fast in comparator applications. With low-level signals, delays a few hundred microseconds can be expected; and once in the linear region, the maximum change of terminal voltage is 0.15/μs. This is illustrated in the plots of *Figures 8* and *9*. In general, high accuracy cannot be obtained with switch frequencies above 100 Hz.

Hysteresis can be provided as shown in *Figure 6* by feedback to the balance terminal. About 1 mV of hysteresis is obtained for a 5V output swing. However, this disappears near 10 Hz operating frequency because of gain loss.

Figure 10 shows a flame detector that can drive digital circuitry directly. The platinum-rhodium thermocouple gives an 8 mV output at 800°C. This threshold is established by connecting the balance pin to the reference otuput.

linear operation

The IC can also operate linearly in the floating mode. The simplest examples of this are the shunt voltage regulator in *Figure 11* and the current regulator in *Figure 12*. The voltage regulator is straightforward, but the current regulator is a bit unusual in that the supply current of the IC flows through the sense resistor and does not affect accuracy as long as it is less than the desired output current.

It is also possible to use remote amplifiers with two-wire signal transmission, as was done with the comparators. Remote sensors can be particularly troublesome when low-level analog signals are involved. Transmission problems include induced noise, ground currents, shunting from cable capacitance, resistance drops and thermoelectric potentials. These problems can be largely eliminated by amplifying the signal at the source and altering impedances to levels more suitable for transmission.

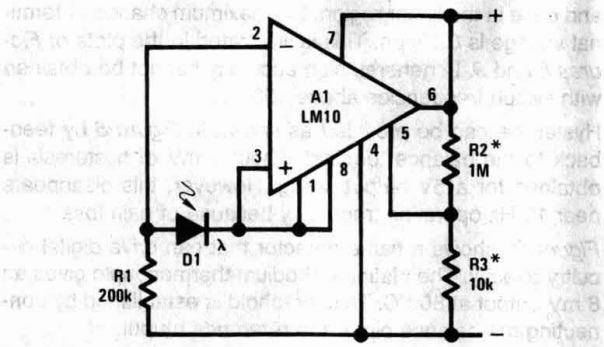
Figure 13 is an example of a remote amplifier. It boosts the output of a high-impedance crystal transducer and provides a low impedance output. No extra wires are needed because DC power is fed in on the signal line.

Figure 14 is a remote signal conditioner that operates in the current mode. A modification of the current source in *Figure 12*, it delivers an output current inversely proportional to sensor resistance. The output can be transmitted over a twisted pair for maximum noise immunity or over a single line with common ground if the signal is slow enough that sufficient noise bypass can be put on the line.

A current-mode signal conditioner for a thermocouple is shown in *Figure 15*. A thermocouple is in reality a two-junction affair that measures temperature differential. Absolute temperature measurements are made by controlling the temperature of one junction, usually by immersing it in an ice bath. This complication can be avoided with cold-junction compensation, which is an absolute thermometer that measures cold-junction temperature and corrects for any deviation from the calibration temperature.

In *Figure 15*, the IC temperature sensor (S1) generates an output proportional to absolute temperature. This current flows through R2, which is chosen so that its voltage drop has the same temperature coefficient as the thermocouple. Thus, changes in cold-junction temperature will not affect calibration as long as it is at the same temperature as S1.

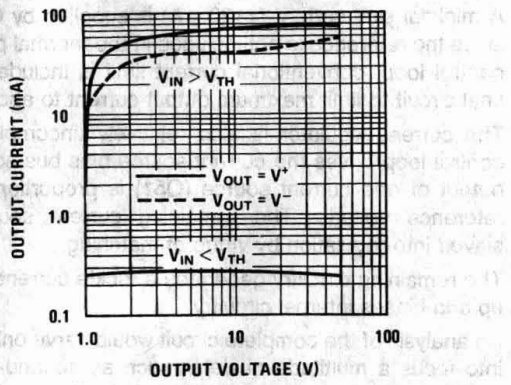
In addition to powering S1, the reference is used to generate an offset voltage such that the output current is within



*provides hysteresis

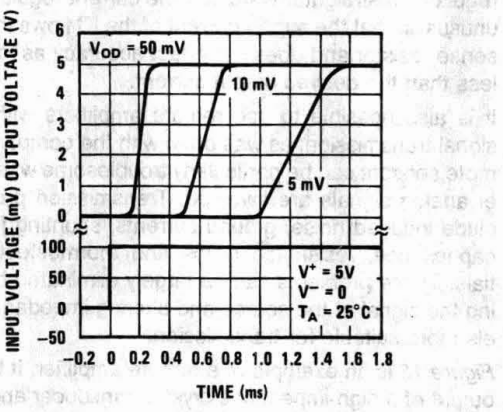
TL/H/7200–6

Figure 6. Two terminal light-level detector with hysteresis



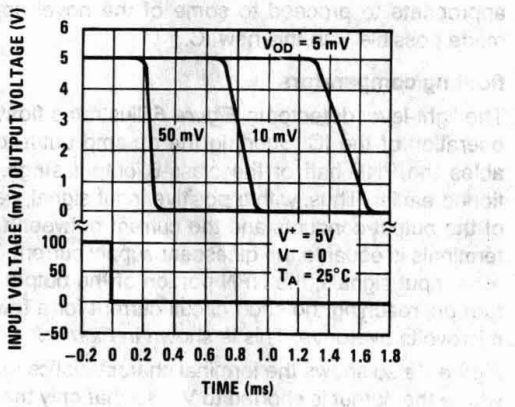
TL/H/7200–7

Figure 7. Terminal Characteristics above and below threshold



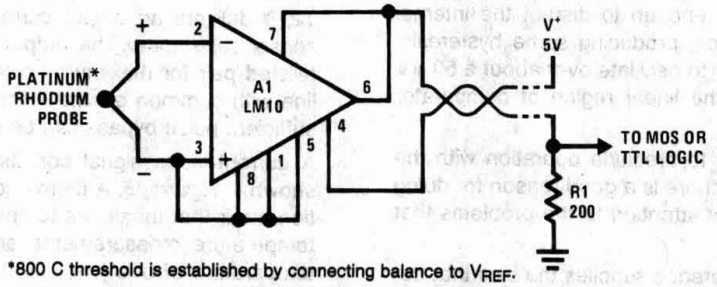
TL/H/7200–8

Figure 8. Comparator response times for various input overdrives



TL/H/7200–9

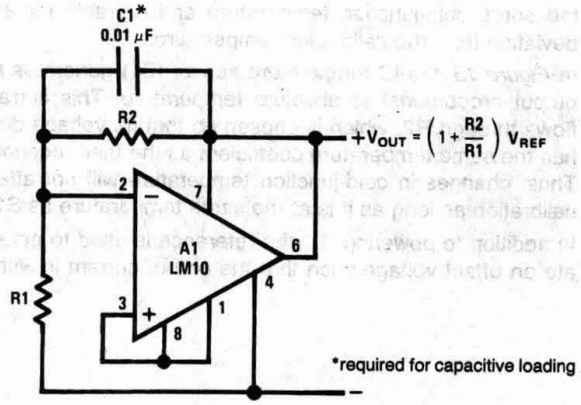
Figure 9. Comparator response times for various input overdrives



*800 C threshold is established by connecting balance to V_{REF}.

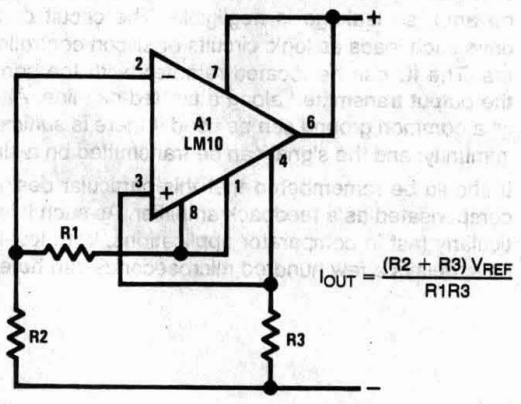
TL/H/7200–10

Figure 10. Flame detector



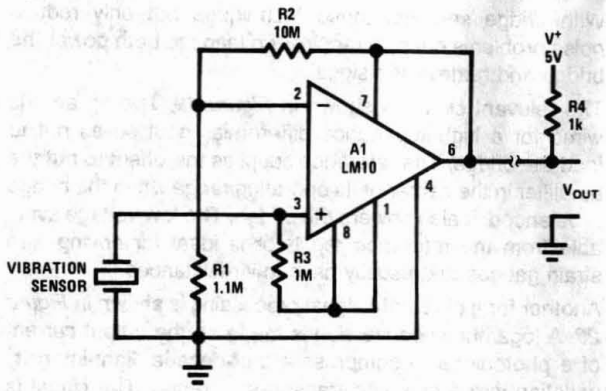
TL/H/7200–11

Figure 11. Shunt voltage regulator



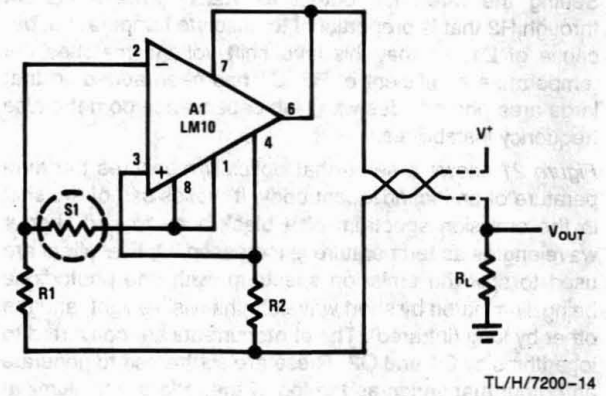
TL/H/7200–12

Figure 12. Current regulator



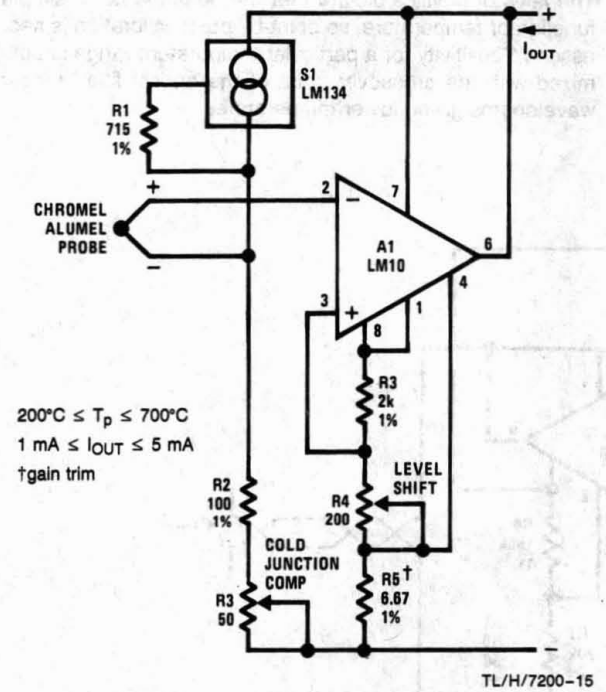
TL/H/7200–13

Figure 13. Remote amplifier



TL/H/7200–14

Figure 14. Two-wire transmitter for variable-resistance sensor



TL/H/7200–15

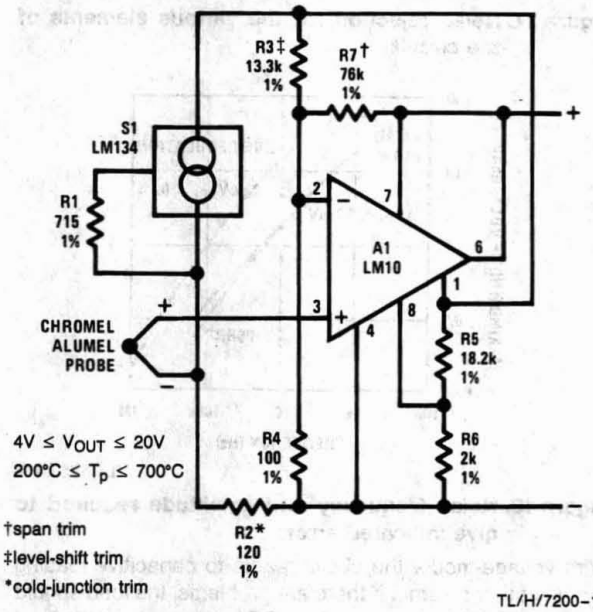
Figure 15. Current transmitter for thermocouple including cold junction compensation

operating limits for temperatures of interest. It is important that the reference be stable because drift will show up as signal.

The indicated output-current range was chosen because it is one of the standards for two-wire transmission. With the new IC, the dynamic range can be increased by a factor of five in some cases (0.8 mA–20 mA) because the supply current is low. This could be used to advantage with a unidirectional signal where zero must be preserved: the less the offset required to put zero on scale, the less the offset-drift error.

The circuit in *Figure 16* is the same thermocouple amplifier operating in the voltage mode. The output voltage range was chosen arbitrarily in that there are no set standards for voltage-mode transmission.

The choice between voltage- and current-mode operation will depend on the peculiarities of the application, although



TL/H/7200–16

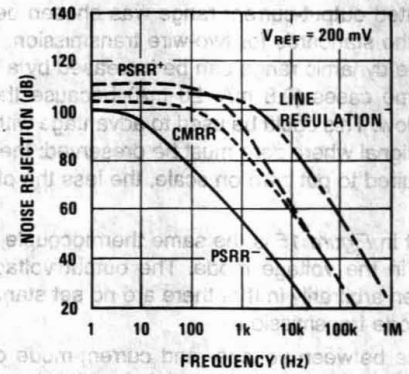
Figure 16. Voltage transmitter for thermocouple, including cold junction compensation

current mode seems to be favored overall. If there is sufficient supply voltage, the dynamic range of both approaches is about equal, provided the transmitter is capable of working at both low voltage and current. This situation could be modified by the voltage and current requirements of the sensor or conditioning circuitry.

With voltage-mode operation, the line resistance can cause error because the DC current that powers the amplifier and sensor circuitry must flow through it. Ground potentials, if they cannot be swamped out with signal swing, would require that twisted pair lines be used. This is not so with current mode.

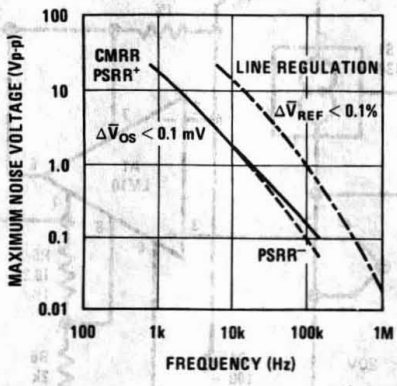
An important consideration is that cable capacitance does not affect the loop stability of the current-mode amplifier. However, large-amplitude noise appearing across the output can give problems. *Figure 17* shows the noise rejections of the LM10. The negative supply rejection applies in current-mode operations with the output connected to V^+. The rejection in this mode is not overly impressive, but transmission can be reduced by bypassing the load resistor. This done, noise slew limiting is the restricting factor in that excessive slew can give rise to a DC error. The maximum

noise amplitude that can be tolerated for a 100 μV input-referred DC error is plotted in *Figure 18*. These limits are not to be pushed as error increases rapidly above them.



TL/H/7200–17

Figure 17. Noise rejection for the various elements of the circuit



TL/H/7200–18

Figure 18. Noise frequency and amplitude required to give indicated error

With voltage-mode, the circuit reacts to capacitive loading like any other op amp. If there are problems, the load should be isolated with a resistor, taking DC feedback from the load and AC feedback from the op amp output. With the LM10, it is also possible to bypass the output with a single, large capacitor (20 μF electrolytic) if speed is no consideration.

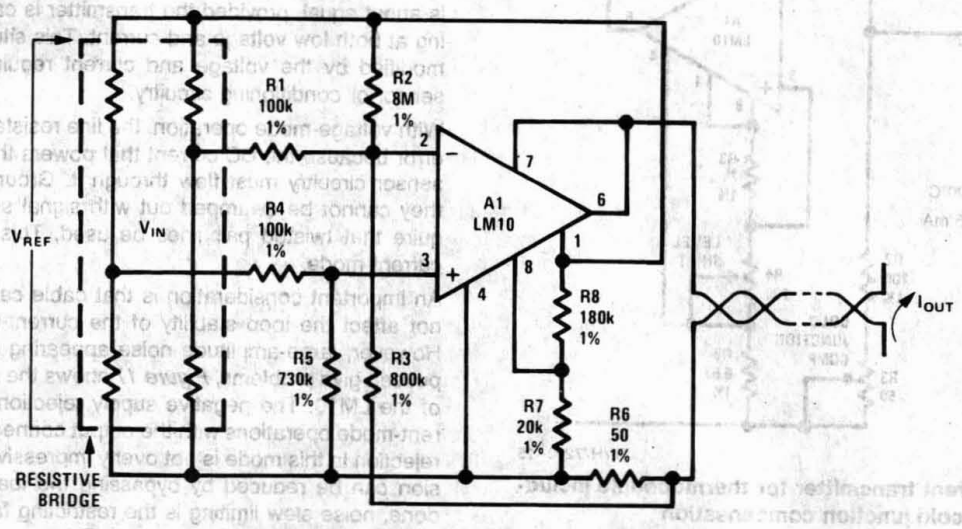
With bridge sensors, these techniques not only reduce noise problems but only require two leads to both power the bridge and retrieve the signal.

The relevant circuit is shown in *Figure 19*. The op amp is wired for a high-impedance differential input so as not to load the bridge. The reference supplies the offset to put the amplifier in the center of its operating range when the bridge is balanced. It also powers the bridge. The low voltage available from the reference regulator is ideal for driving wire strain gauges that usually have low resistances.

Another form of remote signal processing is shown in *Figure 20*. A logarithmic conversion is made on the output current of a photodiode to compress a four-decade, light-intensity variation into a standard transmission range. The circuit is balanced at mid-range, where R3 should be chosen so that the current through it equals the photodiode current. The log-conversion slope is temperature compensated with R6. Setting the reference output to 1.22V gives a current through R2 that is proportional to absolute temperature, because of D1, so that this level-shift voltage matches the temperature coefficient of R6. C1 has been added so that large area photodiodes with high capacitance do not cause frequency instabilities.

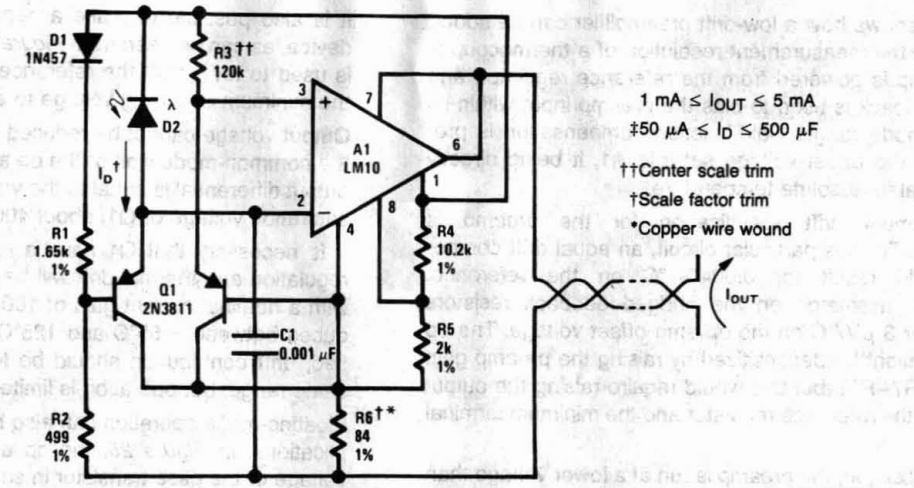
Figure 21 shows a setup that optically measures the temperature of an incandescent body. It makes use of the shift in the emission spectrum of a black body toward shorter wavelengths as temperature is increased. Optical filters are used to split the emission spectrum, with one photodiode being illuminated by short wavelengths (visible light) and the other by long (infrared). The photocurrents are converted to logarithms by Q1 and Q2. These are subtracted to generate an output that varies as the log of the ratio of the illumination intensities. Thus, the circuit is sensitive to changes in spectral distribution, but not intensity. Otherwise, the circuit is quite similar to that in *Figure 20*.

The laws of physics dictate that the output is not a simple function of temperature, so point-by-point calibration is necessary. Sensitivity for a particular temperature range is optimized with the crossover point of the optical filter, longer wavelengths giving lower temperatures.



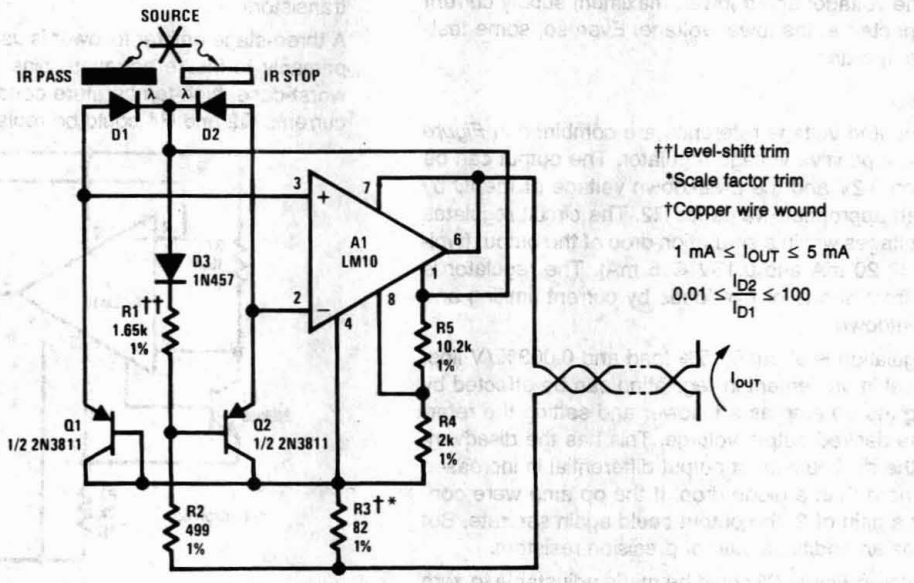
TL/H/7200–19

Figure 19. Two-wire transmitter for resistive bridge



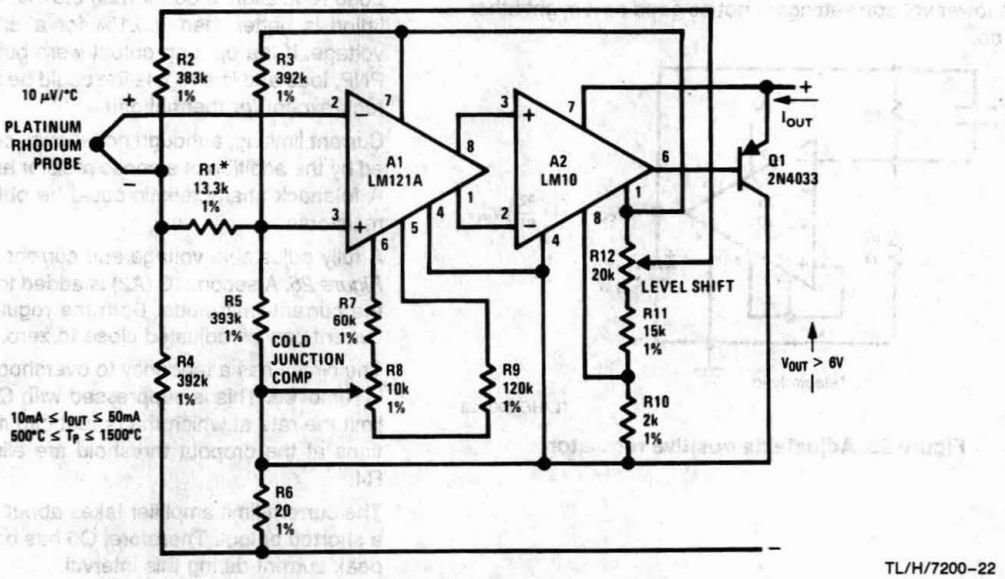
TL/H/7200–20

Figure 20. Log converter/transmitter for a photodiode



TL/H/7200–21

Figure 21. Optoelectric pyrometer with transmitter



TL/H/7200–22

Figure 22. Precision thermocouple amplifier/transmitter

Figure 22 shows how a low-drift preamplifier can be added to improve the measurement resolution of a thermocouple. The preamp is powered from the reference regulator, and bridge feedback is used to bias the preamp input within its common-mode range. Cold-junction compensation is provided with the offset voltage set into A1, it being directly proportional to absolute temperature.

The maximum drift specification for the preamp is 0.2 μV/°C. For this particular circuit, an equal drift component would result for 0.004%/°C on the reference, 0.001%/°C mismatch on the bridged-feedback resistors (R2–R4) or 3 μV/°C on the op amp offset voltage. The op amp drift might be desensitized by raising the preamp gain (lowering R7–R9), but this would require raising the output voltage of the reference regulator and the minimum terminal voltage.

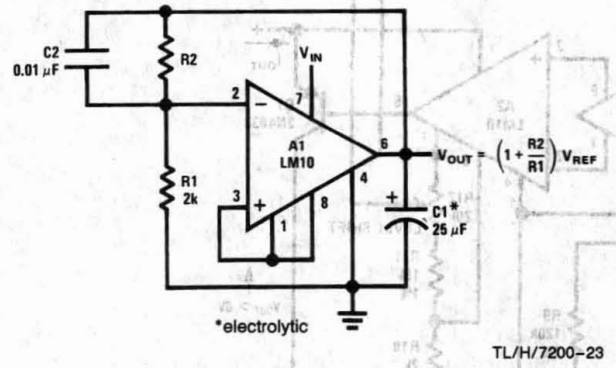
In this application, the preamp is run at a lower voltage than standard parts are tested with, and the maximum supply current specified is high. However, there should be no problem with the voltage; and a lower, maximum supply current can be expected at the lower voltage. Even so, some testing may be in order.

regulators

The op amp and voltage reference are combined in *Figure 23* to make a positive voltage regulator. The output can be set between 0.2V and the breakdown voltage of the IC by selecting an appropriate value for R2. The circuit regulates for input voltages within a saturation drop of the output (typically 0.4V @ 20 mA and 0.15V @ 5 mA). The regulator is protected from shorts or overloads by current limiting and thermal shutdown.

Typical regulation is about 0.05% load and 0.003%/V line. A substantial improvement in regulation can be effected by connecting the op amp as a follower and setting the reference to the desired output voltage. This has the disadvantage that the minimum input-output differential is increased to a little more than a diode drop. If the op amp were connected for a gain of 2, the output could again saturate. But this requires an additional pair of precision resistors.

The regulator in *Figure 23* could be made adjustable to zero by connecting the op amp to a potentiometer on the reference output. This has the disadvantage that the regulation at the lower voltage settings is not as good as it might otherwise be.



TL/H/7200–23

Figure 23. Adjustable positive regulator

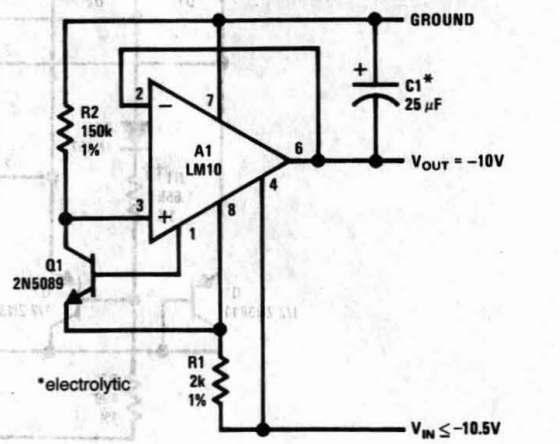
It is also possible to make a negative regulator with this device, as can be seen from *Figure 24*. A discrete transistor is used to level shift the reference current. This increases the minimum operating voltage to about 1.8V.

Output voltage cannot be reduced below 0.85V because of the common-mode limit of the op amp. The minimum input-output differential is equal to the voltage across R1 plus the saturation voltage of Q1, about 400 mV.

It is necessary that Q1 have a high current gain, or line regulation and thermal drift will be degraded. For example, with a nominal current gain of 100, a 1% drift will be introduced between −55°C and 125°C. With the device specified, drift contribution should be less than 0.3% over the same range; but operation is limited to 30V on the input.

Floating-mode operation can also be useful in regulator applications. In *Figure 25*, the op amp controls the turn-on voltage of the pass transistor in such a way that it does not see either the output voltage or the supply voltage. Therefore, maximum voltages are limited only by the external transistors.

A three-stage emitter follower is used for the pass transistor primarily to insure adequate bias voltage for the IC under worst-case, high-temperature conditions. With lower output currents Q2 and R4 could be replaced with a diode.



TL/H/7200–24

Figure 24. Negative regulator

Load regulation is better than 0.01%. Worst-case line regulation is better than ±0.1% for a ±10V change in input voltage. If the op amp output were buffered with a discrete PNP, load and line regulation could be made essentially perfect, except for thermal drift.

Current limiting, although not shown, could easily be provided by the addition of a sense resistor and an NPN transistor. A foldback characteristic could be obtained with two more resistors.

A fully adjustable voltage and current regulator is shown in *Figure 26*. A second IC (A2) is added to provide regulation in the current-limit mode. Both the regulated voltage and the current can be adjusted close to zero.

The circuit has a tendency to overshoot when a short circuit is removed. This is suppressed with Q2, R5 and C3, which limit the rate at which the output can rise. Low-level oscillations at the dropout threshold are eliminated with C2 and R4.

The current-limit amplifier takes about 100 μs to respond to a shorted output. Therefore, Q6 has been added to limit the peak current during this interval.

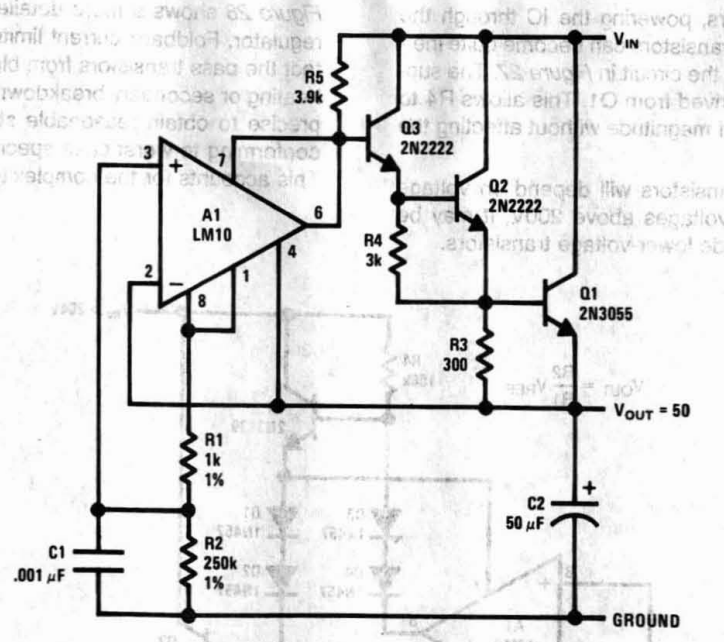


Figure 25. Bootstrapped regulator

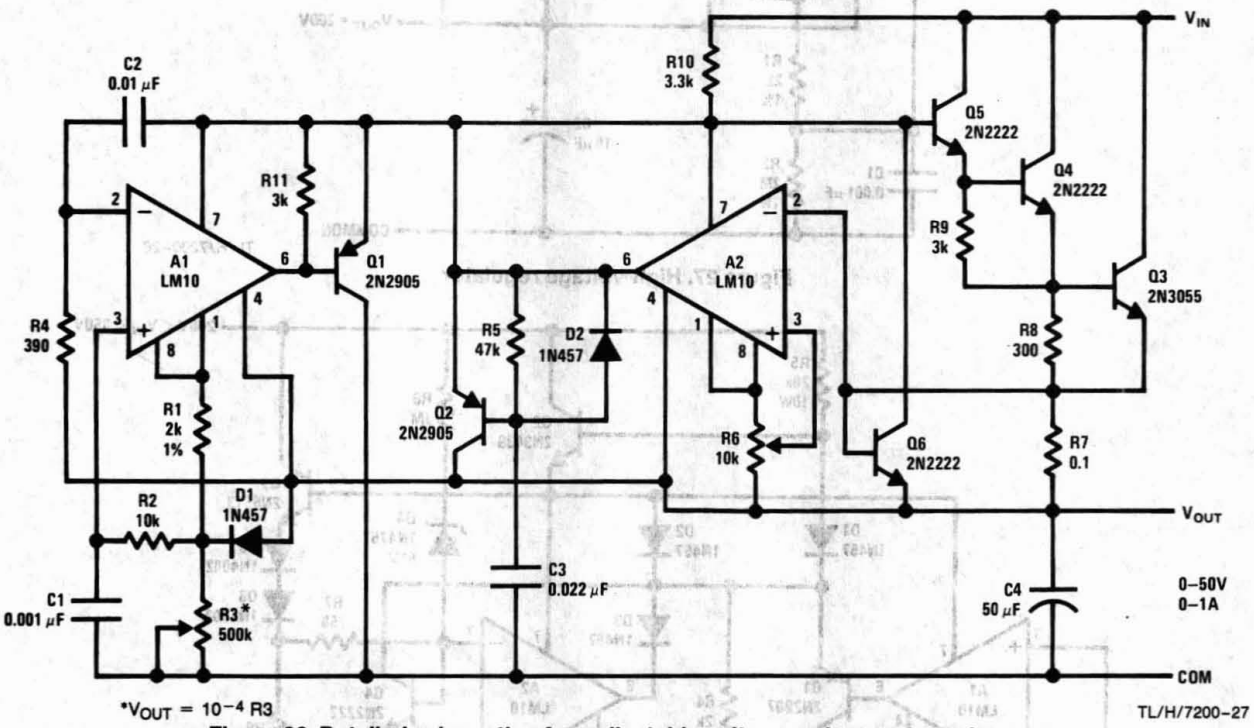


Figure 26. Detailed schematic of an adjustable voltage and current regulator

With high-voltage regulators, powering the IC through the drive resistor for the pass transistors can become quite inefficient. This is avoided with the circuit in *Figure 27*. The supply current for the IC is derived from Q1. This allows R4 to be increased by an order of magnitude without affecting the dropout voltage.

Selection of the output transistors will depend on voltage requirements. For output voltages above 200V, it may be more economical to cascade lower-voltage transistors.

Figure 28 shows a more detailed circuit for a high-voltage regulator. Foldback current limiting has been added to protect the pass transistors from blowout caused by excessive heating or secondary breakdown. This limiting must be fairly precise to obtain reasonable start-up characteristics while conforming to worst case specifications for the transistors. This accounts for the complexity of the circuit.

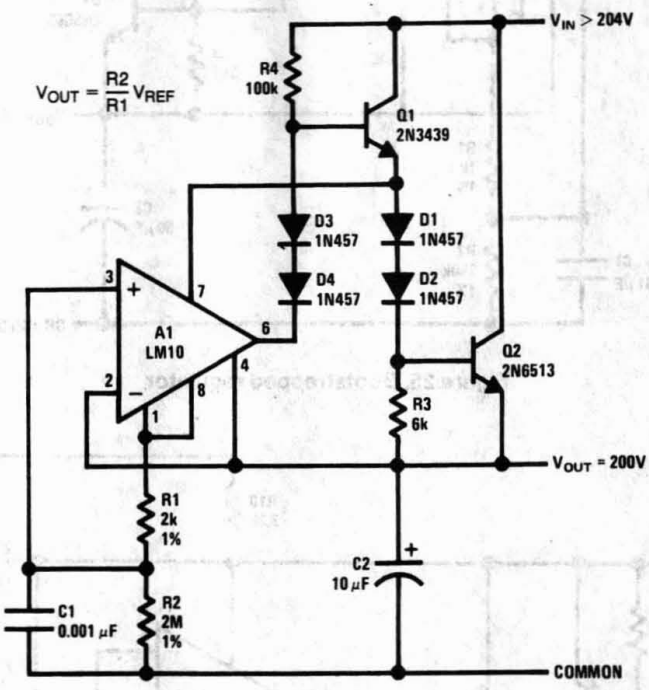


Figure 27. High-voltage regulator

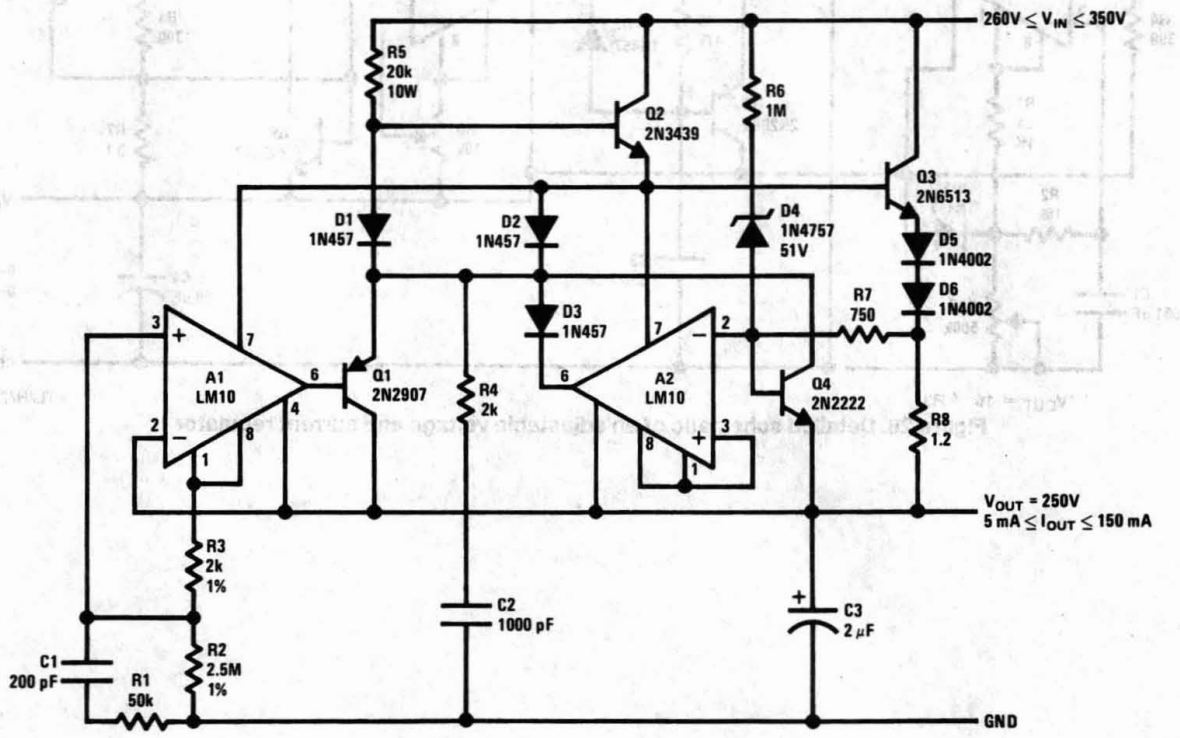


Figure 28. High voltage regulator with foldback current limit

The output current is sensed across R8. This is delivered to the current limit amplifier through R7, across which the foldback potential is developed by R6 with a threshold determined by D4. The values given limit the peak power below 20W and shut off the pass transistors when the voltage across them exceeds 310V. With unregulated input voltages above this value, start-up is initiated solely by the current through R5. Q4 is added to provide some control on current before A2 has time to react.

The design could be considered overly conservative, but this may not be inappropriate considering the start of the art for high-voltage power transistors. Their maximum operating current is in the tens of milliamperes at maximum voltage. Cutting off the power transistor before the maximum input-output voltage differential is reached can cause start-up problems, depending on the nature of the load (those that tend toward a constant-current characteristic being worst).

If a tighter design is required for start-up, the values of R6 and D4 can be altered. In addition, R5 can be lowered, although it may be necessary to add a PNP buffer to A2 in place of D3.

The leakage current of Q3 can be more than several milliamperes. That is why a hard turn-off is provided with D2.

The circuit is stable with an output capacitor greater than about 2 μF. Spurious oscillations in current limit are suppressed by C2 and R4, while a strange, latch-mode oscillation coming out of current limit is killed with C1 and R1.

Switching regulators operating directly from the power lines are seeing increased usage not only because of the reduced weight and size when compared to a 60 Hz transformer but also because they operate over a wide voltage range giving a regulated output with reasonable efficiency. Electrical isolation of the load is generally required in these applications for reasons of safety. Therefore, if precise regulation is needed on the secondary, there must be some way of transmitting the error signal back to the primary.

Figure 29 shows a design that provides this function. The IC serves as a reference and error amplifier, transmitting the error signal through an optical coupler. The loop gain may be controlled by the addition of R1, and C1 and R5 may be added to develop the phase lead that is helpful in frequency stabilizing the feedback.

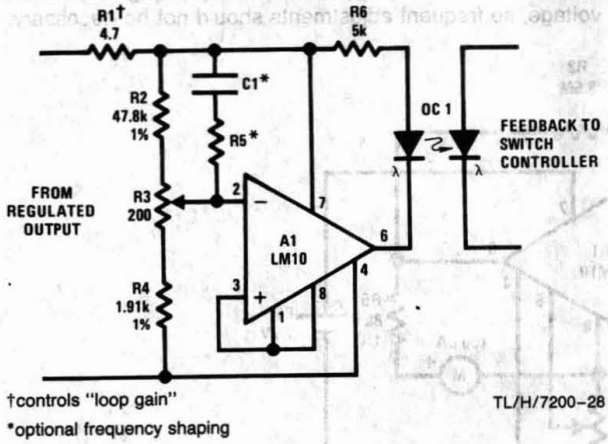


Figure 29. Isolated sensor for an off-line switching regulator

voltage level indicators

In battery-powered circuitry, there is some advantage to having an indicator to show when the battery voltage is high enough for proper circuit operation. This is especially true for instruments that can produce erroneous data.

The battery status indicator drawn in *Figure 30* is designed for a 9V source. It begins dimming noticeably below 7V and extinguishes at 6V. If the warning of incipient battery failure is not desired, R3 can be removed and the value of R1 halved.

A second circuit that also regulates the current through the light-emitting diode is shown in *Figure 31*. This is important so that adequate current is available at minimum voltage, but excessive current is not drawn at maximum voltage. Current regulation is accomplished by using the voltage on the balance pin (5) as a reference for the op amp. This is controlled at approximately 23 mV, independent of temperature, by an internal regulator. When the voltage on the reference-feedback terminal (8) drops below 200 mV, the reference output (1) rises to supply the feedback voltage to the op amp through D2, so the LED current drops to zero.

The minimum threshold voltage for these circuits is basically limited by the bias voltage for the LEDs. Typically, this is 1.7V for red, 2V for green and 2.5V for yellow. These two circuits can be made to operate satisfactorily for threshold voltages as low as 2V if a red diode is used. However, the circuit in *Figure 31* is preferred in that difficulties caused by voltage change across the diode biasing resistor are eliminated.

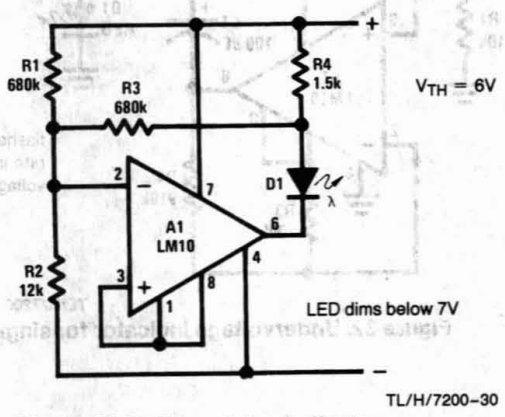


Figure 30. Battery status indicator

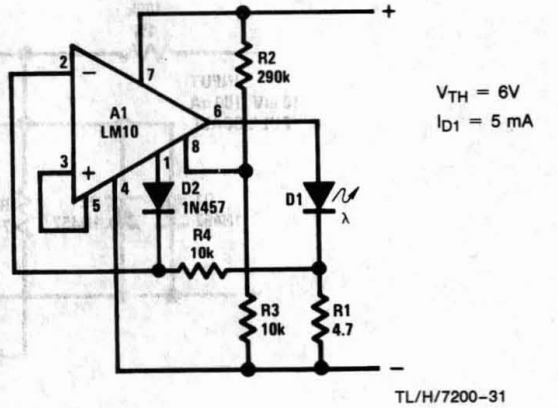


Figure 31. Battery level indicator with regulated LED current

When operating with a single cell, it is necessary to incorporate switching circuitry to develop sufficient voltage to drive the LED. A circuit that accomplishes this is drawn in *Figure 32*. Basically, it is a voltage-controlled asymmetrical multivibrator with a minimum operating threshold given by

$$V_{TH} = \frac{R4\,(R1 + R2)}{R1\,(R3 + R4)} V_{REF} \qquad (1)$$

Above this threshold, the flash frequency increases with voltage. This is a far more noticeable indication of a deteriorating battery than merely dimming the LED. In addition, the indicator can be made visible with considerably less power drain. With the values shown, the flash rate is 1.4 sec^{-1} at 1.2V with a 300 μA drain and 5.5 sec^{-1} at 1.55V with 800 μA drain. Equivalent visibility for continuous operation would require more than 5 mA drain.

The maximum threshold voltage of this circuit is limited because the LED can be turned on directly through R5. Once this happens, the full supply voltage is not delivered to R2, which is how the threshold is determined. This problem can be overcome with the circuit illustrated in *Figure 33*. This design repositions the indicator diode, requiring an input voltage somewhat greater than the diode bias voltaged needed.

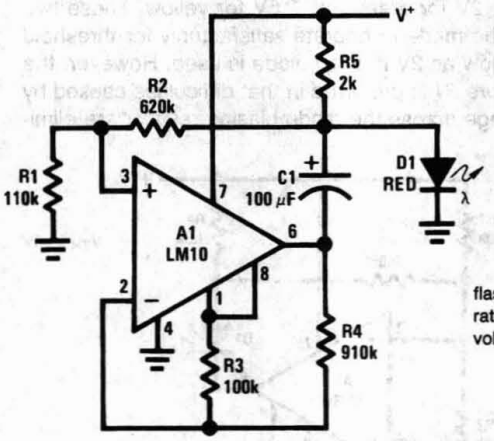


Figure 32. Undervoltage indicator for single call

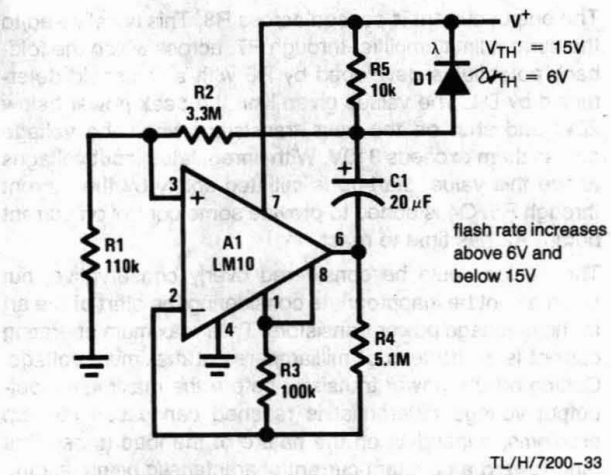


Figure 33. Double-ended voltage monitor

This circuit has the added feature that it can sense an overvoltage condition. The lower activation threshold is given by equation (1), but above a threshold,

$$V_{TH}' = \frac{R4\,(R1 + R2)\,V_{REF}}{R1\,(R3 + R4) - R3\,(R1 + R2)}, \qquad (2)$$

oscillation again ceases. (Below V_{TH} the op amp output is saturated negative while above V_{TH}' it is saturated positive.) The flash rate approaches zero near either limit.

The minimum/maximum limits possible with this circuit along with the possibility of estimating the proximity to the limit and the low power drain ($\sim$ 500 μA) make it attractive for a variety of simple, low-cost test equipment. This could include everything from the measurement of power-line voltage to in-circuit testers for digital equipment.

meter circuits

One obvious application for this IC is a meter amplifier. Accuracy can be maintained over a 15°C to 55°C range for a full-scale sensitivity of 10 mV and 100 nA using the design in *Figure 34*. In fact, initial tests indicate negligible zero drift with1 mV and 10 nA sensitivities, although balancing is troublesome with low-cost potentiometers. Offset voltage error is nulled with R5, and the bias current can be balanced out with R4. The zeroing circuits operates from the reference output and are essentially unaffected by changes in battery voltage, so frequent adjustments should not be necessary.

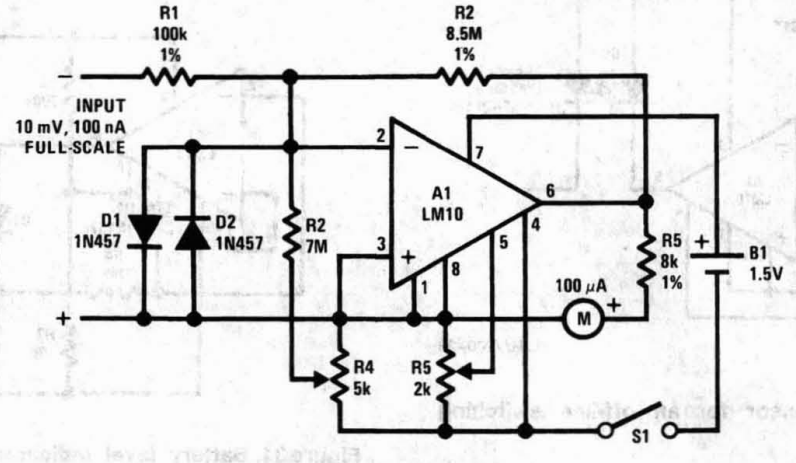


Figure 34. Meter amplifier

Under overload conditions, the current delivered to the meter is kept well in hand by the limited output swing of the op amp. The same is true for polarity reversals. Input clamp diodes protect the circuit from gross overloads.

Total current drain is under 0.5 mA, giving an approximate life of 3–6 months with an "AA" cell and over a year with a "D" cell. With these lifetimes an ON/OFF switch may be unnecessary. A test switch that converts to a battery-test mode may be of greater value.

If the meter amplifier is used in building a multimeter, the internal reference can also be used in measuring resistance. This would make the usual frequent recalibration with falling cell voltage unnecessary.

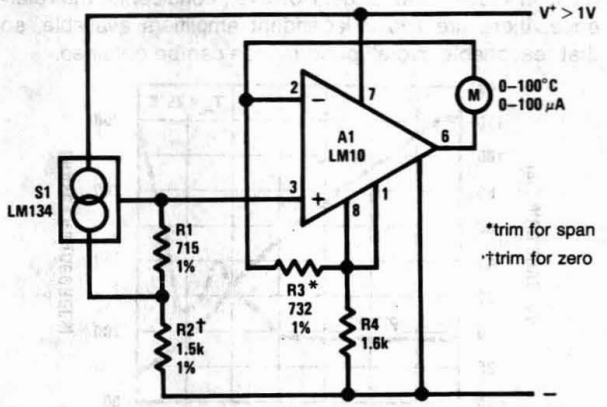
A portable light-level meter with a five-decade dynamic range is shown in *Figure 35*. The circuit is calibrated at mid-range with the appropriate illumination by adjusting R2 such that the amplifier output equals the reference and the meter is at center scale. The emitter-base voltage of Q2 will vary with supply voltage; so R4 is included to minimize the effect on circuit balance. If photocurrents less than 50 nA are to be measured, it is necessary to compensate the bias current of the op amp.

The logging slope is not temperature compensated. With a five-decade response, the error at the scale extremes will be about 40% (a half stop in photography) for a ±18°C temperature change.

If temperature compensation is desired, it is best to use a center-zero meter to introduce the offset, rather than the reference voltage. This done, temperature compensation can be obtained by making the resistor in series with the meter a copper wire-wound unit.

If this design is to be used for photography, it is important to remember that silicon photodiodes are sensitive to near infrared, whereas ordinary film is not. Therefore, an infrared-stop filter is called for. A blue-enhanced photodiode or an appropriate correction filter would also give best results.

An electronic thermometer design, useful in the range of −55°C to 150°C, is shown in *Figure 36*. The sensor, S1, develops a current that is proportional to absolute temperature. This is given the required offset and range expansion by the reference and op amp, resulting in a direct readout in either °C or °F.



TL/H/7200–36

Figure 36. Electronic thermometer

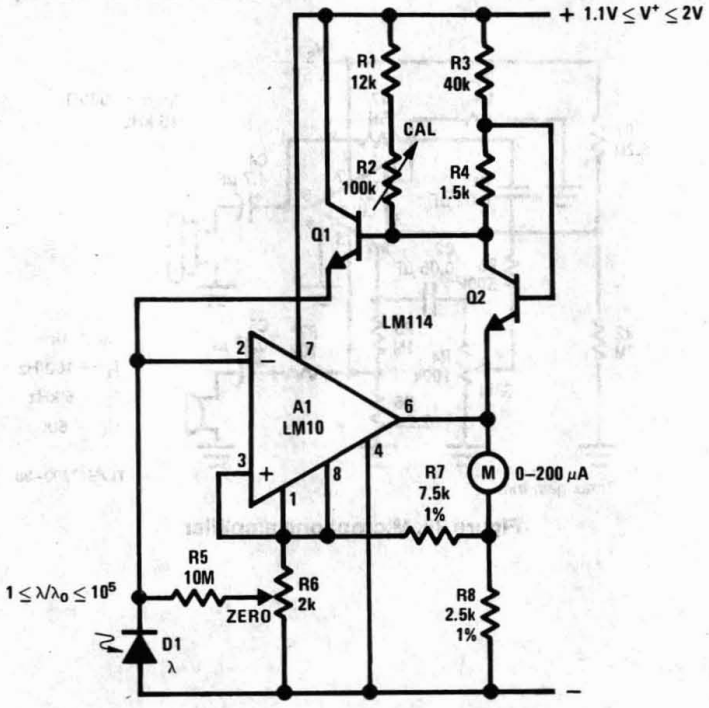


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Figure 35. Logarithmic light-level meter

Although it can operate down to 1V with better than 0.5°C accuracy, the LM134 is not tested below 1.5V. Maverick units were observed to develop a 1°C error going from 1.5V to 1.2V. This should be kept in mind for high-accuracy applications.

The thermocouple transmitter in *Figure 15* can easily be modified to work with a meter if a broader temperature range is of interest. It would likewise be no great problem adapting resistance or thermistor sensors to this function.

audio circuits

As mentioned earlier, the frequency response of the LM10 is not as good as might be desired. The frequency-response curve in *Figure 37* shows that only moderate gains can be realized in the audio range. However, considering the reference, there are two independent amplifiers available, so that reasonable overall performance can be obtained.

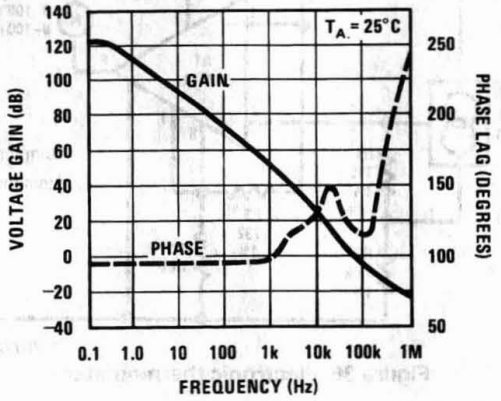

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Figure 37. Open loop frequency response

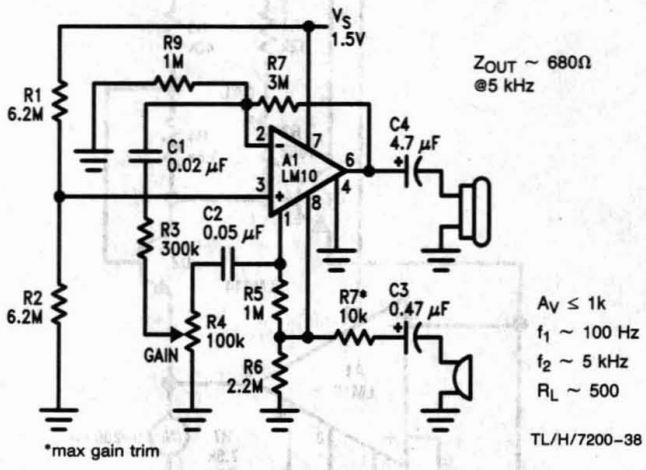
This is illustrated with the microphone amplifier shown in *Figure 38*. The reference, with a 500 kHz unity-gain bandwidth, is used as a preamplifier with a gain of 100. Its output is fed through a gain-control potentiometer to the op amp which is connected for a gain of 10. The combination gives a 60 dB gain with a 10 kHz bandwidth, unloaded, and 5 kHz loaded at 500Ω. Input impedance is 10 kΩ.

Potentially, using the reference as a preamplifier in this fashion can cause excess noise. However, because the reference voltage is low, the noise contribution, which adds root-mean-square, is likewise low. The input noise voltage in this connection is 40–50 nV/$\sqrt{\text{Hz}}$, about equal to that of the op amp.

One point to observe with this connection is that the signal swing at the reference output is strictly limited. It cannot swing much below 150 mV nor closer than 800 mV to the supply. Further, the bias current at the reference feedback terminal lowers the output quiescent level and generates an uncertainty in this level. These facts limit the maximum feedback resistance (R5) and require that R6 be used to optimize the quiescent operating voltage on the output. Even so, the fact that limited swing on the preamplifier can reduce maximum output power with low settings on the gain control must be considered.

In this design, no DC current flows in the gain control. This is perhaps an arbitrary rule, designed to insure long life with noise-free operation. If violations of this rule are acceptable, R5 can be used as the gain control with only the bias current for the reference amplifier (<75 nA) flowing through the wiper. This simplifies the circuit and gives more leeway on getting sufficient output swing from the preamplifier.

The circuit in *Figure 38* can also be modified to provide two-wire transmission for a microphone output.



TL/H/7200–38

Figure 38. Microphone amplifier

conclusions

The applications described here show that some truly unique functions can be performed by the LM10 because of the low-voltage capability and floating mode operation. Among these are accurate, two-terminal comparators that interface directly with most logic forms. They can also drive SCRs in control circuits using low-level sensors like photodiodes or thermocouples, although this was not explored here.

Two-wire transmitters for analog signals were shown to work with a variety of transducers, even to the extent of remotely performing computational functions. These might be used for anything from a microphone preamplifier to a strain gauge measuring stress at some remote location in an aircraft. The power requirements of this IC are modest enough to insure a wide dynamic range and permit operation with lower-voltage supplies.

The IC also proves to be quite useful in regulator circuits, as might be expected from a combined op amp and voltage reference. It makes an efficient series regulator at low voltages. And as a low-level, on-card regulator, it offers greater precision than existing devices. It is also easily applied as a shunt regulator or current regulator.

In the floating mode, it operates with the precision required of laboratory supplies, as either a voltage or current regulator. Maximum output voltage is limited only by discrete pass transistors, because the control circuit sees, at most, a couple volts. Therefore, output voltages of several hundred volts are entirely practical.

A few examples were given of amplifiers and signal conditioners for portable instruments. Emphasis was placed on single-cell operation as this gives the longest life at lowest cost from the smallest power source. The IC is well suited to single-supply operation, where it can be used in any number of standard applications. This can be put to use in digital systems where some linear functions must be performed. The availability of a reference allows precise level shifting or comparisons even when the supply is poorly regulated. The reference can also be used to create an elevated pseudo-ground so that split-supply techniques can be used.

Even when split supplies are available, the increased output capability (40V @ 20 mA) coupled with lower power consumption could well recommend the LM10. This is combined with the more satisfactory fault protection provided by thermal limiting.

acknowledgement

The authors would like to thank Dick Wong for his assistance in building and checking out the applications described here.

references

1. R. J. Widlar, "Low Voltage Techniques," *IEEE J. Solid-State Circuits*, Dec. 1978.

***See Addendum that follows this Application Note.**

Low Voltage Techniques*

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National Semiconductor
Technical Paper 14

Abstract. *A micropower operational amplifier is described that will operate from a total supply voltage of 1.1V. The complementary Class-B output can swing within 10 mV of the supplies or deliver ±20 mA with 0.4V saturation. Common-mode range includes V⁻, facilitating single-supply operation. Otherwise, DC performance compares favorably with that of the LM108. An adjustable-output voltage reference is also presented that uses a new technique to eliminate the bow usually found in the temperature characteristics of the band-gap reference. Minimum supply is 1V, and typical drift is 0.002%/°C.*

introduction

The intrinsic operating voltage limit of bipolar ICs is only 100–200 mV greater than the emitter-base voltage of the transistors. To date, this limit has been pushed only with digital circuitry and relatively simple linear devices. This paper will deal with techniques for fabricating such devices as operational amplifiers, comparators, regulators and voltage references that work from a voltage as low as that supplied by a single nickel-cadmium cell.

Field-effect transistors have been considered for low-voltage applications because their operating voltage can theoretically be made less than that of bipolar transistors. Although their transconductance equals that of bipolar devices at very-low currents, it is considerably less even at moderate current densities. This limits FETs to such functions as input stages where the operating current is relatively low and well controlled.

A combined op amp, voltage reference and reference amplifier was chosen as a design example. A functional diagram is given in *Figure 1*. This configuration will serve to demonstrate that the usefulness of low-voltage operation goes beyond battery-powered equipment. It can be used in a floating mode, independent of fixed supplies. This is illustrated both by the floating voltage regulator in *Figure 2*, where the IC operates from the drive voltage to the pass transistors, and the remote comparator in *Figure 3*, where the IC functions as a 2-terminal device, driving TTL logic directly. A wide range of similar applications have been developed and are discussed elsewhere.[1]

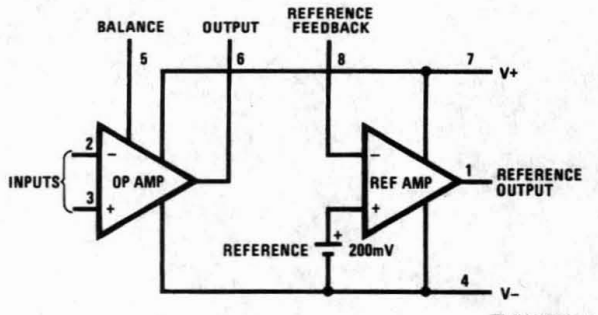

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Figure 1. Functional diagram of the design example

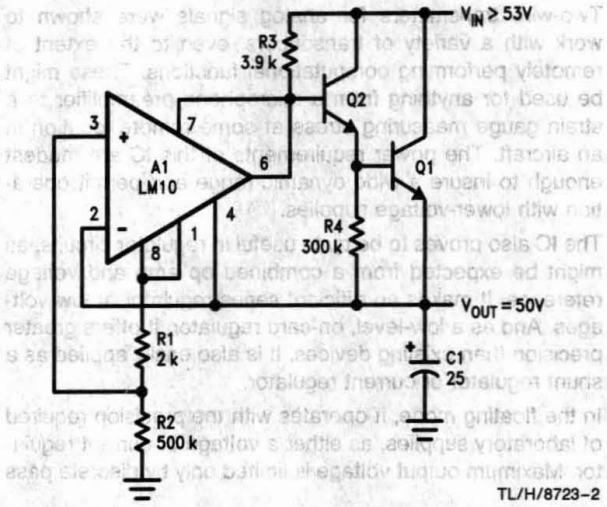

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Figure 2. High voltage regulator with bootstrapped control amplifier

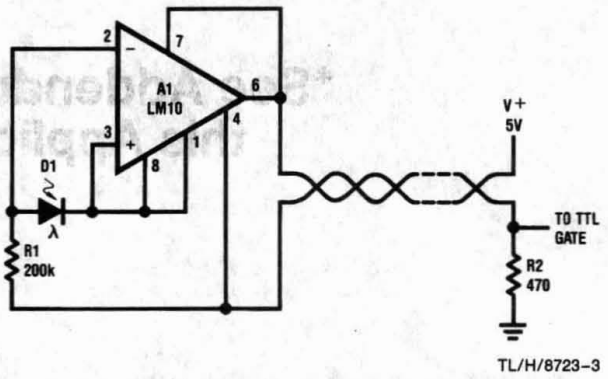

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Figure 3. Light level detector driving TTL directly over 2-wire line

Some small advantage might be gained by limiting operation to low voltages. This is overshadowed by the benefits of making a general-purpose IC. Therefore, it was decided to use standard processing with maximum operating voltages limited only by the BV_{CEO} of the transistors (50V–60V).

Ion-implanted resistors were incorporated to obtain the necessary high values for micropower operation. They also have the advantage that, with proper design, the speed/power tradeoffs can be determined at the final stages of processing by varying the implant dose. However, the advisability of doing this on a production basis has yet to be established.

operational amplifier design

A simplified schematic of the op amp is given in *Figure 4*. Lateral PNP transistors are used on the input because this is the easiest way to secure operation at common-mode voltages equal to the negative supply voltage. Processing that yields typical PNP current gains greater than 100 at low

*Reprinted from *IEEE Journal of Solid-State Circuits*, December, 1978.

†This work was performed under contract to National Semiconductor Corporation, Santa Clara, California.

currents has been in production for nearly 10 years. These lateral transistors also have relatively constant current gain over temperature, giving lower bias-current drift than NPNs.

Protective resistors have been included in the input leads so that current does not become excessive when the inputs are forced below the negative supplies, forward biasing the base tubs.

Offset nulling is accomplished by connecting the balance terminal to a variable voltage derived from the reference output. Both the input-stage current and the reference are tightly regulated over temperature, and the resistance of the adjustment potentiometer can be made very much lower than the resistance looking back into the balance pin. Therefore, offset nulling can produce a minimum-drift condition.

Proceeding through the circuit, the input stage is buffered by vertical PNP followers, Q3 and Q4. This differential signal is converted to single ended by Q5 and Q6 and fed to the base of the second-stage amplifier Q7.

This configuration is not inherently balanced in that the emitter-base voltage of the vertical PNPs is required to match that of the NPNs. As will be seen, the final circuit does include circuitry to correct for the expected variations.

From the collector of Q7, the signal splits, driving separate halves of the complementary Class-B output stage. The NPN output transistor, Q25, is driven through Q13 and Q14. This complementary emitter follower arrangement provides the necessary current gain without requiring the extra bias voltage of a Darlington connection. This is essential in realizing minimum-voltage operation.

Base drive for the NPN output transistor is initially supplied by Q12, but a boost circuit has been added to increase the available drive as a function of load current. This is accomplished with Q24 in conjunction with a current inverter. The inclusion of R23 prevents gross over boosting.

The boost amounts to controlled positive feedback. It does tend to reduce dead zone and linearize gain. Excess boost current is absorbed by Q14, which presents a low enough drive impedance so that the voltage transfer function from its base does not exhibit a negative-gain characteristic. Considerable experience with this and similar boost circuits shows that they do not unfavorably alter frequency response, at least below a few megahertz.

Drive for the PNP half of the output is somewhat more complicated. Again, a compound buffer, Q15 and Q16, is used, although to maintain circuit balance rather than for current gain. The signal proceeds through two inverters, Q17 and Q19, to obtain the correct phase relationship and DC level shift, before it is fed to the PNP output transistor, Q28.

This path has three common-emitter stages; and, potentially, much higher gain than the NPN side. The gain is equalized, however, by the shunting action of Q18-R19 and Q21-R22 as well as negative feedback through Q23.

When the output PNP saturates, Q20 serves to limit its base overdrive with a feedback path to the base of Q17. This is also important to the floating-mode operation of *Figures 2* and *3* in that it disables the PNP drive circuitry when the op amp output is connected to V^+.

The complete schematic of the operational amplifier in *Figure 5* shows the remaining design features. The lower collector on Q1 is outside the normal collector. Its current is quite low until the positive common-mode limit is exceeded, saturating the normal collector of Q1. The auxiliary collector picks up the re-injected current in saturation, which is routed through Q4 to the collector of Q3. When, for example, the amplifier is connected as a follower, this prevents false outputs when the common-mode limit is exceeded. In normal operation, the low-level leakage from the auxiliary collector is evenly divided between the input-stage collectors because the voltage drop across R4 is small.

An extra emitter on Q2 working with Q18 performs a similar function when the negative common-mode limit is exceeded on the inverting input, insuring that the output will be in positive saturation. The non-inverting input is also arranged to give a proper output when the input is driven below V^-.

As mentioned earlier, the optimum collector current of Q13 will depend on the V_{BE} difference between NPN and PNP transistors (Q9-Q10 and Q7-Q13). This is compensated by generating a similar difference current with Q21 and Q22 then processing it with Q19, Q17 and Q15 to generate the required complement in the collector circuit of Q13.

The output stage has been designed to deliver a minimum output current of ± 20 mA with a typical saturation voltage of ± 0.4V. Conventional current limiting cannot be used without significantly increasing the saturation voltage. Since the current gain of lateral PNPs falls off severely at high current and high temperature, it is only necessary to limit the driver current. This is done with R42 and R43, with Q44 insuring that supply current does not become excessive if the BV_{CEO} of Q45 is exceeded on supply transients.

Current limit for the NPN side is done with Q51, Q53 and associated circuitry. In addition, Q49 and Q52 have been added to limit the over boost, should it become larger than can be handled by Q35.

The maximum operating voltage and output current of this device are high enough that current limiting cannot be expected to prevent excessive die temperature, especially with worst-case conditions. Therefore, thermal overload protection has been provided. Die temperature is sensed with Q25, and Q26 introduces hysteresis into the limiting characteristic. The cut out temperature is designed to be 165°C, with operation resuming when the die cools to 155°C. The NPN and PNP halves are shut off by Q27 and Q29, respectively.

Output stage quiescent current is determined by the voltage across R16 and various device geometries. The current is stabilized for varying supply voltage by connecting Q33 in cascode with Q30 and by the addition of Q31 and Q32, which tend to compensate for the collector voltage sensitivity of emitter-base voltage.

At temperatures approaching thermal limit, Q40 must operate beyond the threshold of saturation. The addition of Q39, which is actually a lateral PNP collector ring surrounding the base of Q40, produces a voltage drop across R34 to compensate for the drop across R35 caused by excess base current.

frequency compensation

With feedback amplifiers, the ability to frequency compensate a particular design is generally the bottom line in determining its usefulness. Considering the number of stages involved and the fact that the drive paths for the PNP and NPN output transistors are entirely different, one might rightly conclude that frequency compensation would be difficult.

As much of the frequency compensation network as can be explained in a straightforward manner is shown in the simplified schematic of *Figure 4*. Overall compensation is provided by a MOS capacitor, C2, between the output and the collector of an input transistor. Within this loop, a diffused capacitor, C1, rolls off the gain of Q7, breaking back out where $X_{C1} = R6$.

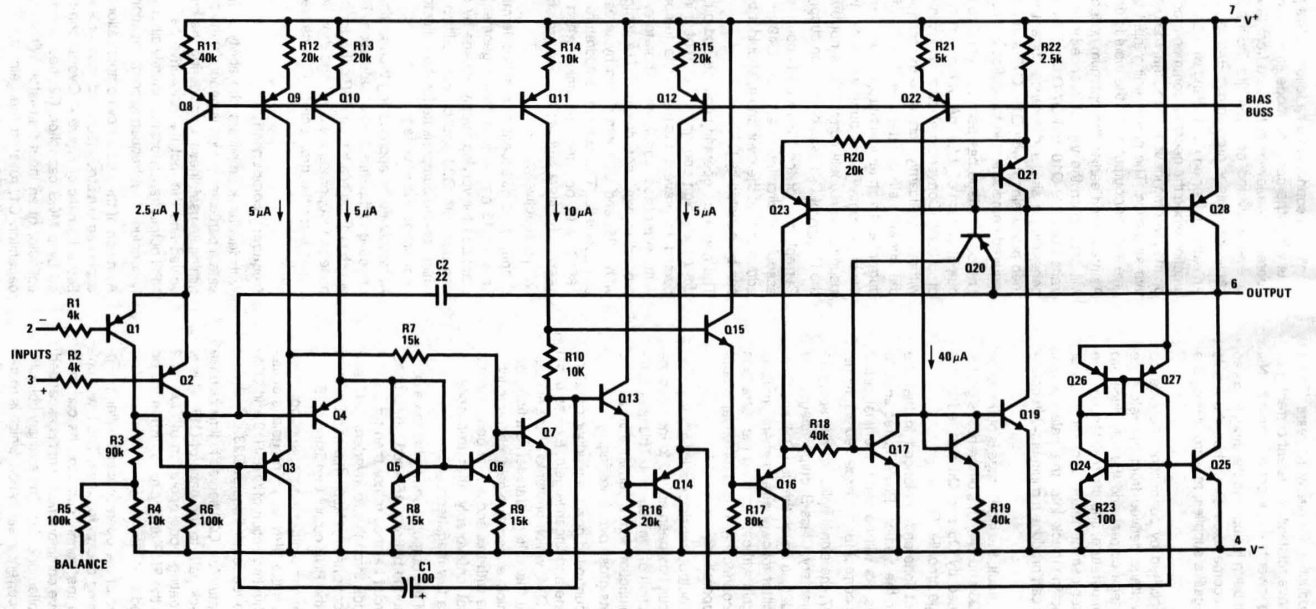

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Figure 4. Essential details of the op amp

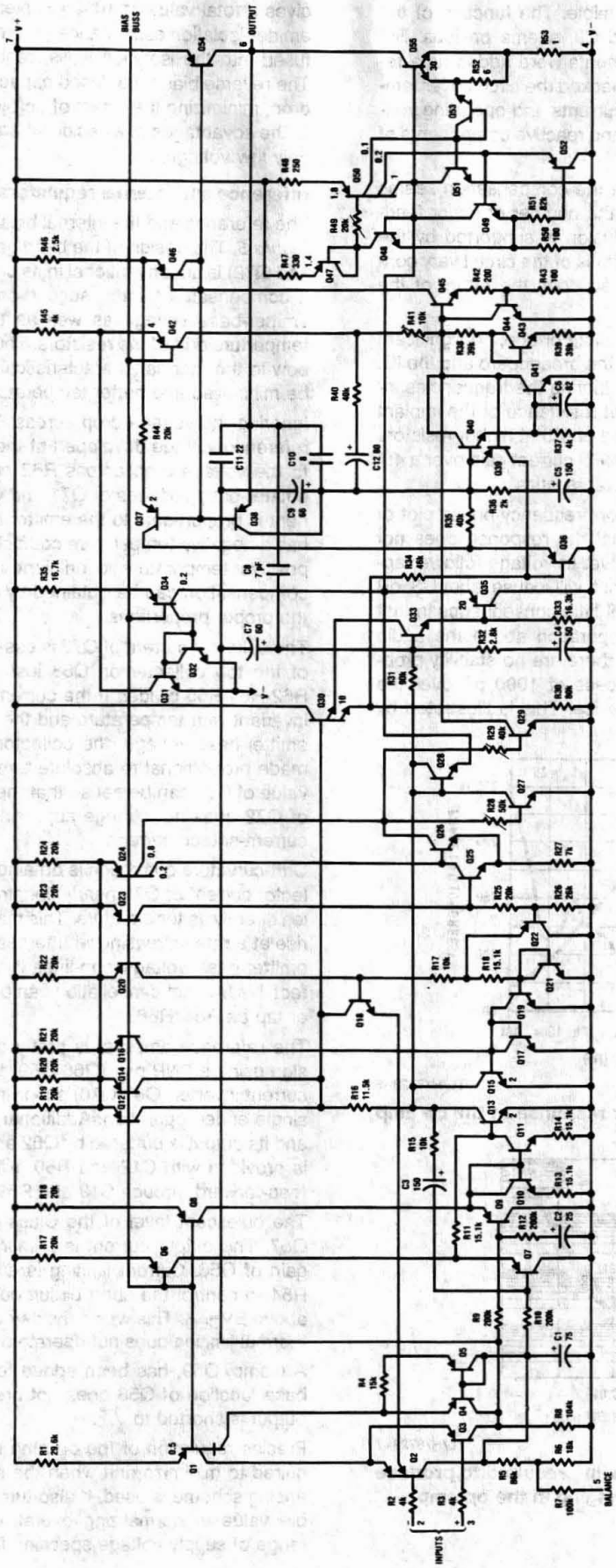

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Figure 5. Complete op amp schematic

Referring again to the complete schematic, it can be seen that things are not really that simiple. The function of the feed-forward capacitors, C7 and C9, seems obvious. But remaining compensation components were added as a result of breadboard tests which checked the circuit over temperature with full range of load currents and operating voltages, while varying the resistive and reactive components of load impedance.

A detailed theoretical analysis of the compensation seems overly complicated, considering the number of minor feedback loops involved. This conclusion is supported by the fact that impedance levels in portions of the circuit vary considerably with load current and so does the effect of the frequency-shaping circuits.

Results show the circuit to be stable. For one, no significant differences were found between the breadboard and the IC. This is not overly surprising considering the frequencies involved. Further, varying the sheet resistance of the implant resistors over a 5:1 range showed only that higher resistors made slower amplifiers. Varying NPN current gain over a 4:1 range had little effect on AC characteristics.

Figure 6 is a plot of the open-loop frequency-phase plot of the amplifier. It can be seen that the response does not exactly follow a 6 dB/octave curve. In voltage follower applications, the excess phase shift will cause about 3 dB peaking around 35 kHz. This is of little consequence in that the circuit is not intended for operation above the audio range. What is important is that there are no stability problems for capacitive loads in excess of 1000 pF over the entire operating range of the device. This is illustrated by the plot in *Figure 7*.

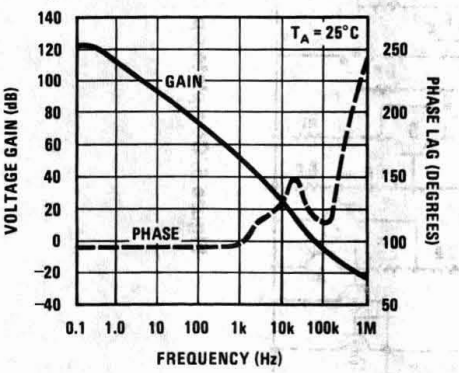

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Figure 6. Open loop frequency response of the op amp

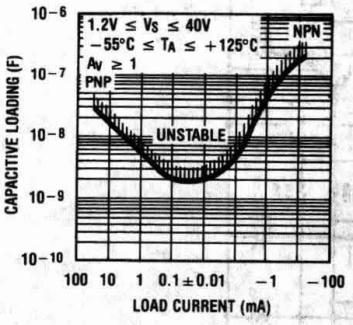

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Figure 7. Plot of capacitive loading required to produce excessive transient ringing in the op amp

A tally of the compensation capacitance for the entire circuit gives a total value of 1000 pF. Nearly all of this is diffused emitter-isolation capacitance (~1 pF/mil^2), and most is diffused into the isolation walls, requiring no extra die area. The reverse bias on diffused capacitors is less than a diode drop, minimizing the effect of soft junctions. This is but one of the advantages of a design where most of the circuit sees only low voltage.

reference and internal regulators

The reference and the internal biasing circuitry are shown in *Figure 8*. The design of the band gap reference[2] (using Q71 and Q72) is unconventional in its configuration and because it compensates for the second-order nonlinearities in the emitter-base voltage as well as those introduced by the temperture drift of the resistors. Thus, the uncompensatable bow in the thermal characteristics of standard devices can be minimized and better temperature stability obtained.

Ignoring the voltage drop across R61 for the moment, the reference voltage developed at the emitter of Q71 is equal to the voltage drop across R62 plus the difference in the emitter-base voltages of Q71 and Q72. The former component is proportional to the emitter-base voltage of Q72 and has a negative temperature coefficient while the latter has a positive temperature coefficient. First order temperature compensation can be obtained by adding these voltages in the proper proportions.

The collector current of Q72 is essentially the output current of the top collector on Q68 less the current through the R62-R64-R66 divider. If the current-source current (Q68) is invariant with temperature and the divider current varies as emitter-base voltage, the collector current of Q72 can be made proportional to absolute temperature. This done, the value of R61 can be set so that the voltage on the collector of Q72 does not change appreciably for small changes in current-source current.

Drift-curvature correction is obtained by maintaining the collector current of Q71 nearly constant while that of Q72 varies directly as temperature. This makes the reference output rise at a rate increasing with temperature. Resistor drift and emitter-base voltage non-linearities have the opposite effect. Near-exact cancellation can be obtained with the proper tap on R64/R66.

The reference amplifier is pretty much a conventional design using a PNP pair (Q66-Q69) for the input, with a NPN current inverter (Q67-Q70) supplying gain and converting to single ended operation. Additional gain is supplied by Q64, and its output is buffered by Q62 and Q56. Frequency rolloff is provided with C12 and R60, with a lead established by feed-forward through C13 and R59.

The quiescent level of the Class-A output stage is set by Q57. The output current is primarily limited by the current gain of Q56. Current limiting is added with Q58, Q61 and R54 to control the short circuit current for supply voltages above BV_{CEO}. This was considered necessary because the thermal limiting does not operate on the reference amplifier.

A clamp, Q59, has been added to insure that the emitter-base junction of Q56 does not break over if the reference output is shorted to V^+.

Precise regulation of the op amp input stage current is required to minimize drift when the recommended offset balancing scheme is used. It also turns out to be of considerable value in normalizing overall operation over the 40:1 range of supply voltage specified for the device.

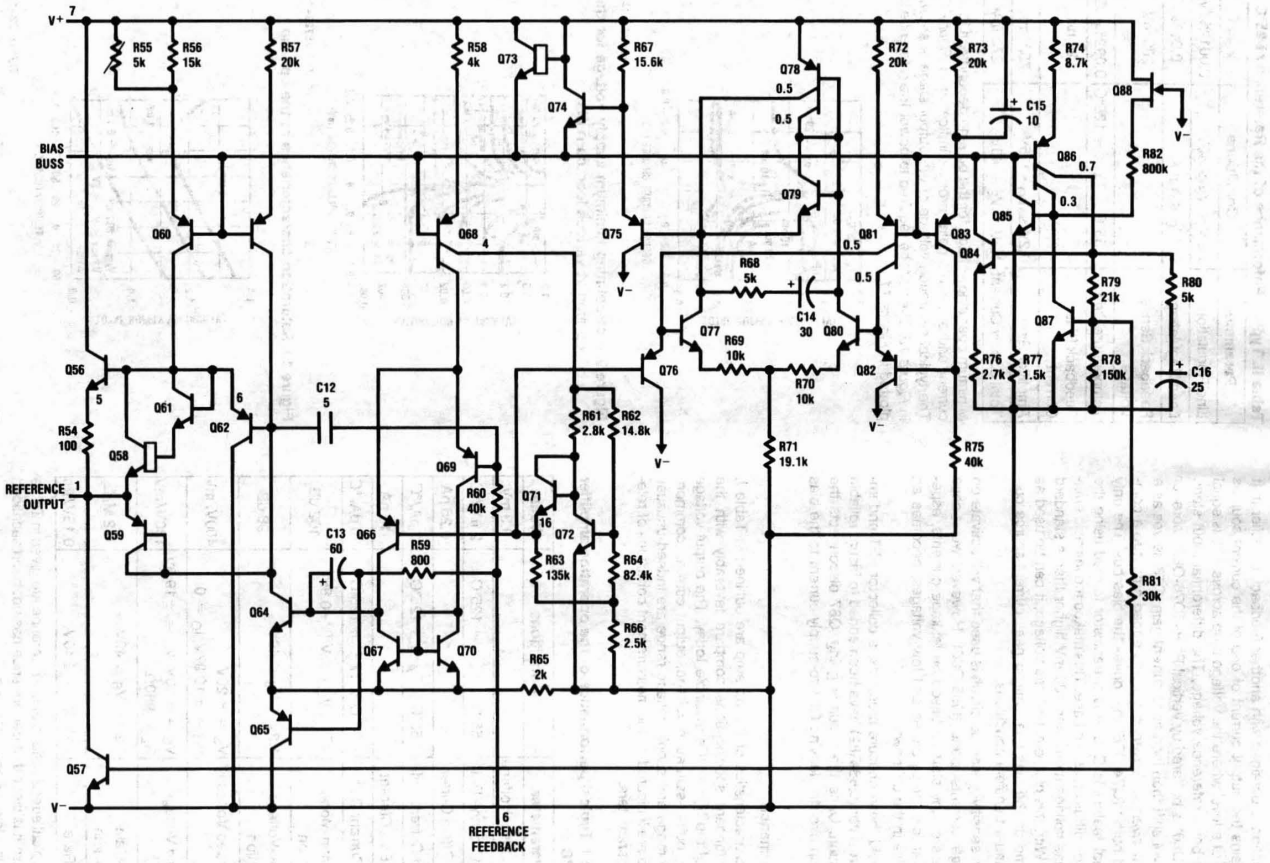

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Figure 8. Complete schematic of the reference and internal regulators

Regulation is obtained with another feedback amplifier that maintains the output current of one of the current sources (Q83) at a level where the voltage drop across R75 is equal to the basic reference voltage. The differential input stage (Q77-Q80) is buffered by vertical PNPs (Q76-Q82) more for DC level shift than increased current gain. Q78 serves as a current inverter, delivering a single-ended output to a compound buffer (Q74-Q75) that drives the bias bus. The only unusual feature is Q73. It is a transistor formed using the isolation diffusion as the base. This makes the intrinsic emitter-base voltage more than 100 mV higher than a standard NPN. With this high emitter-base voltage, it can be used as a clamp on the bias bus, limiting peak current-source current under transient conditions.

A high sensitivity start-up circuit is used that will activate on leakage currents alone (Q85-Q86). However, worst-case analysis of any start up based on leakage currents, especially at low temperatures and low voltages, becomes an exercise in the unknown.

To avoid these obscure problems, a collector FET and implant resistor (Q88-R82) have been added to insure reliable operation. Once the circuit is going, Q87 disconnects the start-up circuitry, leaving Q84 to supply current to the bias bus.

performance

The characteristics of the op amp are outlined in Table I. The standard specifications compare favorably with the best of the bipolar ICs available today. The output-voltage swing, output-saturation voltage, output current, common-mode range and supply-voltage range are indeed unusual. These are indicated by the measurement conditions of relevant parameters.

Table I. Typical performance of the operation amplifier at 25°C

Parameter	Conditions	Value
Input Offset Voltage		0.3 mV
Offset Voltage Drift	$-55°C \le T_A \le +125°C$	2 μV/°C
Input Offset Current		0.25 nA
Offset Current Drift	$-55°C \le T_A \le +125°C$	2 pA/°C
Input Bias Current		10 nA
Bias Current Drift	$-55°C \le T_A \le +125°C$	60 pA/°C
Common-Mode Rejection	$V^- \le V_{CM} \le V^+ - 0.85V$	102 dB
Supply-Voltage Rejection	$1.2V \le V_S \le 40V$	96 dB
Unloaded Voltage Gain	$V_S = \pm 20V$, $V_O = \pm 19.97V$, $I_O = 0$	400V/mV
Loaded Voltage Gain	$V_S = \pm 20V$, $V_O = \pm 19.6V$, $R_L = 980\Omega$	130V/mV
Unity-Gain Bandwidth	$1.2V \le V_S \le 40V$	0.2 MHz
Slew Rate	$1.2V \le V_S \le 40V$	0.15V/μs

The typical specifications of the reference are given in Table II. Again it is clear that performance has not been sacrificed to realize low-voltage operation.

Table II. Typical Peformance of the Reference at 25°C

Parameter	Conditions	Value
Line Regulation	$1.2\ V \le V_S \le 40V$	0.001 %/V
Load Regulation	$0 \le I_O \le 1$ mA	0.01%
Feedback Sense Voltage		200 mV
Temperature Drift	$-55°C \le T_A \le +125°C$	0.002%/°C
Feedback Bias Current		20 nA
Amplifier Gain	$0.2V \le V_O \le 75V$	75 V/mV
Total Supply Current	$1.2V \le V_S \le 40V$	270 μA

Minimum operating voltage for the op amp depends on load current and allowable gain error as indicated in *Figure 9*. The typical saturation voltage of the output stage is shown in *Figure 10*. The voltage required to power the reference is plotted in *Figure 11*.

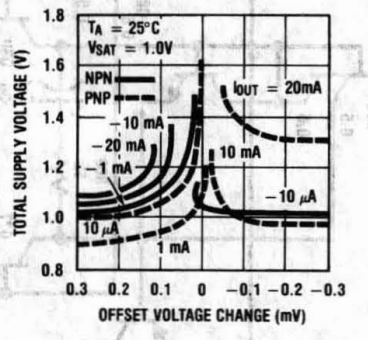

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Figure 9. Plot defining minimum supply voltage for the op amp at various load currents

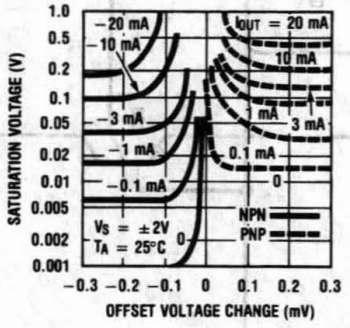

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Figure 10. Saturation characteristics of the op amp

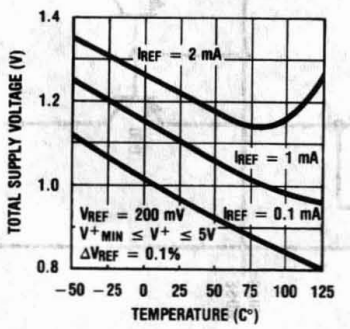

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Figure 11. Minimum supply voltage of the reference as a function of temperature

The total supply current for the complete IC is typically 270 μA. This is impressive only considering the performance and complexity of the circuit. This current might be reduced by a factor of 4, at the expense of speed, by raising the sheet resistance of the implanted resistors.

general

Except for the inclusion of implanted resistors, processing is essentially the same as that developed in 1968 for the LM101A. The high sheet resistivities obtained with implanted resistors strongly recommend them for micropower devices, especially at high levels of complexity. But implanted resistors have a lower breakdown voltage than their diffused counterparts (40V vs 100V). This is caused by the reduced radius of curvature at the junction edges. With higher sheet resistivities, a significant voltage coefficient of resistivity will be observed (resulting in a carrier depletion of about 10^{12} cm^{-2} at the BV_{CEO} of the NPN transistors). These factors recommended that caution be used when operating implant resistors at higher voltages or that they be operated at low voltages where possible. In the circuit under discussion, none of the implant-resistor junctions see the full supply voltage.

A consequence of this low voltage design is that most of the low-level circuitry is operating at junction biases of little more than a diode drop. At this voltage, junctions are not greatly affected by minor defects. Further, in this circuit, most areas that see full supply voltage can tolerate several microamperes of leakage before operation is affected in the least. This can be expected to increase both reliability and manufacturing yield. The overall yield will also be improved because there is a substantial market for devices that will work only at low voltages.

The complete IC is built on a 97 x 105 mil die, shown in *Figure 12*. This is definitely large for an op amp, even when combined with a reference. But with 3-inch wafers and modern processing, die size is not the prime determinant of selling price, as long as reasonable yields are maintained. This is evidenced by the low cost of regulators having equal die area and encapsulated in more expensive power packages.

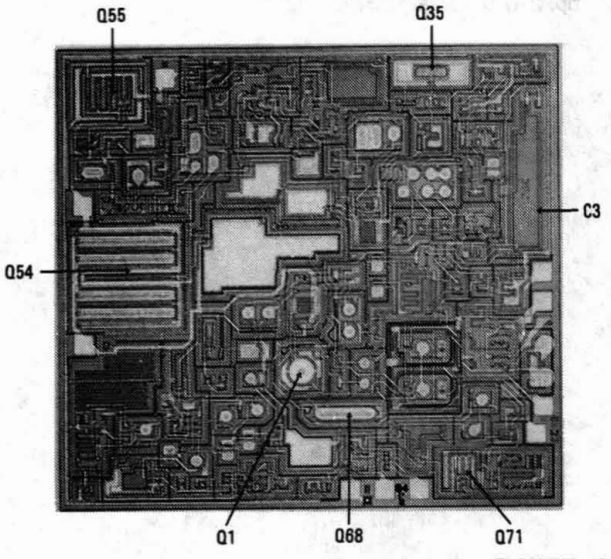

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Figure 12. Photomicrograph of the IC

As can be seen from *Figure 12*, the input-stage current-source, Q1, has been made with about 3 times the base width of the other current-source transistors. This serves both to give it the same emitter-base voltage at roughly half the current density and to make it less sensitive to changes in collector-base voltage. The latter contributes directly to improved common-mode rejection.

To save space, several lateral PNP current-sources have been built with a combination of linear emitter and emitter on a radius. Q68 in *Figure 12* is an example of this. The current density at circular emitters is higher than linear emitters for a given bias voltage. This must be accounted for in design.

As mentioned earlier, operating biases in several places are determined by the difference in the emitter-base voltage between NPN and PNP transistors. Hence, a knowledge of these differences is essential to avoid production problems.

Since the output transistors of the op amp can dissipate considerable power, thermal gradients are potentially a problem. The effects of this dissipation have been measured and the results plotted in *Figure 13*. It is evident that the thermal gradients are well in hand even with 400 mW dissipation. The thermal gradient feed-through into the reference is also plotted in *Figure 14*. Clearly it will be insignificant at the power levels encountered in practical designs. Thermal gradient isolation is primarily the result of careful layout, since many points within the circuit are sensitive. The difficulties are, of course, mitigated by the large die size.

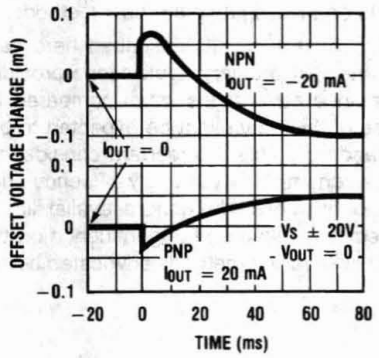

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Figure 13. Effect of a pulsed load on the offset voltage of the op amp showing electrical change and that caused by thermal gradients

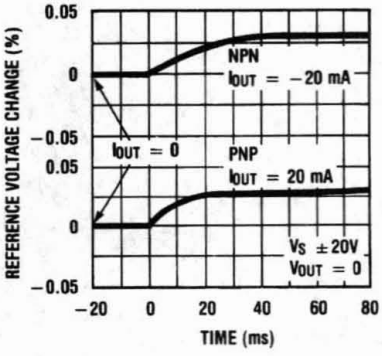

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Figure 14. Cross-coupling from the op amp to the reference caused by thermal gradients

applications

There are many obvious uses for precision functions such as op amps, voltage comparators and voltage references that are capable of operating at low voltages with a small power drain. These include a variety of portable instruments, remote telemetry and even implanted medical devices.

With this battery powered equipment, there is a decided advantage in reducing operating voltage to that of a single cell. The power source will be more simple, less costly and have a higher energy content for a given size and weight. In many respects, current requirements for a given application do not decrease linearly with available supply voltage, giving an even greater advantage to single-cell operation. The resulting increase in the capacity of the power source coupled with the low drain of the electronics could eliminate the need for ON/OFF switches in certain applications.

The control circuits described earlier (*Figures 2* and *3*) that operate from residual voltages independent of fixed supplies suggest an entirely new range of equipment-design possibilities, even with line-operated power supplies. In general, the usefulness of this approach suffers greatly if minimum operating voltage is much above a volt. Low idling current is also an important consideration.

It is difficult to evaluate the impact of these new approaches mainly because they seem to represent a step change in how things can be done at the equipment-design level. But considering that low-voltage operation can be realized with no sacrifice in performance, it would seem that there are few restraints on investigating the new methods.

As a practical matter, the IC described here can also be used in a variety of ordinary applications providing significant performance advantages when compared to existing ICs. Because of this they might be expected to become an "industry standard". This is important considering the volume-related economies that strongly influence pricing in the semiconductor business. The general availability of the part can be expected to have a strong influence on the investigation of the new design methods advocated here and elsewhere.[1]

conclusions

It has been shown here that high-performance linear circuits can be designed to operate with little more than a volt of supply voltage. This precludes many standard design methods that require more than two diode drops of bias. Notable among these is the Darlington connection. Alternate techniques can result in a significant increase in complexity. However, this is not a serious problem with modern manufacturing methods, providing that reasonable yield can be maintained.

Although the 270 μA power drain of the example used is not overly impressive in the realm of micropower, it should be remembered that it is a fairly complex function designed for $-55°C$ to $+125°C$ operation and capable of delivering more than 20 mA of output current. A more specialized device could be built with less than a tenth the drain, especially if the maximum operating temperature could be restricted to 85°C. At elevated temperatures and low currents, the emitter-base voltage of a transistor approaches the saturation offset voltage, creating circuit problems.

In general, feedback amplifiers with more complicated signal paths become more difficult to frequency compensate. The benefits to be gained (i.e., saturating outputs and extended common-mode range) are probably justified only in low-voltage circuits. The isolation-wall capacitors introduced here ease the compensation problem some. A typical integrated circuit (LM108) has over 1000 pF of this capacitance available with no area penalty. Nonetheless, stabilizing some designs requires perseverance.

acknowledgement

Special thanks are due to Mineo Yamatake and Bob Dobkin at National Semiconductor Corporation for invaluable assistance in frequency compensating the op amp and other contributions to the final design.

references

1. R. J. Widlar, "New Op Amp Ideas", (to be published).
2. R. J. Widlar, "New Developments in IC Voltage Regulators", *IEEE J. of Solid-State Circuits,* Vol. SC-6, No. 1, pp. 2–7, February 1971.

Super Matched Bipolar Transistor Pair Sets New Standards for Drift and Noise

National Semiconductor
Application Note 222

Matched bipolar transistor pairs are a very powerful design tool, yet have received less and less attention over the last few years. This is primarily due to the proliferation of high-performance monolithic circuits which are replacing many designs previously implemented with discrete components. State-of-the-art circuitry, however, is still the realm of the discrete component, especially because of recent improvements in the components themselves.

It has become clear in the past few years that ultimate performance in monolithic transistor pairs was being limited by statistical fluctuations in the material itself and in the processing environment. This led to a matched transistor pair fabricated from many different individual transistors physically located in a manner which tended to average out any residual process or material gradients. At the same time, the large number of parallel devices would reduce random fluctuations by the square root of the number of devices.

The LM194 is the end result. It is a monolithic bipolar matched transistor pair which offers an order-of-magnitude improvement in matching properties and parasitic base and emitter resistance over conventional transistor pairs. This was accomplished without compromising breakdown voltage or current gain. The LM194 is specified at 40V minimum collector-to-emitter breakdown voltage and has a minimum h_{FE} of 500 at 1 mA collector current. Maximum offset voltage is 50 μV over a collector current range of 1 μA to 1 mA. Maximum h_{FE} mismatch is 2%. Common mode rejection of offset voltage (dV_{OS}/dV_{CB}) is 124 dB minimum. An added benefit of paralleling many transistors is the resultant drop in overall r_{bb} and r_{ee}, which are 40Ω and 0.4Ω respectively. This makes the logarithmic conformity of emitter-base voltage to collector current excellent even at higher current levels where other devices become non-theoretical. In addition, broadband noise is extremely low, especially at higher operating currents.

The key to the success of the LM194 is the nearly one-to-one correlation between measured parameters and those predicted by a theoretical bipolar transistor model. The relationship between emitter-base voltage and collector current, for instance, is perfectly logarithmic over an extremely wide range of collector currents, deviating in the pA range because of leakage currents and above several milliamperes due to the finite 0.4Ω emitter resistance. This gives the LM194 a distinct advantage in non-linear designs where true logarithmic behavior is essential to circuit accuracy. Of equal importance is the absolute nature of the logarithmic constant, both between the two halves of the device and from unit to unit. The relationship can be expressed as:

$$V_{BE_1} - V_{BE_2} = \frac{kT}{q} \ln \left(\frac{I_{C_1}}{I_{C_2}}\right)$$

This relationship holds true both within a single transistor where I_{C_1} and I_{C_2} represent two different operating currents and between the two halves of the LM194 where collector currents are unbalanced. Of particular importance is the fact that the kT/q logarithmic constant is an absolute quantity dependent only on Boltzman's constant (k), absolute temperature (T), and the charge on the electron (q). Since these values are independent of processing, there is virtually no variation from unit to unit at a fixed temperature. Lab measurements indicate that the logarithmic constant measured at a 10:1 collector current ratio does not vary more than $\pm 0.5\%$ from its theoretical value. Applications such as logarithmic converters, multipliers, thermometers, voltage references, and voltage-controlled amplifiers can take advantage of this inherent accuracy to provide adjustment-free precision circuits.

APPROACHING THEORETICAL NOISE

In many low-level amplifier applications, the limiting factor on performance is noise. With bipolar transistors, the theoretical value for emitter-base voltage noise is a function only of absolute temperature and collector current.

$$e_n = kT\sqrt{\frac{2}{qI_C}} \quad \text{Volts}/\sqrt{\text{Hz}}$$

This formula indicates that voltage noise can be reduced to low levels by simply raising collector current. In fact, that is exactly what happens until collector current reaches a level where parasitic transistor noise limits any further reduction. This "noise floor" is usually created by and modeled as an equivalent resistor (r_{bb}') in series with the base of the transistor. Low parasitic base resistance is therefore an important factor in ultra-low-noise applications where collector current is pushed to the limits. The 40Ω equivalent r_{bb}' of the LM194 is considerably lower than that of other small-signal transistors. In addition, this device has no excess noise at lower current levels and coincides almost exactly with the predicted values. A low-noise design can be done on paper with a minimum of bench testing.

Another noise component in bipolar transistors is base current noise. For any finite source impedance, current noise must be considered as a quadrature addition to voltage noise.

$$\begin{matrix}\text{total equivalent} \\ \text{input voltage noise}\end{matrix} = e_N = \sqrt{e_n^2 + (i_n \bullet r_s)^2} \text{Volts}/\sqrt{\text{Hz}}$$

where r_s is the source impedance

In the LM194, base current noise is a well-defined function of collector current and can be expressed as:

$$i_n = \sqrt{\frac{2q \bullet I_C}{h_{FE}}} \quad \text{Amps}/\sqrt{\text{Hz}}$$

To find the collector current which yields the minimum overall equivalent input noise with a given source impedance, the total noise formula can be differentiated with respect to I_C and set equal to zero for finding a minimum.

$$e_N^2 = e_n^2 + (i_n^2 \bullet r_s^2) + 4\,kT \bullet r_s$$

$$(4\,kT \bullet r_s = \text{noise}^2 \text{ of } r_s)$$

$$= \frac{2k^2 \bullet T^2}{q \bullet I_C} + \frac{2q \bullet I_C \bullet r_s^2}{h_{FE}} + 4kT \bullet r_s$$

$$\frac{d(V_N^2)}{d(I_C)} = \frac{-2k^2 \bullet T^2}{q \bullet I_C^2} + \frac{2q \bullet r_s^2}{h_{FE}} = 0$$

$$I_C\,(\text{optimum}) = \frac{kT}{q} \bullet \frac{\sqrt{h_{FE}}}{r_s}$$

For very low source impedances, the 40Ω r_{bb}' of the LM194 should be added to r_s in this calculation. A plot of noise figure versus collector current (see curve) shows that the formula does indeed predict the optimum value. The curves are very shallow, however, and actual current can be varied by 3:1 without losing more than 1 dB noise figure in most cases. This may be a worthwhile tradeoff if low bias current ($I_C < I_{opt}$) or wide bandwidth ($I_C > I_{opt}$) is also important *Figure 1* is a plot of best obtainable noise figure versus

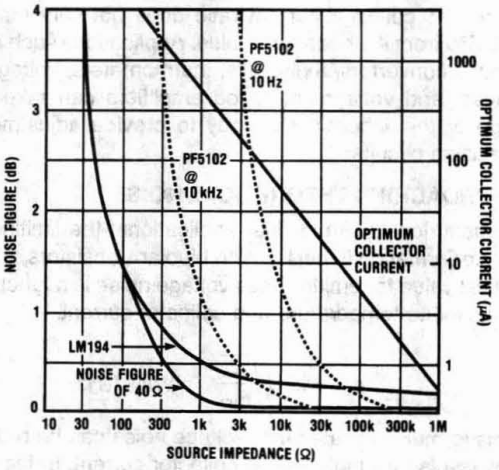

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FIGURE 1. Noise Figure vs Source Impedance

source impedance for the LM194 and a very low noise junction FET (PF5102). Collector current for the LM194 is optimized for each source impedance and is also plotted on the graph using the right side scale. The PF5102 is operated at a constant 1 mA. It is obvious that the bipolar device gives significantly better noise figures for low source impedances and/or low frequencies. FETs are particularly poor at very low frequencies (< 10 Hz) and offer advantages only for very high source impedances.

REACTIVE SOURCES

Calculations may also be done to derive an optimum collector current when the signal source is reactive. In this case, upper and lower frequencies (f_H and f_L) must be specified. Also, optimum current is different for an amplifier with a summing junction input ($Z_{IN} = 0$) as compared to a high impedance input ($Z_{IN} \gg X_C, X_L$). The formulas below give optimum collector current for noise within the frequency band f_L to f_H. For audio applications, lowest "perceived" noise may be somewhat different because of the variation in sensitivity of the ear to frequencies in the audio range (Fletcher-Munson effect).

Capacitive source into high impedance:

$$I_C\,(\text{opt}) = \frac{kT}{q} \bullet C \bullet 2\pi \bullet \sqrt{h_{FE}} \bullet \sqrt{f_H \bullet f_L}$$

Capacitive source into summing junction:

$$I_C\,(\text{opt}) = \frac{kT}{q} \times \frac{\sqrt{h_{FE}}}{R_f} \times \sqrt{\frac{4\pi^2 \bullet R_f^2 \bullet C^2 (f_L^2 + f_H^2 + f_L \bullet f_H)}{3} + \frac{4\pi \bullet R_f \bullet C \bullet (f_H + f_L)}{2} + 1}$$

Inductive source into high impedance:

$$I_C\,(\text{opt}) = \frac{\frac{kT}{q} \bullet \sqrt{h_{FE}}}{2\pi \bullet L} \sqrt{\frac{3}{f_L^2 + f_H^2 + f_L \bullet f_H}}$$

Keep in mind that the simple formula for total input-referred noise, though accurate in itself, does not take into account the effects of noise created in additional stages or noise injected from supply lines. In most cases voltage gain of the LM194 stage will be sufficient to swamp out second stage effects. For this to be true, first stage gain must be at least $3 \bullet v_{n2}/v_N$, where v_{n2} is the voltage noise of the second stage and v_N is the desired total input referred voltage noise. A simple formula for voltage gain of an LM194 stage, assuming no second stage loading, is given by:

$$A_V = \frac{(R_L)(I_C)}{kT/q} \text{ where } R_L \text{ is the load resistor}$$

Noise injected from power supplies is an often overlooked problem in low noise designs. This is probably in part due to the use of IC op amps with their high power supply rejection ratio and differential inputs. Many low-noise designs are single-ended and do not enjoy the inherent supply rejection of differential designs. For a single-ended amplifier with its load resistor tied directly to the power supply, noise on the supply must be no higher than $(R_L \bullet I_C \bullet v_N)/(3\ kT/q)$ or noise performance will be degraded. For a differential stage (see *Figure 2*) with the common emitter resistor tied to the negative supply and the collector resistors tied to the positive supply, supply noise is not generally a problem, at least at low frequencies. For this to be true at higher frequencies, the capacitance at the collector nodes must be kept low and balanced. In an unbalanced situation, noise from either supply will feed through unattenuated at higher frequencies where the reactance of the capacitor is much lower than the collector resistance.

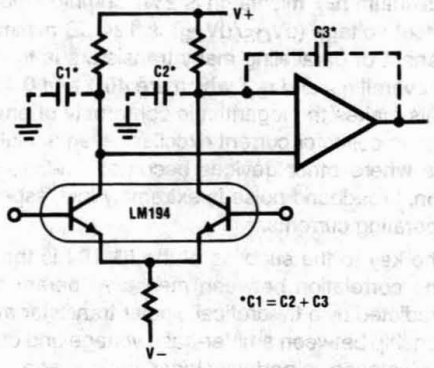

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FIGURE 2. High Frequency Power Supply Rejection

BANDWIDTH CONSIDERATIONS

Because of its large area, the LM194 has capacitance-limited bandwidth. The $h_{fe} \bullet f$ product is roughly 0.08 MHz per microampere of collector current, yielding an f_t of 80 MHz at $I_C = 1$ mA and 800 kHz at $I_C = 10\ \mu A$.

Collector-base capacitance on the LM194 is somewhat higher than ordinary small-signal transistors due to the large device geometry. C_{ob} is 17 pF at $V_{CE} = 5V$. For high gain stages with finite source impedance, the Millering effect of C_{ob} will usually be the limiting factor on voltage gain band-

width. At I_C = 100 μA and R_L = 50 kΩ, for instance, DC voltage gain will be $(R_L)(I_C)/(kT/q)$ = 200, but bandwidth will be limited to

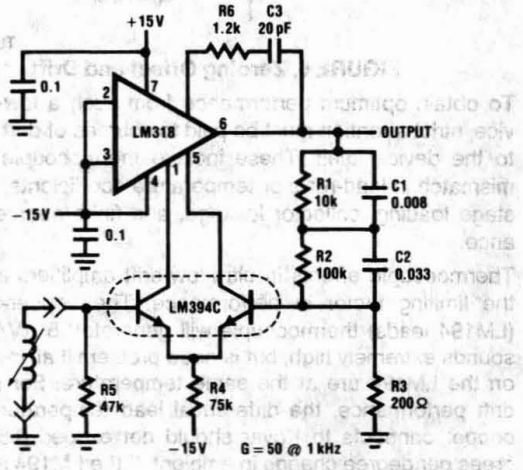
$$BW = \frac{kT/q}{(2\pi)(R_L)(I_C)(R_s)(C_{ob})} = 50\ kHz$$

for a source impedance (R_s) of 1 kΩ.

LOW NOISE APPLICATIONS

Figures 3 and *4* represent two different approaches to low noise designs. In *Figure 3*, the LM194 is used to replace the input stage of an LM118 high speed operational amplifier to create an ultra-low-distortion, low-noise RIAA-equalized phono preamplifier. The internal input stage of the LM118 is shut off by tying the unused inputs to the negative supply. This allows the LM194 to be used in place of the internal input stage, avoiding the loop stability problems created when extra stages are added. The stability problem is especially critical in an RIAA circuit where 100% feedback is used at high frequencies. Performance of this circuit exceeds the ability of most test equipment to measure it. As shown in the accompanying chart, *Figure 3*, harmonic distortion is below the measurable 0.002% level over most of the operating frequency and amplitude range. Noise referred to a 10 mV input signal is 90 dB down, measuring 0.55 μV_{RMS} and 70 pA_{RMS} in a 20 kHz bandwidth. More importantly, the noise figure is less than 2 dB when the amplifier is used with standard phono cartridges, which have an equivalent wideband (20 kHz) noise of 0.7 μV[1]. Further improvements in amplifier noise characteristics would be of little use because of the noise generated by the cartridge itself.

A special test was performed to check for "Transient Intermodulation Distortion"[2]. 10 kHz and 11 kHz were mixed 1:1 at the input to give an RMS output voltage of 2V (input = 200 mV). The resulting 1 kHz intermodulation product measured at the output was 80 μV. This calculates to 0.004% distortion, an incredibly low level considering that the 1 kHz has 14 dB (5:1) gain with respect to the 10 kHz signal in an RIAA circuit. Of special interest also is the use of all DC coupling. This eliminates the overload recovery problems associated with coupling and bypass capacitors. Worst case



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NOTE: Cartridge is assumed to have less than 5 kΩ DC resistance. Do not capacitor couple the cartridge. R1, R2, and R3 should be low noise metal film resistors.

FREQUENCY (Hz)	TOTAL HARMONIC DISTORTION				
20	<0.002	<0.002	<0.002	<0.002	<0.002
100	<0.002	<0.002	<0.002	<0.002	<0.002
1k	<0.002	<0.002	<0.002	<0.002	<0.002
10k	<0.002	<0.002	<0.002	0.0025	<0.003
20k	<0.002	<0.002	0.004	0.004	0.007
	0.03	0.1	0.3	1.0	5.0

OUTPUT AMPLITUDE (V) RMS

FIGURE 3. Ultra Low Noise RIAA Phono Preamplifier

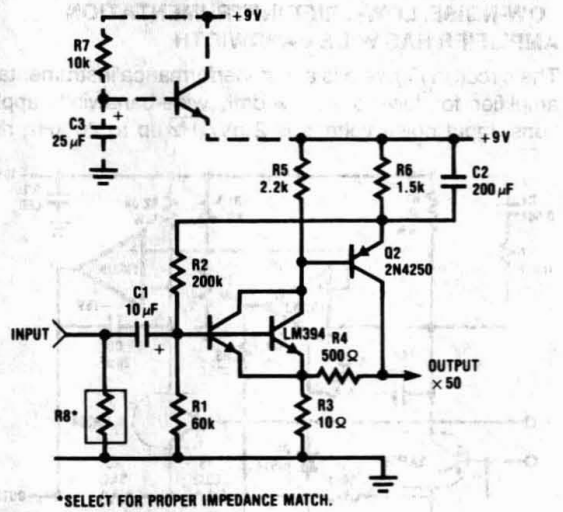

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FIGURE 4. Ultra Low Noise Preamplifier

DC output offset voltage is about 1V with a cartridge having 1 kΩ DC resistance.

The single-ended amplifier shown in *Figure 4* was designed for source impedances below 250Ω. At this level, the LM194 should be biased at 2.5 mA (or higher) collector current. Unfortunately, r_{bb}', even at 40Ω, is the limiting factor on noise at these current levels. To achieve better performance, the two halves of the LM194 are paralleled to reduce r_{bb}' to 20Ω. Total input voltage noise for this design is given by:

$$e_N = \sqrt{4kT(r_{bb}' + R_3) + e_n^2}$$
$$= \sqrt{0.504 + 0.096} = 0.775\ nV/\sqrt{Hz}$$

The current noise is 1.2 $pA/\sqrt{Hz}$, and when this flows through a 250Ω source resistance, it causes an additional 0.30 $nV/\sqrt{Hz}$. Since the Johnson noise of a 250Ω resistor is 2.0 $nV/\sqrt{Hz}$, the noise figure is:

$$NF = 20 \log \frac{\sqrt{(2\ nV)^2 + (0.3\ nV)^2 + (0.775\ nV)^2}}{2nV} = 0.74\ dB$$

Several unique features of this circuit should be pointed out. First, it has only one internal capacitor which functions as an AC bypass for both stages. Second, no input stage load resistor bypassing is used, yet the circuit achieves 56 dB supply rejection referred to input. The optional supply filter shown in dotted lines improves this by an additional 50 dB and is necessary only if supply noise exceeds 20 $nV/\sqrt{Hz}$. Finally, the problem of AC coupling the 10Ω feedback impedance is eliminated by using a DC biasing scheme which biases both stages simultaneously without relying on feedback from the output.

Harmonic distortion is very low for a "simple" two stage design. At 300 mV output, total harmonic distortion measured 0.016%. For normal signal levels of 50 mV and below, distortion was lost in the noise floor. Small-signal bandwidth is 3 MHz.

An ideal application for this amplifier is as a head pre-amp for moving-coil phono cartridges. These cartridges have very low output impedance (< 50Ω at low frequencies) and have a full-output signal below 1 mV. Obviously, the preamp used for such a low signal level must have superb noise properties. The amplifier shown has a total RMS input noise of 0.11 μV in a 20 kHz bandwidth, yielding a signal-to-noise ratio of 70 dB when used with a 40Ω source impedance at a 0.5 mV signal level.

LOW-NOISE, LOW-DRIFT INSTRUMENTATION AMPLIFIER HAS WIDE BANDWIDTH

The circuit in *Figure 5* is a high-performance instrumentation amplifier for low-noise, low-drift, wide-bandwidth applications. Input noise voltage is 2 nV/√Hz up to 20 kHz, rising

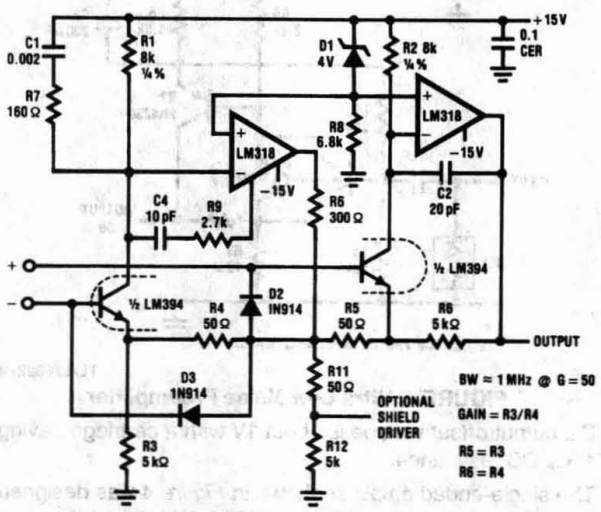

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FIGURE 5. Low Drift-Low Noise Instrumentation Amplifier

to 3.5 nV/√Hz at 100 kHz. Bandwidth at a gain of 50 is 1 MHz and gain can be varied over the range of 10−100 simply by changing the value of R_3 and R_6. Input offset voltage drift is determined by the LM194 and the tracking of the (R_1–R_2), (R_3–R_6), and (R_4–R_5) pairs. 20 ppm/°C mismatch on all pairs will generate 1.1 μV/°C referred to input, dominating the drift due to the LM194. Resistor pairs which track to 5 ppm/°C or better are recommended for very low drift applications. Input bias current is about 1 μA, rather high for general purpose use, but necessary in this case to achieve wide bandwidth and low noise. The tight matching of the LM194, however, reduces input offset current to 20 nA, and input offset current drift to 0.5 nA/°C. Input bias current drift is under 10 nA/°C. In terms of source impedance, total input referred voltage drift will be degraded 1 μV/°C for each 100Ω of unbalanced source resistance and 0.05 μV/°C for each 100Ω of balanced source resistance. DC common mode rejection of this amplifier is extremely good, depending mostly on the match of the ratio of R_3/R_4 to R_5/R_6. 0.1% matching gives better than 90 dB. Rejection will improve with tighter matching and is not limited by the LM194 until CMRR approaches 120 dB. High frequency CMRR is also very good, measuring 80 dB at 20 kHz and 60 dB at 100 kHz. Settling time for a 10V output step is 1.5 μs to 0.1%, and 5 μs to 0.01%. Distortion with 10 V_{p-p} output is virtually unmeasurable (< 0.002%) at low frequencies, rising to 0.1% at 50 kHz, and 1% at 200 kHz.

LOW DRIFT DESIGNS

Offset voltage drive in the LM194 quite closely follows the theoretical value derived by differentiating the logarithmic formula. In other words it is a function only of the original offset voltage. If V_{OS} is the original room temperature offset voltage, drift of offset as given by differentiation yields:

$$\frac{d(V_{OS})}{dT} = \frac{\left(d\,kT/q\,\ln e^{\frac{V_{OS}}{kT/q}}\right)}{dT} = \frac{V_{os}}{T}$$

At room temperature (T = 297°K), 1 mV of offset voltage will generate 1 mV/297°K = 3.37 μV/°C drift. The LM194 with a maximum offset voltage of 50 μV could be expected to have a maximum offset voltage drift of 0.17 μV/°C. Lab measurements indicate that it does not deviate from this theoretical drift by more than 0.1 μV/°C. This means the LM194 can be specified at 0.3 μV/°C drift without an individual drift test on each device. In addition, if initial offset voltage is zeroed out, maximum drift will be less than 0.1 μV/°C. The zeroing, of course, must be done in a way that theoretically zeroes drift. This is best done as shown in *Figure 6* with a small trimpot used to unbalance collector load resistors. (See National's Application Note AN-3.)

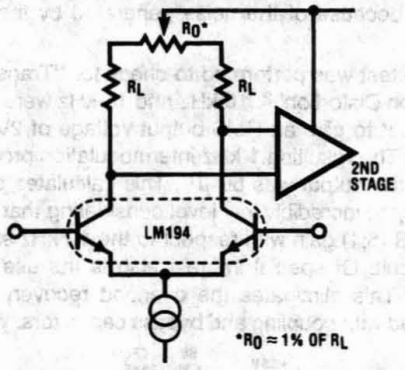

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FIGURE 6. Zeroing Offset and Drift

To obtain optimum performance from such a low-drift device, strict attention must be paid to sources of drift external to the device itself. These include thermocouple effects, mismatch in load-resistor temperature coefficients, second-stage loading, collector leakage, and finite source impedance.

Thermocouple effects in ultra-low-drift amplifiers are often the limiting factor in performance. The copper-to-Kovar (LM194 leads) thermocouple will generate 35 μV/°C. This sounds extremely high, but is not a problem if all input leads on the LM194 are at the same temperature. For optimum drift performance, the differential lead temperature where copper connects to Kovar should not exceed 0.5 millidegrees per degree change in ambient. If the LM194 is mounted on a printed circuit board, emitter and base leads should be soldered to identical size pads and the package orientation should place emitter and base leads on isothermal lines if any significant power is being dissipated on the board. The board should be kept in a still-air environment to minimize the effects of circulating air currents. "Still" air is particularly important when the LM194 leads are soldered di-

rectly to wires and when low (< 10 Hz) noise is critical. Individual wires in air can easily generate a differential end temperature of 10 millidegrees in an ordinary room ambient, even with the wires twisted together. This can cause up to 1 μV_{p-p} fluctuation in offset voltage. The 0.001 Hz to 10 Hz noise of the LM194 operating differentially at 100 μA is typically 40 nV_{p-p} (see *Figure 7*), so the thermally generated signal represents a 25:1 degradation of low frequency noise.

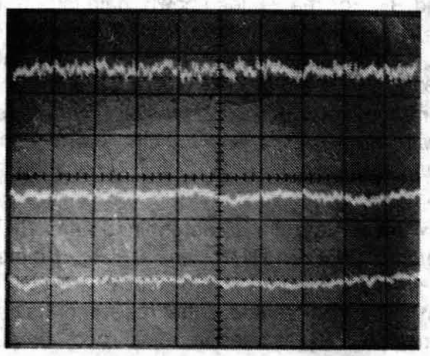

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FIGURE 7. Low Frequency Noise of Differential Pair. Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

If the load resistors used to bias the LM194 do not have identical temperature coefficients, they will contribute to offset voltage drift. A 1 ppm/°C mismatch in resistor drift will generate 0.026 μV/°C drift in the LM194. Resistors with 10 ppm/°C differential drift will seriously degrade the drift of an otherwise perfect circuit design. Resistors specified to track better than 2 ppm/°C are available from several manufacturers including Vishay, Julie, RCL, TRW, and Tel Labs.

Source impedance must be considered in a low-drift amplifier since voltage drift at the output can result from drift of the base currents of the LM194. Base current changes at about −0.8%/°C. This is equal to 2 nA/°C at a collector current of 100 μA and an h_{FE} of 400. If drift error caused by the changing base current is to be kept to less than 0.05 μV/°C, source unbalance cannot exceed 25Ω in this example. If a balanced condition exists, source impedance is still limited by the base current mismatch of the LM194. Worst case offset in the base current is 2%, and this offset can have a temperature drift of up to 2%/°C, yielding a change in offset current of up to

$$(2\%)(100\ \mu A)(2\%/°C)/h_{FE} = 0.1\ nA/°C$$

at a collector current of 100 μA. This limits balanced source impedances to 500Ω at collector currents of 100 μA if drift error is to be kept under 0.05 μV/°C. For higher source impedances, collector current must be reduced, or drift trimming must be used.

Collector-leakage effects on drift are generally very low for temperatures below 50°C. At higher temperatures, leakage can be a factor, especially at low collector currents. At 70°C, total collector leakage (to base and substrate) is typically 2 nA, increasing at 0.2 nA/°C. Assuming a 10% mismatch between collector leakages, input-referred drift will be 0.05 μV/°C at a collector current of 10 μA, and 0.005 μV/°C at 100 μA. At 125°C, input referred drift will be 1.5 μV/°C and 0.15 μV/°C respectively.

The amplifier used in conjunction with the LM194 may contribute significantly to drift if its own drift characteristics are poor. An LM194 operated with 2.5 V_{DC} across its load resistors has a voltage gain of approximately 100. If the second stage amplifier has a voltage drift of 20 μV/°C (normal for an amplifier with V_{OS} = 6 mV) the drift referred to the LM194 inputs will be 0.2 μV/°C, a significant degradation in drift. Amplifiers with low drift such as the LM108A or LM308A (5 μV/°C max) are recommended.

For the ultimate in low drift applications, the residual drift of the LM194 can be zeroed out. This is particularly easy because of the known relationship between a change in room-temperature offset and the resultant change in offset drift. The zeroing technique involves only one oven test to establish initial drift. The drift can then be reduced to below 0.03 μV/°C with a simple room-temperature adjustment. The procedure is as follows: (See *Figure 8.*)

1. Zero the offset voltage at room temperature (T_A).
2. Raise oven temperature to desired level (T_H) and measure offset voltage.
3. Bring circuit back to room temperature and adjust offset voltage to (V_{OS} at T_H) • (T_A)/(T_H − T_A). (T is in °K.)
4. Re-adjust offset voltage to zero with an external reference source by summing the two signals. (Do not re-adjust the offset of the LM194.)

This technique can be extended to include drift correction for source-generated drift as well since the basic correcting mechanism *is independent of the source of drift.*

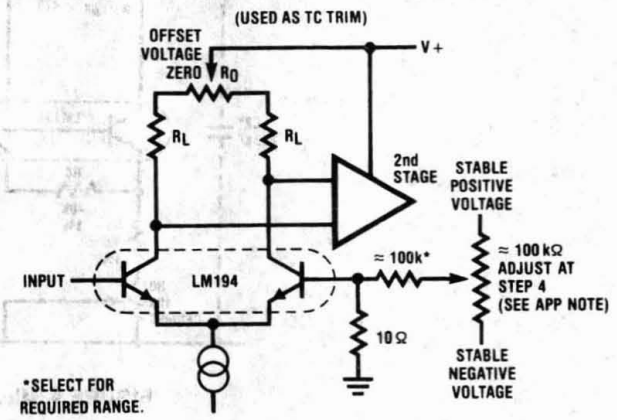

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FIGURE 8. Correcting for Residual or Source Generated Drift

VOLTAGE REFERENCE

Voltage references utilizing the bandgap voltage of silicon were first used 8 years ago, and have since gained wide acceptance in such circuits as the LM109, LM113, LM340, LM117, μA7800, AD580, and REF 01. The theory has been well publicized and is not reiterated here.

The circuit in *Figure 9* is a micropower version of a bandgap technique first used by Analog Devices. It operates off a single 2.5V to 6V supply and draws only 25 μA idling current. Two AA penlight cells will power the reference for over a year of continuous operation. Maximum output current is 0.5 mA, with an output resistance of 0.2Ω. Line regulation is ~0.01%/V and output noise is 20 μV_{RMS} over a 10 kHz bandwidth. Temperature drift is less than ±50 ppm/°C when the output is trimmed to 1.21V. Much lower drift can be obtained by adjusting the output of each reference to the

optimum value. A 1% shift in output voltage changes drift 33 ppm/°C. Temperature range is −25°C to +100°C.

The LM194 is the entire reference in this design, supplying both V_{BE} and ΔV_{BE} portions of the reference. One half LM114 delivers a constant bias current to the LM4250. The other half, in conjunction with the 2N4250 PNP, ensures startup of the circuit under worst cast (2.4k) load current. R_1–R_2 and R_4–R_5 should track to 50 ppm/°C. R_6 should have a TC of under 250 ppm/°C. The circuit is stable for capacitive loads up to 0.047 μF. C_2 is optional, for improved ripple rejection.

STRAIN GAUGE AMPLIFIER

The instrumentation amplifier shown in *Figure 10* is an example of an ultra-low-drift design specifically optimized for strain-gauge applications. A typical strain-gauge bridge has one end grounded and the other driven by a 3-to-10 volt precision voltage reference. The differential output signal of the bridge has a 1.5 to 5 volt common-mode level and a typical full-scale differential signal level of 5–50 mV. Source impedance is in the range of 100Ω to 500Ω, with an impedance imbalance of less than 2%. This amplifier has been specifically optimized for these types of signals. It has a +1V to +10V common mode range, a full scale input of 20 mV (1 mV to 100 mV is possible) and fully balanced inputs with a differential input impedance > 10 MΩ. Common mode input impedance is 100 MΩ. Common mode rejection ratio is 120 dB at 60 Hz, 114 dB at 1 kHz, and 94 dB at 10 kHz referred to input. Power supply rejection at DC is 114 dB on the V+ supply and 108 dB on the V− supply. Small signal bandwidth is > 50 kHz and slew rate is 0.1 V/μs. Gain error is determined by the accuracy of R_9, R_8, R_4, and R_3. For the values shown, gain is 500. R_3 can be varied to set gain as desired from 250 (800Ω) to 10,000 (20Ω). Gain non-linearity is < 0.05% for a 10V output and < 0.012% for a 5V output). R_7 is a +0.3%/°C positive-temperature-coefficient wirewound resistor for compensation of gain with temperature. Without this resistor, gain change with temperature is 0.007%/°C. If R_7 is omitted, replace R_9 with 12.4 kΩ.

Input offset voltage drift is determined primarily by resistor mismatches between R_1/R_2 and R_5/R_6. If either of these ratios drifts by 5 ppm/°C, an input offset voltage drift of 0.15 μV/°C will be created. Other resistor drifts contribute to gain error only. R_{12} is used to adjust room temperature offset voltage to zero.

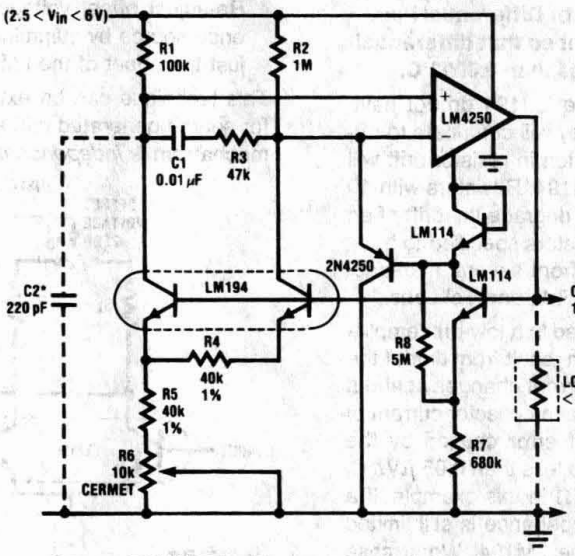

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FIGURE 9. Micropower Reference

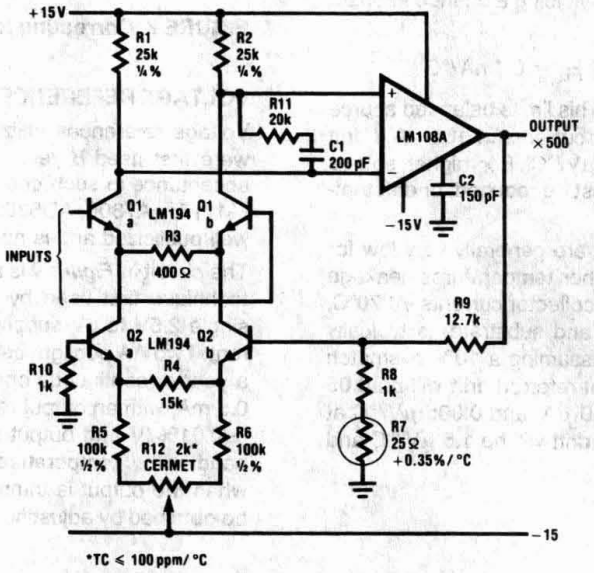

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FIGURE 10. Strain Gauge Instrumentation Amplifier

THERMOCOUPLE AMPLIFIER WITH COLD JUNCTION COMPENSATION

Thermocouple amplifiers need low offset voltage drift, good gain accuracy, low noise, and most importantly, cold-junction compensation. The amplifier in *Figure 11* does all that and more. It is specifically designed for ease of calibration so that repeated oven cycling is not required for calibration of gain and zero. Also, no mathematical calculations are required in the calibration procedure.

The circuit is basically a non-inverting amplifier with the gain set to give 10 mV/(°F or °C) at the output. This output sensitivity is arbitrary and can be set higher or lower. Cold-junction compensation is achieved by deliberately unbalancing the collector currents of the LM194 so that the resulting input offset voltage drift is just equal to the thermocouple output (α) at room temperature. By combining the formulas for offset voltage versus current imbalance and offset voltage drift, the required ratio of collector currents is obtained.

$$\frac{d(V_{os})}{dT} = \frac{V_{OS}}{T} = \frac{k}{q} \ln \frac{I_{C_1}}{I_{C_2}}$$

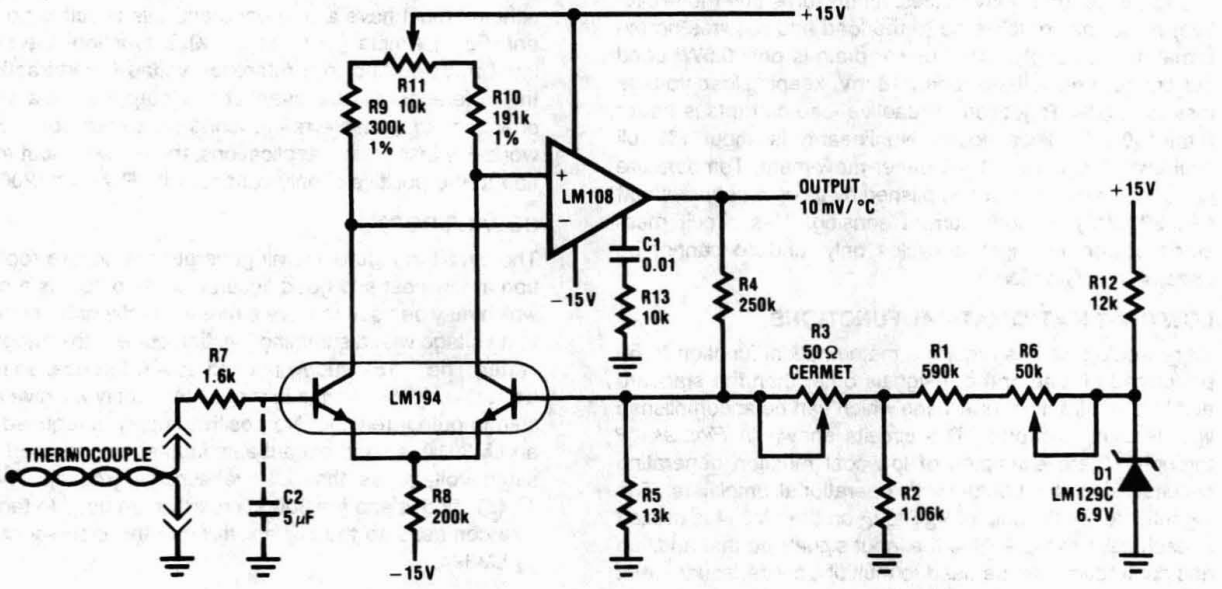
$$\ln \frac{I_{C_1}}{I_{C_2}} = \frac{q \bullet V_{OS}}{k \bullet T} = \frac{q \bullet \alpha}{k}$$

$$\frac{I_{C_1}}{I_{C_2}} = e^{\frac{q \bullet \alpha}{k}}$$

(α = thermocouple output in V/°C)

This technique does require that the LM194 be at the same temperature as the thermocouple cold junction. The thermocouple leads should be terminated close to the LM194.

The deliberate offset voltage created across the LM194 inputs must be subtracted out with an external reference which is also used to zero shift the output to read directly in °C or °F. This is done in a special way so that at some arbitrarily selected temperature (T_1), the gain adjustment has no effect on zero, vastly simplifying the calibration procedure. Design equations for the circuit are shown with the schematic in descending order of their proper use. Also shown is the calibration procedure, which requires only one oven trip for both gain and zero. Use of the nearest pocket calculator should yield all resistor values in a few minutes. The values shown on the schematic are for a 10 mV/°C output with a Chromel-Alumel thermocouple delivering 40 μV/°C, with T_1 selected at room temperature (297°K). All resistors except R_8 and R_{12} should be 1% metal film types



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1. Select R9 = 300 kΩ
2. Set R10 equal to R9 • $e^{-\alpha(1.16 \times 10^4)}$
3. R8 = 200k
4. Select R4 in the range 50 kΩ to 250 kΩ
5. $R5 = \frac{(R4)(T_1)(\alpha)}{S(T_1 - T_0) - \alpha(T_1)}$
6. $R2 = \frac{\alpha(R4)(R5)(1 - E^*/100)}{(S - \alpha)\left[R5 - \frac{\alpha(R4)}{S - \alpha}\right]}$
7. $R1 = \frac{[(R2) \bullet V_Z - \alpha(T_1)]}{\alpha(T_1)}(0.95)$
8. $R3 = \frac{(E)(R2)}{50}$
9. R7 = (R9/R10)(R2)
10. R6 = R1/10

E = Gain error allowed for (≈2.5%)

T_1 = Temperature in °K at which it is desired to have the gain control not interact with the zero control

T_0 = Temperature in °K at which the desired temperature scale (°C or °F) is equal to zero

S = Required output scale factor. Use V/°C even though actual output may be in °F

V_Z = Zener reference voltage

α = Thermocouple output in V/°C

Values shown on schematic are for 10 mV/°C.

See below for 10 mV/°F values using a Chromel-Alumel thermocouple with room temperature for T_1.

R1 = 367k, R2 = 629Ω, R3 = Ω, R4 = 250k, R5 = 4.08k, R6 = 50k, R7 = 1k, R10 = 191k

CALIBRATION:*

a. Set oven to T_1 and adjust R6 to give proper output (zero adjust).

b. Raise (or lower) oven to T_2 and adjust R3 to give proper output at T_2 (gain adjust).

c. Return to room temperature and short thermocouple and D1 to ground. Adjust R11 to give proper output (room ambient) in °K or °R.

For 10 mV/°C, this is 2.98V @ T_A = 25°C.

For 10 mV/°F, this is 5.37V @ T_A = 77°F.

d. Remove shorts and re-adjust R6 if necessary to zero output.

Note: Steps C and D can be eliminated if exact cold junction compensation is not required. R11 is simply shorted out. Compensation will be within ±5% without adjustment (≤0.05°C/°C).

*Thermocouple only in oven.

FIGURE 11. Thermocouple Amplifier with Cold-Junction Compensation

for low thermocouple effects (resistors *do* generate thermocouple voltages if their ends are at different temperatures) and should have low temperature coefficients. R_9 and R_{10} should track to 10 ppm/°C. R_3, R_6, and R_{11} should not have a TC higher than 250 ppm/°C. R_1, R_2, and R_4 should track to 20 ppm/°C. C_2 can be added to reduce spikes and noise from long thermocouple lines.

Input impedance for this circuit is > 100 MΩ, so high thermocouple impedance will not affect scale factor. "Zero shift" due to input bias current is approximately 1°C for each 400Ω of thermocouple lead resistance with a 40 μV/°C thermocouple.

No provision is made for correction of thermocouple non-linearity. This could be accomplished with a slight nonlinearity introduced into R_4 with additional resistors and diodes. Another possibility is to digitize the output and correct the nonlinearity digitally with a ROM programmed for a specific thermocouple type.

POWER METER

The power meter in *Figure 12* is a good example of minimum-parts-count design. It uses only one transistor pair to provide the complete (X) • (Y) function. The circuit is intended for 117 V_{AC} ± 50 V_{AC} operation, but can be easily modified for higher or lower voltages. It measures true (non-reactive) power being delivered to the load and requires no external power supply. Idling power drain is only 0.5W. Load current sensing voltage is only 10 mV, keeping load voltage loss to 0.01%. Rejection of reactive load currents is better than 100:1 for linear loads. Nonlinearity is about 1% full scale when using a 50 μA meter movement. Temperature correction for gain is accomplished by using a copper shunt (+0.32%/°C) for load-current sensing. This circuit measures power on negative cycles only, and so cannot be used on rectifying loads.

LOW COST MATHEMATICAL FUNCTIONS

Many analog circuits require a mathematical function to be performed on one or more signals other than the standard addition, subtraction, or scaling which can be accomplished with resistor networks. The circuits shown in *Figures 13* through *15* are examples of low-cost function generating circuits using the LM394 with operational amplifiers. The logarithmic relationship of V_{BE} to I_C on the LM394 is utilized in each case to log-antilog the input signals so that addition and subtraction can be used to multiply, divide, square, etc. When transistors are used in this manner, matching is very critical. A 1 mV offset in V_{BE} appears as a *4% of signal* error even in the best case where operation is restricted to one quadrant. Parasitic emitter or base resistance (r_{ee}', r_{bb}') can also seriously degrade accuracy. At I_C = 100 μA and h_{FE} = 100, each Ω of emitter resistance and each 100Ω of base resistance will cause 0.4% signal error. Most matched transistor pairs available today have significant parasitic resistances which severely limit their use in high-accuracy circuits. The LM394, with offset guaranteed below 0.15 mV and a typical emitter-referred total parasitic resistance of 0.4Ω gives an order of magnitude improvement in accuracy to nonlinear designs at all current levels.

MULTIPLIER/DIVIDER

The circuit in *Figure 13* will give an output proportional to the product of the (X) and (Y) inputs divided by the Z input. All inputs must be positive, limiting operation to one quadrant, but this restriction removes the large error terms found in 2- and 4-quadrant designs. In a large percentage of cases, analog signals requiring multiplication are of one polarity only and can be inverted if negative. A nice feature of this design is that all gain errors can be trimmed to zero at one point. R_5 is paralleled with 2.4 MΩ to drop its nominal value 2%. R_8 then gives a ±2% gain trim to account for errors in R_1, R_2, R_5, R_7, and any offset in Q_1 or Q_2. For very low level inputs, offset voltage in the LM308s may create large percentage errors referred to input. A simple scheme for offsetting any of the LM308s to zero is shown in dotted lined; the + input of the appropriate LM308 is simply tied to R_x instead of ground for zeroing. The summing mode of operation on all inputs allows easy scaling on any or all inputs. Simply set the input resistor equal to $(V_{IN(max)})/(200\ \mu A)$. V_{OUT} is equal to:

$$V_{OUT} = \frac{\left(\frac{X}{R_1}\right)\left(\frac{Y}{R_2}\right)(R_5)}{\frac{Z}{R_7}}$$

Input voltages above the supply voltage are allowed because of the summing mode of operation. Several inputs may be summed at "X", "Y," or "Z."

Proper scaling will improve accuracy by preventing large current imbalances in Q_1 and Q_2, and by creating the largest possible output swing. Keep in mind that any multiplier scheme must have a reference and this circuit is no different. For a simple (X) • (Y) or (X)/Z function, the unused input must be tied to a reference voltage. Perturbations in this reference will be seen at the output as scale factor changes, so a stable reference is necessary for precision work. For less critical applications, the unused input may be tied to the positive supply voltage, with R = $V^+/200\ \mu A$.

SQUARE ROOT

The circuit in *Figure 14* will generate the square root function at low cost and good accuracy. The output is a current which may be used to drive a meter directly or be converted to a voltage with a summing junction current-to-voltage converter. The −15V supply is used as a reference, so it must be stable. A 1% change in the −15V supply will give a ½% shift in output reading. No positive supply is required when an LM301A is used because its inputs may be used at the same voltage as the positive supply (ground). The two 1N457 diodes and the 300 kΩ resistor are used to temperature compensate the current through the diode-connected ½ LM394.

SQUARING FUNCTION

The circuit in *Figure 15* will square the input signal and deliver the result as an output current. Full scale input is 10V, but this may be changed simply by changing the value of the 100 kΩ input resistor. As in the square root circuit, the −15V supply is used as the reference. In this case, however, a 1% shift in supply voltage gives a 1% shift in output signal. The 150 kΩ resistor across the base-emitter of ½ LM394 provides slight temperature compensation of the reference current from the −15V supply. For improved accuracy at low input signal levels, the offset voltage of the LM301A should be zeroed out, and a 100 kΩ resistor should be inserted in the positive input to provide optimum DC balance.

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1. See National's *Audio Handbook*.

2. *The Audio Amateur*, volume VIII, number 1, Feb. 1977.

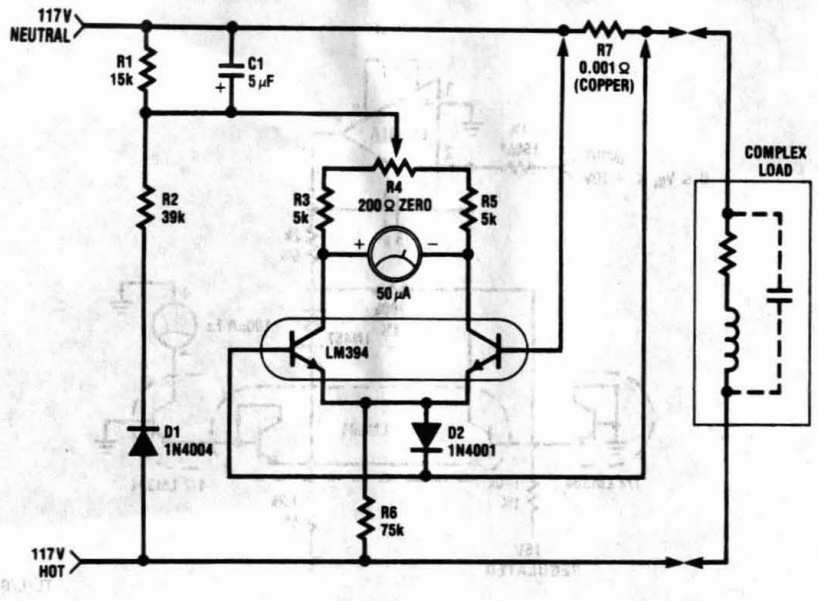

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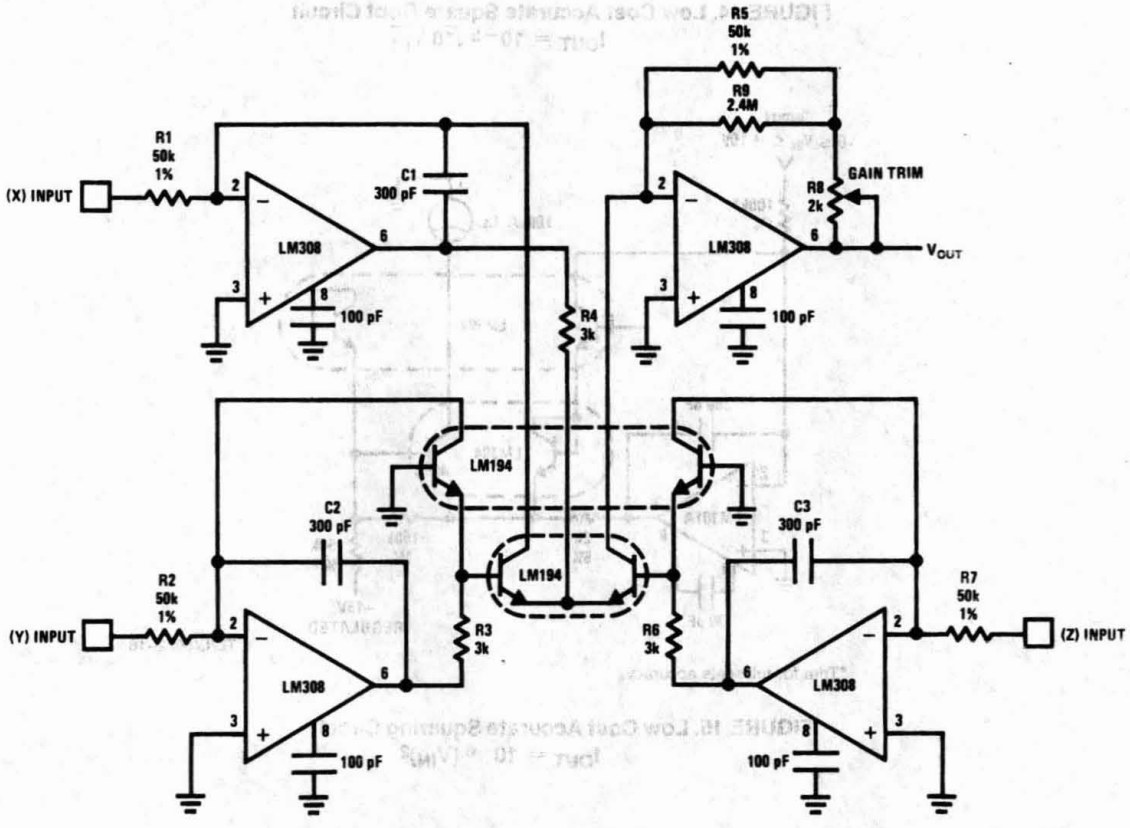
FIGURE 12. Power Meter (1 kW f.s.)



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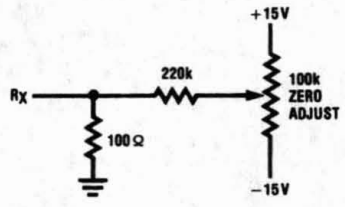

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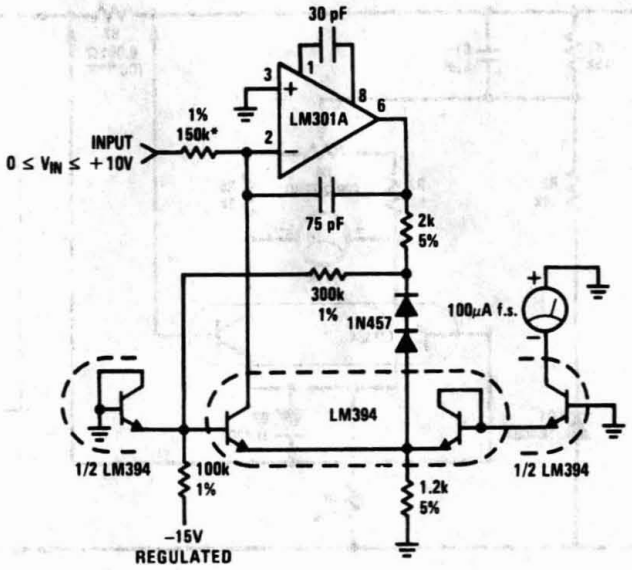
FIGURE 13. High Accuracy One Quadrant Multiplier/Divider



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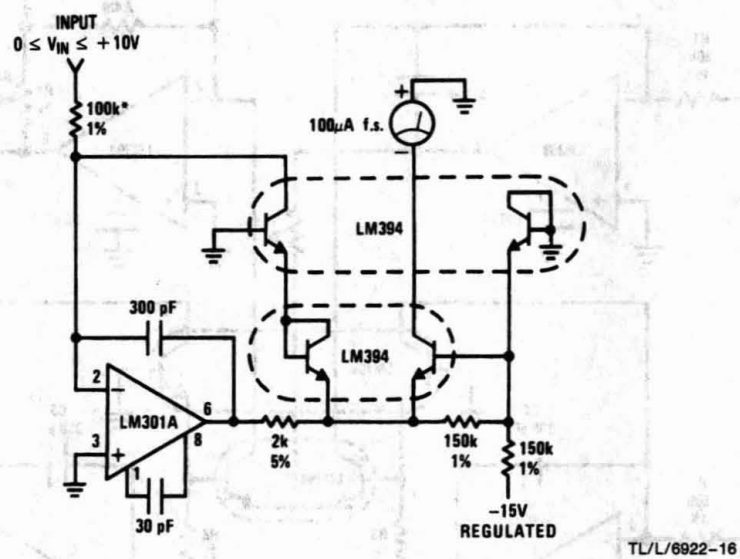
*Trim for full scale accuracy.

FIGURE 14. Low Cost Accurate Square Root Circuit
$I_{OUT} = 10^{-5}\sqrt{10\,V_{IN}}$



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*Trim for full scale accuracy.

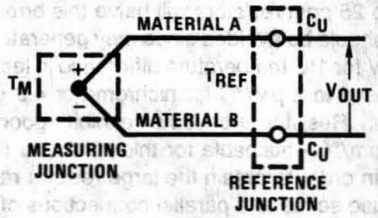
FIGURE 15. Low Cost Accurate Squaring Circuit
$I_{OUT} = 10^{-6}\,(V_{IN})^2$

IC Temperature Sensor Provides Thermocouple Cold-Junction Compensation

National Semiconductor
Application Note 225
Michael X. Maida

INTRODUCTION

Due to their low cost and ease of use, thermocouples are still a popular means for making temperature measurements up to several thousand degrees centigrade. A thermocouple is made by joining wires of two different metals as shown in *Figure 1*. The output voltage is approximately proportional to the temperature difference between the measuring junction and the reference junction. This constant of proportionality is known as the Seebeck coefficient and ranges from 5 μV/°C to 50 μV/°C for commonly used thermocouples.



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$$V_{OUT} \cong \infty(T_M - T_{REF})$$

FIGURE 1. Thermocouple

Because a thermocouple is sensitive to a temperature *difference*, the temperature at the reference junction must be known in order to make a temperature measurement. One way to do this is to keep the reference junction in an ice bath. This has the advantage of zero output voltage at 0°C, making thermocouple tables usable. A more convenient approach, known as cold-junction compensation, is to add a compensating voltage to the thermocouple output so that the reference junction appears to be at 0°C independent of the actual temperature. If this voltage is made proportional to temperature with the same constant of proportionality as the thermocouple, changes in ambient temperature will have no effect on output voltage.

An IC temperature sensor such as the LM135/LM235/LM335, which has a very linear voltage vs. temperature characteristic, is a natural choice to use in this compensation circuit. The LM135 operates by sensing the difference of base-emitter voltage of two transistors running at different current levels and acts like a zener diode with a breakdown voltage proportional to absolute temperature at 10 mV/°K. Furthermore, because the LM135 extrapolates to zero output at 0°K, the temperature coefficient of the compensation circuit can be adjusted at room temperature without requiring any temperature cycling.

SOURCES OF ERROR

There will be several sources of error involved when measuring temperature with thermocouples. The most basic of these is the tolerance of the thermocouple itself, due to varying composition of the wire material. Note that this tolerance states how much the voltage vs. temperature characteristic differs from that of an ideal thermocouple and has nothing to do with nonlinearity. Tolerance is typically ±¾% of reading for J, K, and T types or ±½% for S and R types, so that a measurement of 1000°C may be off by as much as 7.5°C. Special wire is available with half this error guaranteed.

Additional error can be introduced by the compensation circuitry. For perfect compensation, the compensation circuit must match the output of an ice-point-referenced thermocouple at ambient. It is difficult to match the thermocouple's nonlinear voltage vs. temperature characteristic with a linear absolute temperature sensor, so a "best fit" linear approximation must be made. In *Figure 2* this nonlinearity is plotted as a function of temperature for several thermocouple types. The K type is the most linear, while the S type is one of the least linear. When using an absolute temperature sensor for cold-junction compensation, compensation error is a function of both thermocouple nonlinearity and also the variation in ambient temperature, since the straight-line approximation to the thermocouple characteristic is more valid for small deviations.

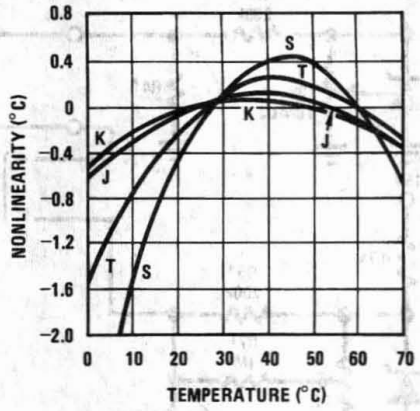

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FIGURE 2. Thermocouple Nonlinearity

Of course, increased error results if, due to component inaccuracies, the compensation circuit does not produce the ideal output. The LM335 is very linear with respect to absolute temperature and introduces little error. However, the complete circuit must contain resistors and a voltage reference in order to obtain the proper offset and scaling. Initial tolerances can be trimmed out, but the temperature coefficient of these external components is usually the limiting factor (unless this drift is measured and trimmed out).

CIRCUIT DESCRIPTION

A single-supply circuit is shown in *Figure 3*. R3 and R4 divide down the 10 mV/°K output of the LM335 to match the Seebeck coefficient of the thermocouple. The LM329B and its associated voltage divider provide a voltage to buck out the 0°C output of the LM335. To calibrate, adjust R1 so that V1 = $\propto$ T, where $\propto$ is the Seebeck coefficient* and T is the ambient temperature in degrees *Kelvin*. Then, adjust R2 so that V1 − V2 is equal to the thermocouple output voltage at the known ambient temperature.

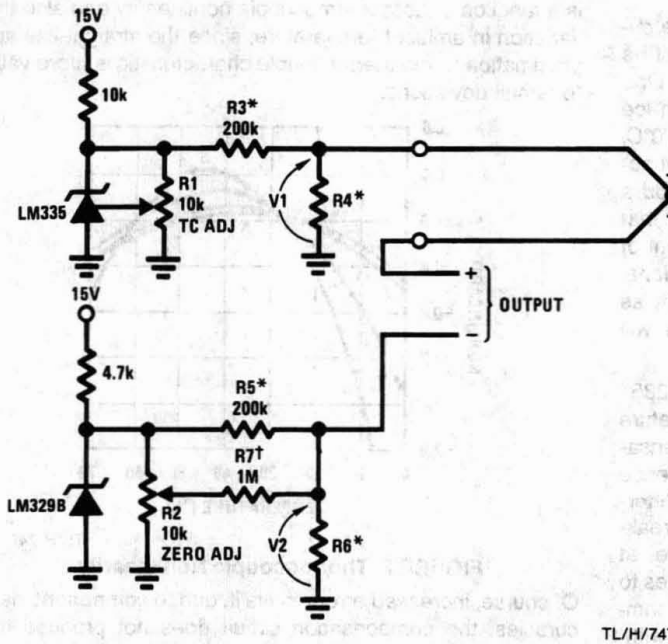
To achieve maximum performance from this circuit the resistors must be carefully chosen. R3 through R6 should be precision wirewounds, Vishay bulk metal or precision metal film types with a 1% tolerance and a temperature coefficient of ±5 ppm/°C or better. In addition to having a low TCR, these resistors exhibit low thermal emf when the leads are at different temperatures, ranging from 3 μV/°C for the TRW MAR to only 0.3 μV/°C for the Vishay types. This is especially important when using S or R type thermocouples that output only 6 μV/°C. R7 should have a temperature coefficient of ±25 ppm/°C or better and a 1% tolerance. Note that the potentiometers are placed where their absolute resistance is not important so that their TCR is not critical. However, the trim pots should be of a stable cermet type. While multi-turn pots are usually considered to have the best resolution, many modern single-turn pots are just as easy to set to within ±0.1% of the desired value as the multi-turn pots.

Also single-turn pots usually have superior stability of setting, versus shock or vibration. Thus, good single-turn cermet pots (such as Allen Bradley type E, Weston series 840, or CTS series 360) should be considered as good candidates for high-resolution trim applications, competing with the more obvious (but slightly more expensive) multi-turn trim pots such as Allen Bradley type RT or MT, Weston type 850, or similar.

With a room temperature adjustment, drift error will be only ±½°C at 70°C and ±¼°C at 0°C. Thermocouple nonlinearity results in additional compensation error. The chromel/alumel (type K) thermocouple is the most linear. With this type, a compensation accuracy of ±¾°C can be obtained over a 0°C–70°C range. Performance with an iron-constantan thermocouple is almost as good. To keep the error small for the less linear S and T type thermocouples, the ambient temperature must be kept within a more limited range, such as 15°C to 50°C. Of course, more accurate compensation over a narrower temperature range can be obtained with any thermocouple type by the proper adjustment of voltage TC and offset.

Standard metal-film resistors cost substantially less than precision types and may be substituted with a reduction in accuracy or temperature range. Using 50 ppm/°C resistors, the circuit can achieve ½°C error over a 10°C range. Switching to 25 ppm resistors will halve this error. Tin oxide resistors should be avoided since they generate a thermal emf of 20 μV for 1°C temperature difference in lead temperature as opposed to 2 μV/°C for nichrome or 4.3 μV/°C for cermet types. Resistor networks exhibit good tracking, with 50 ppm/°C obtainable for thick film and 5 ppm/°C for thin film. In order to obtain the large resistor ratios needed, one can use series and parallel connections of resistors on one or more substrates.

*See Appendix A for calculation of Seebeck coefficient.



Thermocouple Type	Seebeck Coefficient (μV/°C)	R4 (Ω)	R6 (Ω)
J	52.3	1050	385
T	42.8	856	315
K	40.8	816	300
S	6.4	128	46.3

*R3 thru R6 are 1%, 5 ppm/°C. (10 ppm/°C tracking.)

†R7 is 1%, 25 ppm/°C.

$$\text{choose R4} = \frac{\alpha}{10\ \text{mV/°C}} \bullet \text{R3}$$

$$\text{choose R6} = \frac{-T_o \bullet \alpha}{V_Z} \bullet (0.9\text{R5})$$

$$\text{choose R7} = 5 \bullet \text{R5}$$

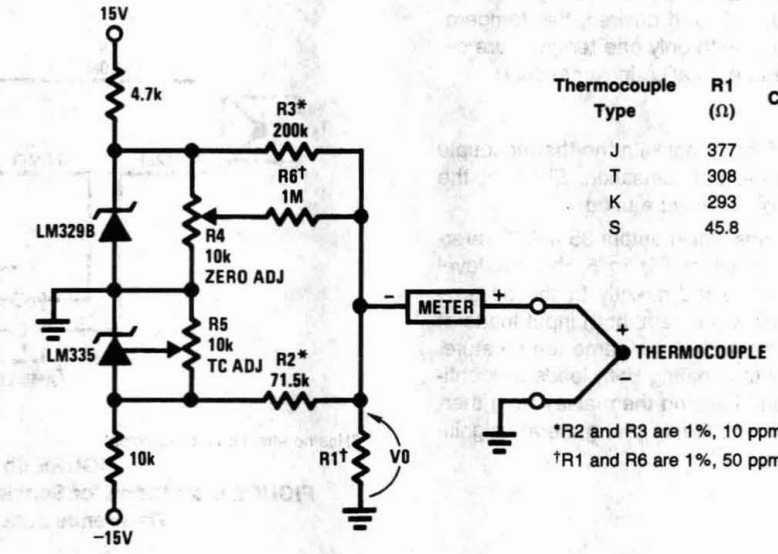
where T_o is absolute zero (−273.16°C)

V_Z is the reference voltage (6.95V for LM329B)

FIGURE 3. Thermocouple Cold-Junction Compensation Using Single Power Supply

A circuit for use with grounded thermocouples is shown in *Figure 4*. If dual supplies are available, this circuit is preferable to that of *Figure 3* since it achieves similar performance with fewer low TC resistors. To trim, short out the LM329B and adjust R5 so that $V_O = \alpha T$, where α is the Seebeck coefficient of the thermocouple and T is the absolute temperature. Remove the short and adjust R4 so that V_O equals the thermocouple output voltage at ambient. A good grounding system is essential here, for any ground differential will appear in series with the thermocouple output.

An electronic thermometer with a 10 mV/°C output from 0°C to 1300°C is seen in *Figure 5*. The trimming procedure is as follows: first short out the LM329B, the LM335 and the thermocouple. Measure the output voltage (equal to the input offset voltage times the voltage gain). Then apply a 50 mV input voltage and adjust the GAIN ADJUST pot until the output voltage is 12.25V above the previously measured value. Next, short out the thermocouple again and remove the short across the LM335. Adjust the TC ADJUST pot so that the output voltage equals 10 mV/°K times the absolute temperature. Finally, remove the short across the LM329B and adjust the ZERO ADJUST pot so that the output voltage equals 10 mV/°C times the ambient temperature in °C.



Thermocouple Type	R1 (Ω)	Seebeck Coefficient (μV/°C)
J	377	52.3
T	308	42.8
K	293	40.8
S	45.8	6.4

*R2 and R3 are 1%, 10 ppm/°C. (20 ppm/°C tracking.)
†R1 and R6 are 1%, 50 ppm/°C.

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FIGURE 4. Cold-Junction Compensation for Grounded Thermocouple

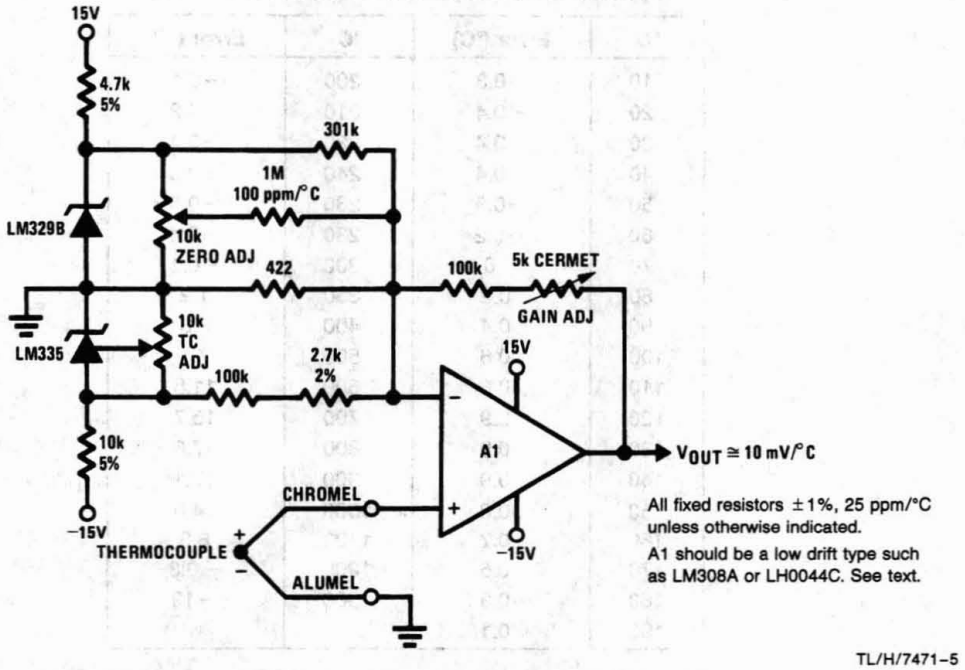

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FIGURE 5. Centigrade Thermometer with Cold-Junction Compensation

The error over a 0°C to 1300°C range due to thermocouple nonlinearity is only 2.5% maximum. Table I shows the error due to thermocouple nonlinearity as a function of temperature. This error is under 1°C for 0°C to 300°C but is as high as 17°C over the entire range. This may be corrected with a nonlinear shaping network. If the output is digitized, correction factors can be stored in a ROM and added in via hardware or software.

The major cause of temperature drift will be the input offset voltage drift of the op amp. The LM308A has a specified maximum offset voltage drift of 5 μV/°C which will result in a 1°C error for every 8°C change in ambient. Substitution of an LH0044C with its 1 μV/°C maximum offset voltage drift will reduce this error to 1°C per 40°C. If desired, this temperature drift can be trimmed out with only one temperature cycle by following the procedure detailed in Appendix B.

CONSTRUCTION HINTS

The LM335 must be held isothermal with the thermocouple reference junction for proper compensation. Either of the techniques of *Figures 6a* or *6b* may be used.

Hermetic ICs use Kovar leads which output 35 μV/°C referenced to copper. In the circuit of *Figure 5*, the low level thermocouple output is connected directly to the op amp input. To avoid this causing a problem, both input leads of the op amp must be maintained at the same temperature. This is easily achieved by terminating both leads to identically sized copper pads and keeping them away from thermal gradients caused by components that generate significant heat.

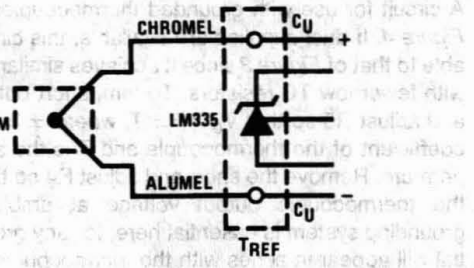

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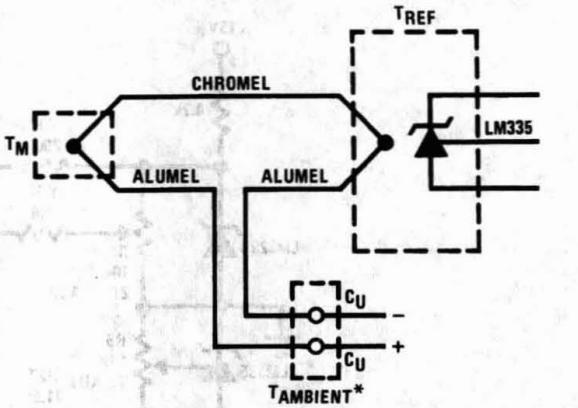
FIGURE 6a



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*Has no effect on measurement.

FIGURE 6b

FIGURE 6. Methods for Sensing Temperature of Reference Junction

TABLE I. Nonlinearity Error of Thermometer Using Type K Thermocouple (Scale Factor 25.47°C/μV)

°C	Error (°C)	°C	Error (°C)
10	−0.3	200	−0.1
20	−0.4	210	−0.2
30	−0.4	220	−0.4
40	−0.4	240	−0.6
50	−0.3	260	−0.5
60	−0.2	280	−0.4
70	0	300	−0.1
80	0.2	350	1.2
90	0.4	400	2.8
100	0.6	500	7.1
110	0.8	600	11.8
120	0.9	700	15.7
130	0.9	800	17.6
140	0.9	900	17.1
150	0.8	1000	14.0
160	0.7	1100	8.3
170	0.5	1200	−0.3
180	0.3	1300	−13
190	0.1		

Before trimming, all components should be stabilized. A 24-hour bake at 85°C is usually sufficient. Care should be taken when trimming to maintain the temperature of the LM335 constant, as body heat nearby can introduce significant errors. One should either keep the circuit in moving air or house it in a box, leaving holes for the trimpots.

CONCLUSION

Two circuits using the LM335 for thermocouple cold-junction compensation have been described. With a single room temperature calibration, these circuits are accurate to ±¾°C over a 0°C to 70°C temperature range using J or K type thermocouples. In addition, a thermocouple amplifier using an LM335 for cold-junction compensation has been described for which worst case error can be as low as 1°C per 40°C change in ambient.

APPENDIX A
DETERMINATION OF SEEBECK COEFFICIENT

Because of the nonlinear relation of output voltage vs. temperature for a thermocouple, there is no unique value of its Seebeck coefficient $\propto$. Instead, one must approximate the thermocouple function with a straight line and determine $\propto$ from the line's slope for the temperature range of interest.

On a graph, the error of the line approximation is easily visible as the vertical distance between the line and the nonlinear function. Thermocouple nonlinearity is not so gross, so that a numerical error calculation is better than the graphical approach.

Most thermocouple functions have positive curvature, so that a linear approximation with minimum mean-square error will intersect the function at two points. As a first cut, one can pick these points at the ⅓ and ⅔ points across the ambient temperature range. Then calculate the difference between the linear approximation and the thermocouple.† This error will usually then be a maximum at the midpoint and endpoints of the temperature range. If the error becomes too large at either temperature extreme, one can modify the slope or the intercept of the line. Once the linear approximation is found that minimizes error over the temperature range, use its slope as the Seebeck coefficient value when designing a cold-junction compensator.

An example of this procedure for a type S thermocouple is shown in Table II. Note that picking the two intercepts (zero error points) close together results in less error over a narrower temperature range.

†A collection of thermocouple tables useful for this purpose is found in the Omega Temperature Measurement Handbook published by Omega Engineering, Stamford, Connecticut.

TABLE II. Linear Approximations to Type S Thermocouple

Centigrade Temperature	Type S Thermocouple Output (μV)	Approximation #1 Zero Error at 25°C and 60°C			Approximation #2 Zero Error at 30°C and 50°C		
		Linear Approx.	Error		Linear Approx.	Error	
			μV	°C		μV	°C
0°	0	−17	−17	−2.7°	−16	−16	−2.8°
5°	27	15	−12	−1.9°	16	−11	−1.7°
10°	55	46	−9	−1.4°	47	−8	−1.3°
15°	84	78	−6	−0.9°	78	−6	−0.9°
20°	113	110	−3	−0.5°	110	−3	−0.5°
25°	142	142	0	0	142	−1	−0.2°
30°	173	174	1	0.2°	173	0	0
35°	203	206	3	0.5°	204	1	0.2°
40°	235	238	3	0.5°	236	1	0.2°
45°	266	270	4	0.6°	268	2	0.3°
50°	299	301	2	0.3°	299	0	0
55°	331	333	2	0.3°	330	−1	−0.2°
60°	365	365	0	0	362	−3	−0.5°
65°	398	397	−1	−0.2°	394	−4	−0.6°
70°	432	429	−3	−0.5°	425	−7	−1.1°
		$\propto$ = 6.4 μV/°C			$\propto$ = 6.3 μV/°C		
		0.6°C error for 20°C < T < 70°C			0.3°C error for 25°C < T < 50°C		

Note: Error is the difference between linear approximation and actual thermocouple output in μV. To convert error to °C, divide by Seebeck coefficient.

APPENDIX B
TECHNIQUE FOR TRIMMING OUT OFFSET DRIFT

Short out the thermocouple input and measure the circuit output voltage at 25°C and at 70°C. Calculate the output voltage temperature coefficient, β as shown.

$$\beta = \frac{V_{OUT\,(70°C)} - V_{OUT(25°C)}}{45°K} \text{ in mV/°K}$$

Next, short out the LM329B and adjust the TC ADJ pot so that $V_{OUT} = (20\ mV/°K - \beta) \times 298°K$ at 25°C. Now remove the short across the LM329B and adjust the ZERO ADJUST pot so that $V_{OUT} = 246$ mV at 25°C (246 times the 25°C output of an ice-point-referenced thermocouple).

This procedure compensates for all sources of drift, including resistor TC, reference drift (±20 ppm/°C maximum for the LM329B) and op amp offset drift. Performance will be limited only by TC nonlinearities and measurement accuracy.

REFERENCES

R. C. Dobkin, "Low Drift Amplifiers," National Semiconductor LB-22, June 1973.

Carl T. Nelson, "Super Matched Bipolar Transistor Pair Sets New Standards for Drift and Noise," National Semiconductor AN-222, February 1979.

Applications of Wide-Band Buffer Amplifiers

National Semiconductor
Application Note 227

INTRODUCTION

The LH0002, LH0033 and LH0063 are wide-band, high current, unity gain buffer amplifiers. They are intended for use alone or in closed-loop combination with op amps to drive co-axial cables and capacitive or other high-current loads. Features and characteristics of these buffers are summarized in Table I. All are active trimmed for low unadjusted output offset voltage and uniform performance. Good thermal coupling between dice is achieved by hybrid thick-film construction on ceramic substrates.

Part I analyzes the AC and DC equivalent circuits.

Part II is a comprehensive guide to applications techniques and shows how to get optimum performance under a variety of circumstances.

Finally, Part III illustrates these techniques in some specific applications including drivers, sample-and-hold amplifiers and active filters.

I. CIRCUIT DESCRIPTIONS

General

The three buffer amplifiers share a similar class AB emitter-follower output stage as shown in *Figure 1*. The symmetrical class AB amplifier output provides current sourcing or sinking and relatively constant low impedance to the load during positive and negative output swing. The input stage of the LH0002 consists of a complementary bipolar emitter-follower. The LH0033 and LH0063 employ junction FETs configured as source-followers, thereby achieving several orders of magnitude improvement in DC input resistance over the LH0002. In each case, the output stage collectors are uncommitted to allow the use of current limiting resistors in series with either or both output collectors.

LH0002 Low Frequency Operation

The LH0002 circuit shown in *Figure 2* is a compound emitter-follower with small-signal current gain of approximately 40,000 (product of first and second stage betas).

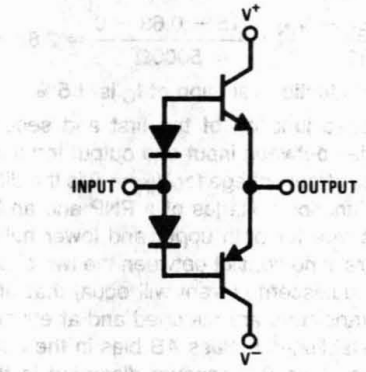

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FIGURE 1. LH0002 Simplified Output Stage

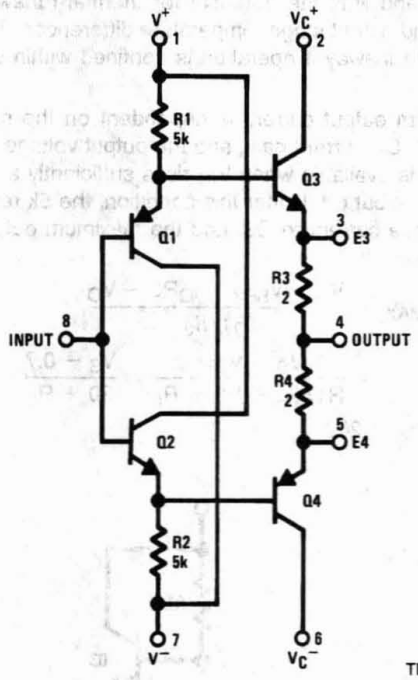

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FIGURE 2. LH0002 Schematic Diagram

TABLE I. Buffer Amplifier Typical Characteristics

Parameter	Conditions	LH0002	LH0033	LH0063	Units
DC Output Current Continuous		±100	±100	±250	mA
Peak Output Current		±200	±250	±500	mA
Slew Rate	R_L = 1 kΩ, R_S = 50Ω	200	1500	6000	V/μs
Bandwidth, 3 dB		50	100	180	MHz
Voltage Gain	V_{IN} = 1V @ 1 kHz, R_L = 1k	0.97	0.98	0.98	V/V
Output Offset Voltage	T_C = 25°C, R_S = 100 kΩ (R_S = 300Ω for LH0002)	±10	±5	±10	mV
Input Bias Current	T_C = 25°C	6 μA	50 pA	100 pA	
Output Resistance		6	6	1	Ω

Operation is symmetrical, and the circuit may be analyzed by considering only the upper or the lower half of the circuit as redrawn in *Figure 3*. Input stage operating current is determined by R1 in conjunction with supply and input voltages. For $V_{IN} = 0$ and $V_S = \pm 15V$, first stage quiescent current is typically:

$$I_C = \frac{V_S - V_{BE} - V_{IN}}{R1} = \frac{15 - 0.63 - 0}{5000\Omega} = 2.88\ mA \qquad (1)$$

The normal production variation of I_C is $\pm 5\%$.

The emitter-base junction of the first and second stages appear in series between input and output terminals, therefore the output offset voltage for $V_{IN} = 0$ is the difference in base-emitter junction voltages of a PNP and an NPN transistor. This is true for both upper and lower halves of the circuit, so there is no conflict between the two circuit halves. Output stage quiescent current will equal that of the input stage if the transistors are matched and at equal temperatures. This establishes a class AB bias in the output stage so there is no class B crossover distortion in the output. Resistors R3 and R4 inserted in the output emitter circuits minimize the effect of unmatched upper and lower circuit halves and limit the potential for thermal runaway due to input and output stage temperature differences. There is no thermal runaway if operation is confined within data sheet limits.

Maximum output current is dependent on the supply voltage, R1, Q3 current gain, and the output voltage. Maximum current is available when V_{IN} rises sufficiently above V_{OUT} that Q1 is cut off. Under this condition, the 5k resistor supplies base current to Q3, and the maximum output current is:

$$I_{O(MAX)} = \frac{V_S - V_{BE3} - I_O R3 - V_O}{R1/\beta_3} = \frac{V_S - V_{BE3}}{R1/\beta_3 + R3 + R_L} \cong \frac{V_S - 0.7}{30 + R_L} \qquad (2)$$

where $\beta_3 \cong 200$.

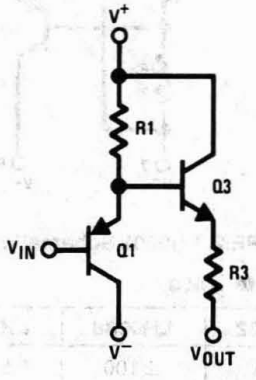

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FIGURE 3. LH0002 Half Circuit

If $V_S = \pm 15V$, the LH0002 can theoretically deliver about 500 mA peak into a shorted load (in practice, only 400 mA peak can be realized, for the current density in the output transistors limits the beta to about 150) or 180 mA peak into 50Ω. Current limiting may be employed for short circuit protection (see section on Current Limiting).

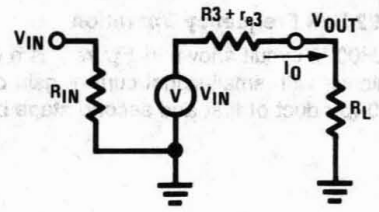
The voltage gain of the LH0002 is slightly less than unity and is a function of load as with any emitter-follower. It is dominated by the finite output resistance of the output stage. Hence, the gain analysis for all three buffers can utilize the hybrid π model as shown in *Figure 4*. Note that r_{e3} is the emitter dynamic resistance of Q3 and is load-current dependent. The gain expression written as a function of load resistance and input voltage is:

$$A_V \cong \frac{R_L}{R_L + R3 + r_{e3}} = \frac{R_L}{R3 + R_L\left(1 + \dfrac{0.026}{V_O + 0.003R_L}\right)} \qquad (3)$$

$$= \left.\frac{R_L}{R3 + R_L\left(1 + \dfrac{0.026}{V_{IN}}\right)}\right|_{V_{IN} > 0.1V}$$

Voltage gain could range from 0.996 for $R_L = 1\ k\Omega$ to 0.978 for $R_L = 100\Omega$ at 10V input. In contrast, the same loads would yield gains of 0.973 to 0.956, respectively, for an input of 1V because r_{e3} would be somewhat larger.

Because of the inherent current-mode feedback, initial offset error is typically 10 mV with a finite (300Ω) series input resistance. Even with unsymmetrical supplies, V_{OS} increases only an additional 3 mV per volt of supply differential. Usually this error component may be ignored as it is relatively small compared to the large-signal error predicted by equation (3) when driving heavy loads.



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Where: $r_{e3} = 0.026/I_O$

FIGURE 4. Equivalent Model of LH0002

LH0002 High Frequency Operation

The high frequency response is limited primarily by internal circuit capacitances; most significant are the junction capacitances shown in *Figure 5*.

Since the base-emitter junction capacitances of emitter-followers see little effective junction voltage change, they may be neglected in the following first-order analysis. For the transistors used we may also assume that the transistor delay and transit time effects are over-shadowed by the RC effect. We can then simplify the half-circuit to that of *Figure 6*: a single transistor emitter-follower plus an equivalent load reflected from the output stage.

Evaluation of the transfer function of equation (4) as derived from *Figure 6b* indicates that the input pole dominates for finite source resistance.

$$\frac{e_o(s)}{e_{in}(s)} = \frac{\left(\frac{R2}{R2 + R_s}\right)\left(\frac{\beta_3 R_L}{\beta_3 R_L + r_{out}}\right)}{[1 + s\,(R2 \| R_s)\,C'_{CB1}]\,[1 + s\,(r_{out} \| \beta_3 R_L)\,C_{CB3}]} \quad (4)$$

$$\cong \frac{A_V \text{ (low frequency)}}{(1 + s\,R_s C_{CB1})\,(1 + s\,r_{e1}\,C_{CB3})}$$

To illustrate, for $R_s = 300\Omega$, the primary pole is predicted to occur at about 60 MHz, a close correlation to the real value, while the output pole is well beyond 1 GHz. The implication of this analysis is quite significant—the fundamental bandwidth of the LH0002 is a function of the input source resistance within a reasonable range of 50Ω to 300Ω. For the case of $R_S = 50\Omega$, the resulting bandwidth is well above 100 MHz.

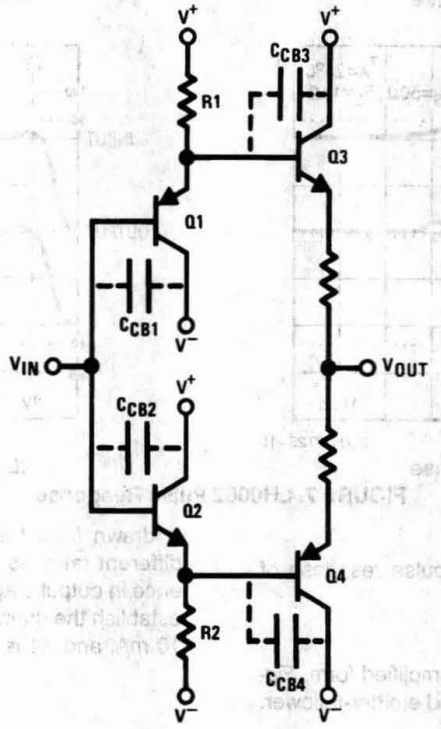

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FIGURE 5. LH0002 High Frequency Circuit

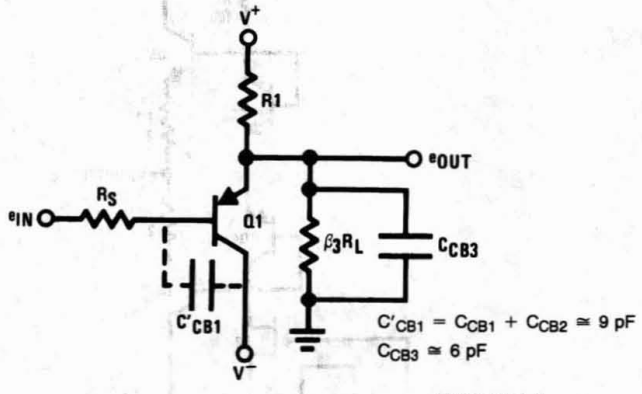

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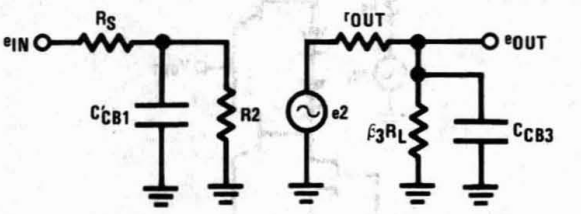
FIGURE 6a. LH0002 Simplified Mirror-Half Input Stage



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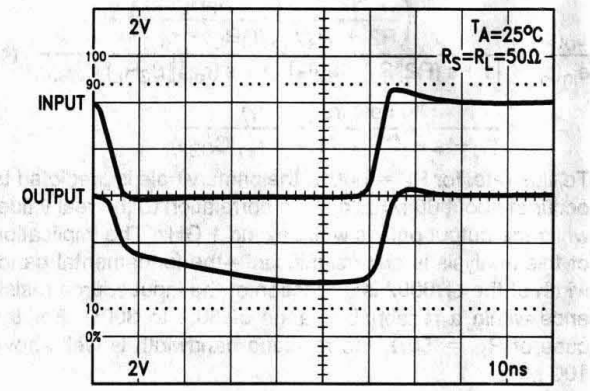
Where: $r_{OUT} \cong \left(r_{e1} + \frac{R_S}{\beta_1}\right) \| R1$

$R2 = \beta_1\,(r_{e1} + R1 \,\|\, \beta_3\,R_L)$

FIGURE 6b. Hybrid π Model



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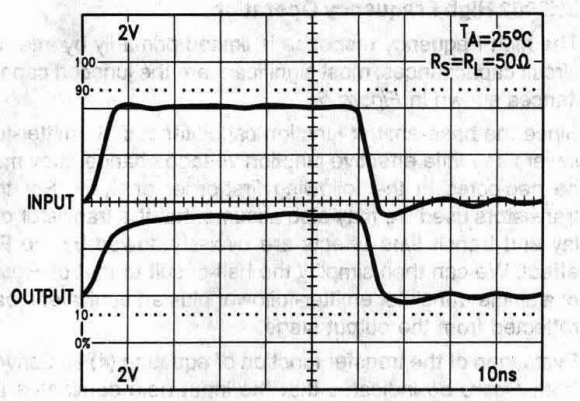
a. Negative Pulse Response



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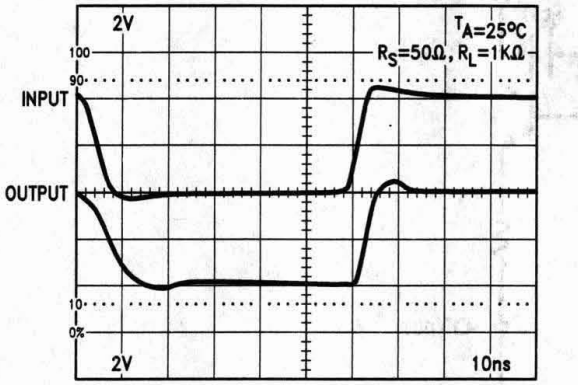
b. Positive Pulse Response



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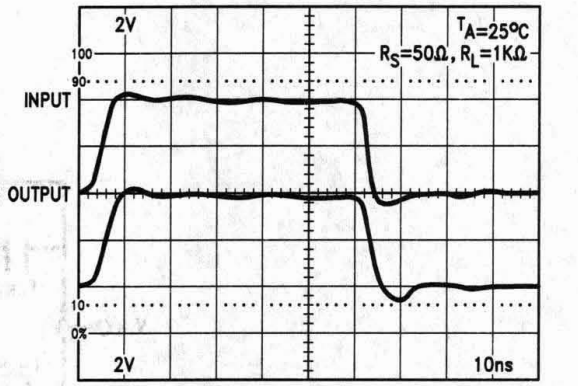
c. Negative Pulse Response



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d. Positive Pulse Response

FIGURE 7. LH0002 Pulse Response

LH0002 Large Signal Pulse Response

Figure 7 shows the typical large signal pulse response of the LH0002.

LH0033 Low Frequency Operation

The LH0033 circuit can be described in simplified form, *Figure 8*, as a source-follower plus a balanced emitter-follower. The complete circuit is shown in *Figure 9*.

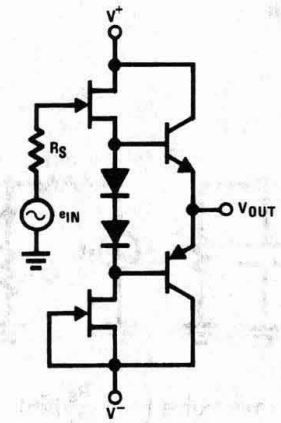

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FIGURE 8. LH0033 Simplified Circuit

When Q1 and Q2 are well matched, offset voltage and drift will be low because the gate-source voltage of Q2, V_{GS2}, is set $\cong 2\ V_{BE}$, thus forcing $V_{GS1} = V_{GS2}$ due to the matching when operating at equal currents. However, as load current is drawn from the output, Q1 and Q2 will drift at slightly different rates as I_{D1} will no longer equal I_{D2} by the difference in output stage base current. Resistor R2 is trimmed to establish the drain current of current-source transistor Q2 at 10 mA, and R1 is trimmed for zero offset.

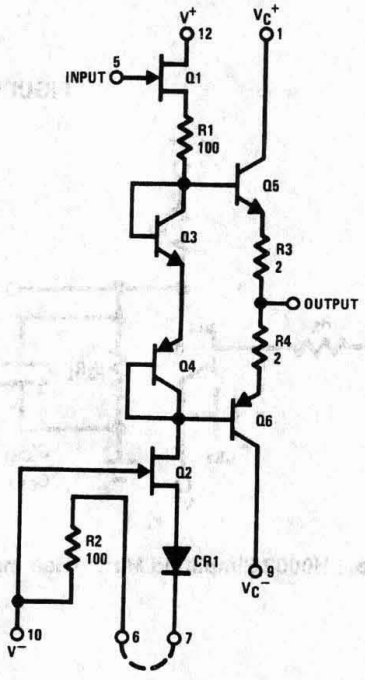

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FIGURE 9. Complete LH0033 Schematic Diagram

The same current flowing through Q2 also flows through Q1 and R1, causing a gate-source voltage of approximately 1.6V. The 10 mA flowing through R1 plus Q3's V_{BE} of 0.6V causes $V_{OUT} = 0$ for $V_{IN} = 0$. The output stage current is established to be approximately equal to that of the input stage by Q3 and Q4.

Voltage gain of the LH0033 is the product of the 1st and 2nd stage gains taken independently. The analysis of each is shown in *Figure 10*. We can write the total amplifier gain expression as:

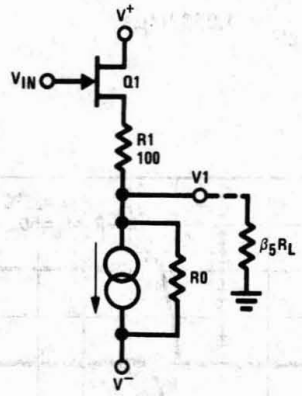
$$A_V = \frac{1}{1 + 2/R_L + 167/\beta_5 R_L + 0.26/V_{IN}} \quad (5)$$

where $\beta_5 \cong 200$.

Voltage gain is predicted to be 0.995 for a 1 kΩ load, and 0.95 for a 50Ω load at 10V output.

LH0033 High Frequency Operation

Low frequency performance is modified at high frequencies by the increasing effect of transistor junction capacitance. Transistors Q3, Q4 and the output emitter-follower pair contribute only minor incremental effect on the first-order high frequency equivalent circuit so they may be omitted to yield the simplified model appearing in *Figure 11*. Modeling of transistor Q1 reduces the circuit to that of *Figure 12*.



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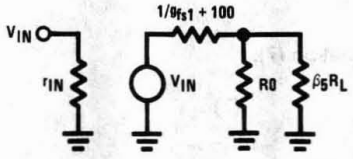

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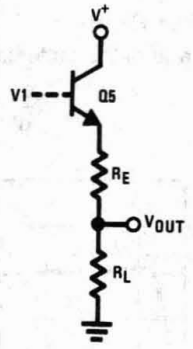
$$A_{v1} = \frac{R0 \| \beta_5 R_L}{R0 \| \beta_5 R_L + 1/g_{fs1} + R1} = \frac{1}{1 + 167/R0 + 167/\beta_5 R_L}$$

for: $g_{fs1} \cong 0.015$ mho

$$R0 \cong \frac{1}{g_{os2}}(1 + g_{fs2}R2) = 125\ k\Omega$$

a. Hybrid π Model of FET Source-Follower Including Effect of Output Load



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$$A_{v2} = \frac{R_L}{R_L + R_E + r_{e5}} = \frac{1}{1 + R_E/R_L + 0.026/V1}$$

b. Output Stage Gain with the Effect of Emitter Dynamic Resistance

FIGURE 10. Voltage Gain Analysis of the LH0033

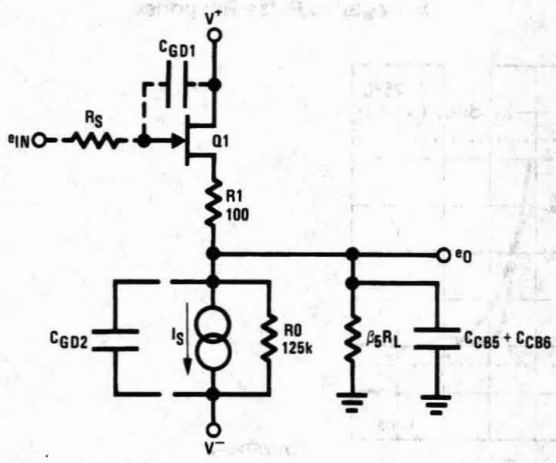

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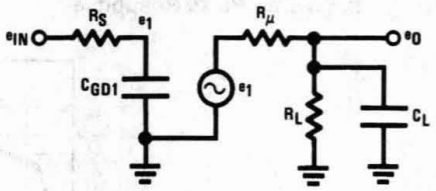
FIGURE 11. LH0033 Simplified Circuit



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Where: $R\mu = R1 + 1/g_{fs1}$

$R_L = R0 \| \beta_5 R_L$

$C_L = G_{GD2} + C_{CB5} + C_{CB6}$

FIGURE 12. LH0033 High Frequency Circuit Model

Capacitors C_{CB5} and C_{CB6} are collector-base junction capacitances of Q5 and Q6, typically 3 pF each. C_{GD1} and C_{GD2} are the gate-drain capacitances of the FETs, typically 3.5 pF each. The frequency-dependent transfer function of the circuit is:

$$\frac{e_0(s)}{e_{in}(s)} = \frac{R_L/(R_L + R1)}{[1 + s\,R_S C_{GD1}]\,[1 + s(R_\mu \| R_L)\,C_L]} \quad (6)$$

Notice that unlike the LH0002, the output pole ($s = 1/R_\mu C_L$) dominates the primary frequency response roll-off occurring at about 100 MHz with an input source resistance $R_S = 50\Omega$. The user is cautioned that as R_S increases, the secondary (input) pole will begin to take effect. To illustrate, for $R_S = 300\Omega$, the secondary pole will have moved from 900 MHz at $R_S = 50\Omega$ to about 150 MHz.

LH0033 Slew Rate

The slew rate of the buffer is predicted by equation (7),

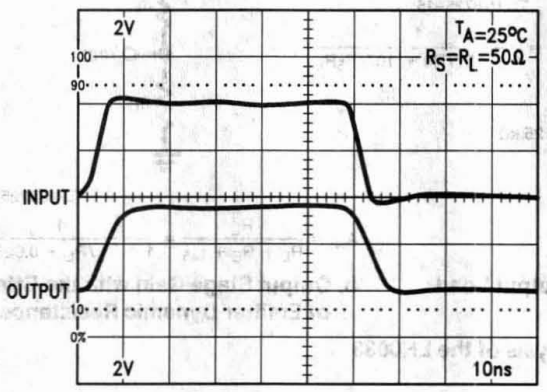
$$\frac{dv}{dt} = \frac{I}{C_L} \quad (7)$$

where I is the input stage current available to charge the circuit capacitance C_L.

With the LH0033, the positive slew is 2–3 times greater than the negative slew. The pulse response in *Figure 13* illustrates this. The reason is that during positive slew, the peak charging current is limited by the value of R1 plus R_S when the FET gate-source junction is forward biased. This could be 30 mA–40 mA peak, allowing a typical slew rate of 3,000 V/μs.

The LH0033 negative-going slew is limited by its input stage quiescent current of 10 mA established by the FET current source. As the input transistor tends to shut off, the circuit capacitance discharges into the current source (sink) at a rate of 10 mA. Therefore, the slew rate is computed to be:

$$\frac{dv}{dt} = \frac{10\text{ mA}}{9.5\text{ pF}} = 1{,}050\text{ V}/\mu\text{s}$$



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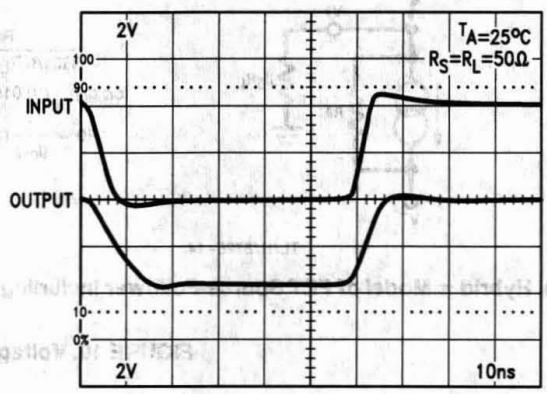
a. Positive Pulse Response



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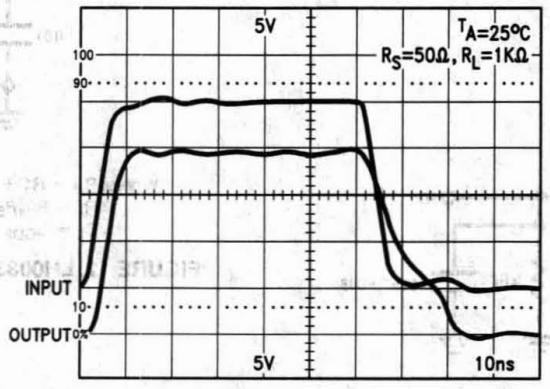
b. Negative Pulse Response



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c. ± 10V Pulse Response

FIGURE 13. LH0033 Large Signal Pulse Response

LH0063 Low Frequency Operation

The LH0063 exhibits several times the slew rate and bandwidth of the LH0033 due to a higher input stage operating current. The push-pull design of the first stage also allows the input FETs to be forward biased for either positive or negative-going input signals. The schematic diagram of *Figure 14* shows a pair of complementary FETs at the input stage. Transistor Q1 is biased by the current source Q4. Resistor R1 is trimmed for a 30 mA input stage operating current. Similarly, Q2 is biased to 30 mA by the current source Q3 and R2. Transistor Q5 and resistors R3 and R4 establish a $2V_{BE}$ forward diode equivalent between the Q6 and Q7 bases. These resistors are trimmed such that the output stage operates at a quiescent current of about 1 mA. Each FET gate-source voltage cancels each output transistor V_{BE} drop. Hence, the output of the buffer sits at 0V for an input 0V. The zero-offset voltage-follower action holds for any input voltage within the buffer operating voltage range.

Because of the high current drive capability, multiple output transistors are employed to limit output transistor current density. Four output degeneration resistors of 1Ω each help to prevent thermal runaway.

The DC voltage gain equation is similar to that of the LH0033. Equation (5) may be used without introducing significant error. It needs modification only because of the multiple transistor output stage. Therefore, the LH0063 voltage gain equation is approximately:

$$A_V \cong \frac{1}{1 + 0.5/R_L + 1g_{fs1}\beta_6 R_L + 0.026/2V_{IN}} \quad (8)$$

where: $\beta_6 \cong 200$, $g_{fs1}\beta 0.010$ mho.

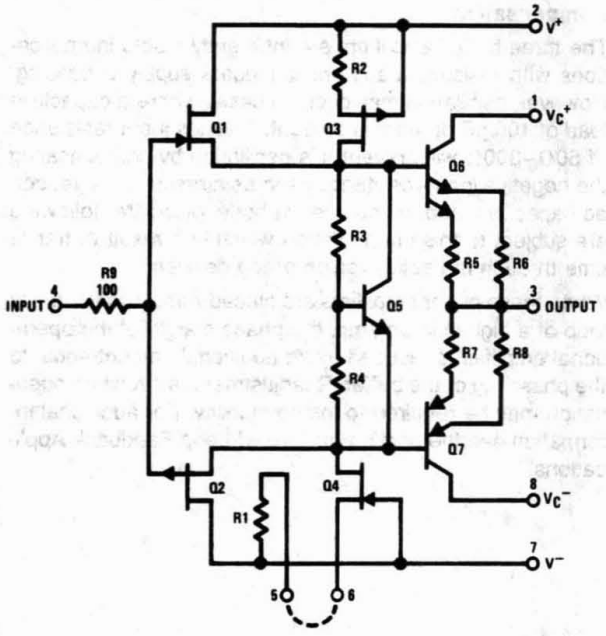

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FIGURE 14. Complete LH0063 Schematic Diagram

LH0063 High Frequency Operation

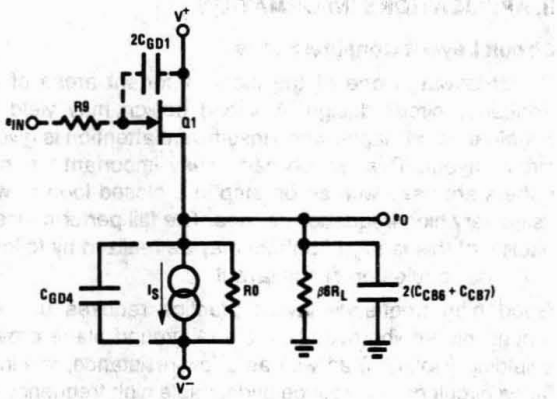
The high frequency equivalent circuit may omit the output stage, including only its load effect. The two mirrored half-circuits, consisting of a pair of complementary junction FETs and their respective current sources, can be reduced to a single half-circuit with the combined effect of both as shown in *Figure 15*.

The frequency-dependent transfer function of the LH0063 as derived from *Figure 15b* is:

$$\frac{e_o(s)}{e_{IN}(s)} = \frac{R_L/(R_L + 1/2g_{fs1})}{[1 + s2R_9 C_{GD1}]\left[1 + s\left(\frac{2}{2g_{fs1}} \parallel R_L\right)C_L\right]} \quad (9)$$

$$= \frac{A_V \text{ (low freq.)}}{[1 + s2R_9 C_{GD1}]\left[1 + s\left(\frac{1}{2g_{fs1}}\right)C_L\right]}$$

Similar to the LH0033, equation (9) indicates that the device output pole ($s = -2g_{fs1}/C_L$) dominates for small value input source resistance (R9 = 100Ω). Using the parameter values given in *Figure 15b*, equation (9) predicts the primary pole to occur at about 190 MHz, and the secondary (input) pole at beyond 300 MHz.



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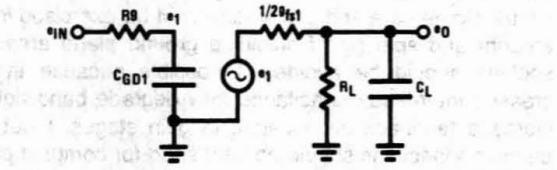
a. Lumping the Combined Effects of Two Complementary Input Stages



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$g_{fs1} \cong 0.010$ mho, $R_L = R0 \| \beta_6 R_L$

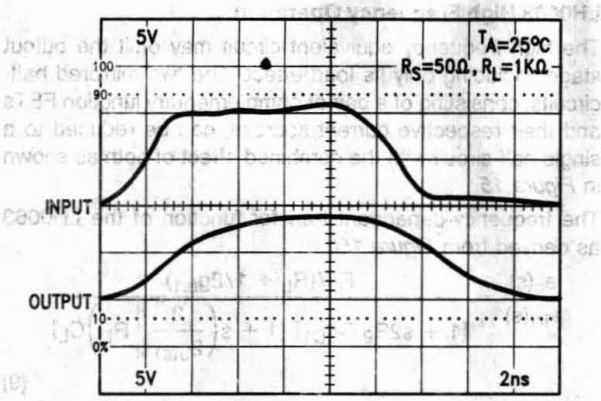
$C_L = 2(C_{CB6} + C_{CB7}) + C_{GD4}$

$C_{CB6} \cong C_{CB7} = 3pF$

$C_{GD1} \cong C_{GD4} = 3.5$ pF

b. Hybrid π Model of the Source Follower Substituted in the Composite Model

FIGURE 15. LH0063 Simplified High Frequency Circuit Model



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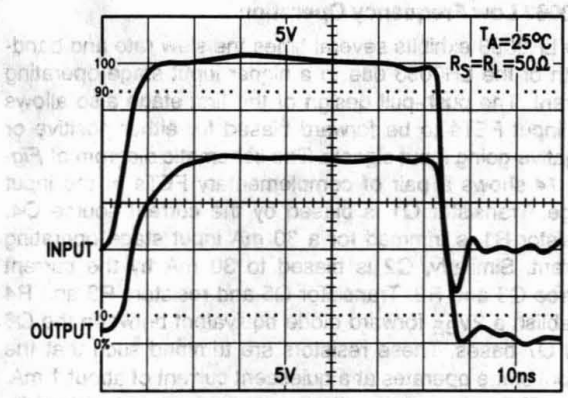
a. Positive Pulse Response



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b. ±10V Pulse Response

FIGURE 16. LH0063 Large Signal Pulse Response

LH0063 Large Signal Pulse Response

Figure 16 demonstrates the large signal pulse response capability of the LH0063 under different load conditions. Note the higher positive as well as negative-going slew rate achieved with the complementary FET input stage operating at higher current, a response superior to that of the LH0033.

II. APPLICATIONS INFORMATION

Circuit Layout Considerations

Circuit layout is one of the most important areas of high frequency circuit design. A sound design may yield only marginal performance when insufficient attention is given to circuit layout. This will be particularly important when the buffers are used with an op amp in a closed loop or when using very high frequency devices. The full performance capability of this family of buffers may be realized by following a few basic rules on circuit layout.

Good high frequency layout practice requires use of a ground plane wherever possible. A ground plane provides shielding (isolation) as well as a low-resistance, low-inductance circuit path to reduce undesirable high frequency coupling. In some cases, signal paths should be shielded by a surrounding ground plane to minimize stray signal pick-up; however, this shielding can cause increased stray capacitance which may be harmful at high impedance points in the circuit. Some care and judgement must be exercised in the amount and spacing of shielding ground plane areas. IC sockets should be avoided if possible because the increased inter-lead capacitance may degrade bandwidth or increase feedback capacitance in gain stages. Input and output connections should be kept short for compact physical layout and minimum coupling. When used with an op amp, layout should minimize capacitance from output to feedback point and from feedback summing junction to ground. Supply and output signal traces should be as wide as practical for these high-current devices.

Power Supply Decoupling

The positive and negative power supply terminals of the devices must be bypassed to ground with one or two 0.1 μF monolithic ceramic capacitors. They should be placed no more than 1/4 to 1/2 inch from the device pins. In difficult cases with the LH0033 and in all cases with the LH0063, a 4.7 μF solid tantalum bypass should also be added at both the plus and minus supplies. The circuit board trace between capacitor ground points should be short and of low inductance.

Compensation

The three buffer amplifiers are inherently stable in applications with resistive loads and adequate supply bypassing. However, oscillation may occur in cases where a capacitive load of 100 pF or more is present. A series input resistance of 50Ω–300Ω will prevent this oscillation by compensating the negative input-resistance seen as a result of the reflected capacitive load. All source, cathode, or emitter-followers are subject to this phenomenon which is a result of transit time through the active region of the devices.

When these buffer amplifiers are placed within the feedback loop of a high-gain op amp, the phase margin of the operational amplifier is reduced by an additional amount equal to the phase lag of the buffer. Readjustment of circuit compensation may be required to insure stability. For additional information see the section on Closed-Loop Feedback Applications.

Power Disspation and Device Rating

Each data sheet specifies the conditions for safe operating power dissipation. These limits must be observed for both continuous and pulsed conditions. *Figure 17* shows the power dissipation limits versus temperature for each device, both with and without heat sinks. To compute total power dissipation, the standby power must be added to the load-related power.

The standby power drain is computed from the device DC operating current and its operating voltage:

$$P_{standby} = (V_S^+ - V_S^-)I_S \quad (10)$$

The load-related power is the average power dissipated in the output stage. It may be estimated as the product of average current delivered to the load and the average voltage across the output stage. Because of the high-current capability of the buffers, it is essential to observe the device dissipation limits. Safe operating areas for each buffer are presented in *Figure 18*. A note of caution: these plots are valid only for 25°C ambient. Additional power derating based on the power derating curves of *Figure 17* is mandatory for operation at higher ambient temperature.

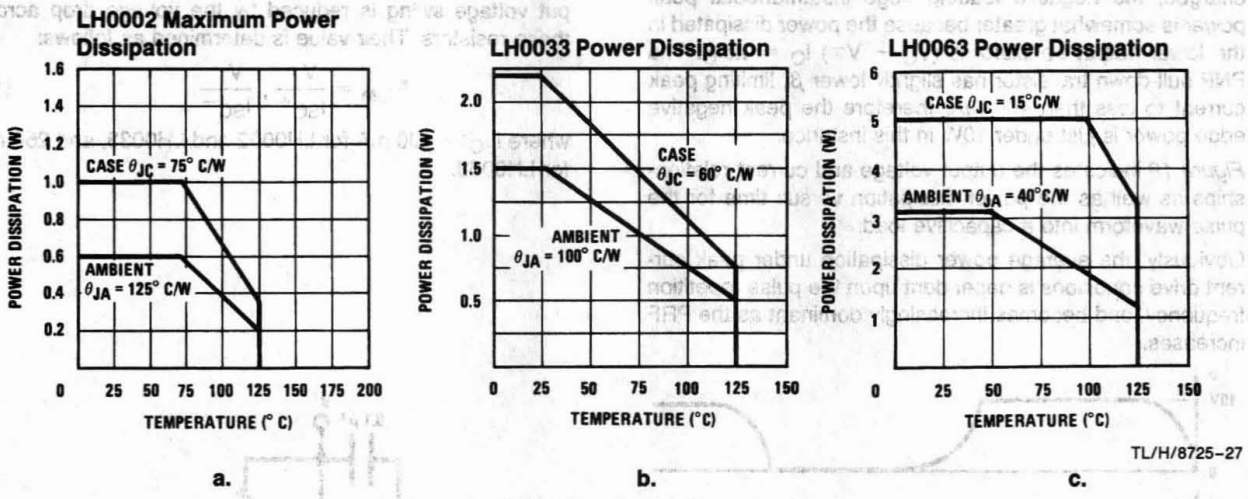


FIGURE 17. Device Power Dissipation

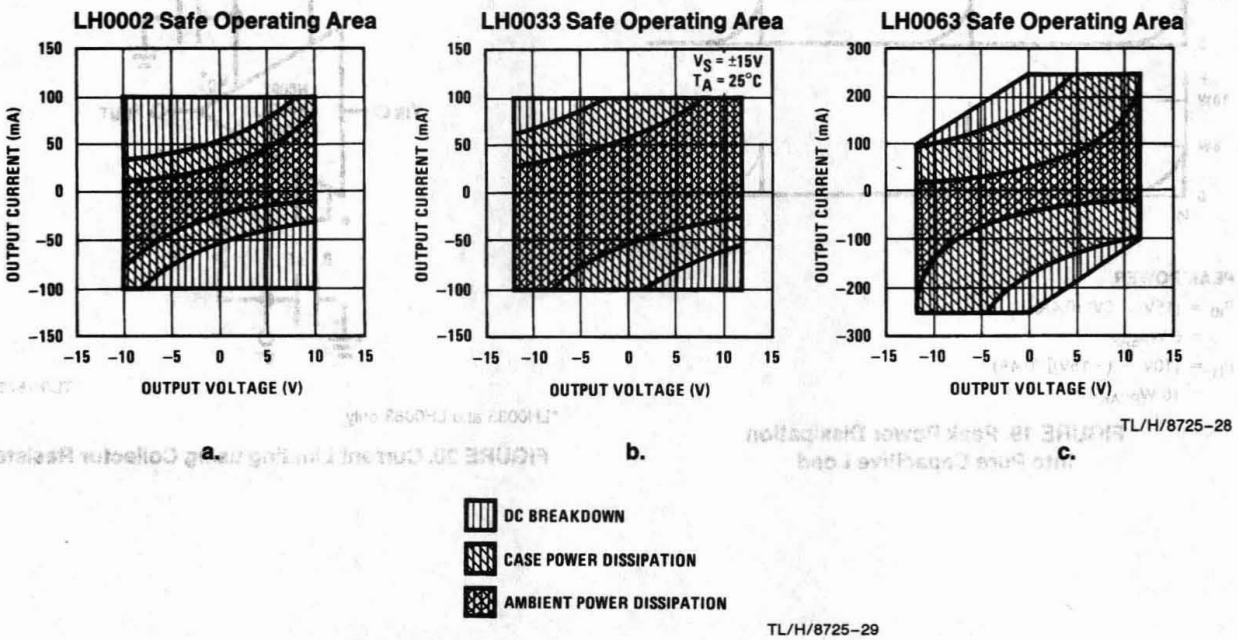


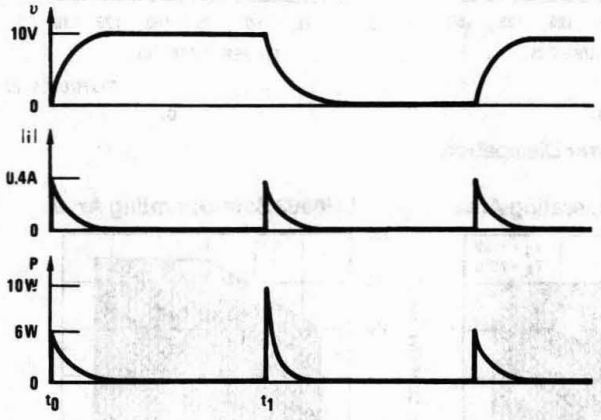
FIGURE 18. Safe Operating Areas at 25°C and $V_S = \pm 15V$

Peak Power Dissipation

An often overlooked power dissipation factor exists when driving a reactive load. Consider the LH0002 with a possible 400 mA peak current drive capability when driving 10V square pulses into 1000 pF. At the rising edge, the upper device transistor charges the capacitor at its limiting current. The charging waveform is not linear, in fact it approaches a logarithmic curve because the resistor $R1/\beta 3$ appears as the principal value of charging resistance [see equation (2)]. The instantaneous power dissipation is simply the product of V^+ and $I_{O(MAX)}$, or 6W, with occurrences at the positive and negative leading edges. Once the load capacitor is charged, the negative leading edge instantaneous peak power is somewhat greater because the power dissipated in the lower output transistor is $(V_O - V^-)\ I_O = 25I_O$. The PNP pull-down transistor has slightly lower β, limiting peak current to less than 400 mA, therefore the peak negative edge power is just under 10W in this instance.

Figure 19 indicates the output voltage and current relationships as well as the power dissipation versus time for the pulse waveform into a capacitive load.

Obviously, the average power dissipation under peak current drive conditions is dependent upon the pulse repetition frequency, and becomes increasingly dominant as the PRF increases.



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PEAK POWER

P_{t0} = (15V − 0V) (0.4A)
= 6 W_{PEAK}

P_{t_1} = [10V − (−15V)] (0.4A)
= 10 W_{PEAK}

FIGURE 19. Peak Power Dissipation Into Pure Capacitive Load

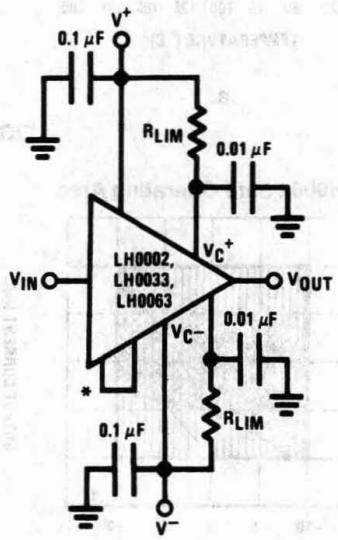
Because each of the buffer amplifiers may be operated on dissimilar supply voltages for input and output stages, device power dissipation is reduced by lowering the output stage supply voltages while retaining the input stage supplies at a higher level for best current driving capability. The limiting factor is, of course, a reduced output voltage swing.

Current Limiting

Current limiting may be provided in either of two ways: by adding series resistors at the collectors of the output stage, or by a single series resistor at the buffer output. The first method (*Figure 20*) is preferred as there is little effect on output resistance and peak current drive. However, the output voltage swing is reduced by the voltage drop across these resistors. Their value is determined as follows:

$$R_{LIM} = \frac{V^+}{I_{SC}^+}, \frac{V^-}{I_{SC}^-} \qquad (11)$$

where I_{SC} = 100 mA for LH0002 and LH0033, and 250 mA for LH0063.



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*LH0033 and LH0063 only

FIGURE 20. Current Limiting using Collector Resistors

The output collectors should be bypassed with 0.01 μF capacitors in addition to the normal supply bypassing, as shown in *Figure 20*. The 0.01 μF capacitors will allow full output voltage and current on an instantaneous basis for transient pulses yet at the same time prevent output stage resonant oscillation.

Alternate active current limit techniques that retain almost the full DC output swing are shown in *Figure 21*. In these circuits, the current sources are saturated during normal operation and thus apply nearly full supply voltage to the load. Under fault conditions, the voltage decreases as determined by the overload.

For *Figure 21a*, the limit-set resistor is set for 60 mA.

$$R_{LIM} = V_{BE}/I_{SC} = 0.6V/0.06A = 10\Omega$$

In *Figure 21b*, the current limit has been set to 200 mA.

$$R_{LIM}\frac{V_{BE}}{I_{SC}} = \frac{0.6V}{0.2A} = 3.0\Omega$$

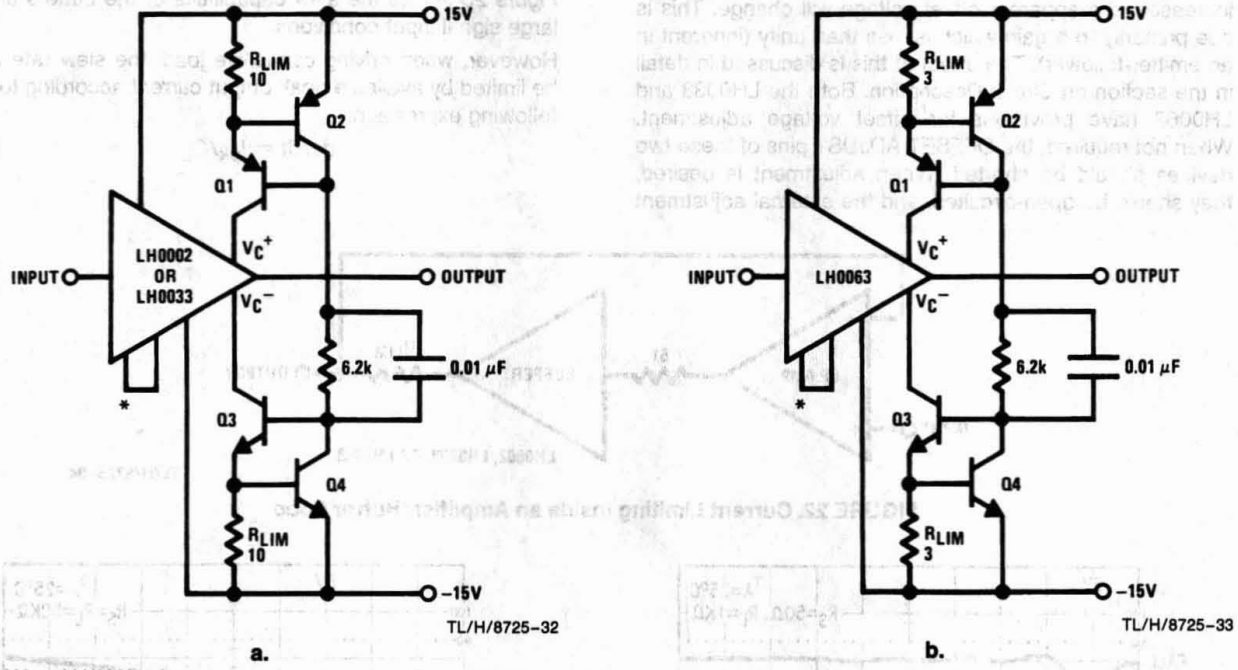
For applications where the buffers are inside the feedback loop of an op amp such as LH0032, LH0024, LH0062 or LM118, a single current limiting resistor may be placed inside the feedback loop at the buffer output as shown in *Figure 22*. Its value is also computed as $R_{LIM} = V^+/I_{SC}$.

Heat Sinking

In order to utilize the full drive capabilities of these devices, low thermal resistance heat sinks should be used. The cases of all three devices are isolated from the circuit and may be connected to system ground or to the buffer output as desired. The following list gives thermal reistance of various heat sinks available for the buffers.

TABLE II. Heat Sinks For LH0033 and LH0063

LH0033	LH0063
Thermalloy 2240A, 33°C/W	Thermalloy 6002B-19, 6°C/W
Wakefield 215CB, 30°C/W	IERC LAIC3V4BC
IERC UP-TO8-48CB, 15°C/W	IERC HP1-TO3-33CB 7°C/W



*LH0033 and LH0063 only

FIGURE 21. Current Limiting using Current Sources

Capacitive Loads

All three devices are capable of driving relatively high capacitive loads. Because capacitive loads on emitter-followers are reflected to the input as negative resistances, it is necessary to add some series compensating positive real resistance; 50Ω–300Ω is usually sufficient. An alternative is to insert the current limiting resistor at the output as shown in *Figure 22*. This will isolate the capacitive load from the buffer.

Any of the buffers can drive twisted pair, shielded or coaxial cables, or other reactive loads. For all practical purposes, an unterminated coaxial cable presents a capacitive load to the driver. On the other hand, terminated coaxial cables appear as resistive loads, and therefore may not require the compensation for capacitive loads. Don't forget consideration of peak power dissipation when driving cable loads, since they may represent capacitive loads (see section on Peak Power Dissipation).

Offset Voltage and Adjustment

Offset voltage is measured with $V_{IN} = 0$. As V_{IN} and I_L are increased, the apparent offset voltage will change. This is due primarily to a gain which is less than unity (inherent in an emitter-follower). The effect of this is discussed in detail in the section on Circuit Description. Both the LH0033 and LH0063 have provisions for offset voltage adjustment. When not required, the OFFSET ADJUST pins of these two devices should be shorted. When adjustment is desired, they should be open-circuited, and the external adjustment is accomplished with a 200Ω variable resistor inserted between V⁻ and pin 7 of the LH0033 or pin 6 of the LH0063. It is good practice to insert a 20Ω resistor in series with the variable resistor to limit excessive power dissipation at the input stage when the pot is at minimum value. The offset adjustment range is typically ±400 mV.

When a buffer amplifier is used as a current booster in conjunction with an operational amplifier, as in *Figure 22*, there is usually no need for output offset adjustment, since the offset is reduced by the open-loop to closed-loop gain ratio.

The total offset of the closed-loop circuit is:

$$V_{OS(TOTAL)} = V_{IOS} \pm V_{OOS}\frac{A_{CL}}{A_{OL}} \qquad (12)$$

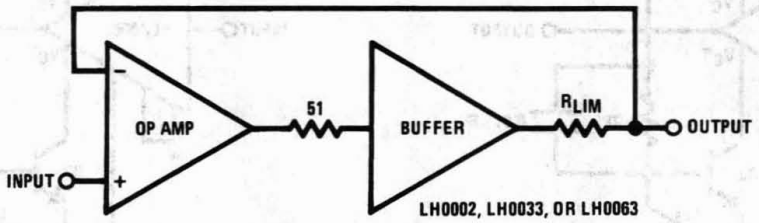
where: V_{IOS} = input offset voltage.
V_{OOS} = buffer offset voltage.

Slew Rate

Slew rate is the rate of change of output voltage for large-signal step input changes. For resistive load, slew rate is limited by internal circuit capacitance and operating current. *Figure 23* shows the slew capabilities of the buffers under large-signal input conditions.

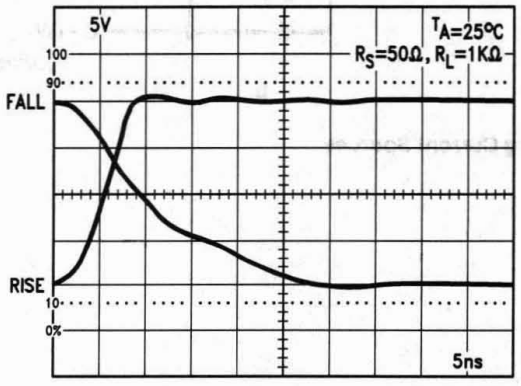
However, when driving capacitive load, the slew rate may be limited by available peak output current according to the following expression.

$$dv/dt = I_{pk}/C_L \qquad (13)$$



TL/H/8725–34

FIGURE 22. Current Limiting Inside an Amplifier/Buffer Loop



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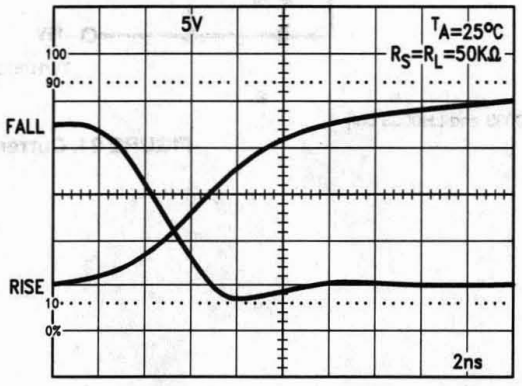
a. LH0033 Slew Response



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b. LH0063 Slew Response

FIGURE 23. Positive and Negative Slew of Each Buffer

Note that the peak current available to the load decreases as C_L changes [see equation (2)]. *Figure 24* illustrates the effect of the load capacitance on slew rate for the three buffers. Slew rate tests are secified for resistance and/or very small capacitance load, otherwise the slew rate test would be a measure of the available output current. For highest slew rate, it is obvious that stray load capacitance should be minimized.

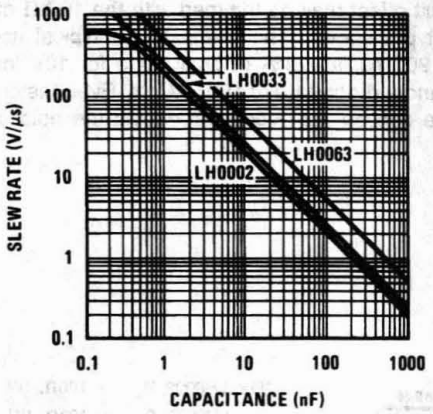

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FIGURE 24. Slew Rate vs Load Capacitance

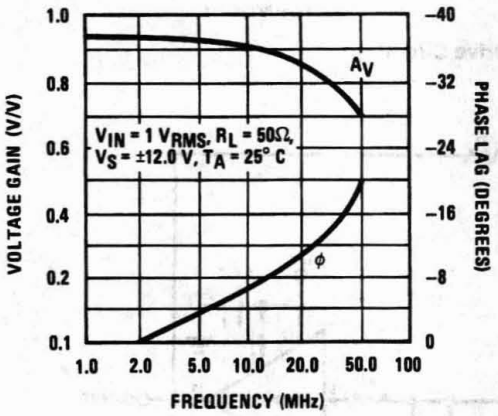
Distortion

The output stage of the three buffer amplifiers are biased at 1 mA to 10 mA to remove any possibility of crossover distortion. The LH0063 may exhibit a small amount of crossover distortion in some circumstances due to the relatively low 1 mA output stage bias. The heavy local feedback inherent in emitter-follower or source-follower operation provides a very low distortion output. The remaining distortion (<0.1%) is primarily due to the modulation effect of nonconstant V_{CE} as the output voltage changes.

Closed-Loop Feedback Operation

Any of the buffer amplifiers may be used inside an op amp feedback loop. When this is done, the additional phase lag introduced by the buffer must be included in loop stability consideration. With most op amps, the bandwidth of these buffers is so great that the op amp totally controls the loop stability. However, when using very wide-band op amps such as the LH0024, LH0032, and LH0062, the small additional phase lag of the buffers should be taken into consideration. *Figure 25* presents the Bode plots of gain and phase for the three buffers. The phase margin and open loop frequency response is altered by the additional pole(s) contributed by the buffer. The buffer phase shift is algebraically summed with the op amp phase shift, and may cause a stable op amp loop to become marginally stable depending upon the relative positions of the op amp and buffer poles. In general, the buffer bandwidth should significantly exceed that of the op amp, so that the loop performance will be determined solely by the op amp.

LH0002 Frequency Response



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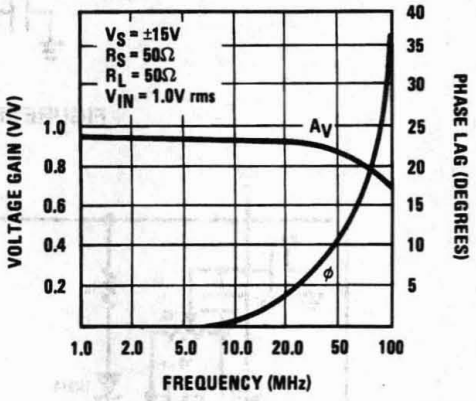
LH0033 Frequency Response



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LH0063 Frequency Response

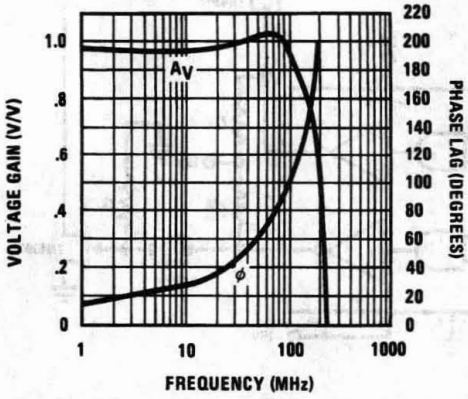

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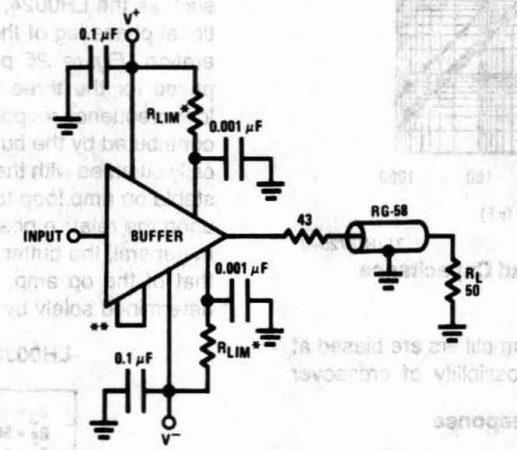
FIGURE 25. Phase-Gain Relationships of Buffers

III. APPLICATIONS CIRCUITS

Because of their high current drive capability, the LH0002, LH0033 and LH0063 buffer amplifiers are suitable for driving terminated or unterminated coaxial cables, and high current or reactive loads. Current limiting resistors should be used to protect the device from excessive peak load currents or accidental short circuit. There is no current limiting built into the devices other than that imposed by the limited beta of the output transistors. *Figure 26* shows a coaxial cable drive circuit. The 43Ω resistor matches the driving source to the cable; however, its inclusion will rarely result in visible improvement in pulse response into a terminated cable. If the 43Ω resistor is included, the output voltage to the load is about half what it would be without the near end termination.

The LH0033 and LH0063 are useful in high speed sample-and-hold or peak detector circuits because of their very high speed and low-bias-current FET input stages. The high speed peak detector circuit shown in *Figure 27* could be changed to a sample-and-hold circuit simply by removing the detector diode and the reset circuitry. For best accuracy, the circuit offset may be trimmed with the 10 kΩ offset adjustment pot shown. The circuit has a typical acquisition time of 900 ns, to 0.1% of final value for 10V input step signal, and a droop rate of 100 μV/ms. Even faster acquisition time can be achieved by reducing the hold capacitor value.



*For: LH0002, R_{LIM} = 100Ω, 1W
LH0033, R_{LIM} = 100Ω, 1W
LH0063, R_{LIM} = 60Ω, 5W
**Jumper for LH0033 and LH0063 only.

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FIGURE 26. Coaxial Cable Drive Circuit

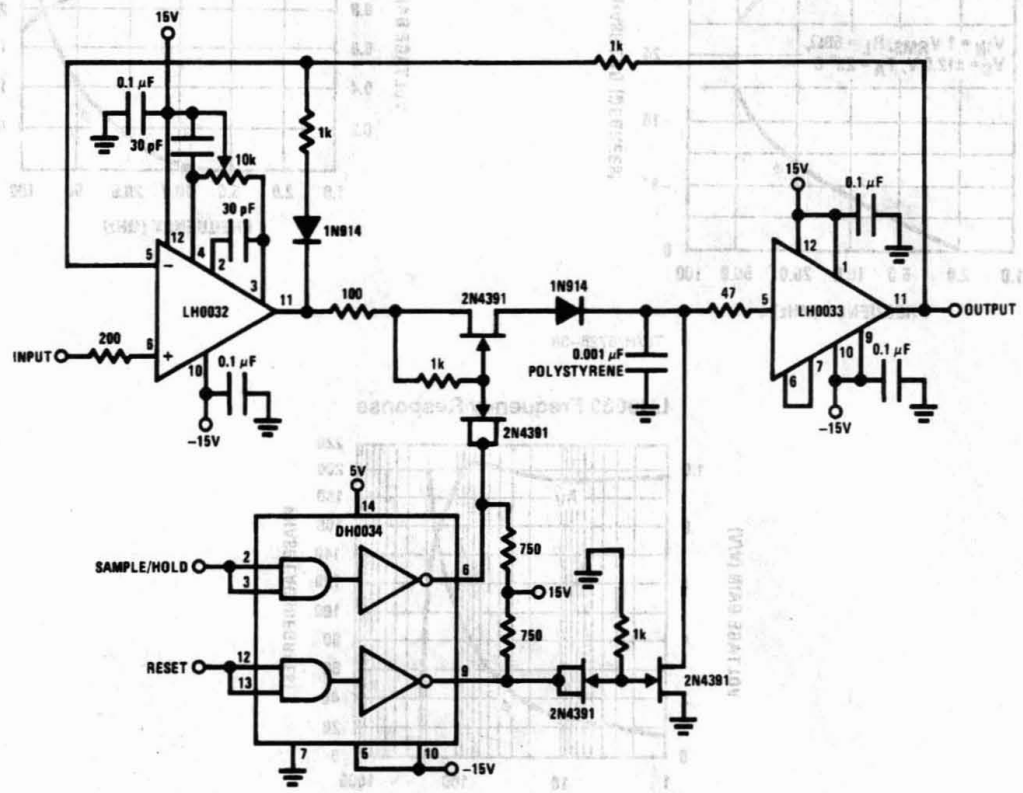

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FIGURE 27. High Speed Peak Detector with Hold and Reset Controls

The LH0033 may be used as a cable-shield driver as shown in *Figure 28*. The advantage is that the source driver is not required to charge the line capacitance of the unterminated coaxial cable, and indeed does not need to match its line impedance; therefore, high speed data transmission is permitted.

The buffers may be used with a single supply without special considerations. A typical application is shown in *Figure 29*. The input is DC biased to mid-operating point and is AC coupled. Its input impedance is approximately 500 kΩ at low frequencies. Note that for DC loads referenced to ground, the quiescent current is increased by the load current set at the input DC bias voltage.

The high input impedance of the LH0033 and LH0063 are suitable for active filter applications. A basic two pole, high pass filter is diagrammed in *Figure 30* using the LH0033. The circuit provides a 10 MHz cutoff frequency. One consideration of the filter is its apparent gain change due to the finite output impedance of the amplifier, which affects the overall gain and the damping factor of the filter stage. Resistor R3 ensures that the input capacitance of the amplifier does not interact with the filter response at the frequency of interest.

An equivalent low pass filter is similarly obtained by capacitance and resistance transformation.

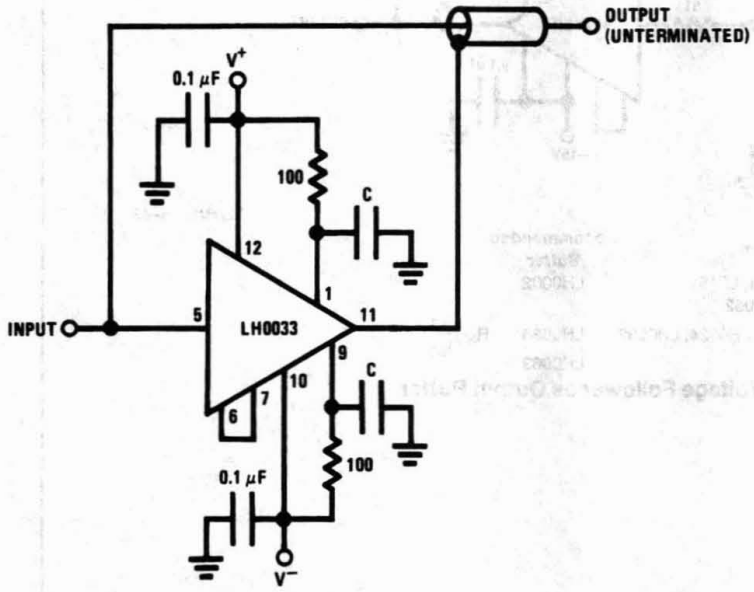

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FIGURE 28. High Speed Shield/Line Driver

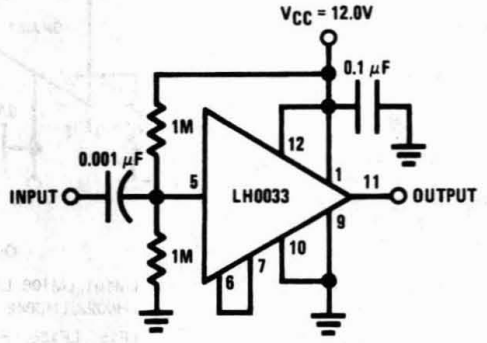

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FIGURE 29. Single Supply AC Buffer Amplifier

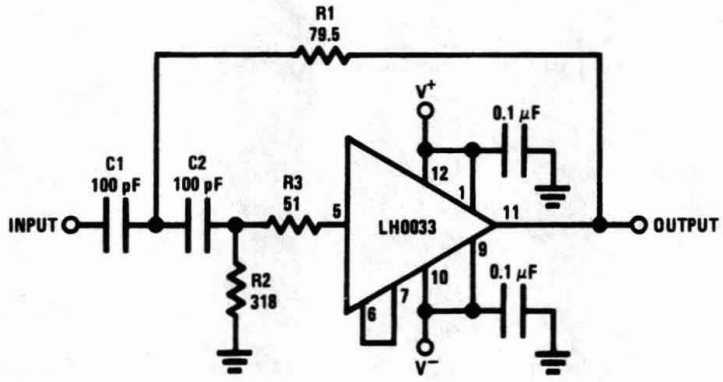

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FIGURE 30. Wide Band Two Pole High Pass Filter

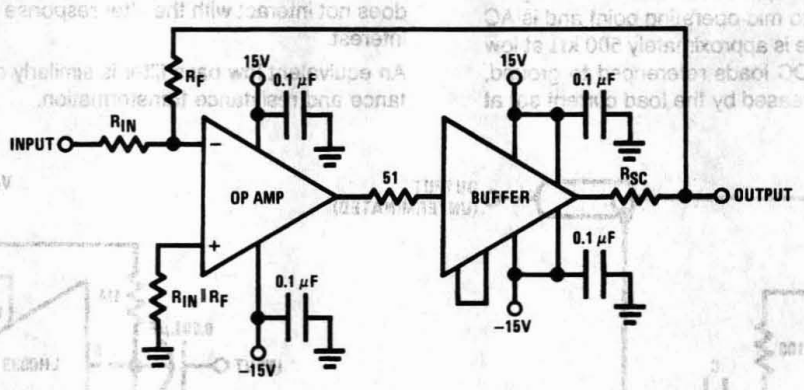
The most common use of the buffers is inside an op amp feedback loop as shown in *Figure 31*. The chart in the figure shows the ideal match of the buffer family to most popular operational amplifiers.

REFERENCES

George S. Moschytz, "Linear Integrated Networks Design," Ch. 3, Active Filter Building Blocks.

"Application of the LH0002 Current Amplifier," National Semiconductor Corporation, AN-13, September 1968.

B. Siegel and L. Van Der Gaag, "Applications For a New Ultra-High Speed Buffer," National Semiconductor Corporation, AN-48, August 1971.



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Op Amp	Recommended Buffer	
LM101, LM108, LM741, LF151 LH0022, LH0042, LH0052	LH0002	
LF155, LF156, LF157, LH0024, LH0032	LH0033	$R_{SC} \frac{V_S}{I_{SC}}$
LH0024, LH0032	LH0063	

FIGURE 31. Using Voltage Follower as Output Buffer

The A/D Easily Allows Many Unusual Applications

National Semiconductor
Application Note 233

Accommodation of Arbitrary Analog Inputs

Two design features of the ADC0801 series of A/D converters provide for easy solutions to many system design problems. The combination of differential analog voltage inputs and a voltage reference input which can range from near zero to $5V_{DC}$ are key to these application advantages.

In many systems the analog signal which has to be converted does not range clear to ground (0.00 V_{DC}) nor does it reach up to the full supply or reference voltage value. This presents two problems: 1) a "zero-offset" provision is needed—and this may be volts, instead of the few millivolts which are usually provided; and 2) the "full scale" needs to be adjusted to accommodate this reduced span. ("Span" is the actual range of the analog input signal, from $V_{IN\ MIN}$ to $V_{IN\ MAX}$.) This is easily handled with the converter as shown in *Figure 1*.

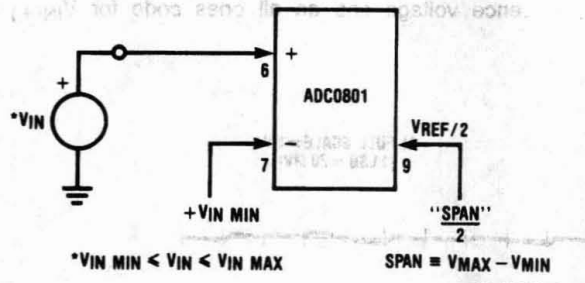

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FIGURE 1. Providing Arbitrary Zero and Span Accommodation

Note that when the input signal, V_{IN}, equals $V_{IN\ MIN}$ the "differential input" to the A/D is zero volts and therefore a digital output code of zero is obtained. When V_{IN} equals $V_{IN\ MAX}$, the "differential input" to the A/D is equal to the "span" (for reference applications convenience, there is an internal gain of two to the voltage which is applied to pin 9, the $V_{REF}/2$ input), therefore the A/D will provide a digital full scale. In this way a wide range of analog input voltages can be easily accommodated.

An example of the usefulness of this feature is when operating with ratiometric transducers which do not output the complete supply voltage range. Some, for example, may output 15% of the supply voltage for a zero reading and 85% of the supply for a full scale reading. For this case, 15% of the supply should be applied to the $V_{IN(-)}$ pin and the $V_{REF}/2$ pin should be biased at one-half of the span, which is ½ (85%−15%) or 35% of the supply. This properly shifts the zero and adjusts the full scale for this application. The $V_{IN(-)}$ input can be provided by a resistive divider which is driven by the power supply voltage and the $V_{REF}/2$ pin should be driven by an op amp. This op amp can be a unity-gain voltage follower which also obtains an input voltage from a resistive divider. These can be combined as shown in *Figure 2*.

This application can allow obtaining the resolution of a greater than 8-bit A/D. For example, 9-bit performance with the 8-bit converter is possible if the span of the analog input voltage should only use one-half of the available 0V to 5V span. This would be a span of approximately 2.5V which could start anywhere over the range of 0V to $2.5V_{DC}$.

The RC network on the output of the op amp of *Figure 2* is used to isolate the transient displacement current demands of the $V_{REF}/2$ input from the op amp.

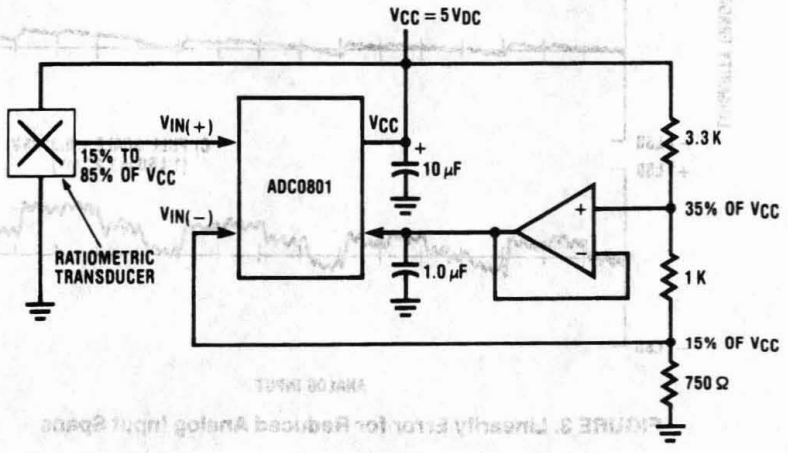

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FIGURE 2. Operating with a Ratiometric Transducer which Outputs 15% to 85% of V_{CC}

Limits of $V_{REF}/2$ Voltage Magnitude

A question arises as to how small in value the span can be made. An ADC0801 part is shown in *Figure 3* where the $V_{REF}/2$ voltage is reduced in steps: from A), 2.5V (for a full scale reading of 5V); to B), 0.625V (for a full scale reading of 1.25V—this corresponds to the resolution of a 10-bit converter over this restricted range); to C), 0.15625V (for a full scale reading of 0.3125V—which corresponds to the resolution of a 12-bit converter). Note that at 12 bits the linearity error has increased to ½ LSB.

For these reduced reference applications the offset voltage of the A/D has to be adjusted as the voltage value of the LSB changes from 20 mV to 5 mV and finally to 1.25 mV as we go from A) to B) to C). This offset adjustment is easily combined with the setting of the $V_{IN\ MIN}$ value at the $V_{IN(-)}$ pin.

Operation with reduced $V_{REF}/2$ voltages increases the requirement for good initial tolerance of the reference voltage (or requires an adjustment) and also the allowed changes in the $V_{REF}/2$ voltage over temperature are reduced.

An interesting application of this reduced reference feature is to directly digitize the forward voltage drop of a silicon diode as a simple digital temperature sensor.

A 10-Bit Application

This analog flexibility can be used to increase the resolution of the 8-bit converter to 10 bits. The heart of the idea is shown in *Figure 4*. The two extra bits are provided by the 2-bit external DAC (resistor string) and the analog switch, SW1.

Note that the $V_{REF}/2$ pin of the converter is supplied with 1/8 V_{REF} so each of the four spans which are encoded will be:

$$2\times\frac{1}{8}V_{REF}=\frac{1}{4}V_{REF}$$

In actual implementation of this circuit, the switch would be replaced by an analog multiplexer (such as the CD4066 quad bilateral switch) and a microprocessor would be programmed to do a binary search for the two MS bits. These two bits plus the 8 LSBs provided by the A/D give the 10-bit data. For a particular application, this basic idea can be simplified to a 1-bit ladder to cover a particular range of analog input voltages with increased resolution. Further, there may exit a *priori* knowledge by the CPU which could locate the analog signal to within the 1 or 2 MSBs without requiring a search algorithm.

A Microprocessor Controlled Voltage Comparator

In applications where set points (or "pick points") are set up by analog voltages, the A/D can be used as a comparator to determine whether an analog input is greater than or less than a reference DC value. This is accomplished by simply grounding the $V_{REF}/2$ pin (to provide maximum resolution) and applying the reference DC value to the $V_{IN(-)}$ input. Now with the analog signal applied to the $V_{IN(+)}$ input, an all zeros code will be output for $V_{IN(+)}$ less than the reference voltage and an all ones code for $V_{IN(+)}$ greater

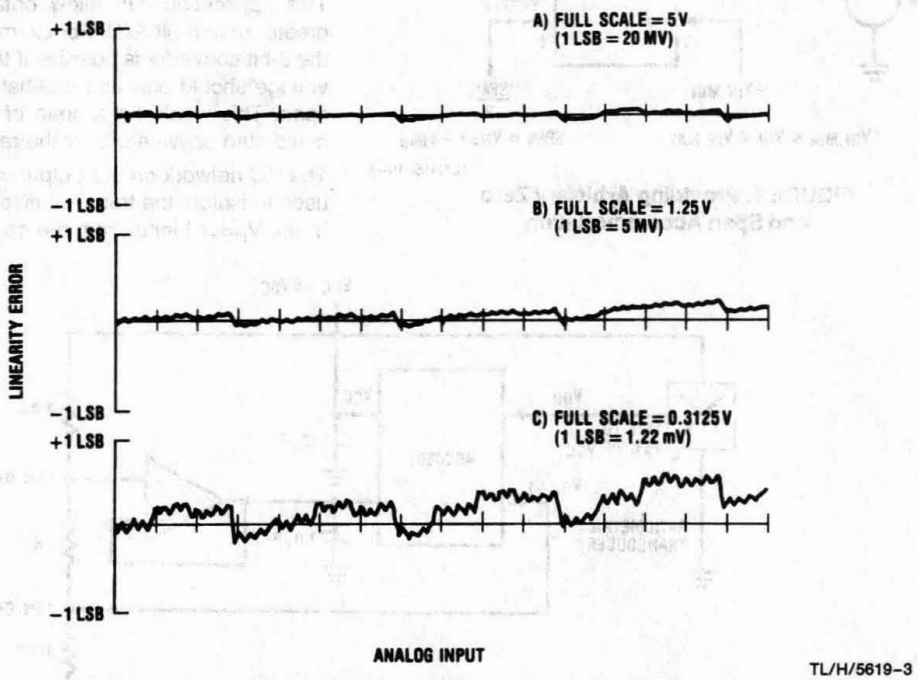

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FIGURE 3. Linearity Error for Reduced Analog Input Spans

than the reference voltage. This reduces the computational loading of the CPU. Further, using analog switches, a single A/D can encode some analog input channels in the "normal" way and can provide this comparator operation, under microprocessor control, for other analog input channels.

DACs Multiply and A/Ds Divide

Computation can be directly done with converter components to either increase the speed or reduce the loading on a CPU. It is rather well known that DACs multiply—and for this reason many are actually called "MDACs" to signify "multiplying DAC." An analog product voltage is provided as an output signal from a DAC for a hybrid pair of input signals—one is analog (the V_{REF} input) and the other is digital.

The A/D provides a digital quotient output for two analog input signals. The numerator or the dividend is the normal analog input voltage to the A/D and the denominator or the divisor is the V_{REF} input voltage.

High speed computation can be provided external to the CPU by either or both of these converter products. DACs are available which provide 4-quadrant multiplications (the MDACs and MICRO-DACs™), but A/Ds are usually limited to only one quadrant.

Combine Analog Self-Test with Your Digital Routines

A new innovation is the digital self-test and diagnostic routines which are being used in equipment. If an 8-bit A/D converter and an analog multiplexer are added, these testing routines can then check all power supply voltage levels and other set point values in the system. This is a major application area for the new generation converter products.

Control Temperature Coefficients with Converters

The performance of many systems can be improved if voltages within the system can be caused to change properly with changes in ambient temperature. This can be accomplished by making use of low cost 8-bit digital to analog converters (DACs) which are used to introduce a "dither" or small change about the normal operating values of DC power supplies or other voltages within the system. Now, a single measurement of the ambient temperature and one A/D converter with a MUX can be used by the microprocessor to establish proper voltage values for a given ambient temperature. This approach easily provides non-linear temperature compensation and generally reduces the cost and improves the performance of the complete system.

Save an Op Amp

In applications where an analog signal voltage which is to be converted may only range from, for example, $0V_{DC}$ to 500 mV_{DC}, an op amp with a closed-loop gain of 10 is required to allow making use of the full dynamic range ($0V_{DC}$ to $5V_{DC}$) of the A/D converter. An alternative circuit approach is shown in *Figure 5*. Here we, instead, attenuate the magnitude of the reference voltage by 10:1 and apply the 0 to 500 mV signal directly to the A/D converter. The $V_{IN(-)}$ input is now used for a V_{OS} adjust, and due to the "sampled-data" operation of the A/D there is essentially no V_{OS} drift with temperature changes.

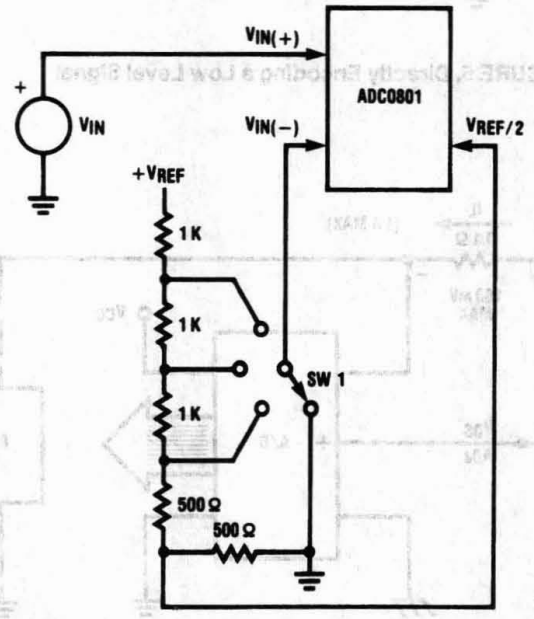

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FIGURE 4. 10-Bit A/D Using the 8-Bit ADC801

As shown in *Figure 5*, all zeros will be output by the A/D for an input voltage (at the $V_{IN(+)}$ input) of $0V_{DC}$ and all ones will be output by the A/D for a $500mV_{DC}$ input signal. Operation of the A/D in this high sensitivity mode can be useful in many low cost system applications.

Digitizing a Current Flow

In system applications there are many requirements to monitor the current drawn by a PC card or a high current load device. This typically is done by sampling the load current flow with a small valued resistor. Unfortunately, it is usually desired that this resistor be placed in series with the V_{CC} line. The problem is to remove the large common-mode DC voltage, amplify the differential signal, and then present the ground referenced voltage to an A/D converter.

All of these functions can be handled by the A/D using the circuit shown in *Figure 6*. Here we are making use of the differential input feature and the common-mode rejection of the A/D to directly encode the voltage drop across the load current sampling resistor. An offset voltage adjustment is provided and the $V_{REF}/2$ voltage is reduced to 50 mV to accommodate the input voltage span of 100 mV. If desired, a multiplexer can be used to allow switching the $V_{IN(-)}$ input among many loads.

Conclusions

At first glance it may appear that the A/D converters were mainly designed for an easy digital interface to the microprocessor. This is true, but the analog interface has also been given attention in the design and a very useful converter product has resulted from this combination of features.

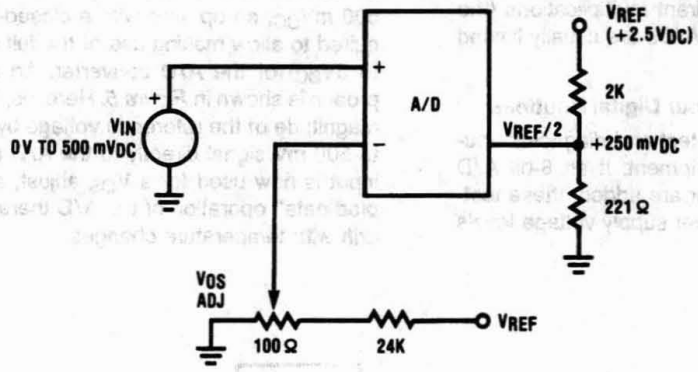

FIGURE 5. Directly Encoding a Low Level Signal

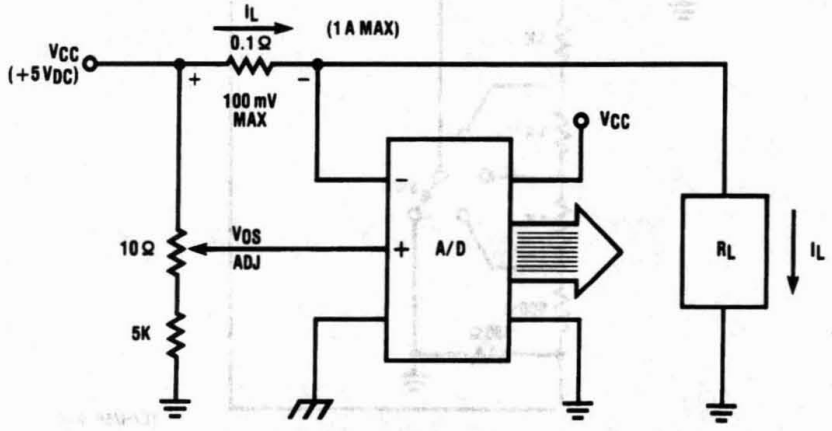

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FIGURE 6. Digitizing a Current Flow

An Introduction to the Sampling Theorem

National Semiconductor
Application Note 236

An Introduction to the Sampling Theorem

With rapid advancement in data acquistion technology (i.e. analog-to-digital and digital-to-analog converters) and the explosive introduction of micro-computers, selected complex linear and nonlinear functions currently implemented with analog circuitry are being alternately implemented with sample data systems.

Though more costly than their analog counterpart, these sampled data systems feature programmability. Additionally, many of the algorithms employed are a result of developments made in the area of signal processing and are in some cases capable of functions unrealizable by current analog techniques.

With increased usage a proportional demand has evolved to understand the theoretical basis required in interfacing these sampled data-systems to the analog world.

This article attempts to address the demand by presenting the concepts of aliasing and the sampling theorem in a manner, hopefully, easily understood by those making their first attempt at signal processing. Additionally discussed are some of the unobvious hardware effects that one might encounter when applying the sampled theorem.

With this . . . let us begin.

I. An Intuitive Development

The sampling theorem by C.E. Shannon in 1949 places restrictions on the frequency content of the time function signal, f(t), and can be simply stated as follows:

> In order to recover the signal function f(t) exactly, it is necessary to sample f(t) at a rate greater than twice its highest frequency component.

Practically speaking for example, to sample an analog signal having a maximum frequency of 2Kc requires sampling at greater than 4Kc to preserve and recover the waveform exactly.

The consequences of sampling a signal at a rate below its highest frequency component results in a phenomenon known as *aliasing*. This concept results in a frequency mistakenly taking on the identity of an entirely different frequency when recovered. In an attempt to clarify this, envision the ideal sampler of *Figure 1(a)*, with a sample period of T shown in (b), sampling the waveform f(t) as pictured in (c). The sampled data points of f'(t) are shown in (d) and can be defined as the sample set of the continuous function f(t). Note in *Figure 1(e)* that another frequency component, a'(t), can be found that has the same sample set of data points as f'(t) in (d). Because of this it is difficult to determine which frequency a'(t), is truly being observed. This effect is similar to that observed in western movies when watching the

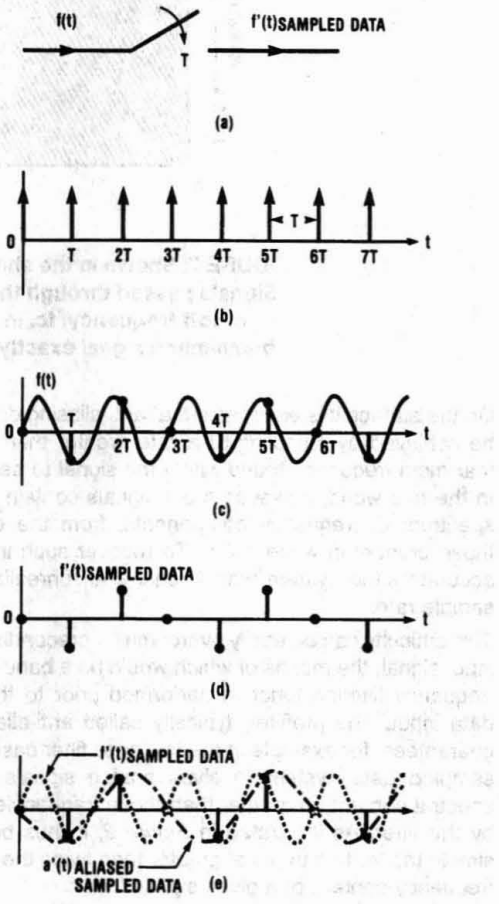

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FIGURE 1. When sampling, many signals may be found to have the same set of data points. These are called aliases of each other.

spoked wheels of a rapidly moving stagecoach rotate backwards at a slow rate. The effect is a result of each individual frame of film resembling a discrete strobed sampling operation flashing at a rate slightly faster than that of the rotating wheel. Each observed sample point or frame catches the spoked wheel slightly displaced from its previous position giving the effective appearance of a wheel rotating backwards. Again, aliasing is evidenced and in this example it becomes difficult to determine which is the true rotational frequency being observed.

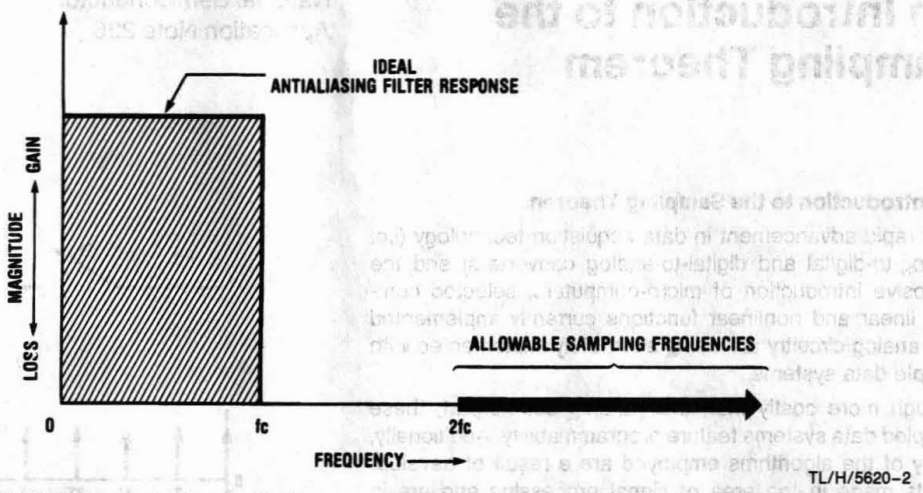

FIGURE 2. Shown in the shaded area is an ideal, low pass, anti-aliasing filter response. Signals passed through the filter are bandlimited to frequencies no greater than the cutoff frequency, fc. In accordance with the sampling theorem, to recover the bandlimited signal exactly the sampling rate must be chosen to be greater than 2fc.

On the surface it is easily said that anti-aliasing designs can be achieved by sampling at a rate greater than twice the maximum frequency found within the signal to be sampled. In the real world, however, most signals contain the entire spectrum of frequency components; from the desired to those present in white noise. To recover such information accurately the system would require an unrealizably high sample rate.

This difficulty can be easily overcome by preconditioning the input signal, the means of which would be a band-limiting or frequency filtering function performed prior to the sample data input. The prefilter, typically called anti-aliasing filter guarantees, for example in the low pass filter case, that the sampled data system receives analog signals having a spectral content no greater than those frequencies allowed by the filter. As illustrated in *Figure 2*, it thus becomes a simple matter to sample at greater than twice the maximum frequency content of a given signal.

A parallel analog of band-limiting can be made to the world of perception when considering the spectrum of white light. It can be realized that the study of violet light wavelengths generated from a white light source would be vastly simplified if initial band-limiting were performed through the use of a prism or white light filter.

II. The Sampling Theorem

To solidify some of the intuitive thoughts presented in the previous section, the sampling theorem will be presented applying the rigor of mathematics supported by an illustrative proof. This should hopefully leave the reader with a comfortable understanding of the sampling theorem.

Theorem: If the Fourier transform $F(\omega)$ of a signal function $f(t)$ is zero for all frequencies above $|\omega| \geq \omega_c$, then $f(t)$ can be uniquely determined from its sampled values

$$f_n = f(nT) \tag{1}$$

These values are a sequence of equidistant sample points spaced $\frac{1}{2fc} = \frac{Tc}{2} = T$ apart. $f(t)$ is thus given by

$$f(t) = \sum_{n=-\infty}^{\infty} f(nT) \frac{\sin \omega_c (t - nT)}{\omega_c (t - nT)} \tag{2}$$

Proof: Using the inverse Fourier transform formula:

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega) \epsilon^{j\omega t} \, d\omega \tag{3}$$

the band limited function, $f(t)$, takes the form, *Figure 3a*,

$$f(t) = \frac{1}{2\pi} \int_{-\omega_c}^{\omega_c} F(\omega) \epsilon^{j\omega t} \, d\omega \tag{4}$$

$f_n = f\left(n \frac{\pi}{\omega_c}\right)$ is then given as

$$f_n = \frac{1}{2\pi} \int_{-\omega_c}^{\omega_c} F(\omega) \epsilon^{j\omega \frac{n\pi}{\omega_c}} \, d\omega \tag{5}$$

See *Figure 3c* and *e*.

Expressing $F(\omega)$ as a Fourier series in the interval $-\omega_c \leq \omega \leq \omega_c$ we have

$$F(\omega) = \sum_{n=-\infty}^{\infty} C_n \epsilon^{-j\omega \frac{n\pi}{\omega_c}} \tag{6}$$

Where,

$$C_n = \frac{1}{2\omega_c}\int_{-\omega_c}^{\omega_c} F(\omega)\epsilon^{j\omega\frac{n\pi}{\omega_c}}\,d\omega \tag{7}$$

Further manipulating eq. (7)

$$C_n = \frac{2\pi}{2\omega_c}\frac{1}{2\pi}\int_{-\omega_c}^{\omega_c} F(\omega)\epsilon^{j\omega\frac{n\pi}{\omega_c}}\,d\omega \tag{8}$$

C_n can be written as

$$C_n = \frac{\pi}{\omega_c} f_n \tag{9}$$

Substituting eq. (9) into eq. (6) gives the periodic Fourier Transform

$$F_P(\omega) = \sum_{n=-\infty}^{\infty} \frac{\pi}{\omega_c} f_n \epsilon^{-j\omega\frac{n\pi}{\omega c}} \tag{10}$$

of *Figure 3f*. Using Poisson's sum formula[1] $F(\omega)$ can be stated more clearly as

$$F(\omega) = \sum_{n=-\infty}^{\infty} F(\omega - 2_n\omega_C) \tag{11}$$

Interestingly for the interval $-\omega_C \le \omega \le \omega_C$ the periodic function $F_p(\omega)$ and *Figure 3f*. equals $F(\omega)$ and *Figure 3b*. respectively. Analogously if $F_p(\omega)$ were multiplied by a rectangular pulse defined,

$$H(\omega) = 1 \qquad -\omega_C \le \omega \le \omega \tag{12}$$

and

$$H(\omega) = 0 \qquad |\omega| \ge \omega_C \tag{13}$$

then as pictured in *Figures 4b, d*, and *f*,

$$F(\omega) = H(\omega) \bullet F_P(\omega) = H(\omega) \sum_{n=-\infty}^{\infty} \frac{\pi}{\omega_C} f_n \epsilon^{-j\omega\frac{n\pi}{\omega_c}} \tag{14}$$

Solving for f(t) the inverse Fourier transform eq (3) is applied to eq (14)

$$f(t) = \frac{1}{2\pi}\int_{-\omega_c}^{\omega_c} F(\omega)\epsilon^{j\omega t}\,d\omega \tag{3}$$

$$= \frac{1}{2\pi}\int_{-\omega_c}^{\omega_c}\left[H(\omega)\sum_{n=-\infty}^{\infty}\frac{\pi}{\omega_c}f_n\epsilon^{-j\omega\frac{n\pi}{\omega c}}\right]\epsilon^{j\omega t}\,d\omega$$

$$= \sum_{n=-\infty}^{\infty} fn\frac{1}{2\omega_c}\int_{-\omega_c}^{\omega_c}\epsilon^{j\omega\left(t-\frac{n\pi}{\omega}\right)}\,d\omega$$

[1]Poisson's sum formula

$$\frac{1}{T}\sum_{n=-\infty}^{\infty} F(\omega - n\omega_s) = \sum_{n=-\infty}^{\infty} f(nT)\epsilon^{-j\omega nT}$$

where $T = \frac{1}{f_s}$ and f_s is the sampling frequency

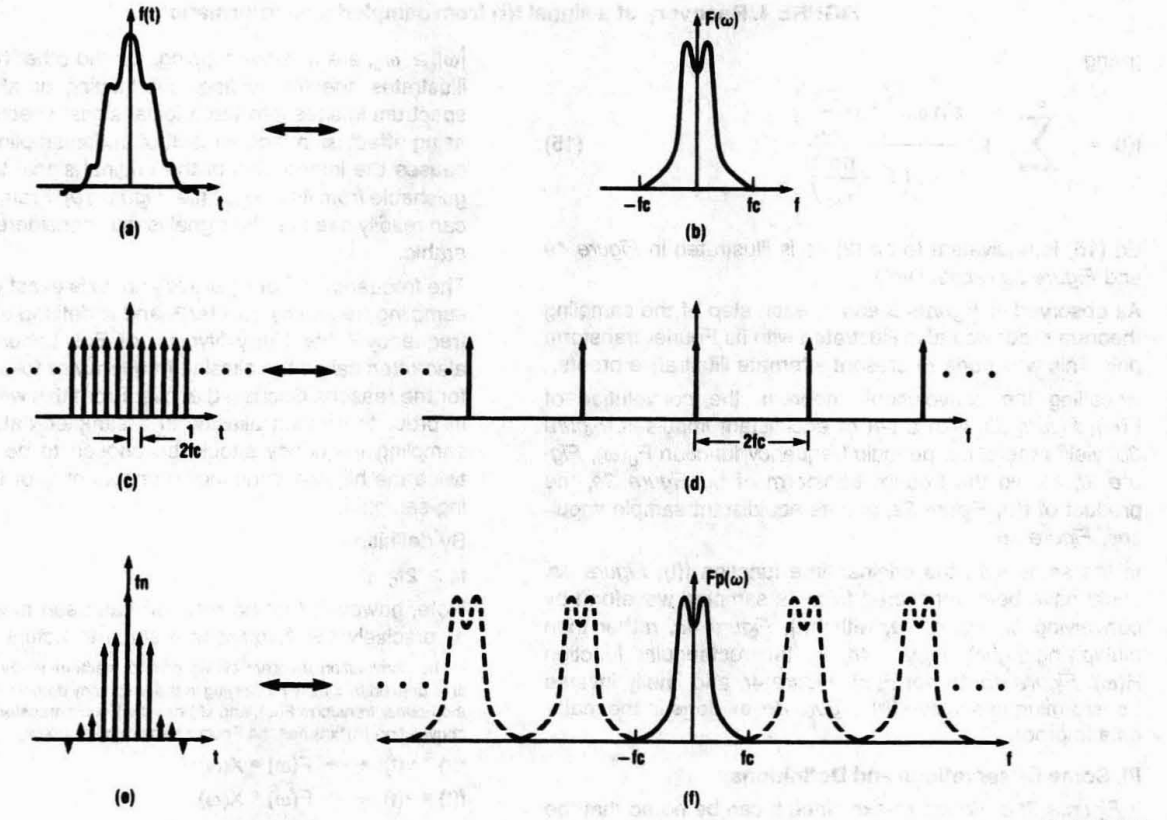

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FIGURE 3. Fourier transform of a sampled signal.

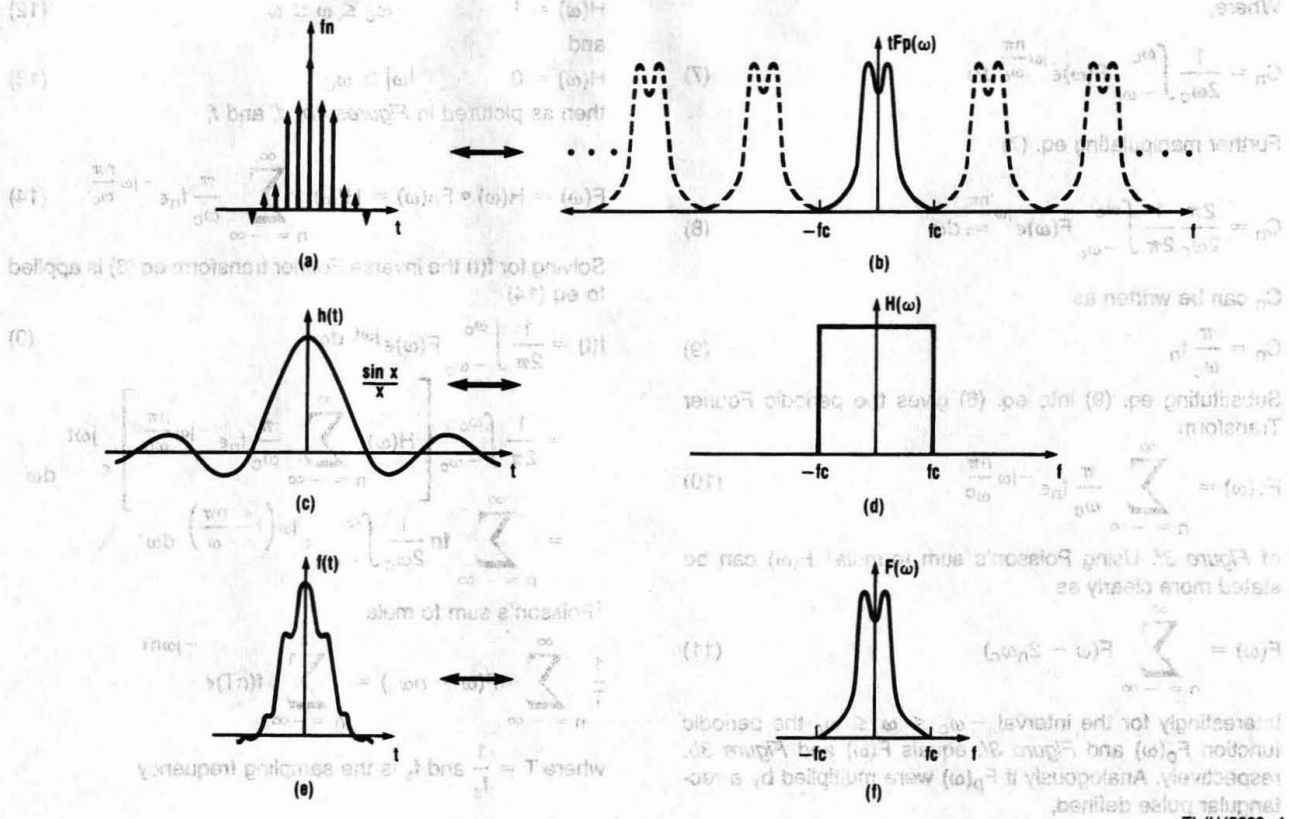

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FIGURE 4. Recovery of a signal f(t) from sampled data information.

giving

$$f(t) = \sum_{n=-\infty}^{\infty} f_n \frac{\sin \omega_c \left(t - \frac{n\pi}{\omega_c}\right)}{\omega_c \left(t - \frac{n\pi}{\omega_c}\right)} \qquad (15)$$

Eq (15) is equivalent to eq (2) as is illustrated in *Figure 4e* and *Figure 3a* respectively.

As observed in *Figures 3* and *4*, each step of the sampling theorem proof was also illustrated with its Fourier transform pair. This was done to present alternate illustrative proofs.

Recalling the convolution[2] theorem, the convolution of $F(\omega)$, *Figure 3b*, with a set of equidistant impulses, *Figure 3d*, yields the same periodic frequency function $F_p(\omega)$, *Figure 3f*, as did the Fourier transform of f_n, *Figure 3e*, the product of f(t), *Figure 3a*, and its equidistant sample impulses, *Figure 3c*.

In the same light the original time function f(t), *Figure 4e*, could have been recovered from its sampled waveform by convolving f_n, *Figure 4a*, with h(t), *Figure 4c*, rather than multiplying $F_p(\omega)$, *Figure 4b*, by the rectangular function $H(\omega)$, *Figure 4d*, to get $F(\omega)$, *Figure 4f*, and finally inverse transforming to achieve f(t), *Figure 4e*, as done in the mathematic proof.

III. Some Observations and Definitions

If *Figures 3f* or *4b* are re-examined it can be noted that the original spectrum $F_p(\omega)$, $|\omega| \leq \omega_c$, and its images $F_p(\omega)$, $|\omega| \geq \omega_c$, are non-overlapping. On the other hand *Figure 5* illustrates spectral folding, overlapping or aliasing of the spectrum images into the original signal spectrum. This aliasing effect is, in fact, a result of undersampling and further causes the information of the original signal to be indistinguishable from its images (i.e. *Figure 1e*). From *Figure 6* one can readily see that the signal is thus considered non-recoverable.

The frequency |fc| of *Figure 3f* and *4b* is exactly one half the sampling frequency, $fc = fs/2$, and is defined as the Nyquist frequency (after Harry Nyquist of Bell Laboratories). It is also often called the aliasing frequency or folding frequency for the reasons discussed above. From this we can say that in order to prevent aliasing in a sampled-data system the sampling frequency should be chosen to be greater than twice the highest frequency component f_c of the signal being sampled.

By definition

$$f_s \geq 2f_c \qquad (16)$$

Note, however, that no mention has been made to sample at precisely the Nyquist rate since in actual practice it is

[2] The convolution theorem allows one to mathematically convolve in the time domain by simply multiplying in the frequency domain. That is, if f(t) has the Fourier transform $F(\omega)$, and x(t) has the Fourier transform $X(\omega)$, then the convolution $f(t)*x(t)$ has the Fourier transform $F(\omega)\bullet X(\omega)$.

$$f(t) * x(t) \longleftrightarrow F(\omega) \bullet X(\omega)$$

$$f(t) \bullet x(t) \longleftrightarrow F(\omega) * X(\omega)$$

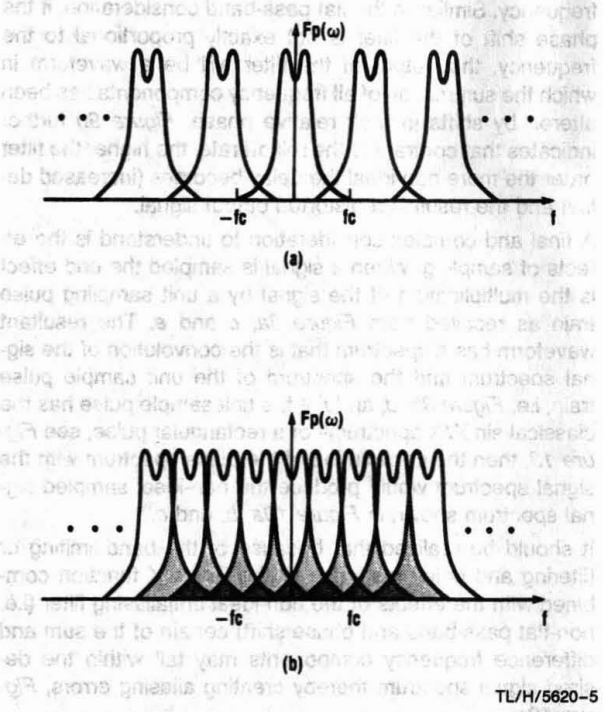

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FIGURE 5. Spectral folding or aliasing caused by:
(a) under sampling
(b) exaggerated under sampling.

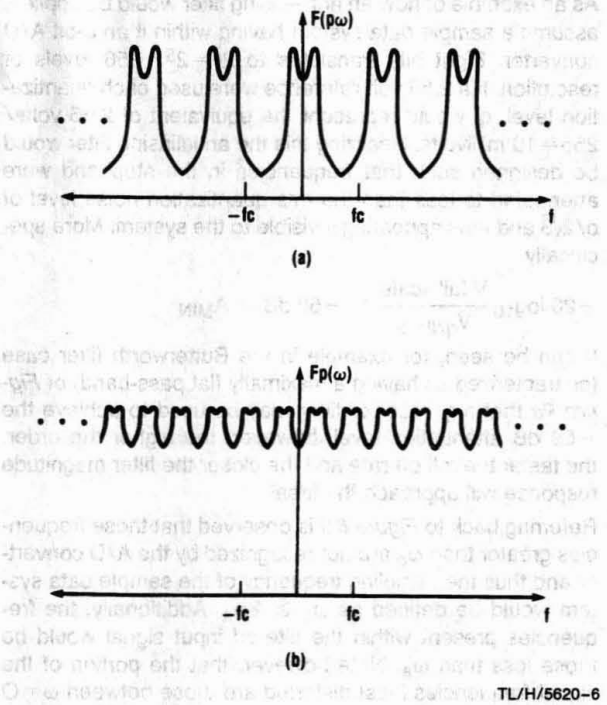

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FIGURE 6. Aliased spectral envelope (a) and (b) of Figures 5a and 5b respectively.

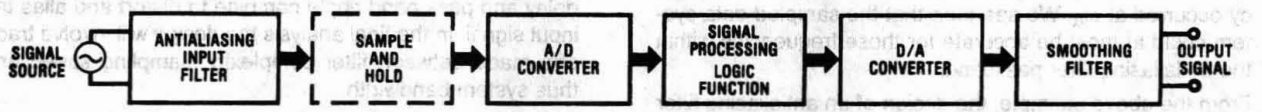

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FIGURE 7. Generalized single channel sample data system.

impossible to sample at $f_s = 2f_c$ unless one can guarantee there are absolutely no signal components above f_c. This can only be achieved by filtering the signal prior to sampling with a filter having infinite rolloff . . . a physical impossibility, see *Figure 2*.

IV. The Sampling Theorem and Its Hardware Implications

Though there are numerous sophisticated techniques of implementation, it is appropriate to re-emphasize that the intent of this article is to give the first time user a basic and fundamental approach toward the design of a sampled-data system. The method with which to achieve this goal will be to introduce a few of the common perils encountered when implementing such a system. We begin by considering the generalized block diagram of *Figure 7*.

As shown in *Figure 7*, prior to any signal processing manipulation the analog input signal must be preconditioned to prevent aliasing and thereafter digitized to logic signals usable by the logic function block. The antialiasing and digitizing functions are performed by an input filter and analog-to-digital converter respectively. Once digitized the signal can then be altered or processed and upon completion, reconstructed back to a continuous analog signal via a digital-to-analog converter followed by a smoothing filter.

To this point no mention has been made concerning the sample and hold circuit block depicted in *Figure 7*. In general the analog-to-digital converter can operate as a stand alone unit. In many high speed operations however, the converter speed is insufficient and thus requires the assistance of a sample and hold circuit. This will be discussed in detail further in the article.

A. The Antialiasing Input Filter

As indicated earlier in the text, the antialiasing filter should band-limit the input signal's spectrum to frequencies no greater than the Nyquist frequency. In the real world however, filters are non-ideal and have typical attenuation or band-limiting and phase characteristics as shown in *Figure 8*.[3] It must also be realized that true band-limiting of a specific frequency spectrum is not possible. In the sample data system band-limiting is achieved by attenuating those frequencies greater than the Nyquist frequency to a level undetectable or invisible to the system analog-to-digital (A/D) converter. This level would typically be less than the rms quantization[4] noise level defined by the specific converter being used.

[3]In order not to disrupt the flow of the discussion a list of filter terms has been presented in Appendix A.

[4]For an explanation of quantization refer to section IV. B. of this article.

As an example of how an antialiasing filter would be applied, assume a sample data system having within it an 8-bit A/D converter. Eight bits translates to $2^n = 2^8 = 256$ levels of resolution. If a 2.56 volt reference were used each quantization level, q, would represent the equivalent of 2.56 volts/256 = 10 millivolts. Realizing this the antialiasing filter would be designed such that frequencies in the stopband were attenuated to less than the rms quantization noise level of $q/2\sqrt{3}$ and thus appearing invisible to the system. More specifically

$$-20 \log_{10} \frac{V \text{ full scale}}{V_{q/2\sqrt{3}}} \cong -59 \text{ dB} = A_{MIN}$$

It can be seen, for example in the Butterworth filter case (characterized as having a maximally flat pass-band) of *Figure 9a* that any order of filter may be used to achieve the −59 dB attenuation level, however, the higher the order, the faster the roll off rate and the closer the filter magnitude response will approach the ideal.

Referring back to *Figure 8* it is observed that those frequencies greater than ω_a are not recognized by the A/D converter and thus the sampling frequency of the sample data system would be defined as $\omega_s \geq 2\omega_a$. Additionally, the frequencies present within the filtered input signal would be those less than ω_a. Note however, that the portion of the signal frequencies least distorted are those between $\omega = O$ and ω_p and those within the transition band are distorted to a substantial degree, though it was originally desired to limit the signal to frequencies less than the cutoff ω_p, because of the non-ideal frequency response the true Nyquist frequency occurred at ω_a. We see then that the sampled-data system could at most be accurate for those frequencies within the antialiasing filter passband.

From the above example, the design of an antialiasing filter appears to be quite straight forward. Recall however, that all waveforms are composed of the sums and differences of various frequency components and as a result, if the response of the filter passband were not flat for the desired signal frequency spectrum, the recovered signal would be an inaccurate summation of all frequency components altered by their relative attenuations in the pass-band.

Additionally the antialiasing filter design should not neglect the effects of delay. As illustrated in *Figure 8* and *9b*, delay time corresponds to a specific phase shift at a particular frequency. Similar to the flat pass-band consideration, if the phase shift of the filter is not exactly proportional to the frequency, the output of the filter will be a waveform in which the summation of all frequency components has been altered by shifts in their relative phase. *Figure 9b* further indicates that contrary to the roll off rate, the higher the filter order the more non-ideal the delay becomes (increased delay) and the result is a distorted output signal.

A final and complex consideration to understand is the effects of sampling. When a signal is sampled the end effect is the multiplication of the signal by a unit sampling pulse train as recalled from *Figure 3a*, *c* and *e*. The resultant waveform has a spectrum that is the convolution of the signal spectrum and the spectrum of the unit sample pulse train, i.e. *Figure 3b*, *d*, and *f*. If the unit sample pulse has the classical sin X/X spectrum[5] of a rectangular pulse, see *Figure 13*, then the convolution of the pulse spectrum with the signal spectrum would produce the non-ideal sampled signal spectrum shown in *Figure 10a*, *b*, and *c*.

It should be realized that because of the band-limiting or filtering and delay response of the Sin X/X function combined with the effects of the non-ideal antialiasing filter (i.e. non-flat pass-band and phase shift) certain of the sum and difference frequency components may fall within the desired signal spectrum thereby creating aliasing errors, *Figure 10c*.

When designing antialiasing filters it will be found that the closer the filter response approaches the ideal the more complex the filter becomes. Along with this an increase in delay and pass-band ripple combine to distort and alias the input signal. In the final analysis the design will involve trade offs made between filter complexity, sampling speed and thus system bandwidth.

B. The Analog-to-Digital Converter

Following the antialiasing filter is the A/D converter which performs the operations of quantizing and coding the input signal in some finite amount of time. *Figure 11* shows the quantization process of converting a continuous analog input signal into a set of discrete output levels. A quantization, q, is thus defined as the smallest step used in the digital

[5]This will be explained more clearly in Section IV. of this article.

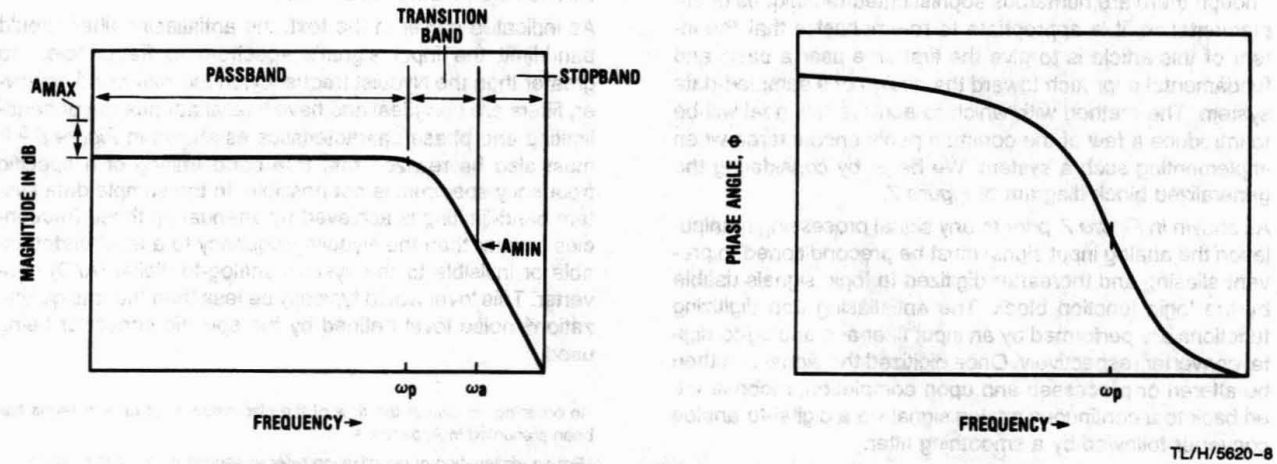

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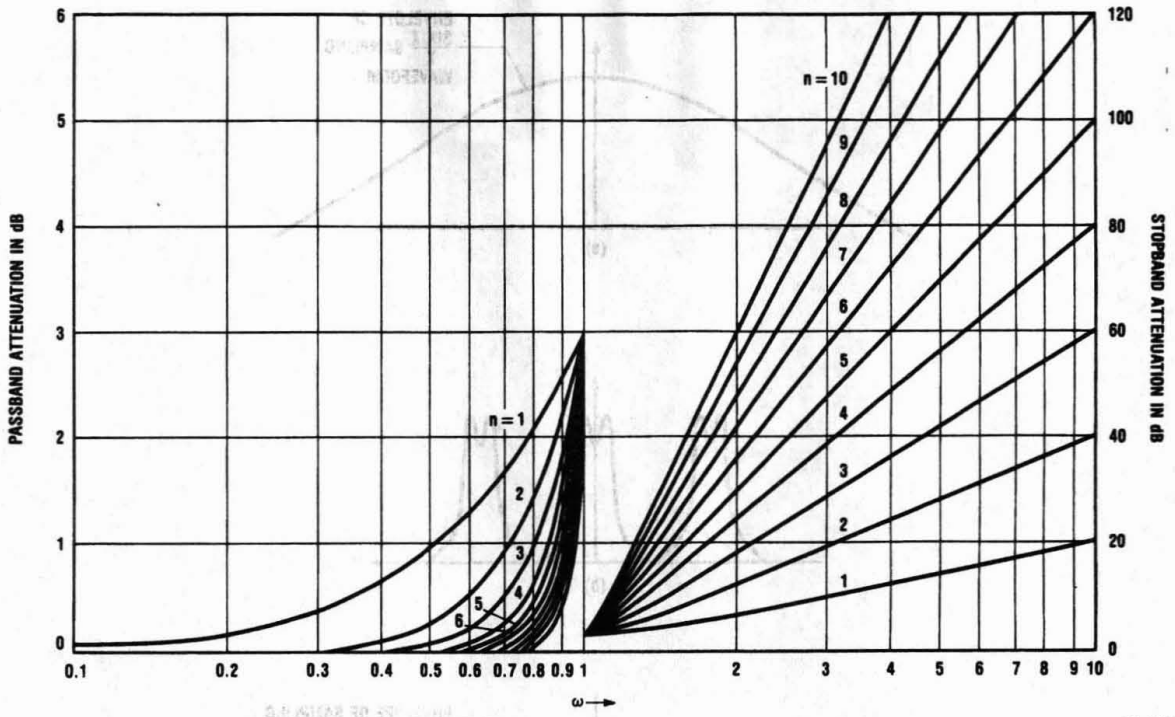
FIGURE 8. Typical filter magnitude and phase versus frequency response.



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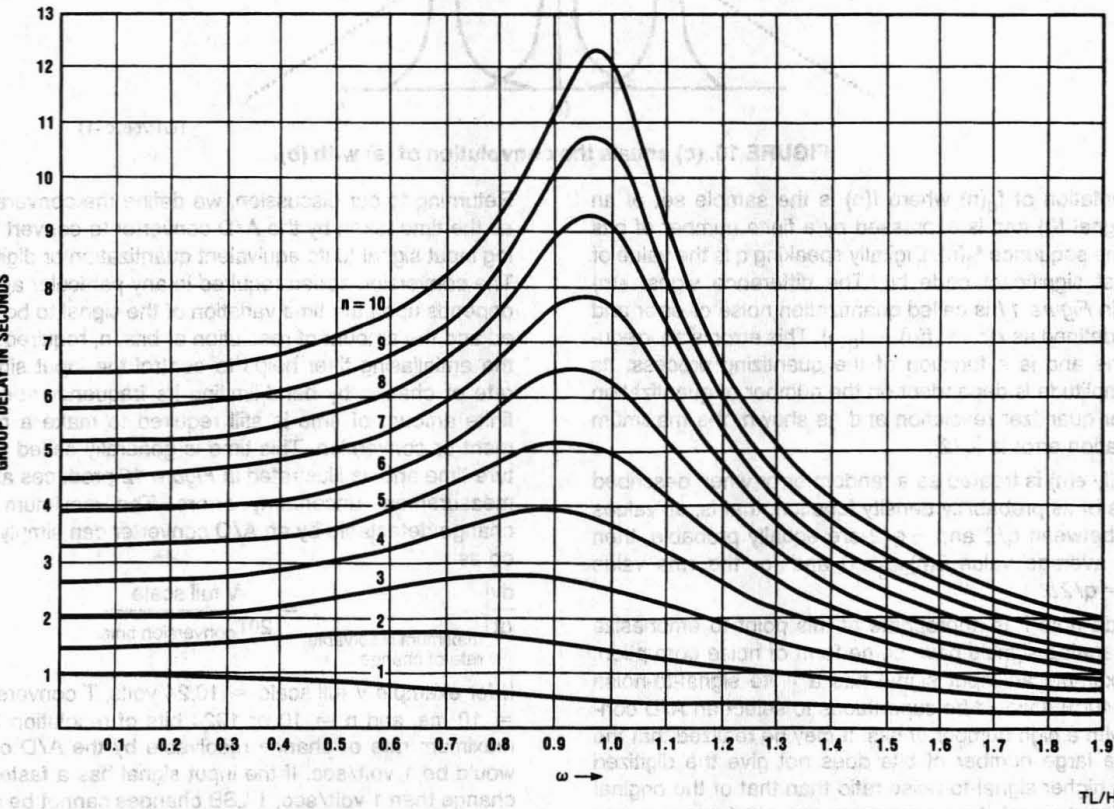
a) Attenuation characteristics of a normalized Butterworth filter as a function of degree n.



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b) Group delay performances of normalized Butterworth lowpass filters as a function of degree n.

FIGURE 9

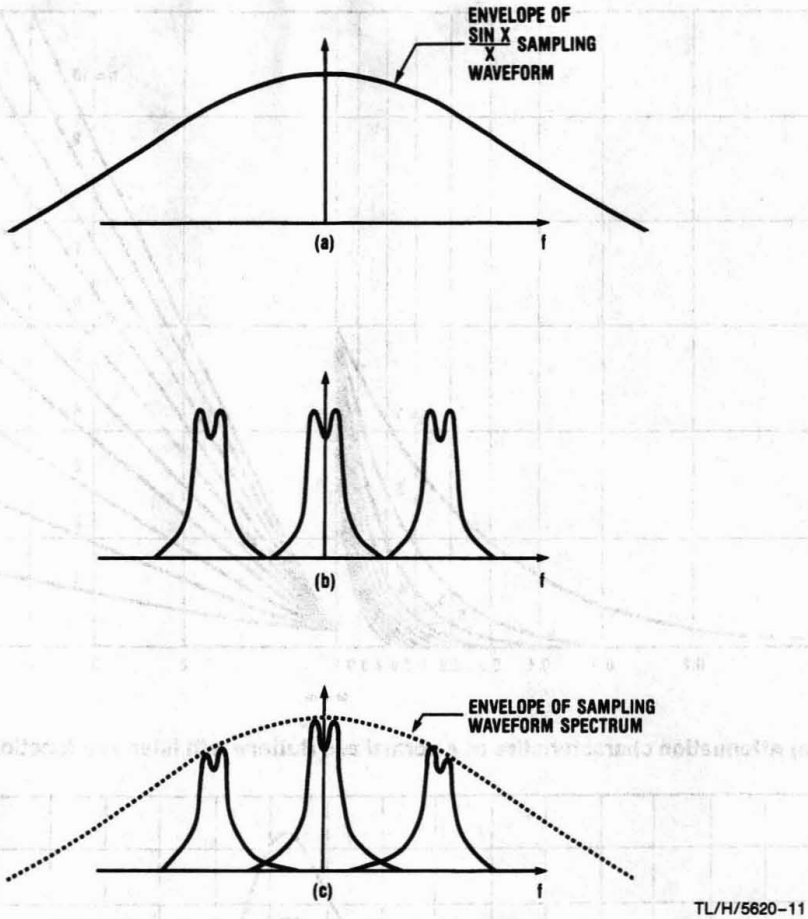

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FIGURE 10. (c) equals the convolution of (a) with (b).

representation of $f_q(n)$ where f(n) is the sample set of an input signal f(t) and is expressed by a finite number of bits giving the sequence $f_q(n)$. Digitally speaking q is the value of the least significant code bit. The difference signal $\epsilon(n)$ shown in *Figure 11* is called quantization noise or error and can be defined as $\epsilon(n) = f(n) - f_q(n)$. This error is an irreducible one and is a function of the quantizing process. Its error amplitude is dependent on the number of quantization levels or quantizer resolution and as shown, the maximum quantization error is $|q/2|$.

Generally $\epsilon(n)$ is treated as a random error when described in terms of its probability density function, that is, all values of $\epsilon(n)$ between $q/2$ and $-q/2$ are equally probable, then for the average value $\epsilon(n)_{avg} = 0$ and for the rms value $\epsilon(n)_{rms} = q/2\sqrt{3}$.

As a side note it is appropriate at this point to emphasize that all analog signals have some form of noise corruption. If for example an input signal has a finite signal-to-noise ratio of 40dB it would be superfluous to select an A/D converter with a high number of bits. It may be realized that the use of a large number of bits does not give the digitized signal a higher signal-to-noise ratio than that of the original analog input signal. As a supportive argument one may say that though the quantization steps q are very small with respect to the peak input signal the lower order bits of the A/D converter merely provide a more accurate representation of the noise inherent in the analog input signal.

Returning to our discussion, we define the conversion time as the time taken by the A/D converter to convert the analog input signal to its equivalent quantization or digital code. The conversion speed required in any particular application depends upon the time variation of the signal to be converted and the amount of resolution or bits, n, required. Though the antialiasing filter helps to control the input signal time rate of change by band-limiting its frequency spectrum, a finite amount of time is still required to make a measurement or conversion. This time is generally called the aperture time and as illustrated in *Figure 12* produces amplitude measurement uncertainty errors. The maximum rate of change detectable by an A/D converter can simply be stated as

$$\left.\frac{dv}{dt}\right|_{\substack{\text{maximum resolvable}\\ \text{rate of change}}} = \frac{V \text{ full scale}}{2^n T_{\text{conversion time}}} \qquad (17)$$

If for example V full scale = 10.24 volts, T conversion time = 10 ms, and n = 10 or 1024 bits of resolution then the maximum rate of change resolvable by the A/D converter would be 1 volt/sec. If the input signal has a faster rate of change than 1 volt/sec, 1 LSB changes cannot be resolved within the sampling period.

In many instances a sample-and-hold circuit may be used to reduce the amplitude uncertainty error by measuring the input signal with a smaller aperture time than the conversion time aperture of the A/D converter. In this case the

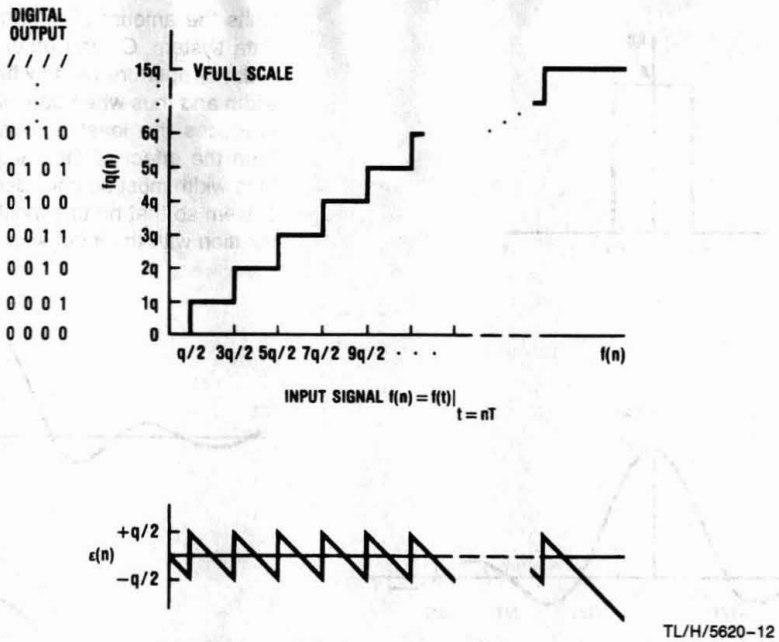
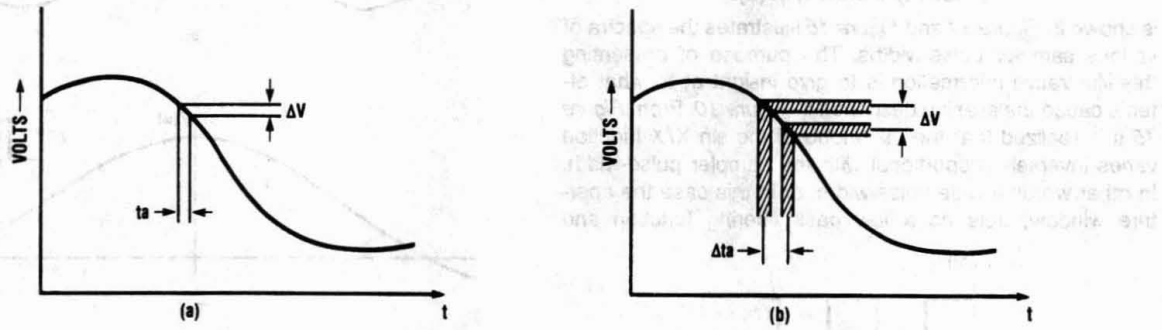


FIGURE 11. Quantization error.



ΔV: AMPLITUDE UNCERTAINTY ERROR
ta: APERTURE TIME
Δta: APERTURE TIME UNCERTAINTY

FIGURE 12. Amplitude uncertainty as a function of (a) a nonvarying aperture and (b) aperture time uncertainty.

maximum rate of change resolvable by the sample-and-hold would be

$$\left.\frac{dv}{dt}\right|_{\substack{\text{maximum resolvable}\\ \text{rate of change}}} = \frac{\text{V full scale}}{\text{t aperture}} \qquad (18)$$

Note also that the actual calculated rate of change may be limited by the slew rate specification fo the sample-and-hold in the track mode. Additionally it is very important to clarify that this does not imply violating the sampling theorem in lieu of the increased ability to more accurately sample signals having a fast time rate of change.

An ideal sample-and-hold effectively takes a sample in zero time and with perfect accuracy holds the value of the sample indefinitely. This type of sampler is also known as a zero order hold circuit and its effect on a sample data system warrants some discussion.

It is appropriate to recall the earlier discussion that the spectrum of a sampled signal is one in which the resultant spectrum is the product obtain by convolving the input signal spectrum with the sin X/X spectrum of the sampling waveform. *Figure 13* illustrates the frequency spectrum plotted from the Fourier transform

$$F(\omega) = AT \frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \qquad (19)$$

of a rectangular pulse. The sin X/X form occurs frequently in modern communication theory and is commonly called the sampling function.

The magnitude and phase of a typical zero order hold sampler spectrum

$$H(\omega) = A\left[\tau \frac{\sin \omega\tau}{\omega\tau} + j\frac{1}{\omega}(\cos \omega - 1)\right] \qquad (20)$$

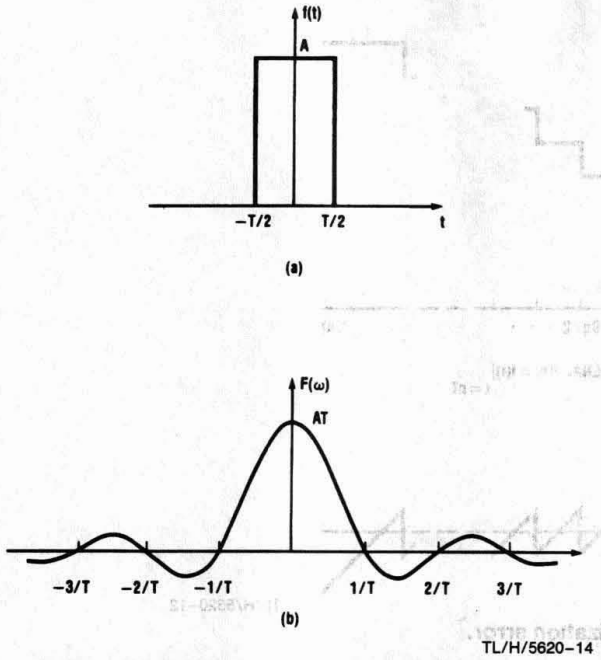


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FIGURE 13. The Fourier transform of the rectangular pulse (a) is shown in (b).

is shown in *Figure 14* and *Figure 15* illustrates the spectra of various sampler pulse-widths. The purpose of presenting this illustrative information is to give insight at to what effects cause the aliasing described in *Figure 10*. From *Figure 15* it is realized that the main lobe of the sin X/X function varies inversely proportional with the sampler pulse-width. In other words a wide pulse-width, or in this case the aperture window, acts as a low pass filtering function and limits the amount of information resolvable by the sample data system. On the other hand a narrow sampler pulse-width or aperture window has a broader main lobe or bandwidth and thus when convolved with the analog input signal produces the least amount of distortion. Understandably then the effect of the sampler's spectral phase and main lobe width must be considered when developing a sampling system so that no unexpected aliasing occurs from its convolution with the input signal spectrum.

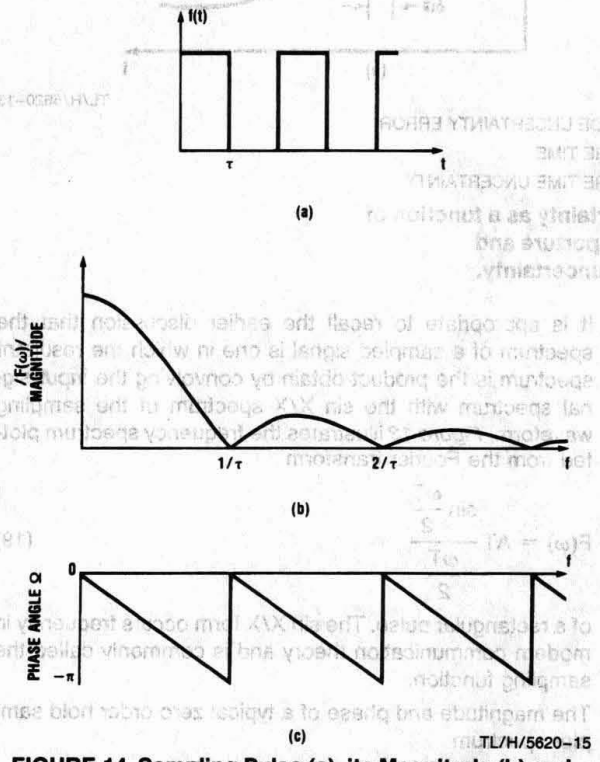

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FIGURE 14. Sampling Pulse (a), its Magnitude (b) and Phase Response (c).

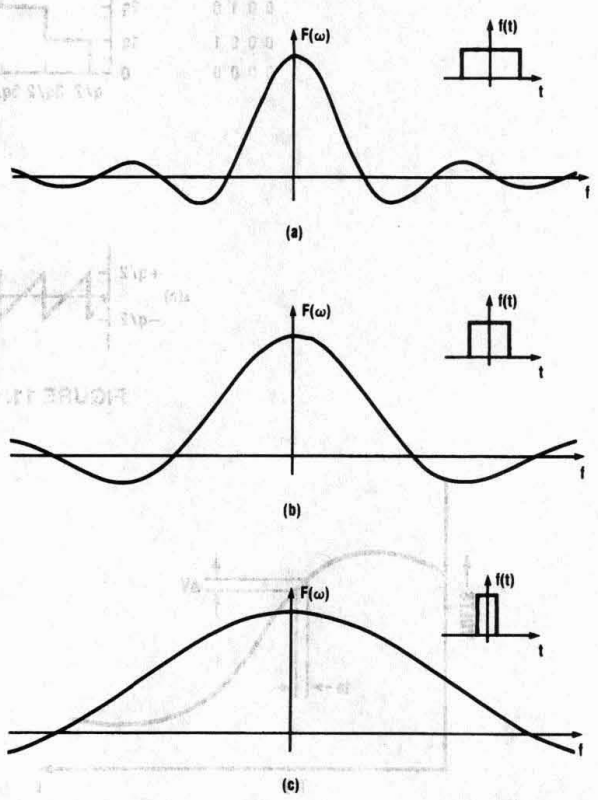

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FIGURE 15. Pulse width and how it effects the sin X/X envelop spectrum (normalized amplitudes).

C. The Digital-to-Analog Converter and Smoothing Filter

After a signal has been digitally conditioned by the signal processing unit of *Figure 7*, a D/A converter is used to convert the sampled binary information back in to an analog signal. The conversion is called a zero order hold type where each output sample level is a function of its binary weight value and is held until the next sample arrives, see *Figure 16*. As a result of the D/A converter step function response it is apparent that a large amount of undesirable high frequency energy is present. To eliminate this the D/A converter is usually followed by a smoothing filter, having a cutoff frequency no greater than half the sampling frequency. As its name suggests the filter output produces a smoothed version of the D/A converter output which in fact is a convolved function. More simply said, the spectrum of the resulting signal is the product of a step function sin X/X spectrum and the band-limited analog filter spectrum. Analogous to the input sampling problem, the smoothed output may have aliasing effects resulting from the phase and attenuation relations of the signal recovery system (defined as the D/A converter and smoothing filter combination).

As a final note, the attenuation due to the D/A converter sin X/X spectrum shape may in some cases be compensated for in the signal processing unit by pre-processing using a digital filter with an inverse response X/sin X prior to D/A conversion. This allows an overall flat magnitude signal response to be smoothed by the final filter.

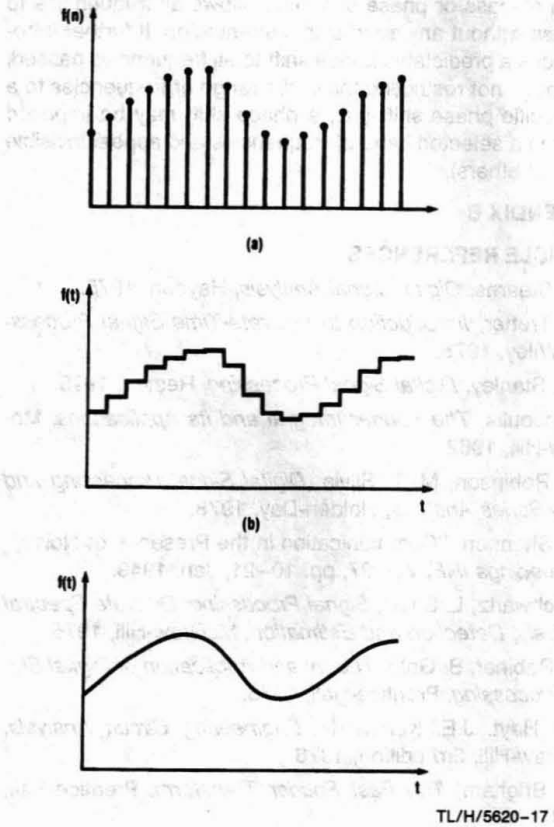

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FIGURE 16. (a) Processed signal data points (b) output of D/A converter (c) output of smoothing filter.

V. A Final Note

This article began by presenting an intuitive development of the sampling theorem supported by a mathematical and illustrative proof. Following the theoretical development were a few of the unobvious and troublesome results that develop when trying to put the sampling theorem into practice. The purpose of presenting these thought provoking perils was to perhaps give the beginning designer some insight or guidelines for consideration when developing a sample data system's interface.

VI. Acknowledgements

The author wishes to thank James Moyer and Barry Siegel for their encouragement and the time they allocated for the writing of this article.

APPENDIX A

Basic Filter Concepts

A filter is a network used for separating signal waves on the basis of their frequency and is usually composed of passive, reactive and active elements such as resistors, capacitors, inductors, and amplifiers, or combinations thereof.

There are basically five types of filters used to pass or reject such signals and they are defined as follows:

1. A low-pass filter passes a band of frequencies called the *passband*, ranging from zero frequency or DC to a certain *cutoff frequency*, ω_C*, and in addition has a maximum attenuation or ripple level of A_{MAX} within the passband. See *Figure 1*.

*Recall that the radian frequency $\omega = 2\pi f$.

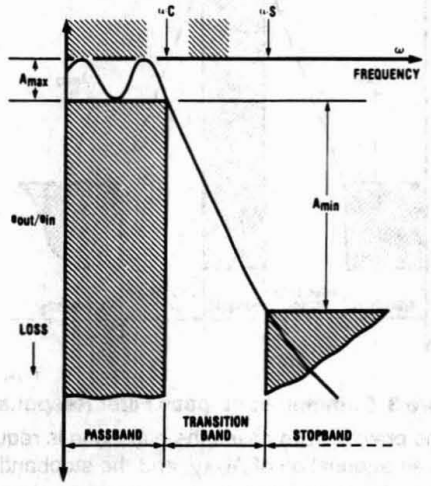

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FIGURE 1. Common Low Pass Filter Response

Frequencies beyond the ω_C may have an attenuation greater than A_{MAX} but beyond a specific frequency ω_S defined as the *stopband frequency*, a minimum attenuation of A_{MIN} must prevail. The band of frequencies higher than ω_S and maintaining attenuation greater than or equal to A_{MIN} is called the *stopband*. The transition region or *transition band* is that band of frequencies between ω_C and ω_S.

2. A high-pass filter allows frequencies above the passband frequency, ω_C, to pass and rejects frequencies below this point. A_{MAX} must be maintained in the passband and frequencies equal to and below the stopband frequency, ω_S, must have a minimum attenuation of A_{MIN}. See *Figure 2*.

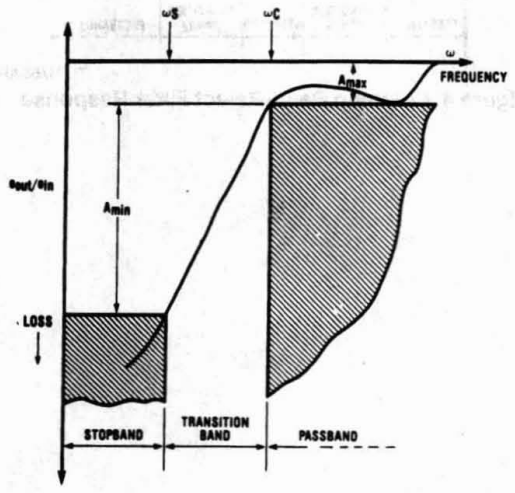

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FIGURE 2. Common High Pass Filter Response

3. A bandpass filter performs the function of passing a specific band of frequencies while rejecting those frequencies above and below ω_{c2} and lower, ω_{c1} cutoff frequency limits. See *Figure 3.*

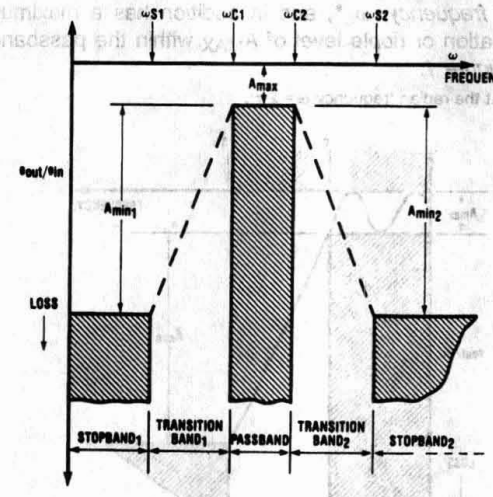

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Figure 3. Common Band-pass Filter Response

As in the previous two cases the passband is required to sustain an attenuation of A_{MAX}, and the stopband of frequencies above and below ω_{s2} and ω_{s2} respectively, must have a minimum attenuation of A_{MIN}.

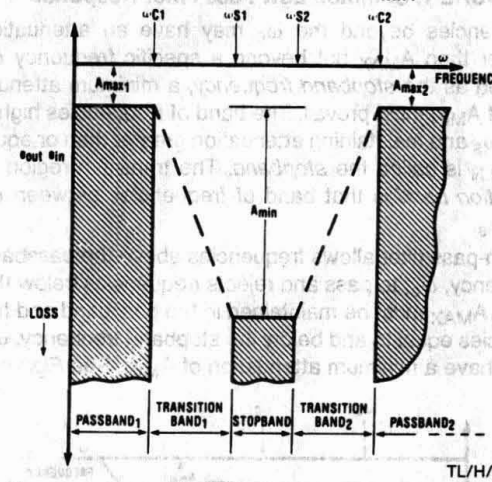

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Figure 4. Common Band-Reject Filter Response

4. A band-reject filter or notch filter allows all but a specific band of frequencies to pass. As shown in Figure 4, those frequencies between ω_{s1} and ω_{s2} are filtered out and those frequencies above and below ω_{c2} and ω_{c1} respectively are passed. The attenuation requirements of the stopband A_{MIN} and passband A_{MAX} must still hold.
5. An all-pass or phase shift filter allows all frequencies to pass without any appreciable attenuation. It further introduces a predictable phase shift to all frequencies passed, though not restricting the entire range of frequencies to a specific phase shift (i.e., a phase shift may be imposed upon a selected band of frequencies and appear invisible to all others).

APPENDIX B

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CONVOLUTION: Digital Signal Processing

National Semiconductor
Application Note 237

Introduction

As digital signal processing continues to emerge as a major discipline in the field of electrical engineering, an even greater demand has evolved to understand the basic theoretical concepts involved in the development of varied and diverse signal processing systems. The most fundamental concepts employed are (not necessarily listed in the order of importance) the sampling theorem[1], Fourier transforms [2] [3], convolution, covariance, etc.

The intent of this article will be to address the concept of convolution and to present it in an introductory manner hopefully easily understood by those entering the field of digital signal processing.

It may be appropriate to note that this article is Part II (Part I is titled "An Introduction to the Sampling Theorem") of a series of articles to be written that deal with the fundamental concepts of digital signal processing.

Let us proceed . . . .

Part II Convolution

Perhaps the easiest way to understand the concept of convolution would be an approach that initially clarifies a subject relating to the frequency spectrum of linear networks.

Determining the frequency spectrum or frequency transfer function of a linear network provides one with the knowledge of how a network will respond to or alter an input signal. Conventional methods used to determine this entail the use of spectrum analyzers which use either sweep generators or variable-frequency oscillators to impress upon a network all possible frequencies of equal amplitude and equal phase.

The response of a network to all frequencies can thus be determined. Any amplitude and phase variations at the output of a network are due to the network itself and as a result define the frequency transfer function.

Another means of obtaining this same information would be to apply an impulse function to the input of a network and then analyze the network impulse-response for its spectual-frequency content. Comparison of the network-frequency transfer function obtained by the two techniques would yield the same information.

This is found to be easily understood (without elaborate experimentation) if the implications of the impulse function are initially clarified.

If the pulse of *Figure 1a* is examined, using the Fourier integral, its frequency spectrum is found to be

$$F(\omega) = \int_{-\infty}^{\infty} f(t)\, \epsilon^{-j\omega t}\, dt \qquad (1)$$

$$= \int_{-T/2}^{T/2} A\, \epsilon^{-j\omega t}\, dt \qquad (2)$$

$$F(\omega) = AT \left[\frac{\sin\left(\frac{\omega T}{2}\right)}{\left(\frac{\omega T}{2}\right)} \right]$$

as shown in *Figure 1b*.

Decreasing the pulse width while increasing the pulse height to allow the area under the pulse to remain constant, *Figure 1c*, shows from eq(1) and eq(2) the bandwidth or spectral-frequency content of the pulse to have increased, *Figure 1d*.

Further altering the pulse to that of *Figure 1e* provides for an even broader bandwidth, *Figure 1f*. If the pulse is finally altered to the limit, i.e., the pulsewidth being infinitely narrow and its amplitude adjusted to still maintain an area of unity under the pulse, it is found in 1g and 1h the unit impulse produces a constant, or "flat" spectrum equal to 1 at all frequencies. Note that if $AT = 1$ (unit area), we get, by definition, the unit impulse function in time.

Since this time function contains equal frequency components at all frequencies, applying it or a good approximation of it to the input of a linear network would be the equivalent of simultaneously impressing upon the system an array of oscillators inclusive of all possible frequencies, all of equal amplitude and phase. The frequencies could thus be determined from this one input time function. Again, variations in amplitude and phase at the system output would be due to the system itself.

Empirically speaking the frequency spectrum or the network frequency transfer function can thus be determined by applying an impulse at the input and using, for example, a spectrum analyzer at the network output. At this point, it is important to emphasize that the above discussion holds true for only linear networks or systems since the superposition principle (The response to a sum of excitations is equal to the sum of the responses to the excitations acting separately), and its analytical techniques break down in non-linear networks.

Since an impulse response provides information of a network frequency spectrum or transfer function, it additionally provides a means of determining the network response to any other time function input. This will become evident in the following development.

If the input to a network, *Figure 2*, having a transfer function $H(\omega)$ is an impulse function $\delta(t)$ at $t = 0$, its Fourier transform using eq(1) can be found to be $F(\omega) = 1$.

The output of the network $G(\omega)$ is therefore

$$G(\omega) = H(\omega) \bullet F(\omega)$$

$$G(\omega) = H(\omega)$$

The inverse transform is

$$g(t) = h(t)$$

and h(T) is defined as the impulse response of the network as a result of being excited by a unit impulse time function at $t = 0$.

Extending this train of thought further, the response of a network to any input excitation can be determined using the same technique.

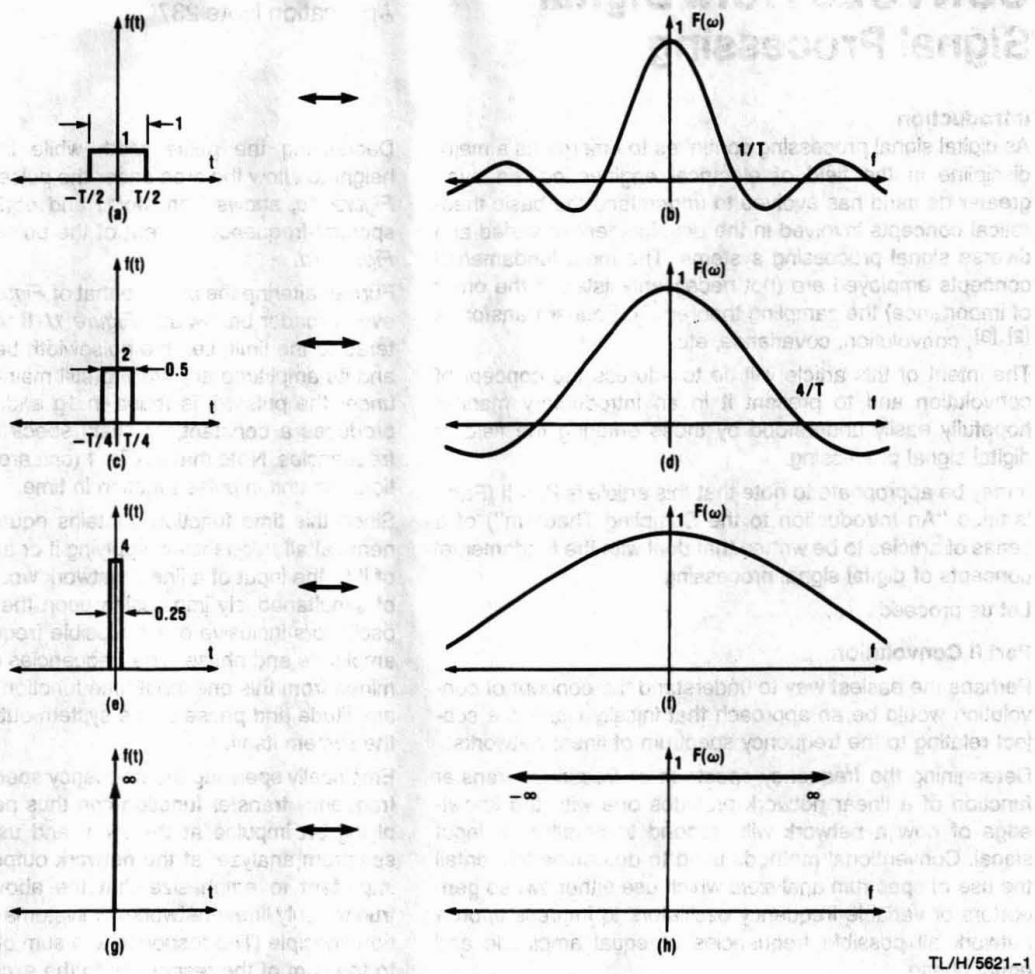

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FIGURE 1. Development of a unit impulse;
(a) (c) (e) (g) its time function
(b) (d) (f) (h) its frequency spectrum

Hence, finding the Fourier transform of the input excitation, $F(\omega)$, multiplying it by the transfer function transform $H(\omega)$ (or the transform of time domain network impulse response) and inverse transforming to find the output g(t) as a function of time.

By definition the convolution integral[1]

$$f(t) * h(t) = \int_0^t f(\tau)\, h(t-\tau)\, d\tau \qquad (3)$$

(where * denotes the convolution operation, h(t) denotes the impulse response function described above and both f(t) and h(t) are zero for $t<0$. Note that the meaning of the variables t and τ will be clarified, later in the article) makes the same claim but in the realm of the time domain alone.

If this is true then the Fourier transform of the convolution integral eq(3) should have the following equivalence −

$$F\left[\int_0^t f(\tau)\, h(t-\tau)\, d\tau\right] = F(\omega) \bullet H(\omega) \qquad (4)$$

As a proof using eq(1) let

$$F\left[f(t) * h(t)\right] = \int_0^\infty \epsilon^{-j\omega t}\left[\int_0^t f(\tau)\, h(t-\tau)\, d\tau\right] dt \qquad (5)$$

Defined by the shifted step function

$$u(t-\tau) = 1 \text{ for } \tau \le t \qquad (6a)$$

and

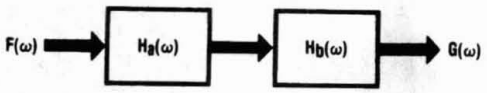
$$u(t-\tau) = 0 \text{ for } \tau > t \qquad (6b)$$

Footnote:

1. It is important to note that the convolution integral is commutative. This implies the reversability of the f(t) and h(t) terms in the definition.

$$g(t) = \int_{-\infty}^{\infty} f(\tau)\, h(t-\tau)\, d\tau = F^{-1}[F(\omega) \bullet H(\omega)]$$

$$\int_{-\infty}^{\infty} f(t-\tau)\, h(\tau)\, d\tau = F^{-1}[H(\omega) \bullet F(\omega)]$$



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$$H(\omega) = H_a(\omega) \bullet H_b(\omega)$$

$$\frac{G(\omega)}{F(\omega)} = H(\omega)$$

FIGURE 2. Block diagram of a network transfer function

the following identity can be made

$$\int_0^t f(\tau)\, h(t-\tau)\, d\tau = \int_0^\infty f(\tau)\, h(t-\tau)\, u(t-\tau)\, d\tau \quad (7)$$

Rewriting eq(5) as

$$F[f(t) * h(t)] = \int_0^\infty \epsilon^{-j\omega t} \int_0^\infty f(\tau)\, h(t-\tau)\, u(t-\tau)\, d\tau dt \quad (8)$$

and letting $x = t - \tau$ so that

$$\epsilon^{-j\omega t} = \epsilon^{-j\omega(x+\tau)} \quad (9)$$

eq(8) finally becomes

$$F[f(t) * h(t)] = \int_0^\infty \int_0^\infty f(\tau)\, h(x)\, u(x)\, \epsilon^{-j\omega t} \epsilon^{-j\omega x}\, d\tau dx$$

$$= \int_0^\infty h(x)\, u(x) * \epsilon^{-j\omega x}\, dx \int_0^\infty f(\tau)\, \epsilon^{-j\omega\tau}\, d\tau$$

$$F[f(t) * h(t)] = H(\omega) \bullet F(\omega) \quad (10)$$

which is the equivalent of eq(4).

In essence the above proof describes one of the most important and powerful tools used in signal processing .... the convolution theorm. In words,

Convolution Theorem:

The convolution theorem allows one to mathematically convolve in the time domain by simply multiplying in the frequency domain. That is, if f(t) has the Fourier transform F(ω) and x(t) has the Fourier transform X(ω), then the convolution f(t) * x(t) has the Fourier transform F(ω) • X(ω).

For the time convolution

$$f(t) * x(t) \longleftrightarrow F(\omega) \bullet X(\omega) \quad (11)$$

and the dual frequency convolution is

$$f(t) \bullet x(t) \longleftrightarrow F(\omega) * X(\omega) \quad (12)$$

Convolutions are fundamental to time series sampled data analysis. First of all, as described earlier all linear networks can be completely characterized by their impulse response functions and furthermore the response to any input is given by its (the input function) convolution with the network impulse response function. Digit filters being linear systems accomplish the filtering task using convolutions. A network or filter transfer function for example can be represented by its inpulse response in the form of a Fourier series. A filtered input excitation response can then be found by convolving the input time function with the network Fourier series or impulse response. With the aid of a high speed computer the same result could be obtained by storing the FFT (Fast Fourier Transform) of the network impulse response into memory, performing an FFT on the sampled continuous input excitation function, multiplying the two transforms and finally computing the inverse FFT of the product.

Moving averages and smoothing operations can further be characterized as lowpass filtering functions and can additionally be implemented using convolution. The above are just a few of the many operations convolution performs and the remainder of this discussion will focus on how convolution is realized.

To start with, an illustrative analysis will be performed assuming continuous functions followed by one performed in discrete form similar to that realized in computer aided sampled-data systems techniques.

As an example, if it were desired to determine the response of a network to the excitation pulse f(t) shown in *Figure 3a*, knowing the network impulse $h_\delta(t)$, *Figure 3b*, the impulse response of an RC network, would allow one to determine the output g(t) using the convolution integral, eq(3).

The convolution of f(t) and $h_\delta(t)$

$$f(t) = 10[u(t) - (u(t-T_o)] \quad (13)$$

$$h_\delta(t) = \epsilon^{-at}$$

could be obtained by first substituting the dummy variable $t - \tau$ for t in $h_\delta(t)$ so that

$$h_\delta(t-\tau) = \epsilon^{-a(t-\tau)} \quad (15)$$

By definition $g(t) = f(t) * h_\delta(t)$ thus becomes

$$\int_0^t f(\tau) h_\delta(t-\tau) d\tau = \int_0^t 10[u(t) - u(t-T_o)]\epsilon^{-a(t-\tau)}\, d\tau \quad (16)$$

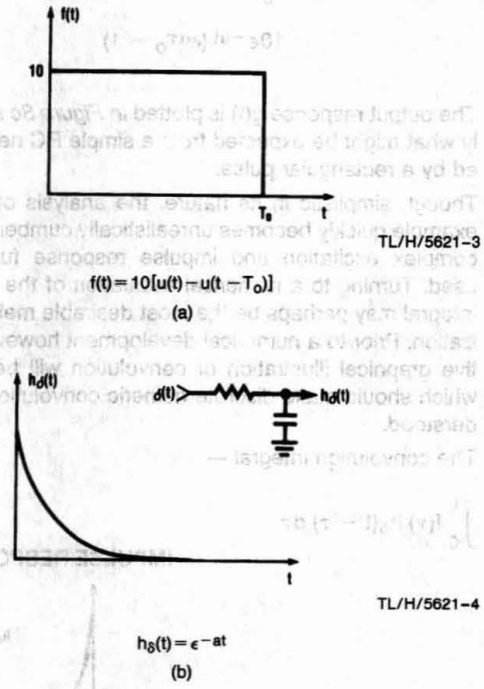

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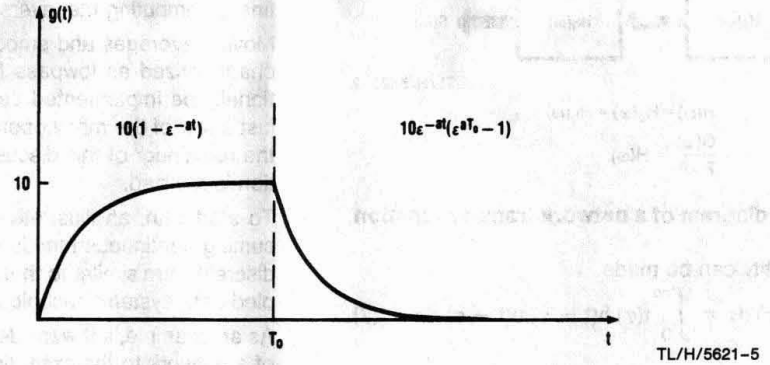
FIGURE 3. (a) rectangular pulse excitation (b) impulse response of a single RC network



(c)

FIGURE 3. (c) output or convolution of the network (b) excited by (a)

Since the piecewise nature of the excitation makes it convenient to calculate the response in corresponding pieces the output is found to be

$0 < t \leq T_o$

$$g(t) = f(t)\, h_\delta(t) = \int_0^t 10\epsilon^{-a(t-\tau)}\, d\tau$$

$$= 10(1 - \epsilon^{-at}) \qquad (17)$$

$t \geq To$

$$g(t) = f(t)^* h_\delta(t) = \int_0^{To} 10\epsilon^{-a(t-\tau)}\, d\tau$$

$$= 10\epsilon^{-at}(\epsilon^{a\tau_o} - 1) \qquad (18)$$

The output response g(t) is plotted in *Figure 3c* and is clearly what might be expected from a simple RC network excited by a rectangular pulse.

Though simplistic in its nature, the analysis of the above example quickly becomes unrealistically cumbersome when complex excitation and impulse response functions are used. Turning to a numerical evaluation of the convolution integral may perhaps be the most desirable method of realization. Prior to a numerical development however, an intuitive graphical illustration of convolution will be presented which should make discrete numeric convolution easily understood.

The convolution integral —

$$\int_0^t f(\tau)\, h_\delta(t - \tau)\, d\tau$$

defines the graphical procedure. Using the same example depicted in *Figure 3* the excitation and impulse response functions replaced with the dummy variable is defined as past data or historical information to be used in a convolution process. Thus

$$f(\tau) = 10[u(\tau) - u(\tau - T_o)] \qquad (19)$$

and

$$h_\delta(\tau) = \epsilon^{-a\tau} \qquad (20)$$

are shown in *Figure 4a* and *b*. *Figure 4c*, $h_\delta(-\tau)$, represents the impulse response folded over [mirror image of $h_\delta(\tau)$] about the ordinate and *Figure 4d*, $h_\delta(t-\tau)$, is simply the function $h_\delta(-\tau)$ time shifted by the quantity t.

Evaluation of the convolution integral is performed by multiplying $f(\tau)$ by each incremental shift in $h_\delta(t-\tau)$. It is understood in *Figure 4e* that a negative value of $-t$ produces no output. For $t > O$ however as the present time t varies, the impulse response $h_\delta(t-\tau)$ scans the excitation function $f(\tau)$, always producing a weighted sum of past inputs and weighing most heavily those values of $f(\tau)$ closet to the present. As seen in *Figures 4e* through *4n*, the response or output of the network at anytime t is the integral of the functions or calculated shaded area under the curves. In terms of the superposition principle the filter response g(t) may be interpreted as being the weighted superposition of past input $f(\tau)$ values weighted or multiplied by $h_\delta(t-\tau)$.

An extension of the continuous convolution to its numerical discrete form is made and shown in *Figure 5*. Again the excitation and impulse response of *Figure 3* are used and are further represented as two finite duration sequences f(n)

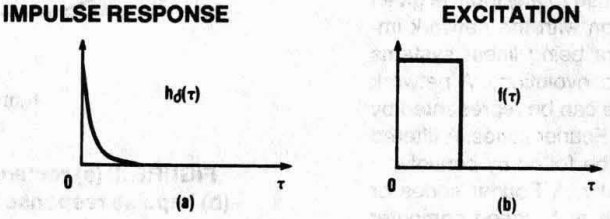


FIGURE 4. a) $h_\delta(\tau)$: network impulse response
b) $f(\tau)$: excitation function

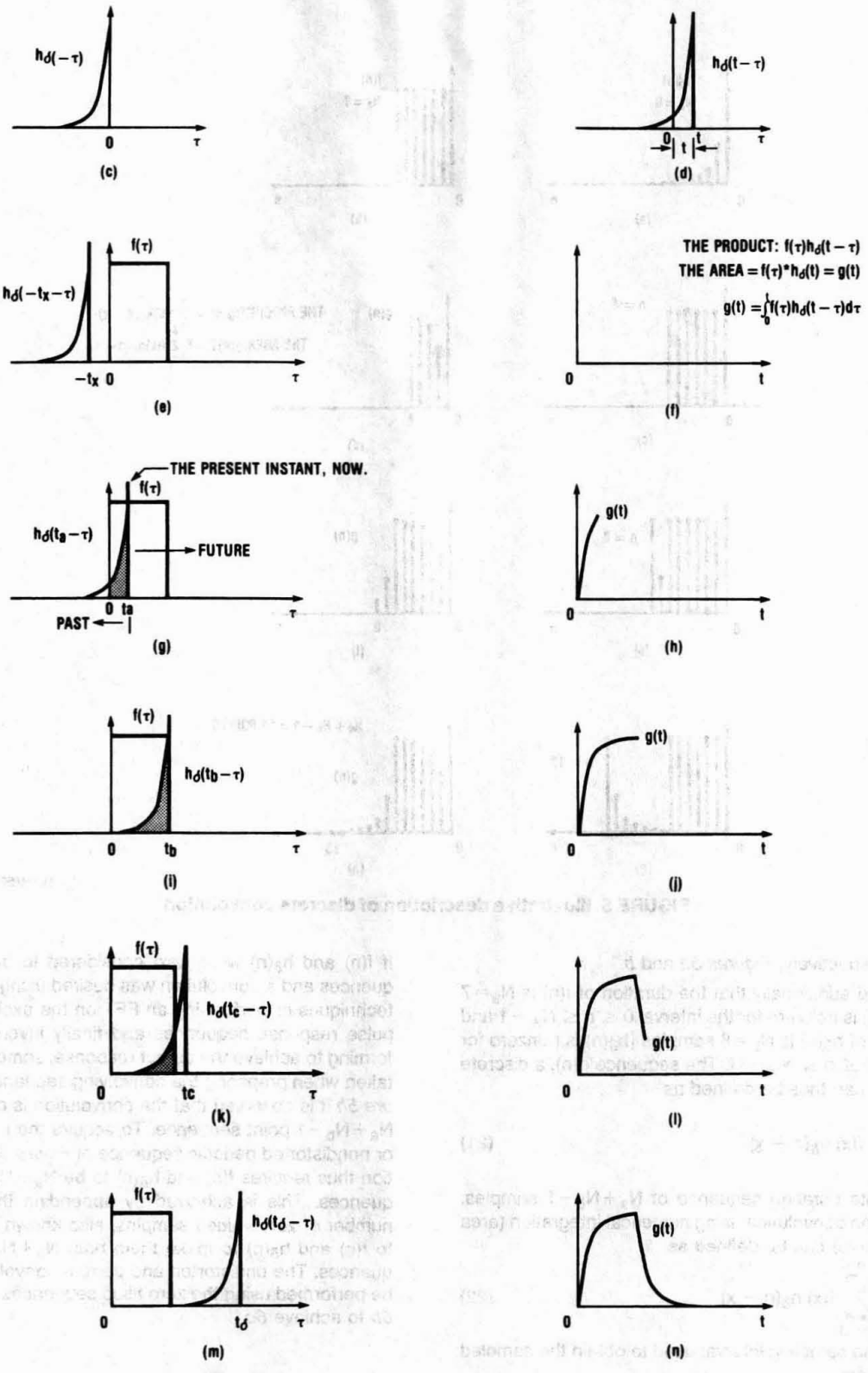


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FIGURE 4. cont'd c) $h_\delta(-\tau)$: $h_\delta(\tau)$ folded about the ordinate
d) $h_\delta(t-\tau)$: $h_\delta(r)$ folded and shifted
e) through n) the output response g(t) of the network whose impulse response $h_\delta(\tau)$ is excited by a function $f(\tau)$.
Or the convolution, $f(\tau)*h_\delta(t)$, of f(t) with $h_\delta(t)$.

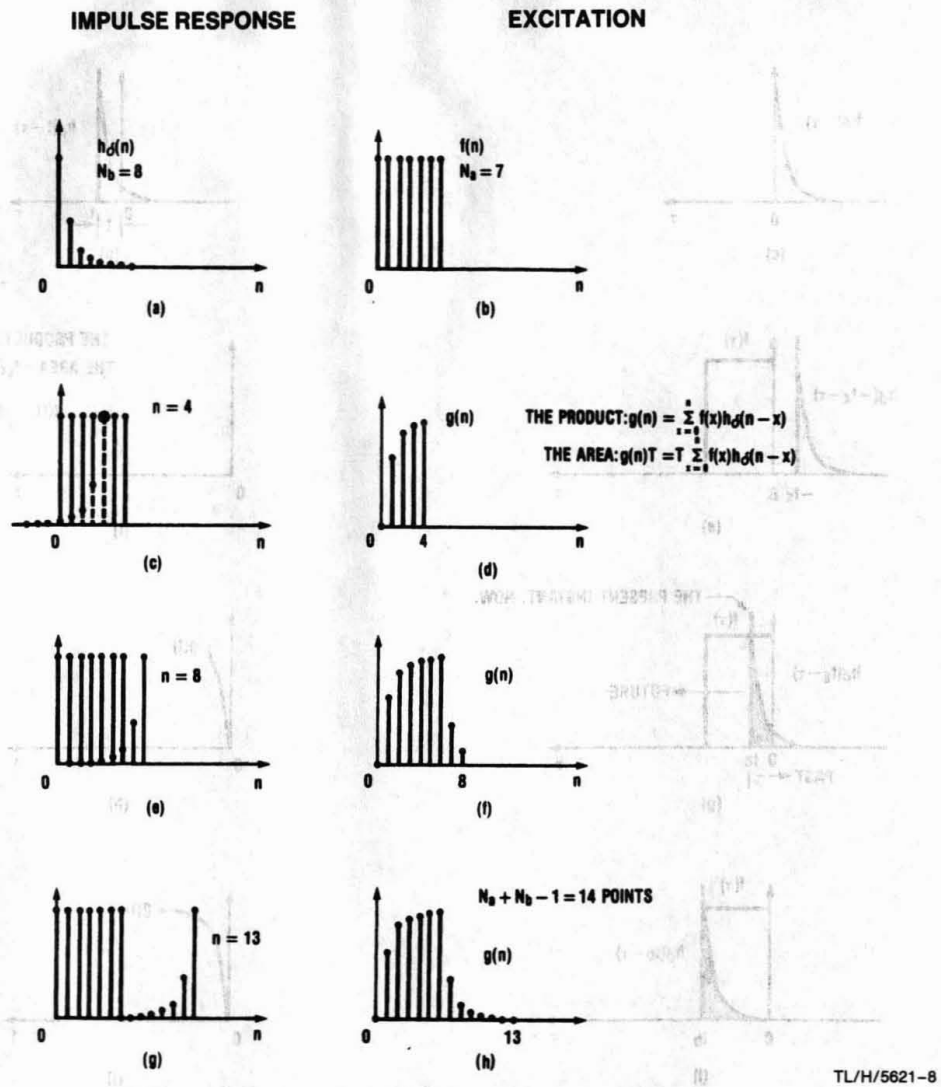


FIGURE 5. Illustrative description of discrete convolution

and $h_\delta(n)$ respectively, *Figures 5a* and *b*.

It is observed additionally that the duration of f(n) is $N_a = 7$ samples [f(n) is nonzero for the interval $0 \le n \le N_a - 1$ and the duration of $h_\delta(n)$ is $N_b = 8$ samples [$h_\delta(n)$ is nonzero for the interval $0 \le n \le N_b - 1$]. The sequence g(n), a discrete convolution, can thus be defined as

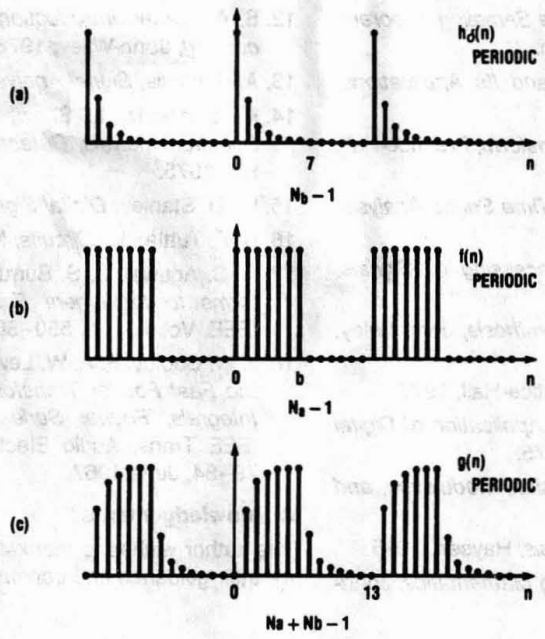
$$g(n) = \sum_{x=0}^{n} f(x)\, h_\delta(n - x) \qquad (21)$$

having a finite duration sequence of $N_a + N_b - 1$ samples, *Figure 5h*. The convolution using numerical integration (area under the curve) can be defined as

$$g(n)T = T \sum_{x=0}^{n} f(x)\, h_\delta(n - x) \qquad (22)$$

where T is the sampling interval used to obtain the sampled data sequences.

If f(n) and $h_\delta(n)$ were next considered to be periodic sequences and a convolution was desired using either shifting techniques or performing an FFT on the excitation and impulse response sequences and finally inverse FFT transforming to achieve the output response, some care must be taken when preparing the convolving sequences. From *Figure 5h* it is observed that the convolution is completed in a $N_a + N_b - 1$ point sequence. To acquire the nonoverlapping or nondistorted periodic sequence of *Figure 6c* the convolution thus requires f(n) and $h_\delta(n)$ to be $N_a + N_b - 1$ point sequences. This is achieved by appending the appropriate number of zero valued samples, also known as zero filling, to f(n) and $h_\delta(n)$ to make them both $N_a + N_b - 1$ point sequences. The undistorted and correct convolution can now be performed using the zero filled sequences *Figure 6a* and *6b* to achieve *6c*.



TL/H/5621–9

FIGURE 6. Linear periodic discrete convolution of f(n) and $h_\delta(n)$, $f(n)*h_\delta(n)$.

A Final Note

This article attempted to simplify the not-so-obvious concept of convolution by first developing the readers knowledge and feel for the implications of the impulse function and its effect upon linear networks. This was followed by a short discussion of network transfer functions and their relative spectrum. Having set the stage, the convolution integral and therorem were introduced and supported with an analytical and illustrative example. This example showed how the response of a simple RC network excited by a rectangular pulse could be determined using the convolution integral.

Finally, two examples of discrete convolution were presented. The first example dealt with finite duration sequences and the second dealt with periodic sequences. Additionally, precautions in the selection on n-point sequences was discussed in the second example to alleviate distorting or spectually overlapping the excitation and impulse response functions during the convolution process.

Appendix A

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Acknowledgements

The author wishes to thank James Moyer and Barry Siegel for their guidance and constructive criticisms.

Wide-Range Current-to-Frequency Converters

National Semiconductor
Application Note 240
Robert A. Pease

Does an analog-to-digital converter cost you a lot if you need many bits of accuracy and dynamic range? Absolute accuracy better than 0.1% is likely to be expensive. But a capability for wide dynamic range can be quite inexpensive. Voltage-to-frequency (V-to-F) converters are becoming popular as a low-cost form of A-to-D conversion because they can handle a wide dynamic range of signals with good accuracy.

Most voltage-to-frequency (V-to-F) converters actually operate with an input current which is proportional to the voltage input:

$$I_{IN} = \frac{V_{IN}}{R_{IN}}$$

(*Figure 1*). This current is integrated by an op amp, and a charge dispenser acts as the feedback path, to balance out the average input current. When an amount of charge Q = I•T (or Q = C•V) per cycle is dispensed by the circuit, then the frequency will be:

$$f = \left(\frac{V_{IN} - V_{OS}}{R_{IN}} + I_b\right) \times \frac{1}{Q}.$$

When V_{IN} is large:

$$f \cong \frac{V_{IN}}{R_{IN}} \times \frac{1}{Q}.$$

When V_{IN} covers a wide dynamic range, the V_{OS} and I_b of the op amp must be considered, as they greatly affect the usable accuracy when the input signal is very small. For example, when the full-scale input is 10V, a signal which is 100 dB below full-scale will be only 100 μV. If the op amp has an offset drift of $\pm$ 100 μ V, (whether caused by time or temperature), that would cause a $\pm$100% error at this signal level. However, a current-to-frequency converter can easily cover a 120 dB range because the voltage offset problem is not significant when the input signal is actually a current source. Let's study the architecture and design of a current-to-frequency converter, to see where we can take advantage of this.

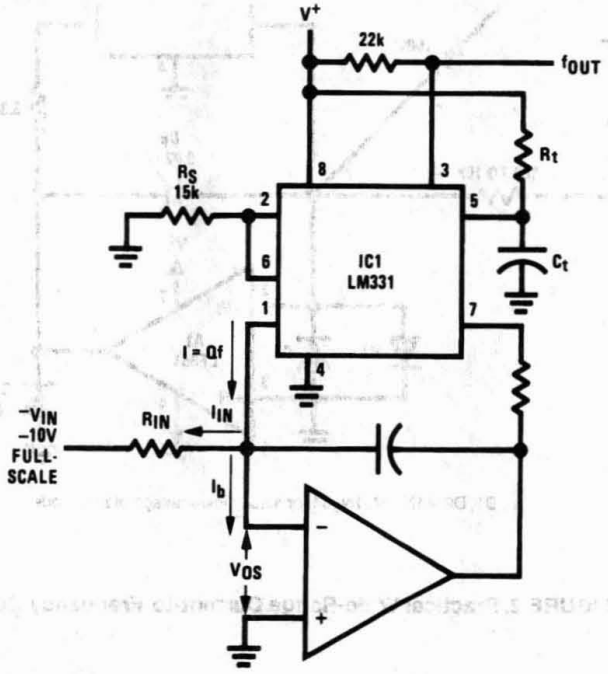

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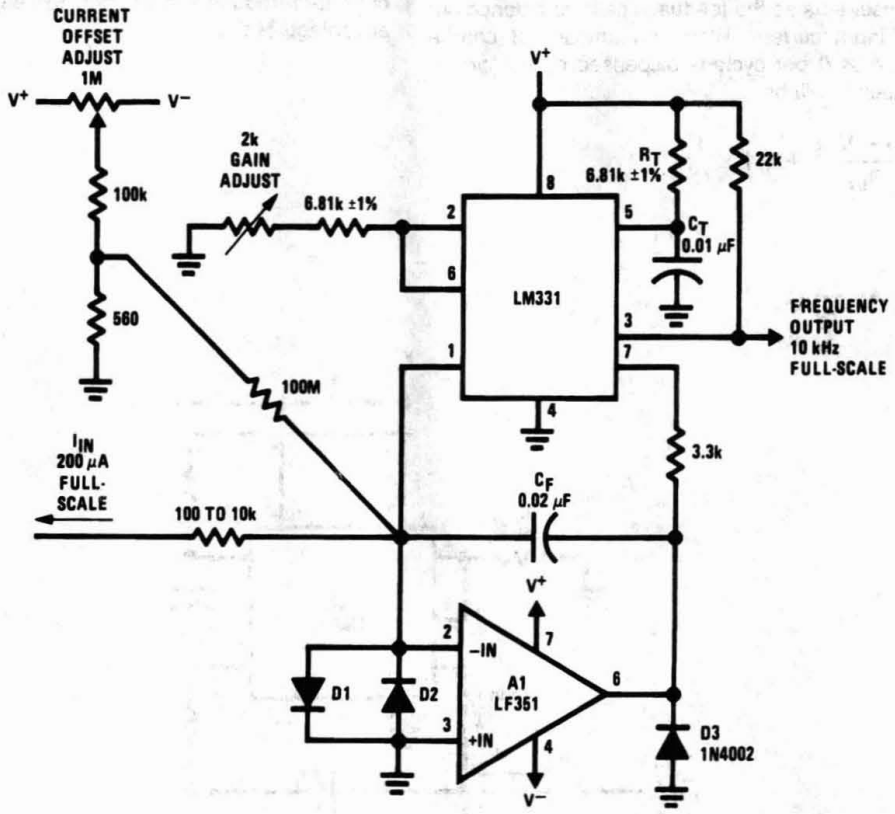
FIGURE 1. Typical Voltage-to-Frequency Converter

When the input signal is a current, the use of a low-voltage-drift op amp becomes of no advantage, and low bias current is the prime specification. A low-cost BI-FET™ op amp such as the LF351A has I_b <100 pA, and temperature coefficient of I_b less than 10 pA/°C, at room temperature. In a typical circuit such as *Figure 2*, the leakage of the charge dispenser is important, too. The LM331 is only specified at 10 nA max at room temperature, because that is the smallest current which can be measured economically on high-speed test equipment. The leakage of the LM331's current-source output at pin 1 is usually 2 pA to 4 pA, and is always less than the 100 pA mentioned above, at 25°C.

The feedback capacitor C_F should be of a low-leakage type, such as polypropylene or polystyrene. (At any temperature above 35°C, mylar's leakage may be excessive.) Also, low-leakage diodes are recommended to protect the circuit's input from any possible fault conditions at the input. (A 1N914 may leak 100 pA even with only 1 millivolt across it, and is unsuitable.)

After trimming this circuit for a low offset when I_{IN} is 1 nA, the circuit will operate with an input range of 120 dB, from 200 μA to 100 pA, and an accuracy or linearity error well below (0.02% of the signal plus 0.0001% of full-scale).

The zero-offset drift will be below 5 or 10 pA/°C, so when the input is 100 dB down from full-scale, the zero drift will be less than 2% of signal, for a ±5°C temperature range. Another way of indicating this performance is to realize that when the input is 1/1000 of full-scale, zero drift will be less than 1% of that small signal, for a 0°C to 70°C temperature range.



D1, D2 = 1N457, 1N484, or similar low-leakage planar diode

FIGURE 2. Practical Wide-Range Current-to-Frequency Converter

What if this isn't good enough? You *could* get a better op amp. For example, an LH0022C has 10 pA max I_b. But it is silly to pay for such a good op amp, with low V offset errors, when only a low input current specification is needed. The circuit of *Figure 3a* shows the simple scheme of using FET followers ahead of a conventional op amp. An LF351 type is suitable because it is a cheap, quick amplifier, well suited for this work. The 2N5909s have a maximum I_b of 1.0 pA, and at room temperature it will drift only 0.1 pA/°C. Typical drift is 0.02 pA/°C.

The voltage offset adjust pot is used to bring the summing point within a millivolt of ground. With an input signal big enough to cause $f_{OUT} = 1$ second per cycle, trim the V offset adjust pot so that closing the *test* switch makes no effect on the output frequency (or, output period). Then adjust the input current offset pot, to get $f_{OUT} = 1/1000$ of full-scale when I_{IN} is 1/1000 of full-scale. When I_{IN} covers the 140 dB range, from 200 μA to 20 pA, the output will be stable, with very good zero offset stability, for a limited temperature range around room temperature. Note these precautions and special procedures:

1. Run the LM331 on 5V to 6V to keep leakage down and to cut the dissipation and temperature rise, too.
2. Run the FETs with a 6V drain supply.
3. Guard all summing point wiring away from all other voltages.

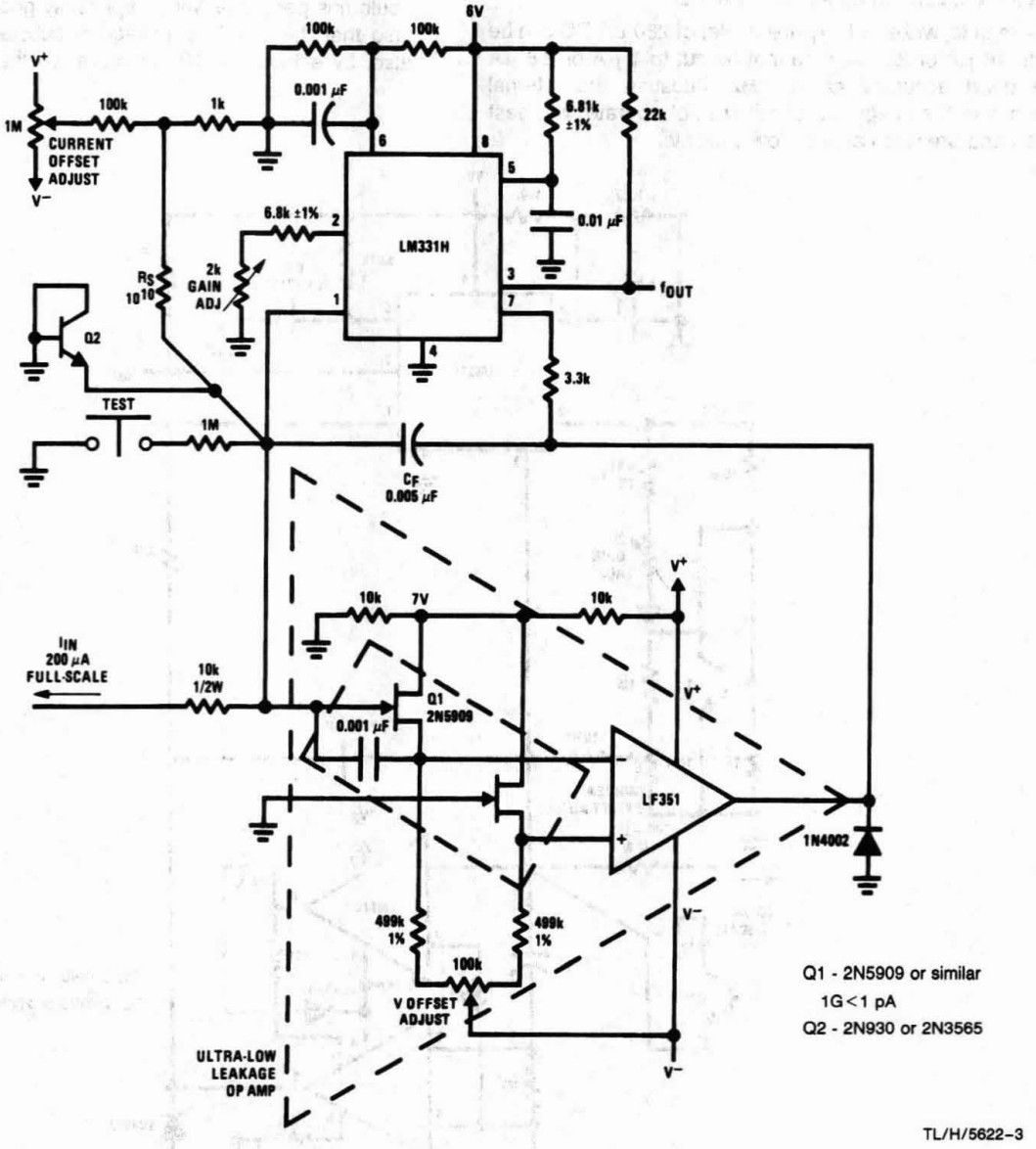


FIGURE 3a. Very-Wide-Range Current-to-Frequency Converter

An alternate approach, shown in *Figure 3b*, uses an LM11C as the input pre-amplifier. The LM11C has much better voltage drift than any of the other amplifiers shown here (normally less than 2 μV/°C) and excellent current drift, less than 1 pA/°C by itself, and typically 0.2 pA/°C when trimmed with the 2N3904 bias current compensation circuit as shown. Of course, the LM331's leakage of 1 pA/°C will still double every 10°C, so that having an amplifier with excellent I_b characteristics does not solve the whole problem, when trying to get good accuracy with a 100 pA signal. For that job, even the leakage of the LM331 must be guarded out!

What if even lower ranges of input current must be accepted? While it might be possible to use a current-to-voltage converter ahead of a V-to-F converter, offset voltage drifts would hurt dynamic range badly. Response and zero-drift of such an I-V will be disappointing. Also, it is not feasible to starve the LM331 to an arbitrary extent.

For example, while its I_{OUT} (full-scale) of 280 μA DC can be cut to 10 μA or 28 μA, it cannot be cut to 1 μA or 2.8 μA with good accuracy at 10 kHz, because the internal switches in the integrated circuit will not operate with best speed and precision at such low currents.

Instead, the output current from pin 1 of the LM331 can be fed through a current attenuator circuit, as shown in *Figure 4*. The LM334 (temperature-to-current converter IC) causes −120 mV bias to appear at the base of Q2. When a current flows out of pin 1 of the LM331, 1/100 of the current will flow out of Q1's collector, and the rest will go out of Q2's collector. As the LM334's current is linearly proportional to Kelvin temperature, the −120 mV at Q2's base will change linearly with temperature so that the Q1/Q2 current divider stays at 1:100, invariant of temperature, according to the equation:

$$i_1/i_2 = e^{\frac{q(Vb1 - Vb2)}{kT}}$$

This current attenuator will work stably and accurately, even at high speeds, such as for 4 μS current pulses. Thus, the output of Q1 is a charge pump which puts out only 10 picocoulombs per pulse, with surprisingly good accuracy. Note also that the LM331's leakage is substantially attenuated also, by a factor of 100 or more, so that source of error

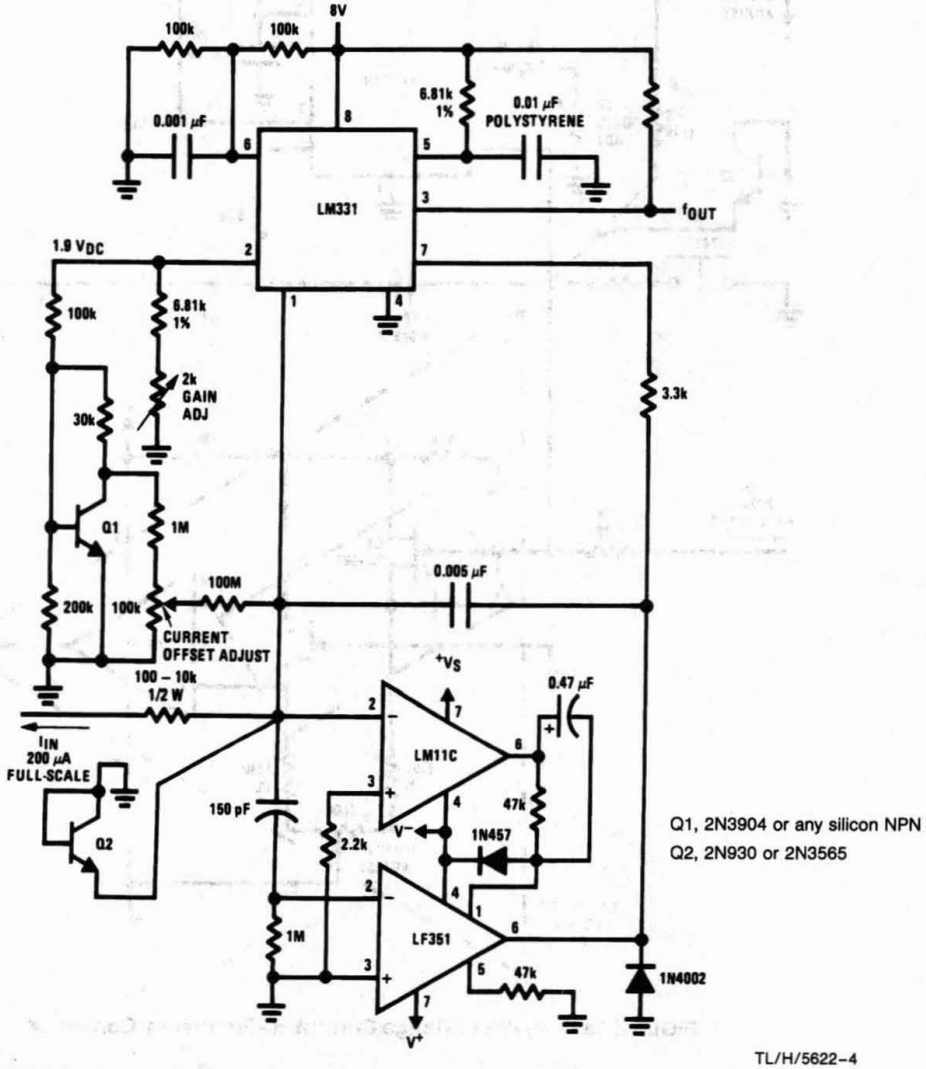


FIGURE 3b. Very-Wide-Range I-to-F Converter with Low Voltage Drift

virtually disappears. When Q1 is off, it is really *OFF,* and its leakage is typically 0.01 pA if the summing point is within a millivolt or two of ground.

To do justice to this low leakage of the VFC, the op amp should be made with MOSFETs for Q3 and Q4, such as the Intersil 3N165 or 3N190 dual MOSFET (with no gate-protection dodes). When MOSFETs have relatively poor offset voltage, offset voltage drift, and voltage noise, this circuit does not care much about these characteristics, but instead takes advantage of the MOSFET's superior current leakage and current drift.

Now, with an input current of 1 μA, the full-scale output frequency will be 100 kHz. At a 1 nA input, the output frequency will be 100 Hz. And, when the input current is 1 pA, the output frequency will drop to 1 cycle per 10 seconds or 100 mHz. When the input current drops to zero, frequencies as small as 500 μHz have been observed, at 25°C and also as warm as 35°C. Here is a wide-range data converter whose zero drift is *well* below 1 ppm per 10°C! (Rather more like 0.001 ppm per°C.) The usable dynamic range is better than 140 dB, with excellent accuracy at inputs between 100% and 1% and 0.01% and 0.0001% of full-scale.

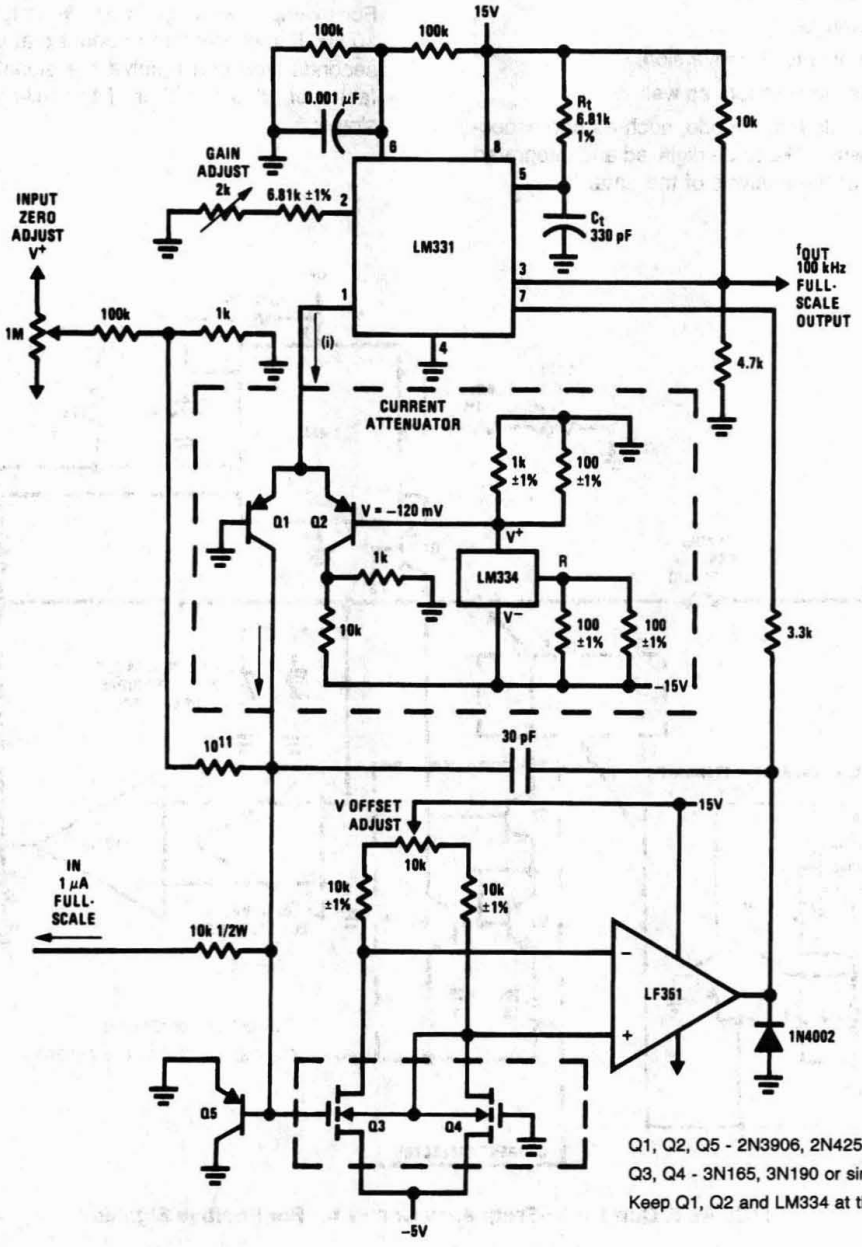


FIGURE 4. Picoampere-to-Frequency Converters

If a positive signal is of interest, the LM331 can be applied with a current reflector as in *Figure 5*. This current reflector has high output impedance, and low leakage. Its output can go directly to the summing point, or via a current attenuator made with NPN transistors, similar to the PNP circuit of *Figure 4*. This circuit has been observed to cover a wide (130 dB) range, with 0.1% of signal accuracy.

What is the significance of this wide-range current-to-frequency converter? In many industrial systems the question of using an inexpensive 8-bit converter instead of an expensive 12-bit data converter is a battle which is decided every day. But if the signal source is actually a current source, then you can use a V-to-F converter to make a cheap 14-bit converter or an inexpensive converter with 18 bits of dynamic range. The choice is yours.

Why use an I-to-F converter?

- It is a natural form of A-to-D conversion.
- It naturally facilitates integration, as well.
- There are many signals in the world, such as photospectrometer currents, which like to be digitized and integrated as a standard part of the analysis of the data.
- Similarly: photocurrents, dosimeters, ionization currents, are examples of currents which beg to be integrated in a current-to-frequency meter.
- Other signal sources which provide output currents are:
  - —Phototransistors
  - —Photo diodes
  - —Photoresistors (with a fixed voltage bias)
  - —Photomultiplier tubes
  - —Some temperature sensors
  - —Some IC signal conditioners

Why have a fast frequency out?

- A 100 kHz output full-scale frequency instead of 10 kHz means that you have 10 times the resolution of the signal. For example, when I_{IN} is 0.01% of full-scale, the f will be 10 Hz. If you integrate or count that frequency for just 10 seconds, you can resolve the signal to within 1% — a factor of 10 better than if the full-scale frequency were slower.

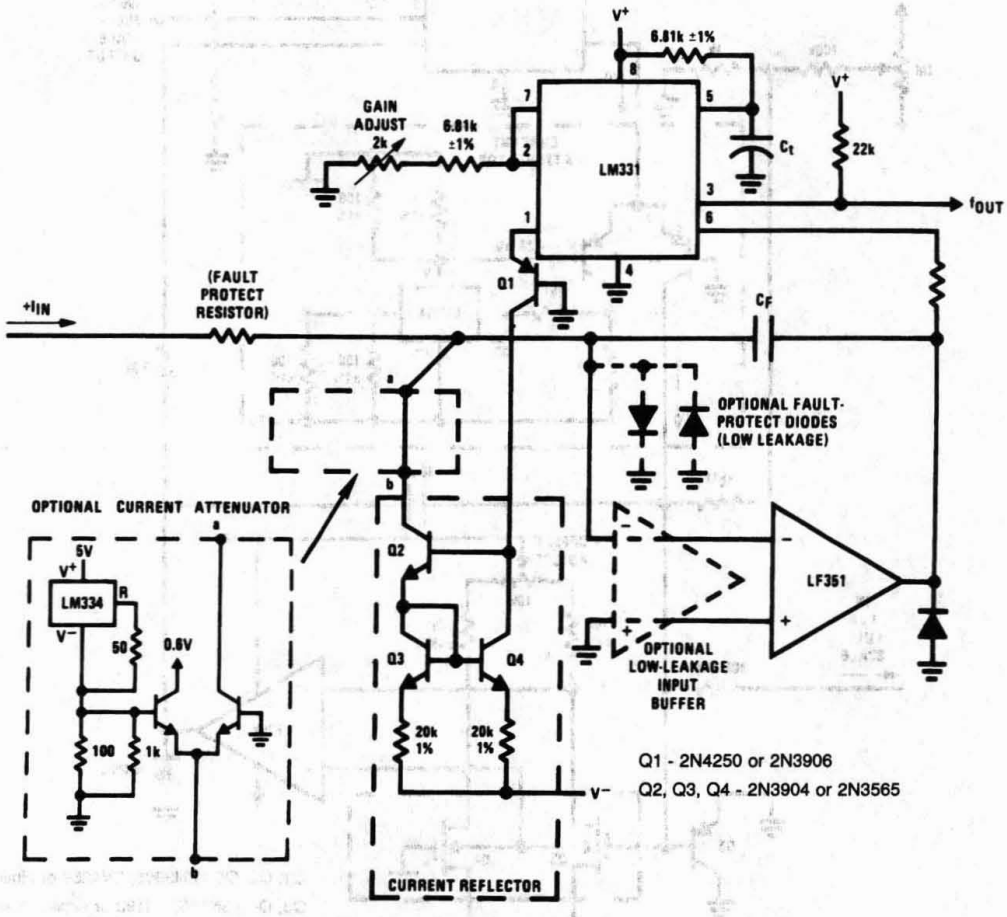


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FIGURE 5. Current-to-Frequency Converter For Positive Signals

Working with High Impedance Op Amps

National Semiconductor
Application Note 241

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Abstract. *New developments have dramatically reduced the error currents of IC op amps, especially at high temperatures. The basic techniques used to obtain this peformance are briefly described. Some of the problems associated with working at the high impedance levels that take advantage of these low error currents are discussed along with their solutions. The areas involved are printed-circuit board leakage, cable leakage and noise generation, semiconductor-switch leakages, large-value resistors and capacitor limitations.*

Introduction

A new, low cost op amp reduces dc error terms to where the amplifier may no longer be the limiting factor in many practical circuits. FET bias currents are equalled at room temperature; but unlike FETs, the bias current is relatively stable even over a −55°C to 125°C temperature range. Offset voltage and drift are low because bipolar inputs and on-wafer trimming are used. The 100 μV offset voltage and 25 pA bias current are expected to advance the state of the art for high impedance sensors and signal conditioners.

bias currents

There has been a continual effort to reduce the bias current of IC op amps ever since the μA709 was introduced in 1965. The LM101A, announced in 1968, dropped this current by an order of magnitude through improved processing that gave better transistor current gain at low operating currents. In 1969, super-gain transistors (see appendix) were applied in the LM108 to beat FET performance when temperatures above 85°C were involved.

In 1974 FETs were integrated with bipolar devices to give the first FET op amp produced in volume, the LF155. These devices were faster than general purpose bipolar op amps and had lower bias current below 70°C. But FETs exhibit higher offset voltage and drift than bipolars. Long-term stability is also about an order of magnitude worse. Typically, this drift is 100 μV/year, but a small percentage could be as bad as 1 mV. Laser trimming and other process improvements have lowered initial offset but have not eliminated the drift problem.

The new IC is an extension of super-gain bipolar techniques. As can be seen from *Figure 1*, it provides low bias currents over a −55°C to 125°C temperature range. The offset current is so low as to be lost in the noise. This level of performance has previously been unavailable for either low-cost industrial designs or high reliability military/space applications.

This low bias current has not been obtained at the expense of offset voltage or drift. Typical offset voltage is under a millivolt and provision is made for on-water trimming to get it below 100 μV. The low drift exhibited in *Figure 2* indicates that the circuit is inherently balanced for exceptionally low drift, typically 1 μV/°C below 100°C.

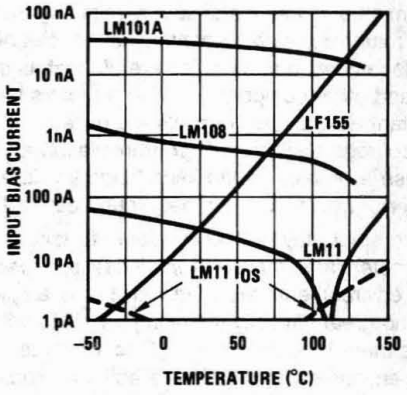

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Figure 1. Comparison of typical bias currents for various types of IC op amps. New bipolar device not only has lower bias current over practical temperature ranges but also lower drift. Offset current is unusually low with the new design.

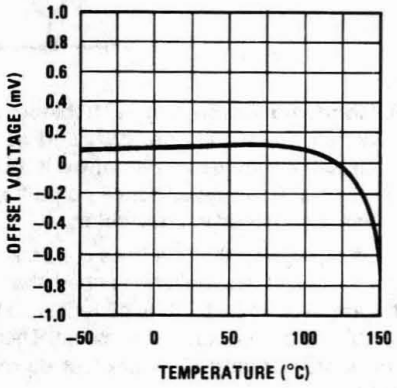

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Figure 2. Bipolar transistors have inherently low offset voltage and drift. The low drift of the LM11 over a wide temperature range shows that there are no design problems degrading performance.

the new op amp

The LM11 is, in essence, a refinement of the LM108. A modified Darlington input stage has been added to reduce bias currents. With a standard Darlington, one transistor is biased with the base current of the other. This degrades dc amplifier performance because base current is noisy, subject to wide variation and generally unpredictable.

Supplying a bleed current greater than the base current, as shown in *Figure 3*, removes this objection. The 60 nA provided is considerably in excess of the 1 nA base current. The bleed current is made to vary as absolute temperature to maintain constant impedance at the emitters of Q1 and Q2. This stabilizes frequency response and also reduces the thermal variation of bias current. Parasitic capacitances of the current generator have been bootstrapped so that the 0.3 V/μs slew rate of the basic amplifier is unaffected.

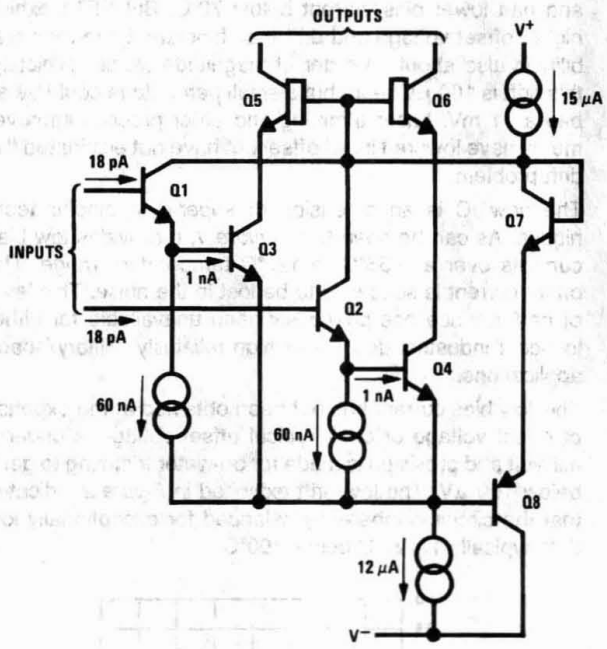

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Figure 3. Modifying Darlington with bleed current reduces offset voltage, drift and noise. Unique circuitry provides well-controlled current with minimal stray capacitance so that speed of the basic amplifier is unaffected.

Results to date suggest that the base currents of this modified Darlington input are better matched than the simple differential amplifier. In fact, offset current is so low as to be unmeasurable on production test systems. Therefore, guaranteed limits are determined by the test equipment rather than the IC.

noise

Operating transistors at very low currents does increase noise. Thus, the LM11 is about a factor of four noisier than the LM108. But the low frequency noise, plotted in *Figure 4*, is still slightly less than that of FET amplifiers. Long-term measurements indicate that the offset voltage shift is under 10 μV.

In contrast to the noise voltage, low frequency noise current is subject to greater unit-to-unit variation. Generally, it is below 1 pA, peak-to-peak, about the same magnitude as the offset current.

With the LM11, both voltage and current related dc errors have been reduced to the point where overall circuit performance could well be noise limited, particularly in limited temperature range applications.

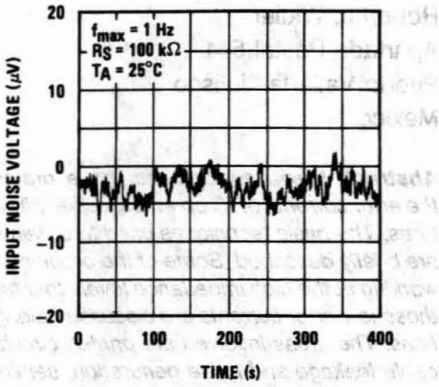

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Figure 4. Lower operating currents increase noise, but low frequency noise is still slightly lower than IC FET amplifiers. Long-term stability is much improved.

reliability

The reliability of the LM11 is not expected to be substantially different than the LM108, which has been used extensively in military and space applications. The only significant difference is the input stage. The low current nodes introduced here might possibly be a problem were they not bootstrapped, biased and guarded to be virtually unaffected by both bulk and surface leakages. This opinion is substantiated by preliminary life-test data.

This IC could, in fact, be expected to improve reliability when used to replace discrete or hybrid amplifiers that use selected components and have been trimmed and tweaked to give the required performance.

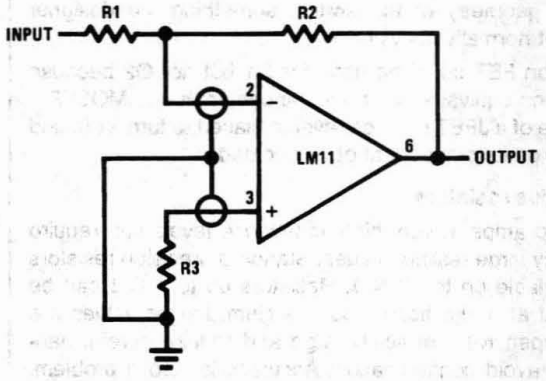
From an equipment standpoint, reliability analysis of insulating materials, surface contamination, cleaning procedures, surface coating and potting are at least as important as the IC and other components. These factors become more important as impedance levels are raised. But this should not discourage designers. If poor insulation and contamination cause a problem when impedance levels are raised by an order of magnitude, it is best found out and fixed.

Even so, it may not be advisable to take advantage of the full potential of the LM11 in all cases, especially when hostile environments are involved. For example, there should be no great difficulty in finding an LM11 with offset current less than 5 pA over a −55°C to 125°C temperature range. But anyone designing high-reliability equipment that is going to be in trouble if combined leakages are greater than 10 pA at 125°C had best know what he is about.

electrical guarding

The effects of board leakage can be minimized using an old trick known as guarding. Here the input circuitry is surrounded by a conductive trace that is connected to a low impedance point at the same potential as the inputs. The electrical connection of the guard for the basic op amp configurations is shown in *Figure 5*. The guard absorbs the leakage from other points on the board, drastically reducing that reaching the input circuitry.

To be completely effective, there should be a guard ring on both sides of the printed-circuit board. It is still recommended for single-sided boards, but what happens on the unguarded side is difficult to analyze unless Teflon inserts are used on the input leads. Further, although surface leakage can be virtually eliminated, the reduction in bulk leakage is much less. The reduction in bulk leakage for double-sided guarding is about an order of magnitude, but this depends on board thickness and the width of the guard ring. If there are bulk leakage problems, Teflon inserts on the through holes and Teflon or kel-F standoffs for terminations can be used. These two materials have excellent surface properties without surface treatment even in high-humidity environments.



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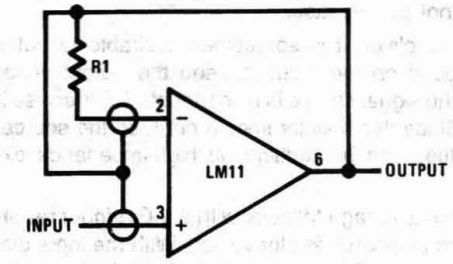
a. inverting amplifier



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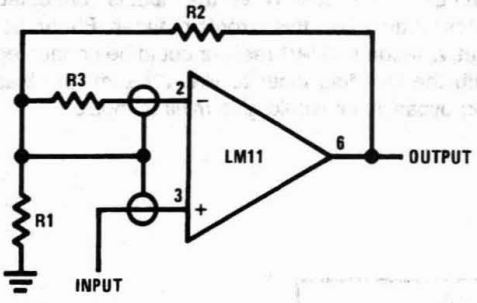
b. follower



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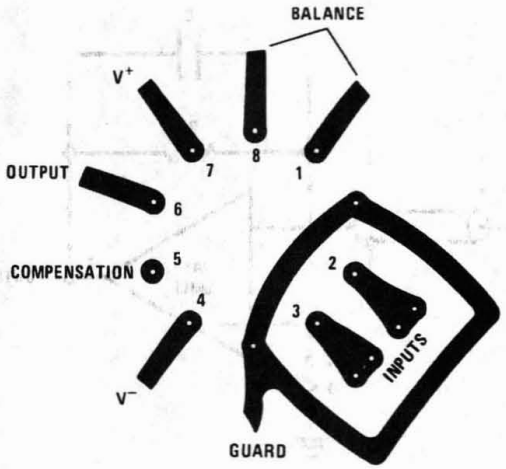
c. non-inverting amplifier

Figure 5. Input guarding for various op amp connections. The guard should be connected to a point at the same potential as the inputs with a low enough impedance to absorb board leakage without introducing excessive offset.

An example of a guarded layout for the metal-can package is shown in *Figure 6*. Ceramic and plastic dual-in-line packages are available for critical applications with guard pins adjacent to the inputs both to facilitate board layout and to reduce package leakage. These guard pins are not internally connected.



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Bottom View

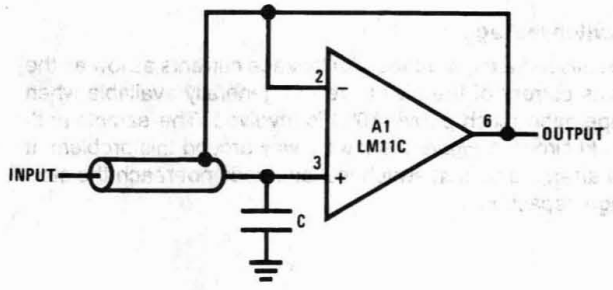
Figure 6. Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.

signal cables

It is advisable to locate high impedance amplifiers as close as possible to the signal source. But sometimes connecting lines cannot be avoided. Coaxially shielded cables with good insulation are recommended. Polyethelene or virgin (not reconstituted) Teflon is best for critical applications.

In addition to potential insulation problems, even short cable runs can reduce bandwidth unacceptably with high source resistances. These problems can be largely avoided by bootstrapping the cable shield. This is shown for the follower connection in *Figure 7*. In a way, bootstrapping is positive feedback; but instability can be avoided with a small capacitor on the input.

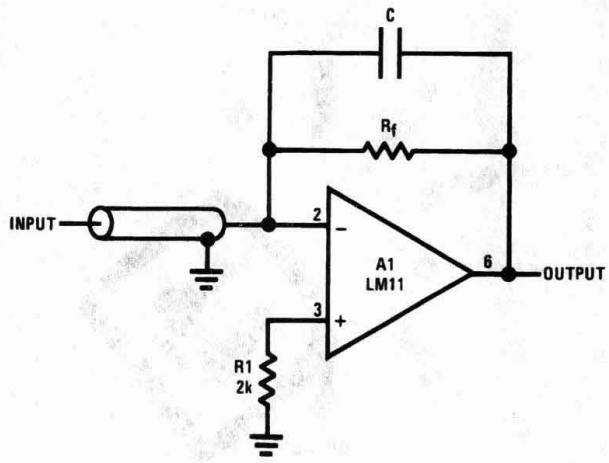
Cable Bootstrapping



TL/H/7478–9

Figure 7. Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.

With the summing amplifier, the cable shield is simply grounded, with the summing node at virtual ground. A small feedback capacitor may be required to insure stability with the added cable capacitance. This is shown in *Figure 8*.



TL/H/7478–10

Figure 8. With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

An inverting amplifier with gain may require a separate follower to drive the cable shield if the influence of the capacitance, between shield and ground, on the feedback network cannot be accounted for.

High impedance circuits are also prone to mechanical noise (microphonics) generated by variable stray capacitances. A capacitance variation will generate a noise voltage given by

$$e_n = \frac{\Delta C}{C} V,$$

where V is the dc bias on the capacitor. Therefore, the wiring and components connected to sensitive nodes should be mechanically rigid.

This is also a problem with flexible cables, in that bending the cable can cause a capacitance change. Bootstrapping the shield nearly eliminates dc bias on the cable, minimizing the voltage generated. Another problem is electrostatic charge created by friction. Graphite lubricated Teflon cable will reduce this.

switch leakage

Semiconductor switches with leakage currents as low as the bias current of the LM11 are not generally available when operation much above 50°C is involved. The sample-and-hold circuit in *Figure 9* shows a way around this problem. It is arranged so that switch leakage does not reach the storage capacitor.

Isolating leakage current requires that two switches be connected in series. The leakage of the first, Q1, is absorbed by R1 so that the second, Q2, only has the offset voltage of the op amp across its junctions. This can be expected to reduce leakage by at least two orders of magnitude. Adjusting the op amp offset to zero at the maximum operating temperature will give the ultimate leakage reduction, but this is not usually required with the LM11.

MOS switches with gate-protection diodes are preferred in production situations as they are less sensitive to damage from static charges in handling. If used, D1 and R2 should be included to remove bias from the protection diode during hold. This may not be required in all cases but is advised since leakage from the protection diode depends on the internal geometry of the switch, something the designer does not normally control.

A junction FET could be used for Q1 but not Q2 because there is no equivalent to the enhancement mode MOSFET. The gate of a JFET must be reverse biased to turn it off, and leakage on its output cannot be avoided.

high-value resistors

Using op amps at very high impedance levels can require unusually large resistor values. Standard precision resistors are available up to 10 MΩ. Resistors up to 1 GΩ can be obtained at a significant cost premium. Larger values are quite expensive, physically large and require careful handling to avoid contamination. Accuracy is also a problem. There are techniques for raising effective resistor values in op amp circuits. In theory, performance is degraded; in practice, this may not be the case.

With a buffer amplifier, it is sometimes desirable to put a resistor to ground on the input to keep the output under control when the signal source is disconnected. Otherwise it will saturate. Since this resistor should not load the source, very large values can be required in high-impedance circuits.

Figure 10 shows a voltage follower with a 1 GΩ input resistance built using standard resistor values. With the input disconnected, the input offset voltage is multiplied by the same factor as R2; but the added error is small because the offset voltage of the LM11 is so low. When the input is connected to a source less than 1 GΩ, this error is reduced. For an ac-coupled input, a second 10 MΩ resistor could be connected in series with the inverting input to virtually eliminate bias current error; bypassing it would give minimal noise.

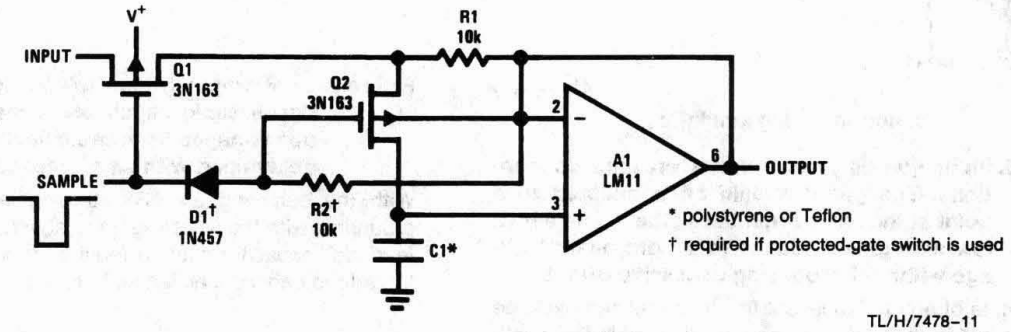


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Figure 9. Switch leakage in this sample and hold does not reach storage capacitor. If Q2 has an internal gate-protection diode, D1 and R2 must be included to remove bias from its junction during hold.

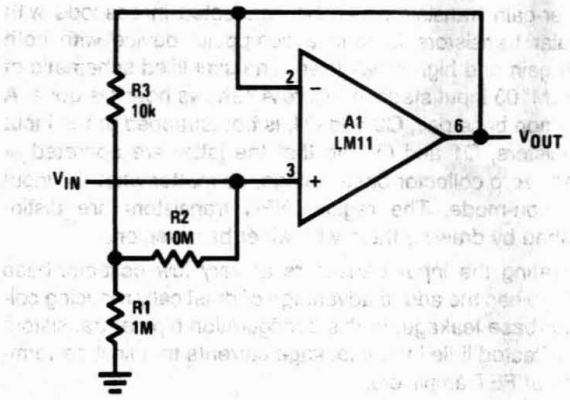

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Figure 10. Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.

The voltage-to-current converter in *Figure 11* uses a similar method to obtain the equivalent of a 10 GΩ feedback resistor. Output offset is reduced because the error can be made dependent on offset current rather than bias current. This would not be practical with large value resistors because of cost, particularly for matched resistors, and because the summing node would be offset several hundred millivolts from ground. In *Figure 11*, this offset is limited to several millivolts. In addition, the output can be nulled with the usual balance potentiometer. Further, gain trimming is easily done.

Resistance Multiplication

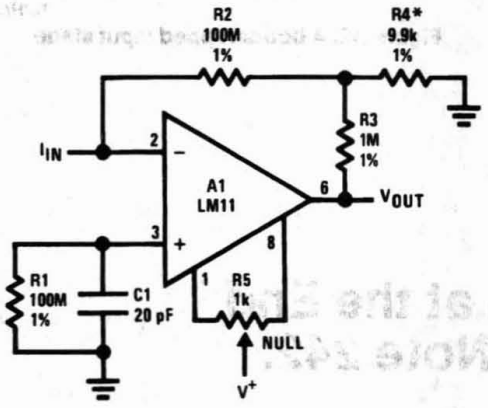

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Figure 11. Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.

This circuit would benefit from lower offset current than can be tested and guaranteed with automatic test equipment. But there should be no problem in selecting a device for critical applications.

capacitors

Op amp circuits impose added requirements on capacitors, and this is compounded with high-impedance circuitry. Frequency shaping and charge measuring circuits require control of the capacitor tolerance, temperature drift and stability with temperature cycling. For smaller values, NPO ceramic is best while a polystyrene-polycarbonate combination gives good results for larger values over a −10°C to 85°C range.

Dielectric absorption can also be a problem. It causes a capacitor that has been quick-charged to drift back toward its previous state over many milliseconds. The effect is most noticeable in sample-and-hold circuits. Polystyrene, Teflon and NPO ceramic capacitors are most satisfactory in this regard. Choice depends mainly on capacitance and temperature range.

Insulation resistance can clearly become a problem with high-impedance circuitry. Best performer is Teflon, with polystyrene being a good substitute below 85°C. Mylar capacitors should be avoided, especially where higher temperatures are involved.

Temperature changes can also alter the terminal voltage of a capacitor. Because thermal time constants are long, this is only a problem when holding intervals are several minutes or so. The effect is reported to be as high as 10 mV/°C, but Teflon capacitors that hold it to 0.5 mV/°C are available*.

An op amp with lower bias current can ease capacitor problems, primarily by reducing size. This is obvious with a sample-and-hold because the capacitor value is determined by the hold interval and the amplifier bias current. The circuit in *Figure 12* is another example. An RC time constant of more than a quarter hour is obtained with standard component values. Even when such long time constants are not required, reducing capacitor size to where NPO ceramics can be used is a great aid in precision work.

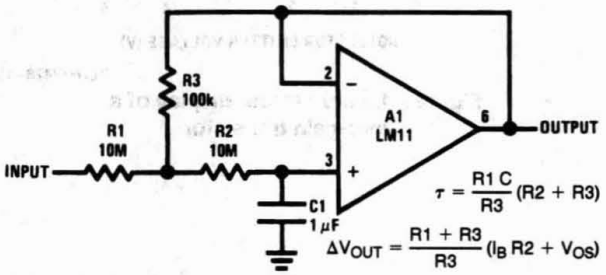

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Figure 12. This circuit multiplies RC time constant to 1000 seconds and provides low output impedance. Cost is lowered because of reduced resistor and capacitor values.

conclusions

A low cost IC op amp has been described that not only has low offset voltage but also advances the state of the art in reducing input current error, particularly at elevated temperatures. Designers of industrial as well as military/space equipment can now work more freely at high impedance levels.

Although high-impedance circuitry is more sensitive to board leakages, wiring capacitances, stray pick-up and leakage in other components, it has been shown how input guarding, bootstrapping, shielding and leakage isolation can largely eliminate these problems.

*Component Research Co., Inc., Santa Monica, California.

acknowledgment

The author would like to acknowledge the assistance of the staff at National Semiconductor in implementing this design and sorting out the application problems. Discussions with Bob Dobkin, Bob Pease, Carl Nelson and Mineo Yamatake have been most helpful.

appendix

super-gain techniques

Super-gain transistors are not new, having been developed for the LM102/LM110 voltage followers in 1967 and later used on the LM108 general-purpose op amp. They are similar to regular transistors, except that they are diffused for high current gains (2,000–10,000) at the expense of breakdown voltage. A curve-tracer display of a typical device is shown in *Figure A1*. In an IC, super-gain transistors can be made simultaneously with standard transistors by including a second, light base predeposition that is diffused less deeply.

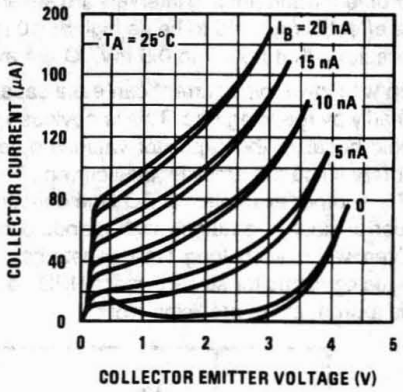

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Figure A1. curve tracer display of a super-gain transistor

Super-gain transistors can be connected in cascode with regular transistors to form a composite device with both high gain and high breakdown. The simplified schematic of the LM108 input stage in *Figure A2* shows how it is done. A common base pair, Q3 and Q4, is bootstrapped to the input transistors, Q1 and Q2, so that the latter are operated at nearly zero collector-base voltage, no matter what the input common-mode. The regular NPN transistors are distinguished by drawing them with wider base regions.

Operating the input transistors at very low collector-base voltage has the added advantage of drastically reducing collector-base leakage. In this configuration bipolar transistors are affected little by the leakage currents that limit performance of FET amplifiers.

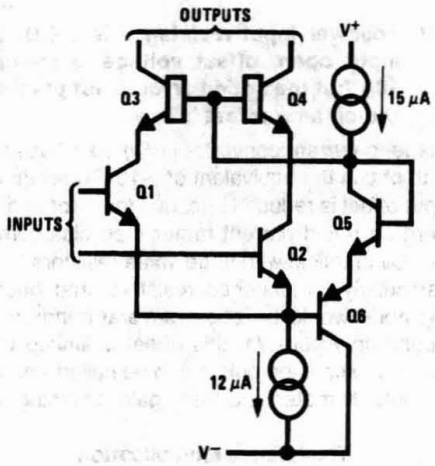

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Figure A2. A bootstrapped input stage

***See Addendum at the End of Application Note 242.**

Applying a New Precision Op Amp

National Semiconductor
Application Note 242

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***Abstract**: A new bipolar op amp design has advanced the state of the art by reducing offset voltage and bias current errors. Its characteristics are described here, indicating an ultimate input resolution of 10 μV and 1 pA under laboratory conditions. Practical circuits for making voltmeters, ammeters, differential instrumentation amplifiers and a variety of other designs that can benefit from the improved performance are covered in detail. Methods of coupling the new device to existing fast amplifiers to take advantage of the best characteristics of both, even in follower applications, are explored.*

introduction

A low cost, mass-produced op amp with electrometer-type input currents combined with low offset voltage and drift is now available. Designated the LM11, this IC can minimize production problems by providing accuracy without adjustments, even in high-impedance circuitry. On the other hand, if pushed to its full potential, what has been impossible in the past becomes entirely practical.

Significantly, the LM11 is not restricted to commercial and industrial use. Devices can be completely specified over a −55°C to +125°C range. Preliminary data indicates that reliability is the same as standard ICs qualified for military and space applications.

The essential details of the design along with an introduction to the peculiarities of high-impedance circuits have been presented elsewhere.* This will be expanded here. Practical circuitry that reduces effective bias current for those applications where performance cannot be made dependent on offset current are described. In addition, circuits combining the DC characteristics of the new part with the AC performance of existing fast amplifiers will be shown. This will be capped with a number of practical designs to provide some perspective into what might be done.

dc errors

Barring the use of chopper or reset stabilization, the best offset voltage, drift and long-term stability are obtained using bipolar transistors for the op amp input stage. This has been done with the LM11. On-wafer trimming further improves performance. Typically, a 100 μV offset with 1 μV/°C drift results.

Transistors with typical current gains of 5000 have been used in the manufacture of the LM11. The input stage employs a Darlington connection that has been modified so that offset voltage and drift are not degraded. The typical input currents, plotted in *Figure 1,* demonstrate the value of the approach.

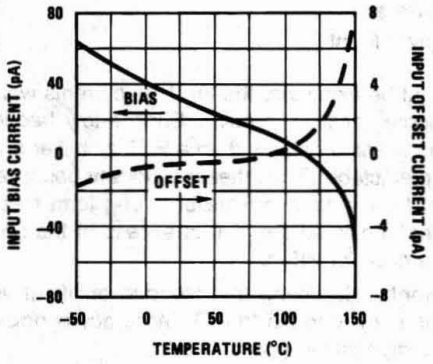

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Figure 1. Below 100°C, bias current varies almost linearly with temperature. This means that simple circuitry can be used for compensation. Offset current is unusually low.

The offset current of this op amp is so low that it cannot be measured on existing production test equipment. Therefore, it probably cannot be specified tighter than 10 pA. For critical applications, the user should have little difficulty in selecting to a tighter limit.

The bias current of the LM11 equals that of monolithic FET amplifier at 25°C. Unlike FETs, it does not double every 10°C. In fact, the drift over a −55°C to +125°C temperature range is about the same as that of a FET op amp during normal warm up.

Other characteristics are summarized in Table I. It can be seen that the common-mode rejection, supply-voltage rejection and voltage gain are high enough to take full advantage of the low offset voltage. The unspectacular 0.3V/μs slew rate is balanced by the 300 μA current drain.

*R. J. Widlar, "Working with High Impedance Op Amps", National Semiconductor AN-241.

Table I. Typical characteristics of the LM11 for $T_j = 25°C$ and $V_S = \pm 15V$. Operation is specified down to $V_S = \pm 2.5V$.

Parameter	Conditions	Value
Input Offset Voltage		100 μV
Input Offset Current		500 fA
Input Bias Current		25 pA
Input Noise Voltage	0.01 Hz ≤ f ≤ 10 Hz	8 μVpp
Input Noise Current	0.01 Hz ≤ f ≤ 10 Hz	1 pApp
Long Term Stability	$T_j = 25°C$	10 μV
Offset Voltage Drift	$-55°C \le T_j \le 125°C$	1 μV/°C
Offset Current Drift	$-55°C \le T_j \le 125°C$	20 fA/°C
Bias Current Drift	$-55°C \le T_j \le 125°C$	500 fA/°C
Voltage Gain	$V_{OUT} = \pm 12V$, $I_{OUT} = \pm 0.5$ mA	1,200V/mV
	$V_{OUT} = \pm 12V$, $I_{OUT} = \pm 2$ mA	300V/mV
Common-Mode Rejection	$-12.5V \le V_{CM} \le 14V$	130 dB
Supply-Voltage Rejection	$\pm 2.5V \le V_S \le \pm 20V$	118 dB
Slew Rate		0.3V/μs
Supply Current		300 μA

As might be expected, the low bias currents were obtained with some sacrifice in noise. But the low frequency noise voltage is still a bit less than a FET amplifier and probably more predictable. The latter is important because this noise cannot be tested in production. Long term measurements have not indicated any drift in excess of the noise. This is not the case for FETs.

It is worthwhile noting that the drift of offset voltage and current is low enough that DC accuracy is noise limited in room-temperature applications.

bias current compensation

The LM11 can operate from MΩ source resistances with little increase in the equivalent offset voltage, as can be seen in *Figure 2*. This is impressive considering the low initial offset voltage. The situation is much improved if the design can be configured so that the op amp sees equal resistance on the two inputs. However, this cannot be done with all circuits. Examples are integrators, sample and holds, logarithmic converters and signal-conditioning amplifiers. And even though the LM11 bias current is low, there will be those applications where it needs to be lower.

Referring back to *Figure 1*, it can be seen that the bias current drift is essentially linear over a −50°C to +100°C range. This is a deliberate consequence of the input stage design. Because of it, relatively simple circuitry can be used to develop a compensating current.

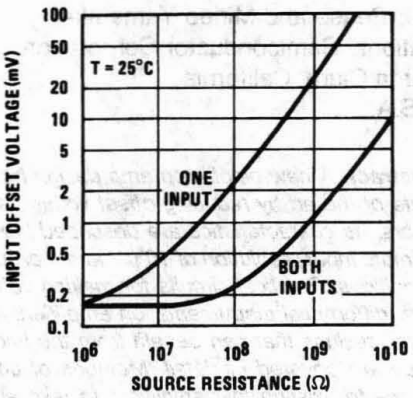

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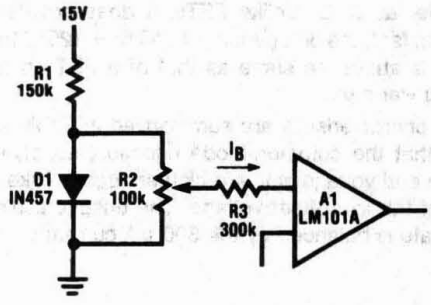
Figure 2. The LM11 operates from MΩ source resistances with little DC error. With equal source resistances, accuracy is essentially limited by low frequency current noise.

Bias current compensation is not new, but making it effective with even limited temperature excursions has been a problem. An early circuit suggested for bipolar ICs is shown in *Figure 3a*. The compensating current is determined by the diode voltage. This does not vary as rapidly with temperature as bias current nor does it match the usual non-linearities.

With the improved circuit in *Figure 3b*, the temperature coefficient can be increased by using a transistor and including R2. The drop across R2 is nearly constant with temperature. The voltage delivered to the potentiometer has a 2.2 mV/°C drift while its magnitude is determined by R2. Thus, as long as the bias current varies linearly with temperature, a value for R2 can be found to effect compensation.



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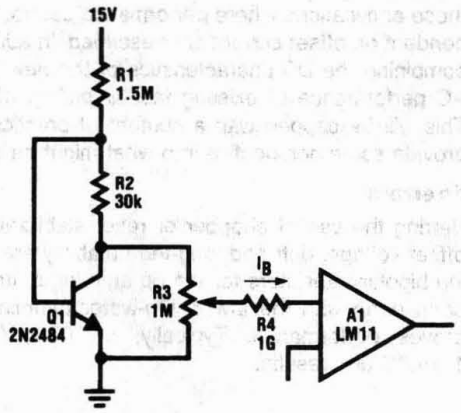
a. original circuit



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b. improved version

Figure 3. Bias-current compensation. With the improved version, the temperature coefficient of the compensating current can be varied with R2. It is effective only if bias current has linear, negative temperature coefficient.

In production, altering resistors based on temperature testing is to be avoided if at all possible. Therefore, the results that can be obtained with simple nulling at room temperature and a fixed value for R2 are of interest. *Figure 4* gives this data for a range of parts with different initial bias currents. This was obtained from pre-production and initial-production runs. The bias current variations were the result of both h_{FE} variations and changes in internal operating currents and represent the worst as well as best obtained. They are therefore considered a realistic estimate of what would be encountered among various production lots.

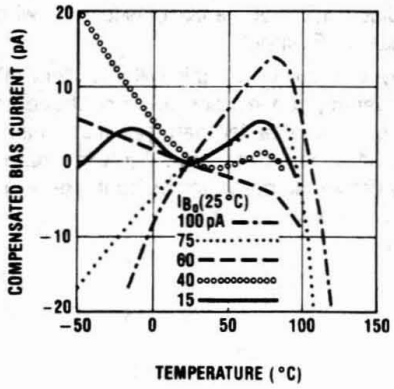

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Figure 4. Compensated bias current for five representative units with a range of initial bias currents. The circuit in *Figure 3b* was used with balancing at 25°C. High drift devices could be improved further by altering R2.

Little comment need be made on these results, except that the method is sufficiently predictable that another factor of five reduction in worst case bias current could be made by altering R2 based on the results of a single temperature run.

One disadvantage of the new circuit is that it is more sensitive to supply variations than the old. This is no problem if the supplies are regulated to 1%. But with worst regulation it suffers because, with R2, the transistor no longer functions as a regulator and because much tighter compensation is obtained.

The circuit in *Figure 5* uses pre-regulation to solve this problem. The added reference diode has a low breakdown so that the minimum operating voltage of the op amp is unrestricted. Because of the low breakdown, the drop across R3 can no longer be considered constant. But it will vary linearly with temperature, so this is of no consequence. The fact that this reference can be used for other functions should not be overlooked because a regulated voltage is frequently required in designs using op amps.

In *Figure 5,* a divider is used so that the resistor feeding the compensating current to the op amp can be reduced. There will be an error current developed for any offset voltage change across R6. This should not be a problem with the LM11 because of its low offset voltage. But for tight compensation, mismatch in the temperature characteristics of R4 and R5 must be considered.

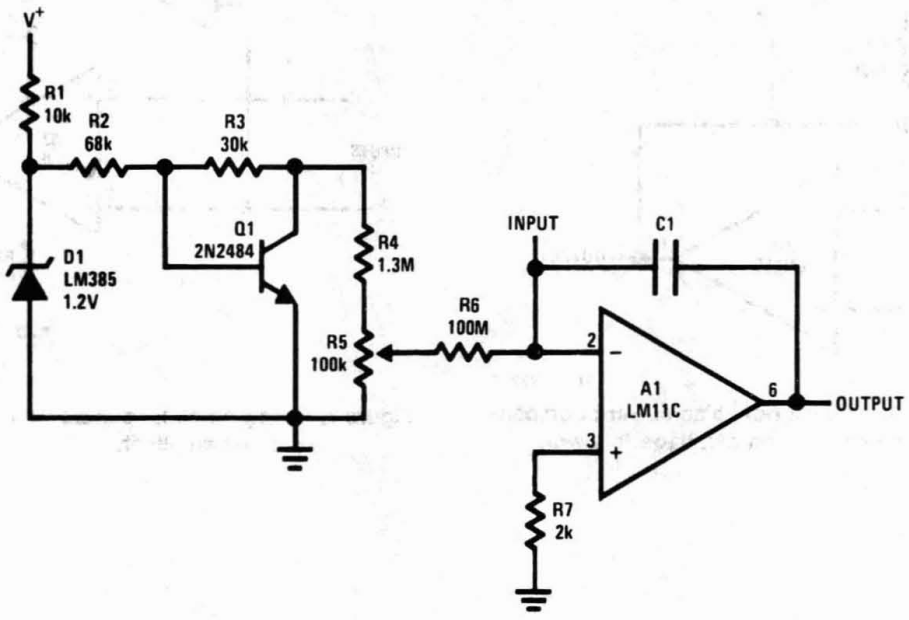

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Figure 5. Bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.

Bias current compensation is more difficult for non-inverting amplifiers because the common-mode voltage varies. With a voltage follower, everything can be bootstrapped to the output and powered by a regulated current source, as shown in *Figure 6.* The LM334 is a temperature sensor. It regulates against voltage changes and its output varies linearly with temperature, so it fits the bill.

Although the LM334 can accommodate voltage changes fast enough to work with the LM11, it is not fast enough for the high-speed circuits to be described. But compensation can still be obtained by using the zener diode pre-regulator bootstrapped to the output and powered by either a resistor or FET current source. The LM385 fits well here because both the breakdown voltage and minimum operating current are low.

With ordinary op amps, the collector base voltage of the input transistors varies with the common-mode voltage. A 50% change in bias current over the common-mode range is not unusual, so compensating the bias current of a follower has limited value. However, the bootstrapped input stage of the LM11 reduces this to about 2 pA for a ±20V common-mode swing, giving a $2 \times 10^{13}\Omega$ common-mode input resistance.

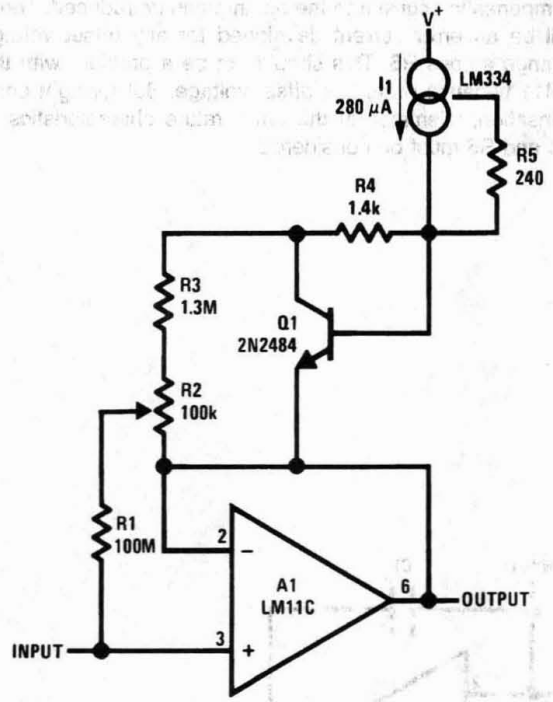


Figure 6. This circuit shows how bias current compensation can be used on a voltage follower.

fast amplifiers

A precision DC amplifier, although slow, can be used to stabilize the offset voltage of a less precise fast amplifier. As shown in *Figure 7,* the slow amplifier senses the voltage across the input terminals and supplies a correction signal to the balance terminals of the fast amplifier. The LM11 is particularly interesting in this respect as it does not degrade the input bias current of the composite even when the fast amplifier has a FET input.

Surprisingly, with the LM11, this will work for both inverting and non-inverting connections because its common-mode slew recovery is a lot faster than that of the main loop. This was accomplished, even with circuitry running under 100 nA, by proper clamping and by bootstrapping of internal stray capacitances.

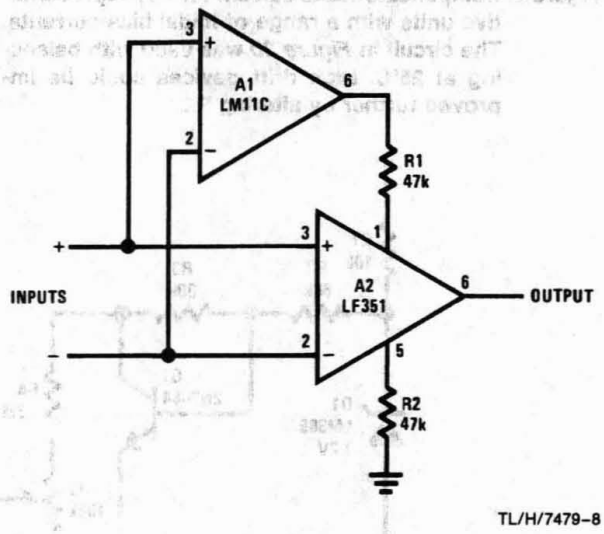


Figure 7. A slow amplifier can be used to null the offset of a fast amplifier.

An optimized circuit for the inverting amplifier connection is shown in *Figure 8.* The LM11 is DC coupled to the input and drives the balance terminals of the fast amplifier. The fast amplifier is AC coupled to the input and drives the output. This isolates FET leakage from the input circuitry.

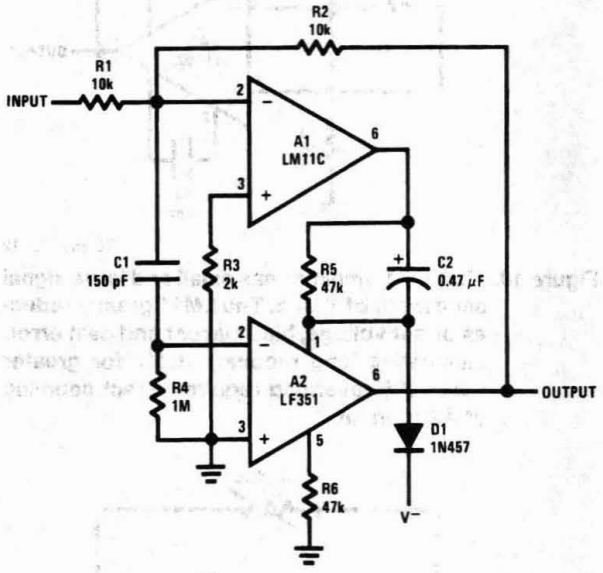
As can be seen, the method of coupling into the balance terminals will vary depending on the internal configuration of the fast amplifier. If the quiescent voltage on the balance terminals is beyond the output swing of the LM11, a differential coupling must be used, as in *Figure 8a.* A lead capacitor, C2, reduces the AC swing required at the LM11 output. The clamp diode, D1, insures that the LM11 does not overdrive the fast amplifier in slew.

If the quiescent voltage on the balance terminals is such that the LM11 can drive directly, the circuit in *Figure 8b* can be used. A clamp diode from the other balance terminal to internal circuitry of the LM11 keeps the output from swinging too far from the null value, and a resistor may be required in series with its output to insure stability.

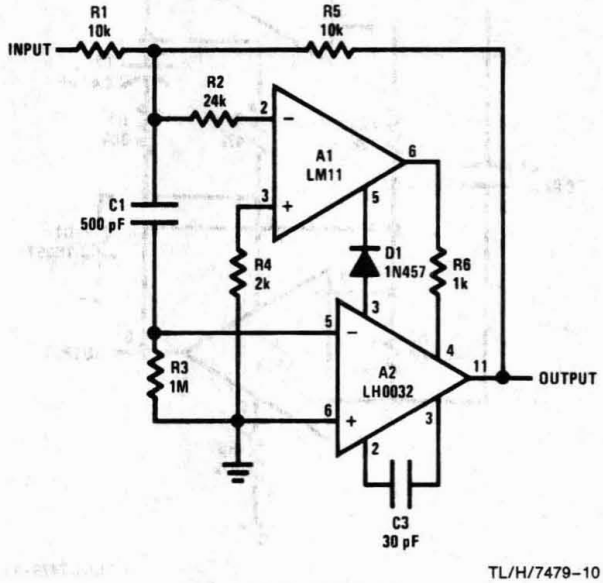
Measurements indicate that the slew rate of the fast amplifier is unimpaired, as is the settling time to 1 mV for a 20V output excursion. If the composite amplifier is overdriven so that the output saturates, there will be an added recovery delay because the coupling capacitor to the fast amplifier takes on a charge with the summing node off ground. Therefore, C1 should be made as small as possible. But going below the values given may introduce gain error.

If the bias current of the fast amplifier meets circuit requirements, it can be direct-coupled to the input. In this case, offset voltage is improved, not bias current. But overload recovery can be reduced. The AC coupling to the fast-amplifier input might best be eliminated for limited-temperature-range operation.

This connection also increases the open-loop gain beyond that of the LM11, particularly since two-pole compensation can be effected to reduce AC gain error at moderate frequencies. The DC gains measured showed something in excess of 140 dB.



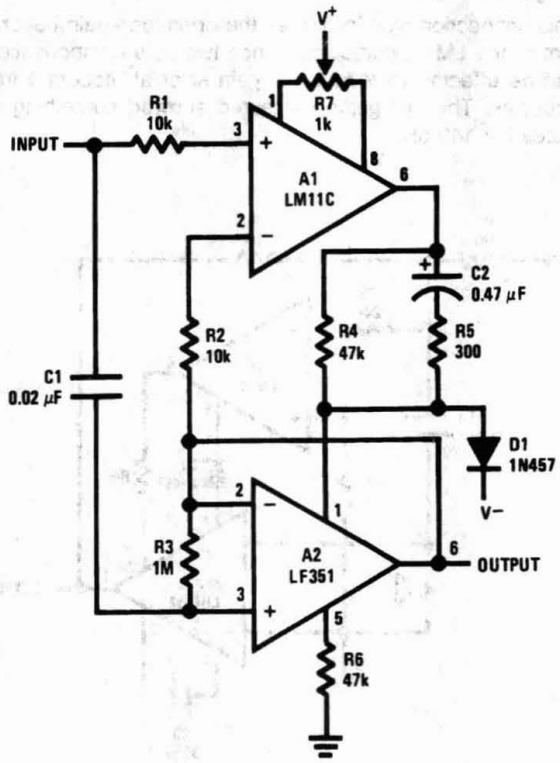
a. with standard BI-FET



b. with fast hybrid

Figure 8. These inverters have bias current and offset voltage of LM11 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 μs. Excess overload-recovery delay can be eliminated by directly coupling the FET amplifier to summing node.

A voltage-follower connection is given in *Figure 9.* The coupling circuitry is similar, except that R5 was added to eliminate glitches in slew. Overload involves driving the fast amplifier outside its common-mode range and should be avoided by limiting the input. Thus, AC coupling the fast amplifier is less a problem. But the repetition frequency of the input signal must also be limited to 10 kHz for ±10V swing. Higher frequencies produce a DC error, believed to result from rectification of the input signal by the voltage sensitive input capacitance of the FET amplifier used. A fast bipolar amplifier like the LM118 should work out better in this respect. To avoid confusion, it should be emphasized that this problem is related to repetition frequency rather than rise time.



TL/H/7479–11

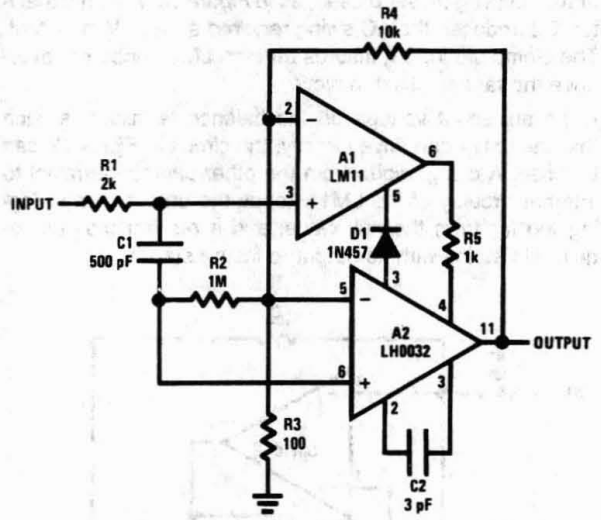
Figure 9. Follower has 10 μs settling to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is AC coupled to input. The circuit does not behave well if common-mode range is exceeded.

A precision DC amplifier with a 100 MHz gain-bandwidth product is shown in *Figure 10.* It has reasonable recovery (~7 μs) from a 100% overload; but beyond that, AC coupling to the fast amplifier causes problems. Alone, the gain error and thermal feedback of the LH0032 are about 20 mV, input referred, for ±10V output swing. Adding the LM11 reduces this to microvolts.

picoammeter

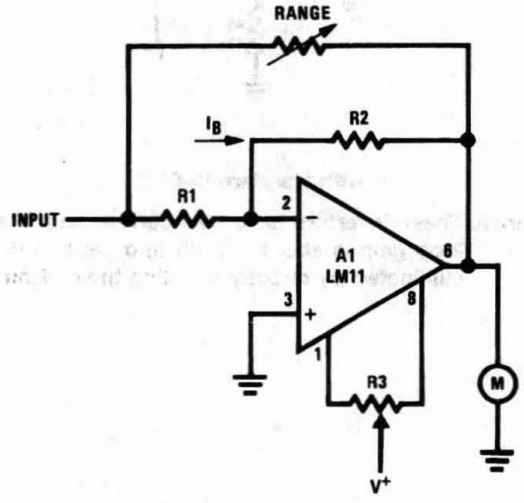
Ideally, an ammeter should read zero with no input current and have no voltage drop across its inputs even with full-scale deflection. Neither should spurious indications nor inaccuracy result from connecting it to a low impedance. Meeting all these requirements calls for a DC amplifier, and one in which both bias current and offset voltage are controlled.

The summing amplifier connection is best for measuring current, because it minimizes the voltage drop across the input terminals. However, when the inputs are shorted, the output state is indeterminate because of offset voltage. Adding degeneration as shown in *Figure 11* takes care of this problem. Here, R2 is the feedback resistor for the most sensitive range, while R1 is chosen to get the meter deflection out of the noise with a shorted input. Adding the range resistor, as shown, does not affect the degeneration, so that there is minimal drop across the input for full-scale on all ranges.



TL/H/7479–12

Figure 10. This 100X amplifier has small and large signal bandwidth of 1 MHz. The LM11 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.



TL/H/7479–13

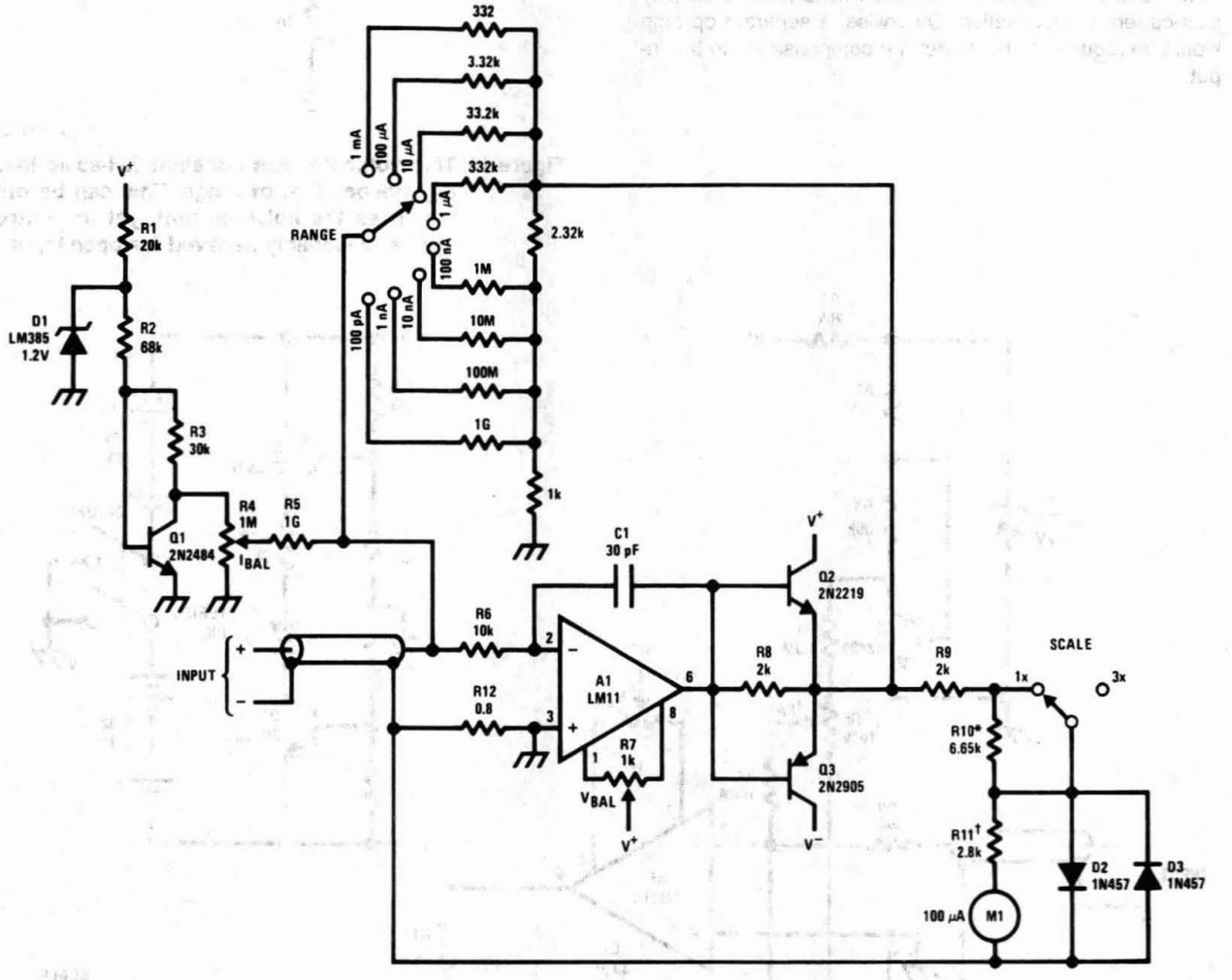
Figure 11. An ammeter that has constant voltage drop across its input at full-scale, no matter what the range. It can have a reasonably-behaved output even with shorted inputs, yet a maximum drop of ten times the op amp noise voltage.

The complete meter circuit in *Figure 12* uses a different scheme. A floating supply is available so that the power ground and the signal ground can be separated with R12. At full-scale, the meter current plus the measured current flow through this resistor, establishing the degeneration. This method has the advantage of allowing even-value range resistors on the lower ranges but increases degeneration as the measured current approaches the meter current.

Bias-current compensation is used to increase the meter sensitivity so there are two zeroing adjustments; current balancing, that is best done on the most sensitive range where it is needed, and voltage balancing that should be done with the inputs shorted on a range below 100 μA, where the degeneration is minimal.

With separate grounds, error could be made dependent on offset current. This would eliminate bias-current compensation at the expense of more complicated range switching.

The op amp input has internal, back-to-back diodes across it, so R6 is added to limit current with overloads. This type of protection does not affect operation and is recommended whenever more than 10 mA is available to the inputs. The output buffers are added so that input overloads cannot drag down the op amp output on the least-sensitive range, giving a false meter indication. These would not be required if the maximum input current did not approach the output current limit of the op amp.



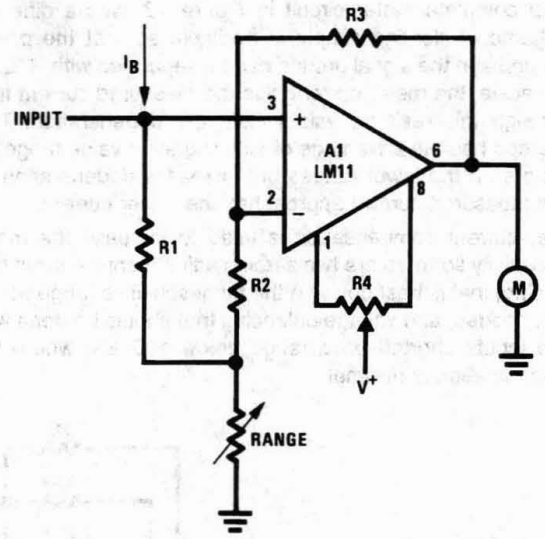
TL/H/7479–14

Figure 12. Current meter ranges from 100 pA to 3 mA, full-scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.

millivoltmeter

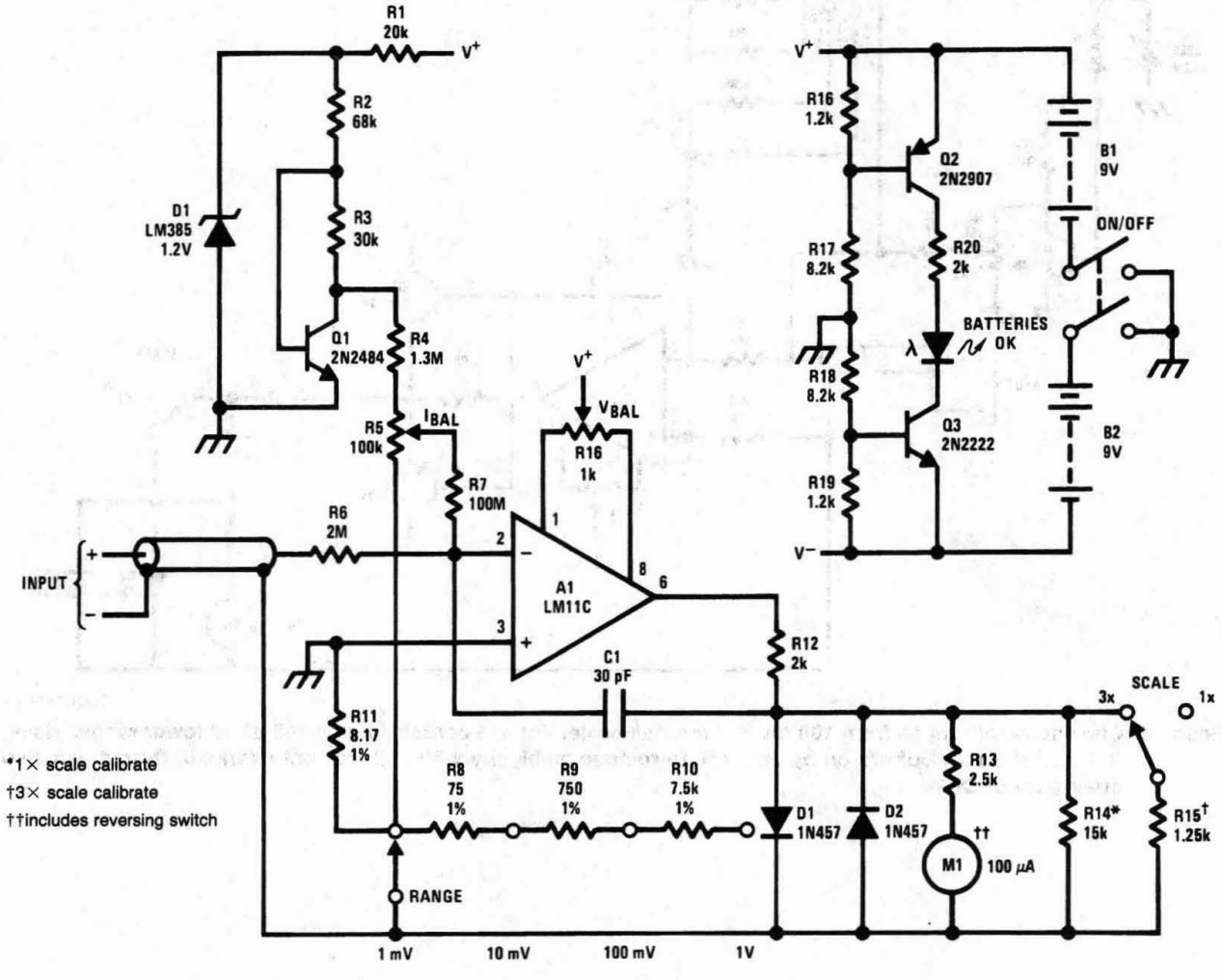
An ideal voltmeter has requirements analogous to those discussed for the ammeter, and *Figure 13* shows a circuit that will satisfy them. In the most-sensitive position, the range resistor is zero and the input resistance equals R1. As voltage measurement is desensitized by increasing the range resistor, the input resistance is also increased, giving the maximum input resistance consistent with zero stability with the input open. Thus, at full-scale, the source will be loaded by whatever multiple of the noise current is required to give the desired open-input zero stability.

This technique is incorporated into the voltmeter circuit in *Figure 14* to give a 100 MΩ input resistance on the 1 mV scale rising to 300 GΩ on the 3V scale. The separation of power and signal grounds has been used here to simplify bias-current compensation. Otherwise, a separate op amp would be required to bootstrap the compensation to the input.



TL/H/7479–15

Figure 13. This voltmeter has constant full-scale loading independent of range. This can be only ten times the noise current, yet the output will be reasonably behaved for open input.

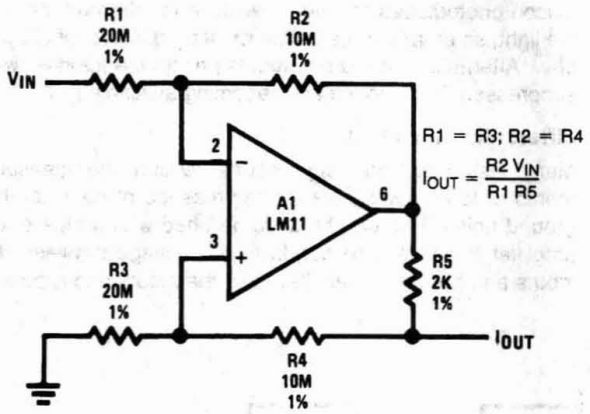


TL/H/7479–16

Figure 14. High input impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full-scale. Reference could be used to make direct reading linear ohmmeter.

The input resistor, R6, serves two functions. First, it protects the op amp input in the event of overload. Second, it insures that an overload will not give a false meter indication until it exceeds a couple hundred volts.

Since the reference is bootstrapped to the input, this circuit is easily converted into a linear, direct-reading ohmmeter. A resistor from the top of D1 to the input establishes the measurement current so that the voltage drop is proportional to the resistance connected across the input.



TL/H/7479–17

Figure 15. Output resistance of this voltage/current converter depends both on high value feedback resistors and their matching.

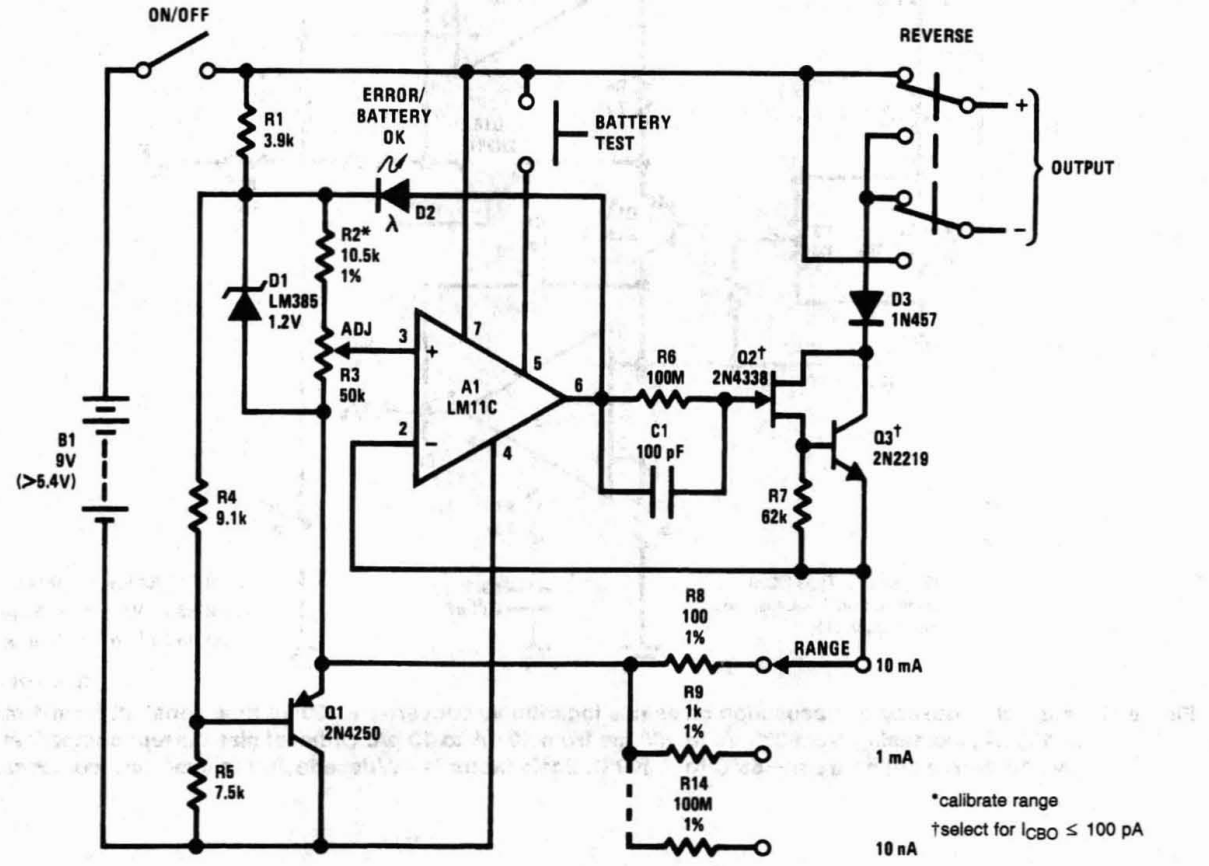
current sources

The classical op amp circuit for voltage-to-current conversion is shown in *Figure 15.* It is presented here because the output resistance is determined by both the matching and the value of the feedback resistors. With the LM11, these resistors can be raised while preserving DC stability.

While the circuit in *Figure 15* can provide bipolar operation, better performance can be obtained with fewer problems if a unipolar output is acceptable. A complete, battery-powered current source suitable for laboratory use is given in *Figure 16* to illustrate this approach. The op amp regulates the voltage across the range resistors at a level determined by the voltage on the arm of the calibrated potentiometer, R3. The voltage on the range resistors is established by the current through Q2 and Q3, which is delivered to the output.

The reference diode, D1, determines basic accuracy. Q1 is included to insure that the LM11 inputs are kept within the common-mode range with diminishing battery voltage. A light-emitting diode, D2, is used to indicate output saturation. However, this indication cannot be relied upon for output-current settings below about 20 nA unless the value of R6 is increased. The reason is that very low currents can be supplied to the range resistors through R6 without developing enough voltage drop to turn on the diode.

If the LED illuminates with the output open, there is sufficient battery voltage to operate the circuit. But a battery-test switch is also provided. It is connected to the base of the op amp output stage and forces the output toward V^+.



TL/H/7479–18

Figure 16. Precision current source has 10 nA to 10 mA ranges with output compliance of 30V to −5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates output saturation.

Bias current compensation is not used because low-range accuracy is limited by the leakage currents of Q2 and Q3. As it is, these parts must be selected for low leakage. This should not be difficult because the leakage specified is determined by test equipment rather than device characteristics. It should be noted in making substitutions that Q2 was selected for low pinch-off voltage and that Q3 may have to dissipate 300 mW on the high-current range. Heating Q3 on the high range could increase leakage to where the circuit will not function for a while when switched to the low range.

logarithmic converter

A logarithmic amplifier that can operate over an eight-decade range is shown in *Figure 17.* Naturally, bias current compensation must be used to pick up the low end of this range. Leakage of the logging transistors is not a problem as long as Q1A is operated at zero collector-base voltage. In the worst case, this may require balancing the offset voltage of A1. Non-standard frequency compensation is used on A1 to obtain fairly uniform response time, at least at the high end of the range. The low end might be improved by optimizing C1. Otherwise, the circuit is standard.

light meter

This logging circuit is adapted to a battery-powered light meter in *Figure 18.* An LM10, combined op amp and reference, is used for the second amplifier and to provide the regulated voltage for offsetting the logging circuit and powering the bias current compensation. Since a meter is the output indicator, there is no need to optimize frequency compensation. Low-cost single transistors are used for logging since the temperature range is limited. The meter is protected from overloads by clamp diodes D2 and D3.

Silicon photodiodes are more sensitive to infrared than visible light, so an appropriate filter must be used for photography. Alternately, gallium-arsenide-phosphide diodes with suppressed IR response are becoming available.

differential amplifiers

Many instrumentation applications require the measurements of low-level signals in the presence of considerable ground noise. This can be accomplished with a differential amplifier because it responds to the voltage between the inputs and rejects signals between the inputs and ground.

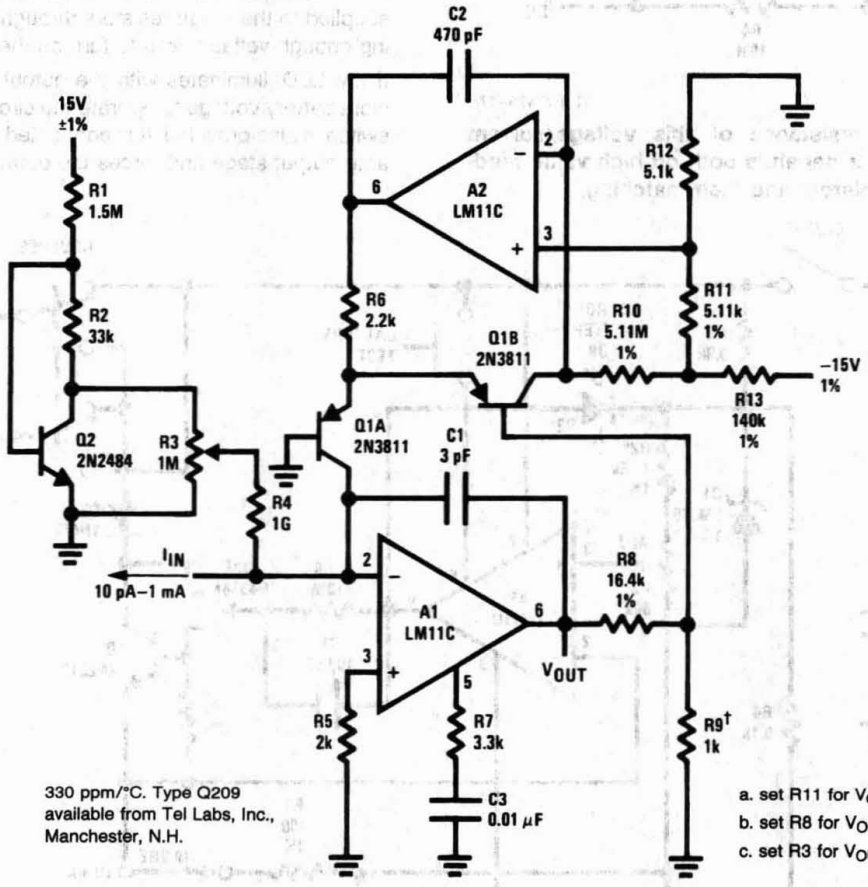


Figure 17. Unusual frequency compensation gives this logarithmic converter a 100 μs time constant from 1 mA down to 100 nA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to +100°C. Scale factor is 1V/decade and temperature compensated.

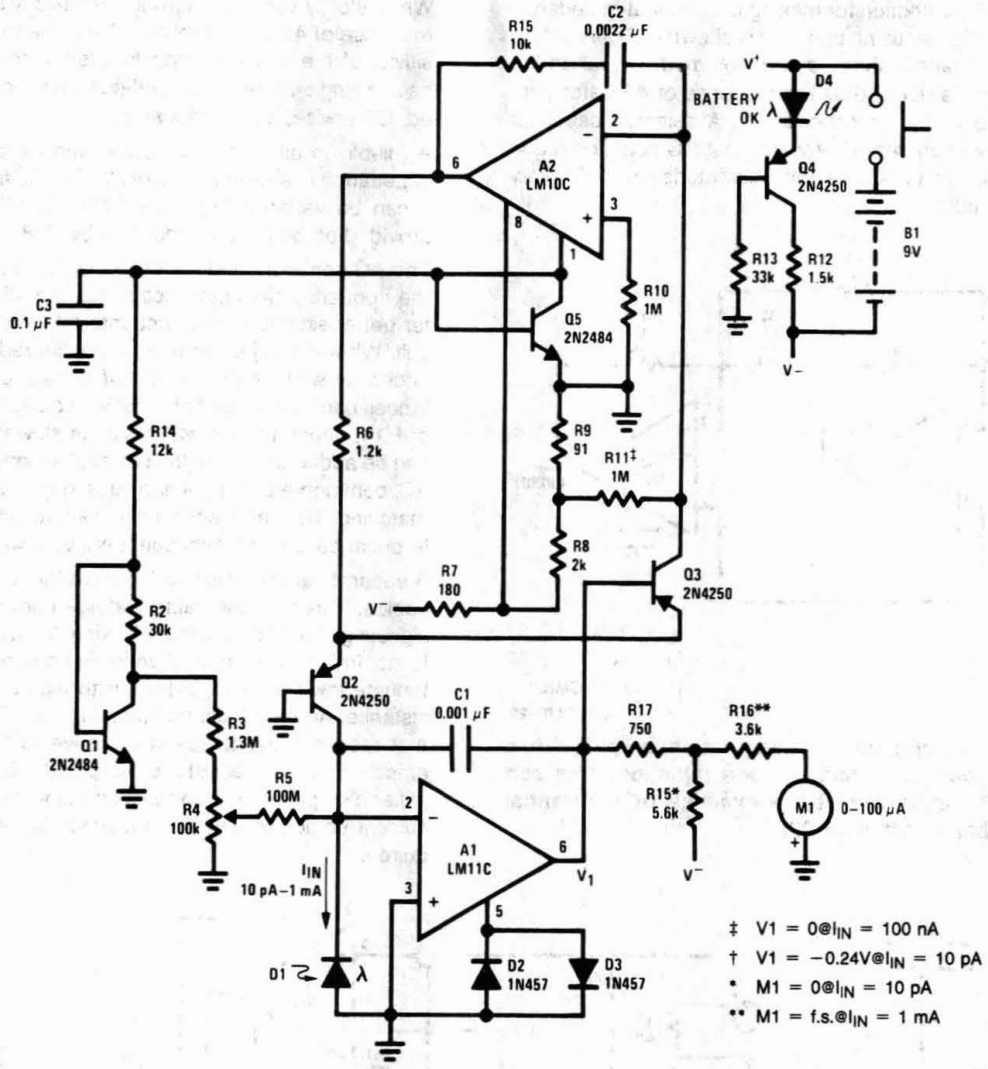


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Figure 18. Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.

Figure 19 shows the classic op amp differential amplifier connection. It is not widely used because the input resistance is much lower than alternate methods. But when the input common-mode voltage exceeds the supply voltage for the op amp, this cannot be avoided. At least with the LM11, large feedback resistors can be used to reduce loading without affecting DC accuracy. The impedances looking into the two inputs are not always the same. The values given equalize them for common-mode signals because they are usually larger. With single-ended inputs, the input resistance on the inverting input is R1, while that on the non-inverting input is the sum of R2, R4 and R5.

Provision is made to trim the circuit for maximum DC and AC common-mode rejection. This is advised because well matched high-value resistors are hard to come by and because unbalanced stray capacitances can cause severe deterioration of AC rejection with such large values. Particular attention should be paid to resistor tracking over temperature as this is more of a problem with high-value resistors. If higher gain or gain trim is required, R6 and R7 can be added.

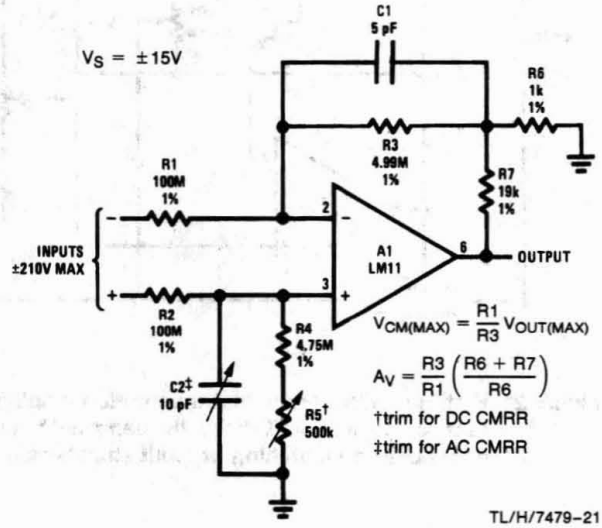

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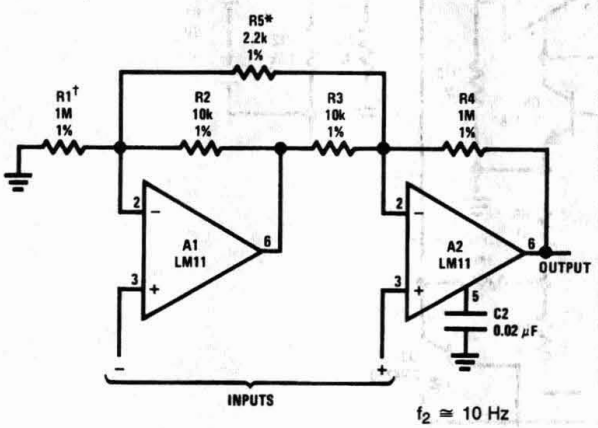
Figure 19. This differential amplifier handles high input voltages. Resistor mismatches and stray capacitances should be balanced out for best common-mode rejection.

The simplest connection for making a high-input-impedance differential amplifier using op amps is shown in *Figure 20.* Its main disadvantage is that the common-mode signal on the inverting input is delayed by the response of A1 before being delivered to A2 for cancellation. A selected capacitor across R1 will compensate for this, but AC common-mode rejection will deteriorate as the characteristics of A1 vary with temperature.



$f_2 \cong 10$ Hz

*gain set

†trim for DC CMRR

TL/H/7479–22

Figure 20. Two-op-amp instrumentation amplifier has poor AC common-mode rejection. This can be improved at the expense of differential bandwidth with C2.

When slowly varying differential signals are of interest, the response of A2 can be rolled off with C2 to reduce the sensitivity of the circuit to high frequency common-mode signals. If single-resistor gain setting is desired, R5 can be added. Otherwise, it is unnecessary.

A full-blown differential amplifier with extremely high input impedance is shown in *Figure 21.* Gain is fixed at 1000, but it can be varied with R10. Differential offset balancing is provided on both input amplifiers by R18.

The AC common-mode rejection is dependent on how well the frequency characteristics of A2 and A3 match. This is a far better situation than encountered with the previous circuit. When AC rejection must be optimized, amplifier differences as well as the effects of unbalanced stray capacitances can be compensated for with a capacitor across R13 or R14, depending on which side is slower. Alternately, C1 can be added to control the differential bandwidth and make AC common-mode rejection less dependent on amplifier matching. The value shown gives approximately 100 Hz differential bandwidth, although it will vary with gain setting.

A separate amplifier is used to drive the shields of the input cables. This reduces cable leakage currents and spurious signals generated from cable flexing. It may also be required to neutralize cable capacitance. Even short cables can attenuate low-frequency signals with high enough source resistance. Another balance potentiometer, R8, is included so that resistor mismatches in the drive to the bootstrapping amplifier can be neutralized. Adding the bootstrapping amplifier also provides a connection point, as shown, for bias-current compensation if the ultimate in performance is required.

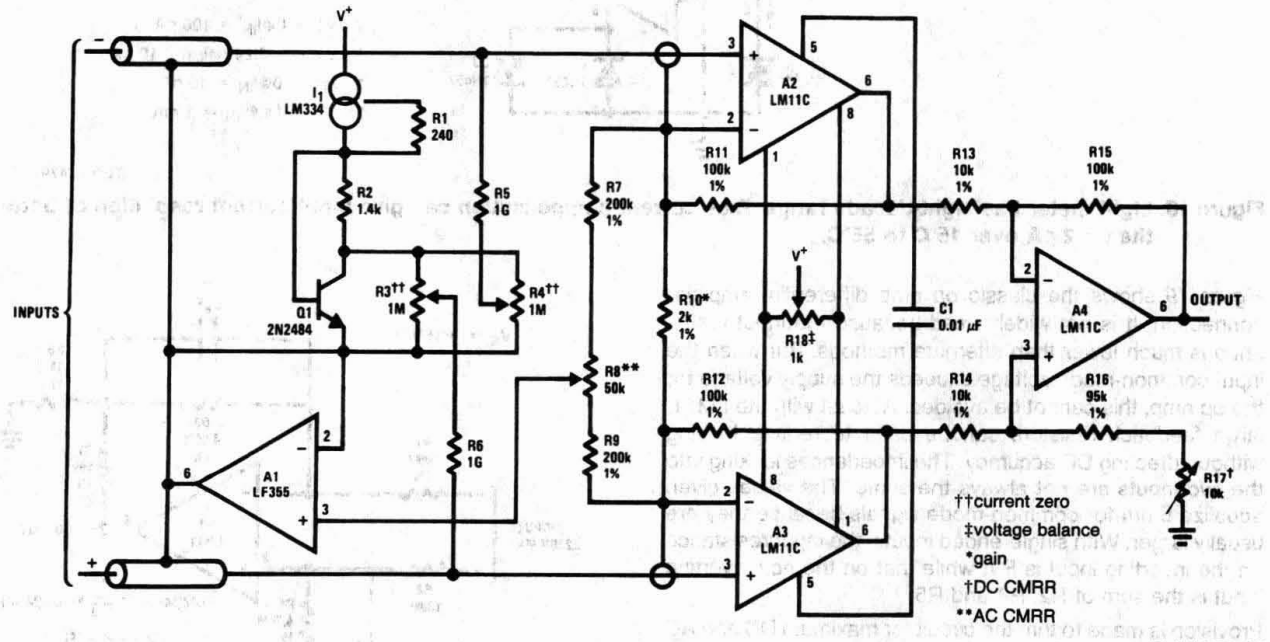


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Figure 21. High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.

As can be seen in *Figure 22,* connecting the input amplifiers as followers simplifies the circuit considerably. But single resistor gain control is no longer available and maximum bandwidth is less with all the gain developed by A3. Resistor matching is more critical for a given common-mode rejection, but AC matching of the input amplifier is less a problem. Another method of trimming AC common-mode rejection is shown here.

Integrator reset

When pursuing the ultimate in performance with the LM11, it becomes evident that components other than the op amp can limit performance. This can be the case when semiconductor switches are used. Their leakage easily exceeds the bias current when elevated temperatures are involved.

The integrator with electrical reset in *Figure 23* gives a solution to this problem. Two switches in series are used to shunt the integrating capacitor. In the off state, one switch, Q2, disconnects the output while the other, Q1, isolates the leakage of the first. This leakage is absorbed by R3. Only the op amp offset appears across the junctions of Q1, so its leakage is reduced by two orders of magnitude.

A junction FET could be used for Q1 but not for Q2 because there is no equivalent to the enhancement mode MOSFET. The gate of a JFET must be reverse biased to turn it off and leakage on its output cannot be avoided.

MOS switches with gate-protection diodes are preferred in production situations as they are less sensitive to damage from static charges in handling. If used, D1 and R2 should be inlcuded to remove bias from the internal protection diode when the switch is off.

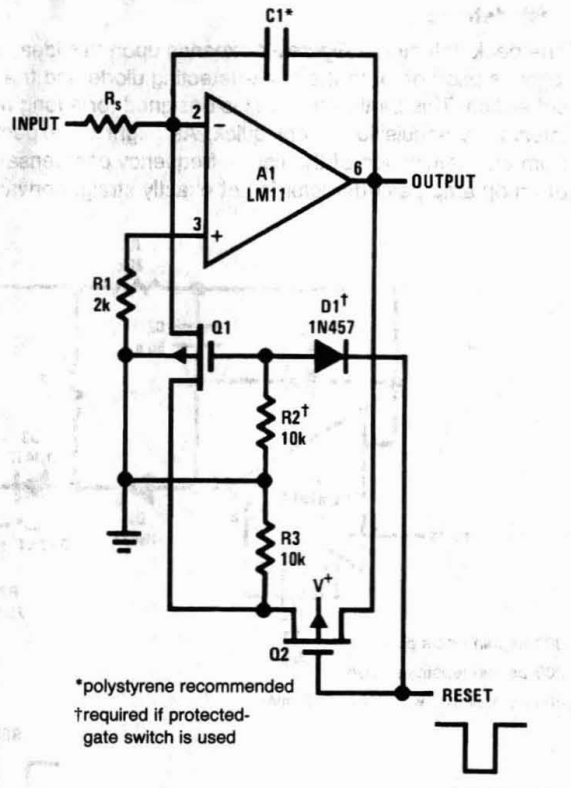

Figure 23. Reset is provided for this inegrator and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.

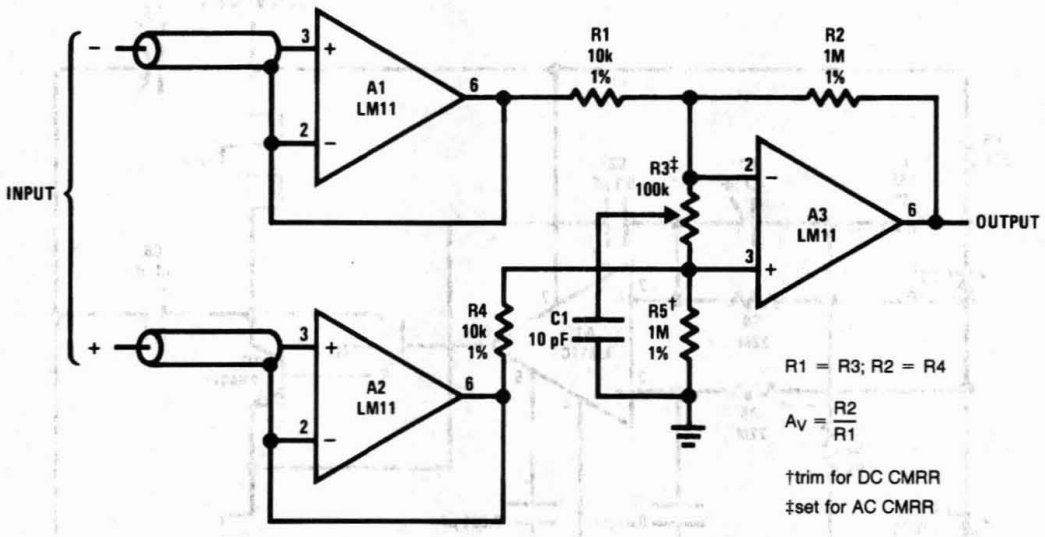

Figure 22. For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A3 must also have low drift.

peak detector

The peak detector in *Figure 24* expands upon this idea. Isolation is used on both the peak-detecting diode and the reset switch. This particular circuit is designed for a long hold interval so acquisition is not quick. As might be expected from an examination of the figure, frequency compensation of an op amp peak detector is not exactly straightforward.

oven controller

The LM11 is quite useful with slow servo systems because impedance levels can be raised to where reasonable capacitor values can be used to effect loop stabilization without affecting accuracty. An example of this is shown in *Figure 25*. This is a true proportional controller for a crystal oven.

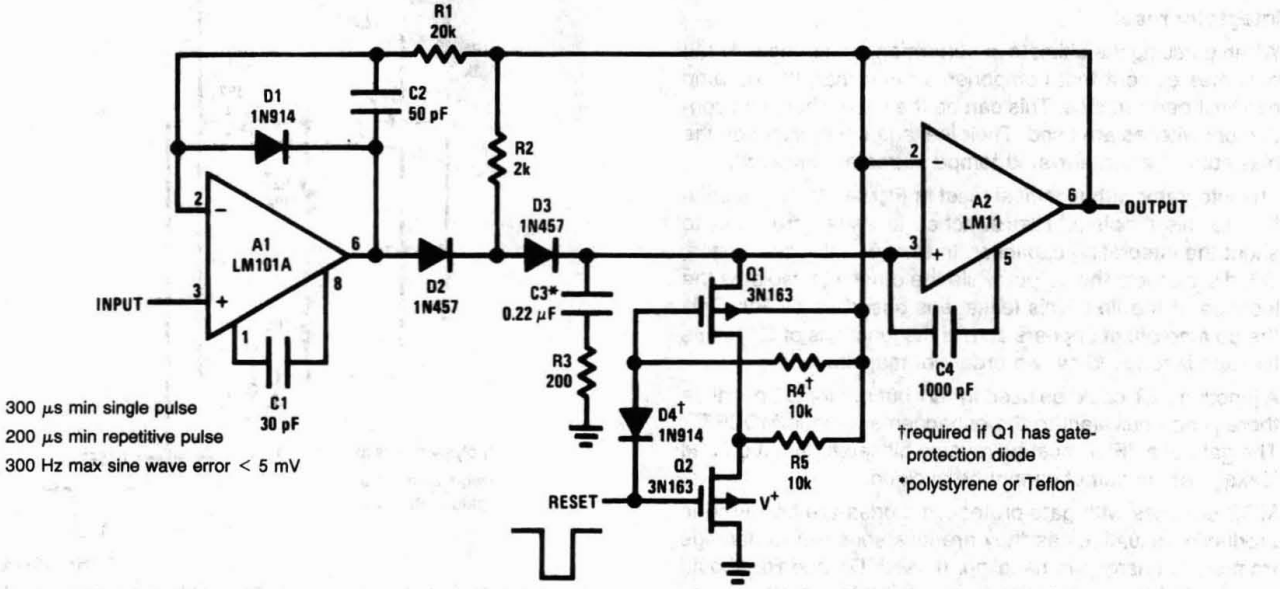

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Figure 24. A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.

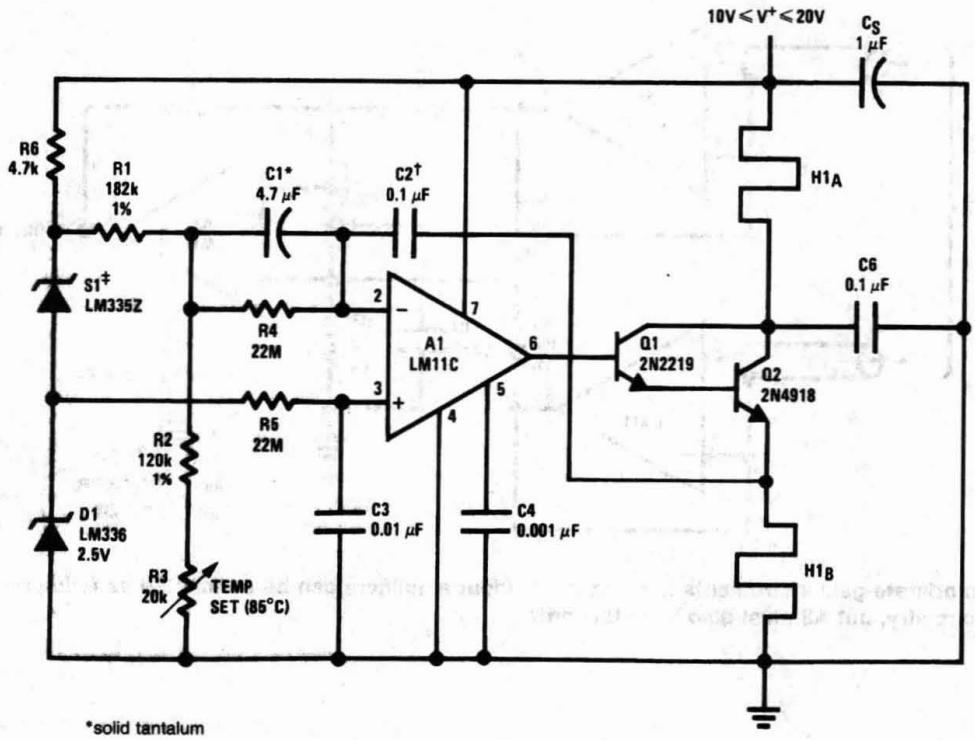

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FIGURE 25. Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.

Temperature sensing is done with a bridge, one leg of which is formed by an IC temperature sensor, S1, and a reference diode, D1. Frequency stabilization is done with C2 providing a lag that is finally broken out by C1. If the control transistor, Q2, is put inside the oven for maximum heating efficiency, some level of regulation is suggested for the heater supply when precise control is required. With Q2 in the oven, abrupt supply changes will alter heating, which must be compensated for by the loop. This takes time, causing a small temperature transient.

Because the input bias current of the LM11 does not increase with temperature, it can be installed inside the oven for best performance. In fact, when an oven is available in a piece of equipment, it would be a good idea to put all critical LM11s inside the oven if the temperature is less than 100°C.

ac amplifier

Figure 26 shows an op amp used as an AC amplifier. It is unusual in that DC bootstrapping is used to obtain high input resistance without requiring high-value resistors. In theory, this increases the ouput offset because the op amp offset voltage is multiplied by the resistance boost.

But when conventional resistor values are used, it is practical to include R5 to eliminate bias-current error. This gives less output offset than if a single, large resistor were used. C1 is included to reduce noise.

standard cell buffer

The accuracy and lifetime of a standard cell deteriorate with loading. Further, with even a moderate load transient, recovery is measured in minutes, hours or even days. The circuit in *Figure 27* not only buffers the standard cell but also disconnects it in the event of malfunction.

The fault threshold is determined by the gate turn-on voltage of Q1. As the voltage on the gate approaches the threshold either because of low battery voltage or excessive output loading, the MOS switch will begin to turn off. At the turn off threshold, the output voltage can rise because of amplifier bias current flowing through the increasing switch resistance. Therefore, a LED indicator is included that extin-

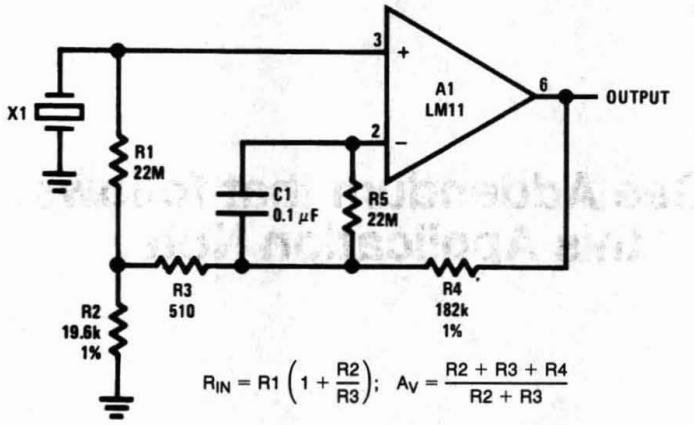

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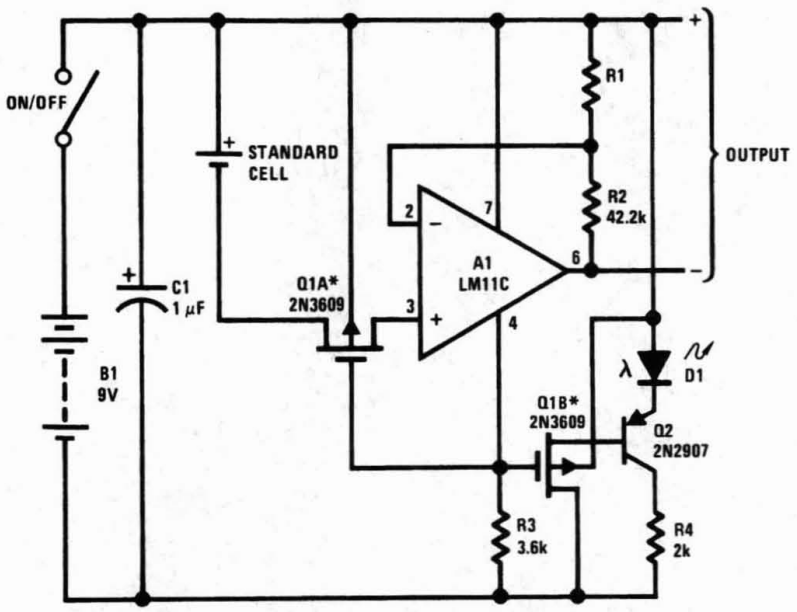
Figure 26. A high input impedance AC amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.



TL/H/7479–29

*cannot have gate protection diode; $V_{TH} > V_{OUT}$

Figure 27. Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.

guishes as the fault condition is approached. The MOS threshold should be higher than the buffer output so that he disconnect and error indicator operates before the output saturates.

conclusions

Although the LM11 does not provide the ultimate in performance in either offset voltage or bias current for nominal room temperature applications, the combination offered is truly noteworthy. With significant temperature excursions, the results presented here are much more impressive. With full-temperature-range operation, this device does represent the state of the art when high-impedance circuitry is involved.

Combining this new amplifier with fast op amps to obtain the best features of both is also interesting, particularly since the composite works well in both the inverting and non-inverting modes. However, making high-impedance circuits fast is no simple task. If higher temperatures are not involved, using the LM11 to reduce the offset voltage of a FET op amp without significantly increasing bias current may be all that is required.

An assortment of measurement and computational circuits making use of the unique capabilities of this IC were presented. These circuits have been checked out and the results should be of some value to those working with high impedances. These applications are by no means all-inclusive, but they do show that an amplifier with low input current can be used in a wide variety of circuits.

Although emphasis was on high-performance circuits requiring adjustments, the LM11 will see widest usage in less demanding applications where its low initial offset votlage and bias current can eliminate adjustments.

acknowledgement

The authors would like to thank Dick Wong for his assistance in building and checking out the applications described here.

***See Addendum that follows this Application Note.**

Reducing DC Errors in Op Amps

National Semiconductor
Technical Paper 15

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Abstract. *An IC op amp design that reduces bias currents below 100 pA over a −55°C to +125°C temperature range is discussed. Super-gain bipolar transistors with on-wafer trimming are used, providing low offset voltage and drift. The key to low bias current is the control of high temperature leakage currents along with the development of reasonably accurate nanoampere current sources with low parasitic capacitance.*

introduction

A bipolar replacement for the LM108 [1] drastically reduces offset voltage, bias current and temperature drift. This design, the LM11, does not depend on new technology. Instead, the improvements result from a better understanding of transistor behavior, new circuit techniques and the application of proven offset trimming methods. Table I summarizes the results obtained. The combination of low offset voltage and low bias current is unique to IC op amps, while the performance at elevated temperatures represents an advance in the state of the art.

TABLE I. Input error terms of the LM11 show an improvement over FET op amps even at room temperature. There is little degradation in performance from −55°C to 125°C. Other important specifications are somewhat better than LM108A.

Parameter	$T_j = 25°C$		$-55°C \le T_j \le +125°C$	Units
	Typ	Max	Max	
Input Offset Voltage	0.1	0.3	0.6	mV
Input Offset Current	0.5	10	30	pA
Input Bias Current	25	50	150	pA
Offset Voltage Drift	1		3	μV/°C
Offset Current Drift	20			fA/°C
Bias Current Drift	0.5		0.5	pA/°C

junction FETs

At first glance, field effect transistors seem to be the ideal input stage for an op amp, mainly because they have a low gate current, independent of their operating current. Practically, they do provide an attractive combination of performance characteristics in a relatively simple design. But there are serious shortcomings.

For one, FETs do not match as well as bipolar devices: the offset voltage is at least an order of magnitude worse. Laser trimming can compensate for this to some extent. But with FETs, low offset voltage does not guarantee low drift, as it does with bipolars. FETs are also sensitive to mechanical strains and subject to offset shifts during assembly or with temperature cycling.

Typically, long term stability is about 100 μV/year, although this can go to 1 mV/year with no prior warning in early life. This contrasts to a 10 μV/year long term stability for bipolar pairs.

Lastly, although the input current of FETs is low at room temperature, it doubles for every 10°C increase. This, coupled with high offset voltage drift, makes FETs much less attractive as operating temperature is increased.

MOS FETs

Field effect transistors, with a metal gate and oxide insulation, give the ultimate in low input current. Practically, this advantage disappears when diodes are included to protect the gate from static charges encountered in normal handling. Further, the offset voltage problems of JFETs go double for MOS FETs. They are also subject to offset shifts due to contamination.

Interesting designs are on the horizon for various chopper-stabilized complementary MOS ICs. These solve most offset voltage problems, but not that of input leakage current. Even at moderate temperatures, this input current will seriously degrade the low offset voltage and drift even with relatively low source resistances. Chopper-stabilized amplifiers have added problems with overload recovery and noise, especially with high source impedances. These problems have limited solutions, but chopper stabilization is not usually suitable for general purpose applications.

bipolar op amps

Offset voltage, its drift or long term stability has not been a serious problem with bipolar-input op amps. Such techniques as cross-coupling or zener-zap trimming have reduced offset voltage to 25 μV in production. The real problem has been bias current. The LM108, introduced in 1968, has represented the state of the art in low bias currents for standard bipolar devices. At 3 nA, maximum over temperature, the bias current is lower than FETs above 85°C.

A Darlington version of the LM108, the LM216, provided bias currents in the 50 pA range; but this design was seriously marred by high offset voltage, drift, excessive low frequency noise and anomalous leakage currents at higher temperatures.

Improvements in this design were thwarted by the inability to provide nanoampere bleed currents to stabilize the Darlington input and the erroneous belief that uncontrollable surface states created the anomalous leakage.

a new design

With bipolar transistors, there is a tradeoff between current gain and breakdown voltage. Super-gain transistors are devices that have been diffused for maximum current gain at the expense of breakdown voltage (which is typically a couple volts for a current gain of 5000). These low voltage transistors can be operated in a cascode connection with standard transistors to give a composite device with both high gain and breakdown voltage.

Figure 1 shows a modified Darlington input stage for a super-gain op amp. Common base standard transistors (Q5 and Q6, drawn with a wider base) are bootstrapped to the super-gain input transistors so that the latter are operated at near zero collector base voltage. In addition to permitting the use of super-gain inputs, this connection also isolates the input transistors from common-mode variations, increasing common-mode rejection.

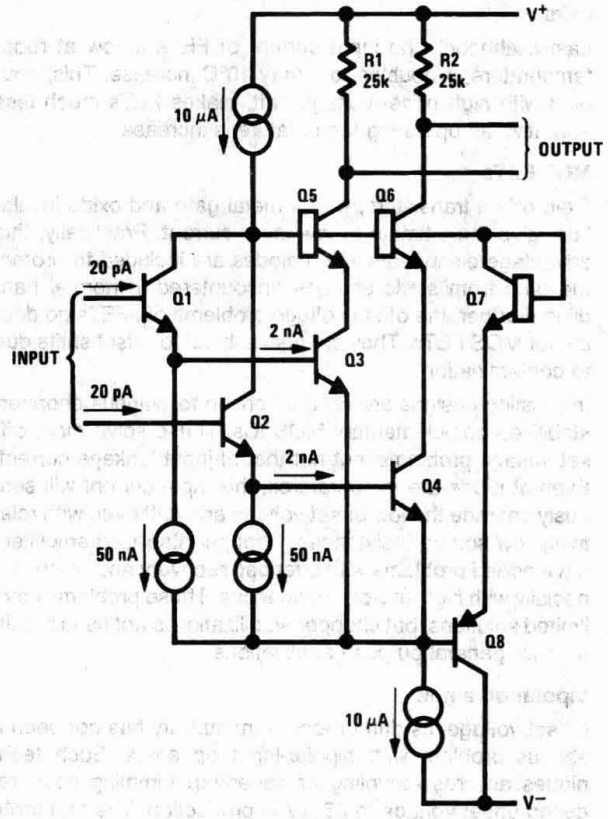

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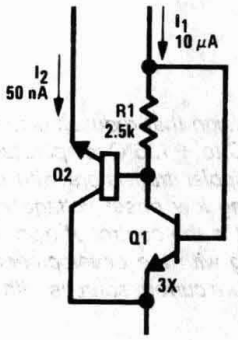
Figure 1. Bootstrapped input stage using super-gain transistors in modified-Darlington connection. The objectionable characteristics of the Darlington are virtually eliminated by operating the input transistors at a much larger current than the base current of the transistors they are driving.

The usual problems with the Darlington connection are avoided by providing a bleed current that operates the input transistors, Q1 and Q2, at a current much higher than the base current of the transistors they are driving, Q3 and Q4. This is necessary because the base currents are not that well matched, especially over temperature, and have excess low frequency noise.

a nanoampere current source

A circuit that generates the 50 nA bleed current is shown in *Figure 2*. A super-gain transistor operated in the forward mode is used to bias a standard transistor in the reverse mode. The reverse connection is used because the capacitance of an ordinary collector tub would reduce the common-mode slew rate from 2 V/μs to 0.02 V/μs.



$$I_2 = \frac{h_{fe2}A_2I_1}{h_{fe1}A_1} \exp \frac{qI_1R_1}{kT}$$

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Figure 2. Forming a nanoampere current source with low parasitic capacitance. Design takes advantage of predictable V_{BE} difference between standard and super-gain transistors and fact that V_{BE} of a transistor is the same when operated in forward or reverse mode.

At first look, this biasing scheme would seem to be subject to a number of process variations. This is not so. For one, the V_{BE} of a transistor depends on the base Gummel number ($Q_B/\bar{\mu}_B$), the number of majority carriers per unit area divided by their effective mobility. Since the Gummel number and the effective area are unchanged when the collector and emitter are interchanged, the V_{BE} will be the same in either connection, provided that base recombination is not excessive. In standard IC transistors, reverse h_{fe} is about 30, indicating that recombination is not a significant factor. Measured reverse h_{fe} is much lower, but this is the result of a parasitic PNP that does not affect V_{BE} or α_E, the common base current gain.

The bleed current depends also on the ratio of super-gain to standard transistor h_{fe}, as indicated by the equation in *Figure 2*. Intuition suggests that super-gain h_{fe} will increase much faster than standard transistor h_{fe} with increasing emitter diffusion time, giving lower bleed current with higher super-gain h_{fe}. However, measurements with variances of standard LM108 processing indicate that the bleed current remains within 25% of design center.

As shown in *Figure 2*, higher current ratios can be obtained by increasing the area of Q1 relative to Q2 or by including R1. The equation in *Figure 2* assumes that I_1 varies as absolute temperature. If the voltage drop across R1 is equal to kT/q, changes in the V_{BE} of Q1 with small changes in I_1 will be cancelled by changes in the voltage drop across R1. This makes input bias current essentially unaffected by variations in supply or common-mode voltage as long as I_1 is reasonably well controlled.

leakage currents

The input leakage currents of bipolar op amps can be kept under control because small geometry devices are satisfactory and because the collector-base junction can be operated at an arbitrarily low voltage if bootstrapping is used.

Simple theory predicts that bulk leakage saturates for reverse biases above 2kT/q. But generation in the depletion zone dominates below 125°C. Because the depletion width varies with reverse bias, so does leakage. The characteristics of a high quality junction plotted in *Figure 3* show that leakage current can be reduced with lower bias.

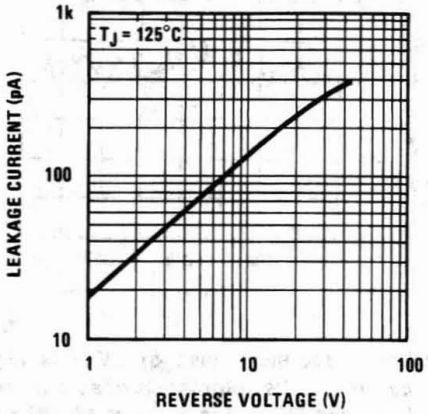

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Figure 3. Voltage sensitivity of collector base leakage indicates that generation in the depletion zone dominates even at 125°C.

When more than one junction is involved, minimum leakage is not necessarily obtained for zero bias. This is illustrated in *Figure 4*, a plot of I_{CBO} for a junction isolated NPN transistor. A parasitic PNP is formed between the base and the isolation as diagrammed in the inset. Zero leakage is obtained when V_{CB} is set so that the PNP diffusion current equals I_{CBO} of the NPN.

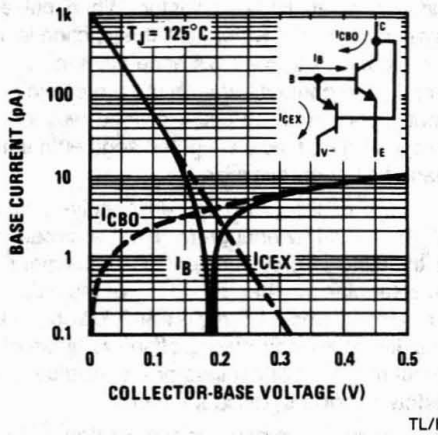

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Figure 4. Plot above explains "anomalous" leakage of NPN transistors in ICs. As collector base bias is reduced, base current reverses then increases exponentially. This excess current is the forward diffusion current of parasitic PNP to substrate (see inset).

input protection

The input clamps perform a dual function. Most important, they protect the emitter base junction of the input transistors from damage by in-circuit overloads or static charges in handling. Secondly, they limit the voltage change across junction capacitances on low current nodes under transient conditions. This minimizes recovery delays.

The clamp circuitry is shown in *Figure 5*. Emitters are added on the input transistors and cross-coupled to limit the differential input voltage. Another transistor, Q5, has been added to limit voltage on the input transistors if the inputs are driven below V^-.

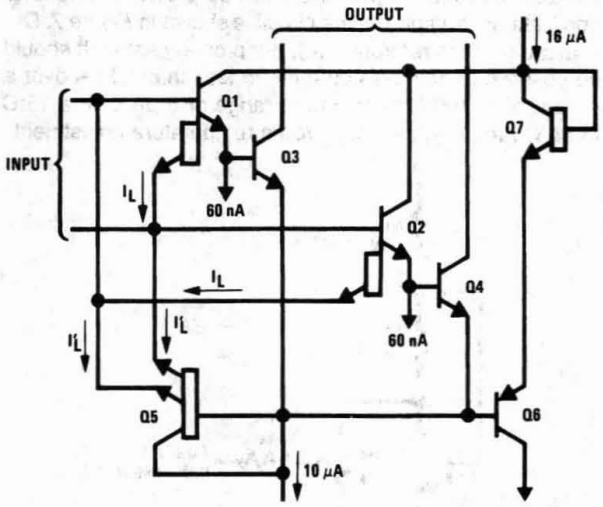

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Figure 5. Separate clamps are used for differential and common-mode overloads. Leakage currents, I_{CES} of forward and reverse connected transistors, cancel.

The differential clamp transitors do contribute to input current because $V_{CB} > 0$, so collector current is not zero for $V_{BE} \cong 0$ ($I_{CES} \cong 100$ pA at 125°C). The common-mode input clamp, Q5, is also operated at $V_{BE} = 0$ and $V_{CB} > 0$, although in the inverted mode. The resulting error is diffusion current, dependent only on the characteristic V_{BE} of the transistors. Thus, the current contributed by the differential clamp transistors is cancelled, within a couple percent, by that from the common-mode clamp.

bias current

Figure 6 shows some results of the design approach described here. A room temperature bias current of 25 pA is obtained, and this his held to 60 pA over a −55°C to 125°C temperature range. The figure also shows the results of

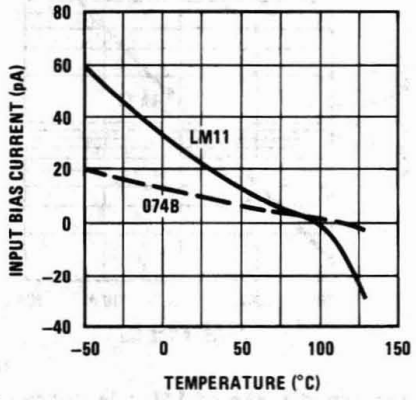

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Figure 6. Input bias current of the LM11 remains low over military temperature range. Improvements in development give even better results (074B). Offset current is usually below 1 pA.

some improvements in development that have reduced bias current to 20 pA over the full operating temperature range.

Figure 6 shows that bias current is very nearly a linear function of temperature, at least from −55°C to +100°C. This, coupled with the fact that bias current is virtually unaffected by changes in common-mode or supply voltage, suggests that bias current compensation can be provided for critical applications. An appropriate circuit is shown in *Figure 7*. Details are given in reference [2], but properly set up it should be possible to hold bias currents to less than 20 pA over a −55°C to +100°C temperature range or 5 pA over a 15°C to 55°C range with a simple room temperature adjustment.

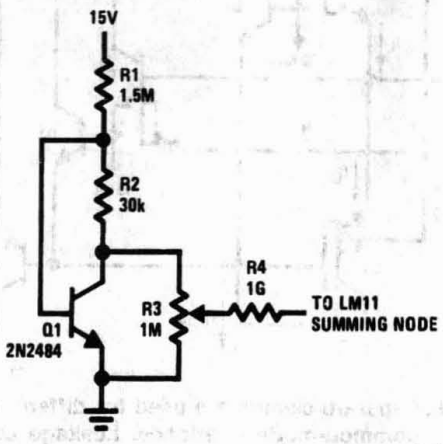

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Figure 7. Bias current of LM11 varies linearly with temperature so it can be effectively compensated with this circuit. Bias currents less than 5 pA over 15°C to 55°C range or 20 pA over −55°C to +100°C are practical.

noise

The broadband noise of a bipolar transistor is given by

$$e_n = kT\sqrt{2\Delta f/qI_C}. \quad (1)$$

Therefore, operating the input transistors at low collector current does increase noise. Because the noise of most op amps is greater than the theoretical noise voltage of the input transistors, the noise increase from low current input buffers is not as great as might be expected. In addition, when operating from higher source resistances, op amp noise is obscured by resistor noise, as shown in *Figure 8*.

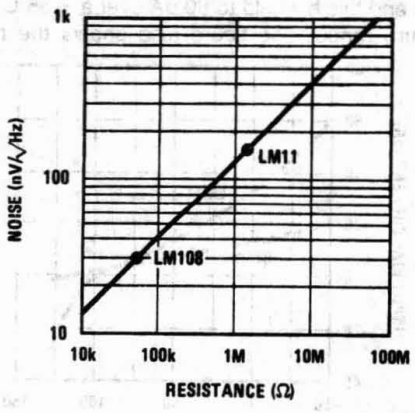

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Figure 8. Increased noise of LM11 is consequence of low collector current in input transistors. But in high impedance applications, op amp noise is masked by the thermal noise of source resistance given above.

Low frequency noise is not as easily accounted for as broadband noise, but lower operating currents increase noise in much the same fashion. The low frequency noise of the LM11, shown in *Figure 9*, is a bit less than FETs but greater than that of the LM108 when it is operated from source resistances less than 500 kΩ.

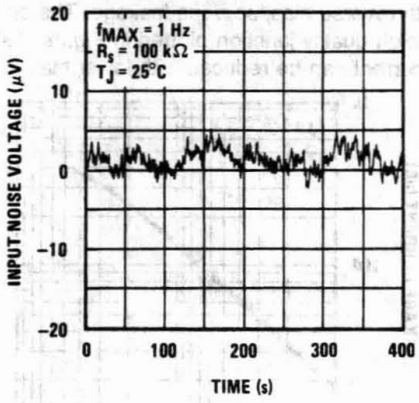

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Figure 9. Low frequency noise of LM11 is high compared to other bipolar devices but somewhat less than FETs. It is equal to LM108 operating from 500 kΩ source resistances.

complete circuit

A schematic diagram of an IC op amp using the techniques described is shown in *Figure 10*. Other than the input stage, the circuitry is much like the LM112, a compensated version of the LM108 that includes offset balancing.

One significant change has been the inclusion of wafer level trimming for offset voltage. This is done using zener-zap trimming across portions of the input stage collector load resistors, R4 and R5. This kind of zener is simply the emitter base junction of an NPN transistor. When pulsed with a large reverse current at wafer sort, the junction is destroyed by the formation of a low resistance filament between the emitter and base contact beneath the protective oxide. This shorts out a portion of the collector load resistor. The process is repeated on binary weighted segments until the offset voltage has been minimized.

Offset voltage of the LM11 is conservatively specified at 300 μV. Although low enough for most applications, offset voltage trimming is provided for fine adjustment. Balance range is determined by the resistance of the balance potentiometer, varying from ±5 mV at 100 kΩ to ±400 μV at 1 kΩ. Incidentally, when nulling offset voltages of 300 μV, the thermal matching of balance-pot resistance to the internal resistors is not a significant factor.

The actual balancing is done on the emitters of lateral PNP transistors, Q9 and Q10, that imbalance the collector loads of the input stage. This particular arrangement was used so that no damage would result from accidental connection of the balance pins to voltages outside either supply. Not obvious is that a balance pin voltage 15V more negative than V^+ can effectively short these PNP transistors with a parallel P-channel MOS transistor, forcing the output to one limit or another.

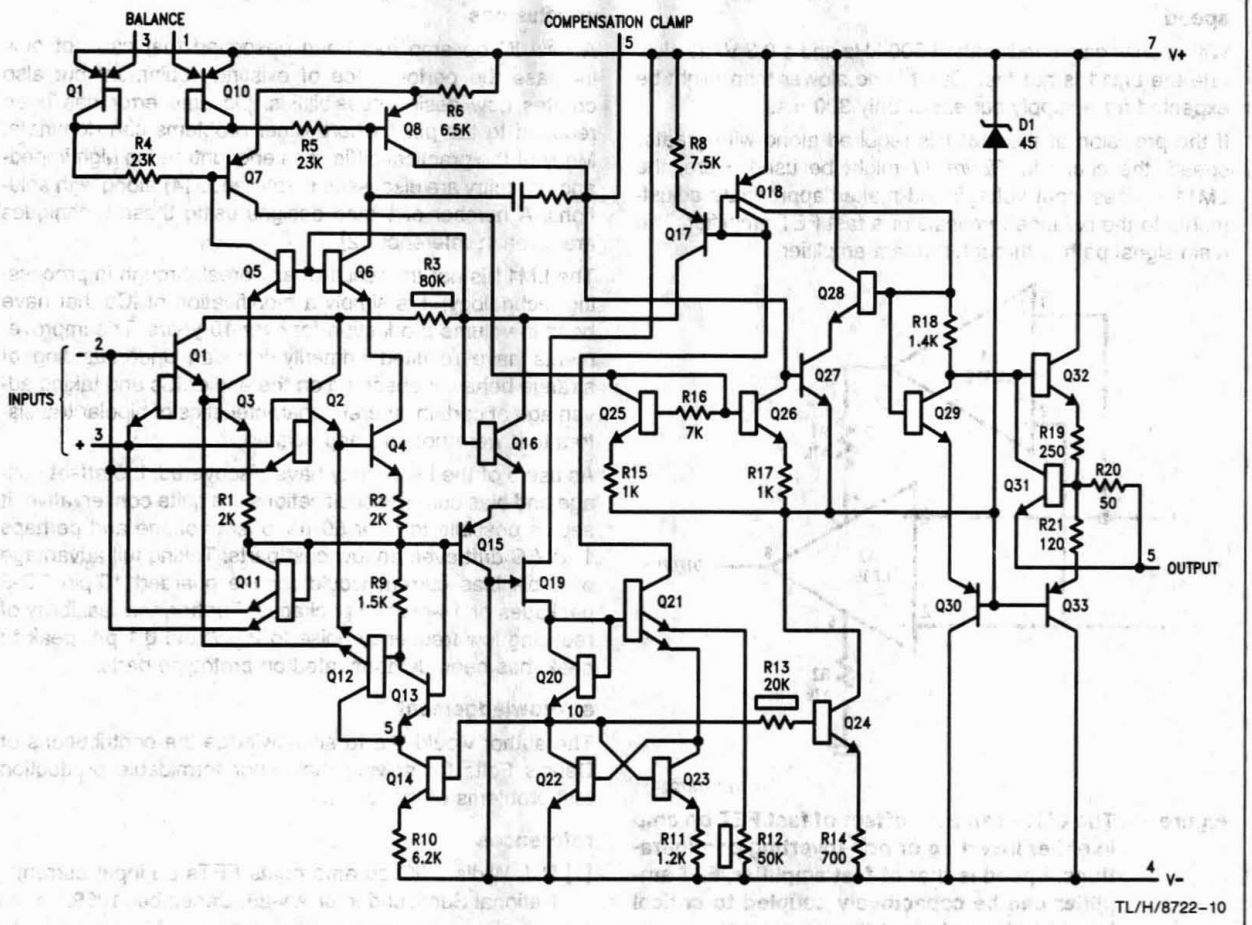

Figure 10. Complete schematic of the LM11. Except for the input stage, circuit is much like the LM112, a compensated version of the LM108 that includes offset balancing.

Although the LM11 is specified to a lower voltage than the LM108, the minimum common-mode voltage is a diode drop further from V^- because the bleed current generator, Q12 and Q13, has been added.

Proceeding from the input stage, the second stage amplifier is a differential pair of lateral PNPs, Q7 and Q8. These feed a current mirror, Q25 and Q26, which drive a super-gain follower, Q27. The collector base voltage of Q26 is kept near zero by including Q28. The current mirror is bootstrapped to the output so that second stage gain error depends only on how well Q7 and Q8 match with changes in output voltage. This gives a gain of 120 dB in a two stage amplifier. Frequency compensation is provided by MOS capacitor C1.

The output stage is a complementary class-B design with current limiting. Biasing has been altered so that the guaranteed output current is twice the LM108. A zener diode, D1, limits output voltage swing to prevent stressing the MOS capacitor to the point of catastrophic failure in the event of gross supply transients.

The main bias current generator design (Q20–Q23) is due to Dobkin [3]. It is powered by Q19, a collector FET. The circuit is auto-compensated so that output current of Q14 and Q21 varies as absolute temperature and changes by less than 1% for a 100:1 shift in Q19 current.

speed

With a unity gain bandwidth of 500 kHz and a 0.3 V/μs slew rate the LM11 is not fast. But it is no slower than might be expected for a supply current of only 300 μA.

If the precision of the LM11 is required along with greater speed, the circuit in *Figure 11* might be used. Here, the LM11 senses input voltage and makes appropriate adjustments to the balance terminals of a fast FET amplifier. The main signal path is through the fast amplifier.

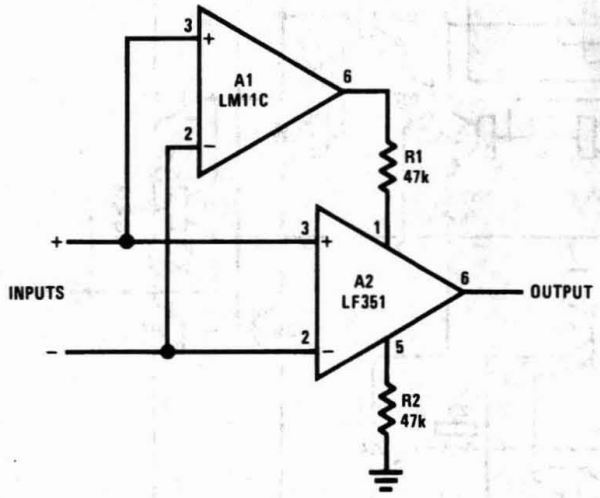

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Figure 11. The LM11 can zero offset of fast FET op amp in either inverting or non-inverting configurations. Speed is that of fast amplifier. FET amplifier can be capacitively coupled to critical input to eliminate its leakage current.

Surprisingly, this connection will work even as a voltage follower. The common-mode slew recovery of the LM11 is about 10 μs to 1 mV, even for 30V excursions. This was accomplished by minimizing or bootstrapping stray capacitances and providing clamping to limit the voltage excursion across the strays.

When bias current is an important consideration, it will be advisable to ac couple the FET op amp to the critical input. Reference [2] discusses this and other practical aspects of fast operation with the LM11.

conclusions

A new IC op amp has been described that can not only increase the performance of existing equipment but also creates new design possibilities. Op amp error has been reduced to the point where other problems can dominate. Many of the practical difficulties encountered in high impedance circuitry are discussed in reference [4] along with solutions. A number of tested designs using these techniques are given in reference [2].

The LM11 is not the result of any breakthrough in processing technology. It is simply a modification of ICs that have been in volume production for over 10 years. The improvements have resulted primarily from an understanding of strange behavior observed on the earlier ICs and taking advantage of certain inherent characteristics of bipolar transistors that were not fully appreciated.

As users of the LM11 may have discovered, the offset voltage and bias current specifications are quite conservative. It seems possible to offer 50 μV offset voltage and perhaps 1 μV/°C drift even on low cost parts. Taking full advantage of 5 pA bias current would require guarded 10-pin TO-5 packages or 14-pin DIP packages. Further, the feasibility of reducing low frequency noise to 2 μV and 0.1 pA, peak to peak, has been demonstrated on prototype parts.

acknowledgement

The author would like to acknowledge the contributions of Dennis Foltz for solving the rather formidable production test problems of the LM11.

references

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[2] R.J. Widlar, R. Pease and M. Yamatake, "Applying a new precision op amp", National Semiconductor AN-242, April 1980.

[3] R. Dobkin, U.S. patent no. 3930172.

[4] R.J. Widlar, "Working with high impedance op amps", National Semiconductor AN-241, February 1980.

Application of the ADC1210 CMOS A/D Converter

National Semiconductor
Application Note 245

INTRODUCTION

The ADC1210 is the answer to a need for analog to digital conversion in applications requiring low power, medium speed, or medium to high accuracy for low cost. The versatile input configurations allow many different input scale ranges and output logic formats.

The wide supply voltage range of 5V to 15V readily adapts the device to many applications. The very low power dissipation yields remarkable conversion linearity over the full operating temperature range. Table I below summarizes the typical performance of the ADC1210.

TABLE I. ADC1210 Performance Characteristics

Resolution	12 bits
Linearity Error, T_A = 25°C	±0.0183% FS MAX
Over Temperature	±0.0366 % FS MAX
Full Scale Error, T_A = 25°C	0.2% FS MAX
Zero Scale Error, T_A = 25°C	0.2% FS MAX
Quantization Error	±½ LSB MAX
Conversion Time	200 µs MAX

This note expands the scope of application configurations and techniques beyond those shown in the data sheet. The first section discusses the theory of operation. The remaining sections are devoted to applications that extract the optimum potential from the ADC1210.

THEORY OF OPERATION

Like most successive approximation A to D's, the ADC1210 consists of a successive approximation register (SAR), a D to A converter, and a comparator to test the SAR's output against the unknown analog input. In the case of the ADC1210, these elements are connected to allow unusual versatility in matching performance to the user's applications.

The SAR is a specialized shift register programmed such that a start pulse applies a logical low to the most significant bit (MSB) and logical highs to all other bits, thus applying a half scale digital signal to the DAC. If the comparator finds that the unknown analog input is below half scale, the low is shifted to the second bit to test for quarter scale. If, on the other hand, the comparator finds that the analog input is above half scale, the "low" state is not only shifted to the second bit, but also retained in the MSB, thus forming the digital code for three quarters scale. Upon completing the quarter (or three-quarter) sacle test, the next clock pulse sets the SAR to test either ⅛, ⅜, ⅝, or ⅞ full scale, depending on the input and the previous decisions. This successive half-the-previous-scale approximation sequence continues for the remaining lower order bits. The thirteenth clock pulse shifts the test bit off the end of the working register and into the conversion complete output. *Figure 1* shows the schematic diagram of the device.

OPERATING CONFIGURATIONS

Figures 2 through *5* show four operating configurations in addition to those presented in the data sheet.

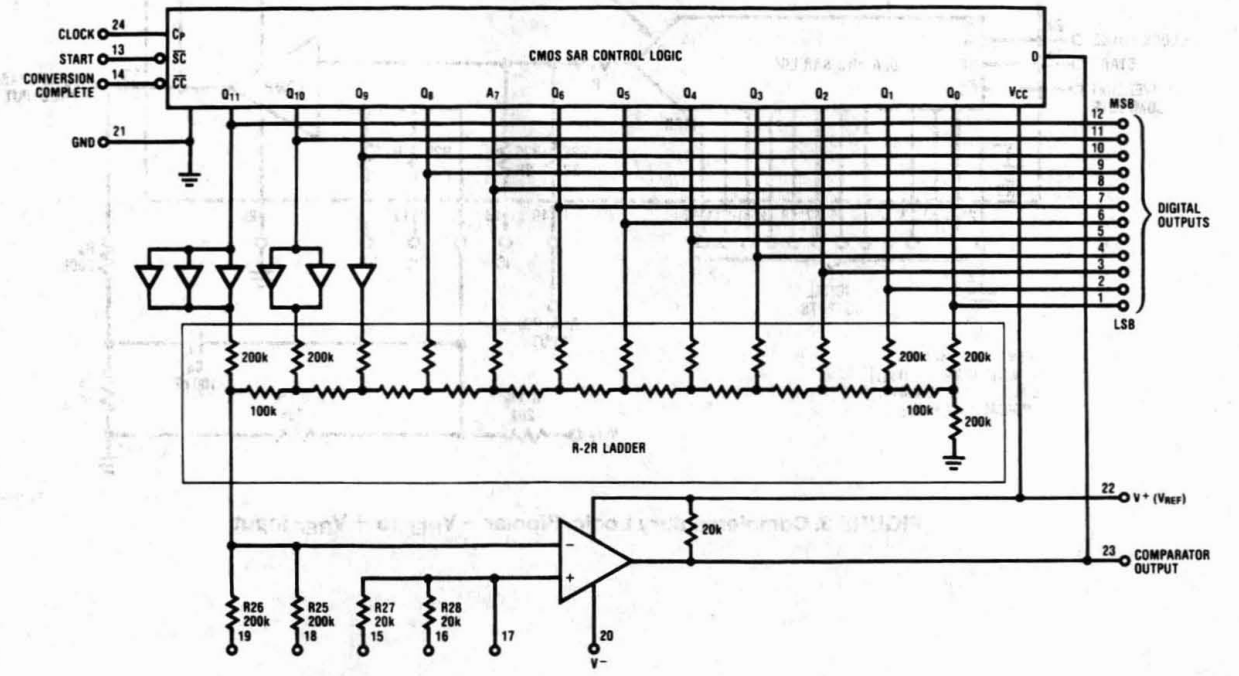

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FIGURE 1. Schematic Drawing

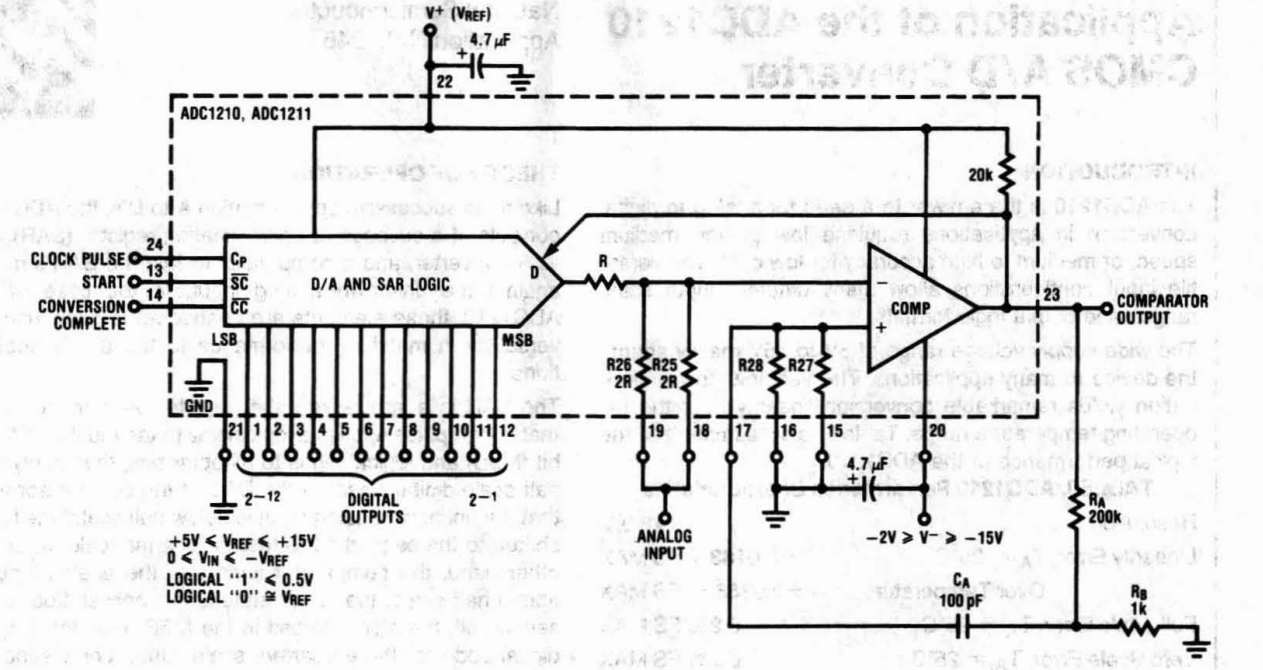

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FIGURE 2. Complementary Logic, 0V to $-V_{REF}$ Input

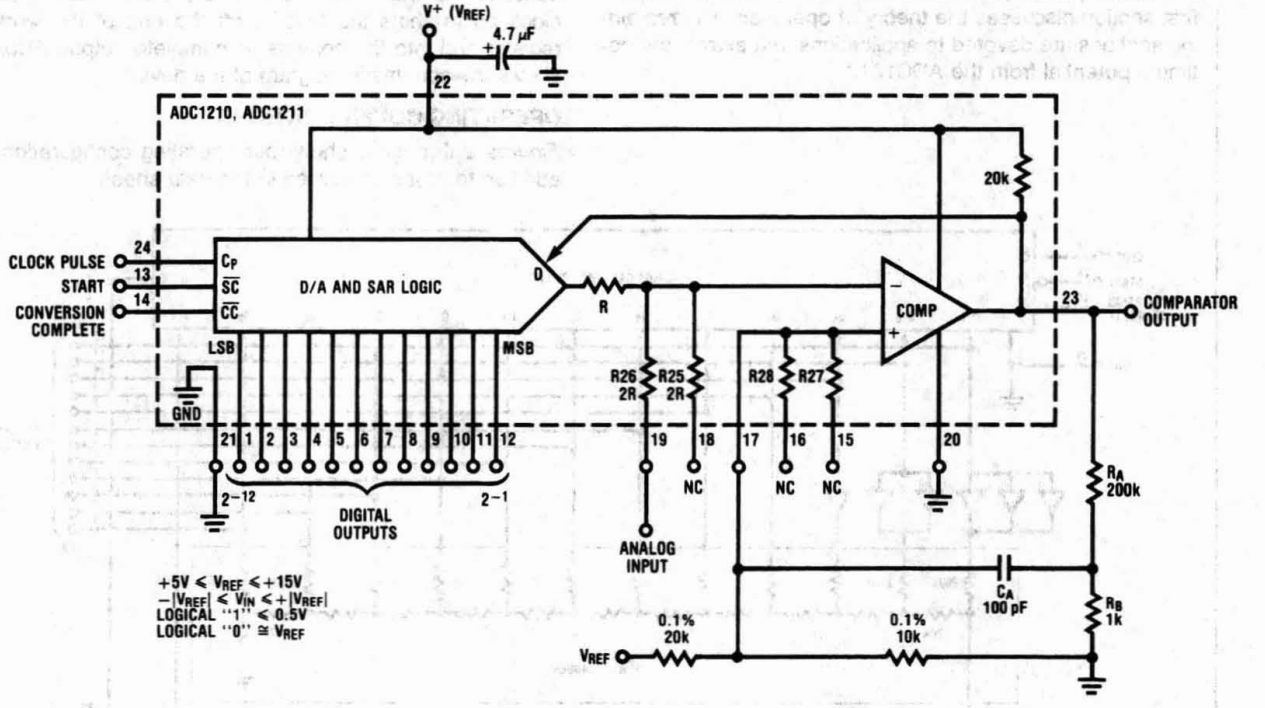

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FIGURE 3. Complementary Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

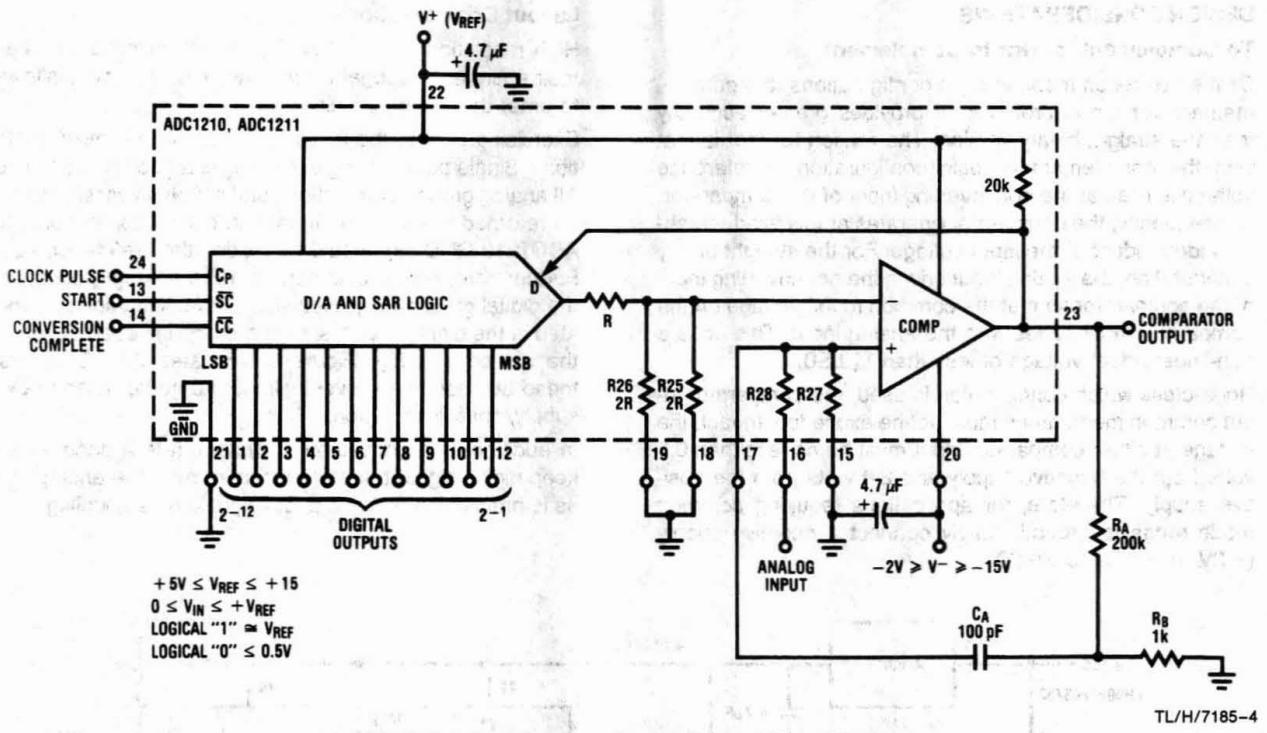

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FIGURE 4. Positive True Logic, 0V to $+V_{REF}$ Input

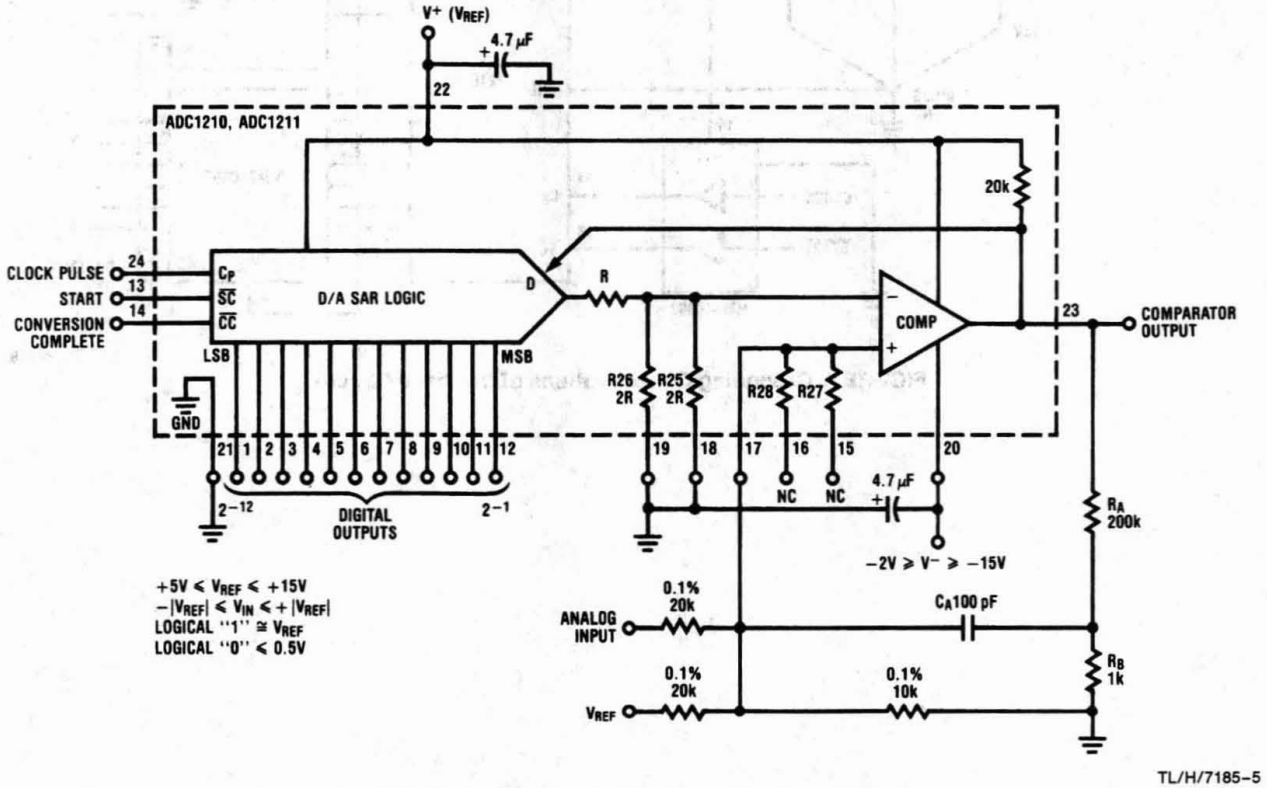

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FIGURE 5. Positive True Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

DESIGN CONSIDERATIONS

To Complement, or Not to Complement

Of the two recommended logic configurations, the complementary version is preferred. It provides greater accuracy than the straight binary version. The reason for that is that with the complementary logic configuration, a reference voltage is fixed at the non-inverting input of the comparator. Consequently, the comparator operates at this fixed threshold independent of the input voltage. For the straight binary configuration, the analog input drives the non-inverting input of the comparator so that the common mode voltage on the comparator input varies with the analog input. This adds a non-linear offset voltage of less than ¼ LSB.

Regardless which configuration is used, the comparator input common mode range must not be exceeded. In fact, the voltage at either comparator input must be no less than 0.5 volts from the negative supply and 2.0 volts from the positive supply. Therefore, for applications requiring common mode range to ground, simply connect a negative supply (−2V to −15V) to pin 20.

Layout Considerations

High resolution D/A and A/D converter circuits may have their entire error budget blown if any digital noise is allowed to enter the analog circuit.

Exercising care in the layout is certain to minimize frustrations. Single point analog grounding is a good place to start. All analog ground connections and supply bypassing should be returned to this point. In fact, in critical applications, the ADC1210 GND pin should be made "the" reference node. Furthermore, one should separate the analog ground from the digital ground. Any excursion of switching spikes generated in the digital circuit is, to some degree, decoupled from the analog circuitry. *Figure 6* illustrates this. Of course, these two points are eventually tied together at the power supply/chassis common.

In addition to a good ground system, it is a good idea to keep digital signal traces as far apart from the analog input as is practical in order to avoid signal cross coupling.

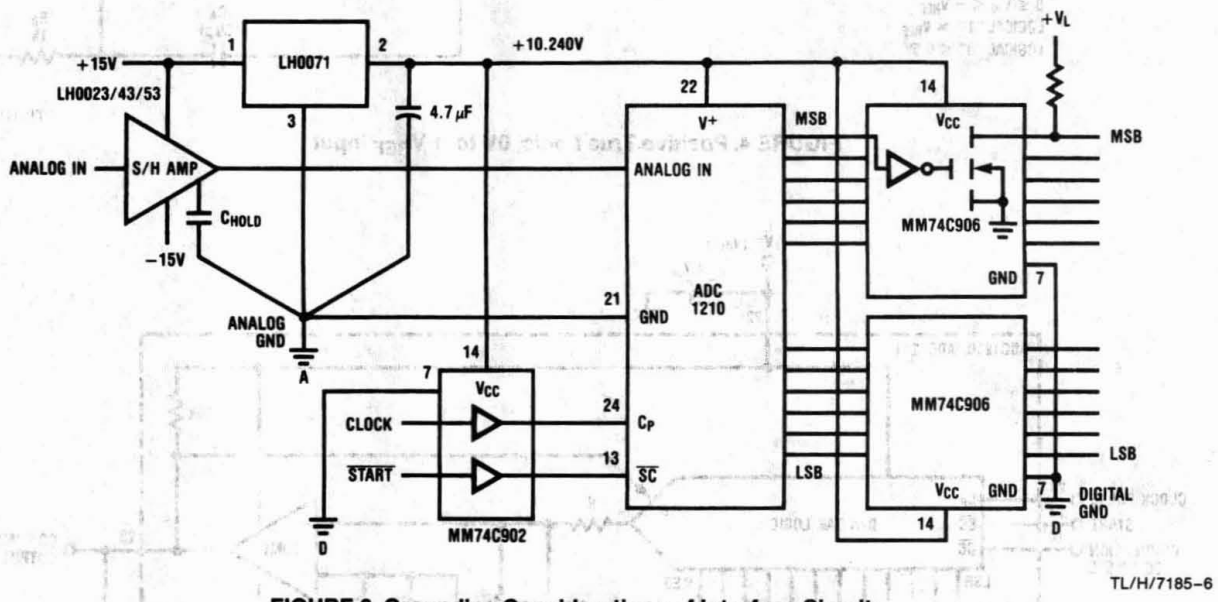

FIGURE 6. Grounding Considerations of Interface Circuits

Power Supply Bypassing

The supply input only provides power to the digital logic, it is also a reference voltage to the resistor ladder network of the ADC1210. This voltage must be a very stable source. A precision reference device such as the LH0070 or LH0071 is ideal for the ADC1210. However, the internal CMOS Successive Approximation Register (SAR) invariably generates current spikes (10–20 mA peak) in the supply pin as the logic circuit switches past the linear region. Consequently, if a reference device such as the LH0070 is used, the current spike tends to cause excursions in the reference voltage, thus threatening conversion accuracy. To preserve the 12-bit accuracy, bypass the supply pin with a 4.7 μF tantalum capacitor. In high noise environments, a 22 μF capacitor shunted by a 0.1 μF ceramic disc capacitor is desirable.

If pin 20 is connected to a negative supply, it too should be bypassed to prevent voltage fluctuations from affecting the comparator operation.

Output Drive Capability

The digital outputs of the ADC1210 and the outputs of the SAR, through which the resistor ladder is referenced, are one and the same. Any excessive load current on the digital output lines will degrade conversion accuracy. For this reason, the ADC1210 must interface with CMOS logic. However, the three most significant bits (pins 10, 11, and 12) are buffered from the R-2R ladder and are capable of driving light loads without degrading linearity. This could prove useful in 2's complement applications where an inverter is necessary in the MSB; one might construct this inverter with a discrete NPN transistor and two resistors. The bit most sensitive to output loading is the fourth most significant (pin 9). An error voltage at this pin gets divided down by a factor of 16 before being applied to the comparator, so if we wish to limit the error due to output loading to say, ½ LSB, or 1.25 mV at the comparator, we can tolerate 20 mV at pin 9. If all lower bits will have the same output load, the error must be limited to 10 mV. Since all of the digital outputs have a maximum ON resistance of 350Ω at 10V V_{REF} in both high and low states, the maximum allowable load current is 10 mV/350Ω = 29 μA. This current requirement is easily satisfied with an MM74C914 or MM74C901 thru MM74C902 level translators for interface with logic levels different than V_{REF}.

Comparator Hysteresis

Even an ideal comparator can be expected to oscillate due to stray capacitive feedback if biased in the linear region. It is the normal operation of the SAR feedback loop to do just that . . . at least at or toward the end of the conversion cycle. For most applications, this oscillation is only a minor bother, as the SAR register would have locked out the converted data from further changes at the end of conversion. If that is still undesirable, the Conversion Complete ($\overline{CC}$) Signal may be used to drive an open-collector gate (such as the MM74C906) with the output wire-ORed to the comparator output. In this way, the comparator is always clamped to the low state at the end of conversion. Normal operation resumes upon restart of a new conversion cycle.

In normal operation, however, if we want to preserve 12-bit accuracy, the comparator oscillation should be suppressed. The recommended technique is to apply a slight amount of AC hysteresis (50 mV) at the beginning of the decision cycle, but let it decay away to an acceptable accuracy before the decision is actually recorded in the SAR. The approximate decay time is (5) × (10k + 1k) × (100 pF), or 5.5 μs (see *Figure 2*).

For those applications using supply voltage other than 10V, say 5V, and if 50 mV initial hysteresis is to be maintained, the 200 kΩ (R_A) resistor in *Figure 2* should be changed to 100 kΩ based on the relationship:

$$\frac{R_B}{R_A + R_B} V_{REF} = 50\ mV$$

Where: R_B = 1 kΩ

High Speed Conversion Technique

By using one IC, one discrete NPN transistor, and a resistor, the ADC1210 can be made to run at up to 500 kHz clock frequency, or 12-bit conversion time of 26 μs. The circuit is shown in *Figure 7*. The idea is to clamp the comparator output low until the SAR is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions. This technique eliminates the need for the AC hysteresis circuit.

To implement the idea, a complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The inverted clock, generated from the same clock signal, is inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in working order. During the last half cycle, the comparator output is unclamped. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propagation delay such that the comparator output data is held long enough to resolve any internal logic set-up time requirements.

The 500 kHz clock implies that the absolute minimum amount of time required for the comparator output to be unclamped is 1 μs. Therefore, for applications with clock signal other than 50% duty cycle, this 1 μs period must be observed.

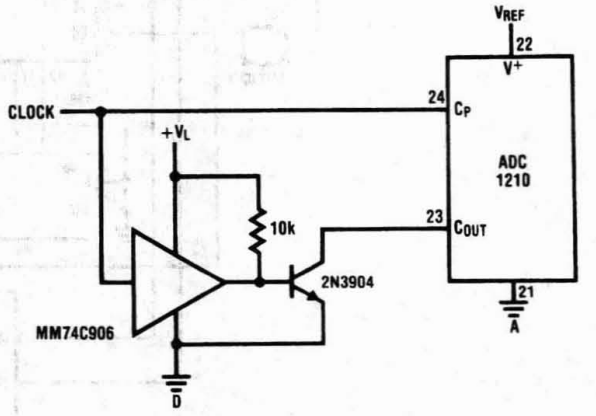

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FIGURE 7. High Speed Conversion Circuit

Testing has demonstrated reliable performance from this circuit beyond the recommended device operating frequency of 65 kHz. However, the AC hysteresis circuit is still a very reliable technique below this clock frequency and, therefore, should be used. Only in applications where the required clock frequency is above 65 kHz should the above-mentioned technique be adopted.

Synchronizing Conversion Start Signal

It is recommended that the $\overline{\text{START CONVERT}}$ input be synchronized to the CLOCK input. This avoids the possibility of the comparator making an error on the first (MSB) decision when the analog input is near ½ scale. There is a chance that energy can be coupled to the comparator from the rising edge of the $\overline{\text{START}}$ signal. If this occurs just before the rising edge of the clock, a wrong MSB decision can be made if time is not allowed for the charge to dissipate. The synchronization circuit in *Figure 8* effectively prevents this from occurring.

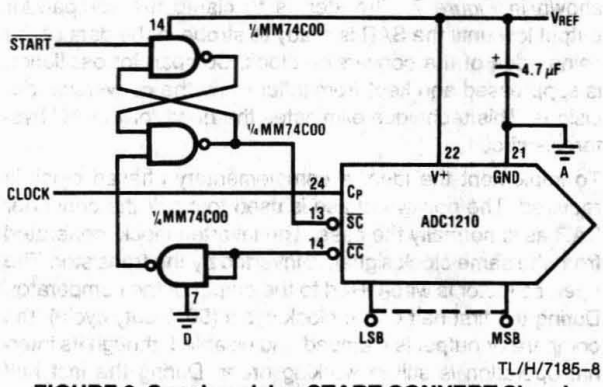

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FIGURE 8. Synchronizing START CONVERT Signal

The circuit operates as follows: initially the latch is in the RESET state and the converter is in the end-of-conversion state ($\overline{\text{CC}}$ output at logic low). The $\overline{\text{START}}$ signal sets the latch and, on the next positive clock transition, initializes all internal registers in the converter. The $\overline{\text{CC}}$ output is set to logic high, presetting the external latch. The latch is held in the "RESET" state during the entire conversion period, effectively preventing a new $\overline{\text{START}}$ signal from interrupting the conversion.

Serial Output

The comparator output does contain the stream of serially converted data with the most significant bit first. However, recognizing the danger of comparator oscillation, there is a potential for the external serial data register to latch a data bit different from that recorded in the SAR due to different logic set-up time requirements. If the ADC1210 accepts an error in any one data bit, the subsequent lower order bits tend to correct for it. On the other hand, an external serial register has no provision for error correction. All subsequent bits following a bit in error will not be valid data.

The 12 bits of information can be shifted out serially by using an MM74C150 digital multiplexer. The circuit is shown in *Figure 9*. This scheme permits valid data to be available at the serial output port as fast as half a clock cycle after the most current decision. The data are thus synchronized to the converter clock (here the serial data are synchronized at the falling edge of the system CLOCK, to avoid clock skew). Obviously, a number of variations can be made to this basic circuit for use with different handshake protocols.

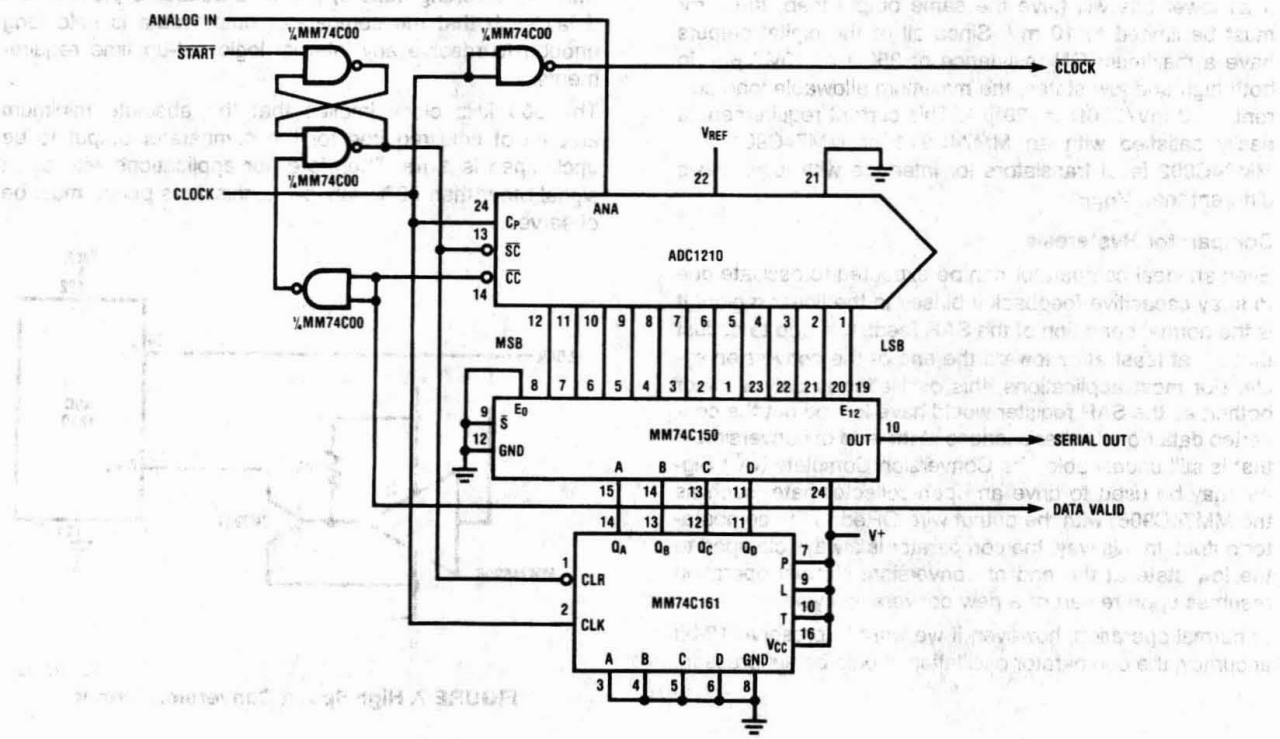

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FIGURE 9. 12-Bit A/D Converter with Serial Output

APPLICATIONS

Long Time Sample and Hold

The circuit in *Figure 10* is a particularly simple realization of an infinite sample and hold. This scheme requires two low-cost analog sample-and-hold amplifiers to complete the circuit.

The idea is to utilize the digital-loop feedback mechanism of the ADC1210 which, in the normal conversion mode, replicates the analog input voltage at the output of the SAR/D-to-A converter.

The operation of the circuit may be described as follows: During the normal "hold" mode, the replicated analog voltage is buffered straight through the S/H amplifier to the output. Upon an issuance of a $\overline{\text{SAMPLE}}$ signal, this S/H amplifier is placed in the hold mode, holding the voltage until the new analog voltage is valid. The same $\overline{\text{SAMPLE}}$ signal triggers an update to the input sample-and-hold amplifier. The most current analog voltage is captured and held for conversion. This way, the previously determined voltage is held stable at the output during the conversion cycle while the SAR/D-to-A continuously adjust to replicate the new input voltage. At the end of the conversion, the output sample-and-hold amplifier is once again placed in the track mode. The new analog voltage is then regenerated.

An Auto-Ranging Gain-Programmed A/D Converter

The circuit in *Figure 11* shows one possible circuit of an auto-ranging A/D converter. The circuit has a total of 8 gain ranges, with the ranging done in the LH0086 Programmable Gain Amplifier (for differential input, use the LH0084 with ranges of 1, 2, 5, 10 digitally programmed, or pin strap programmed for multiplying factors of 1, 4, and 10). The gain ranges are: 1, 2, 5, 10, 20, 50, 100, and 200. It effectively improves the A/D *resolution* from 12 bits to an equivalent of 19 bits, a dynamic range of better than 100 dB.

The circuit has relatively high speed ranging due to the very fast settling time of the LH0086, typically 5 μs for 10V swing, well within the 15 μs converter clock period. Thus, the ranging circuit is designed to work off the same clock.

The circuit is designed such that the auto-ranging function is transparent to the user. All command signals into and out of the system are identical to those of an ADC1210 operating alone. The only exception is that the system requires one and one-half clock cycle (mandatory auto range cycle), plus however many ranges it has to scale to (each scale requires one clock period, 7 possible range switching in all) in addition to the basic 13 conversion cycle required by the ADC1210. Therefore, in the best case where no ranging is necessary, the circuit adds 22.5 μs to the conversion time; and in the worst case, an additional 128 μs.

In the quiescent state where the ADC1210 is in the non-conversion mode, the auto-ranging circuit is free to function normally. Upon an issuance of a $\overline{\text{START}}$ signal, the next clock rising edge puts the circuit in the final auto range cycle before conversion begins. If the need for up-range or down-range is detected, the circuit remains in the auto range mode until all necessary scaling is completed. The control circuit then issues a start conversion signal to the ADC1210. Half a clock cycle later, the ADC1210 begins conversion and suspends the auto-ranging operation until the conversion is completed. At which time the 12-bit converter data plus the 3-bit range data are valid for further processing.

This design is suitable for applications in data-acquisition systems or portable instruments, particularly where low power is an important consideration. Other variations from this basic scheme can be realized depending on the user's requirements.

SUMMARY

The ADC1210 is a low-cost, medium-speed CMOS analog-to-digital converter with 12-bit resolution and linearity. It has wide supply range and flexible configuration to allow varied applications such as field instruments and sampled data systems.

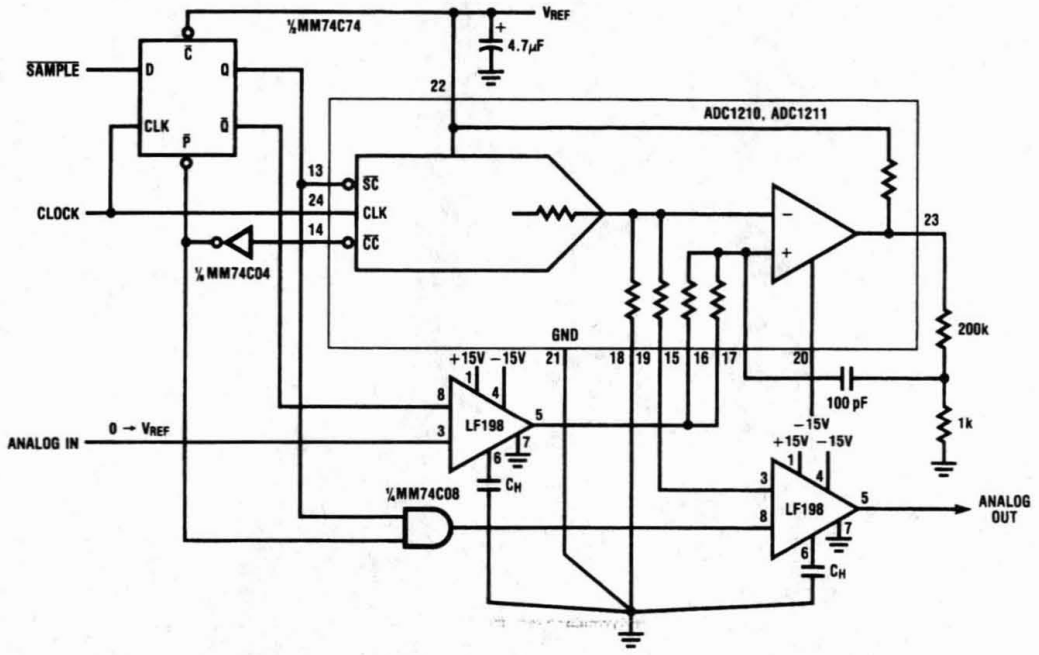

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FIGURE 10. Infinite Sample and Hold Amplifier

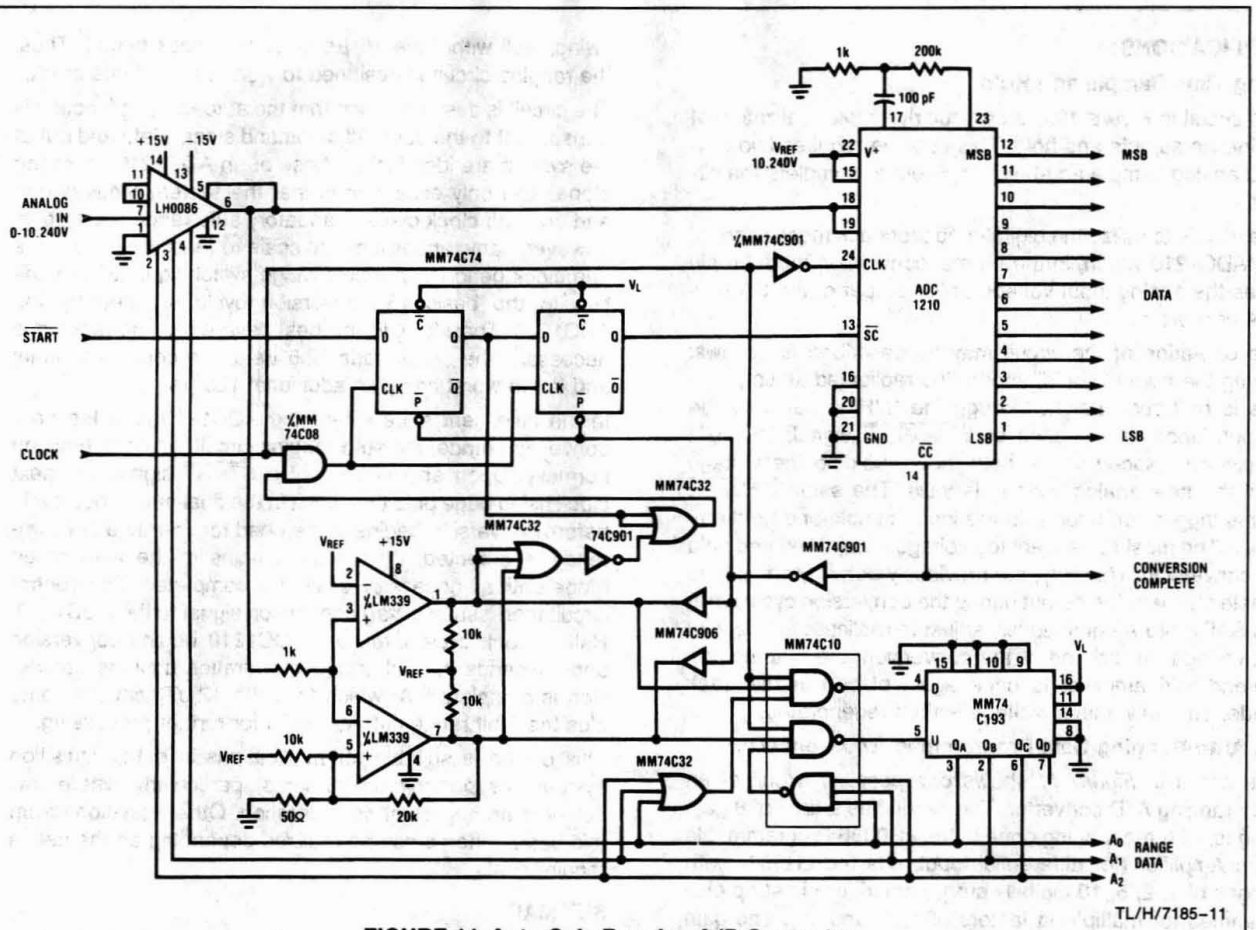

FIGURE 11. Auto Gain Ranging A/D Converter

Using the ADC0808/ ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Analog Multiplexer

National Semiconductor
Application Note 247
Larry Wakeman

INTRODUCTION

The ADC0808/ADC0809 Data Acquisition Devices (DAD) implement on a single chip most the elements of the standard data acquisition system. They contain an 8-bit A/D converter, 8-channel multiplexer with an address input latch, and associated control logic. These devices provide most of the logic to interface to a variety of microprocessors with the addition of a minimum number of parts.

These circuits are implemented using a standard metal-gate CMOS process. This process is particularly suitable to applications where both analog and digital functions must be implemented on the same chip.

These two converters, the ADC0808 and ADC0809, are functionally identical except that the ADC0808 has a total unadjusted error of ±½ LSB and the ADC0809 has an unadjusted error of ±1 LSB. They are also related to their big brothers, the ADC0816 and ADC0817 expandable 16 channel converters. All four converters will typically do a conversion in ~100 μs when using a 640 kHz clock, but can convert a single input in as little as ~50 μs.

1.0 FUNCTIONAL DESCRIPTION

The ADC0808/ADC0809, shown in *Figure 1*, can be functionally divided into 2 basic subcircuits. These two subcircuits are an analog multiplexer and an A/D converter. The multiplexer uses 8 standard CMOS analog switches to provide for up to 8 analog inputs. The switches are selectively turned on, depending on the data latched into a 3-bit multiplexer address register.

The second function block, the successive approximation A/D converter, transforms the analog output of the multiplexer to an 8-bit digital word. The output of the multiplexer goes to one of two comparator inputs. The other input is derived from a 256R resistor ladder, which is tapped by a MOSFET transistor switch tree. The converter control logic controls the switch tree, funneling a particular tap voltage to the comparator. Based on the result of this comparison, the control logic and the successive approximation register (SAR) will decide whether the next tap to be selected should be higher or lower than the present tap on the resistor ladder. This algorithm is executed 8 times per conversion, once every 8 clock periods, yielding a total conversion time of 64 clock periods.

When the conversion cycle is complete the resulting data is loaded into the TRI-STATE® output latch. The data in the output latch can then be read by the host system any time before the end of the next conversion. The TRI-STATE capability of the latch allows easy interface to bus oriented systems.

The operation of these converters by a microprocessor or some control logic is very simple. The controlling device first selects the desired input channel. To do this, a 3-bit channel address is placed on the A, B, C input pins; and the ALE input is pulsed positively, clocking the address into the multiplexer address register. To begin the conversion, the START pin is pulsed. On the rising edge of this pulse the internal registers are cleared and on the falling edge the start conversion is initiated.

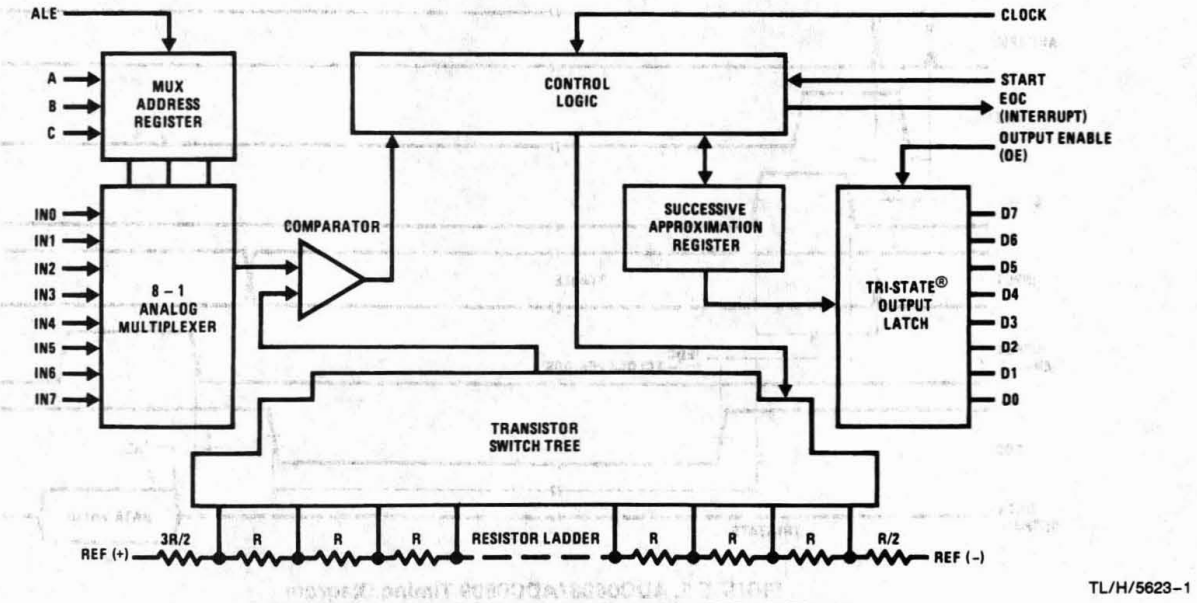

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FIGURE 1. ADC0808/ADC0809 Functional Block Diagram

As mentioned earlier, there are 8 clock periods per approximation. Even though there is no conversion in progress the ADC0808/ADC0809 is still internally cycling through these 8 clock periods. A start pulse can occur any time during this cycle but the conversion will not actually begin until the converter internally cycles to the beginning of the next 8 clock period sequence. As long as the start pin is held high no conversion begins, but when the start pin is taken low the conversion will start within 8 clock periods.

The EOC output is triggered on the rising edge of the start pulse. It, too, is controlled by the 8 clock period cycle, so it will go low within 8 clock periods of the rising edge of the start pulse. One can see that it is entirely possible for EOC to go low before the conversion starts internally, but this is not important, since the positive transition of EOC, which occurs at the end of a conversion, is what the control logic is looking for.

Once EOC does go high this signals the interface logic that the data resulting from the conversion is ready to be read. The output enable (OE) is then raised high. This enables the TRI-STATE outputs, allowing the data to be read. *Figure 2* shows the timing diagram.

2.0 ANALOG INPUTS

2.1 Ratiometric Inputs

The arrangement of the REF(+) and REF(−) inputs is intended to enable easy design of ratiometric converter systems. The REF inputs are located at either end of the 256R resistor ladder and by proper choice of the input voltages several applications can be easily implemented.

Figure 3 shows a typical input connection for ratiometric transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full-scale value. In other words, the transducer's absolute output value is of no particular concern but the ratio of the output to the full-scale is of great importance. For example, the potentiometric displacement transducers of *Figure 3* have this feature. When the wiper is at midscale, the output voltage is $V_O = V_F \times$ (Wiper Displacement) $= V_F \times 0.5$. This enables the use of much less accurate and less expensive references. The important consideration for this reference is noise. The reference must be "glitch free" because a voltage spike during a conversion cycle could cause conversion inaccuracies.

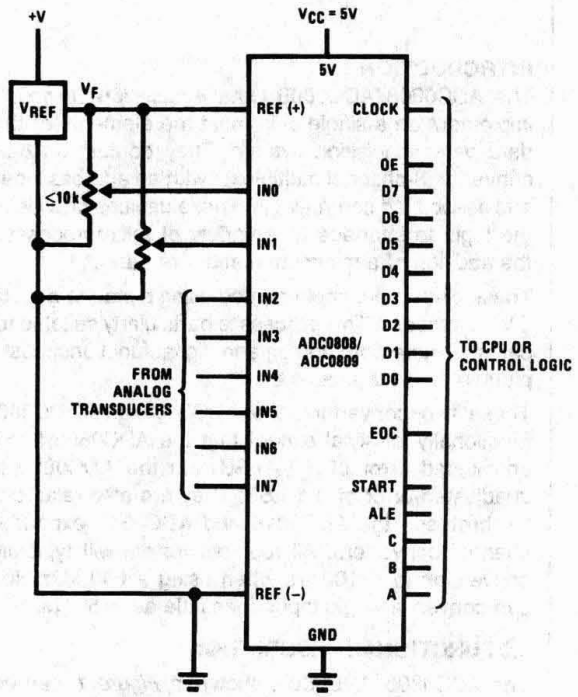

FIGURE 3. Ratiometric Converter with Separate Reference

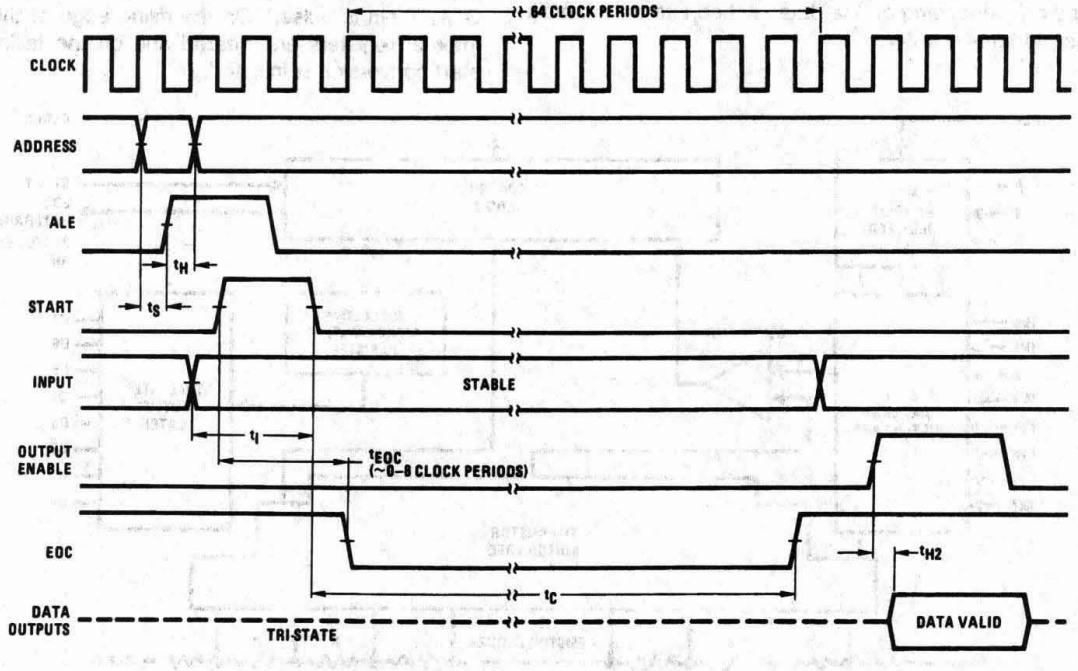

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FIGURE 2. ADC0808/ADC0809 Timing Diagram

Since highly accurate references aren't required it is possible to use the system power supply as a reference, as shown in *Figure 4*. If the power supply is to be used in this manner supply noise must be kept to a minimum to preserve conversion accuracy. If possible the supply should be well bypassed and separate reference and supply PC board traces, originating as close as possible to the power supply or regulator, should be used. This is illustrated in *Figure 4*. External accessibility of both ends of the resistor ladder enables several variations on these basic connections, and are shown in *Figures 5* and *6*. The magnitude of the reference voltage, V_{REF} = REF(+) − REF(−), can be varied from about ~0.5V to V_{CC}, but the center voltage must be maintained within ±0.1V of $V_{CC}/2$. This constraint is due to the design of the transistor switch tree, which could malfunction if the offset from center scale becomes excessive. Variation of the reference voltage can sometimes eliminate the need for external gain blocks to scale the input voltage to a full-scale range of 5V.

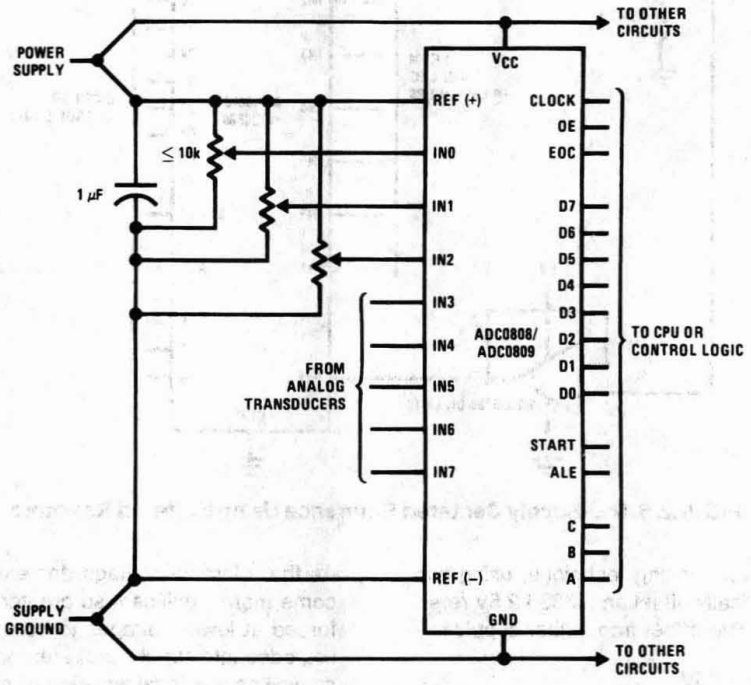

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FIGURE 4. Ratiometric Converter with Power Supply Reference

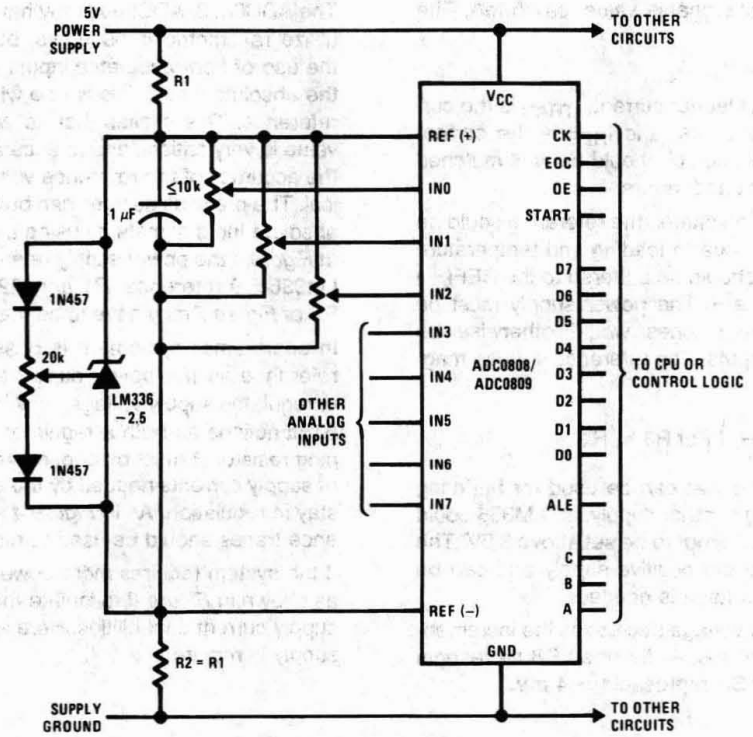

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FIGURE 5. Mid-Supply Centered Reference Using LM336 2.5V Reference

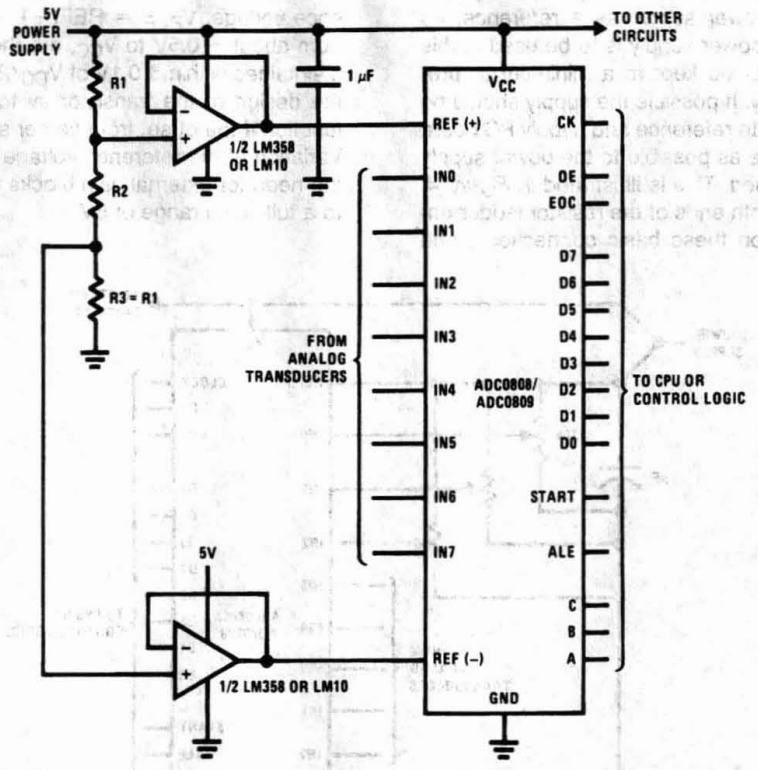

FIGURE 6. Mid-Supply Centered Reference Using Buffered Resistors

Figure 5 shows a center referencing technique, using two equal resistors to symmetrically offset an LM336 2.5V reference, from both supplies. The offset from either supply is:

$$V_{OFF} = \frac{V_{CC} - V_{REF}}{2} = 1.25V$$

These resistors should be chosen so that they limit current through the LM336 to a reasonable value, say 5 mA. The total resistor current is:

$$I_R = I_{REF} + I_{LADDER} + I_{TRAN}$$

where I_{LADDER} is the 256R ladder current, I_{TRAN} is the current through all the transducers, and I_{REF} is the current through the reference. R1 and R2 should be well matched and track each other over temperature.

For odd values of reference voltage, the reference could be replaced by a resistor, but due to loading and temperature problems, these resistors should be buffered to the REF(+) and REF(−) inputs, *Figure 6*. The power supply must be well bypassed as supply glitches would otherwise be passed to the reference inputs. The reference voltage magnitude is:

$$V_{REF} = V_{DD}\left(\frac{R2}{2R1 + R2}\right) \text{ For } R3 = R1$$

There are several op amps that can be used for buffering this ladder. Without adding another supply, an LM358 could be used if the REF(+) input is not to be set above 3.5V. The LM10 can swing closer to the positive supply and can be used if a higher $V_{REF(+)}$ voltage is needed.

As the REF(+) to REF(−) voltage decreases the incremental voltage step size decreases. At 5V one LSB represents ~20 mV, but at 1V, one LSB represents ~4 mV.

As the reference voltage decreases, system noise will become more significant so greater precaution should be enforced at lower voltages to compensate for system noise; i.e., adequate supply and reference bypassing, and physical as well as electrical isolation of the inputs.

2.2 Absolute Analog Inputs

The ADC0808/ADC0809 may have been designed to easily utilize ratiometric transducers, but this does not preclude the use of non-ratiometric inputs. A second type of input is the absolute input. This is one which is independent of the reference. This implies that its *absolute* numerical voltage value is very critical, and to accurately measure this voltage the accuracy of the reference voltage becomes equally critical. The previous designs can be modified to accommodate absolute input signals by using a more accurate reference. In *Figure 4* the power supply reference could be replaced by LM336-5.0 reference. R1 and R2 of *Figure 6*, and R1 and R3 of *Figure 7* may have to be made more accurately equal.

In some small systems it is possible to use the precision reference as the power supply as shown in *Figure 7*. An unregulated supply voltage >5V is required, but the LM336-5.0 functions as both a regulator and reference. The dropping resistor R must be chosen so that, for the whole range of supply currents needed by the system, the LM336-5.0 will stay in regulation. As in *Figure 4* separate supply and reference traces should be used to maintain a noiseless supply.

If the system requires more power, an op amp can be used as shown in *Figure 8* to isolate the reference and boost the supply current capabilities. Here again, a single unregulated supply is required.

2.3 Differential Inputs

Differential measurements can be obtained by playing a little software trick. This simply involves sequentially converting two channels then subtracting the two results. For example, if the difference voltage between channel 1 and 2 is required, merely convert channel 1 and read the result. Then convert channel 2, input the result, and subtract it from the first result. (See *Figure 9.*) When using this procedure, both input signals must be stable throughout both conversion times or the end result will be incorrect. One way to get around this is to use two sample/holds which are sampled at the same time.

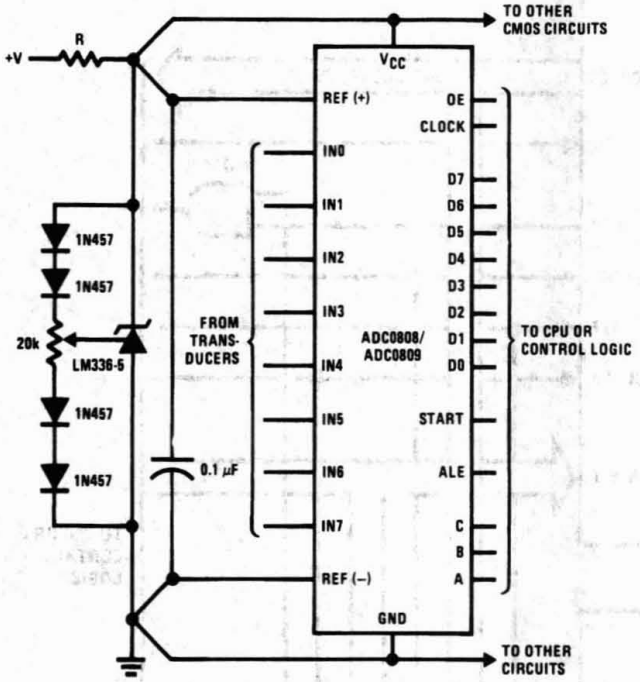

FIGURE 7. Precision Reference used as a Power Supply

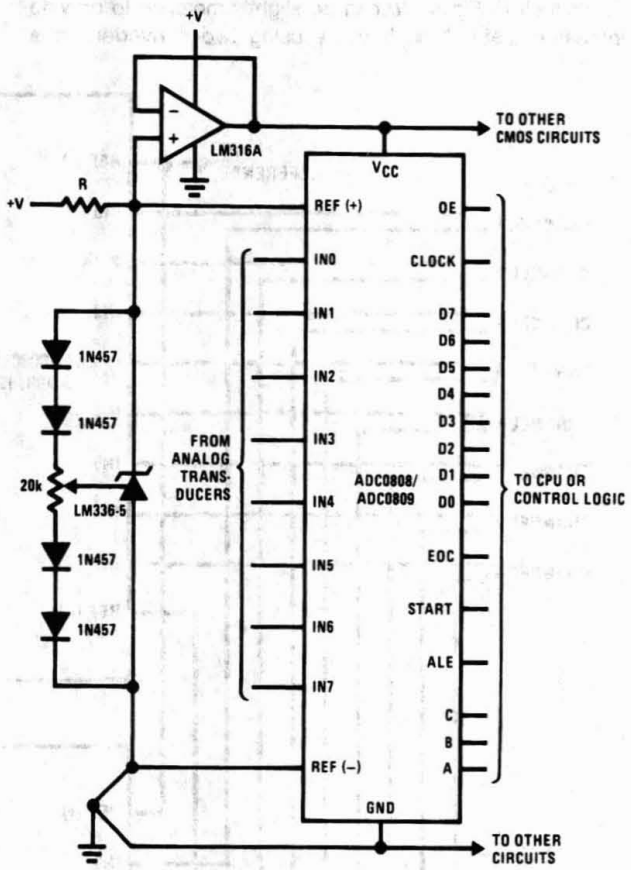

FIGURE 8. Precision Reference Buffered for Power Supply

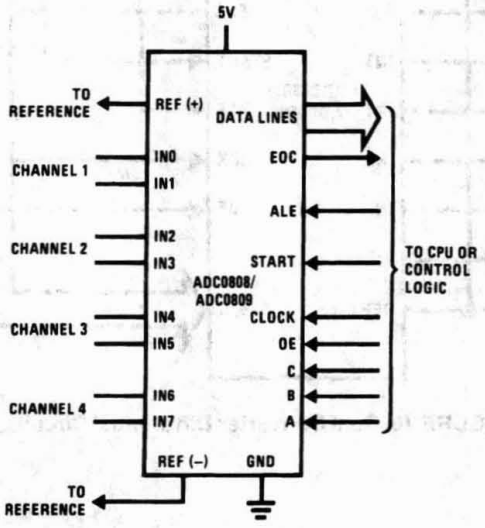

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FIGURE 9. Software Controlled Differential Converter

A second method is to use two chips to convert a differential channel, *Figure 10*. Typically each channel 1 would be connected to opposite sides of the differential input. Both converters are started simultaneously. When both converters' EOC outputs go high the output of the AND gate will go high indicating that the data is ready to be read.

The circuit in *Figure 10* can be slightly modified to provide increased data throughput by using two converters in a parallel data acquisition scheme. *Figure 11* shows this circuit in which all the input channels are connected in pairs through LF398 monolithic sample/holds. Under normal operation a sample/hold is accessed through an MM74C42 which will pulse an MM74C221, generating a sample pulse. After a sample/hold is done sampling the signal, the appropriate channel is started. If this process is alternated between two converters the sample rate can be doubled.

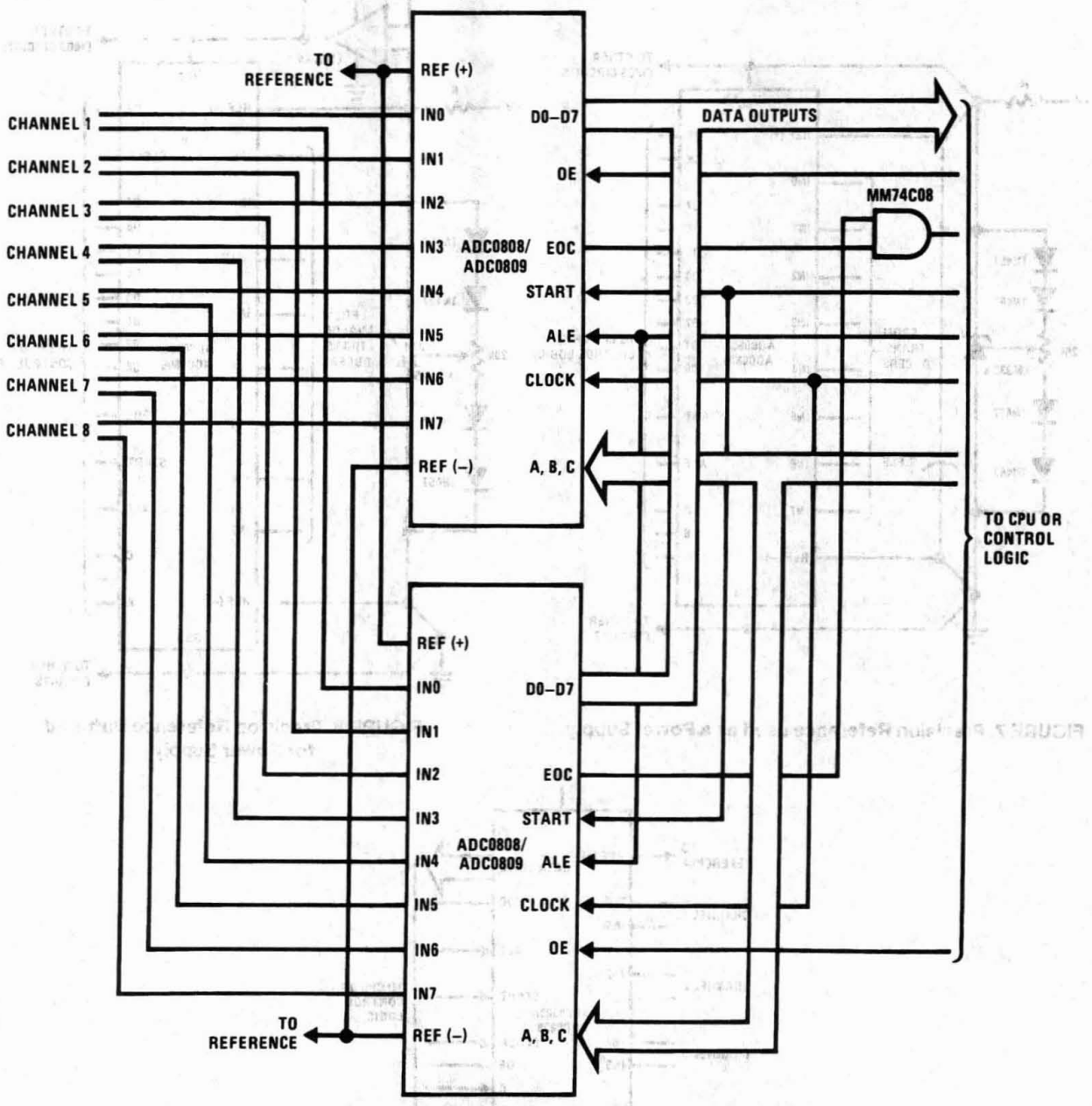

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FIGURE 10. Dual Converter Differential Circuit

2.4 Analog Input Considerations

Analog inputs into the ADC0808/ADC0809 can handle any input signal that is maintained within the supply limits, but some careful consideration must be given to the output impedance of the transducer or buffer. Using transducers with large source impedances can cause errors due to comparator input currents.

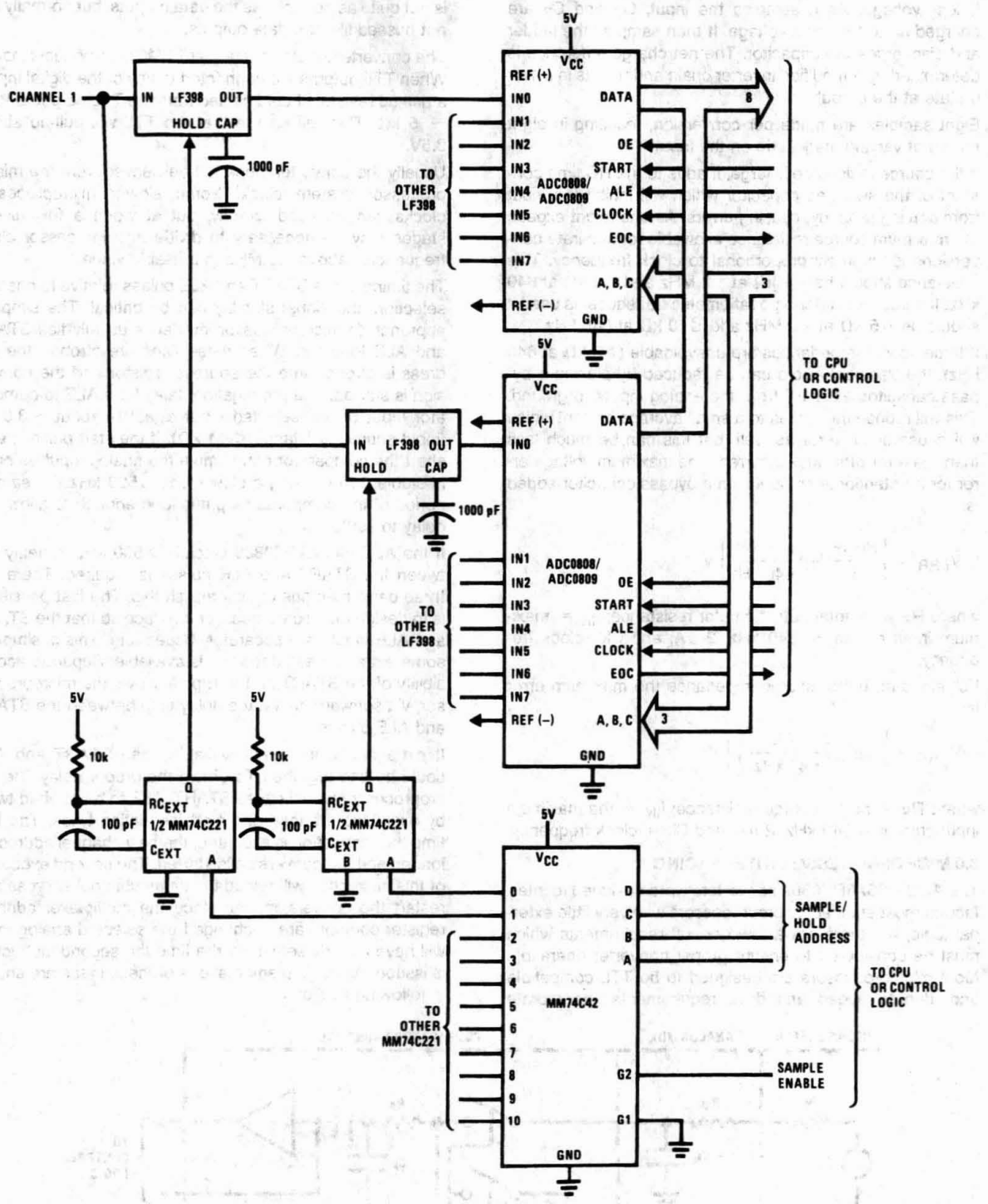


FIGURE 11. Parallel Data Acquisition with Sample/Holds

To understand the nature of these currents a short discussion of comparator operation is required. *Figure 12* shows a simplified model of the comparator and multiplexer. This comparator alternately samples the input voltage and the ladder voltage. As it samples the input, C_C and C_P are charged up to the input voltage. It then samples the ladder and discharges the capacitor. The net charge difference is determined by a modified inverter chain and results in a 1 or 0 state at the output.

Eight samples are made per conversion, resulting in eight spikes of varying magnitude on the input.

If the source resistance is large, it adds to the RC time constant of the switched capacitor which will inhibit the input from settling properly, causing errors. As one might expect, the maximum source resistance allowable for accurate conversions is inversely proportional to clock frequency. This resistance should be ≤ 1 kΩ at 1.2 MHz and ≤ 2 kΩ at 640 kHz. If a potentiometer-type ratiometric transducer is used it should be ≤ 5 kΩ at 1.2 MHz and ≤ 10 kΩ at 640 kHz.

If large source impedances are unavoidable (≥ 2 kΩ at 640 kHz), the transient errors can be reduced by placing a bypass capacitor ≥ 0.1 μF from the analog inputs to ground. This will reduce the spikes to a small average current which will cause some error as well, but this can be much less than the error otherwise incurred. The maximum voltage error for a potentiometer input with a bypass capacitor added is:

$$V_{ERR} \approx \left[\frac{R_{POT}}{5}(I_{IN})\frac{Ck}{640\ kHz}\right] V$$

where R_{POT} = total potentiometer resistance; I_{IN} = maximum input current at 640 kHz, 2 μA; and Ck = clock frequency.

For standard buffer source impedance the maximum error is:

$$V_{ERR} = \left[I_{IN}R_S\left(\frac{Ck}{640\ kHz}\right)\right] V$$

where R_S = buffer source resistance; I_{IN} = the maximum input current at 640 kHz, 2 μA; and Ck = clock frequency.

3.0 MICROPROCESSOR INTERFACING

The ADC0808/ADC0809 converters were designed to interface to most standard microprocessors with very little external logic, but there are a few general requirements which must be considered to ensure proper converter operation. Most microprocessors are designed to be TTL compatible and, due to speed and drive requirements, incorporate many TTL circuits. The data outputs of the ADC0808/ADC0809 are capable of driving one standard TTL load which is adequate for most small systems, but for larger systems extra buffering may be necessary. The EOC output is not quite as powerful as the data outputs, but normally it is not bussed like the data outputs.

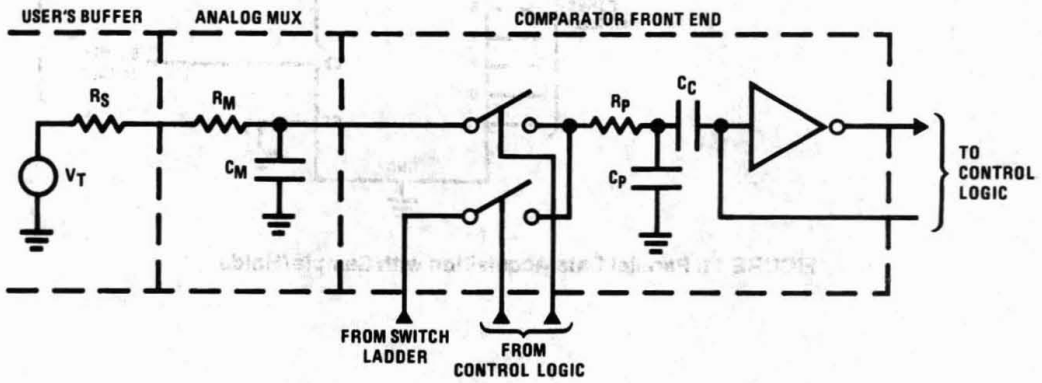
The converter inputs are standard CMOS compatible inputs. When TTL outputs are connected to any of the digital inputs a pull-up resistor should be tied from the TTL output to V_{CC}, $\sim$ 5 kΩ. This will ensure that the TTL will pull-up above 3.5V.

Usually the converter clock will be derived from the microprocessor system clock. Some slower microprocessor clocks can be used directly, but at worst a few divider stages may be necessary to divide microprocessor clock frequencies above 1.2 MHz to a usable value.

The timing of the START and ALE pulses relative to channel selection and signal stability can be critical. The simplest approach to microprocessor interfaces usually ties START and ALE together. When these lines are strobed the address is strobed into the address register and the conversion is started. The propagation delay from ALE to comparator input of the selected input signal is about ~ 3.0 μs (input source resistance $<<1$ kΩ). If the start pulse is very short the comparator can sample the analog input before it is stable. When using a slow clock ≤ 500 kHz the sample period of the comparator input is long enough to allow this delay to settle out.

If the ADC0808/ADC0809 clock is >500 kHz, a delay between the START and ALE pulses is required. There are three basic methods to accomplish this. The first possibility is to design the microprocessor interface so that the START and ALE inputs are separately accessible. This is simple if some extra address decoding is available. Separate accessibility of the START and ALE pins allows the microprocessor, via software, to set the delay time between the START and ALE pulses.

If extra decoding is not available, then START and ALE could be tied together. To obtain the proper delay, the microprocessor would cause START/ALE to be strobed twice by executing the load and start instruction twice. The first time this instruction is executed, the new channel address is loaded and the conversion is started. The second execution of this instruction will reload the same channel address and restart the conversion. But since the multiplexer address register contents are unchanged the selected analog input will have already settled by the time the second instruction is issued. Actual implementations of these ideas are shown in following sections.



TL/H/5623–8

FIGURE 12. Analog Multiplexer and Comparator Input Model

A third possibility when ALE and START are tied together is to stretch the microprocessor derived ALE/START pulse by inserting a one-shot at these inputs and creating a positive pulse >3 μs. Since ALE loads the multiplexer register on the positive going edge of the pulse and START begins the conversion on the falling edge, the width of the pulse sets the ALE to START delay time.

Most microprocessor interfaces would be designed such that a START pulse is issued by a memory or I/O write instruction, although a memory or I/O read can be used. The ALE strobe on the other hand, requires a write by the CPU when A, B, and C are connected to the data bus, and could use a read instruction if A, B, and C are connected to the address bus, but the software could get confusing. The logic to derive the OE strobe must be connected to the microprocessor so that a memory or I/O read instruction will cause OE to be pulsed. A read is required since the ADC0808/ADC0809 data must be read.

3.1 Interfacing to the 8080

The simplest interface would contain no address decoding, which may seem unreasonable; but if the system ports are I/O mapped, up to 8 of them can be connected to the CPU with no decoding. Each of the 8 I/O address lines would serve as a simple port enable line which would be gated with read and write strobes to select a particular port. This scheme is shown in *Figure 13*. A7 is the address line used and, whenever it is zero and an I/O read or write is low, the port is accessed. This implementation shows A, B, C connected to D0, D1, D2 causing the information on the data bus to select the channel, but A, B, and C could be connected to the address bus, with a loss of only 3 ports. Both decoding schemes are tabulated in *Figure 14*. (Remember A, B, C inputs are only valid when selecting a channel to convert, and are not used to read data.)

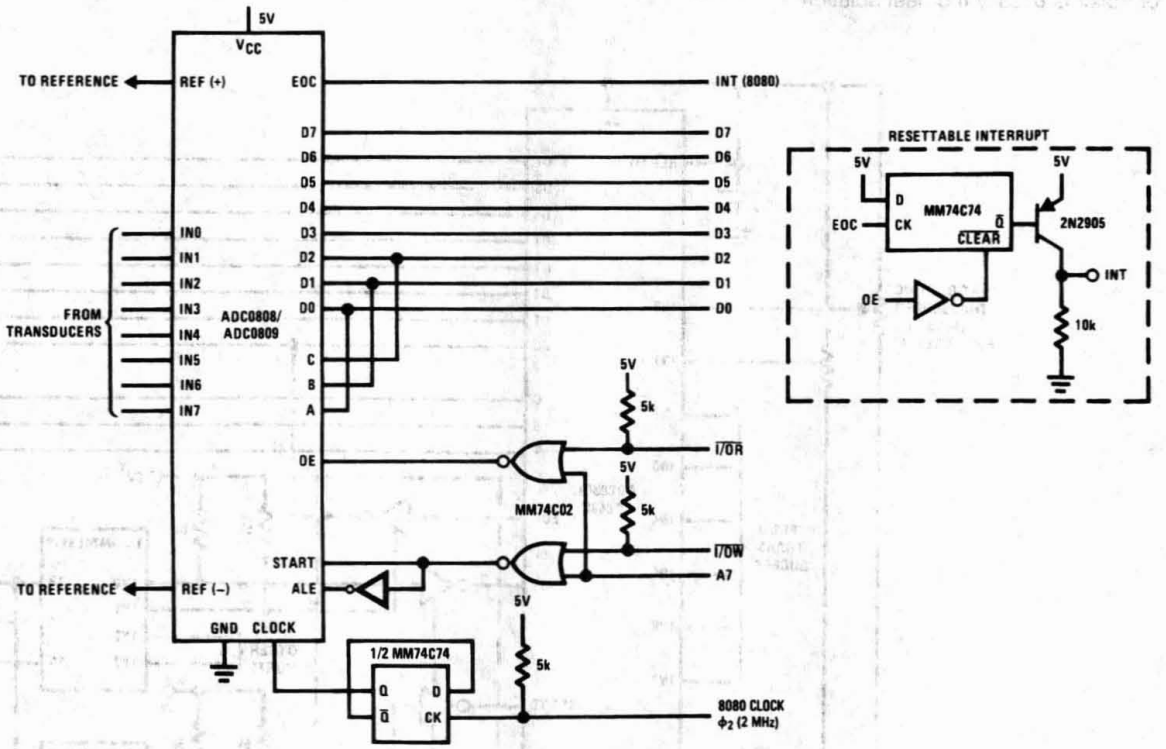


FIGURE 13. Minimum 8080/8224/8228 Interface

TL/H/5623–9

A7	A6	A5	A4	A3	A2	A1	A0	D2	D1	D0	Output Port Description
1	1	1	1	1	1	1	0	X	X	X	Spare Port
1	1	1	1	1	1	0	1	X	X	X	Spare Port
1	1	1	1	1	0	1	1	X	X	X	Spare Port
1	1	1	1	0	1	1	1	X	X	X	Spare Port
1	1	1	0	1	1	1	1	X	X	X	Spare Port
1	1	0	1	1	1	1	1	X	X	X	Spare Port
1	0	1	1	1	1	1	1	X	X	X	Spare Port
0	1	1	1	1	1	1	1	0	0	0	Channel 0 Port
0	1	1	1	1	1	1	1	0	0	1	Channel 1 Port
0	1	1	1	1	1	1	1	0	1	0	Channel 2 Port
0	1	1	1	1	1	1	1	0	1	1	Channel 3 Port
0	1	1	1	1	1	1	1	1	0	0	Channel 4 Port
0	1	1	1	1	1	1	1	1	0	1	Channel 5 Port
0	1	1	1	1	1	1	1	1	1	0	Channel 6 Port
0	1	1	1	1	1	1	1	1	1	1	Channel 7 Port

FIGURE 14a. Write Address Decoding for 8080 Output Ports (A, B, C Connected to D0, D1, D2)

A7	A6	A5	A4	A3	A2	A1	A0	Output Port Description
0	1	1	1	1	0	0	0	Channel 0 Port
0	1	1	1	1	0	0	1	Channel 1 Port
0	1	1	1	1	0	1	0	Channel 2 Port
0	1	1	1	1	0	1	1	Channel 3 Port
0	1	1	1	1	1	0	0	Channel 4 Port
0	1	1	1	1	1	0	1	Channel 5 Port
0	1	1	1	1	1	1	0	Channel 6 Port
0	1	1	1	1	1	1	1	Channel 7 Port
1	1	1	1	0	X	X	X	Spare Port
1	1	1	0	1	X	X	X	Spare Port
1	1	0	1	1	X	X	X	Spare Port
1	0	1	1	1	X	X	X	Spare Port

X = don't care

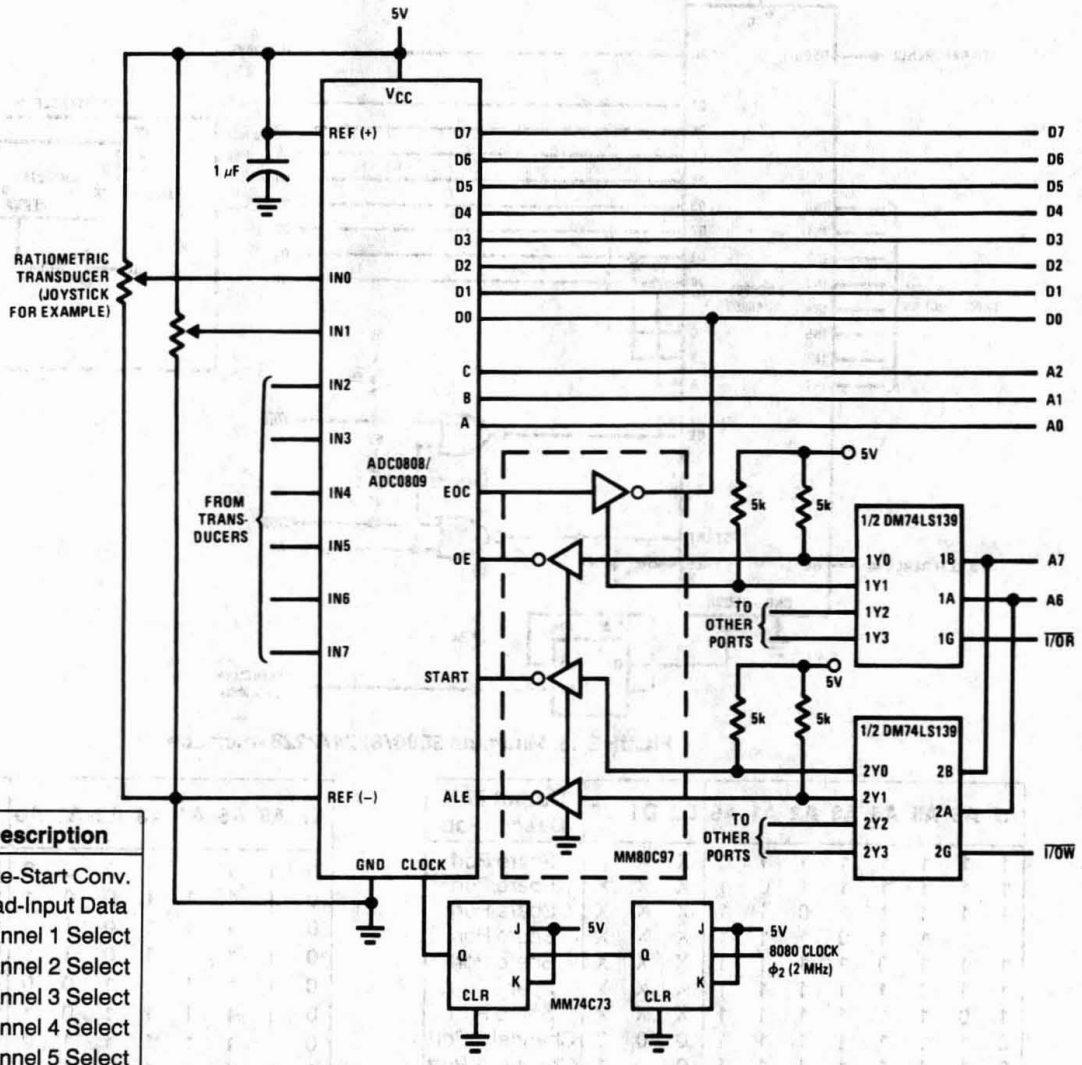
FIGURE 14b. Modified Write Address Decoding for 8080 Output Ports (A, B, C Connected to A0, A1, A2)

Two LSTTL NOR gates are used to generate the ADC0808/ADC0809 read/write strobes. When the 8080 writes to the ADC0808/ADC0809 the ALE and START inputs are strobed, loading and starting the conversion. When the CPU reads the ADC0808/ADC0809 the OE input is taken high, and the data outputs are enabled.

Figure 13 implements a simple interrupt concept where EOC is tied directly to the 8080 interrupt input. When the INS8228 is used and the INTA pin is tied high through a 1 kΩ resistor, the interrupt will cause a restart, RST, instruction to be executed, which will then cause a jump to a restart vector and execution of the interrupt routine. If a very simple multi-interrupt system is desired, a wire OR'ed configuration employing resettable latches as shown in *Figure 13's* inset can be used. In this simple design the MM74C74 is reset when the ADC0808/ADC0809 data is read. If more complicated interrupt structures are required, then an interrupt controller is usually the best solution.

The I/O port address structure for *Figure 13's* implementation is shown in *Figure 14a.* If the A, B, C inputs are tied to A0, A1, A2 inputs the port structure is as shown in *Figure 14b.* The later method makes each channel look like a separate port address, whereas if A, B, C are tied to the data bus the ADC0808/ADC0809 looks like one start conversion port address whose channel is selected by the 3-bit status word written to it on the data bus.

Figure 15 shows a slightly more complex interface, where the address is partially decoded by a DM74LS139, dual 2-4 line decoder which creates the read and write strobes to operate the converter. This design interfaces to the processor in a polled type of interface. An MM80C97 TRI-STATE buffer is used to buffer the EOC line to the data bus, as well as provide the correct level for the START, ALE, and OE pulses. The converter clock is a divided 8080 system clock.



Address A7–A0	Description
0 0 X X X X X X	Write-Start Conv.
0 0 X X X X X X	Read-Input Data
0 1 X X X 0 0 0	Channel 1 Select
0 1 X X X 0 0 1	Channel 2 Select
0 1 X X X 0 1 0	Channel 3 Select
0 1 X X X 0 1 1	Channel 4 Select
0 1 X X X 1 0 0	Channel 5 Select
0 1 X X X 1 0 1	Channel 6 Select
0 1 X X X 1 1 0	Channel 7 Select
0 1 X X X 1 1 1	Channel 8 Select
0 1 X X X X X X	Read-Input EOC

FIGURE 15. 8080/8224/8228 Interface Using Partial Decoding

Typically, the software to use *Figure 15* would first select the desired channel by writing the channel address to the ALE port address, 01XXXCBA, where X = don't care, and CBA is the channel address. Next the conversion is started by writing to the START address, 00XXXXXX. Now the processor must wait a few instruction cycles to allow EOC to fall. Once EOC falls, its status can be checked by reading the EOC line, address 01XXXXXX. When the EOC line is detected high again (a low on DO), the data can be read by accessing the OE port, address 00XXXXXX. As in the previous example the A, B, C inputs can be tied to D0, D1, D2 rather than A0, A1, A2, so that the information on the data bus selects the channel to be converted. *Figure 15* can be connected in an interrupt mode by incorporating the interrupt flip-flop of *Figure 13*.

A few typical utility routines to operate the ADC0808/ADC0809 application in *Figure 13* are shown in *Figure 16a*. These routines assume that the resettable interrupt flip-flop is used. *Figure 16b* illustrates some typical polled I/O routines for *Figure 15*. Notice that in *Figure 16a* the OUT START1 instruction is executed twice to allow the analog input signal to settle as discussed earlier.

```
;
;
; START CONVERSION (A, B, C CONNECTED TO D0, D1, D2)
;
CHANN1          EQU     7
START1          EQU     7FH
DATA            EQU     7FH
;
START:          LDA     CHANN1      ; LOAD CHANNEL ADDRESS INTO ACE
                OUT     START1      ; STORE IT TO ADC0808/ADC0809 AND START
                OUT     START1      ; RESTART ADC0808/ADC0809 TO ACCOUNT FOR
;                                   ; MULTIPLEXER DELAY
                EI                  ; ENABLE INTERRUPTS IF NOT ALREADY
                —       —           ; PROCESS PROGRAM
;
; INTERRUPT HANDLER ROUTINE
;
INTRP:          IN      DATA        ; READ DATA AND RESET INTERRUPT
                —       —           ; PROCESS DATA
                EI                  ; ENABLE INTERRUPTS IF DESIRED
                RET                 ; RETURN TO MAIN PROGRAM
```

FIGURE 16a. Typical 8080 Resettable Interrupt I/O Routines

```
;
; START CONVERSION (A, B, C CONNECTED TO A0, A2, A3) AND POLL EOC
; (FIGURE 15)
SELECT          EQU     40H         ; SELECT CHANNEL 0
START           EQU     00H         ; START CONVERTER
EOCIN           EQU     40H         ; READ EOC
DATA            EQU     00H         ; READ DATA
START:          OUT     SELECT      ; SELECT CHANNEL
                OUT     START       ; START CONVERSION
                N0P                 ; INSERT INSTRUCTIONS TO WAIT 0-8
                N0P                 ; CLOCK PERIODS OF ADC0808/ADC0809 CLOCK
                N0P                 ; FOR EOC TO DROP (8N0Ps MINIMUM)
                N0P
                N0P
;
; READ AND TEST EOC
;
STATUS:         IN      EOCIN       ; INPUT EOC BIT
                ANI     01H         ; MASK OUT OTHER BITS
                JZ      READY       ; IF INPUT BIT IS ZERO JUMP READY
                —       —           ; ELSE CONTINUE EXECUTING PROGRAM
; OR
; CONTINUOUS POLLING ROUTINE
;
STAT 2:         IN      EOCIN       ; INPUT EOC STATUS BIT
                ANI     01H         ; MASK OUT ALL BITS BUT D0
                JNZ     STAT 2      ; JUMP TO TRY AGAIN IF NOT READY
READY:          IN      DATA        ; IF READY INPUT DATA
                —       —           ; CONTINUE EXECUTING PROGRAM
```

FIGURE 16b. Typical Polled I/O Routines for ADC0808/ADC0809

The application in *Figure 17* uses a 6-bit bus comparator and a few gates to decode a read and write strobe. Viewed from the CPU this interface looks like a bidirectional data port whose address is set by the logic levels on the T_n inputs of the DM8131 comparator. When data is written to the ADC0808/ADC0809 the 3 least significant bits on the address bus define the channel to be converted. The rest of the bits are decoded to provide the START and ALE strobes. When the conversion is completed EOC sets the interrupt flip-flop, and when the data is read the interrupt is reset.

Both the decoder and the bus comparator methods of address decoding have their own advantages. Bus comparators will more completely decode addresses but are capable of only a limited number of port strobes. Decoders, on the other hand, provide less decoding but more port strobes. There is a trade off for minimum parts systems as far as which route to go, and it will depend on the CPU and type of system.

3.2 Interfacing to the 6800

The ADC0808/ADC0809 easily interface to more than one microprocessor. The 6800 can also be used to control the converter. The 6800 has no separate I/O address space so all I/O transfers must be memory mapped. In general more address decoding logic is required to ensure that the I/O ports don't overlap existing memory. For small systems a partial address decoding scheme is shown in *Figure 18*. Generally, if several ports are desired, a small block of memory would be set aside, as is accomplished by the DM8131. *Figure 18* also illustrates a typical 6800 interrupt scheme using a flip-flop and open collector transistor. The interrupt is reset when the data is read. If more ports are needed, a decoder could be added as shown in *Figure 19*. *Figure 19* also illustrates a polled I/O mode using TRI-STATE buffer to gate EOC onto the data bus. As with the INS8080 the A, B, C inputs of the ADC0808/ADC0809 can be connected to the address bus or the data bus.

The 6800 differs from the INS8080 in that the 6800 has a single read/write (R/$\overline{W}$) strobe and a valid memory address (VMA), whereas the INS8080 has separate read and write strobes ($\overline{I/OR}$ and $\overline{I/OW}$). Normally, to obtain a read pulse, VMA, R/$\overline{W}$ and ϕ_2 are gated together and, for a write R/$\overline{W}$ is inverted. ϕ_2 is the 6800 phase 2 system clock. Also notice that the 6800 $\overline{INT}$ interrupt input is active low. This enables a standard wired-OR open collector design to be implemented.

Figure 20 illustrates some typical 6800 software utility routines for either polled or interrupt interfaces. Again notice double start instructions.

3.3 Z80 Interface

Interfacing the Z80 to the ADC0808 is much the same as interfacing to an 8080/8224/8228 CPU group. CPU instruction timing is very similar, except the read/write control signals are slightly different. Instead of the $\overline{I/OW}$ write strobe there is the $\overline{IOREQ}$ and $\overline{WR}$ and instead of $\overline{I/OR}$, $\overline{IOREQ}$ and $\overline{RD}$ are supplied.

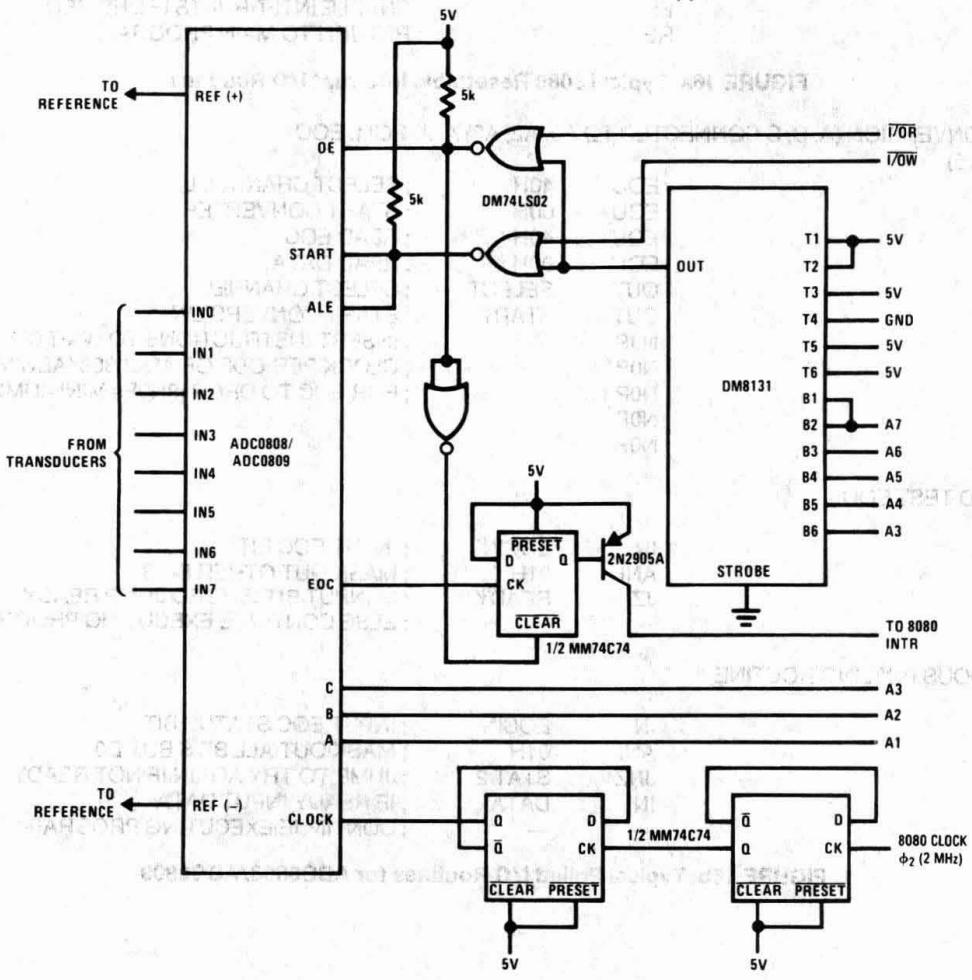


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FIGURE 17. Interrupt-Type 8080/8224/8228 Interface Using 6-Bit Bus Comparator

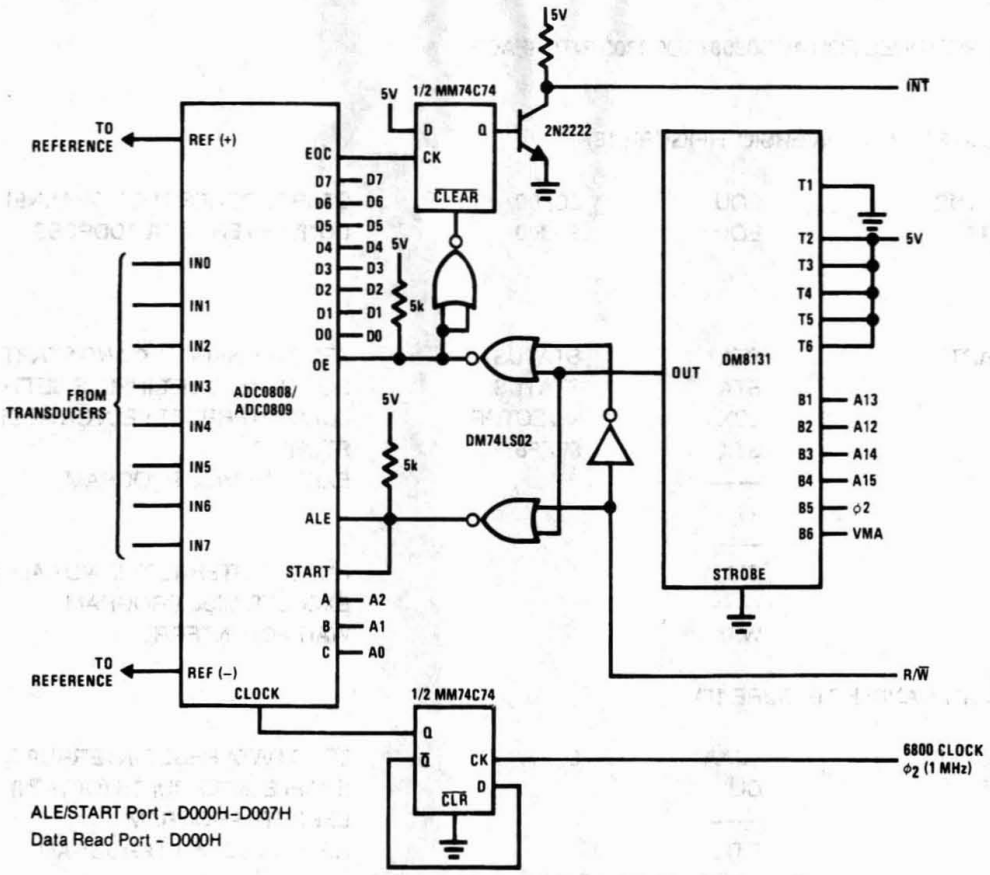

FIGURE 18. Typical 6800 Interface with Partial Address Decoding

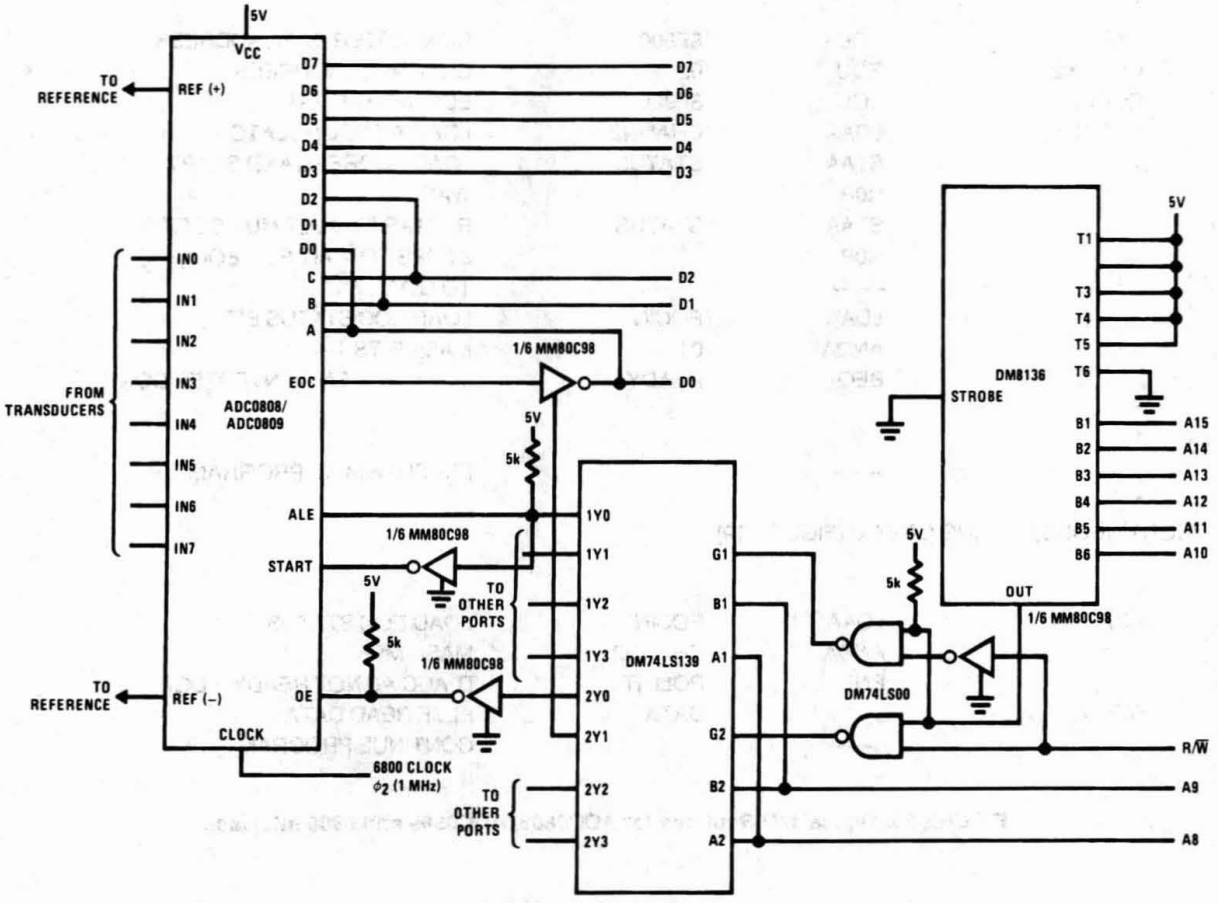

FIGURE 19. Full Decoded 6800 Interface Address

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```
        *
*UTILITY ROUTINES FOR ADC0808/ADC0809 INTERFACE
        *
        *
*LOAD AND START CONVERSION (FIGURE 18)
        *
STATUS      EQU     $D800     START ADDRESS FOR CHANNEL 0
DATA        EQU     $D800     CONVERTER DATA ADDRESS
        *
        *
        *
START       STA     STATUS    SELECT CHANNEL 0 AND START
            STA     STATUS    DO AGAIN TO LET INPUTS SETTLE
            LDX     #VECTOR   LOAD INTERRUPT VECTOR ADDRESS
            STX     $FFF8     STORE IT
            — —               EXECUTE MISC PROGRAM
            — —
            — —
            CLI               ENABLE INTERRUPT IF NOT ALREADY
            — —               EXECUTE MISC PROGRAM
            WAI               WAIT FOR INTERRUPT
        *
*INTERRUPT HANDLER (FIGURE 18)
        *
VECTOR      LDAA    DATA      LOAD DATA RESET INTERRUPT
            CLI               ENABLE INTERRUPTS (OPTION)
            — —               EXECUTE PROGRAM
            RTI               RETURN TO MAIN PROGRAM
        *
*START AND TEST CONVERSION POLLED MODE (FIGURE 19)
        *
DATA2       EQU     $F800     CONVERTER DATA ADDRESS
CHANN2      EQU     02        CHANNEL 2 ADDRESS
EOCIN       EQU     $F900     EOC INPUT PORT
START2      LDAA    CHANN2    LOAD A ACCUMULATOR
            STAA    STATUS    LOAD ADDRESS AND START
            N0P               WAIT
            STAA    STATUS    RESTART TO LET MUX SETTLE
            N0P               8 N0PS TO WAIT FOR EOC
            — —               TO GO LOW
            LDAA    EOCIN     LOAD EOC STATUS BIT
            ANDA    01        MASK BITS 1–7
            BEQ     READY     IF A = 0 THEN CONVERTER DONE
        *
        *
            — —               EXECUTE MISC PROGRAM
        *
*CONTINUOUS POLLING OF EOC (FIGURE 19)
        *
        *
POLLIT      LDAA    EOCIN     LOAD EOC STATUS
            ANDA    CHANN2    MASK MSBs
            BNE     POLL IT   IT ACC≠0 NOT READY, LOOP
READY LDAA          DATA      ELSE READ DATA
            — —               CONTINUE PROGRAM
            — —
```

FIGURE 20. Typical I/O Routines for ADC0808/ADC0809 and 6800 Interface

Figure 21 shows a very simple Z80 interface, which is similar to the INS8080 interface of *Figure 13*, except that the interrupt flip-flop design is closer to the 6800 designs. This is because the Z80 $\overline{INT}$ is active low as is the 6800, but the INS8080 INT is active high.

Figure 22 shows a fully decoded bus comparator design where the DM8131 decodes 5 address bits and the $\overline{IOREQ}$ I/O request strobe. Two NOR gates gate the $\overline{RD}$ and $\overline{WR}$ strobes for ALE, START and OE inputs.

4.0 CONCLUSION

Both the ADC0808 and the ADC0809 can be easily used in microprocessor controlled environments. Many sophisticated medium throughput applications can be handled with a minimum of extra hardware, but additional hardware can increase flexibility and simplify software. Putting both the multiplexer and A/D on the same chip frees the designer from matching multiplexers and A/Ds to implement a 7 or 8-bit accurate system. Design time and overall system cost can be reduced by using these low cost converters.

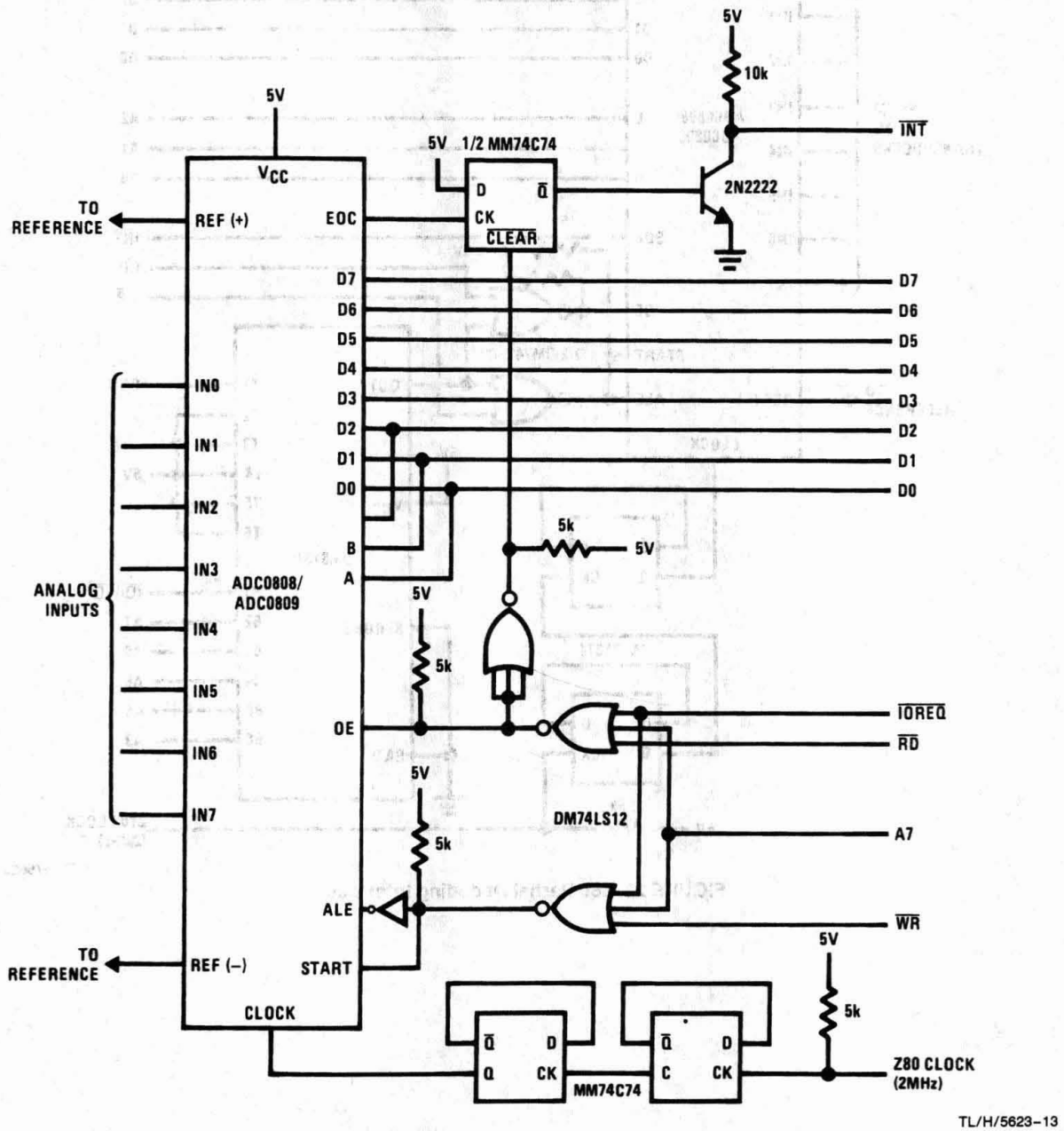

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FIGURE 21. Simple Z80 Interface

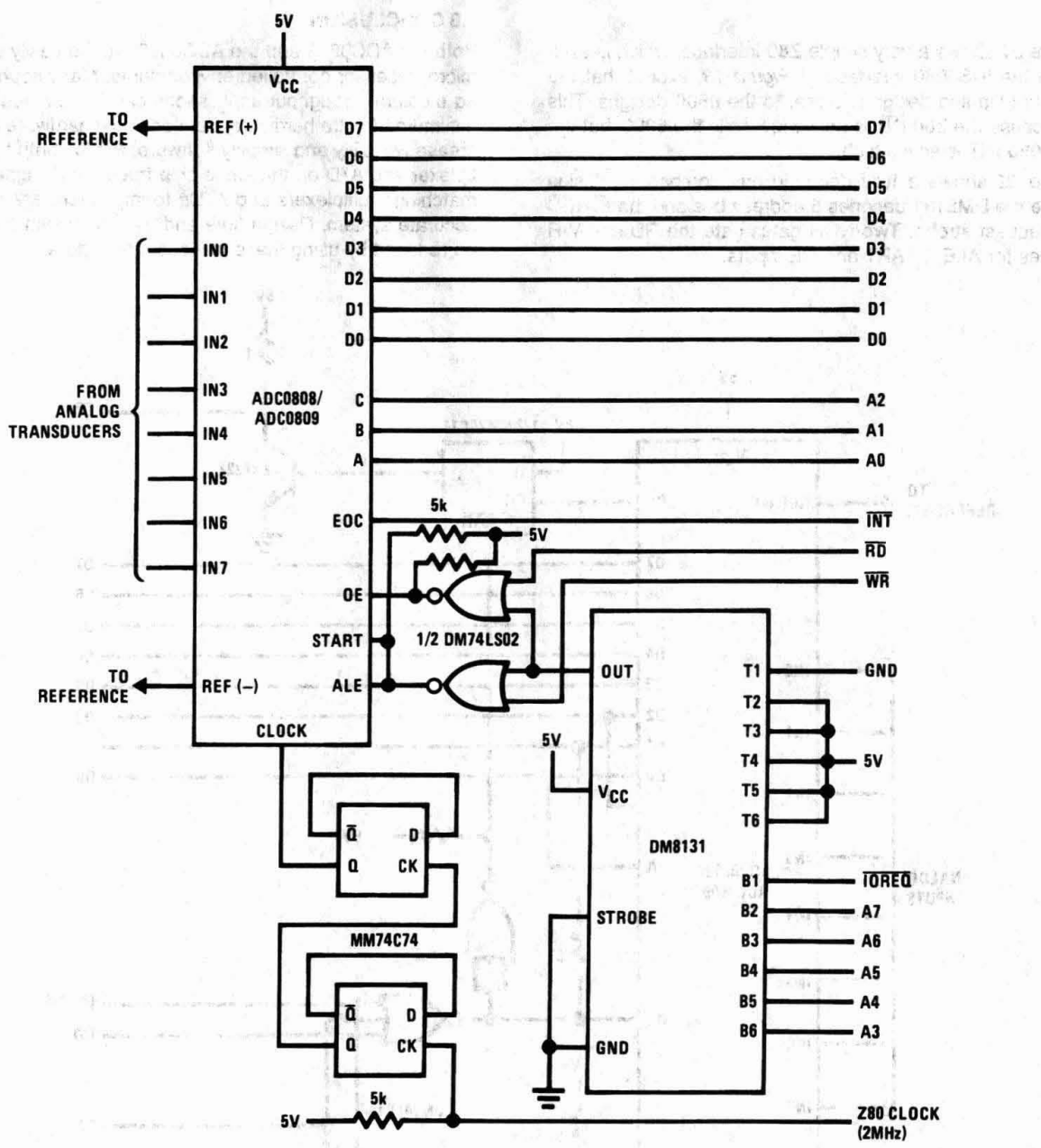

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FIGURE 22. Z80 Partial Decoding Interface

LH0024 and LH0032 High Speed Op Amp Applications

National Semiconductor
Application Note 253

INTRODUCTION

The LH0024 and LH0032 are very high speed general purpose operational amplifiers exhibiting 70 MHz bandwidths, 500 V/μs slew rates and 100 to 300 ns settling time to 0.1%. The LH0032 has the added advantage of FET input characteristics. Both, however, can drive loads with peak currents of 100 milliamperes (mA). The op amps are stable without external compensation when operating at closed-loop gains of more than 100. Both are constructed with thick film hybrid technology and are actively trimmed for consistent device performance. Table I summarizes the typical performance data for these op amps. Additional information may be obtained from the respective data sheets.

This note is divided into three parts, with the first giving a general description of the circuit topology of each op amp. In the following section, several high performance applications are discussed. Finally, the last section consolidates all application techniques into an integral design approach, much of which is applicable to any high frequency circuit.

LH0024 CIRCUIT DESCRIPTION

The LH0024 contains two gain stages: One is a differential NPN pair and the other is a single-ended PNP stage. The complete schematic is shown in *Figure 1*.

The input stage differential pair, Q8 and Q9, is biased at 6 mA by a current source made up of Q1, Q2, R3, and R5. First stage differential voltage gain is typically 2. Its output is applied differentially from base to emitter of the second stage transistor Q3 which has a gain of about 1,700. This stage also converts the differential signal to a single-ended output.

Current source Q5 and R4 provide 5 mA of DC bias current and a high impedance load to Q3. Overall amplifier gain is the product of the gains of the two stages—2 x 1700 = 3,400, or 71 dB.

The output complementary pair with class B bias provides a low impedance sourcing and sinking output drive. Although the class B bias contributes a small amount of cross-over distortion, it is barely detectable in closed loop operation.

LH0032 CIRCUIT DESCRIPTION

The LH0032 is a general purpose operational amplifier similar to the LH0024, but with JFET input devices instead of bipolar. As a result, the LH0032 DC input bias and offset currents are three orders of magnitude lower than the LH0024. Its output drive capability is improved due to the use of a larger package with lower thermal resistance, and its class AB output, which is normally biased on, virtually eliminates cross-over distortion.

The improved DC performance is due, in part, to the incorporation of monolithic dual junction FETs in the input stage of the LH0032, providing matched DC tracking and good

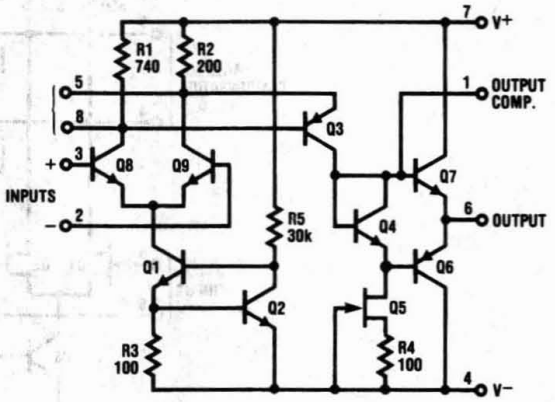

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FIGURE 1. Complete LH0024 Schematic Diagram

TABLE I. *Typical* Performance Characteristics

Parameter (T_A = 25°C)	Conditions	LH0024	LH0032	Units
Input Offset Voltage		2	2	mV
Input Bias Current		15 μA	10 pA	
Large Signal Voltage Gain	V_{OUT} = ±10V f = 1 kHz, R_L = 1 kΩ	71	70	dB
Slew Rate	A_V = +1, ΔV_{IN} = 20V	500	500	V/μs
Small Signal Rise Time	A_V = +1, ΔV_{IN} = 1V	8	8	ns
Settling Time to 1.0% of Final Value	A_V = −1, ΔV_{IN} = 20V	80	100	ns
Settling Time to 0.1% of Final Value		275	300	ns
Unity Gain Bandwidth	(uncompensated)	70	70	Mhz

common-mode input characteristics. First stage operating current is set at 6 mA by the current source made up of transistors Q8 and Q9 and resistors R4 and R9, as shown in *Figure 2*. The first stage voltage gain is:

$$A_V \text{ (1st stage)} = g_m R_L = 1.4 \quad (1)$$

Where: gm = 3.5 mmho

$$R_L = R_1 \parallel (\beta_3 + 1)(r_{e3} + 2R_3)$$

The second stage consists of two identical pairs of differential PNP transistors in a cascode configuration. Each side operates at 5 mA set by the emitter resistor R3 and the bias of the first stage. The differential amplifier Q3 and Q4 feeds the common-base pair Q5 and Q6 with the base voltage fixed at $V^+ - 1.9$ volts by the diode string Q13–A15. Thus the collectors of the differential pair Q3 and Q4 are held at one V_{BE} drop more positive than the reference voltage. Any signal amplified by the differential stage produces only a very small change in Q3 nd Q4 collector voltage. Consequently, the Miller effect on Q3 and Q4 (base-to-collector capacitances) is virtually eliminated. Using hybrid π model of the transistor, the voltage gain of the cascode stage may be approximated as:

$$A_V \text{ (2nd stage)} = g_{m4} \times R_{eq} \cong 1{,}400 \quad (2)$$

Where: $g_{m4} = \dfrac{5 \text{ mA}}{0.026\text{V}}$

$$R_{eq} = \frac{1}{h_{ob6}} \parallel \frac{1}{h_{oe10}} \parallel (\beta_{11} + 1)(R_L)$$

Notice that the full differential gain is realized with the use of the current mirror Q10 and Q16, which also provides high active load resistance to the PNP cascoded pair, resulting in high amplifier gain.

The collector output of the cascode stage is buffered by a pair of complementary emitter follower transistors, Q11 and Q12. This class AB output stage is normally biased at 1 mA by the 1.8 V_{BE} voltage produced by Q7, R5, and R6. The emitter degeneration resistors provide protection from thermal runaway.

APPLICATIONS OF THE LH0024/LH0032

Applications of the high speed LH0024 and LH0032 range from video amplifiers to sampling circuits. The applications described below include high speed sample and hold circuits, photo-detector amplifiers, fast settling digital to analog converters and buffered amplifiers.

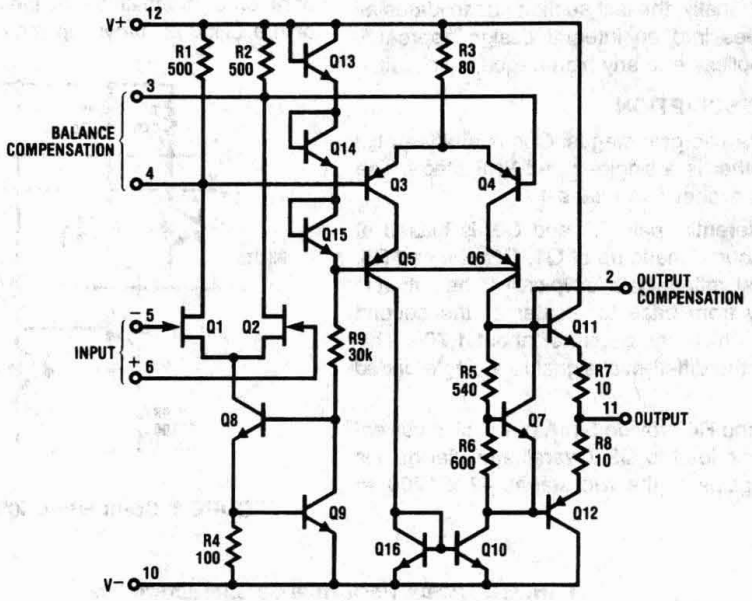

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FIGURE 2. Complete LH0032 Schematic Diagram

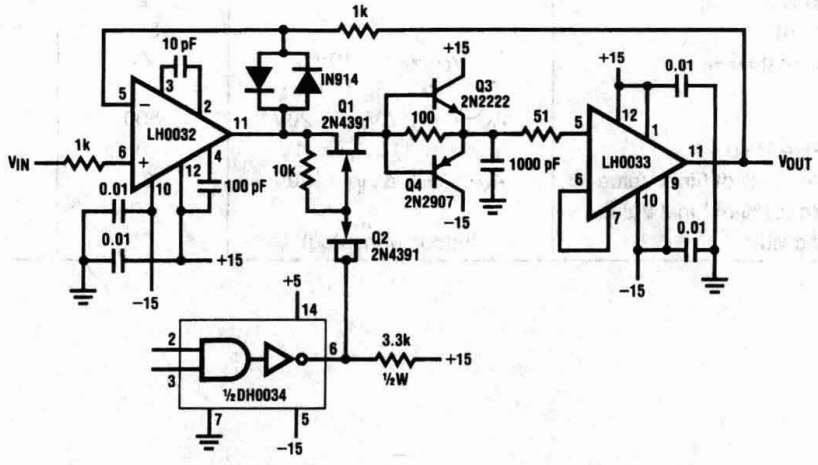

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FIGURE 3. High Speed Sample and Hold Circuit

A High Speed S/H Circuit

High Speed sample-and-hold circuits require high slew rate and fast settling amplifiers. The LH0032 is ideal for these applications. An example is shown in *Figure 3*.

The complementary emitter-follower Q3 and Q4 sources or sinks large peak current to rapidly charge or discharge the hold capacitor during step changes, thus effectively buffering the FET switch, Q1, whose $r_{D(ON)}$ would otherwise slow the charge time. The LH0033 FET-input amplifier buffers the output signal, providing 100 mA drive capability.

The circuit exhibits a 10V acquisition time of 900 ns to 0.1% accuracy and a droop rate of only 100 μV/ms at 25°C ambient condition. An even faster acquisition time can be obtained using a smaller value hold-capacitor. By decreasing the value from 1000 pF to 220 pF, the acquisition time improves to 500 ns for a 10V step. However, droop rate increases to 500 μV/ms.

Fiber Optic Transmitter-Receiver Applications

Many fiber optic applications require analog drivers and receivers operating in the megahertz region where many so-called wide-band op amps simply run out of steam. Packed with 70 MHz gain-bandwidth product (unity gain compensated), the LH0032 is quite suitable for optical communication applications up to 3.5 MHz. *Figure 4* demonstrates a complete analog transmission system using this device.

The transmitter incorporates the LF356 to drive the light emitter. The LED is normally biased at 50 mA operating current. The input is capacitively coupled and ranges from 0V to 5V, modulating the LED current from 0 mA to 100 mA. The circuit can be easily modified to operate from a single +15V power supply. The only requirement is that the amplifier must be biased within the input common mode range.

The receiver circuit uses an LH0032 configured as a transimpedance amplifier. A photodiode with 0.5 amp per watt responsivity such as the Hewlett-Packard type HP5082-4220, generates 50 mV signal at the receiver output for 1 μW of light input.

Expectedly, the bandwidth of the entire optical link rests on the receiver circuit. Therefore, if the response time is to be optimized, one should reverse bias the photodiode to minimize junction capacitance. As a result, rise time improves more than 2 orders of magnitude. Next, the feedback resistor value should be chosen to be as large as possible in order to maximize sensitivity within the limits of allowable bandwidth degradation. Using 100 kΩ feedback resistor, the maximum system bandwidth is 3.5 MHz.

Fast Settling 12-BIT D/A Converter

A high resolution, fast-settling DAC can be constructed using the LH0032. Its low input bias current causes no significant DC error in conversion accuracy. Great care must be exercised in circuit layout to assure highest performance. A single point analog ground should be used with the digital ground separated. A complete circuit with 12-bit resolution is shown in *Figure 5*. The converter typically settles to ½ LSB in 800 ns for a 10V full-scale swing. Similarly, 10-bit or 8-bit resolution DACs may be constructed using the DAC1020 or DAC0808, respectively.

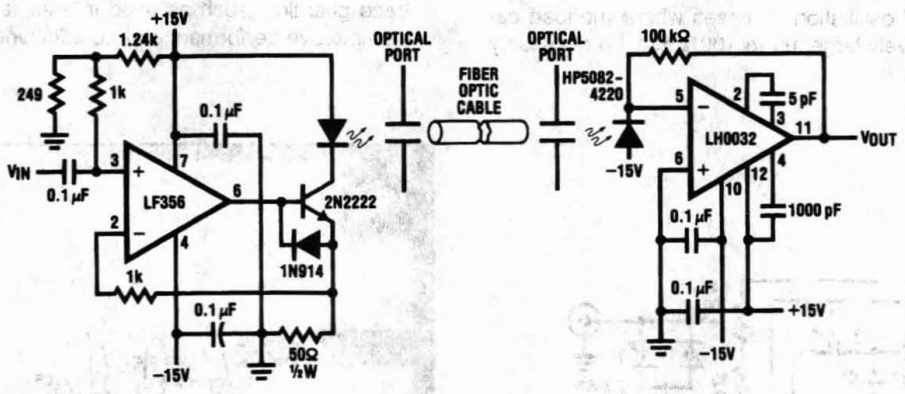

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FIGURE 4. Fiber Optic Link

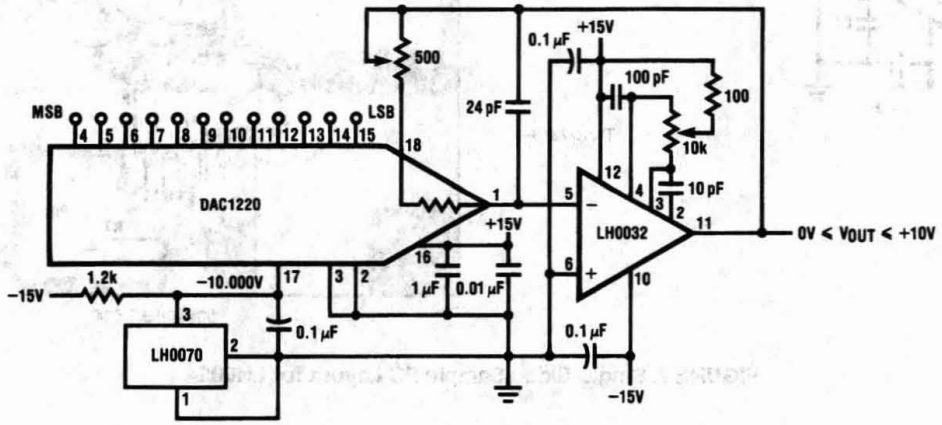

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FIGURE 5. Fast Settling DAC

Buffered Amplifier

Whenever higher output current is required, a buffer amplifier may be added to the loop as shown in *Figure 6*. The LH0033 boosts the output drive capability to ±100 mA continuous and ±400 mA peak.

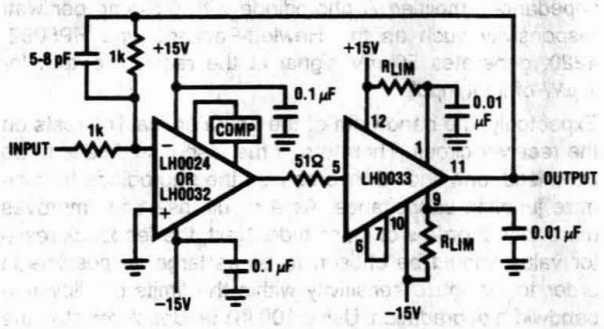

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FIGURE 6. Wide Band Amplifier with 100 mA Output Capability

Despite its 100 MHz bandwidth, the LH0033 introduces about 15 degrees of phase lag at the LH0032 unity-gain frequency of 70 MHz. As a result, phase margin is degraded by the same amount. Slight overcompensation may be required in order to restore adequate phase margin. One way is to increase the feedback capacitor from 5 pF to a slightly larger value, 6 to 8 pF should be sufficient. If the load is predominantly capacitive, the total phase shift of the buffer stage may exceed 180° and appear as negative impedance seen looking into the input of the buffer. The 51Ω resistor restores some real resistance to alleviate this condition and prevents potential oscillation. In cases where the load capacitance is relatively large, up to 100Ω may be necessary to compensate for it.

DESIGN CONSIDERATIONS

Optimizing LH0024/32 Performance

The LH0024 and LH0032 allow considerable flexibility in designing high performance circuits if care is taken in the way they are used and implemented. Indeed, the printed circuit board layout in high frequency circuits is as important as the design of the hybrid devices themselves.

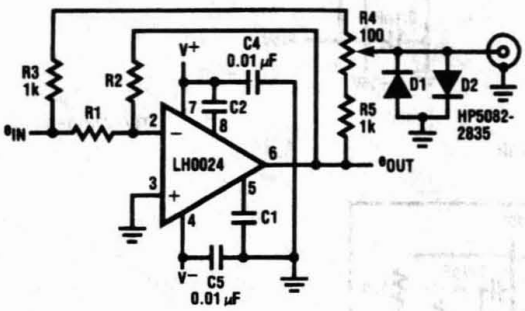
It is good practice to use ground plane PC board design. It provides a low resistance, low inductance path, and reduces stray signal coupling to sensitive circuitry. A double-sided ground plane is usually better and should be considered.

In addition, signal trace connections should be kept as short and wide as possible. Avoid closely-spaced parallel signal traces as signal cross-coupling may occur. Circuit elements should be placed close to the amplifier, particularly critical components that directly affect the amplifier's frequency response, such as compensation capacitors. If at all possible, one should maintain single point ground throughout the circuit to minimize signal phase delay.

Examples of single-sided PC layouts for the LH0024 and LH0032 are shown in *Figure 7* and *Figure 8*, respectively. The layouts include a settling time test circuit, optional inverting or noninverting mode. Note that the summing junction side of the feedback resistor is kept very close to the device pin, thus minimizing lead capacitance. The power supply decoupling capacitors should also be kept close to the device pins, preferably 3/8 of an inch.

Input Guarding and Bootstrapping

In applications where input leakage currents are important, trace guarding, such as used in sample and hold circuits, can improve performance at no additional cost.



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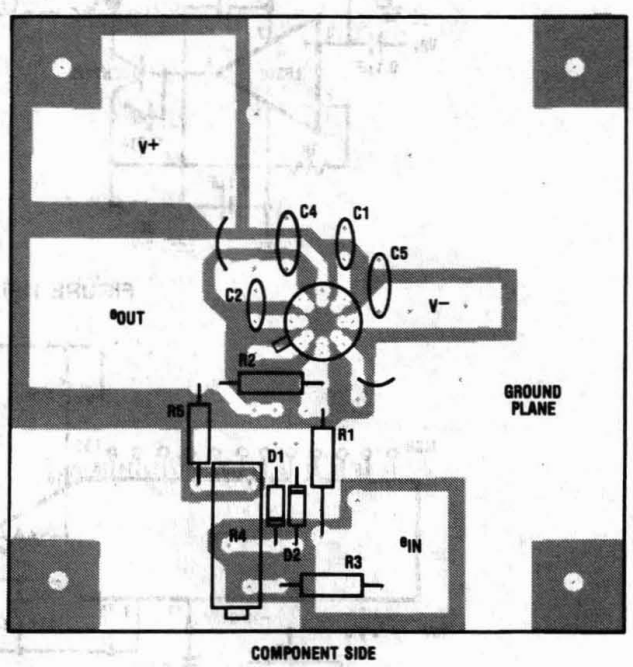

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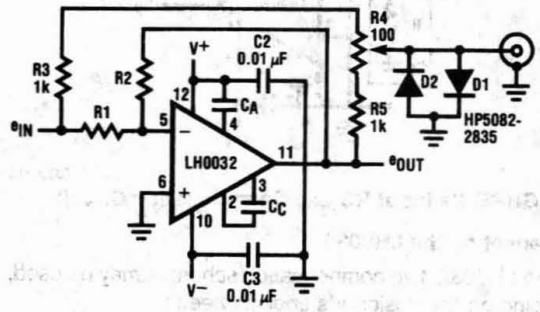
FIGURE 7. Single-Sided Sample PC Layout for LH0024



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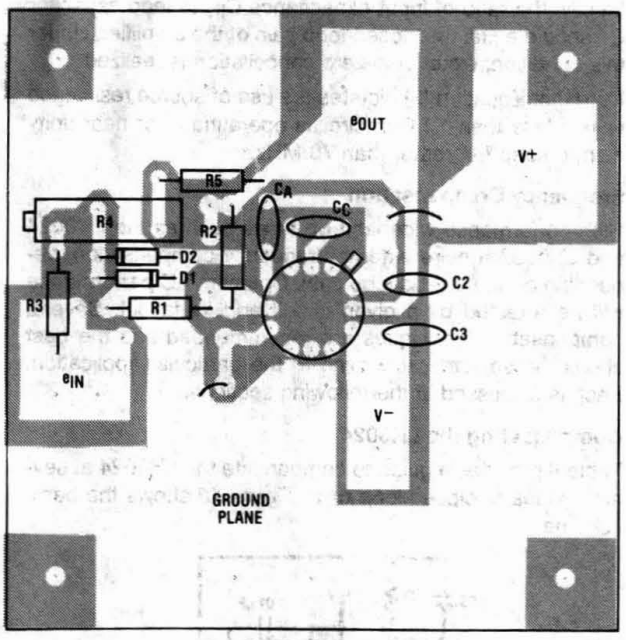

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FIGURE 8. Single-Sided Sample PC Layout for LH0032

The guard conductor serves to intercept leakage currents from inputs to the surrounding circuit. It is most effective when it is driven to the same potential as the guarded circuit. *Figures 9* and *10* show how the technique is implemented in inverting and non-inverting configurations, respectively.

One other benefit of input guarding is the reduction of input stray capacitance effects. A comprehensive discussion of this technique is described in Application Note AN-63.

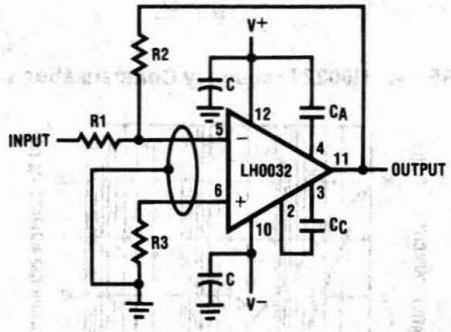

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FIGURE 9. Guarding Inverting Figure Amplifier

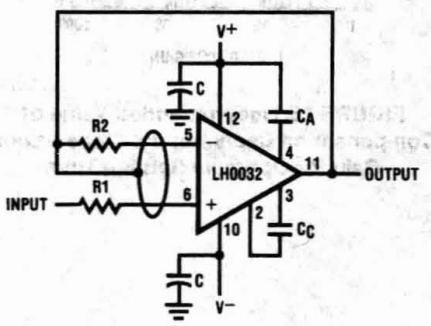

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FIGURE 10. Guarding Non-Inverting Unity Gain Amplifier

Input Capacitance Cancellation

The intrinsic input capacitance of the amplifier cannot be totally eliminated by the input guarding technique. This input capacitance introduces a pole in the amplifier response at the frequency given by:

$$f_p = \frac{1}{2\pi R_S C_{IN}} \quad (3)$$

This pole may become extremely important as, for example, a C_{IN} of 5 pF (typical input capacitance of the LH0024 and LH0032) with a 500Ω effective source resistance creates a pole at about 64 MHz—well before the amplifier's natural frequency response rolls off to unity gain at 70 MHz. If closed-loop gain is unity, more than 135° total phase lag is introduced even before the crossover frequency is reached and will destroy phase margin. Oscillation is certain to occur. The solution is to cancel its effect. As shown in *Figure 11*, the lead capacitor C1 across the feedback resistor is used to introduce a zero in the loop response such that it exactly cancels the pole caused by the input RC network.

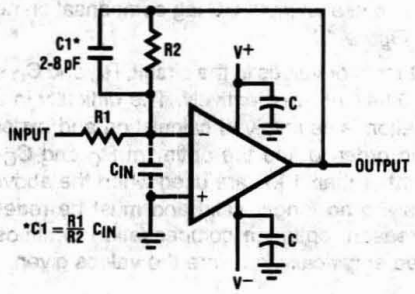

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FIGURE 11. Compensating Amplifier Input Capacitance

Ideally, the ratio of input capacitance C_{IN} to lead capacitor C1 should equal the closed-loop gain of the amplifier. Under this condition, exact pole-zero cancellation is realized.

Note that Equation (3) dictates the use of source resistance values less than 1 kΩ in circuits operating at or near unity gain to keep f_P greater than 70 MHz.

Frequency Compensation

High-performance wideband op amps such as the LH0024 and LH0032 require external frequency compensation, depending on the closed-loop gain. Optimum AC performance will be affected by a given circuit and its layout. Several compensation techniques are recommended and the best should be selected according to the particular application. Each is discussed in the following sections.

Compensating the LH0024

Table II provides a guide to compensate the LH0024 at several values of closed-loop gain. *Figure 12* shows the basic scheme.

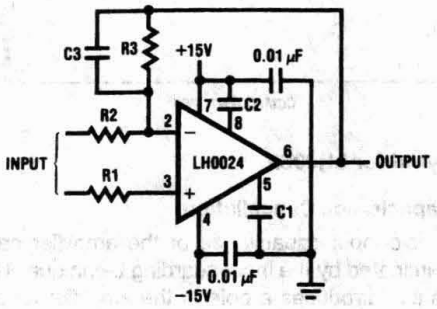

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FIGURE 12. LH0024 Frequency Compensation Circuit

When operating with closed-loop gain of −1, C3 is required and may need slight adjustment to completely cancel the input capacitance of the device, typically 5 pF.

TABLE II

Closed-Loop Gain	C1	C2	C3
100	0	0	0
20	0	0	0
10	0	20 pF	1 pF
1	30 pF	30 pF	5 pF

An alternate technique for compensation at a closed-loop gain of 1 is to use an input RC lag compensation network as shown in *Figure 13*.

With 1 kΩ resistor values in the circuit, R_C and C_C should be 82Ω and 0.047 μF, respectively. The difficulty in using this compensation is its involved calculation and experimenting required in order to find the optimum R_C and C_C values if resistors other than 1 kΩ are used when the above R_C and C_C values are no longer valid and must be redetermined. For this reason, optimum compensation is almost always determined empirically, as were the values given.

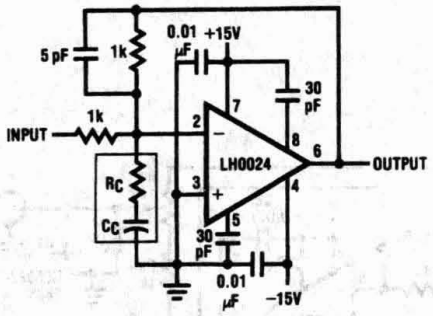

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FIGURE 13. Input RC Lag Compensation Circuit

Compensating the LH0032

With the LH0032, two compensation schemes may be used, depending on the designer's specific needs.

The first technique is shown in *Figure 14*. It offers the best 0.1% settling time for a ±10V square wave input. The compensation capacitors C_C and C_A should be selected from *Figure 15* for various closed-loop gains. *Figure 16* shows how the LH0032 frequency response is modified for different value compensation capacitors.

Although this approach offers the shortest settling time, the falling edge exhibits overshoot up to 30% lasting 200 to 300 ns. *Figure 17* shows the typical pulse response.

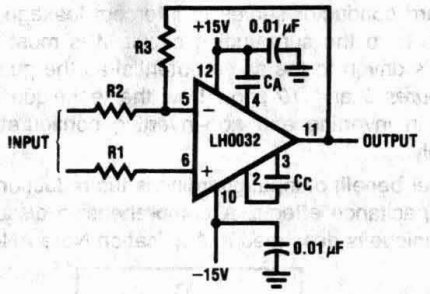

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FIGURE 14. LH0032 Frequency Compensation Circuit

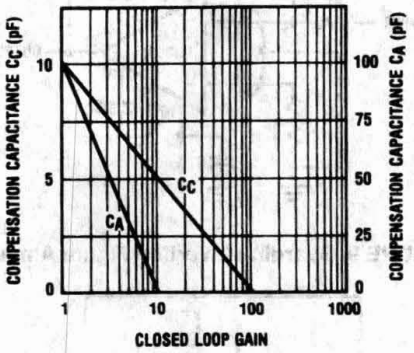

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FIGURE 15. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Settling Time

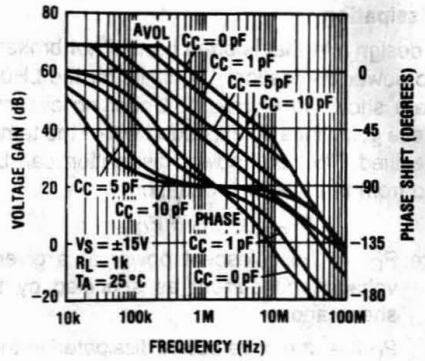

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FIGURE 16. The Effect of Various Compensation Capacitors on LH0032 Open Loop Frequency Response

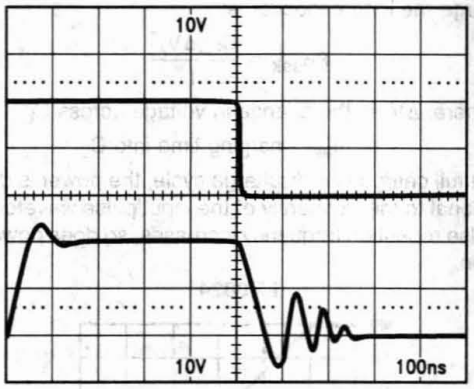

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FIGURE 17. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: T_A = 25°C, C_C = 10 pF, C_A = 100 pF

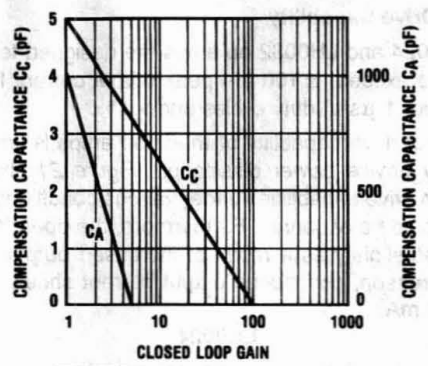

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FIGURE 18. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Slew Rate

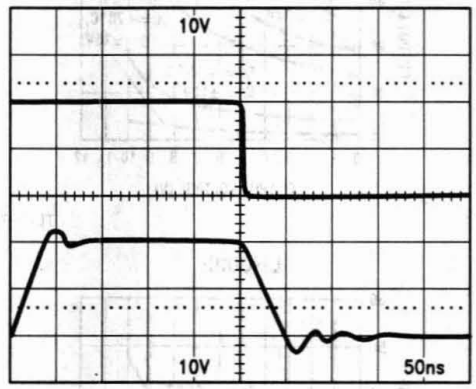

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FIGURE 19. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: C_C = 5 pF, C_A = 1000 pF

If obtaining minimum ringing at the falling edge is the primary objective, a slight modification to the above is recommended. It is based on the same circuit as that of *Figure 14*.

The values of the unity gain compensation capacitors C_C and C_A should be modified to 5 pF and 1000 pF, respectively. *Figure 18* shows the suitable capacitance to use for various closed-loop gains. The resulting unity gain pulse response waveform is shown in *Figure 19*. The settling time to 1% final value is actually superior to the first method of compensation. However, the LH0032 suffers slow settling thereafter to 0.1% accuracy at the falling edge, and nearly four times as much at the rising edge, compared to the previous scheme. Note, however, that the falling edge ringing is considerably reduced. Furthermore, the slew rate is consistently superior using this compensation because of the smaller value of Miller capacitance C_C required. Typical improvement is as much as 50%. A more detailed discussion of this effect is provided in the Slew Response section of this Application Note.

The second compensation scheme works well with both inverting or non-inverting modes. *Figure 20* shows the circuit schematic, in which a 270Ω resistor and a 0.01 μF capacitor are shunted across the inputs of the device. This lag compensation introduces a zero in the loop modifying the response such that adequate phase margin is preserved at unity gain crossover frequency. Note that the circuit requires no additional compensation.

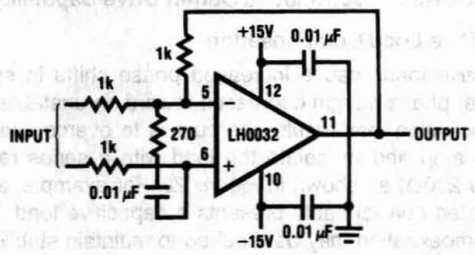

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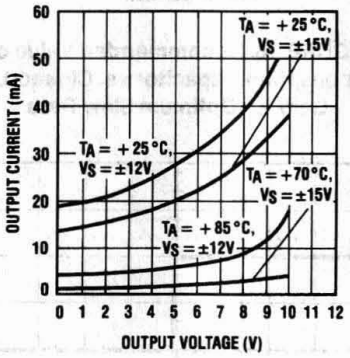
FIGURE 20. LH0032 Non-Compensated Unity Gain Compensation

Output Drive Capability

The LH0024 and LH0032 op amps are designed to deliver, but not to exceed, ±100 mA peak output current for durations under 1 μs at duty cycles under 1%.

The output drive capability of these op amps is limited primarily by device power dissipation. *Figure 21* shows the maximum drive capabilities under various conditions. These limits should be observed. Furthermore, the open loop gain decreases slightly as a result of increased output loading. For this reason, continuous output current should be kept under 50 mA.

LH0024



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LH0032

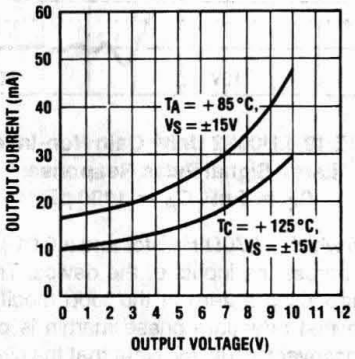

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FIGURE 21. Continuous Output Drive Capability

Capacitive Load Compensation

Capacitive loads cause increased phase shifts in such a way that phase margin decreases toward an unstable state and oscillating may result. The cure is to overcompensate the op amp and to isolate the load with a series resistor (100 to 200Ω) as shown in *Figure 22*. For example, an unterminated coaxial cable presents a capacitive load. Slight overcompensation may be required to maintain stability.

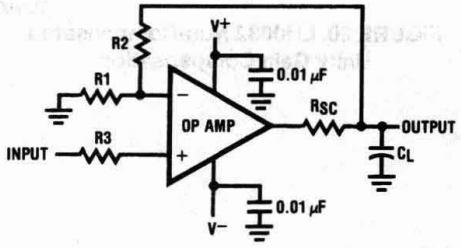

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FIGURE 22. Output Protection when Driving Capacitive Load

Power Dissipation

A simple design rule that is often bent, if not broken, is that relating to power dissipation. The limits for the LH0024 and LH0032 are shown in *Figure 23*. Under no circumstances should these guidelines be exceeded within the temperature range specified. The total power dissipation can be easily calculated from the following equation:

$$P_{Total} = P_Q + P_{Out} \quad (4)$$

Where: P_Q = the quiescent power at a given supply voltage and current as specified by the data sheet, and,

P_{Out} = the drive power dissipated in the device output stage, computed as the net rms collector-emitter voltage of the output transistor times the load current.

Determining power dissipation when driving a capacitive load is more involved. The peak power required to charge or discharge the load capacitor is:

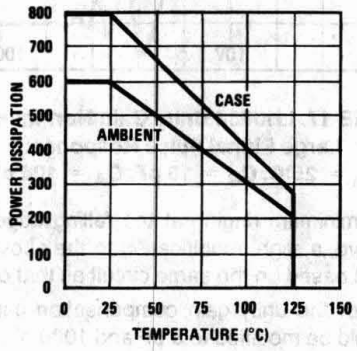
$$P_{Peak} = \frac{C_L (\Delta V)^2}{t} \quad (5)$$

Where: ΔV = the change in voltage across C_L.

t = I_{Peak} charging time into C_L.

Over a full charge and discharge cycle, the power is directly roportional to the frequency of the input pulse waveform. As the pulse repetition frequency increases, so does power dissipation.

LH0024



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LH0032

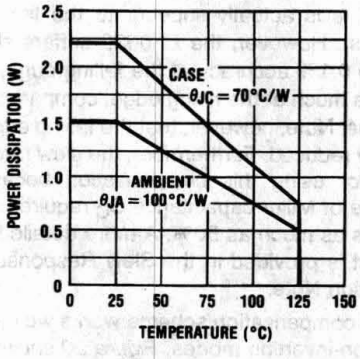

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FIGURE 23. Maximum Power Dissipation

Short Circuit Protection

Since the LH0024 and LH0032 have no internal short circuit protection, their relatively high drive capability can sustain current levels sufficient to destroy the devices if high frequency oscillation is induced. This can occur with a large capacitance load. To design in protection, a current limiting resistor R_{SC} should be inserted at the output of the amplifier inside the feedback loop as shown in *Figure 22*. The value of R_{SC} can be determined from the following equation:

$$R_{SC} = \frac{V^+}{I_{SC}} \quad (6)$$

Where: V^+ is the power supply voltage.

Heat Sinking Considerations

Under severe environmental and electrical operating conditions, a low thermal resistance heat sink should be used to assure safe operation. The following is a list of heat sinks from various sources recommended for the TO-8 case style:

Thermalloy 2240A, 33°C/W

Wakefield 215CB, 30°C/W

IERC, UP-TO 8-48CB, 15°C/W

Heat sinks for the TO-5 case style are readily available from many manufacturers. A reasonably priced clip-on unit from Thermalloy, Model 2228B, offers modest thermal resistance of 35°C/W.

Case Grounding

Grounding the case of the device offers improved immunity from circuit cross-talk, but it compromises additional stray capacitance to every device pin (usually 1–2 pF). In the rare situation where case grounding is required, slight recompensation may be necessary. However, most applications are not demanding enough to warrant its use.

There are several ways to strap, or ground the case. For the LH0032, the best approach is to solder a small metal washer or a small piece of wire between the base of the device metal can and the base of an unassigned lead post. Dedicating pin 7 of the LH0032 for this purpose is recommended, although any other "no connection" pin is acceptable. High temperature solder should be used to avoid solder reflow during normal assembly operations.

The LH0024 has no unused pins available, and thus is not readily adaptable to case strapping. An alternative approach is to use an electrically conductive heatsink with a PC board-mountable option, such as Thermalloy type 2230C-5.

In all uses of case grounding, be on the lookout for ground-induced noise into the signal path. In short, be sure the ground is a *quiet* ground.

Power Supply Bypass

Power supply pins must be bypassed in all cases to prevent oscillation. A 0.01 μF to 0.1 μF disc or monolithic ceramic capacitor at each supply pin to ground is adequate. The capacitors should be placed no more than ½ inch from the device pins.

Adjustment of Offset Voltages

When required, the offset voltage of the operational amplifiers may be nulled using a balance potentiometer as shown in *Figure 24*. The 100Ω series resistors prevent any adverse oscillation or malfunction when the pot is shorted to either end of the adjustment range.

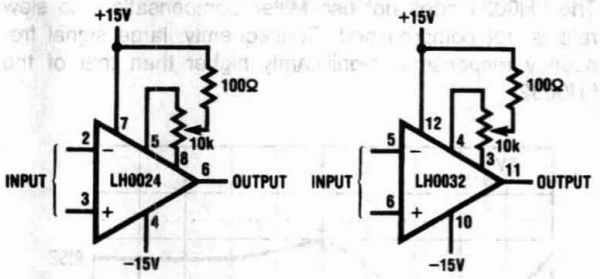

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FIGURE 24. Offset Voltage Adjustment

Slew Response Improvement

Slew rate is the internally limited maximum rate of rise, or fall, at maximum amplifier output swing when driven by a large signal step input. It is primarily limited by the operating current of the input stage. When overdriven by a step fuction, the input stage operating current charges or discharges the effective circuit capacitance of the second stage. The rate of charge is:

$$\frac{dV}{dt} = \frac{I_{Input\ Stage}}{C_{Node}} \quad (7)$$

In the case of the LH0032, where Miller Compensation is used, the external capacitance adds to the internal circuit capacitance, resulting in reduced slew rate. *Figure 25* illustrates this effect as a function of the capacitance value.

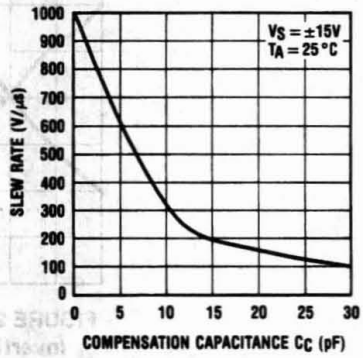

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FIGURE 25. LH0032 Slew Rate vs. Frequency Compensation Capacitance

Figures 26, *27*, and *28* demonstrate the rising and falling slew capabilities of the LH0024 and LH0032. Notice the improved slew rate peformance of the LH0032 using the alternative compensation technique in *Figure 28* compared to *Figure 27*. The difference is due to the smaller Miller capacitance used in the former.

The LH0024 does not use Miller Compensation, so slew rate is not compromised. Consequently, large signal frequency response is significantly higher than that of the LH0032.

Finally, power supply voltage affects slew rate. As the voltage decreases, input stage operating current decreases accordingly. The net effect is a reduction in the slew rate as the available charging current drops off. *Figure 29* shows the typical slew response of each op amp as a function of supply voltage.

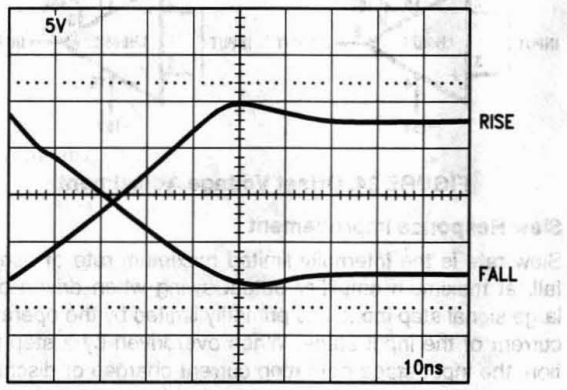

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FIGURE 26. LH0024 Slew Response, Unity Gain Inverting Mode

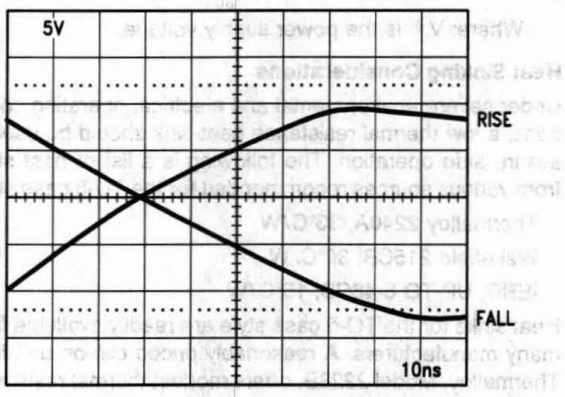

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FIGURE 27. LH0032 Slew Response, Unity Gain Inverting Mode, Standard Compensation (C_C = 10 pF, C_A = 100 pF)

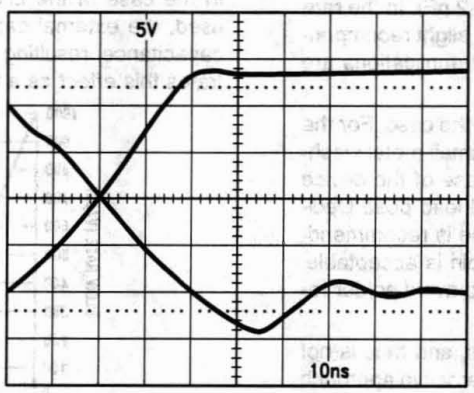

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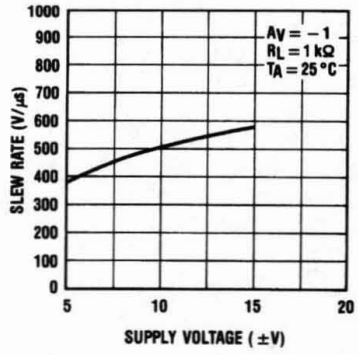
FIGURE 28. LH0032 Slew Response, Unity Gain Inverting Mode, Improved Compensation (C_C = 5 pF, C_A = 1000 pF)

LH0024



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LH0032

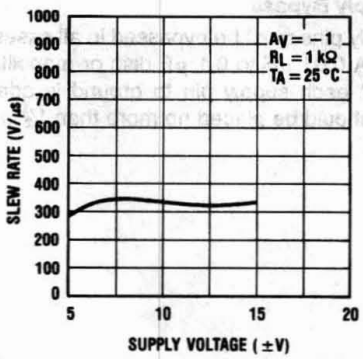

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FIGURE 29. Slew Rate Response as a Function of Supply Voltages

Settling Time

Settling time is the time between the start of a step input to the time it takes the output to settle to within a specified error band of the final voltage. This parameter is heavily influenced by the frequency compensation of the amplifier (degree of damping). Undercompensation results in excessive phase shift, overshoot and ringing, and therefore, a long settling time. Equally poor performance results from overcompensation, which yields an overdamped system, slow decay and, again, a long settling time.

Expectedly, settling time is affected by the loop gain of the amplifier. *Figure 30* illustrates this effect for these two devices.

One of the most demanding applications is driving a capacitive load in a circuit such as a high speed sample-and-hold, where accuracy and fast settling time are both important. Because of the additional phase shift introduced by driving the sampling capacitor, the LH0032 must be recompensated. *Figure 31* presents the optimum compensation to obtain fastest settling time under these conditions.

CONCLUSION

At first glance, the LH0024 and LH0032 seem harmless enough. A more in-depth look reveals the challenges in applying these high performance op amps. The ultimate capabilities that can be extracted are a direct function of careful engineering. With prudence, these devices are harmless indeed.

Application of these high performance amplifiers requires an understanding of compensation and layout technique. With the information presented in this note, the designer should be able to enjoy the benefits of their superior capabilities.

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2. R. K. Underwood, "New Design Techniques for FET Op Amps" National Semiconductor AN-63, March 1972.
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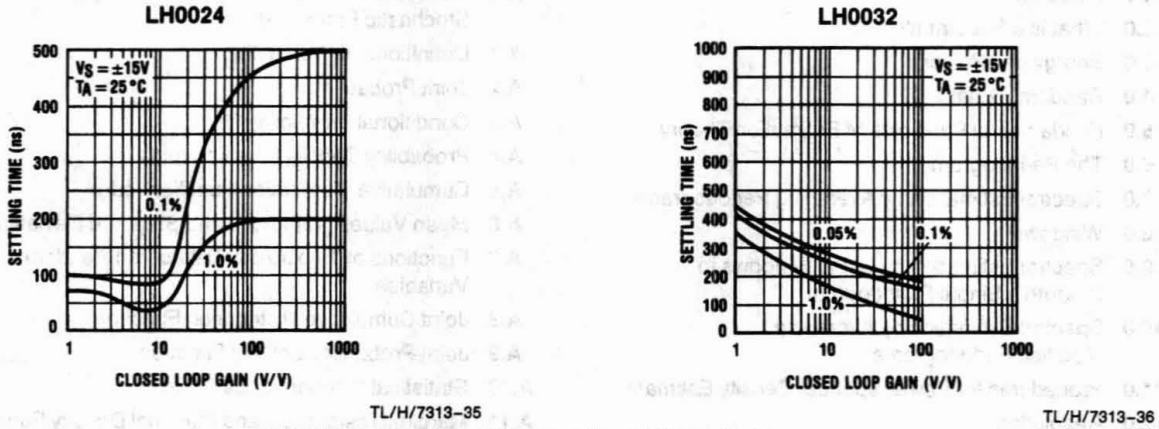

FIGURE 30. Settling Time vs. Closed-Loop Gain

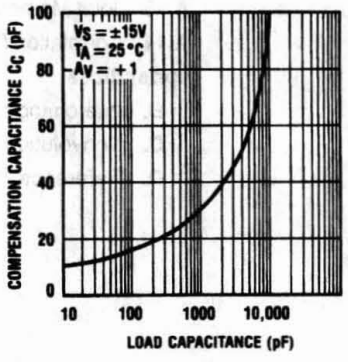

FIGURE 31. Frequency Compensation vs. Load Capacitance

Power Spectra Estimation

National Semiconductor
Application Note 255

1.0 INTRODUCTION

Perhaps one of the more important application areas of digital signal processing (DSP) is the power spectral estimation of periodic and random signals. Speech recognition problems use spectrum analysis as a preliminary measurement to perform speech bandwidth reduction and further acoustic processing. Sonar systems use sophisticated spectrum analysis to locate submarines and surface vessels. Spectral measurements in radar are used to obtain target location and velocity information. The vast variety of measurements spectrum analysis encompasses is perhaps limitless and it will thus be the intent of this article to provide a brief and fundamental introduction to the concepts of power spectral estimation.

Since the estimation of power spectra is statistically based and covers a variety of digital signal processing concepts, this article attempts to provide sufficient background through its contents and appendices to allow the discussion to flow void of discontinuities. For those familiar with the preliminary background and seeking a quick introduction into spectral estimation, skipping to Sections 6.0 through 11.0 should suffice to fill their need. Finally, engineers seeking a more rigorous development and newer techniques of measuring power spectra should consult the excellent references listed in Appendix D and current technical society publications.

As a brief summary and quick lookup, refer to the Table of Contents of this article.

TABLE OF CONTENTS

Section	Description
1.0	Introduction
2.0	What is a Spectrum?
3.0	Energy and Power
4.0	Random Signals
5.0	Fundamental Principles of Estimation Theory
6.0	The Periodogram
7.0	Spectral Estimation by Averaging Periodograms
8.0	Windows
9.0	Spectral Estimation by Using Windows to Smooth a Single Periodogram
10.0	Spectral Estimation by Averaging Modified Periodograms
11.0	Procedures for Power Spectral Density Estimates
12.0	Resolution
13.0	Chi-Square Distributions
14.0	Conclusion
15.0	Acknowledgements

Appendix A	Description
A.0	Concepts of Probability, Random Variables and Stochastic Processes
A.1	Definitions of Probability
A.2	Joint Probability
A.3	Conditional Probability
A.4	Probability Density Function (pdf)
A.5	Cumulative Distribution Function (cdf)
A.6	Mean Values, Variances and Standard Deviation
A.7	Functions of Two Jointly Distributed Random Variables
A.8	Joint Cumulative Distribution Function
A.9	Joint Probability Density Function
A.10	Statistical Independence
A.11	Marginal Distribution and Marginal Density Functions
A.12	Terminology: Deterministic, Stationary, Ergodic
A.13	Joint Moments
A.14	Correlation Functions

Appendices

- **B.** Interchanging Time Integration and Expectations
- **C.** Convolution
- **D.** References

2.0 WHAT IS A SPECTRUM?

A spectrum is a relationship typically represented by a plot of the magnitude or relative value of some parameter against frequency. Every physical phenomenon, whether it be an electromagnetic, thermal, mechanical, hydraulic or any other system, has a unique spectrum associated with it.

In electronics, the phenomena are dealt with in terms of signals, represented as fixed or varying electrical quantities of voltage, current and power. These quantities are typically described in the time domain and for every function of time, f(t), an equivalent frequency domain function $F(\omega)$ can be found that specifically describes the frequency-component content (frequency spectrum) required to generate f(t). A study of relationships between the time domain and its corresponding frequency domain representation is the subject of Fourier analysis and Fourier transforms.

The *forward Fourier transform*, time to frequency domain, of the function x(t) is defined

$$F[x(t)] = \int_{-\infty}^{\infty} x(t)\epsilon^{-j\omega t}\,dt = X(\omega) \qquad (1)$$

and the *inverse Fourier transform*, frequency to time domain, of $X(\omega)$ is

$$F^{-1}[X(\omega)] = \frac{1}{2\pi}\int_{-\infty}^{\infty} X(\omega)\epsilon^{j\omega t}\,d\omega = x(t) \qquad (2)$$

(For an in-depth study of the Fourier integral see reference 19.) Though these expressions are in themselves self-explanatory, a short illustrative example will be presented to aid in relating the two domains.

If an arbitrary time function representation of a periodic electrical signal, f(t), were plotted versus time as shown in *Figure 1*, its Fourier transform would indicate a spectral content consisting of a DC component, a fundamental frequency component ω_0, a fifth harmonic component $5\omega_0$ and a ninth harmonic component $9\omega_0$ (see *Figure 2*). It is illustratively seen in *Figure 3* that the superposition of these frequency components, in fact, yields the original time function f(t).

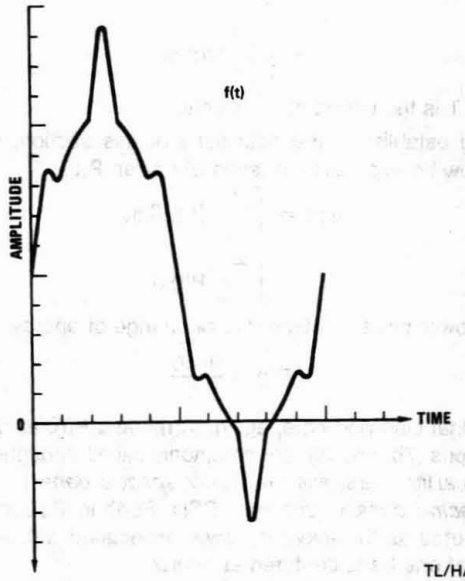

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FIGURE 1. An Electrical Signal f(t)

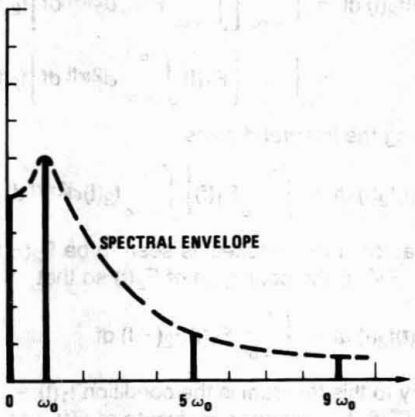

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FIGURE 2. Spectral Composition or Spectrum $F(\omega)$ or f(t)

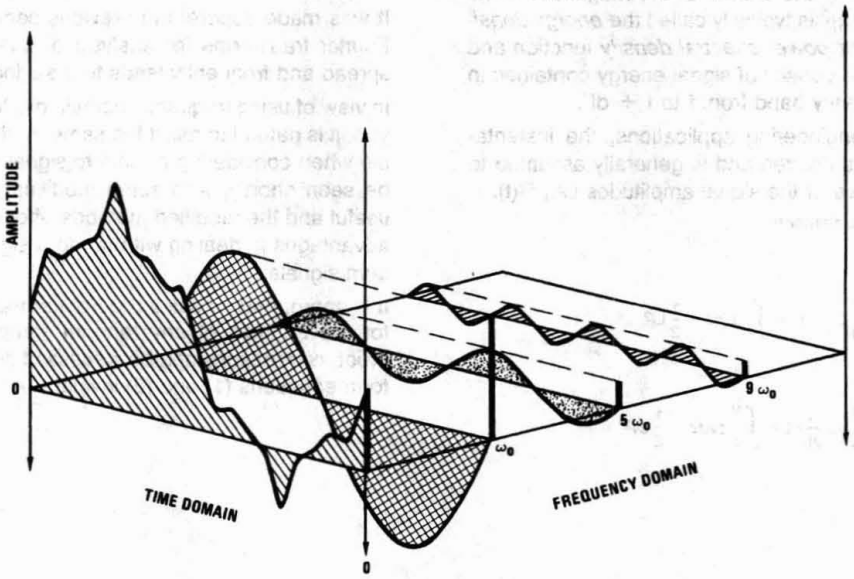

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FIGURE 3. Combined Time Domain and Frequency Domain Plots

3.0 ENERGY AND POWER

In the previous section, time and frequency domain signal functions were related through the use of Fourier transforms. Again, the same relationship will be made in this section but the emphasis will pertain to signal power and energy.

Parseval's theorem relates the representation of energy, $\omega(t)$, in the time domain to the frequency domain by the statement

$$\omega(t) = \int_{-\infty}^{\infty} f_1(t)f_2(t)\,dt = \int_{-\infty}^{\infty} F_1(f)F_2(f)\,df \qquad (3)$$

where f(t) is an arbitrary signal varying as a function of time and F(t) its equivalent Fourier transform representation in the frequency domain.

The proof of this is simply

$$\int_{-\infty}^{\infty} f_1(t)f_2(t)\,dt = \int_{-\infty}^{\infty} f_1(t)f_2(t)\,dt \qquad (4a)$$

Letting $F_1(f)$ be the Fourier transform of $f_1(t)$

$$\int_{-\infty}^{\infty} f_1(t)f_2(t)\,dt = \int_{-\infty}^{\infty}\left[\int_{-\infty}^{\infty} F_1(f)\epsilon^{j2\pi ft}\,df\right]f_2(t)\,dt \qquad (4b)$$

$$= \int_{-\infty}^{\infty}\left[F_1(f)\int_{-\infty}^{\infty}\epsilon^{j2\pi ft}\,df\right]f_2(t)\,dt \qquad (4c)$$

Rearranging the integrand gives

$$\int_{-\infty}^{\infty} f_1(t)f_2(t)\,dt = \int_{-\infty}^{\infty} F_1(f)\left[\int_{-\infty}^{\infty} f_2(t)\epsilon^{j2\pi ft}\,dt\right]df \qquad (4d)$$

and the factor in the brackets is seen to be $F_2(-f)$ (where $F_2(-f) = F_2^*(f)$ the conjugate of $F_2(f)$ so that

$$\int_{-\infty}^{\infty} f_1(t)f_2(t)\,dt = \int_{-\infty}^{\infty} F_1(f)F_2(-f)\,df \qquad (4e)$$

A corollary to this theorem is the condition $f_1(t) = f_2(t)$ then $F(-f) = F^*(f)$, the complex conjugate of F(f), and

$$\omega(t) = \int_{-\infty}^{\infty} f^2(t)\,dt = \int_{-\infty}^{\infty} F(f)F^*(f)\,df \qquad (5a)$$

$$= \int_{-\infty}^{\infty} |F(f)|^2\,df \qquad (5b)$$

This simply says that the total energy† in a signal f(t) is equal to the area under the square of the magnitude of its Fourier transform. $|F(f)|^2$ is typically called the *energy density, spectral density,* or *power spectral density* function and $|F(f)|^2df$ describes the density of signal energy contained in the differential frequency band from f to f + dF.

In many electrical engineering applications, the instantaneous signal power is desired and is generally assumed to be equal to the square of the signal amplitudes i.e., $f^2(t)$.

†Recall the energy storage elements

Inductor $v = L\frac{di}{dt}$

$$\omega(t) = \int_0^T vidt = \int_0^T L\frac{di}{dt}idt = \int_0^I Lidt = \frac{1}{2}LI^2$$

Capacitor $i = c\frac{dv}{dt}$

$$\omega(t) = \int_0^T vidt = \int_0^T vc\frac{dv}{dt}dt = \int_0^V cvdv = \frac{1}{2}cv^2$$

This is only true, however, assuming that the signal in the system is impressed across a 1Ω resistor. It is realized, for example, that if f(t) is a voltage (current) signal applied across a system resistance R, its true instantaneous power would be expressed as $[f(t)]^2/R$ (or for current $[f(t)]^2R$) thus, $[f(t)]^2$ is the true power only if $R = 1\Omega$.

So for the general case, power is always proportional to the square of the signal amplitude varied by a proportionality constant R, the impedance level in a circuit. In practice, however, it is undesirable to carry extra constants in the computation and customarily for signal analysis, one assumes signal measurement across a 1Ω resistor. This allows units of power to be expressed as the square of the signal amplitudes and the units of energy measured as volts^2-second (amperes^2-second).

For periodic signals, equation (5) can be used to define the average power, P_{avg}, over a time interval t_2 to t_1 by integrating $[f(t)]^2$ from t_1 to t_2 and then obtaining the average after dividing the result by $t_2 - t_1$ or

$$P_{avg} = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} f^2(t)\,dt \qquad (6a)$$

$$= \frac{1}{T}\int_0^T f^2(t)\,dt \qquad (6b)$$

where T is the period of the signal.

Having established the definitions of this section, energy can now be expressed in terms of power, P(t),

$$\omega(t) = \int_{-\infty}^{\infty} [f(t)]^2\,dt \qquad (7a)$$

$$= \int_{-\infty}^{\infty} P(t)\,dt \qquad (7b)$$

with power being the time rate of change of energy

$$P(t) = \frac{d\omega(t)}{dt} \qquad (8)$$

As a final clarifying note, again, $|F(f)|^2$ and P(t), as used in equations (7b) and (8), are commonly called throughout the technical literature, *energy density, spectral density,* or *power spectral density* functions, PSD. Further, PSD may be interpreted as the average power associated with a bandwidth of one hertz centered at f hertz.

4.0 RANDOM SIGNALS

It was made apparent in previous sections that the use of Fourier transforms for analysis of linear systems is widespread and frequently leads to a saving in labor.

In view of using frequency domain methods for system analysis, it is natural to ask if the same methods are still applicable when considering a random signal system input. As will be seen shortly, with some modification, they *will* still be useful and the modified methods offer essentially the same advantages in dealing with random signals as with nonrandom signals.

It is appropriate to ask if the Fourier transform may be used for the analysis of any random sample function. Without proof, two reasons can be discussed which make the transform equations (1) and (2) invalid.

Firstly, $X(\omega)$ is a random variable since, for any fixed ω, each sample would be represented by a different value of the ensemble of possible sample functions. Hence, it is not a frequency representation of the process but only of one member of the process. It might still be possible, however, to use this function by finding its mean or expected value over the ensemble except that the second reason netages this approach. The second reason for not using the $X(\omega)$ of equations (1) and (2) is that, for stationary processes, it almost never exists. As a matter of fact, one of the conditions for a time function to be Fourier transformable is that it be integrable so that,

$$\int_{-\infty}^{\infty} |x(t)|\, dt < \infty \tag{9}$$

A sample from a stationary random process can never satisfy this condition (with the exception of generalized functions inclusive of impulses and so forth) by the argument that if a signal has nonzero power, then it has infinite energy and if it has finite energy then it has zero power (average power). Shortly, it will be seen that the class of functions having no Fourier integral, due to equation (9), but whose average power is finite can be described by statistical means.

Assuming x(t) to be a sample function from a stochastic process, a truncated version of the function $x_T(t)$ is defined as

$$x_T(t) = \begin{cases} x(t) & |t| \le T \\ 0 & |t| > T \end{cases} \tag{10}$$

and

$$x(t) = \lim_{T \to \infty} x_T(t) \tag{11}$$

This truncated function is defined so that the Fourier transform of $x_T(t)$ can be taken. If x(t) is a power signal, then recall that the transform of such a signal is not defined

$$\int_{-\infty}^{\infty} |x(t)|\, dt \text{ not less than } \infty \tag{12}$$

but that

$$\int_{-\infty}^{\infty} |x_T(t)|\, dt < \infty \tag{13}$$

The Fourier transform pair of the truncated function $x_T(t)$ can thus be taken using equations (1) and (2). Since x(t) is a power signal, there must be a power spectral density function associated with it and the total area under this density must be the average power despite the fact that x(t) is non-Fourier transformable.

Restating equation (5) using the truncated function $x_T(t)$

$$\int_{-\infty}^{\infty} x_T^2(t)\, dt = \int_{-\infty}^{\infty} |X_T(f)|^2\, df \tag{14}$$

and dividing both sides by 2T

$$\frac{1}{2T}\int_{-\infty}^{\infty} x_T^2(t)\, dt = \frac{1}{2T}\int_{-\infty}^{\infty} |X_T(f)|^2\, df \tag{15}$$

gives the left side of equation (15) the physical significance of being proportional to the average power of the sample function in the time interval $-T$ to T. This assumes $x_T(t)$ is a voltage (current) associated with a resistance. More precisely, it is the square of the *effective value* of $x_T(t)$ and for an ergodic process approaches the *mean-square* value of the process as T approaches infinity.

At this particular point, however, the limit as T approaches infinity cannot be taken since $X_T(f)$ is non-existent in the limit. Recall, though, that $X_T(f)$ is a random variable with respect to the ensemble of sample functions from which x(t) was taken. The limit of the *expected value* of

$$\frac{1}{2T}|X_T(f)|^2$$

can be reasonably assumed to exist since its integral, equation (15), is always positive and certainly does exist. If the expectations $E\{\ \}$, of both sides of equation (15) are taken

$$E\left\{\frac{1}{2T}\int_{-\infty}^{\infty} x_T^2(t)\, dt\right\} = E\left\{\frac{1}{2T}\int_{-\infty}^{\infty} |x_T(f)|^2\, df\right\} \tag{16}$$

then interchanging the integration and expectation and at the same time taking the limit as $T \to \infty$

$$\lim_{T \to \infty} \frac{1}{2T}\int_{-\infty}^{\infty} \overline{x^2}(t)\, dt = \lim_{T \to \infty} \frac{1}{2T}\int_{-\infty}^{\infty} E\{|x_T(f)|^2\}\, df \tag{17}$$

results in

$$< \overline{x^2}(t) > = \int_{-\infty}^{\infty} \lim_{T \to \infty} \frac{E\{|x_T(f)|^2\}}{2T}\, df \tag{18}$$

where $\overline{x^2}(t)$ is defined as the mean-square value ($\bar{}$ denotes ensemble averaging and $< >$ denotes time averaging).

For stationary processes, the time average of the mean-square value is equal to the mean-square value so that equation (18) can be restated as

$$\overline{x^2}(t) = \int_{-\infty}^{\infty} \lim_{T \to \infty} \frac{E\{|X_T(f)|^2\}}{2T}\, df \tag{19}$$

The integrand of the right side of equation (19), similar to equation (5b), is called the *energy density* spectrum or *power spectral density* function of a random process and will be designated by S(f) where

$$S(f) = \lim_{T \to \infty} \frac{E\{X_T(f)|^2\}}{2T} \tag{20}$$

Recall that letting $T \to \infty$ is not possible before taking the expectation.

Similar to the argument in Section III, the physical interpretation of power spectral density can be thought of in terms of average power. If x(t) is a voltage (current) associated with a 1Ω resistance, $\overline{x^2}(t)$ is just the average power dissipated in that resistor and S(f) can be interpreted as the average power associated with a bandwidth of one hertz centered at f hertz.

S(f) has the units volts^2-second and its integral, equation (19), leads to the mean square value hence,

$$\overline{x^2}(t) = \int_{-\infty}^{\infty} S(f)\, df \tag{21}$$

Having made the tie between the power spectral density function S(f) and statistics, an important theorem in power spectral estimation can now be developed.

Using equation (20) and recalling that $X_T(f)$ is the Fourier transform of $x_T(t)$, assuming a nonstationary process,

$$S(f) = \lim_{T \to \infty} \frac{E\{|X_T(f)|^2\}}{2T} \tag{22}$$

$$S(f) = \lim_{T \to \infty} \frac{1}{2T} E\left\{\int_{-\infty}^{\infty} x_T(t_1)\epsilon^{j\omega t_1}\, dt_1 \int_{-\infty}^{\infty} x_T(t_2)\epsilon^{j\omega t_2}\, dt_2\right\} \tag{23}$$

Note that $|X_T(f)|^2 = X_T(f)X_T(-f)$ and that in order to distinguish the variables of integration when equation (23) is remanipulated the subscripts of t_1 and t_2 have been introduced. So, (see Appendix B)

$$S(f) = \lim_{T \to \infty}\left\{\frac{1}{2T} E\left[\int_{-\infty}^{\infty} dt_2 \int_{-\infty}^{\infty} \epsilon^{-j\omega(t_2-t_1)} x_T(t_1)x_T(t_2)\, dt_1\right]\right\} \tag{24}$$

$$= \lim_{T \to \infty}\left\{\frac{1}{2T}\int_{-\infty}^{\infty} dt_2 \int_{-\infty}^{\infty} E[x_T(t_1)x_T(t_2)]\, \epsilon^{-j\omega(t_2-t_1)}\, dt_1\right\} \tag{25}$$

Finally, the expectation $E[x_T(t_1)x_T(t_2)]$ is recognized as the autocorrelation, $R_{xx}(t_1, t_2)$ (Appendix A.14) function of the truncated process where

$$E[x_T(t_1)x_T(t_2)] = R_{xx}(t_1, t_2) \qquad |t_1|, |t_2| \le T$$
$$= 0 \qquad \text{everywhere else.}$$

Substituting

$$t_2 - t_1 = \tau \tag{26}$$

$$dt_2 = d\tau \tag{27}$$

equation (25) next becomes

$$S(f) = \lim_{T \to \infty} \frac{1}{2T}\int_{-\infty}^{\infty} d\tau \int_{-T}^{T} R_{xx}(t_1, t_1+\tau)\epsilon^{-j\omega\tau}\, dt \tag{28}$$

or

$$S(f) = \left\{\left[\int_{-\infty}^{\infty} \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} R_{xx}(t_1, t_1+\tau)\, dt_1\right]\epsilon^{-j\omega t}\right\} d\tau \tag{29}$$

We see then that the special density is the Fourier transform of the time average of the autocorrelation function. The relationship of equation (29) is valid for a nonstationary process.

For the stationary process, the autocorrelation function is independent of time and therefore

$$\langle R_{xx}(t_1, t_1, +\tau)\rangle = R_{xx}(\tau) \tag{30}$$

From this it follows that the spectral density of a stationary random process is just the Fourier transform of the autocorrelation function where

$$S(f) = \int_{-\infty}^{\infty} R_{xx}(\tau)\epsilon^{-j\omega t}\, d\tau \tag{31}$$

and

$$R_{xx}(\tau) = \int_{-\infty}^{\infty} S(f)\epsilon^{j\omega t}\, df \tag{32}$$

are described as the Wiener-Khintchine theorem.

The Wiener-Khintchine relation is of fundamental importance in analyzing random signals since it provides a link between the time domain [correlation function, $R_{xx}(\tau)$] and the frequency domain [spectral density, S(f)]. Note that the uniqueness is in fact the Fourier transformability. It follows, then, for a stationary random process that the autocorrelation function is the inverse transform of the spectral density function. For the nonstationary process, however, the autocorrelation function cannot be recovered from the spectral density. Only the time average of the correlation is recoverable, equation (29).

Having completed this section, the path has now been paved for a discussion on the techniques used in power spectral estimation.

5.0 FUNDAMENTAL PRINCIPLES OF ESTIMATION THEORY

When characterizing or modeling a random variable, estimates of its statistical parameters must be made since the data taken is a finite sample sequence of the random process.

Assume a random sequence x(n) from the set of random variables $\{x_n\}$ to be a realization of an ergodic random process (random for which ensemble or probability averages, E[ ], are equivalent to time averages, < >) where for all n,

$$m = E[x_n] = \int_{-\infty}^{\infty} x f_x(x)\, dx \tag{33}$$

Assuming further that the estimate of the desired averages of the random variables $\{x_n\}$ from a finite segment of the sequence, x(n) for $0 \le n \le N-1$, to be

$$m = \langle x_n\rangle = \lim_{N \to \infty} \frac{1}{2N+1} \sum_{n=-N}^{N} x_n \tag{34}$$

then for each sample sequence

$$m = \langle x(n)\rangle = \lim_{N \to \infty} \frac{1}{2N+1} \sum_{n=-N}^{N} x(n) \tag{35}$$

Since equation (35) is a precise representation of the mean value in the limit as N approaches infinity then

$$\hat{m} = \frac{1}{N} \sum_{n=0}^{N-1} x(n) \tag{36}$$

may be regarded as a fairly accurate estimate of m for sufficiently large N. The caret ($\wedge$) placed above a parameter is representative of an estimate. The area of statistics that pertains to the above situations is called *estimation theory*.

Having discussed an elementary statistical estimate, a few common properties used to characterize the estimator will next be defined. These properties are *bias, variance* and *consistency*.

Bias

The difference between the mean or expected value $E[\hat{\eta}]$ of an estimate $\hat{\eta}$ and its true value η is called the *bias*.

$$\text{bias} = B_{\hat{\eta}} = \eta - E[\hat{\eta}] \tag{37}$$

Thus, if the mean of an estimate is equal to the true value, it is considered to be *unbiased* and having a *bias* value equal to zero.

Variance

The variance of an estimator effectively measures the width of the probability density (Appendix A.4) and is defined as

$$\sigma^2_{\hat{\eta}} E = \left[(\hat{\eta} - E[\hat{\eta}])^2 \right] \tag{38}$$

A good estimator should have a small variance in addition to having a small bias suggesting that the probability density function is concentrated about its mean value. The mean square error associated with this estimator is defined as

$$\text{mean square error} = E\left[(\hat{\eta} - \eta)^2 \right] = \sigma^2_{\hat{\eta}} + B^2_{\hat{\eta}} \tag{39}$$

Consistency

If the bias and variance both tend to zero as the limit tends to infinity or the number of observations become large, the estimator is said to be consistent. Thus,

$$\lim_{N \to \infty} \sigma^2_{\hat{\eta}} = 0 \tag{40}$$

and

$$\lim_{N \to \infty} B_{\hat{\eta}} = 0 \tag{41}$$

This implies that the estimator converges in probability to the true value of the quantity being estimated as N becomes infinite.

In using estimates the mean value estimate of m_x, for a Gaussian random process is the *sample mean* defined as

$$\hat{m}_x = \frac{1}{N} \sum_{i=0}^{N-1} x_i \tag{42}$$

the mean square value is computed as

$$E[\hat{m}_x^2] = \frac{1}{N^2} \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} E[x_i x_j] \tag{43}$$

$$= \frac{1}{N^2} \left[\sum_{i=0}^{N-1} E[x_i^2] + \sum_{i=0}^{N-1} \sum_{\substack{j=0 \\ i \neq j}}^{N-1} E[x_i] \bullet E[x_j] \right] \tag{44}$$

$$= \frac{1}{N_2} \left[N(E[x_n^2]) + \left(\sum_{i=0}^{N-1} E[x_i] \right) \left(\sum_{\substack{j=0 \\ i \neq j}}^{N-1} E[x_j] \right) \right] \tag{45}$$

$$= \frac{1}{N} E[x_n^2] + (m_x)^2 \frac{N-1}{N} \tag{46}$$

thus allowing the variance to be stated as

$$\sigma^2_{\hat{m}_x} = E[(\hat{m}_x)^2] - \{E[\hat{m}_x]\}^2 \tag{47}$$

$$= \frac{1}{N} E[x_n^2] + (m_x^2) \frac{N-1}{N} - \{E[\hat{m}_x]\}^2 \tag{48}$$

$$= \frac{1}{N} E[x_n^2] + (m_x^2) \frac{N-1}{N} - m_x^2 \tag{49}$$

$$= \frac{1}{N} (E[x_n^2] - m_x^2) \tag{50}$$

$$= \frac{\sigma_x^2}{N} \tag{51}$$

This says that as the number of observations N increase, the variance of the sample mean decreases, and since the bias is zero, the sample mean is a consistent estimator.

If the variance is to be estimated and the mean value is a known then

$$\hat{\sigma}_x^2 = \frac{1}{N} \sum_{i=0}^{N-1} (x_i - m_x)^2 \tag{52}$$

this estimator is consistent.

If, further, the mean and the variance are to be estimated then the sample variance is defined as

$$\hat{\sigma}_x^2 = \frac{1}{N} \sum_{i=0}^{N-1} (x_i - \hat{m}_x)^2 \tag{53}$$

again $\hat{m}_x$ is the sample mean.

The only difference between the two cases is that equation (52) uses the true value of the mean, whereas equation (53) uses the estimate of the mean. Since equation (53) uses an estimator the bias can be examined by computing the expected value of $\hat{\sigma}_x^2$ therefore,

$$E[\hat{\sigma}_x^2] = \frac{1}{N} \sum_{i=0}^{N-1} (E[x_i] - E[\hat{m}_x])^2 \tag{54}$$

$$= \frac{1}{N} \sum_{i=0}^{N-1} \left\{ E[x_i^2] - 2E[x_i \hat{m}_x] + E[\hat{m}_x^2] \right\} \tag{55}$$

$$= \frac{1}{N} \sum_{i=0}^{N-1} E[x_i^2] - \frac{2}{N^2} \sum_{i=0}^{N-1} \left(\sum_{j=0}^{N-1} E[x_i x_j] \right) + \frac{1}{N^2} \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} E[x_i x_j] \tag{56}$$

$$= \frac{1}{N}\sum_{i=0}^{N-1} E[x_i^2] - \frac{2}{N^2}\left(\sum_{i=0}^{N-1} E[x_i^2] + \sum_{i=0}^{N-1}\sum_{\substack{j=0 \\ i\neq j}}^{N-1} E[X_i]\bullet E[x_j]\right) + \frac{1}{N^2}\left(\sum_{i=0}^{N-1} E[x_i^2] + \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} E[x_i]\bullet E[x_j]\right) \quad (57)$$

$$= \frac{1}{N}\left(N\bullet E[x_i^2]\right) - \frac{2}{N^2}\left[N\bullet E[x_i^2] + N(N-1)m_x^2\right] + \frac{1}{N^2}\left[N\bullet E[x_i^2] + N(N-1)m_x^2\right] \quad (58)$$

$$= \frac{1}{N}\left(N\bullet E[x_i^2]\right) - \frac{2N}{N^2}\left(E[x_i^2]\right) - \frac{2N(N-1)}{N^2}m_x^2 + \frac{N}{N^2}E[x_i^2] + \frac{N(N-1)}{N^2}m_x^2 \quad (59)$$

$$= \frac{1}{N}\left(N\bullet E[x_i^2]\right) - \frac{2}{N}(E[x_i^2]) - \frac{2(N-1)}{N}m_x^2 + \frac{1}{N}E[x_i^2] + \frac{(N-1)}{N}m_x^2 \quad (60)$$

$$= \frac{1}{N}(N - E[x_i^2]) - \frac{1}{N}(E[x_i^2]) - \frac{(N-1)}{N}m_x^2 \quad (61)$$

$$= \frac{(N-1)}{N}(E[x_i^2]) - \frac{(N-1)}{N}m_x^2 \quad (62)$$

$$= \frac{(N-1)}{N}\sigma_x^2 \quad (63)$$

It is apparent from equation (63) that the mean value of the sample variance does not equal the variance and is thus biased. Note, however, for large N the mean of the sample variance asymptotically approaches the variance and the estimate virtually becomes unbiased. Next, to check for consistency, we will proceed to determine the variance of the estimate sample variance. For ease of understanding, assume that the process is zero mean, then letting

$$\psi = \hat{\sigma}_x^2 = \frac{1}{N}\sum_{i=0}^{N-1} x_i^2 \quad (64)$$

so that,

$$E[\psi^2] = \frac{1}{N^2}\sum_{i=1}^{N}\sum_{k=1}^{N} E[x_i^2 x_k^2] \quad (65)$$

$$= \frac{1}{N^2}\left[NE[x_n^4] + N(N-1)\,(E[x_n^2])^2\right] \quad (66)$$

$$= \frac{1}{N}\left[E[x_n^4] + (N-1)(E[x_n^2])^2\right] \quad (67)$$

the expected value

$$E[\psi] = E[x_n^2] \quad (68)$$

so finally

$$\text{var}[\hat{\sigma}_x^2] = E[\psi^2] - (E[\psi])^2 \quad (69)$$

$$= \frac{1}{N}\left[E[x_n^4] - (E[x_n^2])^2\right] \quad (70)$$

Re-examining equations (63) and (70) as N becomes large clearly indicates that the sample variance is a consistent estimate. Qualitatively speaking, the accuracy of this estimate depends upon the number of samples considered in the estimate. Note also that the procedures employed above typify the style of analysis used to characterize estimators.

6.0 THE PERIODOGRAM

The first method defines the sampled version of the Wiener-Khintchine relation, equations (31) and (32), where the power spectral density estimate $S_{N_{xx}}(f)$ is the discrete Fourier transform of the autocorrelation estimate $R_{N_{xx}}(k)$ or

$$S_{N_{xx}}(f) = \sum_{k=-\infty}^{\infty} R_{N_{xx}}(k)\,\epsilon^{-j\omega kT} \quad (71)$$

This assumes that x(n) is a discrete time random process with an autocorrelation function $R_{N_{xx}}(k)$.

For a finite sequence of data

$$x(n) = \begin{cases} x_n & \text{for } n = 0, 1, \ldots, N-1 \\ 0 & \text{elsewhere} \end{cases} \quad (72)$$

called a rectangular data window, the sample autocorrelation function (sampled form of equation A.14-9)

$$R_{N_{xx}}(k) = \frac{1}{N}\sum_{n=-\infty}^{\infty} x(n)x(n+k) \quad (73)$$

can be substituted into equation (71) to give the spectral density estimate

$$S_{N_{xx}}(f) = \frac{1}{N}|X_N(f)|^2 \quad (74)$$

called the periodogram.

$$\left(\text{Note: } \frac{|X_N(f)|^2}{N} = \frac{X_N(f)X_{N^*(f)}}{N} = \frac{X_N^2(f)_{real} + X_N^2(f)_{imag}}{N} = F\left[R_{N_{xx}}(k)\right] = F\left[E[x(n)x(n+k)]\right]\right).$$

Hence,

$$S_{N_{xx}}(f) = \sum_{k=-\infty}^{\infty} R_{N_{xx}}(k)\,\epsilon^{-j\omega kT} \quad (75)$$

$$= \sum_{k=-\infty}^{\infty}\left[\frac{1}{N}\sum_{n=-\infty}^{\infty} x(n)x(n+k)\right]\epsilon^{-j\omega kT} \quad (76)$$

so letting $1 = \epsilon^{j\omega nT}\,\epsilon^{-j\omega nT}$

$$S_{N_{XX}}(f) = \frac{1}{N}\left(\sum_{n=-\infty}^{\infty} x(n)\epsilon^{j\omega nT} \sum_{k=-\infty}^{\infty} x(n+k)\,\epsilon^{-j\omega(n+k)T}\right) \quad (77)$$

and allowing the variable $m = n + k$

$$S_{N_{xx}}(f) = \frac{1}{N}X_N(f)X_N^*(f) = \frac{1}{N}|X_N(f)|^2 \quad (78)$$

in which the Fourier transform of the signal is

$$X_N(f) = \sum_{n=-\infty}^{\infty} x(n)\,\epsilon^{-j\omega nT} \quad (79)$$

The current discussion leads one to believe that the periodogram is an excellent estimator of the true power spectral density S(f) as N becomes large. This conclusion is false and shortly it will be verified that the periodogram is, in fact, a poor estimate of S(f). To do this, both the expected value and variance of $S_{N_{xx}}(f)$ will be checked for consistency as N becomes large. As a side comment it is generally faster to determine the power spectral density, $S_{N_{xx}}(f)$, of the random process using equation (74) and then inverse Fourier transforming to find $R_{N_{xx}}(k)$ than to obtain $R_{N_{xx}}(k)$ directly. Further, since the periodogram is seen to be the magnitude squared of the Fourier transformed data divided by N, the power spectral density of the random process is unrelated to the angle of the complex Fourier transform $X_N(f)$ of a typical realization.

Prior to checking for the consistency of $S_{N_{xx}}(f)$, the sample autocorrelation must initially be found consistent. Proceeding, since the sample autocorrelation estimate

$$R_{N_{xx}}(k) = \frac{x(0)x(k)+x(1)x(|k|+1)+\ldots+x(N-1-|k|)x(N-1)}{N} \quad (80)$$

$$= \frac{1}{N}\sum_{n=0}^{N-1-|k|} x(n)x(n+|k|) \quad (81)$$

$$k = 0, \pm 1, \pm 2, \ldots, \pm N-1$$

which averages together all possible products of samples separated by a lag of k, then, the mean value of the estimate is related to the true autocorrelation function by

$$E[R_{N_{xx}}(k)] = \left(\frac{1}{N}\sum_{n=0}^{N-1-|k|} E[x(n)x(n+|k|)]\right) \quad (82)$$

$$= \frac{N-|k|}{N}R(k)$$

where the true autocorrelation function R(k) is defined as (the sample equivalent of equation A.14-8)

$$R(k) = E[x(n)x(n+k)] \quad (83)$$

From equation (82) it is observed that $R_{N_{xx}}(k)$ is a biased estimator. It is also considered to be asymptotically unbiased since the term

$$\frac{N-|k|}{N}$$

approaches 1 as N becomes large. From these observations $R_{N_{xx}}(k)$ can be classified as a good estimator of R(k). In addition to having a small bias, a good estimator should also have a small variance. The variance of the sample autocorrelation function can thus be computed as

$$\text{var}[R_{N_{xx}}(k)] = E[R^2_{N_{xx}}(k)] - E^2[R_{N_{xx}}(k)] \quad (84)$$

Examining the $E[R_{N_{xx}}(k)]$ term of equation (84), substituting the estimate of equation (81) and replacing n with m, it follows that

$$E[R^2_{N_{xx}}(k)] = E\left\{\left[\frac{1}{N}\sum_{n=0}^{N-1-|k|} x(n)x(n+|k|)\right]\left[\frac{1}{N}\sum_{m=0}^{N-1-|k|} x(m)x(m+|k|)\right]\right\} \quad (85)$$

$$= \frac{1}{N^2}\left(\sum_{n=0}^{N-1-|k|}\sum_{m=0}^{N-1-|k|} E[x(n)x(n+|k|)x(m)x(m+|k|)]\right) \quad (86)$$

If the statistical assumption that x(n) is a zero-mean Gaussian process, then the zero-mean, jointly Gaussian, random variables symbolized as X_1, X_2, X_3 and X_4 of equation (86) can be described as [Ref. (30)].

$$E[X_1X_2X_3X_4] = E[X_1X_2]\,E[X_3X_4] + E[X_1X_3]\,E[X_2X_4] + E[X_1X_4]\,E[X_2X_3] \quad (87)$$

$$= \Big[E[x(n)\,x(n+|k|)]\,E[x(m)\,x(m+|k|)] + E[x(n)x(m)]E[x(n+|k|)x(m+|k|)] + E[x(n)\,x(m+|k|)]\,E[x(n+|k|)\,x(m)]\Big] \quad (88)$$

Using equation (88), equation (84) becomes

$$\text{Var}[R_{N_{xx}}(k)] = \left\{\frac{1}{N^2}\sum_{n=0}^{N-1-|k|}\sum_{m=0}^{N-1-|k|} R_{N_{xx}}(k)R_{N_{xx}}(k) + R_{N_{xx}}(n-m)\,R_{N_{xx}}(n-m) + R_{N_{xx}}(n-m-|k|)\,R_{N_{xx}}(n-m+|k|)\right\} - \left[\frac{1}{N}\sum_{n=0} R_{N_{xx}}(k)\right]^2 \quad (89)$$

$$\text{Var}[R_{N_{xx}}(k)] = \frac{1}{N^2}\sum_{n=0}^{N-1-|k|}\sum_{m=0}^{N-1-|k|}\left\{R^2_{N_{xx}}(n-m) + R_{N_{xx}}(n-m-k)R_{N_{xx}}(n-m+|k|)\right\} \quad (90)$$

where the lag term n − m was obtained from the lag difference between $\tau = n - m = (n + k) - (m + k)$ in the second term of equation (88). The lag term n − k + m and n − k − m was obtained by referencing the third term in equation (88) to n, therefore for

$$E[x(n)\, x(m + |k|)] \tag{91}$$

the lag term $\tau = n - (m + |k|)$ so

$$E[x(n)\, x(m + |k|)] = R_{N_{xx}}(n - m + |k|) \tag{92}$$

and for

$$E[x(n + |k|)\, x(m)] \tag{93}$$

first let n − m then add |k| so $\tau = n - m + |k|$ and

$$E[x(n + |k|)\, x(m)] = R_{N_{xx}}(n - m + |k|) \tag{94}$$

Recall that a sufficient condition for an estimator to be consistent is that its bias and variance both converge to zero as N becomes infinite. This essentially says that an estimator is consistent if it converges in probability to the true value of the quantity being estimated as N approaches infinity.

Re-examining equation (90), the variance of $R_{N_{xx}}(k)$, and equation (82), the expected value of $R_{N_{xx}}(k)$, it is found that both equations tend toward zero for large N and therefore $R_{N_{xx}}(k)$ is considered as a consistent estimator of R(k) for fixed finite k in practical applications.

Having established that the autocorrelation estimate is consistent, we return to the question of the periodogram consistency.

At first glance, it might seem obvious that $S_{N_{xx}}(f)$ should inherit the asymptotically unbiased and consistent properties of $R_{N_{xx}}(k)$, of which it is a Fourier transform. Unfortunately, however, it will be shown that $S_{N_{xx}}(f)$ does not possess these nice statistical properites.

Going back to the power spectral density of equation (71).

$$S_{N_{xx}}(f) = \sum_{k=-\infty}^{\infty} R_{N_{xx}}(k)\, \epsilon^{-j\omega kT}$$

and determining its expected value

$$E[S_{N_{xx}}(f)] = \sum_{k=-\infty}^{\infty} E[R_{N_{xx}}(k)]\, \epsilon^{-j\omega kT} \tag{95}$$

the substitution of equation (82) into equation (95) yields the mean value estimate

$$E[S_{N_{xx}}(f)] = \sum_{K=-N}^{N} R(k) \left(1 - \frac{|k|}{N}\right) \epsilon^{-j\omega kT} \tag{96}$$

the $\left(1 - \frac{|k|}{N}\right)$

term of equation (96) can be interpreted as a(k), the triangular window resulting from the autocorrelation of finite-sequence rectangular-data window ω(k) of equation (72). Thus,

$$a(k) = \begin{cases} 1 - \dfrac{|k|}{N} & |k| < N - 1 \quad (97a) \\ 0 & \text{elsewhere} \quad (97b) \end{cases}$$

and the expected value of the periodogram can be written as the finite sum

$$E[S_{N_{xx}}(f)] = \sum_{k=-\infty}^{\infty} R_{N_{xx}}(k)\, a(k)\, \epsilon^{-j\omega kT} \tag{98}$$

Note from equation (98) that the periodogram mean is the discrete Fourier transform of a product of the true autocorrelation function and a triangular window function. This frequency function can be expressed entirely in the frequency domain by the convolution integral. From equation (98), then, the convolution expression for the mean power spectral density is thus,

$$E[S_{N_{xx}}(f)] = \int_{-1/2}^{1/2} S(\eta)\, A(f - \eta)\, d\eta \tag{99}$$

where the general frequency expression for the transformed triangular window function A(f) is

$$A(f) = \frac{1}{N} \left[\frac{\sin (2\pi f) \frac{N}{2}}{\sin \frac{(2\pi f)}{2}} \right]^2 \tag{100}$$

Re-examining equation (98) or (96) it can be said that equation (71) or (74) gives an asymptotically unbiased estimate of S(f) with the distorting effects of a(k) vanishing as N tends toward infinity. At this point equation (98) still appears as a good estimate of the power spectral density function. For the variance var $[S_{N_{xx}}(f)]$ however, it can be shown [Ref. (10)] that if the data sequence x(n) comes from a Gaussian process then the variance of $S_{N_{xx}}(f)$ approaches the square of the true spectrum, $S^2(f)$, at each frequency f. Hence, the variance is not small for increasing N,

$$\lim_{N \to \infty} \text{var}[S_{N_{xx}}(f)] = S^2(f) \tag{101}$$

More clearly, if the ratio of mean to standard deviation is used as a kind of signal-to-noise ratio, i.e.

$$\frac{E[S_{N_{xx}}(f)]}{\{\text{var}[S_{N_{xx}}(f)]\}^{1/2}} \cong \frac{S(f)}{S(f)} = 1 \tag{102}$$

it can be seen that the true signal spectrum is only as large as the noise or uncertainty in $S_{N_{xx}}(f)$ for increasing N. In addition, the variance of equation (101), which also is approximately applicable for non-Gaussian sequences, indicates that calculations using different sets of N samples from the same x(n) process will yield vastly different values of $S_{N_{xx}}(f)$ even when N becomes large. Unfortunately, since the variance of $S_{N_{xx}}(f)$ does not decrease to zero as N approaches infinity, the periodogram is thus an inconsistent estimate of the power spectral density and cannot be used for spectrum analysis in its present form.

7.0 SPECTRAL ESTIMATION BY AVERAGING PERIODOGRAMS

It was shown in the last section that the periodogram was not a consistent estimate of the power spectral density

function. A technique introduced by Bartlett, however, allows the use of the periodogram and, in fact, produces a consistent spectral estimation by averaging periodograms. In short, Bartlett's approach reduces the variance of the estimates by averaging together several independent periodograms. If, for example $X_1, X_2, X_3, \ldots, X_L$ are uncorrelated random variables having an expected value E[x] and a variance σ^2, then the arithmetic mean

$$\frac{X_1 + X_2 + X_3 + \ldots + X_L}{L} \tag{103}$$

has the expected value E[x] and a variance of σ^2/L. This fact suggests that a spectral estimator can have its variance reduced by a factor of L over the periodogram. The procedure requires the observed process, an N point data sequence, to be split up into L nonoverlapping M point sections and then averaging the periodograms of each individual section.

To be more specific, dividing an N point data sequence x(n), $0 \le n \le N-1$, into L segments of M samples each the segments $X_M^{\ell}(n)$ are formed. Thus,

$$x_M^{\ell}(f) = x(n + \ell M - M) \quad \begin{cases} 0 \le n \le M-1 \\ 1 \le \ell \le L \end{cases} \tag{104}$$

where the superscript ℓ specifies the segment or interval of data being observed, the subscript M represents the number of data points or samples per segment and depending upon the choice of L and M, we have $N \ge LM$. For the computation of L periodograms

$$S_M^{\ell}(f) = \left| \frac{1}{M} \sum_{n=0}^{M-1} x_M^{\ell}(n)\, \epsilon^{-j\omega nT} \right|^2 \quad 1 \le \ell \le L \tag{105}$$

If the autocorrelation function $R_{N_{xx}}(m)$ becomes negligible for m large relative to M, $m > M$, then it can be said that the periodograms of the separate sections are virtually independent of one another. The corresponding *averaged periodogram estimator* $\hat{S}_M^{\ell}(f)$ computed from L individual periodograms of length M is thus defined

$$\hat{S}_M^{\ell}(f) = \frac{1}{L} \sum_{\ell=1}^{L} S_M^{\ell}(f) \tag{106}$$

Since the L subsidiary estimates are identically distributed periodograms, the averaged spectral estimate will have the same mean or expected value as any of the subsidiary estimates so

$$E[\hat{S}_M^{\ell}(f)] = \frac{1}{L} \sum_{\ell=1}^{L} E[S_M^{\ell}(f)] \tag{107}$$

$$= E[S_M^{\ell}(f)] \tag{108}$$

From this, the expected value of the Bartlett estimate can be said to be the convolution of the true spectral density with the Fourier transform of the triangular window function corresponding to the M sample periodogram where $M \le N/L$ equations (98) or (99) we see that

$$E[\hat{S}_M^{\ell}(f)] = E[S_M^{\ell}(f)] = \frac{1}{M} \int_{-1/2}^{1/2} S(\eta)\, A(f - \eta)\, d\eta \tag{109}$$

where A(f) is the Fourier transformed triangular window function of equation (100). Though the averaged estimate is no different than before, its variance, however, is smaller. Recall that the variance of the average of L identical independent random variables is 1/L of the individual variances, equation (51). Thus, for L statistically independent periodograms, the variance of the averaged estimate is

$$\text{var}[\hat{S}_M^{\ell}(f)] = \frac{1}{L} \text{var}[S_{N_{xx}}(f)] \cong \frac{1}{L} [S(f)]^2 \tag{110}$$

So, again, the averaging of L periodograms results in approximately a factor of L reduction in power spectral density estimation variance. Since the variance of equation (110) tends to zero as L approaches infinity and through equation (98) and (99) $\hat{S}_M^{\ell}(f)$ is asymptotically unbiased, $\hat{S}_M^{\ell}(f)$ can be said to be a consistent estimate of the true spectrum.

A few notes are next in order. First, the L fold variance reduction or $(L)^{1/2}$ signal-to-noise ratio improvement of equation (102) is not precisely accurate since there is some dependence between the subsidiary periodograms. The adjacent samples will correlated unless the process being analyzed is white.

However, as indicated in equation (110), such a dependence will be small when there are many sample intervals per periodogram so that the reduced variance is still a good approximation. Secondly, the bias of $\hat{S}_M^{\ell}(f)$, equation (106), is greater than $\hat{S}_M^{\ell}(f)$, equation (105), since the main lobe of the spectral window is larger for the former. For this situation, then, the bias can be thought of as effecting spectral resolution. It is seen that increasing the number of periodograms for a fixed record length N decreases not only the variance but, the samples per periodograms M decrease also. This decreases the spectral resolution. Thus when using the Bartlett procedure the actual choice of M and N will typically be selected from prior knowledge of a signal or data sequence under consideration. The tradeoff, however, will be between the spectral resolution of bias and the variance of the estimate.

8.0 WINDOWS

Prior to looking at other techniques of spectrum estimation, we find that to this point the subject of spectral windows has been brought up several times during the course of our discussion. No elaboration, however, has been spent explaining their spectral effects and meaning. It is thus appropriate at this juncture to diverge for a short while to develop a fundamental understanding of windows and their spectral implications prior to the discussion of Sections 9 and 10 (for an in depth study of windows see *Windows, Harmonic Analysis and the Discrete Fourier Transform*; Frederic J. Harris; submitted to IEEE Proceedings, August 1976).

In most applications it is desirable to taper a finite length data sequence at each end to enhance certain characteristics of the spectral estimate. The process of terminating a sequence after a finite number of terms can be thought of as multiplying an infinite length, i.e., impulse response sequence by a finite width window function. In other words, the window function determines how much of the original impulse sequence can be observed through this window,

see *Figures 4a, 4b,* and *4c*. This tapering by mulitiplying the sequence by a data window is thus analogous to multiplying the correlation function by a lag window. In addition, since multiplication in the time domain is equivalent to convolution in the frequency domain then it is also analogous to convolving the Fourier transform of a finite-length-sequence with the Fourier transform of the window function, *Figures 4d, 4e,* and *4f*. Note also that the Fourier transform of the rectangular window function exhibits significant oscillations and poor high frequency convergence, *Figure 4e*. Thus, when convolving this spectrum with a desired amplitude function, poor convergence of the resulting amplitude response may occur. This calls for investigating the use of other possible window functions that minimize some of the difficulties encountered with rectangular function.

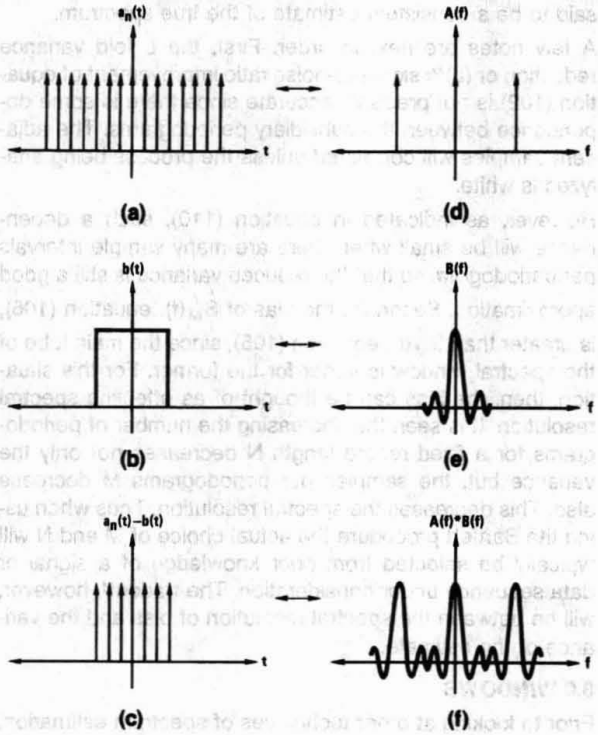

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FIGURE 4

In order for the spectrum of a window function to have minimal effects upon the desired amplitude response, resulting from convolving two functions, it is necessary that the window spectrum approximate an impulse function. This implies that as much of its energy as possible should be concentrated at the center of the spectrum. Clearly, an ideal impulse spectrum is not feasible since this requires an infinitely long window.

In general terms, the spectrum of a window function typically consists of a main lobe, representing the center of the spectrum, and various side lobes, located on either side of the main lobe (see *Figures 6* thru *9*). It is desired that the window function satisfy two criteria; (1) that the main lobe should be as narrow as possible and (2) relative to the main lobe, the maximum side lobe level should be as small as possible. Unfortunately, however, both conditions cannot be simultaneously optimized so that, in practice, usable window functions represent a suitable compromise between the two criteria. A window function in which minimization of the main lobe width is the primary objective, fields a finer frequency resolution but suffers from some oscillations, i.e., the spectrum passband and substantial ripple in the spectrum stopband. Coversely, a window function in which minimization of the side lobe level is of primary concern tends to have a smoother amplitude response and very low ripple in the stopband but, yields a much poorer frequency resolution. Examining *Figure 5* assume a hypothetical impulse response, *Figure 5a*, whose spectrum is *Figure 5b*. Multiplying the impulse response by the rectangular window, *Figure 4b*, yields the windowed impulse response, *Figure 5c*, implying the convolution of the window spectrum, *Figure 4e*, with the impulse response spectrum, *Figure 5b*. The result of this convolution is seen in *Figure 5d* and is a distorted version of the ideal spectrum, *Figure 5b*, having passband oscillations and stopband ripple. Selecting another window, i.e., *Figure 9* with more desirable spectral characteristics, we see the appropriately modified windowed data, *Figure 5e*, results in a very good approximation of *Figure 5b*.

This characteristically provides a smoother passband and lower stopband ripple level but sacrifices the sharpness of the roll-off rate inherent in the use of a rectangular window (compare *Figures 5d* and *5f*). Concluding this brief discussion, a few common window functions will next be considered.

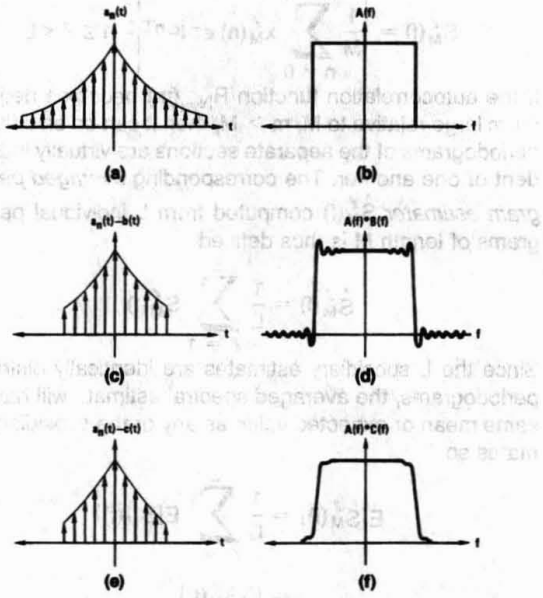

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FIGURE 5. (a)(b) Unmodified Data Sequence (c)(d) Rectangular Windowed Data Sequence (e)(f) Hamming Windowed Data Sequence

Rectangular window: *Figure 6*

$$w(n) = 1 \qquad |n| < \frac{N-1}{2} \qquad (111)$$

$$= 0 \qquad \text{otherwise}$$

Bartlett or triangular window: *Figure 7*

$$w(n) = 1 - \frac{2|n|}{N} \qquad |n| < \frac{N-1}{2} \qquad (112)$$

$$= 0 \qquad \text{otherwise}$$

Hann window: *Figure 8*

$$w(n) = 0.5 + 0.5 \cos\left(\frac{2\pi n}{N}\right) \qquad |n| < \frac{N-1}{2} \qquad (113)$$

$$= 0 \qquad \text{otherwise}$$

Hamming window: *Figure 9*

$$w(n) = 0.54 + 0.46 \cos\left(\frac{2\pi n}{N}\right) \qquad |n| < \frac{N-1}{2} \qquad (114)$$

$$= 0 \qquad \text{otherwise}$$

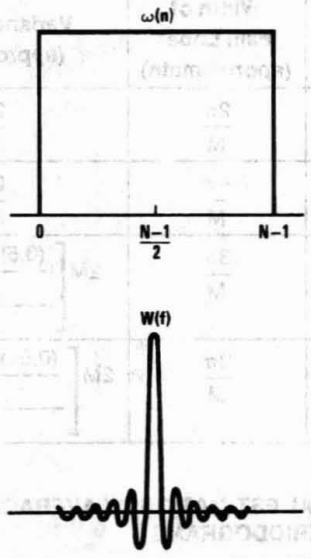

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FIGURE 6. Rectangular Window

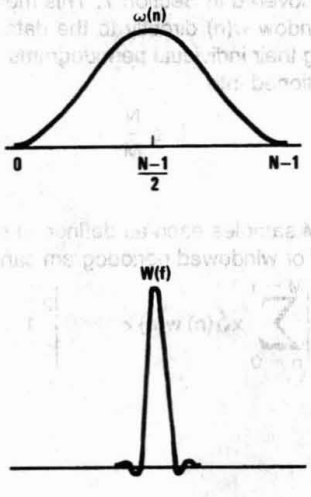

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FIGURE 7. Bartlett or Triangular Window

Again the reference previously cited should provide a more detailed window selection. Nevertheless, the final window choice will be a compromise between spectral resolution and passband (stopband) distortion.

9.0 SPECTRAL ESTIMATION BY USING WINDOWS TO SMOOTH A SINGLE PERIODOGRAM

It was seen in a previous section that the variance of a power spectral density estimate based on an N point data sequence could be reduced by chopping the data into shorter segments and then averaging the periodograms of the individual segments. This reduced variance was acquired at the expense of increased bias and decreased spectral resolution. We will cover in this section an alternate way of computing a reduced variance estimate using a smoothing operation on the single periodogram obtained from the entire N point data sequence. In effect, the periodogram is smoothed by convolving it with an appropriate spectral window. Hence if $S_{XX}(f)$ denotes the smooth periodogram then,

$$S_{W_{XX}}(f) = \int_{-1/2}^{1/2} S_{N_{XX}}(\eta)\, W(f-\eta)\, d\eta = S_{N_{XX}}(\eta) * W(\eta) \qquad (115)$$

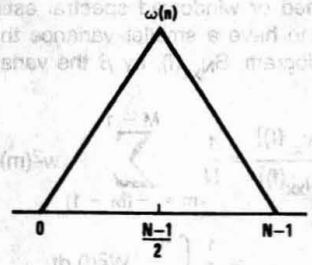

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FIGURE 8. Hann Window

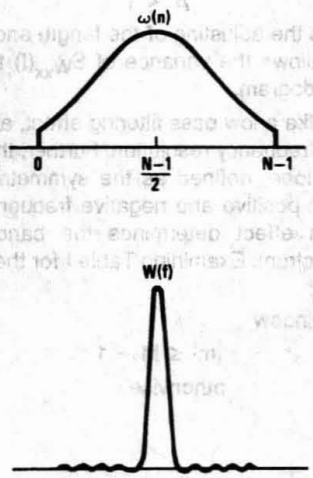

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FIGURE 9. Hamming Window

where $W(f - \eta)$ is the spectral window and * denotes convolution. Since the periodogram is equivalent to the Fourier transform of the autocorrelation function $R_{N_{xx}}(k)$ then, using the frequency convolution theorem

$$F\{x(t)\, y(t)\} = X(f) * Y(\eta - f) \tag{116}$$

where $F\{\ \}$ denotes a Fourier transform, $S_{XX}(f)$ is the Fourier transform of the product of $R_{N_{xx}}(k)$ and the inverse Fourier transform of $W(f)$. Therefore for a finite duration window sequence of length $2K - 1$,

$$S_{W_{xx}}(f) = \sum_{k\,=\,-(K\,-\,1)}^{K\,-\,1} R_{N_{xx}}(k)\, w(k)\, \epsilon^{-j\omega kT} \tag{117}$$

where

$$w(k) = \sum_{-1/2}^{1/2} W(f)\, \epsilon^{j\omega kT}\, df \tag{118}$$

References (10)(16)(21) proceed further with a development to show that the smoothed single windowed periodogram is a consistent estimate of the power spectral density function. The highlights of the development, however, show that a smoothed or windowed spectral estimate, $S_{W_{xx}}(f)$, can be made to have a smaller variance than that of the straight periodogram, $S_{N_{xx}}(f)$, by β the variance ratio relationship

$$\beta = \frac{\text{var}\,[S_{W_{xx}}(f)]}{\text{var}\,[S_{N_{xx}}(f)]} = \frac{1}{N} \sum_{m\,=\,-(M\,-\,1)}^{M\,-\,1} w^2(m) = \frac{1}{N} \int_{-1/2}^{1/2} W^2(f)\, df \tag{119}$$

where N is the record length and $2M - 1$ is the total window width. Note that the energy of the window function can be found in equation (119) as

$$E_\omega = \sum_{m\,=\,-(M\,-\,1)}^{M\,-\,1} w^2(m) = \int_{-1/2}^{1/2} W^2(f)\, df \tag{120}$$

Continuing from equation (119), it is seen that a satisfactory estimate of the periodogram requires the variance of $S_{W_{xx}}(f)$ to be small compared to $S^2_{N_{xx}}$ so that

$$\beta \ll 1 \tag{121}$$

Therefore, it is the adjusting of the length and shape of the window that allows the variance of $S_{W_{xx}}(f)$ to be reduced over the periodogram.

Smoothing is like a low pass filtering effect, and so, causes a reduction in frequency resolution. Further, the width of the window main lobe, defined as the symmetric interval between the first positive and negative frequencies at which $W(f) = 0$, in effect determines the bandwidth of the smoothed spectrum. Examining Table I for the following defined windows;

Rectangular window

$$w(m) = 1 \qquad |m| \le M - 1 \tag{122}$$
$$= 0 \qquad \text{otherwise}$$

Bartlett or triangular window

$$w(m) = 1 - \frac{|m|}{M} \qquad |m| \le M - 1 \tag{123}$$
$$= 0 \qquad \text{otherwise}$$

Hann window

$$w(m) = 0.5 + 0.5 \cos\left(\frac{\pi m}{M - 1}\right) \qquad |m| \le M - 1 \tag{124}$$
$$= 0 \qquad \text{otherwise}$$

Hamming window

$$w(m) = 0.54 + 0.46 \cos\left(\frac{\pi m}{M - 1}\right) \qquad |m| \le M - 1 \tag{125}$$
$$= 0 \qquad \text{otherwise}$$

We see once again, as in the averaging technique of spectral estimation (Section 7), the smoothed periodogram technique of this discussion also makes a trade-off between variance and resolution for a fixed N. A small variance requires a small M while high resolution requires a large M.

TABLE I

Window Function	Width of Main Lobe* (approximate)	Variance Ratio* (approximate)
Rectangular	$\frac{2\pi}{M}$	$\frac{2M}{N}$
Bartlett	$\frac{4\pi}{M}$	$\frac{2M}{3N}$
Hann	$\frac{3\pi}{M}$	$2M\left[\frac{(0.5)^2 + \frac{(0.5)^2}{2}}{N}\right]$
Hamming	$\frac{3\pi}{M}$	$2M\left[\frac{(0.54)^2 + \frac{(0.46)^2}{2}}{N}\right]$

*Assumes $M \gg 1$

10.0 SPECTRAL ESTIMATION BY AVERAGING MODIFIED PERIODOGRAMS

Welch [Ref. (36)(37)] suggests a method for measuring power spectra which is effectively a modified form of Bartlett's method covered in Section 7. This method, however, applies the window w(n) directly to the data segments before computing their individual periodograms. If the data sequence is sectioned into

$$L \le \frac{N}{M}$$

segments of M samples each as defined in equation (104), the L modified or windowed periodogram can be defined as

$$I^{\ell}_M(f) = \frac{1}{UM} \left| \sum_{n\,=\,0}^{M\,-\,1} x^{\ell}_M(n)\, w(n)\, \epsilon^{-j\omega nT} \right|^2 \quad 1 \le \ell \le L \tag{126}$$

where U, the energy in the window is

$$U = \frac{1}{M}\sum_{n=0}^{M=1} w^2(n) \qquad (127)$$

Note the similarity between equations (126) and (105) and that equation (126) is equal to equation (105) modified by functions of the data window w(n).

The spectral estimate $\hat{I}_M^{\ell}$ is defined as

$$\hat{I}_M^{\ell}(f) = \frac{1}{L}\sum_{\ell=1}^{L} I_M^{\ell}(f) \qquad (128)$$

and its expected value is given by

$$E[I_M^{\ell}(f)] = \int_{-1/2}^{1/2} S_{N_{xx}}(\eta)\, W(f-\eta)\, d\eta = S_{N_{xx}}(\eta) * W(\eta) \qquad (129)$$

where

$$W(f) = \frac{1}{UM}\left|\sum_{n=0}^{M=1} w(n)\, \epsilon^{-j\omega nT}\right|^2 \qquad (130)$$

The normalizing factor U is required so that the spectral estimate $\hat{I}_m^{\ell}(f)$, of the modified periodogram, $\hat{I}_m^{\ell}(f)$, will be asymptotically unbiased [Ref. (34)]. If the intervals of x(n) were to be nonoverlapping, then Welch [Ref. (37)] indicates that

$$\text{var}\,[\hat{I}_m^{\ell}(f)] \cong \frac{1}{L}\,\text{var}\,[S_{N_{xx}}(f)] \cong \frac{1}{L}\,[S(f)]^2 \qquad (131)$$

which is similar to that of equation (110). Also considered is a case where the data segments overlap. As the overlap increases the correlation between the individual periodograms also increase. We see further that the number of M point data segments that can be formed increases. These two effects counteract each other when considering the variance $I_m^{\ell}(f)$. With a good data window, however, the increased number of segments has the stronger effect until the overlap becomes too large. Welch has suggested that a 50 percent overlap is a reasonable choice for reducing the variance when N if fixed and cannot be made arbitrarily large. Thus, along with windowing the data segments prior to computing their periodograms, achieves a variance reduction over the Bartlett technique and at the same time smooths the spectrum at the cost of reducing its resolution. This trade-off between variance and spectral resolution or bias is an inherent property of spectrum estimators.

11.0 PROCEDURES FOR POWER SPECTRAL DENSITY ESTIMATES

Smoothed single periodograms [Ref. (21)(27)(32)]

A. 1. Determine the sample autocorrelation $R_{N_{xx}}(k)$ of the data sequence x(n)

2. Multiply $R_{N_{xx}}(k)$ by an appropriate window function w(n)

3. Compute the Fourier transform of the product

$$R_{N_{XX}}(k)\, w(n) \longleftrightarrow S_{W_{xx}}(f) \qquad (71)$$

B. 1. Compute the Fourier transform of the data sequence x(n)

$$x(n) \longleftrightarrow X(f)$$

2. Multiply X(f) by its conjugate to obtain the power spectral density $S_{N_{xx}}(f)$

$$S_{N_{xx}}(f) = \frac{1}{N}|X(f)|^2 \qquad (74)$$

3. Convolve $S_{N_{xx}}(f)$ with an appropriate window function W(f)

$$S_{W_{xx}}(f) = S_{N_{xx}}(f) * W(f) \qquad (115)$$

C. 1. Compute the Fourier transform of the data sequence x(n)

$$x(n) \longleftrightarrow X(f)$$

2. Multiply X(f) by its conjugate to obtain the power spectral density $S_{N_{xx}}(f)$

$$S_{N_{xx}}(f) = \frac{1}{N}|X(f)|^2 \qquad (74)$$

3. Inverse Fourier transform $S_{N_{xx}}(f)$ to get $R_{N_{xx}}(k)$

4. Multiply $R_{N_{xx}}(k)$ by an appropriate window function w(n)

5. Compute the Fourier transform of the product to obtain $S_{W_{xx}}(f)$

$$S_{W_{xx}}(f) \longleftrightarrow R_{N_{xx}}(k) \bullet w(n) \qquad (117)$$

Averaging periodograms [Ref. (32)(37)(38)]

A. 1. Divide the data sequence x(n) into $L \leq N/M$ segments, $x_M^{\ell}(n)$

2. Multiply a segment by an appropriate window

3. Take the Fourier transform of the product

4. Multiply procedure 3 by its conjugate to obtain the spectral density of the segment

5. Repeat procedures 2 through 4 for each segment so that the average of these periodogram estimates produce the power spectral density estimate, equation (128)

12.0 RESOLUTION

In analog bandpass filters, resolution is defined by the filter bandwidth, Δf_{BW}, measured at the passband half power points. Similarly, in the measurement of power spectral density functions it is important to be aware of the resolution capabilities of the sampled data system. For such a system resolution is defined as

$$\Delta f_{BW} = \frac{1}{NT} \qquad (132)$$

and for;

Correlation resolution

$$\Delta f_{BW} = \frac{1}{\tau_{max}} \qquad (133)$$

$\tau_{max} = mT$, where m is the maximum value allowed to produce τ_{max}, the maximum lag term in the correlation computation

Fourier transform (FFT) resolution

$$\Delta f_{BW} = \frac{1}{P_L} = \frac{m}{NT} = \frac{1}{LT}$$

where P is the record length, N, the number of data points and m, the samples within each L segment,

$$L = \frac{N}{M}. \quad (134)$$

Note that the above Δf_{BW}'s can be substantially poorer depending upon the choice of the data window. A loss in degrees of freedom (Section 13) and statistical accuracy occurs when a data sequence is windowed. That is, data at each end of a record length are given less weight than the data at the middle for anything other than the rectangular window. This loss in degrees of freedom shows up as a loss in resolution because the main lobe of the spectral window is widened in the frequency domain.

Finally, the limits of a sampled data system can be described in terms of the maximum frequency range and minimum frequency resolution. The maximum frequency range is the Nyquist or folding frequency, f_c,

$$f_c = \frac{f_s}{2} = \frac{1}{2T_s} \quad (135)$$

where f_s is the sampling frequency and T_s the sampling period. And, secondly, the resolution limit can be described in terms of a (Δf_{BW}) NT product where

$$\Delta f_{BW} \geq \frac{1}{NT} \quad (136)$$

or

$$(\Delta f_{BW})\, NT \geq 1 \quad (137)$$

13.0 CHI-SQUARE DISTRIBUTIONS

Statistical error is the uncertainty in power spectral density measurements due to the amount of data gathered, the probabilistic nature of the data and the method used in deriving the desired parameter. Under reasonable conditions the spectral density estimates approximately follow a chi-square, χ_n^2, distribution. χ_n^2 is defined as the sum of the squares of χ_n, $1 \leq n \leq N$, independent Gaussian variables each with a zero mean and unit variance such that

$$\chi_N^2 = \sum_{n=1}^{N} \chi_n^2 \quad (138)$$

The number n is called the *degrees of freedom* and the χ_n^2 probability density function is

$$f(\chi_n^2) = \frac{1}{2^{n/2}\Gamma\left(\frac{n}{2}\right)}\left[(\chi_n^2)^{\frac{n-2}{2}}\right]\epsilon^{\frac{-\chi_n^2}{2}} \quad (139)$$

where $\Gamma\left(\frac{n}{2}\right)$ is the statistical gamma function (Ref. (14)].

Figure 10 shows the probability density function for several n values and it is important to note that as n becomes large the chi-square distribution approximates a Gaussian distribution. We use this χ_n^2 distribution in our analysis to discuss the variability of power spectral densities. If x_n has a zero mean and N samples of it are used to compute the power spectral density estimate S(f) then, the probability that the true spectral density, S(f), lies between the limits

$$A \leq S(f) \leq B \quad (140)$$

is

$$P = (1 - \alpha) = \text{probability} \quad (141)$$

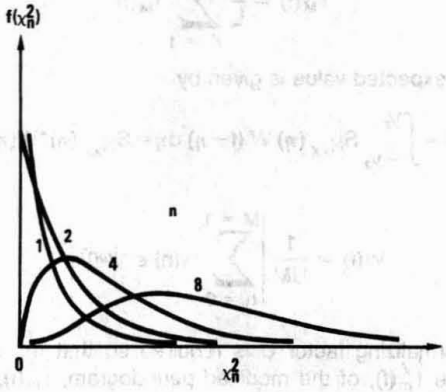

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FIGURE 10

The lower A and upper B limits are defined as

$$A = \frac{n\hat{S}(f)}{\chi^2_{n;\frac{\alpha}{2}}} \quad (142)$$

and

$$B = \frac{n\hat{S}(f)}{\chi^2_{n;1-\frac{\alpha}{2}}} \quad (143)$$

respectively. $\chi^2_{n;\alpha}$ is defined by

$$\chi^2_{n;\alpha} = \left[\nu \text{ so that } \int_{\nu}^{\infty} f(\chi_n^2)\, d\chi_n^2\right] = \alpha \quad (144)$$

see *Figure 11* and the interval A to B is referred to as a confidence interval. From Otnes and Enrochson [Ref. (35) pg. 217] the degrees of freedom can be described as

$$n = 2(\Delta f_{BW})\, NT = 2(\Delta f_{BW})\, P_L \quad (145)$$

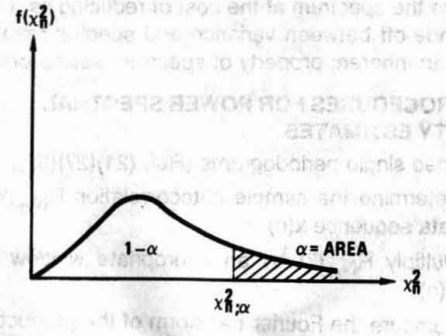

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FIGURE 11

and that for large n i.e., $n \geq 30$ the χ^2_n distribution approaches a Gaussian distribution so that the standard deviation or standard error, ϵ_o, can be given by

$$\epsilon_o = \frac{1}{\sqrt{\Delta f_{BW}\, NT}} \tag{146}$$

The degrees of freedom and associated standard error for the correlation and Fourier transform are as follows:

$$\text{correlation: } n = \frac{2N}{m} \qquad \epsilon_o = \sqrt{\frac{m}{N}} \tag{147}$$

$$\text{FFT: } n = 2M \qquad \epsilon_o = \sqrt{\frac{1}{M}} \tag{148}$$

where M is the number of $|X(f)|^2$ values

$$M = NT\,(\Delta f_{BW})_{desired} \tag{149}$$

and m is the maximum lag value.

An example will perhaps clarify the usage of this information.

Choosing T = 100 ms, N = 8000 samples and n = 20 degrees of freedom then

$$f_c = \frac{1}{2T} = 5 \text{ Hz}$$

$$n = 2(NT)\,(\Delta f_{BW})$$

so

$$\Delta f_{BW} = \frac{n}{2NT} = 0.0125 \text{ Hz}$$

If it is so desired to have a 95% confidence level of the spectral density estimate then

$$P = (1 - \alpha)$$

$$0.95 = 1 - \alpha$$

$$\alpha = 1 - 0.95 = 0.05$$

the limits

$$B = \frac{n\hat{S}(f)}{\chi^2_{n;\,1-\alpha/2}} = \frac{20\hat{S}(f)}{\chi^2_{20;\,0.975}}$$

$$A = \frac{n\hat{S}(f)}{\chi^2_{n;\,\alpha/2}} = \frac{20\hat{S}(f)}{\chi^2_{20;\,0.025}}$$

yield from Table II

$$\chi^2_{20;\,0.975} = 9.59$$

$$\chi^2_{20;\,0.025} = 34.17$$

so that

$$\frac{20\hat{S}(f)}{34.17} \leq S(f) \leq \frac{20\hat{S}(f)}{9.59}$$

$$0.5853\,\hat{S}(f) \leq S(f) \leq 2.08\,\hat{S}(f)$$

There is thus a 95% confidence level that the true spectral density function S(f) lies within the interval $0.5853\,\hat{S}(f) \leq S(f) \leq 2.08\,\hat{S}(f)$.

As a second example using equation (148) let T = 1 ms, N = 4000 and it is desired to have (Δf_{BW}) desired = 10 Hz. Then,

$$NT = 4$$

$$f_c = \frac{1}{2T} = 500 \text{ Hz}$$

$$\epsilon_o = \sqrt{\frac{1}{M}} = \sqrt{\frac{1}{NT\,(\Delta f_{BW})_{desired}}} = 0.158$$

$$N = 2M = 2NT\,(\Delta f_{BW})_{desired} = 80$$

If it is again desired to have a 95% confidence level of the spectral density estimate then

$$\alpha = 1 - p = 0.05$$

$$\chi^2_{80;\,0.975} = 5.75$$

$$\chi^2_{80;\,0.025} = 106.63$$

and we thus have a 95% confidence level that the true spectral density S(f) lies within the limits

$$0.75\,\hat{S}(f) \leq S(f) \leq 1.39\,\hat{S}(f)$$

It is important to note that the above examples assume Gaussian and white data. In practical situations the data is typically colored or correlated and effectively results in reducing number of degrees of freedom. It is best, then, to use the white noise confidence levels as guidelines when planning power spectral density estimates.

14.0 CONCLUSION

This article attempted to introduce to the reader a conceptual overview of power spectral estimation. In doing so a wide variety of subjects were covered and it is hoped that this approach left the reader with a sufficient base of "tools" to indulge in the mounds of technical literature available on the subject.

15.0 ACKNOWLEDGEMENTS

The author wishes to thank James Moyer and Barry Siegel for their support and encouragement in the writing of this article.

TABLE II. Percentage Points of the Chi-Square Distribution

n	α							
	0.995	0.990	0.975	0.950	0.050	0.025	0.010	0.005
1	0.000039	0.00016	0.00098	0.0039	3.84	5.02	6.63	7.88
2	0.0100	0.0201	0.0506	0.1030	5.99	7.38	9.21	10.60
3	0.0717	0.115	0.216	0.352	7.81	9.35	11.34	12.84
4	0.207	0.297	0.484	0.711	9.49	11.14	13.28	14.86
5	0.412	0.554	0.831	1.150	11.07	12.83	15.09	16.75
6	0.68	0.87	1.24	1.64	12.59	14.45	16.81	18.55
7	0.99	1.24	1.69	2.17	14.07	16.01	18.48	20.28
8	1.34	1.65	2.18	2.73	15.51	17.53	20.09	21.96
9	1.73	2.09	2.70	3.33	16.92	19.02	21.67	23.59
10	2.16	2.56	3.25	3.94	18.31	20.48	23.21	25.19
11	2.60	3.05	3.82	4.57	19.68	21.92	24.72	26.76
12	3.07	3.57	4.40	5.23	21.03	23.34	26.22	28.30
13	3.57	4.11	5.01	5.89	22.36	24.74	27.69	29.82
14	4.07	4.66	5.63	6.57	23.68	26.12	29.14	31.32
15	4.60	5.23	6.26	7.26	25.00	27.49	30.58	32.80
16	5.14	5.81	6.91	7.96	26.30	28.85	32.00	34.27
17	5.70	6.41	7.56	8.67	27.59	30.19	33.41	35.72
18	6.26	7.01	8.23	9.39	28.87	31.53	34.81	37.16
19	6.84	7.63	8.91	10.12	30.14	32.85	36.19	38.58
20	7.43	8.26	9.59	10.85	31.41	34.17	37.57	40.00
21	8.03	8.90	10.28	11.59	32.67	35.48	38.93	41.40
22	8.64	9.54	10.98	12.34	33.92	36.78	40.29	42.80
23	9.26	10.20	11.69	13.09	35.17	38.08	41.64	44.18
24	9.89	10.86	12.40	13.85	36.42	39.36	42.98	45.56
25	10.52	11.52	13.12	14.61	37.65	40.65	44.31	46.93
26	11.16	12.20	13.84	15.38	38.89	41.92	45.64	48.29
27	11.81	12.88	14.57	16.15	40.11	43.19	46.96	49.64
28	12.46	13.56	15.31	16.93	41.34	44.46	48.28	50.99
29	13.12	14.26	16.05	17.71	42.56	45.72	49.59	52.34
30	13.79	14.95	16.79	18.49	43.77	46.98	50.89	53.67
40	20.71	22.16	24.43	26.51	55.76	59.34	63.69	66.77
50	27.99	29.71	32.36	34.76	67.50	71.42	76.15	79.49
60	35.53	37.48	40.48	43.19	79.08	83.80	88.38	91.95
70	43.28	45.44	48.76	51.74	90.53	95.02	100.43	104.22
80	51.17	53.54	57.15	60.39	101.88	106.63	112.33	116.32
90	59.20	61.75	65.65	69.13	113.14	118.14	124.12	128.30
100	67.33	70.06	74.22	77.93	124.34	129.56	135.81	140.17

APPENDIX A

A.0 CONCEPTS OF PROBABILITY, RANDOM VARIABLES AND STOCHASTIC PROCESSES

In many physical phenomena the outcome of an experiment may result in fluctuations that are random and cannot be precisely predicted. It is impossible, for example, to determine whether a coin tossed into the air will land with its head side or tail side up. Performing the same experiment over a long period of time would yield data sufficient to indicate that on the average it is equally likely that a head or tail will turn up. Studying this average behavior of events allows one to determine the frequency of occurrence of the outcome (i.e., heads or tails) and is defined as the notion of *probability*.

Associated with the concept of probability are probability density functions and cumulative distribution functions which find their use in determining the outcome of a large number of events. A result of analyzing and studying these functions may indicate regularities enabling certain laws to be determined relating to the experiment and its outcomes; this is essentially known as *statistics*.

A.1 DEFINITIONS OF PROBABILITY

If n_A is the number of times that an event A occurs in N performances of an experiment, the frequency of occurrence of event A is thus the ratio n_A/N. Formally, the probability, P(A), of event A occurring is defined as

$$P(A) = \lim_{N \to \infty} \left[\frac{n_A}{N}\right] \qquad \text{(A.1-1)}$$

Where it is seen that the ratio n_A/N (or fraction of times that an event occurs) asymptotically approaches some mean value (or will show little deviation from the exact probability) as the number of experiments performed, N, increases (more data).

Assigning a number,

$$\frac{n_A}{N},$$

to an event is a measure of how likely or probable the event.

Since n_A and N are both positive and real numbers and $0 \leq n_A \leq N$; it follows that the probability of a given event cannot be less than zero or greater than unity. Furthermore, if the occurrence of any one event excludes the occurrence of any others (i.e., a head excludes the occurrence of a tail in a coin toss experiment), the possible events are said to be *mutually exclusive*. If a complete set of possible events A_1 to A_n are included then

$$\frac{n_{A_1}}{N} + \frac{n_{A_2}}{N} + \frac{n_{A_3}}{N} + \ldots + \frac{n_{A_n}}{N} = 1 \qquad \text{(A.1-2)}$$

or

$$P(A_1) + P(A_2) + P(A_3) + \ldots + P(A_n) = 1 \qquad \text{(A.1-3)}$$

Similarly, an event that is absolutely certain to occur has a probability of one and an impossible event has a probability of zero.

In summary:

1. $0 \leq P(A) \leq 1$
2. $P(A_1) + P(A_2) + P(A_3) + \ldots + P(A_n) = 1$, for an entire set of events that are mutually exclusive
3. $P(A) = 0$ represents an impossible event
4. $P(A) = 1$ represents an absolutely certain event

A.2 JOINT PROBABILTY

If more than one event at a time occurs (i.e., events A and B are not mutually excusive) the frequency of occurrence of the two or more events at the same time is called the *joint probability*, P(AB). If n_{AB} is the number of times that event A and B occur together in N performances of an experiment, then

$$P(A,B) = \lim_{N \to \infty} \left[\frac{n_{AB}}{N}\right] \qquad \text{(A.2-1)}$$

A.3 CONDITIONAL PROBABILITY

The probability of event B occurring given that another event A has already occurred is called *conditional probability*. The dependence of the second, B, of the two events on the first, A, will be designated by the symbol P(B)|A) or

$$P(B|A) = \frac{n_{AB}}{n_A} \qquad \text{(A.3-1)}$$

where n_{AB} is the number of joint occurrences of A and B and N_A represents the number of occurrences of A with or without B. By dividing both the numerator and denominator of equation (A.3-1) by N, conditional probability P(B|A) can be related to joint probability, equation (A.2-1), and the probability of a single event, equation (A.1-1)

$$P(B|A) = \left(\frac{n_{AB}}{n_A}\right)\left(\frac{\frac{1}{N}}{\frac{1}{N}}\right) = \frac{P(A,B)}{P(A)} \qquad \text{(A.3-2)}$$

Analogously

$$P(A|B) = \frac{P(A,B)}{P(A)} \qquad \text{(A.3-3)}$$

and combining equations (A.6) and (A.7)

$$P(A|B)\,P(B) = P(A,B) = P(B|A)\,P(A) \qquad \text{(A.3-4)}$$

results in Bayes' theorem

$$P(A|B) = \frac{P(A)\,P(B|A)}{P(B)} \qquad \text{(A.3-5)}$$

Using Bayes' theorem, it is realized that if P(A) and P(B) are *statistically independent* events, implying that the probability of event A does not depend upon whether or not event B has occurred, then $P(A|B) = P(A)$, $P(B|A) = P(B)$ and hence the joint probability of events A and B is the product of their individual probabilities or

$$P(A,B) = P(A)\,P(B) \qquad \text{(A.3-6)}$$

More precisely, two random events are statistically independent only if equation (A.3-6) is true.

A.4 PROBABILITY DENSITY FUNCTIONS

A formula, table, histogram, or graphical representation of the probability or possible frequency of occurrence of an event associated with variable X, is defined as $f_X(x)$, the *probability density function* (pdf) or *probability distribution function*. As an example, a function corresponding to height histograms of men might have the probability distribution function depicted in *Figure A.4.1*.

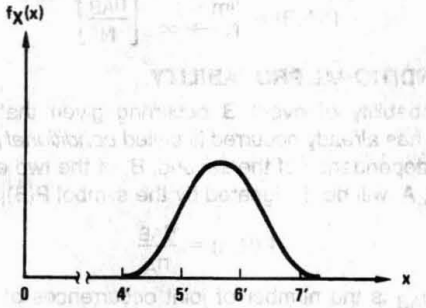

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FIGURE A.4.1

The *probability element*, $f_X(x)\,dx$, describes the probability of the event that the random variable X lies within a range of possible values between

$$\left(x - \frac{\Delta x}{2}\right) \text{ and } \left(x + \frac{\Delta x}{2}\right)$$

i.e., the area between the two points 5′5″ and 5′7″ shown in *Figure A.4.2* represents the probability that a man's height will be found in that range. More clearly,

(A.4-1)

$$\text{Prob}\left[\left(x - \frac{\Delta x}{2}\right) \le X \le \left(x + \frac{\Delta x}{2}\right)\right] = \int_{x-\frac{\Delta x}{2}}^{x+\frac{\Delta x}{2}} f_X(x)\,dx$$

or

$$\text{Prob}\,[5'5'' \le X \le 5'7''] = \int_{5'5''}^{5'7''} f_X(x)\,dx$$

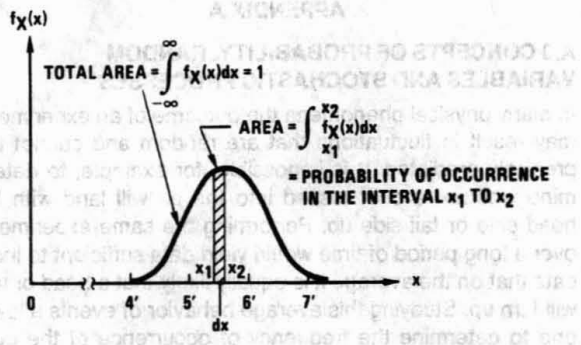

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FIGURE A.4.2

Continuing, since the total of all probabilities of the random variable X must equal unity and $f_X(x)\,dx$ is the probability that X lies within a specified interval

$$\left(x - \frac{\Delta x}{2}\right) \text{ and } \left(x - \frac{\Delta x}{2}\right),$$

then,

$$\int_{-\infty}^{\infty} f_X(x)\,dx = 1 \qquad \text{(A.4-2)}$$

It is important to point out that the density function $f_X(x)$ is in fact a mathematical description of a curve and is not a probability; it is therefore not restricted to values less than unity but can have any non-negative value. Note however, that in practical application, the integral is normalized such that the entire area under the probability density curve equates to unity.

To summarize, a few properties of $f_X(x)$ are listed below.

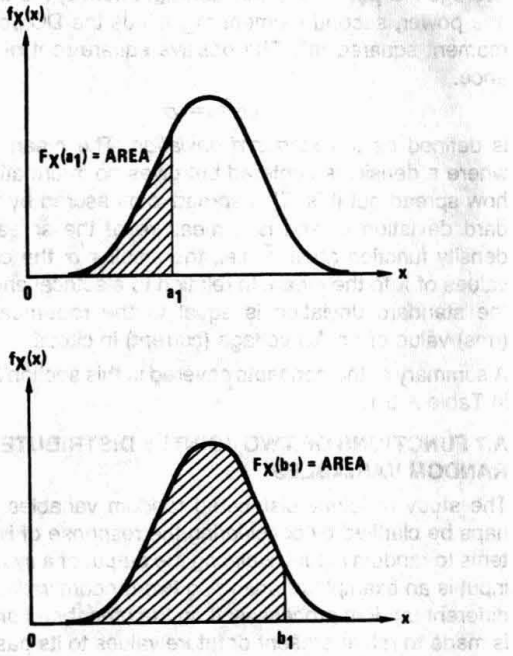
1. $f_X(x) \ge 0$ for all values of x or $-\infty < x < \infty$
2. $\int_{-\infty}^{\infty} f_X(x)\,dx = 1$
3. $\text{Prob}\left[\left(x - \frac{\Delta x}{2}\right) \le X \le \left(x + \frac{\Delta x}{2}\right)\right] = \int_{x-\frac{\Delta x}{2}}^{x+\frac{\Delta x}{2}} f_X(x)\,dx$

A.5 CUMULATIVE DISTRIBUTION FUNCTION

If the entire set of probabilities for a random variable event X are known, then since the probability element, $f_X(x)\,dx$, describes the probability that event X will occur, the accumulation of these probabilities from $x = -\infty$ to $x = \infty$ is unity or an absolutely certain event. Hence,

$$F_X(x) \int_{-\infty}^{\infty} f_X(x)\,dx = 1 \qquad \text{(A.5-1)}$$

where $F_X(x)$ is defined as the *cumulative distribution function* (cdf) or *distribution function* and $f_X(x)$ is the pdf of random variable X. Illustratively, *Figures A.5.1a* and *A.5.1b* show the probability density function and cumulative distribution function respectively.



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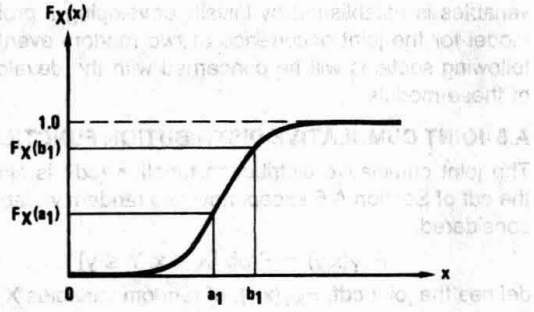
(a) Probability Density Function



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(b) Cumulative Distribution Function

FIGURE A.5.1

In many texts the notation used in describing the cdf is

$$F_X(x) = \text{Prob}[X \le x] \qquad \text{(A.5-2)}$$

and is defined to be the probability of the event that the observed random variable X is less than or equal to the allowed or conditional value x. This implies

$$F_X(x) = \text{Prob}[X \le x] = \int_{-\infty}^{x} f_X(x)\,dx \qquad \text{(A.5-3)}$$

It can be further noted that

$$\text{Prob}[x_1 \le x \le x_2] = \int_{x_1}^{x_2} f_X(x)dx = F_X(x_2) - F_X(x_1) \qquad \text{(A.5-4)}$$

and that from equation (A.5-1) the pdf can be related to the cdf by the derivative

$$f_X(x) = \frac{d[F_X(x)]}{dx} \qquad \text{(A.5-5)}$$

Re-examining *Figure A.5.1* does indeed show that the pdf, $f_X(x)$, is a plot of the differential change in slope of the cdf, $F_X(x)$.

$F_X(x)$ and a summary of its properties.

1. $0 \le F_X(x) \le 1 \quad -\infty < x < \infty$ (Since F_X = Prob [X < x] is a probability)
2. $F_X(-\infty) = 0 \; F_X(+\infty) = 1$
3. $F_X(x)$ the probability of occurrence increases as x increases
4. $F_X(x) = \int f_X(x)\,dx$
5. Prob $(x_1 \le x \le x_2) = F_X(x_2) - F_X(x_1)$

A.6 MEAN VALUES, VARIANCES AND STANDARD DEVIATION

The procedure of determining the average weight of a group of objects by summing their individual weights and dividing by the total number of objects gives the average value of x. Mathematically the discrete *sample mean* can be described

$$\bar{x} = \frac{1}{n}\sum_{i-1}^{n} x_i \qquad \text{(A.6-1)}$$

for the continuous case that *mean value* of the random variable X is defined as

$$\bar{x} = E[X] = \int_{-\infty}^{\infty} x f_X(x)\,dx \qquad \text{(A.6-2)}$$

where E[X] is read "the expected value of X".

Other names for the same *mean value* $\bar{x}$ or the *expected value* E[X] are average value and statistical average.

It is seen from equation (A.6-2) that E[X] essentially represents the sum of all possible values of x with each value being weighted by a corresponding value of the probability density function of $f_X(x)$.

Extending this definition to any function of X for example h(x), equation (A.6-2) becomes

$$E[h(x)] = \int_{-\infty}^{\infty} h(x)\, f_X(x)\,dx \qquad \text{(A.6-3)}$$

An example at this point may help to clarify matters. Assume a uniformly dense random variable of density 1/4 between the values 2 and 6, see *Figure A.6.1*. The use of equation (A.6-2) yields the expected value

$$\bar{x} = E[X] = \int_{2}^{6} x\,\tfrac{1}{4}\,dx = \frac{x^2}{8}\Big|_2^6 = 4$$

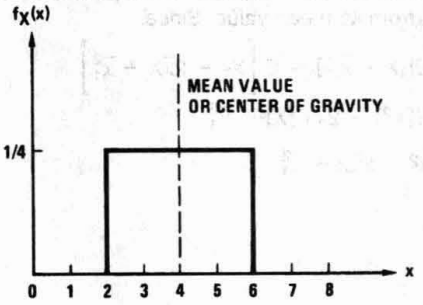

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FIGURE A.6.1

which can also be interpreted as the first moment or center of gravity of the density function $f_X(x)$. The above operation is analogous to the techniques in electrical engineering where the DC component of a time function is found by first integrating and then dividing the resultant area by the interval over which the integration was performed.

Generally speaking, the time averages of random variable functions of time are extremely important since essentially no statistical meaning can be drawn from a single random variable (defined as the value of a time function at a given single instant of time). Thus, the operation of finding the *mean value* by integrating over a specified range of possible values that a random variable may assume is referred to as *ensemble averaging*.

In the above example, $\bar{x}$ was described as the first moment m_1 or DC value. The mean-square value $\overline{x^2}$ or $E[X^2]$ is the second moment m_2 or the total average power, AC plus DC and in general the nth moment can be written

$$m_n = E[X^n] = \int_{-\infty}^{\infty} [h(x)]^2 f_X(x)\, dx \qquad \text{(A.6-4)}$$

Note that the first moment squared m_1^2, $\bar{x}^2$ or $E[X]^2$ is equivalent to the DC power through a 1Ω resistor and is *not* the same as the second moment m_2, $\overline{x^2}$ or $E[X]^2$ which, again, implies the total average power.

A discussion of central moments is next in store and is simply defined as the moments of the difference (deviation) between a random variable and its mean value. Letting $[h(x)]^n = (X - \bar{x})^n$, mathematically

$$\overline{(X - \bar{x})^n} = E[(X - \bar{x})^n] = \int_{-\infty}^{\infty} (X - \bar{x})^n f_X(x)\, dx \qquad \text{(A.6-5)}$$

For $n = 1$, the first central moment equals zero i.e., the AC voltage (current) minus the mean, average or DC voltage (current) equals zero. This essentially yields little information. The second central moment, however, is so important that it has been named the *variance* and is symbolized by σ^2. Hence,

$$\sigma^2 = E[(X - \bar{x})^2] = \int_{-\infty}^{\infty} (X - \bar{x})^2 f_X(x)\, dx \qquad \text{(A.6-6)}$$

Note that because of the squared term, values of X to either side of the mean $\bar{x}$ are equally significant in measuring variations or deviations away from $\bar{x}$ i.e., if $\bar{x} = 10$, $X_1 = 12$ and $X_2 = 8$ then $(12 - 10)^2 = 4$ and $(8 - 10)^2 = 4$ respectively. The variance therefore is the measure of the variability of $[h(x)]^2$ about its mean value $\bar{x}$ or the expected square deviation of X from its mean value. Since,

$$\sigma^2 = E[(X - \bar{x})^2] = E\left[X^2 - 2\bar{x}X + \bar{x}_1^2\right] \qquad \text{(A.6-7a)}$$

$$= E[X^2] - 2\bar{x}\,E[X] + \bar{x}_1^2 \qquad \text{(A.6-7b)}$$

$$= \overline{x^2} - 2\bar{x}\bar{x} + \bar{x}_1^2 \qquad \text{(A.6-7c)}$$

$$= \overline{x^2} - \bar{x}_1^2 \qquad \text{(A.6-7d)}$$

or

$$m_2 - m_1^2 \qquad \text{(A.6-7e)}$$

The analogy can be made that variance is essentially the average AC power of a function h(x), hence, the total average power, second moment m_2, minus the DC power, first moment squared m_1^2. The positive square root of the variance.

$$\sqrt{\sigma^2} = \sigma$$

is defined as the *standard deviation*. The mean indicates where a density is centered but gives no information about how spread out it is. This spread is measured by the standard deviation σ and is a measure of the spread of the density function about $\bar{x}$, i.e., the smaller σ the closer the values of X to the mean. In relation to electrical engineering the standard deviation is equal to the root-mean-square (rms) value of an AC voltage (current) in circuit.

A summary of the concepts covered in this section are listed in Table A.6.1.

A.7 FUNCTIONS OF TWO JOINTLY DISTRIBUTED RANDOM VARIABLES

The study of jointly distributed random variables can perhaps be clarified by considering the response of linear systems to random inputs. Relating the output of a system to its input is an example of analyzing two random variables from different random processes. If on the other hand an attempt is made to relate present or future values to its past values, this, in effect, is the study of random variables coming from the same process at different instances of time. In either case, specifying the relationship between the two random variables is established by initially developing a probability model for the joint occurrence of two random events. The following sections will be concerned with the development of these models.

A.8 JOINT CUMULATIVE DISTRIBUTION FUNCTION

The joint cumulative distribution function (cdf) is similar to the cdf of Section A.5 except now two random variables are considered.

$$F_{XY}(x,y) = \text{Prob}\,[X \le x, Y \le y] \qquad \text{(A.8-1)}$$

defines the joint cdf, $F_{XY}(x,y)$, of random variables X and Y. Equation (A.8-1) states that $F_{XY}(x, y)$ is the probability associated with the joint occurrence of the event that X is less than or equal to an allowed or conditional value x and the event that Y is less than or equal to an allowed or conditional value y.

TABLE A.6-1

Symbol	Name	Physical Interpretation
$\overline{X}$, E[X], m_1: $\int_{-\infty}^{\infty} x f_X(x)\,dx$	Expected Value, Mean Value, Statistical Average Value	• Finding the mean value of a random voltage (current) is equivalent to finding its DC component. • First moment; e.g., the first moment of a group of masses is just the average location of the masses or their center of gravity. • The range of the most probable values of x.
$E[X]^2$, $\overline{X}^2$, m_1^2		• DC power
$\overline{X^2}$, $E[X^2]$, m_2: $\int_{-\infty}^{\infty} x^2 f_X(x)\,dx$	Mean Square Value	• Interpreted as being equal to the time average of the square of a random voltage (current). In such cases the mean-square value is proportional to the total average power (AC plus DC) through a 1Ω resistor and its square root is equal to the rms or effective value of the random voltage (current). • Second moment; e.g., the moment of inertia of a mass or the turning moment of torque about the origin. • The mean-square value represents the spread of the curve about $\overline{x} = 0$
var[ ], σ^2, $(X - \overline{x})^2$, $E[(X - \overline{x})^2]$,) m_2: $\int_{-\infty}^{\infty} (X - \overline{x})^2 f_X(x)\,dx$	Variance	• Related to the average power (in a 1Ω resistor) of the AC components of a voltage (current) in power units. The square root of the variances is the rms voltage (current) again not reflecting the DC component. • Second movement; for example the moment of inertia of a mass or the turning moment of torque about the value $\overline{x}$. • Represents the spread of the curve about the value $\overline{x}$.
$\sqrt{\sigma^2}$,σ	Standard Deviation	• Effective rms AC voltage (current) in a circuit. • A measure of the spread of a distribution corresponding to the amount of uncertainty or error in a physical measurement or experiment. • Standard measure of deviation of X from its mean value $\overline{x}$.

$(\overline{X})^2$ is a result of smoothing the data and then squaring it and $\overline{(X^2)}$ results from squaring the data and then smoothing it.

A few properties of the joint cumulative distribution function are listed below.

1. $0 \le F_{XY}(x,y) \le 1$ $\quad -\infty < x < \infty$, $-\infty < y < \infty$

(since $F_{XY}(x,y) = \text{Prob}[X \le x, Y \le y]$ is a probability)

2. $F_{XY}(-\infty,y) = 0$
   $F_{XY}(x,-\infty) = 0$
   $F_{XY}(-\infty,-\infty) = 0$
3. $F_{XY}(+\infty,+\infty) = 0$
4. $F_{XY}(x,y)$ The probability of occurrence increases as either x or y, or both increase

A.9 JOINT PROBABILITY DENSITY FUNCTION

Similar to the single random variable probability density function (pdf) of sections A.4 and A.5, the joint probability density function $f_{XY}(x, y)$ is defined as the partial derivative of the joint cumulative distribution function $F_{XY}(x, y)$. More clearly,

$$f_{XY}(x,y) = \frac{d^2}{dx\,dy} F_{XY}(x,y) \qquad \text{(A.9-1)}$$

Recall that the pdf is a *density* function and must be integrated to find a probability. As an example, to find the probability that (X, Y) is within a rectangle of dimension ($x_1 \le X \le x_2$) and ($y_1 \le Y \le y_2$), the pdf of the joint or two-dimensional random variable must be integrated over both ranges as follows,

$$\text{Prob}[x_1 \le X \le x_2, y_1 \le Y \le y_2] = \int_{x_1}^{x_2}\int_{y_1}^{y_2} f_{XY}(x,y)\,dydx = 1 \qquad \text{(A.9-2)}$$

It is noted that the double integral of the joint pdf is in fact the cumulative distribution function

$$F_{XY}(x, y) = \int\int_{-\infty}^{\infty} f_{XY}(x, y)\,dxdy = 1 \qquad \text{(A.9-3)}$$

analogous to Section A.5. Again $f_{XY}(x, y)\,dxdy$ represents the probability that X and Y will jointly be found in the ranges

$$x \pm \frac{dx}{2} \text{ and } y \pm \frac{dy}{2},$$

respectively, where the joint density function $f_{XY}(x, y)$ has been normalized so that the volume under the curve is unity.

A few properties of the joint probability density functions are listed below.

1. $f_{XY}(x,y) > 0$ For all values of x and y or $-\infty < x < \infty$ and $-\infty < y < \infty$, respectively
2. $\int\int_{-\infty}^{\infty} f_{XY}(x,y)\,dxdy = 1$
3. $F_{XY}(x,y) = \int_{-\infty}^{y}\int_{-\infty}^{x} f_{XY}(x,y)\,dxdy$
4. $\text{Prob}[x_1 \le X \le x_2, y_1 \le Y \le y_2] = \int_{y_1}^{y^2}\int_{x_1}^{x^2} f_{XY}(x,y)\,dxdy$

A.10 STATISTICAL INDEPENDENCE

If the knowledge of one variable gives no information about the value of the other, the two random variables are said to be statistically independent. In terms of the joint pdf

$$f_{XY}(x,y) = f_X(x)\,f_Y(y) \qquad \text{(A.10-1)}$$

and

$$f_X(x)\,f_Y(y) = f_{XY}(x,y) \qquad \text{(A.10-2)}$$

imply statistical independence of the random variables X and Y. In the same respect the joint cdf

$$F_{XY}(x, y) = F_X(x)F_Y(y) \qquad \text{(A.10-3)}$$

and

$$F_X(x)F_Y(y) = F_{XY}(x, y) \qquad \text{(A.10-4)}$$

again implies this independence.

It is important to note that for the case of the expected value E[XY], statistical independence of random variables X and Y implies

$$E[XY] = E[X]\,E[Y] \qquad \text{(A.10-5)}$$

but, the converse is *not* true since random variables can be uncorrelated but not necessarily independent.

In summary

1. $F_{XY}(x,y) = F_X(x)\,F_Y(y)$ reversible
2. $f_{XY}(x,y) = f_X(x)\,f_Y(y)$ reversible
3. $E[XY] = E[X]\,E[Y]$ non-reversible

A.11 MARGINAL DISTRIBUTION AND MARGINAL DENSITY FUNCTIONS

When dealing with two or more random variables that are jointly distributed, the distribution of each random variable is called the *marginal distribution*. It can be shown that the marginal distribution defined in terms of a joint distribution can be manipulated to yield the distribution of each random variable considered by itself. Hence, the marginal distribution functions $F_X(x)$ and $F_Y(y)$ in terms of $F_{XY}(x, y)$ are

$$F_X(x) = F_{XY}(x, \infty) \qquad \text{(A.11-1)}$$

and

$$F_Y(y) = F_{XY}(\infty,y) \qquad \text{(A.11-2)}$$

respectively.

The marginal density functions $f_X(x)$ and $f_Y(x)$ in relation to the joint density $f_{XY}(x, y)$ is represented as

$$f_X(x) = \int_{-\infty}^{\infty} f_{XY}(x,y)\, dy \qquad \text{(A.11-3)}$$

and

$$f_Y(x) = \int_{-\infty}^{\infty} f_{XY}(x,y)\, dx \qquad \text{(A.11-4)}$$

respectively.

A.12 TERMINOLOGY

Before continuing into the following sections it is appropriate to provide a few definitions of the terminology used hereafter. Admittedly, the definitions presented are by no means complete but are adequate and essential to the continuity of the discussion.

Deterministic and Nondeterministic Random Processes: A random process for which its future values cannot be exactly predicted from the observed past values is said to be *nondeterministic*. A random process for which the future values of any sample function can be exactly predicted from a knowledge of all past values, however, is said to be a *deterministic* process.

Stationary and Nonstationary Random Processes: If the marginal and joint density functions of an event do not depend upon the choice of i.e., time origin, the process is said to be *stationary*. This implies that the mean values and moments of the process are constants and are not dependent upon the absolute value of time. If on the other hand the probability density functions do change with the choice of time origin, the process is defined *nonstationary*. For this case one or more of the mean values or moments are also time dependent. In the strictest sense, the stochastic process x(f) is stationary if its statistics are not affected by the shift in time origin i.e., the process x(f) and $x(t + \tau)$ have the same statistics for any τ.

Ergodic and Nonergodic Random Processes: If every member of the ensemble in a stationary random process exhibits the same statistical behavior that the entire ensemble has, it is possible to determine the process statistical behavior by examining only one typical sample function. This is defined as an *ergodic* process and its mean value and moments can be determined by time averages as well as by ensemble averages. Further ergodicity implies a stationary process and any process not possessing this property is *nonergodic*.

Mathematically speaking, any random process or, i.e., wave shape x(t) for which

$$\lim_{T \to \infty} \overline{x(t)} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} x(t)\, dt = E[x(t)]$$

holds true is said to be an ergodic process. This simply says that as the averaging time, T, is increased to the limit $T \to \infty$, time averages equal ensemble averages (the *expected value* of the function).

A.13 JOINT MOMENTS

In this section, the concept of joint statistics of two continuous dependent variables and a particular measure of this dependency will be discussed.

The joint moments m_{ij} of the two random variables X and Y are defined as

$$m_{ij} = E[X^i Y^j] = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} x^i y^j f_{XY}(x,y)\, dx\, dy \qquad \text{(A.13-1)}$$

where $i + j$ is the order of the moment.

The second moment represented as μ_{11} or σ_{XY} serves as a measure of the dependence of two random variables and is given a special name called the *covariance* of X and Y. Thus

$$\mu_{11} = \sigma_{XY} = E[(X - \bar{x})(Y - \bar{y})] = \qquad \text{(A.13-2)}$$

$$\int \int_{-\infty}^{\infty} (X - \bar{x})(Y - \bar{y})\, f_{XY}(x,y)\, dx\, dy$$

$$= E[XY] - E[X]\, E[Y] \qquad \text{(A.13-3)}$$

or

$$= m_{11} - \bar{x}\bar{y} \qquad \text{(A.13-4)}$$

If the two random variables are independent, their covariance function μ_{11} is equal to zero and m_{11}, the average of the product, becomes the product of the individual averages hence.

$$\mu_{11} = 0 \qquad \text{(A.13-5)}$$

implies

$$m_{11} = E[(X - \bar{x})(Y - \bar{y})] = E[X - \bar{x}]\, E[Y - \bar{y}] \qquad \text{(A.13-6)}$$

Note, however, the converse of this statement in general is not true but does have validity for two random variables possessing a joint (two dimensional) Gaussian distribution.

In some texts the name cross-covariance is used instead of covariance, regardless of the name used they both describe processes of two random variables each of which comes from a separate random source. If, however, the two random variables come from the same source it is instead called the autovariance or auto-covariance.

It is now appropriate to define a normalized quantity called the *correlation coefficient*, ρ, which serves as a numerical measure of the dependence between two random variables. This coefficient is the covariance normalized, namely

$$\rho = \frac{\text{covar}[X,Y]}{\sqrt{\text{var}[X]\, \text{var}[Y]}} = \frac{E\{[X - E[X]]\, [Y - E[Y]]\}}{\sqrt{\sigma_X^2\, \sigma_Y^2}} \qquad \text{(A.13-7)}$$

$$= \frac{\mu_{11}}{\sigma_X\, \sigma_Y} \qquad \text{(A.13-8)}$$

where ρ is a dimensionless quantity

$$-1 \leq \rho \leq 1$$

Values close to 1 show high correlation of i.e., two random waveforms and those close to -1 show high correlation of the same waveform except with opposite sign. Values near zero indicate low correlation.

A.14 CORRELATION FUNCTIONS

If x(t) is a sample function from a random process and the random variables

$$x_1 = x(t_1)$$
$$x_2 = x(t_2)$$

are from this process, then, the *autocorrelation* function $R(t_1, t_2)$ is the joint moment of the two random variables;

$$R_{xx}(t_1,t_2) = E[x(t_1)x(t_2)] \quad \text{(A.14-1)}$$

$$= \int\int_{-\infty}^{\infty} x_1 x_2 f_{x_1x_2}(x_1,x_2)\, d_{x_1}\, d_{x_2}$$

where the autocorrelation is a function of t_1 and t_2.

The auto-covariance of the process x(t) is the covariance of the random variables $x(t_1)$ $x(t_2)$

$$c_{xx}(t_1,t_2) = E\{[x(t_1) - \overline{x(t_1)}]\,[x(t_2) - \overline{x(t_2)}]\} \quad \text{(A.14-2)}$$

or rearranging equation (A.14-1)

$$c(t_1,t_2) = E\{[x(t_1) - \overline{x(t_1)}]\,[x(t_2) - \overline{x(t_2)}]\}$$
$$= E\{x(t_1)\,x(t_2) - x(t_1)\,\overline{x(t_2)} - \overline{x(t_1)}\,x(t_2) + \overline{x(t_1)x(t_2)}\}$$
$$= E\{x(t_1)\,x(t_2) - x(t_1)\,E[x(t_2)] - E[x(t_1)]\,x(t_2) + E[x(t_1)]\,E[x(t_2)]\}$$
$$= E[x(t_1)\,x(t_2)] - E[x(t_1)]\,E[x(t_2)] - E[x(t_1)]\,E[x(t_2)] + E[x(t_1)]\,E[x(t_2)]$$
$$= E[x(t_1)\,x(t_2)] - E[x(t_1)]\,E[x(t_2)] \quad \text{(A.14-3)}$$

or

$$= R(t_1, t_2) - E[x(t_1)]\,E[x(t_2)] \quad \text{(A.14-4)}$$

The autocorrelation function as defined in equation (A.14-1) is valid for both stationary and nonstationary processes. If x(t) is stationary then all its ensemble averages are independent of the time origin and accordingly

$$R_{xx}(t_1,t_2) = R_{xx}(t_1 + T, t_2 + T) \quad \text{(A.14-5a)}$$
$$= E[x(t_1 + T), x(t_2 + T)] \quad \text{(A.14-5b)}$$

Due to this time origin independence, T can be set equal to $-t_1$, $T = -t_1$, and substitution into equations (A.14-5a, b)

$$R_{xx}(t_1,t_2) = R_{xx}(0, t_2 - t_1) \quad \text{(A.14-6a)}$$
$$= E[x(0)\,x(t_2 - t_1)] \quad \text{(A.14-6b)}$$

imply that the expression is only dependent upon the time difference $t_2 - t_1$. Replacing the difference with $\tau = t_2 - t_1$ and suppressing the zero in the argument $R_{XX}(0, t_2 - t_1)$ yields

$$R_{xx}(\tau) = E[x(t_1)\,x(t_1 - \tau)] \quad \text{(A.14-7)}$$

Again since this is a stationary process it depends only on τ. The lack of dependence on the particular time, t_1, at which the ensemble was taken allows equation (A.14-7) to be written without the subscript, i.e.,

$$R_{xx}(\tau) = E[x(t)\,x(t + \tau)] \quad \text{(A.14-8)}$$

as it is found in many texts. This is the expression for the autocorrelation function of a stationary random process.

For the autocorrelation function of a nonstationary process where there is a dependence upon the particular time at which the ensemble average was taken as well as on the time difference between samples, the expression must be written with identifying subscripts, i.e., $R_{xx}(t_1, t_2)$ or $R_{xx}(t_1, \tau)$.

The time autocorrelation function can be defined next and has the form

$$R_{xx}(\tau) = \lim_{t \to \infty} \frac{1}{T}\int_{-T/2}^{T/2} x(t)\,x(t + \tau)\,dt \quad \text{(A.14-9)}$$

For the special case of an ergodic process (Ref. Appendix A.12) the two functions, equations (A.14-8) and (A.14-9), are equal

$$R_{xx}(\tau) = R_{xx}(\tau) \quad \text{(A.14-10)}$$

It is important to point out that if $\tau = 0$ in equation (A.14-7) the autocorrelation function

$$R_{xx}(0) = E[x(t_1)\,x(t_1)] \quad \text{(A.14-11)}$$

would equal the mean square value or total power (AC plus DC) of the process. Further, for values other than $\tau = 0$, $R_x(\tau)$ represents a measure of the similarity between its waveforms x(t) and $x(t + \tau)$.

In the same respect as the previous discussion, two random variables from two different jointly stationary random processes x(t) and y(t) have for the random variables

$$x_1 = x(t_1)$$
$$y_2 = y(t_1 + \tau)$$

the *crosscorrelation* function

$$R_{xy}(\tau) = E\{x(t_1)\, y(t_1+\tau)\] = \int\int_{-\infty}^{\infty} x_1 y_2\, f_{x_1y_2}(x_1,y_2)\, dx_1\, dy_2 \quad \text{(A.14-12)}$$

The crosscorrelation function is simply a measure of how much these two variables depend upon one another.

Since it was assumed that both random processes were jointly stationary, the crosscorrelation is thus only dependent upon the time difference τ and, therefore

$$R_{xy}(\tau) = R_{yx}(\tau) \quad \text{(A.14-13)}$$

where

$$y_1 = y(t_1)$$
$$x_2 = x(t_1 + \tau)$$

and

$$R_{yx}(\tau) = E\{y(t_1)\, x(t_1+\tau)\] = \int\int_{-\infty}^{\infty} y_1 x_2\, f_{y_1x_2}(y_1,x_2)\, dy_1\, dx_2 \quad \text{(A.14-14)}$$

The time crosscorrelation functions are defined as before by

$$R_{xy}(\tau) = \lim_{t\to\infty} \frac{1}{T}\int_{-T/2}^{T/2} x(t)\, y(t+\tau)\, dt \quad \text{(A.14-15)}$$

and

$$R_{yx}(\tau) = \lim_{t\to\infty} \frac{1}{T}\int_{-T/2}^{T/2} y(t)\, x(t+\tau)\, dt \quad \text{(A.14-16)}$$

and finally

$$R_{xy}(\tau) = R_{xy}(\tau) \quad \text{(A.14-17)}$$
$$R_{yx}(\tau) = R_{yx}(\tau) \quad \text{(A.14-18)}$$

for the case of jointly ergodic random processes.

APPENDIX B

B.0 INTERCHANGING TIME INTEGRATION AND EXPECTATIONS

If f(t) is a nonrandom time function and a(t) a sample function from a random process then,

$$E\left[\int_{t_1}^{t_2} a(t)\, f(t)\, dt\right] = \int_{t_1}^{t_2} E[a(t)]\, f(t)\, dt \quad \text{(B.0-1)}$$

This is true under the condition

a) $\int_{t_1}^{t_2} E[|a(t)|]\, |f(t)|\, dt < \infty$ (B.0-2)

b) a(t) is bounded by the interval t_1 to t_2. [t_1 and t_2 may be infinite and a(t) may be either stationary or nonstationary]

APPENDIX C

C.0 CONVOLUTION

This appendix defines convolution and presents a short proof without elaborate explanation. For complete definition of convolution refer to National Semiconductor Application Note AN-237.

For the *time convolution* if

$$f(t) \longleftrightarrow F(\omega) \quad \text{(C.0-1)}$$
$$x(t) \longleftrightarrow X(\omega) \quad \text{(C.0-2)}$$

then

$$y(t) = \int_{-\infty}^{\infty} x(\tau)\, f(t-\tau)\, d\tau \longleftrightarrow Y(\omega) = X(\omega) * F(\omega) \quad \text{(C.0-3)}$$

or

$$y(t) = x(t) * f(t) \longleftrightarrow Y(\omega) = X(\omega) * F(\omega) \quad \text{(C.0-4)}$$

proof:

Taking the Fourier transform, F[ ], of y(t)

$$F[y(t)] = Y(\omega) = \int_{-\infty}^{\infty}\left[\int_{-\infty}^{\infty} x(\tau)\, f(t-\tau)\, d\tau\right]\epsilon^{-j\omega t}\, dt \quad \text{(C.0-5)}$$

$$Y(\omega) = \int_{-\infty}^{\infty} x(\tau)\left[\int_{-\infty}^{\infty} f(t-\tau)^{-j\omega t}\, dt\right] d\tau \quad \text{(C.0-6)}$$

and letting $k = t - \tau$, then, $dk = dt$ and $t = k + \tau$.

Thus,

$$Y(\omega) = \int_{-\infty}^{\infty} x(\tau) \left[\int_{-\infty}^{\infty} f(k)\, \epsilon^{-j\omega(k+\tau)}\, dk \right] d\tau \quad \text{(C.0-7)}$$

$$= \int_{-\infty}^{\infty} x(\tau)\, \epsilon^{-j\omega\tau}\, d\tau \int_{-\infty}^{\infty} f(k)\, \epsilon^{-j\omega k}\, dk \quad \text{(C.0-8)}$$

$$Y(\omega) = X(\omega) \bullet F(\omega) \quad \text{(C.0-9)}$$

For the *frequency convolution* of

$$f(t) \longleftrightarrow F(\omega) \quad \text{(C.0-10)}$$

$$x(t) \longleftrightarrow X(\omega) \quad \text{(C.0-11)}$$

then

$$H(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\nu)\, X(\omega - \nu)\, d\nu \longleftrightarrow h(t) = f(t) \bullet x(t) \quad \text{(C.0-12)}$$

or

$$H(\omega) = \frac{1}{2\pi} F(\omega) * X(\omega) \longleftrightarrow h(t) = f(t) \bullet x(t) \quad \text{(C.0-13)}$$

proof:

Taking the inverse Fourier transform $F^{-1}[\ ]$ of equation (C.0-13)

$$h(t) = F^{-1}\left[\frac{X(\omega) * F(\omega)}{2\pi} \right] \quad \text{(C.0-14)}$$

$$= \frac{1}{2\pi} \int_{-\infty}^{\infty} \left[\frac{1}{2\pi} \int_{-\infty}^{\infty} F(\nu)(\omega - \nu)\, d\nu \right] \epsilon^{j\omega t}\, d\omega$$

$$= \left(\frac{1}{2\pi} \right)^2 \int_{-\infty}^{\infty} F(\nu) \int_{-\infty}^{\infty} X(\omega - \nu)\, \epsilon^{j\omega t}\, d\omega\, d\nu \quad \text{(C.0-15)}$$

and letting $g = \omega - \nu$, then $dg = d\omega$ and $\omega = g + \nu$.

Thus,

$$F^{-1} \frac{X(\omega) * F(\omega)}{2\pi} \quad \text{(C.0-16)}$$

$$h(t) = \left(\frac{1}{2\pi} \right)^2 \int_{-\infty}^{\infty} F(\nu) \int_{-\infty}^{\infty} X(g)\, \epsilon^{j(g+\nu)t}\, dg\, d\nu$$

$$h(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\nu)\, \epsilon^{j\nu t}\, d\nu \bullet \int_{-\infty}^{\infty} X(g)\, \epsilon^{jgt}\, dg \quad \text{(C.0-17)}$$

$$h(t) = f(t) \bullet x(t) \quad \text{(C.0-18)}$$

APPENDIX D

D.0 REFERENCES

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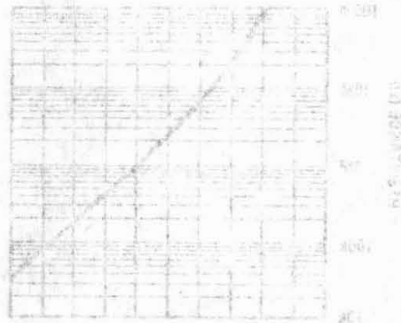

Circuitry for Inexpensive Relative Humidity Measurement

National Semiconductor
Application Note 256

Of all common environmental parameters, humidity is perhaps the least understood and most difficult to measure. The most common electronic humidity detection methods, albeit highly accurate, are not obvious and tend to be expensive and complex (See Box). Accurate humidity measurement is vital to a number of diverse areas, including food processing, paper and lumber production, pollution monitoring and chemical manufacturing. Despite these and other applications, little design oriented material has appeared on circuitry to measure humidity. This is primarily due to the small number of transducers available and a generally accepted notion that they are difficult and expensive to signal condition.

Although not as accurate as other methods, the sensor described by the response curve *(Figure 1)* is inexpensive and provides a direct readout of relative humidity. The curve reveals a close exponential relationship between the sensor and relative humidity spanning almost 4 decades of resistance. Linearization of this curve may be accomplished by taking the logarithm of the resistance value and utilizing breakpoint approximation techniques to minimize the residual non-linearities. A further consideration in signal conditioning is that the manufacturer specifies that no significant DC current component may pass through the sensor. This device must be excited with an unbiased AC waveform to preclude detrimental electrochemical migration. In addition, it has a 0.36 RH unit/°C positive temperature coefficient. The sensor is a chemically treated styrene copolymer which has a surface layer whose resistivity varies with relative humidity. Because the humidity sensitive portion of the sensor is at its surface, time response is reasonably rapid and is on the order of seconds.

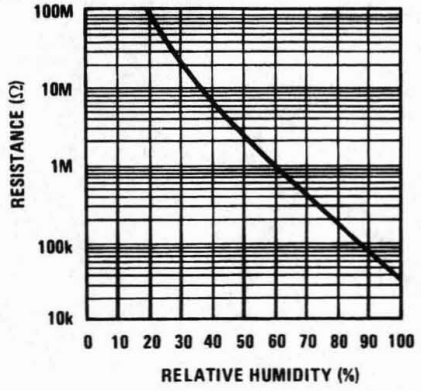

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FIGURE 1. Phys-Chemical Research Corp. Model PCRC-55 Humidity Sensor

A block diagram of the concept chosen to instrument the sensor appears in *Figure 2*. An amplitude stabilized square wave which is symmetrical about zero volts is used to provide a precision alternating current through the sensor, satisfying the requirement for a zero DC component drive. The current through the sensor is fed into a current sensitive (e.g. the input is at virtual ground) logarithmic amplifier, which linearizes sensor response. The output of the logarithmic amplifier is scaled, rectified and filtered to provide a DC output which represents relative humidity. Residual non-linearity due to the sensors non-logarithmic response below RH = 40% is compensated by breakpoint techniques in this final stage.

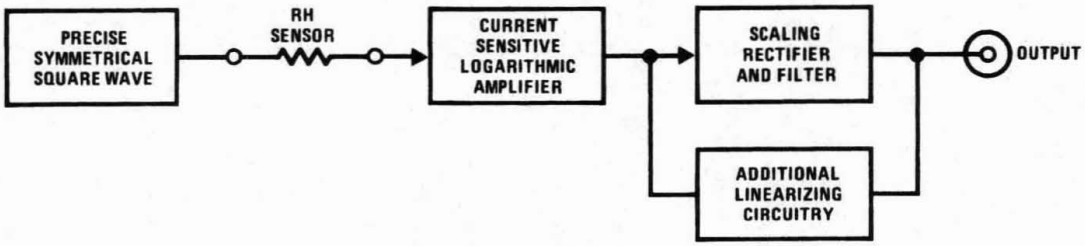

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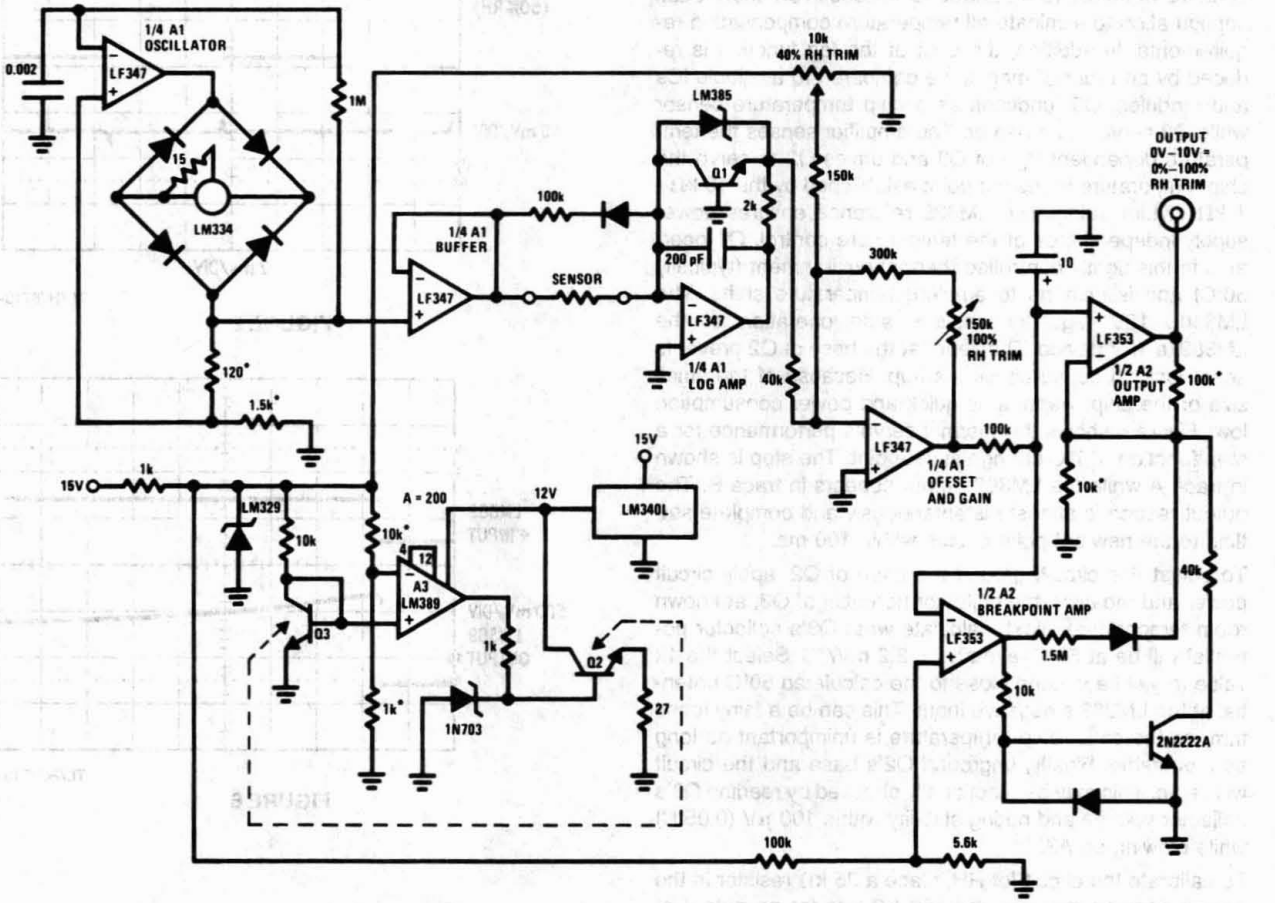
FIGURE 2

The detailed circuitry appears in *Figure 3*. It is worth noting that the entire funtion described in *Figure 2* requires a small number of inexpensive ICs. This is accomplished by novel circuitry approaches, especially in the design of the logarithmic amplifier. The stabilized symmetrical square wave is generated by A1, ¼ of an LF347 quad amplifier. A1 is set up in a positive feedback configuration, causing it to oscillate. The output of A1 is current limited and clamped to ground for either polarity output by the LM334 current source diode bridge combination. The LM334 is programmed by the 15Ω resistor to current limit at about 5 mA. This forces the voltage across the 120Ω–1.5 kΩ resistor string to stabilize at about ±8V. Each time A1's output changes state the charging current into the 0.002 μF capacitor reverses, causing the amplifier to switch again when the capacitor reaches a threshold established by the 120Ω–1.5 kΩ divider (waveforms, *Figure 4*). This circuit's output is buffered by the A1 follower. The amplitude stability of the waveform is dependent upon the +0.33%/°C temperature coefficient of the LM334. This T.C. has been intentionally designed into the LM334 so that it may be used in temperature sensing and compensation applications. Here, the negative 0.3%/°C temperature dependence of the humidity sensor is reduced by more than an order of magnitude by the LM334's T.C. and thermally induced inaccuracy in the humidity sensor's response drops out as an error term. In practice, the LM334 should be mounted in proximity to the humidity sensor. The residual −0.03%/°C temperature coefficient is negligibly small compared to the sensors ±1% accuracy specification.

The output square wave is used to drive current through the sensor and into the summing junction of another ¼ of A1, which is connected as a logarithmic amplifier. On negative cycles of the input waveform the transistor (Q1) in the feedback loop provides logarithmic response, due to the well known relationship between V_{BE} and collector current in transistors. During positive excursions of the input waveform the diode provides feedback to the amplifier's summing junction. In this manner the summing junction always remains at virtual ground while the input current is expressed in logarithmic form by the negative going square wave at the transistor emitter. Since the summing junction is always at ground potential the sensor sees the required symmetrical drive (waveforms, *Figure 5*).



LF347 and LF353 run on ±15V supply.
Q1, Q2, Q3 are on LM389 chip.
* = 1% Metal Film
▶| = 1N4148

Sensor = PCRC-55 - Phys-Chemical Research Corporation
A1 = LF347
A2 = LF353

TL/H/8713–3

FIGURE 3

The output of this stage is fed to another ¼ of A1. This amplifier is used to sum in the 40% RH trim and provide adjustable gain to set the 100% RH trim. The output is filtered to DC and routed to one half of A2, an LF353, which unloads the filter and provides additional gain and the final output.

The other ½ of A2 is used to compensate the sensor departure from logarithmic conformity below 40% RH *(Figure 1)*. This is accomplished by changing the gain of the output amplifier for RH readings below 40%. The input to the output amplifier is sensed by the breakpoint amplifier. When this input goes below RH = 40% (about 0.36V at the output amplifiers "+" terminal) the breakpoint amplifier swings positive. This turns on the 2N2222A, causing the required gain change to occur at the output amplifier. For RH values above 40% the transistor is off and the circuits linearizing function is determined solely by the logarithmic amplifier.

In logarithmic configurations such as this, Q1's DC operating point will vary wildly with temperature and the circuit normally requires careful attention to temperature compensation, resulting in the expense associated with logarithmic amplifiers. Here, A3, an LM389 audio amplifier IC which also contains three discrete transistors, is used in an unorthodox configuration to eliminate all temperature compensation requirements. In addition, the cost of the log function is reduced by an order of magnitude compared to available ICs and modules. Q3 functions as a chip temperature sensor while Q2 serves as a heater. The amplifier senses the temperature dependent V_{BE} of Q3 and drives Q2 to servo the chip temperature to the set-point established by the 10 kΩ–1 kΩ divider string. The LM329 reference ensures power supply independence of the temperature control. Q1 operates in this tightly controlled thermal environment (typically 50°C) and is immune to ambient temperature shifts. The LM340L 12V regulator ensures safe operation of the LM389, a 12V device. The zener at the base of Q2 prevents servo lock-up during circuit start-up. Because of the small size of the chip, warm-up is quick and power consumption low. *Figure 6* shows the thermal servo's performance for a step function of 7°C change in set-point. The step is shown in trace A while the LM389 output appears in trace B. The output responds almost instantaneously and complete settling to the new set-point occurs within 100 ms.

To adjust this circuit, ground the base of Q2, apply circuit power and measure the collector potential of Q3, at known room temperature. Next, calculate what Q3's collector potential will be at 50°C, allowing −2.2 mV/°C. Select the 1k value to yield a voltage close to the calculated 50°C potential at the LM389's negative input. This can be a fairly loose trim, as the exact chip temperature is unimportant so long as it is stable. Finally, unground Q2's base and the circuit will servo. This may be functionally checked by reading Q3's collector voltage and noting stability within 100 μV (0.05°C) while blowing on A3.

To calibrate the circuit for RH, place a 35 kΩ resistor in the sensor position and trim the 150 kΩ pot for an output of 10V. Next, substitute an 8 MΩ resistor for the sensor and trim the 10k potentiometer for an output of 4V. Repeat this procedure until the adjustments do not interfere with each other. Finally, substitute a 60 MΩ resistor for the sensor and select the nominal 40 kΩ value in the breakpoint amplifier for a reading of RH = 24%. It may be necessary to select the 1.5 MΩ value to minimize "hop" at the circuit output when the breakpoint is activated. The circuit is now calibrated and will read ambient relative humidity when the PCRC-55 sensor is connected.

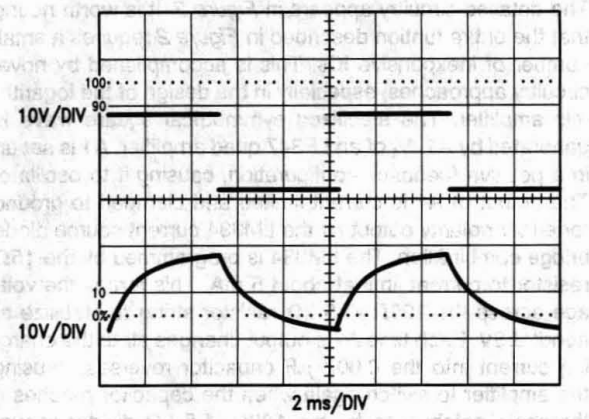


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FIGURE 4

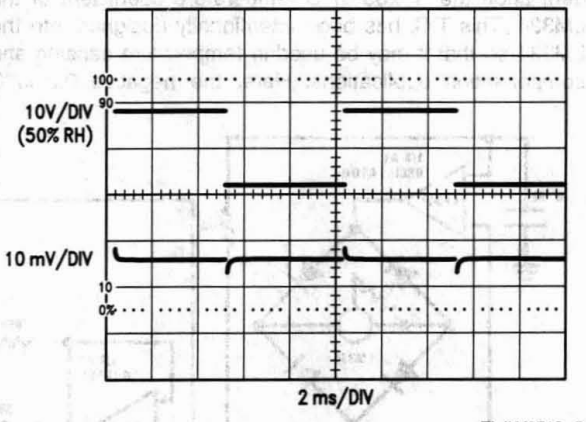

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FIGURE 5

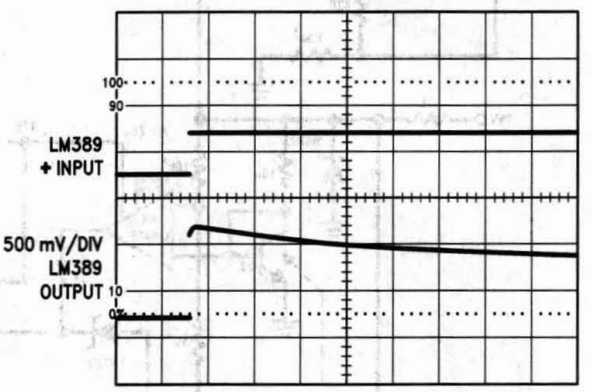

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FIGURE 6

HUMIDITY

Humidity is simply water gas. In air the humidity may vary from zero percent for 90°F dry air to as much as 4.5 percent for heavily water laden air at 90°F. The amount of water air will hold is dependent upon temperature. *Relative* humidity is an expression denoting the ratio of water vapor in the air to the amount possible in saturated air at the same temperature.

Some of the more common ways of expressing humidity related information include wet bulb temperature, dew point and frost point. Wet bulb temperature refers to the minimum temperature reached by a wetted thermometer bulb in a stream of air. The dew point is the point at which water saturation occurs in air. It is evidenced by water condensation. When temperatures below 0°C are required to produce this phenomenon it is called the frost point.

Other measurements and ways of expressing humidity exist and are useful in a variety of applications. For additional information consult the bibliography.

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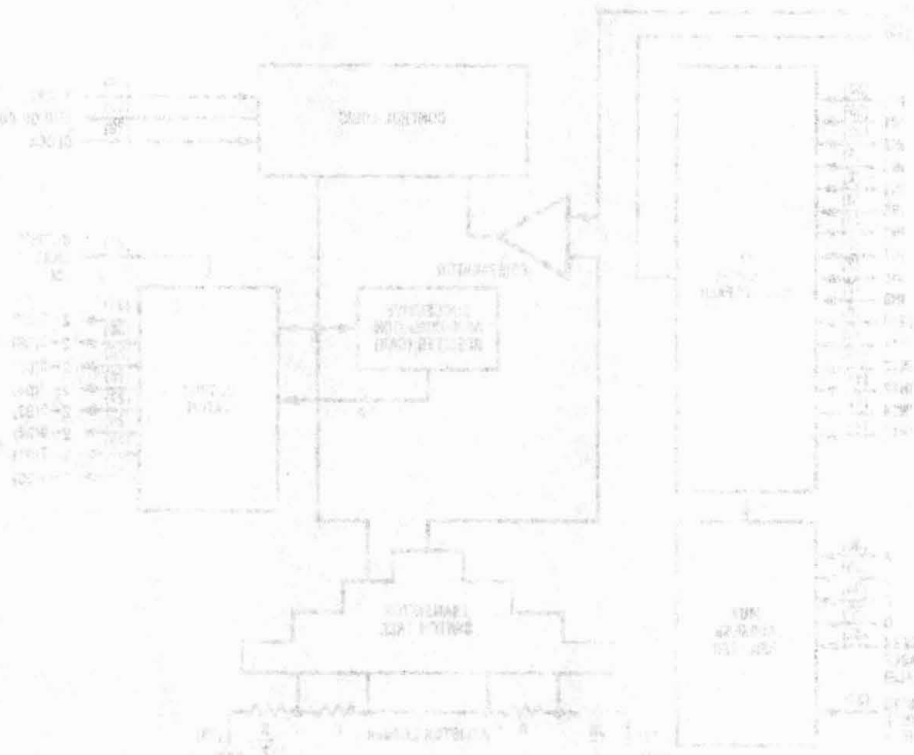

Data Acquisition Using the ADC0816 and ADC0817 8-Bit A/D Converter with On-Chip 16 Channel Multiplexer

National Semiconductor
Application Note 258
Larry Wakeman

I. Introduction

The ADC0816 and ADC0817, CMOS 16-Channel Data Acquisition devices are selectable multi-input 8-bit A/D converters. In addition to a standard 8-bit successive approximation type A/D converter, these devices contain a 16 channel analog multiplexer with 4-bit latched address inputs. They include much of the circuitry required to build an 8-bit accurate, medium through-put data acquisition system.

These two converters are similar to the ADC0808/ADC0809 A/D converters except that the ADC0816/ADC0817 have 16 analog inputs instead of 8, and the multiplexer output and the A/D comparator input are externally available. (The ADC0808/ADC0809 connect these internally.) This feature is useful when connecting signal processing circuitry to the A/D. Also the ADC0816/ADC0817 have an expansion control pin to allow addition of more multiplexers, hence more input channels.

The ADC0816 is identical to the ADC0817 except for accuracy. The ADC0816 is the more accurate part, having a total unadjusted error of $\pm\frac{1}{2}$ LSB. The ADC0817 has a total unadjusted error ± 1 LSB. In many applications where a slightly lower accuracy is tolerable, the ADC0817 represents a more economical solution.

II. Functional Description

The ADC0816/ADC0817 can be subdivided into two major functional blocks; a multiplexer/latch and an A/D converter, *Figure 1*. The multiplexer/latch is composed of a 16 channel multiplexer, a 4 bit channel select register, and some channel select decoding circuitry.

The channel select address is loaded on the positive transition of the Address Latch Enable (ALE) input. *Figure 2*

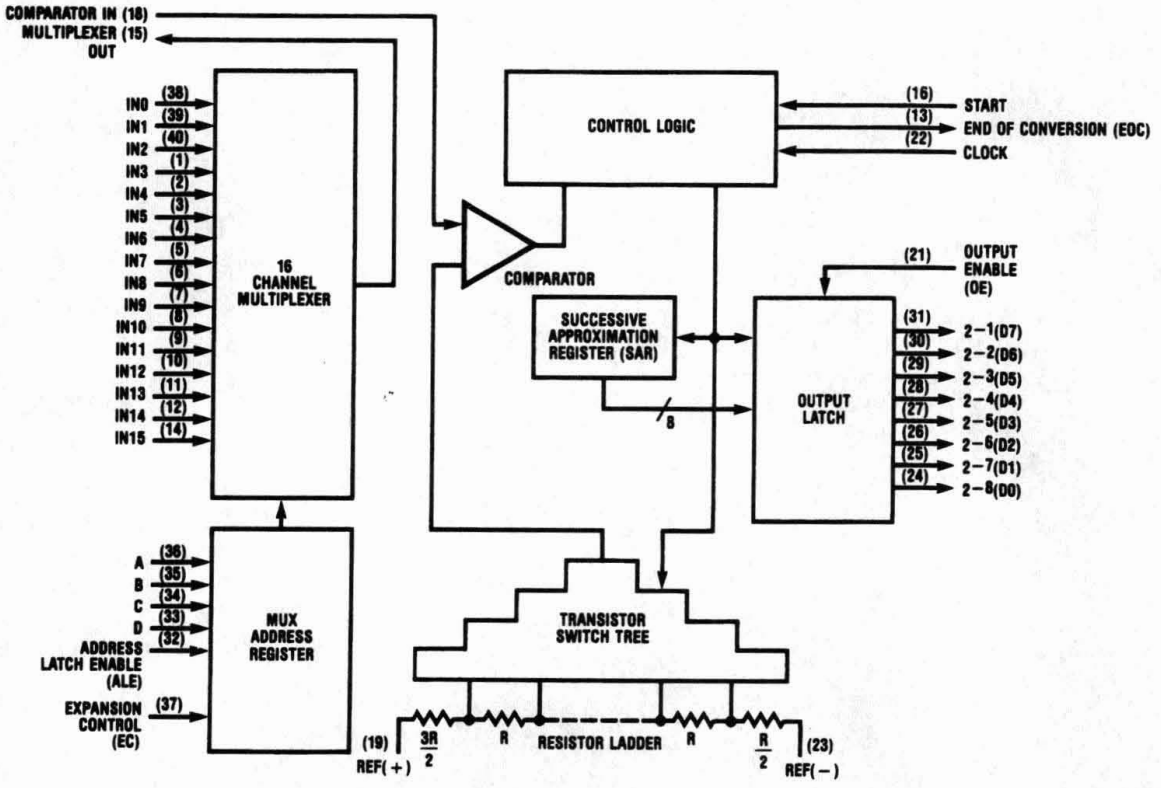

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FIGURE 1. ADC0816/ADC0817 Functional Block Diagram

shows this addressing scheme. A multiplexer enable pin called Expansion Control (EC) is also provided. Taking this pin low will disable the on chip multiplexer, allowing other multiplexers to be used, thus expanding the number of inputs.

Address				Expansion	Selected
D	C	B	A	Control	Channel
0	0	0	0	1	IN0
0	0	0	1	1	IN1
0	0	1	0	1	IN2
0	0	1	1	1	IN3
0	1	0	0	1	IN4
0	1	0	1	1	IN5
0	1	1	0	1	IN6
0	1	1	1	1	IN7
1	0	0	0	1	IN8
1	0	0	1	1	IN9
1	0	1	0	1	IN10
1	0	1	1	1	IN11
1	1	0	0	1	IN12
1	1	0	1	1	IN13
1	1	1	0	1	IN14
1	1	1	1	1	IN15
X	X	X	X	0	NONE

FIGURE 2. Analog Input Selection Table

The output of the multiplexer usually feeds the input of the second major functional block, the A/D converter. This converter is a successive approximation type converter that is composed of a comparator, 256R type resistor ladder, successive approximation register (SAR), control logic, and output data latch.

Under normal operation the control logic of the A/D will first detect a positive going pulse on the START input. On the rising edge of this pulse the internal registers are cleared, and will remain clear as long as START is high. When the START input goes low, the conversion is initiated. The control logic will cycle to the beginning of the next approximation cycle at which time End of Conversion goes low and the conversion is started. During a conversion, the control logic will select a tap on the resistor ladder, and route the signal through a transistor switch tree to the input of the comparator. The comparator will decide whether this tap voltage is higher or lower than the input signal and indicate this to the control logic. The control logic then decides which tap is to be selected next. Meanwhile, the SAR maintains a record of the conversion's progress. This algorithm takes 8 clock periods per approximation and requires 8 approximations to convert 8 bits. Thus 64 clock periods are required for a complete conversion.

Once the entire conversion is completed the data in the SAR is loaded into the output register. This is a TRI-STATE® register which requires that its outputs be enabled by rising the Output Enable (OE or TRI-STATE) input. The data can then be read by the controlling logic.

During operation, the EOC output must be monitored to determine whether the device is actively converting or is ready to output data. Once the channel address is loaded, a positive going pulse on START will start the conversion and cause EOC to fall. When EOC goes high again the data is ready to be read, which, as was previously stated, is accomplished by raising the OE input. The data can be read any time prior to one clock period before the completion of the *next* conversion. The ADC0816/ADC0817 timing is shown in *Figure 3*. (See data sheet for exact specifications.)

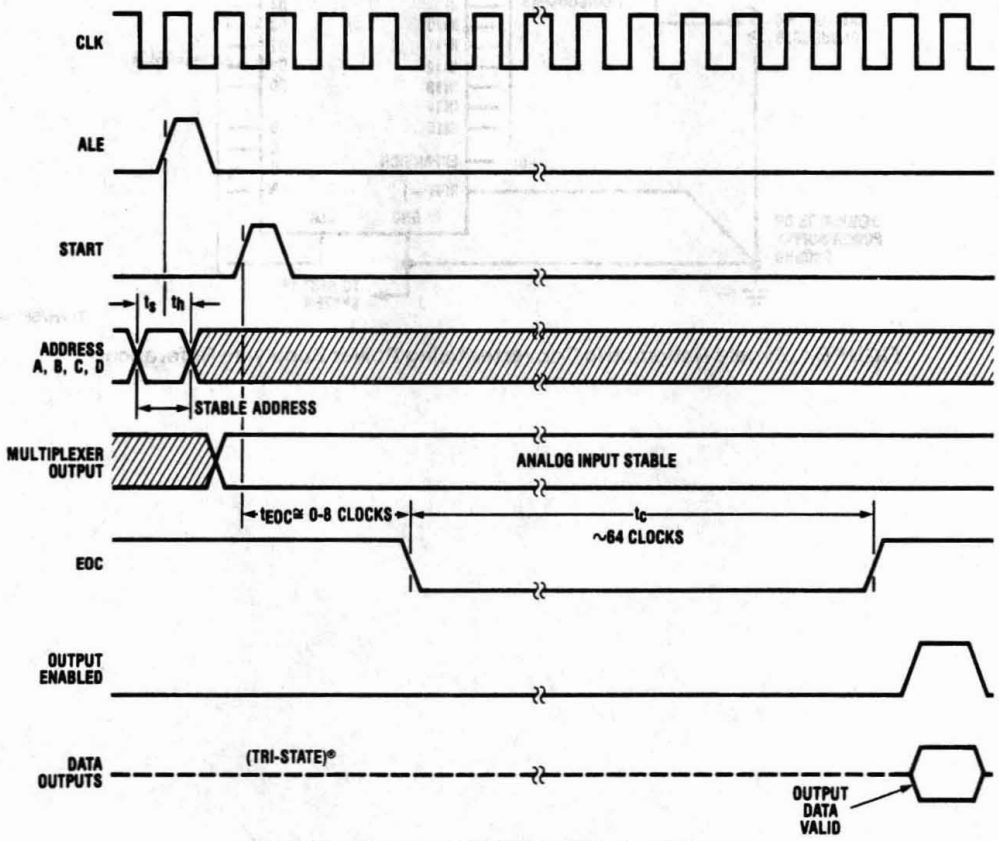

FIGURE 3. ADC0816/ADC0817 Timing Diagram

III. Analog Input Designs

A. Ratiometric Conversion

The external availability of both ends of the 256R resistor ladder makes this converter ideally suited to use with ratiometric transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full scale value. In other words, the actual value of the transducers output is of no great importance, but the ratio of this output to the full scale reference is valuable. For example, the potentiometric transducers of *Figure 4* have this feature.

The prime advantage of these transducers is that an accurate reference is not required. However, the reference should be noise free because voltage spikes during a conversion could cause inaccurate results.

Perhaps the simplest method to obtain a reference would be to use a voltage already present in the system, the power supply. As shown in *Figure 4* the 5V supply can be easily connected as the reference, but care must be taken to reduce power supply noise. The supply lines should be well bypassed with filter capacitors and it is recommended that separate PC board traces be used to route the 5V and ground to the reference inputs and to the supply pins.

B. Absolute Conversion

Absolute conversion refers to the use of transducers whose output value is not related to some other voltage. The "absolute" value of the transducer's output voltage is very important. This implies that the reference must be very accurately known to be able to accurately determine the value of the transducers output. *Figure 5* shows a typical grounded reference connection using the LM336-5, 5V reference. Note that ratiometric transducers can also be used in this application along with absolute transducers.

In most of the following applications either absolute or ratiometric transducers can be used. The only difference being that when absolute transducers are employed, more accurate references should be used.

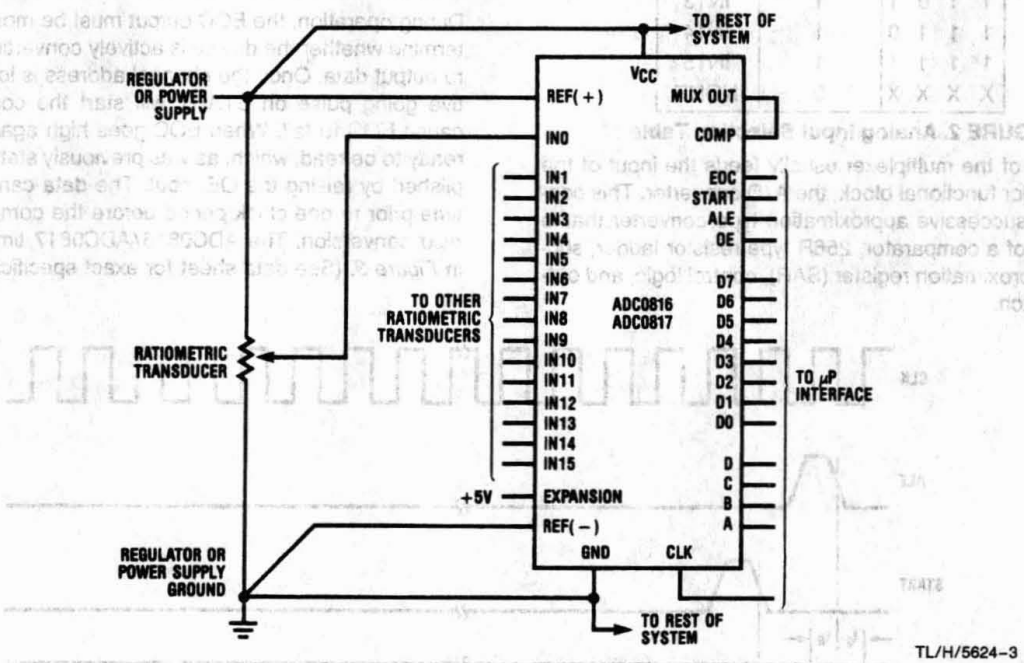

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FIGURE 4. Simple Ratiometric Converter Using Power Supply as Reference

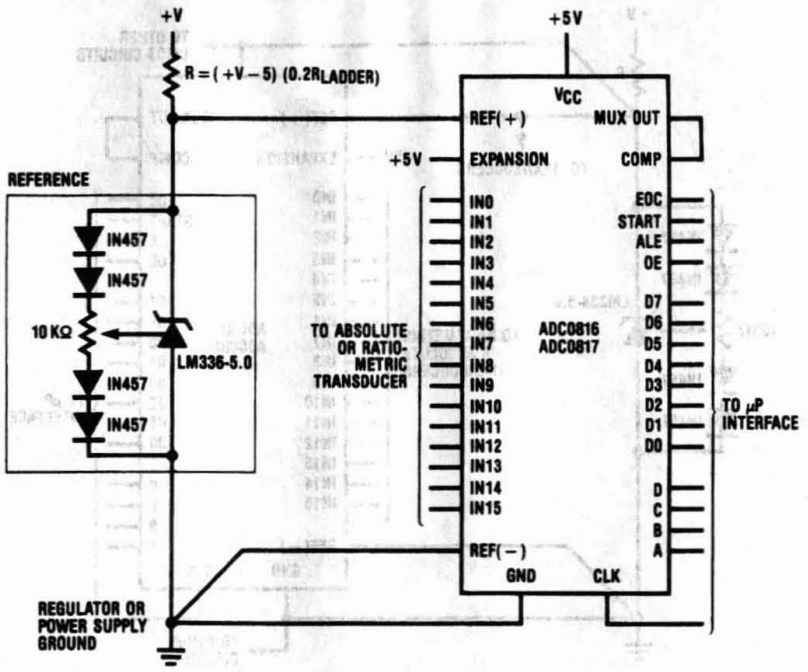

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FIGURE 5. Simple Absolute Converter Using LM336-5.0 Converter

C. Reference Manipulation

In some small systems (particularly CMOS systems) where a reference is required, one can use the reference as a supply as shown in *Figure 6*. In this case the LM336-5 is used to generate the 5V reference and also the 5V supply. An unregulated supply greater than 5V is required to allow the reference to operate. The series resistor, R, is chosen such that the maximum current needed by the system is supplied while keeping the LM336-5 in regulation. The value of this resistor is simply:

$$R = \frac{V_S - V_{REF}}{I_{LAD} + I_{TR} + I_P + I_R}$$

where V_S = unregulated supply voltage; V_{REF} = reference voltage; $I_{LAD} = V_{REF}/1\ k\Omega$, resistor ladder current; I_{TR} = transducer currents; I_p = system power supply requirements; and I_R = minimum reference current.

Figure 7 shows a simple method of buffering the references to provide higher current capabilities. This eliminates the I_p term in the above equation. In *Figures 5, 6*, and *7*, it is advisable to add some supply bypass capacitors to reduce noise, typically 0.1 μF.

D. Reference Voltage Variation

In some cases it is possible to eliminate the need for gain adjustments on the analog input signals by varying the Ref(+) and Ref(−) voltages to achieve various full scale ranges. The reference voltage can be varied from 5V to about 0.5 volts with the one restriction that $[V_{Ref(+)} - V_{Ref(-)}]/2 = (V_{CC}\text{-GND})/2 \pm 0.1$ volts. In other words, the center of the reference voltage must be within ±0.1V of mid-supply. The reason for this is that the reference ladder is taped by an n or p-channel MOSFET switch tree. Offsetting the voltage at the center of the switch tree from $V_{CC}/2$ will cause the transistors to incorrectly turn off, resulting in inaccurate and erratic conversions. However, if properly applied, this method can reduce parts counts as well as eliminate extra power supplies for the input buffers.

Figure 8 shows a simple supply centered reference where R1 and R2 offset Ref(+) and Ref(−) from V_{CC} and Ground. An LM336, 2.5V reference is shown here, but any reference between 0.5V and 5V can be used. For odd reference values the simple op amp scheme shown in *Figure 9* can be used. Single power supply op amps such as the LM324's or LM10's would work well. R1, R2, and R3 form a resistor divider in which R1 and R3 center the reference at $V_{CC}/2$ and R2 can be varied to obtain the proper reference magnitude.

E. Analog Channel Expansion

The ADC0816/ADC0817 have an expansion control (EC) pin which is actually a multiplexer enable. When this signal is low, all the switches are inhibited so that another signal can be applied to the comparator input. Additional channels can be implemented very simply, as shown in *Figure 10*. This design has expanded the number of channels from 16 to 32. To address the channels, 5 address lines are required. The lower 4 bits are directly applied to the A/D's A, B, C, and D inputs. All 5 bits are also applied to an MM74C174 Hex "D" flip-flop which is used as an address latch for the two CD4051's. The 1Q, 2Q, and 3Q outputs of the MM74C174 feed the CD4051 address inputs 4Q and 5Q are gated to form enable signals for each CD4051. 5Q is also routed to the EC input to properly enable the A/D's multiplexer.

The CD4051s are used with a 5V supply, so their specifications are very similar to the ADC0816/ADC0817 multiplexer. Thus, anything that can be done with the ADC0816/ADC0817 multiplexer can be done with the CD4051's. This includes making use of the previously discussed input designs as well as others.

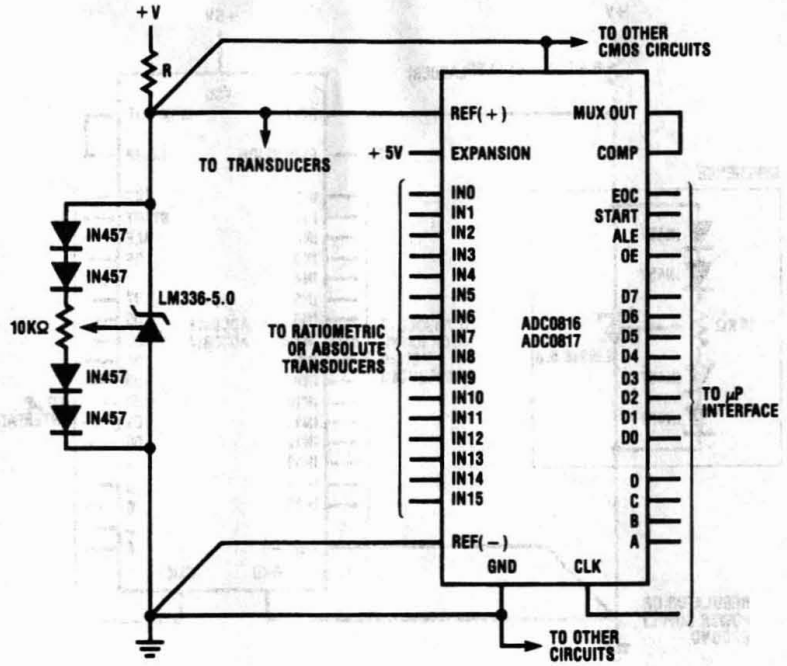

FIGURE 6. Reference Used as Power Supply

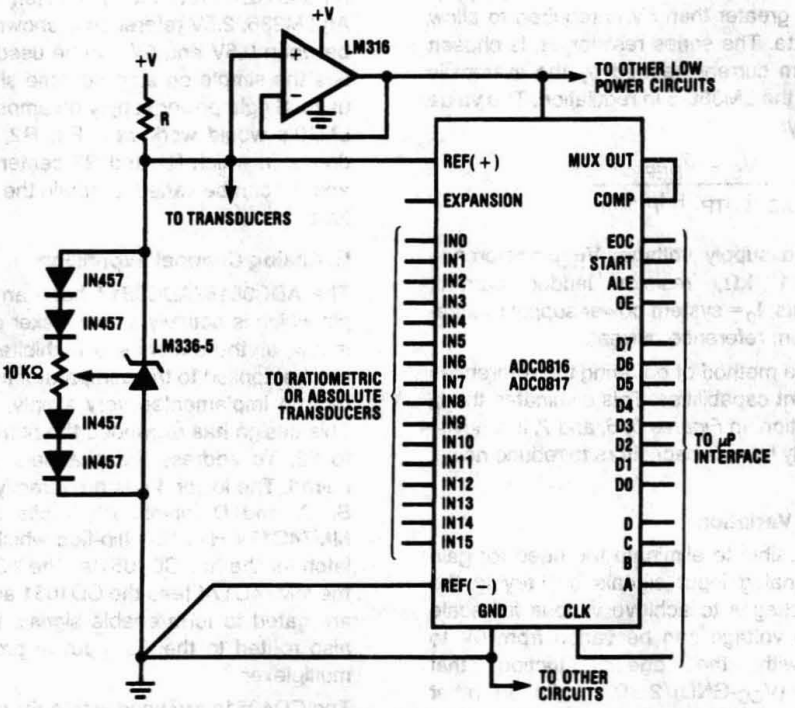

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FIGURE 7. Buffered Reference Used as Power Supply

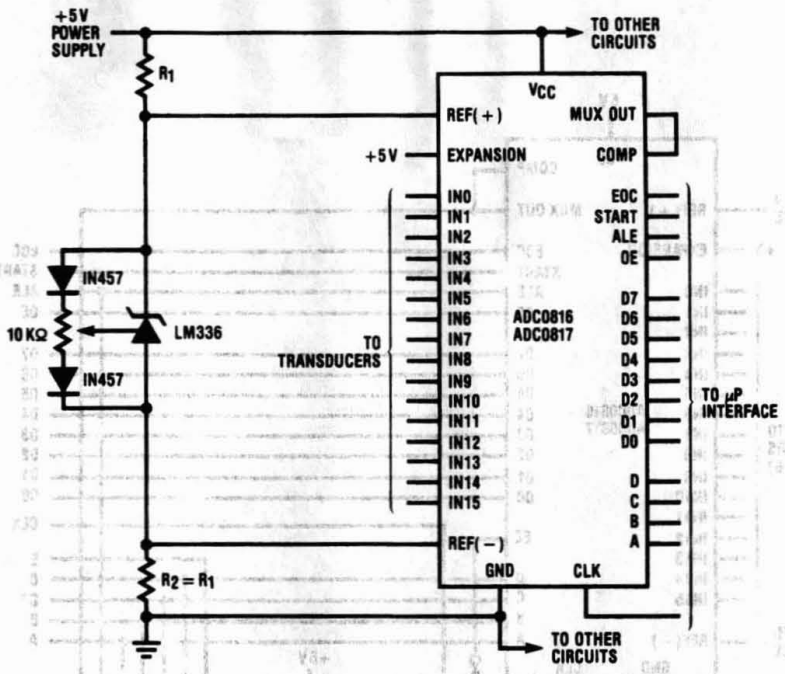

FIGURE 8. Supply Centered Reference Using LM336 2.5V Reference

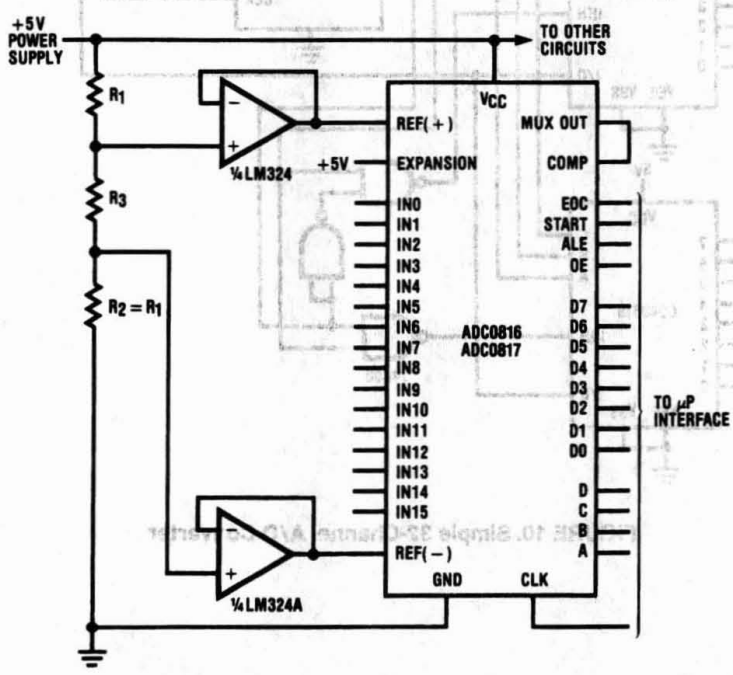

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FIGURE 9. Supply-Centered Reference Using Buffered Resistor Divider

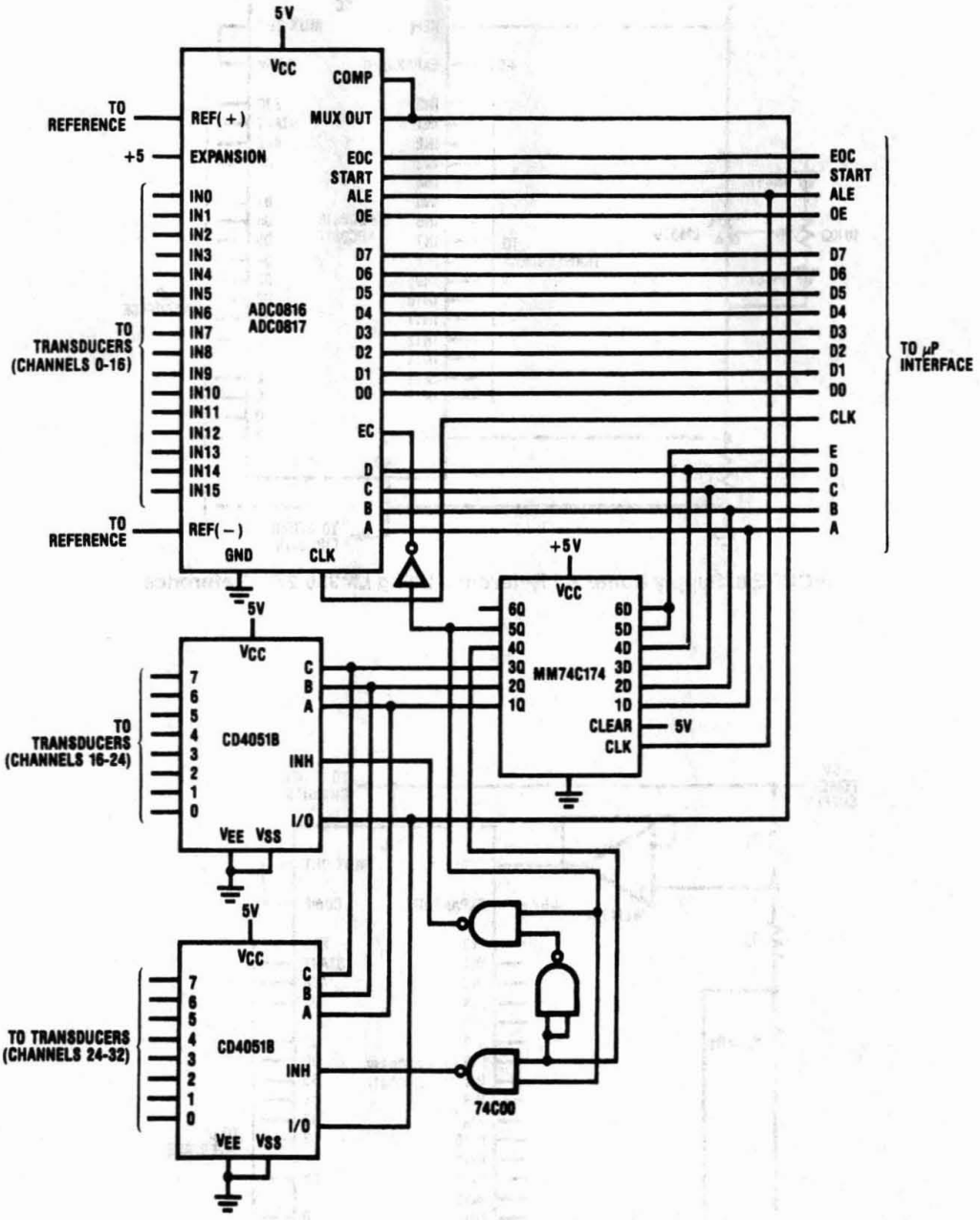

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FIGURE 10. Simple 32-Channel A/D Converter

F. Differential Analog Inputs

An easy, and sometimes overlooked method for implementing a differential input scheme is shown in *Figure 11*. This approach actually implements the differential in software. All 16 channels are paired into positive and negative inputs. Then the controlling logic or microprocessor will convert each channel of a differential pair, load each result, and then subtract the two results. This method requires two single ended conversions to do one differential conversion, hence the effective differential conversion time is twice that of a single channel or a little over 200 μS (Ck=640 kHz). The differential inputs should be stable throughout both of the conversions to produce accurate results.

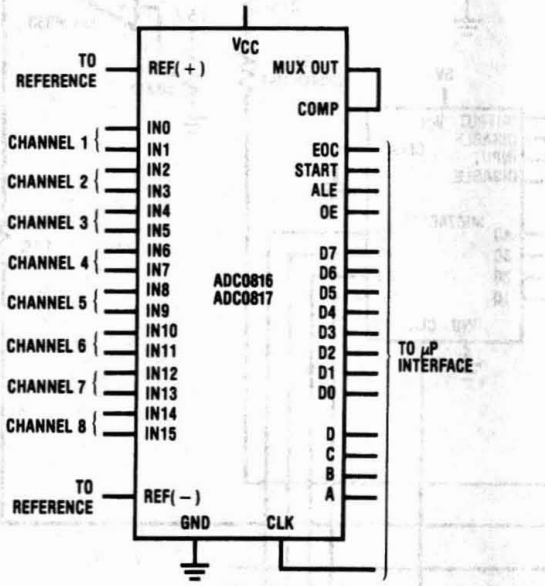

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FIGURE 11. Simple 8-Differential Channel Converter

A 16 channel differential system can be realized by modifying *Figure 10*. This is accomplished by changing the CD4051's addressing and adding a differential amplifier in between the multiplexer outputs and the comparator input. The select logic for the CD4051's has been modified to enable the switches to be selected in parallel with the ADC0816/ADC0817. The outputs of the three multiplexers are connected to a differential amplifier, composed of 2 inverting amplifiers with gain and offset trimmers. A dual op amp configuration of inverting amplifiers can more easily be trimmed and has less stringent feed-back resistor matching requirements, as compared to a single op amp design. The transfer equation for the dual op amp amplifier shown in *Figure 12* is:

$$V_o = \left[\frac{R_2R_5}{R_1R_3}\right] V_1 - \left[\frac{R_5}{R_4}\right] V_2$$

Propagation delay through the op amps should be considered to provide sufficient time between the analog switch selection and start conversion to allow the analog signal at the comparator input to settle. Using the LF353 op amp, this delay should be about 5 μs.

G. Input Signal Buffering

There are three basic ranges of input signal levels that can occur when interfacing the ADC0816/ADC0817 to the "real world". These are: a) signals which exceed V_{CC} and/or go below ground; b) signals whose input ranges are less than V_{CC} and Ground, but are different than the reference range; c) and signals that have an input range that is equal to the reference range. Each of these situations require different buffering.

The last situation, case "c" is usually trivial. No buffering is required unless the source impedance of the input signal is very high. If this is the case a buffer may be added between the multiplexer output and comparator input pins. If a high input impedance op amp is used, the input leakage looking from the multiplexer input can be greatly reduced. This circuit is shown in *Figure 13*. Using a buffer like this eliminates the necessity for large capacitors on the multiplexer inputs (explained later), but these buffers usually require two supplies and can contribute their own conversion errors.

If the input signal is within the supply, but the reference cannot be manipulated to conform to the full input range, the unity gain buffer of *Figure 13* can be replaced by another op amp as shown in the *Figure 13* inset. This type of amplifier will provide gain and/or offset control to create a full scale range equal to the reference.

The third case, c, where the input range exceeds V_{CC} and/or goes below ground, the input signals must be level shifted before they can go to the multiplexer with the only exception being when the magnitude of the input voltage range is within 5V, but outside the 0-5V supply range. In this case the supply for the entire chip could be shifted to the analog input range, and the digital signals level shifted to the system's 5V supply.

A typical example would be bipolar inputs from −2.5V to +2.5. If the ADC0816/ADC0817 have their supply and reference derived as shown in *Figure 14*, then the ±2.5V logic outputs need only to be level shifted to 0 and 5V logic levels, *Figure 15*.

H. Digital Data Acquisition

The ADC0816/ADC0817 make good analog data acquisition subsystems, but there are many instances where these converters are good digital data acquisition systems as well. If a system has unused channels, digital inputs can be connected to these channels instead of being separately buffered into the system. In the case of a microprocessor system this could eliminate an I/O port and associated logic. The speed at which this input is accessed is one conversion cycle, but many times this will be fast enough. These inputs can be used as input switches, power supply indicator devices, or other system status flags. The microprocessor converts the digital input channel and reads it. Software then decides whether the input is high enough or low enough to cause a particular action.

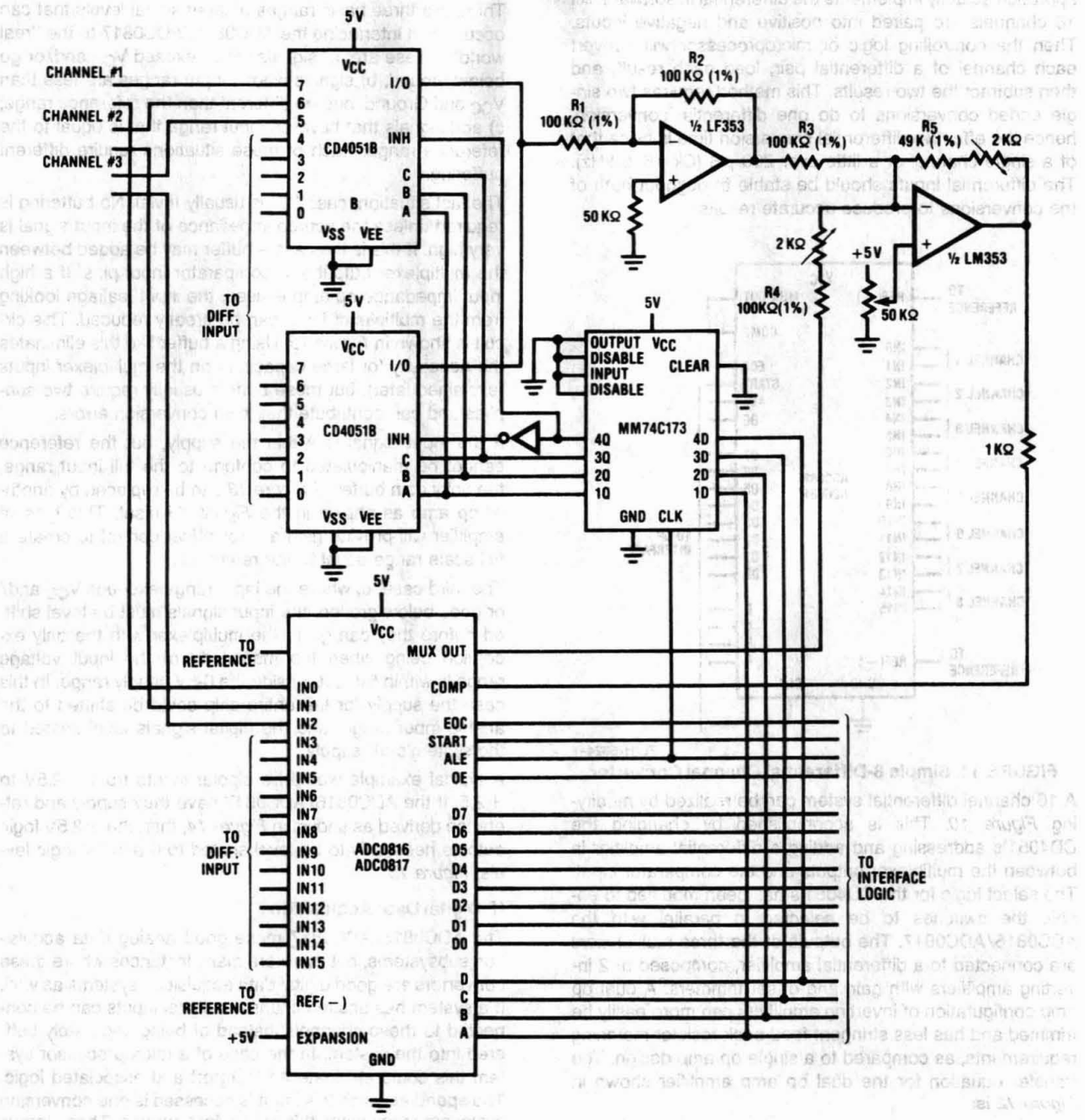

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FIGURE 12. Differential 16-Channel A/D Converter

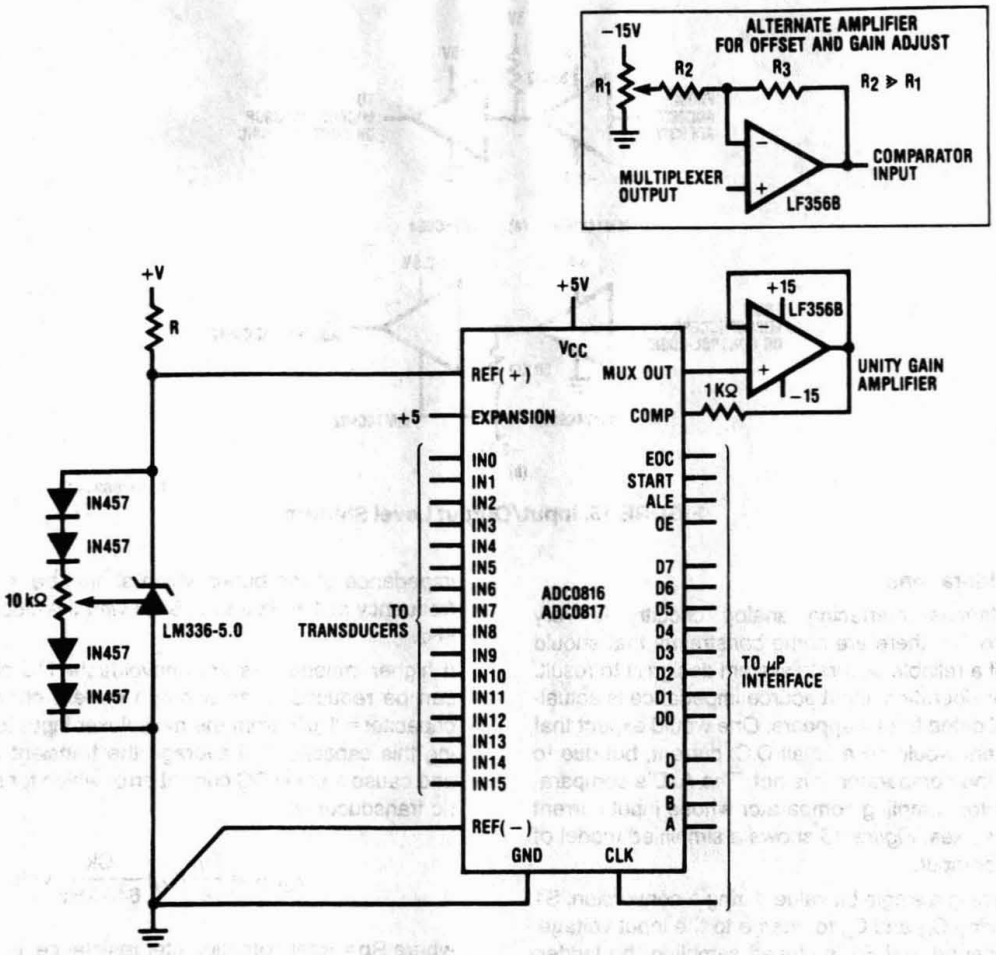

FIGURE 13. Single Input Amplifier Buffering

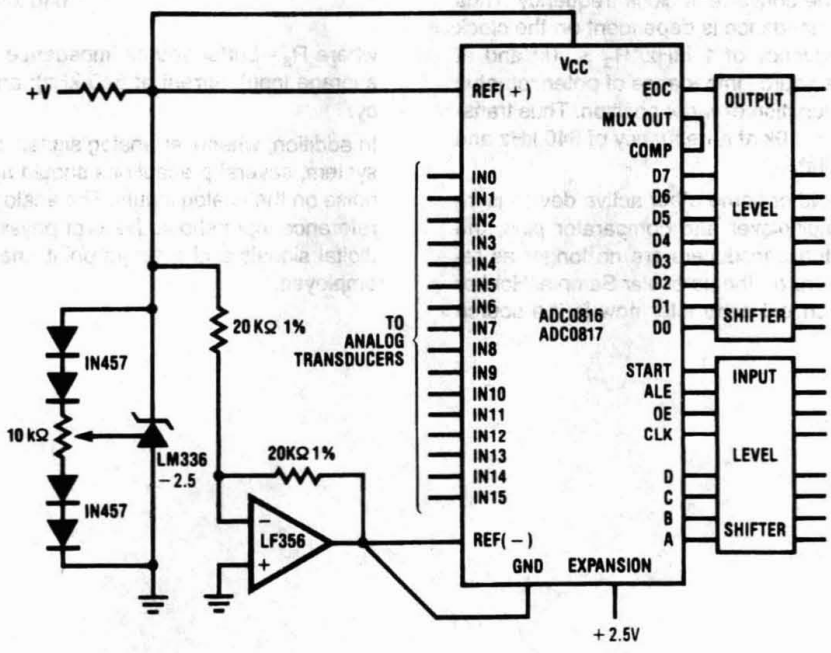

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FIGURE 14. ±2.5V Input Range Data Acquisition

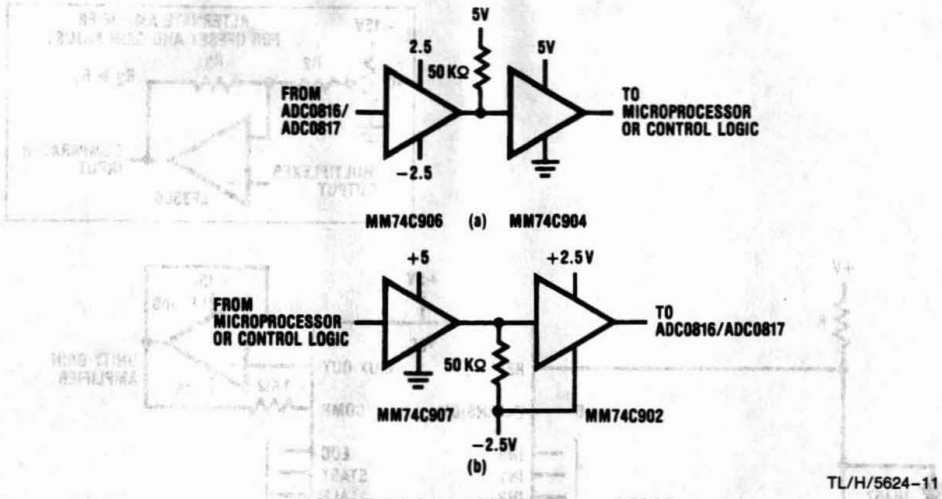

FIGURE 15. Input/Output Level Shifters

I. Input Considerations

In most instances interfacing analog circuitry is very straightforward, but there are some constraints that should be observed if a reliable accurate system design is to result. One major consideration, input source impedance is actually more complicated than it appears. One would expect that the input current would be a small D.C. current, but due to the nature of the comparator, it is not. The A/D's comparator is a capacitor sampling comparator whose input current is a series of spikes. *Figure 16* shows a simplified model of the comparator input.

When determining a single bit value during a conversion, S1 will close causing C_C and C_p to charge to the input voltage. Then S1 is opened and S2 is closed sampling the ladder. The input current is an RC transient charging current whose magnitude and duration is dependent on the values of C_C, C_p, R_S, R_m and R_L. The duration of the transient must be shorter than the input sample period, and the sample period is dependent on the converter's clock frequency. Thus the maximum source impedance is dependent on the clock period. At a clock frequency of 1 MHz, $R_S \leq 1k$; and at 640 kHz, $R_S \leq 2k$. The source impedance of potentiometric transducers vary as a function of wiper position. Thus transducers with a value of $\leq 10k$ at a frequency of 640 kHz and $\leq 5k$ at 1 MHz are suitable.

When a sample-and-hold or some other active device is inserted between the multiplexer and comparator pins, the output impedance of the transducers are no longer as restricted and depend more on the particular Sample/Hold or op amp chosen. The critical parameter now is the source impedance of the buffer which should be $\leq 3k$ at a clock frequency of 1 MHz and $\leq 5\ k\Omega$ with the clock equal to 640 kHz.

If higher impedances are unavoidable, RC charging errors can be reduced to an average current error by placing a capacitor = 1 μF, from the multiplexer input to ground. Adding this capacitor will average the transient current spikes and cause a small DC current error which for a potentiometric transducer is:

$$V_{ERR} = \frac{Rp}{8}(I_{IN})\frac{Ck}{640\ kHz}\ Volts$$

where Rp = total potentiometer resistance; $I_{IN} = 2\ \mu A$ (maximum input current at 640 kHz); and Ck = clock frequency. For a standard buffer source impedance the voltage error is:

$$V_{ERR} = I_{IN}(R_S)\frac{Ck}{640\ kHz}\ Volts$$

where R_S = buffer source impedance; $I_{IN} = 2\ \mu A$ (maximum average input current at 640 kHz); and Ck = clock frequency.

In addition, whenever analog signals are present in a digital system, several precautions should be exercised to reduce noise on the analog inputs. The analog input signals and the reference input should be kept physically isolated from the digital signals and a single point analog ground should be employed.

J. Protecting the Analog Inputs Against Over Voltages

During normal operation, it is important to keep the analog input voltages to the multiplexer or comparator between V_{CC} and Ground to ensure proper operation. There may be some occasions where over or under voltages cannot be avoided. Protecting the analog inputs, due to their unique nature, can be more difficult than digital inputs. The most effective method is to use external Schottky diodes as shown in *Figure 17a*. Since the Schottky knee voltage is 0.4 volts the IN5166 diodes of *Figure 17a* will safely shunt currents up to several milliamps. To shunt possible currents larger than several milliamps some series resistance may be added to limit these currents as shown in *Figure 17b*, but this value resistor must be no greater than the values specified in the previous section.

A less expensive solution would be to replace the Schottky diode with some standard switching diodes, *Figure 17b*, but since these diodes could only partially shunt the input current from the internal clamp diodes, some series resistor should be used as in *Figure 17c*. If the external diode must shunt a large amount of current the two series resistors of *Figure 17d* should be used. If the input design is such that the input can exceed only one supply the diode going to the other supply can be omitted.

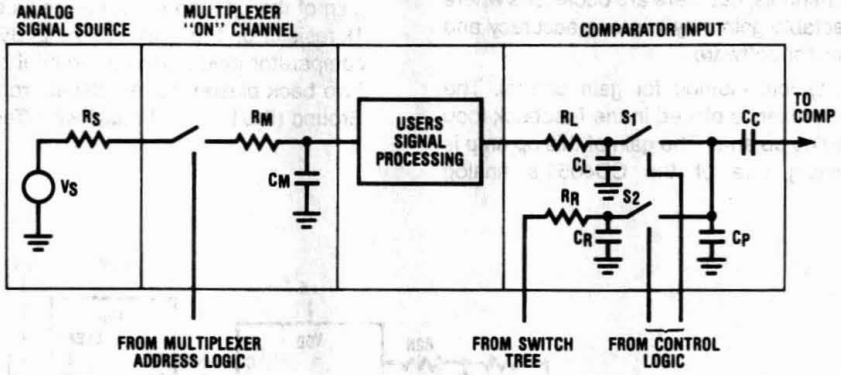

FIGURE 16. Simplified Multiplexer/Comparator Equivalent Circuit

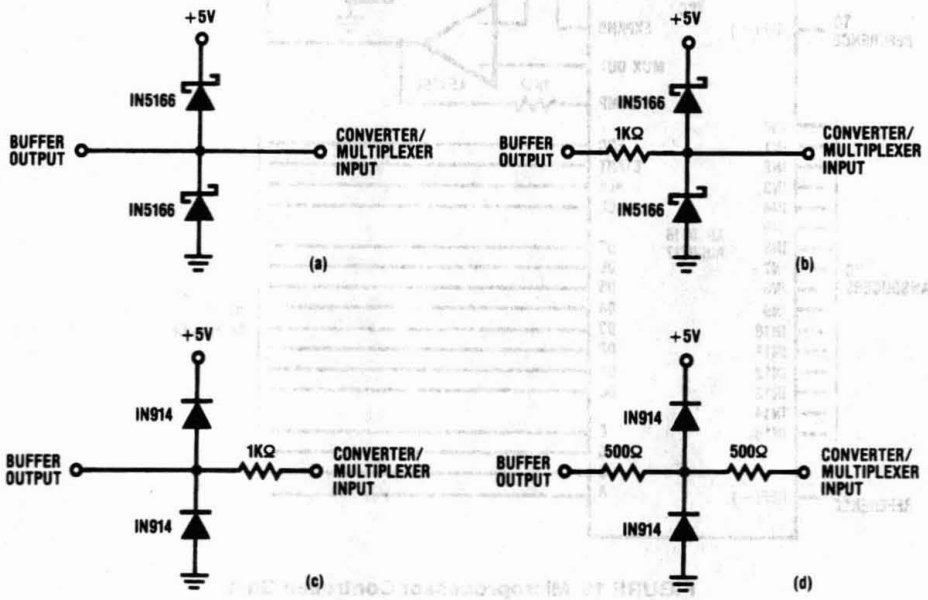

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FIGURE 17. Analog Input Protection Circuitry

IV. Signal Conditioning

There are many applications where it is desirable to add some signal processing circuitry to improve circuit performance. Typical additions would be filter circuits, sample/holds, gain controlled amplifiers, and others. Here again the external accessibility of the multiplexer output and comparator input pins can greatly reduce the amount of circuitry required by enabling the use of only one circuit required by all 16 outputs instead of 1 for each input.

A. Gain Control

Previous examples of gain manipulation have dealt with one fixed gain for all 16 channels, but there are occasions where variable gain or selectable gain may improve accuracy and simplify hardware and/or software.

Figure 18 shows a typical method for gain control. The CD4051, analog multiplexer, is placed in the feedback loop of a simple non-inverting op amp. The gain of this op amp is controlled by selecting one of the CD4051's analog switches.

This will switch a resistor in and out of the feedback loop. If these resistors, R_{2N}, are of different values, different gains are realized. These gains are given by:

$$A_V = 1 + \frac{R_{2N}}{R_1}$$

A microprocessor or some control logic would select a gain by latching the channel address into a MM74C173. It is important to ensure the output of the LF356B does not exceed the power supply, so before a new channel is selected the gain of the op amp should be reduced to a safe value. The 1k resistor on the output of the LF356 is to help protect the comparator inputs from accidental over or under voltages. Two back biased diodes placed from the input to V_{CC} and Ground (IN914 or Schottky) will offer further protection.

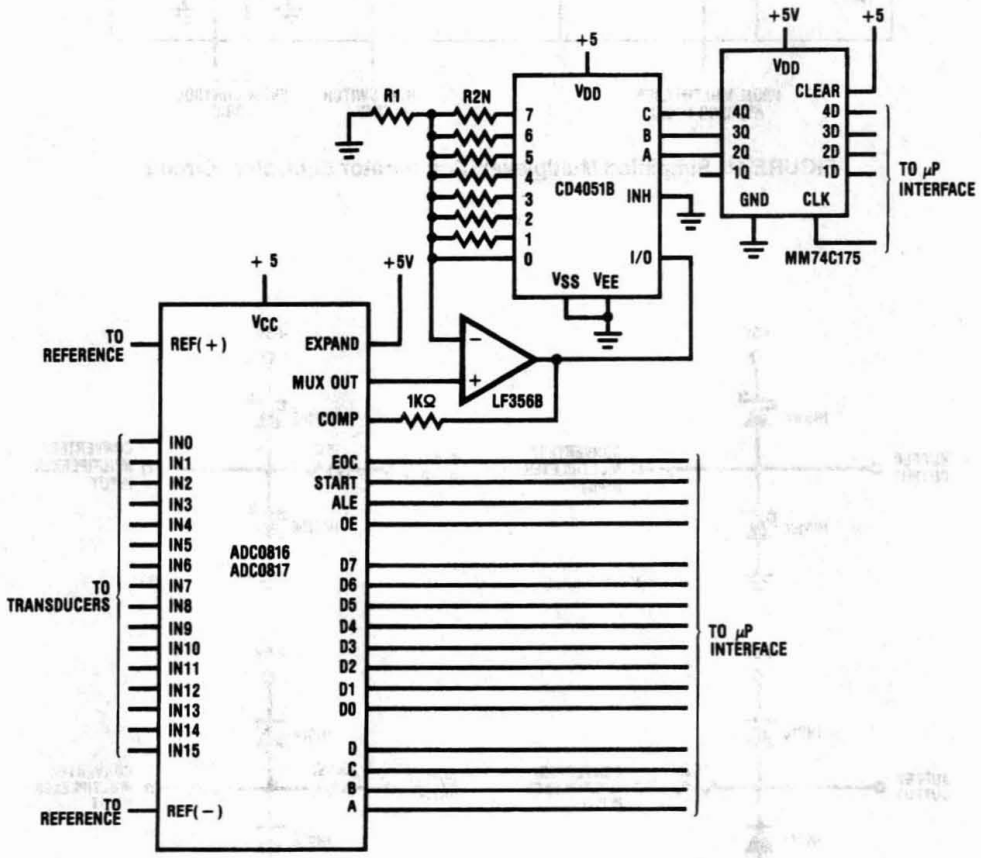

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FIGURE 18. Microprocessor Controlled Gain

B. Sample/Holds

The only major data acquisition element not included on the ADC0816 is a sample/hold circuit. If the input signals are fast moving then a S/H should be used to quickly acquire the signal and then hold it while the ADC0816/ADC0817 converts it. This circuit can be easily implemented by inserting it between the multiplexer output and the comparator input.

The simplest solution is to tie a capacitor on the multiplexer output and then tie this pin to the comparator input pin. The expansion control pin is used as a sample control. When this pin is high one switch is on and the capacitor voltage will follow the input. However, when the expansion control pin is pulled low, all switches are turned off and the capacitor holds its last value, almost. The input bias to the comparator is about 2 μA (worst case with Ck = 640 kHz). Thus the droop rate for a 1000 pF is approximately 2000 V/S or about 0.2 V/conversion. This is totally impractical. If a 0.01 μF capacitor is used instead then the droop rate is 20 mV, which may be satisfactory. Unfortunately, the acquisition time is on the order 100 μS, or about the length of a conversion.

The problem is that the comparator input leakage is too high for this sample and hold. To eliminate this, the input can be buffered by using an LM356B. *Figure 19*. The leakage, now due mostly to multiplexer leakages, is reduced to approximately 100 nA. The droop per conversion is typically less than 1.0 mV per conversion when using a 1000 pF capacitor and the acquisition time is approximately 20 μS.

A more accurate solution would be to isolate the capacitor from both the multiplexer comparator pins of the ADC0816/ADC0817. This is easily accomplished by using the LF398 monolithic sample/hold, as shown in *Figure 20*. The acquisition time for this part is typically 4 μS to 0.1%, and the droop rate is 20 μV/conversion. This circuit has its own hold control thus the expansion control is free to be used normally.

The choice of the hold capacitor is critical to the performance of the sample/hold circuit. Some capacitors are composed of dielectrics that will have an initial droop after the hold is strobed. This is due to dielectric absorption. Polypropylene and polystyrene dielectrics have very little dielectric absorption and thus make excellent sample/hold capacitors. Such materials as mylar polyethylene have higher absorption properties and should not be used.

C. Filtering Analog Inputs

Under some conditions the analog input may have come from a noisy environment and to recapture the original signal some filtering may be required. Typically high frequency noise must be filtered. The ADC0816/ADC0817 can easily accommodate the addition of many standard low pass filters. Another useful filter is a 50 Hz or 60 Hz notch filter to eliminate the noise contributed to the circuit by A.C. power lines.

It is particularly easy to place a single passive filter between the multiplexer output and comparator input pins, but passive filters must be carefully designed to reduce input loading. The filter capacitor will tend to average the comparator sampling current as mentioned in the Input Considerations section. To eliminate this, the passive filter can be buffered by an op amp or an active filter could be used.

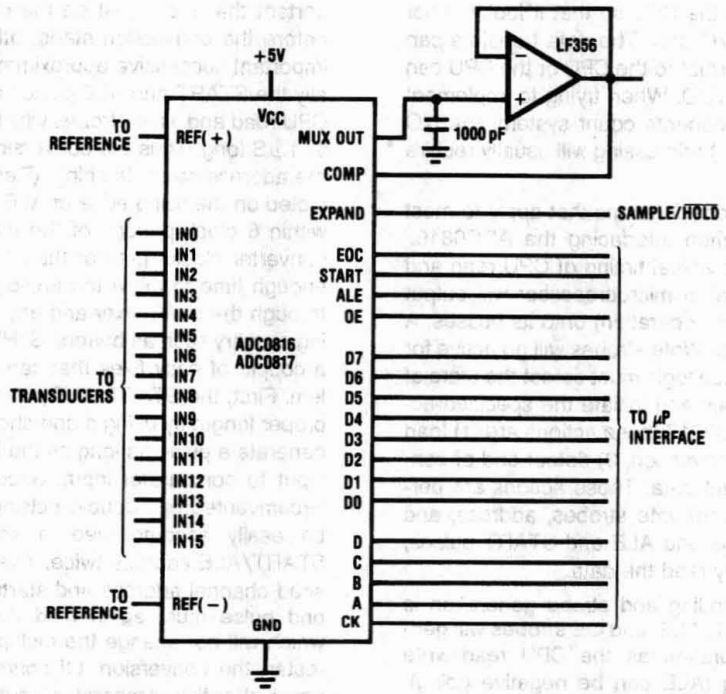

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FIGURE 19. Op Amp Sample Hold Circuit

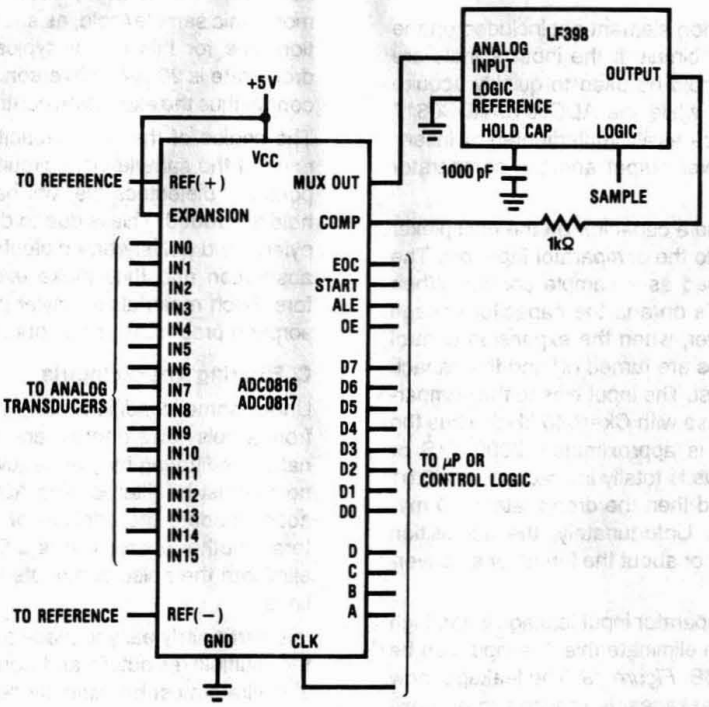

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FIGURE 20. Sample/Hold Converter Using LF398

V. Microprocessor Interface

The interface requirements for the ADC0816/ADC0817 interconnection to various microprocessors are essentially the same as the ADC0808/ADC0809 requirements. The devices can be connected to the CPU so that it looks either like a memory location or I/O port. The data transfers can be initiated by either an interrupt to the CPU or the CPU can periodically interrogate the A/D. When trying to implement an absolute minimum components count system, the I/O port (as opposed to memory) addressing will usually require fewer components.

There are several design considerations that apply to most microprocessor systems when interfacing the ADC0816/ADC0817. Even though the actual timing of CPU read and write cycles vary, in general, a microprocessor will output the address and data (if write operation) onto its busses. A certain time later the Read or Write strobes will go active for a specified time. The interface logic must detect the state of the address and data busses and initiate the specified action. For the ADC0816/ADC0817 these actions are: 1) load channel address, 2) start conversion, 3) detect end of conversion and 4) read resultant data. These actions are performed by decoding the read/write strobes, address, and data information to form the and ALE and START pulses, then detect EOC, and finally read the data.

For the most part the decoding and strobe generation is straight forward. The START, ALE, and OE strobes will generally be of the same duration as the CPU read/write strobes and positive going (ALE can be negative going). One subtle choice is where to derive the A, B, C, and D channel select address. These lines can be connected to either the address bus or the data bus. The advantage of connecting them to the data bus is that in minimum systems, more I/O address lines are available for simple decoding. When the A, B, C, and D inputs are connected to the address bus each analog channel becomes a separate I/O port.

In most designs it is very tempting to tie START and ALE together, enabling one pulse to both write the channel address and then start the conversion. However, it is very important that the signal on the comparator input be stable before the conversion starts, otherwise the first and most important successive approximation could be in error. Usually the START and ALE pulses are the same length as the CPU read and write strobes which are normally between 0.2 to 1.μS long. Thus the conversion may start within 1 μS of the address select latching. (Remember the channel is selected on the rising edge of ALE and the conversion begins within 8 clock periods of the falling edge of START.) For converter clocks greater than 500 kHz, 1 μS may not be enough time to allow the analog input signal to propagate through the multiplexer and any additional signal conditioning circuitry such as buffers, S/H's, etc. There are, however, a couple of easy fixes that can correct this possible problem. First, the START/ALE pulse could be stretched to the proper length by using a one-shot (MM74C221 or similar) to generate a pulse as long as the total delay from multiplexer input to comparator input. Secondly, the problem can be circumvented by "double pulsing" the converter. This can be easily accomplished in software by writing to the START/ALE address twice. The first pulse latches the desired channel address and starts the conversion. The second pulse must again load the same channel address, which will not change the multiplexer's state, and will then restart the conversion. Of course, the second pulse must occur after the comparator input has settled.

Even though the hardware to interface the ADC0816/ADC0817 to various microprocessors will differ and the system software will vary, the basic routines to operate the ADC0816/ADC0817 are usually similar. There are many variations, but *Figures 21* & *22* illustrate flow charts that typify these routines. The ADC0816/ADC0817 is tied directly

to the address and data bus (as opposed to using a peripheral controller). Generally, the hardware to create START and ALE pulses. This does not necessarily have to be true, but write instructions are conceptually easier and little is gained by designing the logic such that read instructions intiate these pulses. The OE pulse must be created by an I/O or memory read as the converter's data must be read.

The major design consideration is whether EOC should be polled by the microprocessor or whether EOC should cause an interrupt. This decision is system dependent, however the following applications illustrate both methods.

A. Interfacing to INS8080

Interfacing the ADC0816/ADC0817 to an INS8080 system is extremely simple, because the INS8080/INS8224/INS8228 CPU group have separate I/O read ($\overline{I/OR}$) and I/O write ($\overline{I/OW}$) strobes which imply that the INS8080 has separate I/O addressing. In small systems this means that very little or no address decoding is necessary. *Figure 23* shows a very simple interface which uses two NOR gates to gate the I/O strobes with the most significant address bit A7. The INS8080 has 8 bits of port address which will yield a maximum of 4 I/O ports if inputs A, B, C, and D are connected to the address bus. A MM74C74 flip-flop is used as a divide-by-2 to generate a converter clock of 1 MHz. If the INS8080 system clock is $\leq$1 MHz this flip-flop is unnecessary.

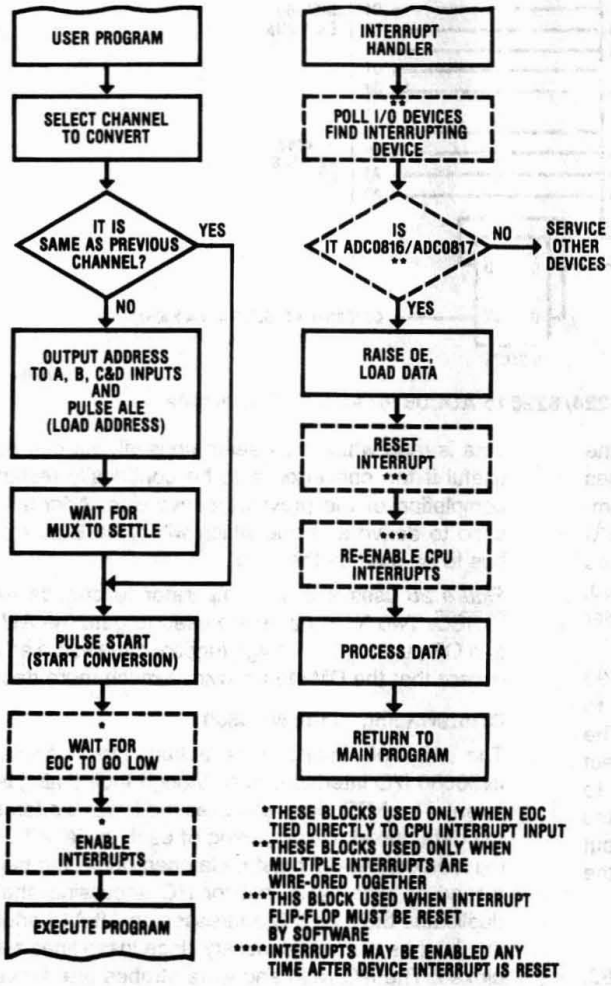
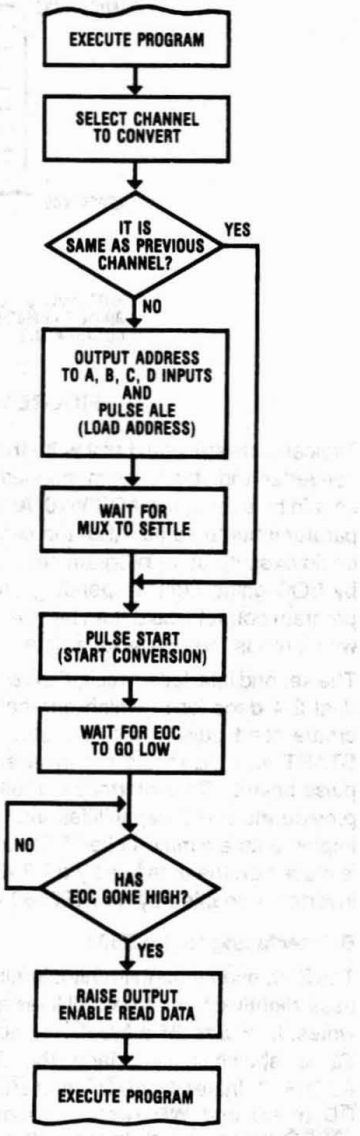

USER PROGRAM
SELECT CHANNEL TO CONVERT
IT IS SAME AS PREVIOUS CHANNEL?
YES
NO
OUTPUT ADDRESS TO A, B, C&D INPUTS AND PULSE ALE (LOAD ADDRESS)
WAIT FOR MUX TO SETTLE
PULSE START (START CONVERSION)
WAIT FOR EOC TO GO LOW
ENABLE INTERRUPTS
EXECUTE PROGRAM
INTERRUPT HANDLER
POLL I/O DEVICES FIND INTERRUPTING DEVICE
IS IT ADC0816/ADC0817
NO
SERVICE OTHER DEVICES
YES
RAISE OE, LOAD DATA
RESET INTERRUPT
RE-ENABLE CPU INTERRUPTS
PROCESS DATA
RETURN TO MAIN PROGRAM
*THESE BLOCKS USED ONLY WHEN EOC TIED DIRECTLY TO CPU INTERRUPT INPUT
**THESE BLOCKS USED ONLY WHEN MULTIPLE INTERRUPTS ARE WIRE-ORED TOGETHER
***THIS BLOCK USED WHEN INTERRUPT FLIP-FLOP MUST BE RESET BY SOFTWARE
****INTERRUPTS MAY BE ENABLED ANY TIME AFTER DEVICE INTERRUPT IS RESET

FIGURE 21. Flow Chart for Interrupt Control of ADC0816/ADC0817



TL/H/5624–16

FIGURE 22. Flow Chart to Control ADC0816/ADC0817 in a Polled I/O Mode

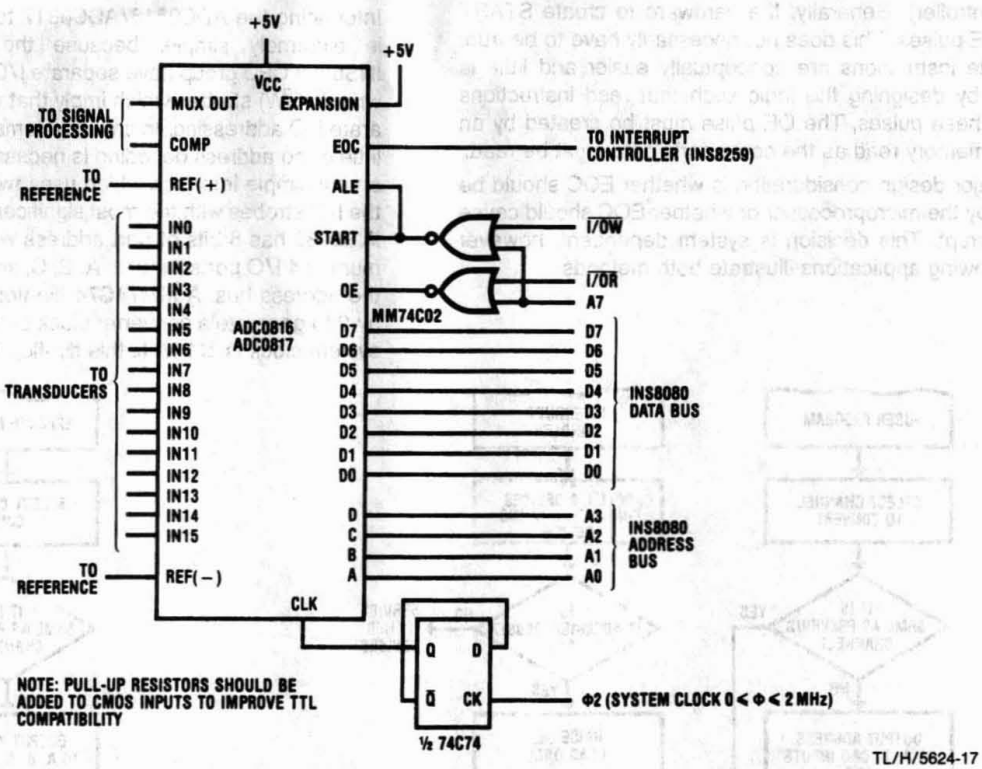


FIGURE 23. Simple INS8080/8224/8228 to ADC0816/ADC0817 Interface

Typical software would first write the channel address to the converter and start it. As mentioned before, two start pulses should be sent to the ADC0816/ADC0817 to allow the comparator input to settle. After the second start pulse the CPU could execute other program segments until it is interrupted by EOC going high. Depending on the interrupt structure, program control would then be given to the interrupt handler which reads the converter's data.

The second interface circuit, *Figure 24* utilizes a DM74LS139 dual 2-4 decoder in which one-half of the chip is used to create read pulses and the other half write pulses. The START and OE inputs are inverted to provide the correct pulse polarity. This interface partially decodes A6 and A7 to provide more I/O capabilities than before. This circuit also implements a simple polled I/O structure. The EOC output is placed on the data bus by a TRI-STATE inverter when the inverter is enabled by an INS8080 read.

B. Interfacing to the Z80®

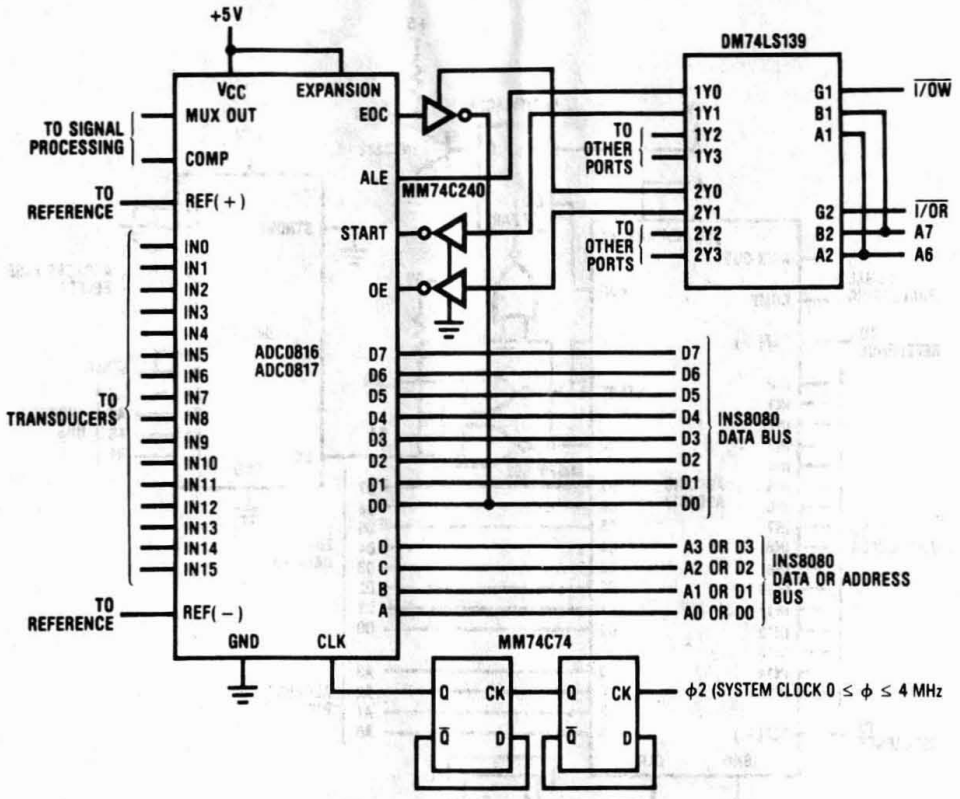
The Z80, even though architecturally similar to the INS8080, uses slightly different control lines to perform I/O reads and writes. In *Figure 25* a NOR gate approach similar to *Figure 22* is shown to interface the Z80 to the ADC0816/ADC0817. Instead of $\overline{I/OR}$ and $\overline{I/OW}$ strobes the Z80 has $\overline{RD}$ (read) and $\overline{WR}$ (write) strobes which are gated with $\overline{IOREQ}$ (I/O request). In the Z80 interface, to show a slight variation, START is connected to OE instead of ALE. This will cause a new conversion to be started whenever the data is read which may seem unusual, but can actually be useful if the converter is to be continually restarted upon completion of the previous conversion. Address bit A6 is used to derive a strobe which will place EOC on the data bus to be read by the CPU.

Figure 26 uses a 6 bit comparator to decode A4-A7 and $\overline{IOREQ}$. Two NOR gates are used to gate the ALE/START and OE pulses. This design functions the same as *Figure 23* except that the DM8131 provides much more decoding.

C. Interfacing to the NSC800

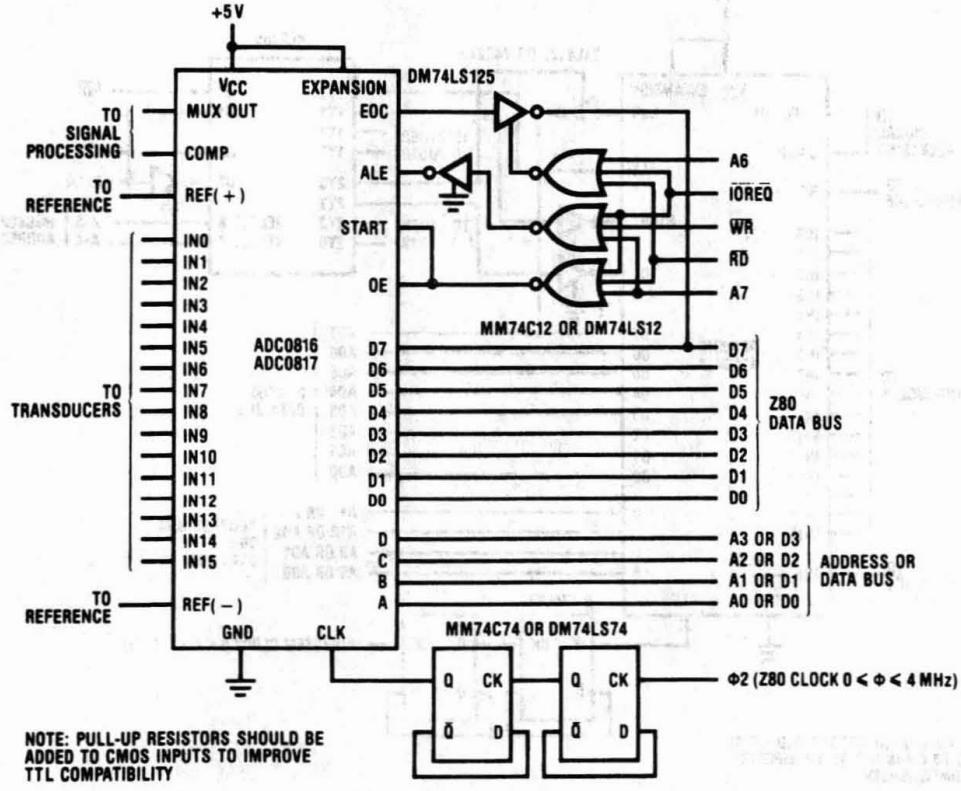
The NSC800 interface is actually very similar to the INS8080 I/O interface, even though their timing is very different. The NSC800 multiplexes the lower 8 address bits on the data bus at the beginning of each cycle. When accessing memory, A0-A7 must be latched out at the beginning of a read or write cycle, but for I/O accessing; the NSC800 duplicates the 8 bit I/O addresses on A8-A15 address lines and latches are not necessary since these lines aren't multiplexed. The I/O read and write strobes are derived from a $\overline{RD}$ (read) and $\overline{WR}$ (write) line and the IO/$\overline{M}$ signal.

Figure 27 shows a design using a dual 2-4 line decoder which decodes A15, and A14 and is enabled by the read/write strobes. TRI-STATE inverters are used to implement a scheme similar to *Figure 24*. This scheme has START and ALE accessed separately so that "double pulsing" isn't required.



NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

FIGURE 24. Partial Address Decoding INS8080/8224/8228 to ADC0816/ADC0817



NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

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FIGURE 25. Simple Z80 Interface to ADC0816/ADC0817

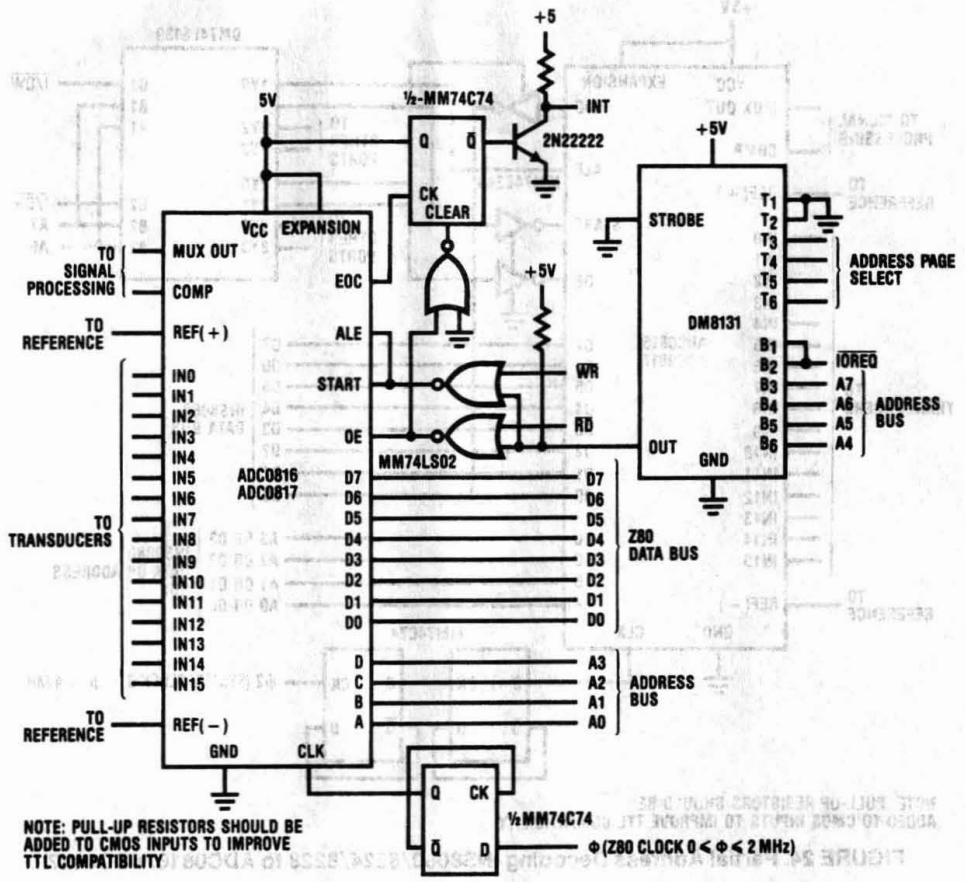
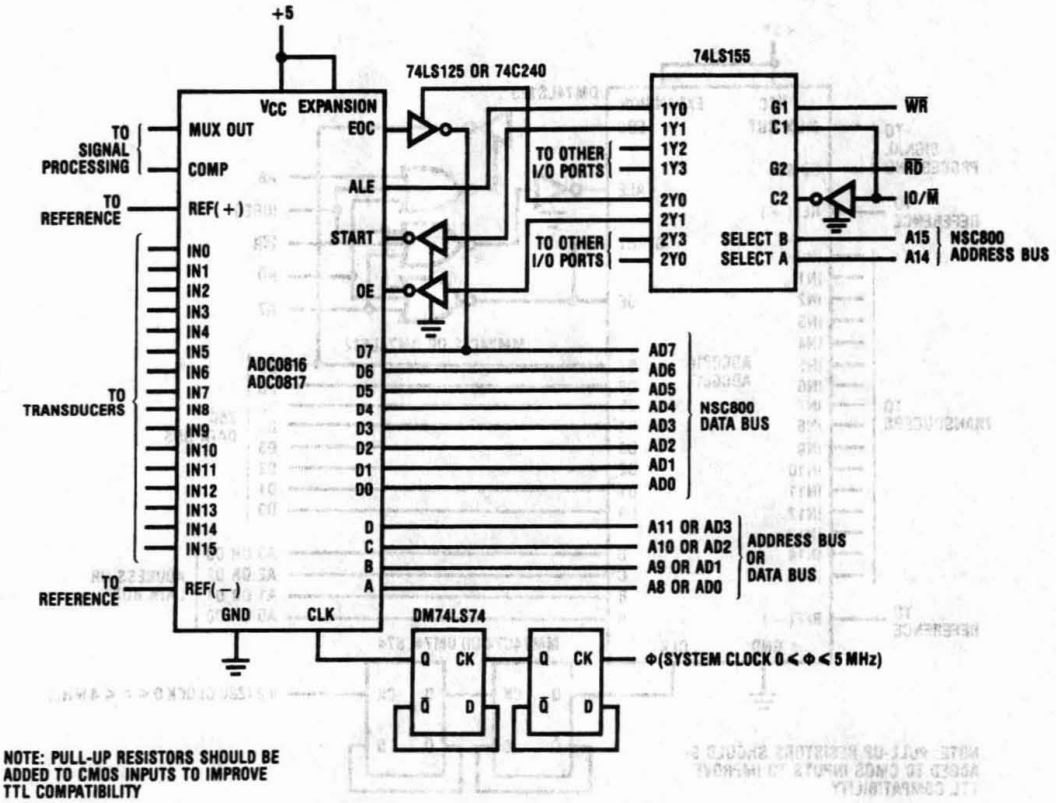


FIGURE 26. Decoded Z80 Interface



TL/H/5624-19

FIGURE 27. Partially Decoded NSC800 to ADC0816/ADC0817 Interface

The next design, *Figure 28*, uses the same simple NOR gating scheme as *Figure 23*, except the NSC800 control signals are slightly different. A simple interrupt scheme for EOC is employed using an MM74C74. When EOC goes high the flip-flop is set and $\overline{INTR}$ goes low. When the NSC800 acknowledges the interrupt by lowering $\overline{INTA}$, the flip-flop will reset. If more than one interrupt can occur simultaneously either $\overline{INTA}$ should be gated with EOC, or some other signal instead of $\overline{INTA}$ must be used. This is required since it is possible for the NSC800 to detect another interrupt and clear the ADC0816/ADC0817 interrupt before it's detected.

D. Interfacing to the 6800

The 6800 has no separate I/O addressing capabilities, so the system I/O must be addressed as though it is memory. As mentioned before, memory mapping can require more address decoding in order to separate memory from I/O, but in small systems very minimal parts count is still attainable.

Figure 29 illustrates an interface which uses a DM8131 comparator to partially decode the A12, A13, A14, and A15 address lines with the ϕ_2 clock and Valid Memory Address (VMA), to provide an address decode pulse for the two NOR gates which in turn generate the START/ALE Pulse and the output enable signal. This design will locate the A/D in one 4k byte block.

This design tied EOC to $\overline{IREQ}$ interrupt through an inverter. This is only usable in single interrupt systems since the 6800 has no way of resetting this interrupt except by starting a new conversion. Since EOC is directly tied to the interrupt input, the controlling software must not re-enable interrupts until 8 converter clock periods after the START pulse when EOC is low.

The memory control signals are very different from the INS8080 type CPU's. One line indicates whether the operation is a read or write, R/$\overline{W}$ instead of separate read/write outputs on the INS8080/Z80/NSC800. This signal along with VMA indicates a valid read/write operation.

Figure 30 is slightly more complex, but provides more I/O port strobes. A NAND gate and inverter are used to decode the addresses, VMA and ϕ_2 clock. The I/O addresses are located at 11110XXXXXAABBBB (Binary); where X = don't care; A = 00 (Binary) for ALE write or IREQ reset/EOC read and A = 01 for START write or Data read; and B = channel select address if A, B, C and D are connected to the address bus and ALE is accessed. A dual 2-4 line decoder is used to generate these strobes and inverters are used to create the correct logic levels.

The 6800 supports only a wired-OR interrupt structure. In a multi-interrupt environment only one interrupt is received and the interrupt handler routine must determine which device has caused the interrupt and service that device. (Although the INS8080/Z80/NSC800 can implement a similar structure, hardware interrupt controllers can also be used which will automatically vector the μP to the correct service routine.) To do this EOC is brought out to the data bus so the CPU can check it.

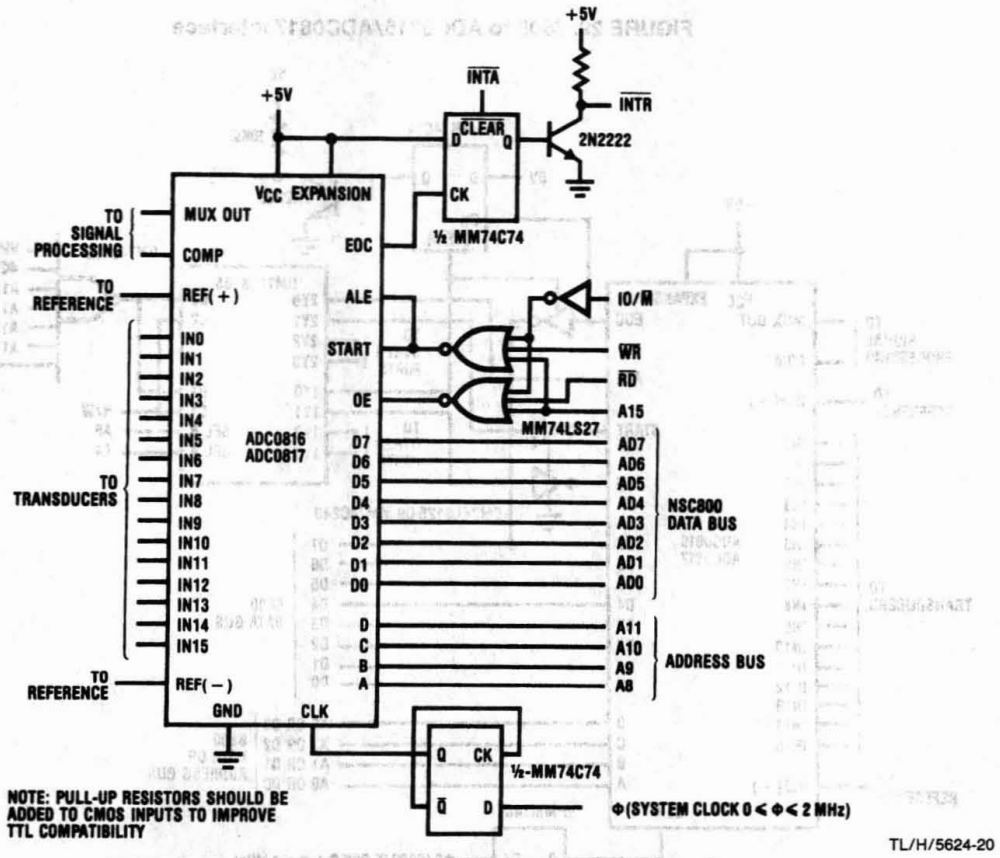


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FIGURE 28. Minimal NSC800 to ADC0816/ADC0817 Interface

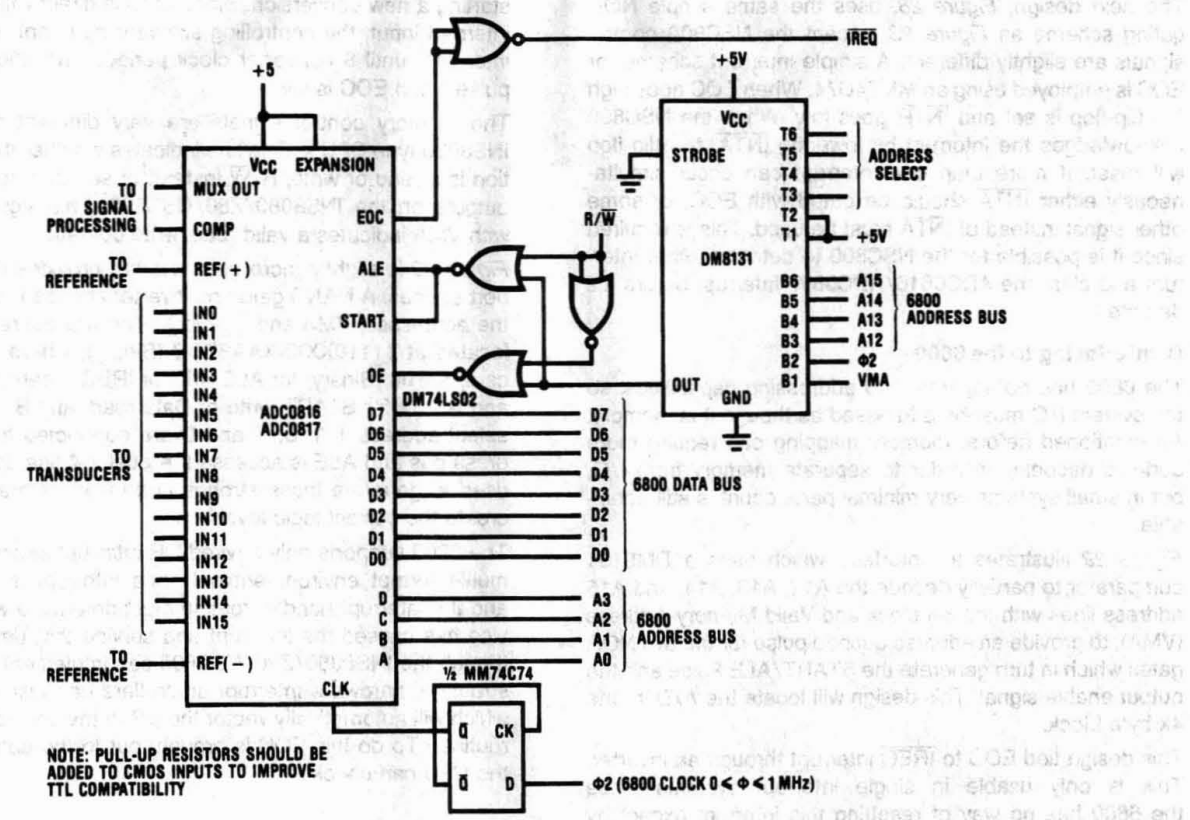

FIGURE 29. 6800 to ADC0816/ADC0817 Interface

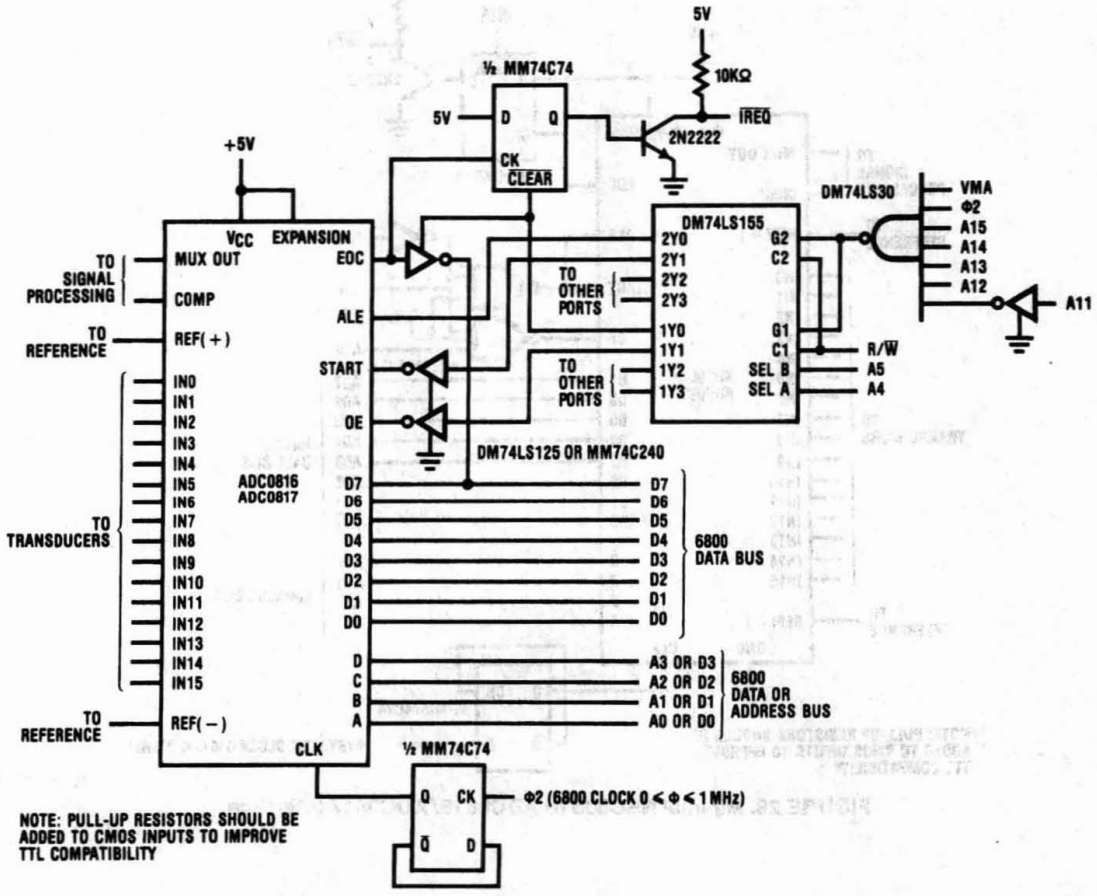

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FIGURE 30. Partially Decoded 6800 to ADC0816/ADC0817 Interface

F. Parallel Interface Circuits

In some cases μP support chips can be used to interface the ADC0816/ADC0817 to microprocessors. Most parallel I/O chips can be used, and provide enough flexibility to enable all functions to be under software control. Typical parallel I/O chips that could be used are INS8255, 6820, Z80-PIO and others. Typically these support IC's would be connected directly to the data and control pins and the software would manipulate the START and ALE pins via the interface chip. In some cases the chips provide handshaking and/or interrupt capabilities which can ease the converter interface. In some cases, the interface circuits will not provide a clock, and therefore must be provided externally.

While use of parallel I/O circuits simplify designs and increase versatility, they are more expensive than the 1 or 2 SSI or MSI circuits that they would replace, and thus not always the best choice.

VI. Conclusion

The ADC0816/ADC0817 are easy to use general purpose A/D converters with the additional benefit of a 16 channel analog multiplexer. The IC's can become a simple standard 8-bit data acquisition circuit or the basis of a more powerful data acquisition system. Both integrated circuits provide features to enable easy microprocessor interface, yet also allow hardwired control logic to be used. In those applications which require less accuracy, the less expensive ADC0817 can be used to reduce overall system cost.

A 20-Bit (1 ppm) Linear Slope-Integrating A/D Converter

National Semiconductor
Application Note 260

By combining an "inferior", 20 year old A/D conversion technique with a microprocessor, a developmental A/D converter achieves 1 part-per-million (20-bit) linearity. The absolute accuracy of the converter is primarily limited by the voltage reference available. The precision achieved by the unlikely combination of technologies surpasses conventional approaches by more than an order of magnitude. The approach used points the way towards a generation of "smart" converters, which would feature medium to high resolution (12 bits and above) with high accuracy over extended temperature range. The conversion technique employed, while slow speed, suits transducer based measurement systems which require high resolution over widely varying conditions of time and temperature. In addition, extensions of the basic converter have achieved 15-bit digitization of signal inputs of only 30 mV full-scale with no sacrifice in linearity or stability. This offers the prospect of an "instrumentation converter" which could interface directly with low level analog signals.

One of the many A/D techniques utilized in the late 50's and early 60's was the single-slope-integrating converter. One form of this circuit compares a linear reference ramp to the unknown voltage input (see About Integrating Converters and Capacitors). When the ramp potential crosses the unknown input voltage a comparator changes state. The length of time between the start of the ramp and the comparator changing state is proportional to the input voltage. This length of time is measured digitally and presented as the converter output. The inherent strengths of this type of converter are simplicity and high linearity. Although single-slope-integrators were used in early A/Ds and voltmeters their dependence on an integrating capacitor for stability was considered an intolerable weakness. The advent of the dual-slope converter (see About Integrating Converters and Capacitors) solved the problem of integrating capacitor drift with time and temperature by error cancellation techniques. In a dual-slope converter the output represents the ratio of the time required to integrate the unknown voltage for a fixed time and then, using a reference voltage of opposing polarity, measures the amount of time required to get back to the original starting point (see About Integrating Converters and Capacitors). The technique eliminates capacitor drift as an error term.

Limitations of Dual-Slope Converters

The dual-slope converter, and variants on it, have been refined to a point where 16 and 17-bit resolution units are available. A primary detriment to linearity in these converters is a parasitic effect in capacitors called dielectric absorption. Dielectric absorption can be conceptualized as a slight hysteresis of response by the capacitor to charging and discharging. It is influenced by the recent history of current flow in the capacitor, including the magnitude, duration and direction of current flow (see About Integrating Converters and Capacitors).

The nature of operation of dual-slope and related converters requires the instantaneous reversal of current in the integrating capacitor. This puts a substantial burden on the dielectric absorption characteristics of the capacitor. Although dual-slope and related techniques go far to cancel zero and full-scale drifts, residual non-linearity exists due to the effects of dielectric absorption. In addition to non-linearity, dielectric absorption can also cause the converter to give different outputs with a fixed input as the conversion rate is varied over any significant range. Various compensation arrangements are employed to partially offset these effects in present converters. What is really needed for high precision, however, is a conversion scheme which inherently acts to cancel the effects of dielectric absorption, while simultaneously correcting for zero and full-scale drifts.

Overcoming Dual-Slope Limitations

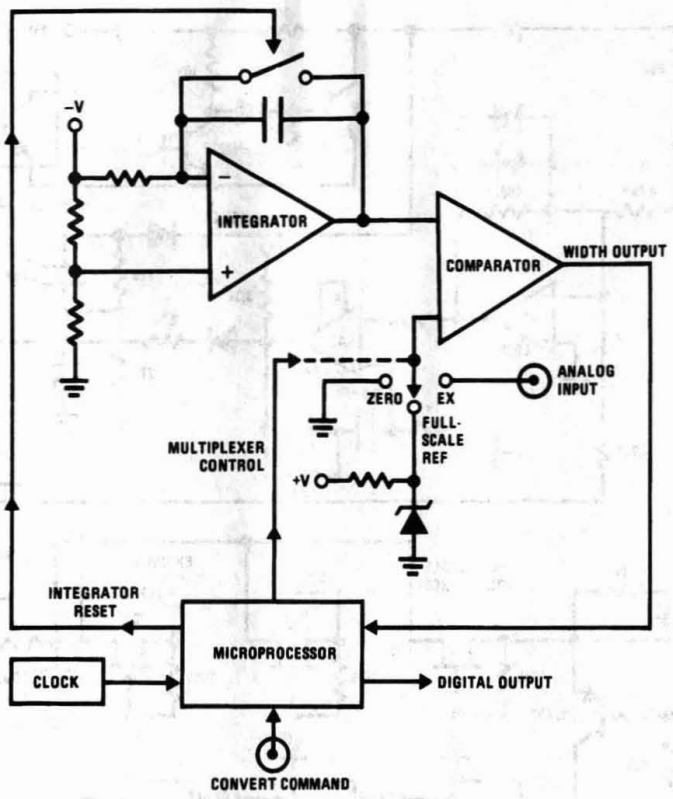
Figure 1 diagrams a converter which meets the requirement noted previously. In this arrangement a microprocessor is used to sequentially switch zero, full-scale reference and EX signals into one input of a comparator. The other comparator input is driven from the ramp output of an operational amplifier integrator. With no convert command applied to the microprocessor, the circuit is at quiescence. In this state the microprocessor sends a continuous, regularly spaced signal to the integrator reset switch. This results in a relatively fixed frequency, period and height ramp at the amplifier's output. This relationship never changes, regardless of the converter's operating state. In addition, the time between ramps is lengthy, resulting in an effective and repeatable reset for the capacitor. When a convert command is applied, the microprocessor switches the comparator input to the zero position, waits for the next available ramp and then measures the amount of time required for the ramp to cross zero volts. This information is stored in memory. The microprocessor then repeats this procedure for the full-scale reference and EX switch positions. With all this information, and the assumption that the integrator ramps are highly linear, the absolute value of EX is determined by the processor according to the following equation.

$$EX = \frac{[C_{EX} - C_{ZERO}]}{[C_{FULL\text{-}SCALE} - C_{ZERO}]} \times K\,\mu V$$

where C = count obtained

and K = a constant, typically 10^7

After this equation is solved and the answer presented as the converter's output, the conversion is complete and the microprocessor is ready to receive the next convert command.



TL/H/5625–1

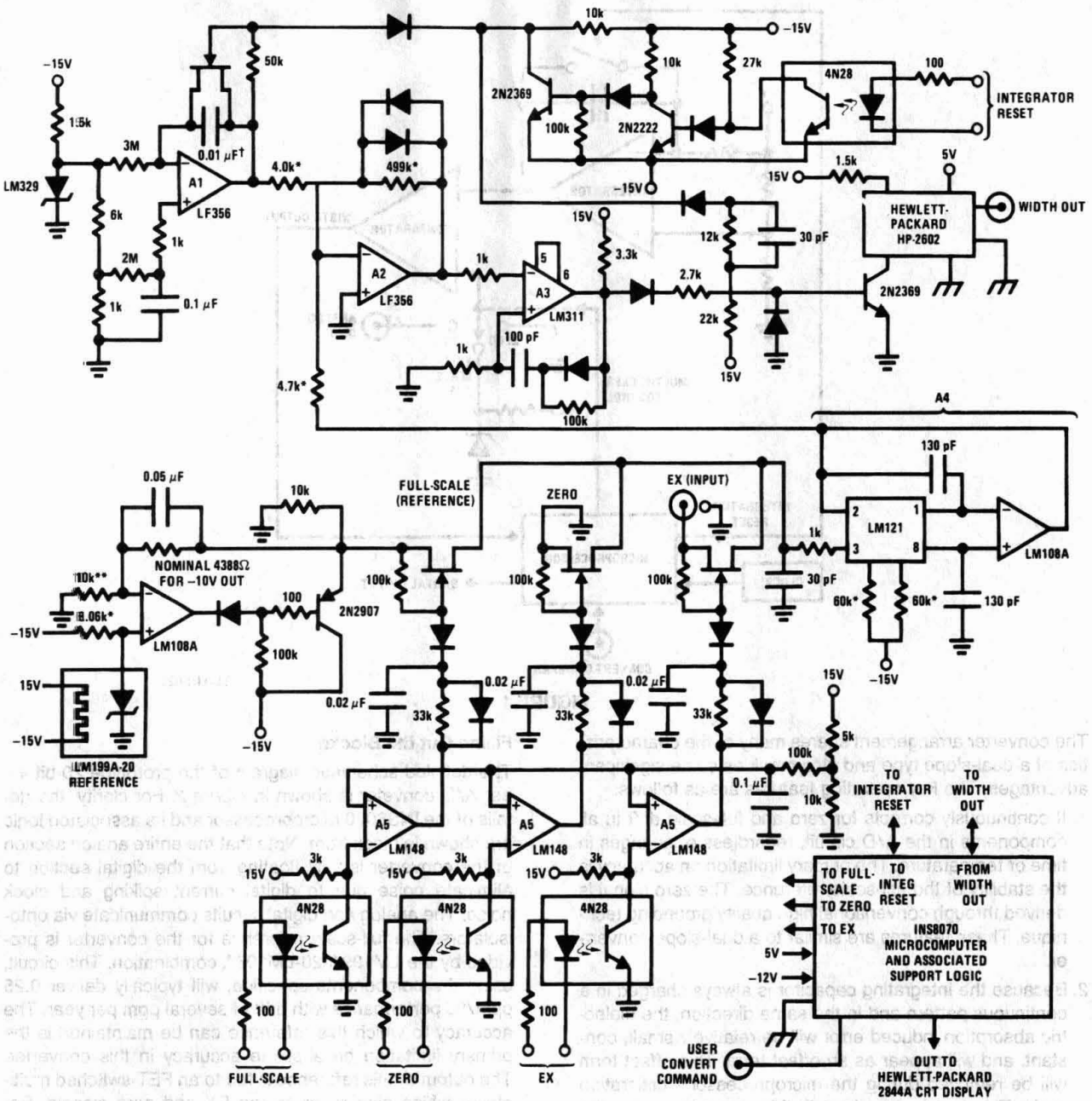
FIGURE 1

The converter arrangement shares many of the characteristics of a dual-slope type and also provides some significant advantages. The key operating features are as follows:

1. It continuously corrects for zero and full-scale drift in all components in the A/D circuit, regardless of changes in time or temperature. The primary limitation on accuracy is the stability of the full-scale reference. The zero signal is derived through conventional high quality grounding technique. These features are similar to a dual-slope converter.
2. Because the integrating capacitor is always charged in a continuous pattern and in the same direction, the dielectric absorption induced error will be relatively small, constant, and will appear as an offset term. This offset term will be removed during the microprocessor's calibration cycle. This feature is unique to this converter and is the key to high linearity.
3. The comparator always sees the ramp voltage approaching the trip point from the same direction and at the same slew rate, regardless of operating conditions. This helps maintain repeatability at the trip point in the face of noise and gain-bandwidth limitations in the comparator.
3. Unlike a dual-slope, this converter has no inherent noise rejection capability. The EX input signal is directly coupled to the comparator input with no filtering. This is a decided disadvantage because most "real world" signals require some smoothing. If a filter was placed at the input substantial time lag due to settling requirements would occur. This is unacceptable because the converter relies on short time intervals between multiplexer states to effectively cancel drift. The solution is to use the microprocessor to filter the signal digitally, using averaging techniques.

Filling Out the Blocks

The detailed schematic diagram of the prototype 20-bit linear A/D conveter is shown in *Figure 2*. For clarity, the details of the INS8070 microprocessor and its associated logic are shown in block from. Note that the entire analog section of the converter is fully floating from the digital section to eliminate noise due to digital current spiking and clock noise. The analog and digital circuits communicate via opto-isolators. The full-scale reference for the converter is provided by the LM199A-20-LM108A combination. This circuit, using the components specified, will typically deliver 0.25 ppm/°C performance with drift of several ppm per year. The accuracy to which this reference can be maintained is the primary limitation on absolute accuracy in this converter. The output of this reference is fed to an FET-switched multiplexer which also receives the EX and zero signals. Because all these sources are at low impedance, and only one is switched on at a time, the leakage and ON resistances do not contribute significant error. The A4 combination provides a low bias current unity gain follower with greater than 1,000,00:1 (120 dB) of CMRR, preserving converter linearity. Drifts in this follower are not significant because they will be cancelled out by the microprocessor's calibration cycle. The microprocessor's digital commands to the FET switches are received by the 4N28 opto-isolators. The LM148 quad op-amp (A5) is used to generate the voltage swing necessary to control the FET switches. The discrete components at each amplifier output are used to generate one-way time delays to give the FET switches break-before-make action. This prevents cross talk between the zero, full-scale reference and EX sources.



Notes

All ⊓⊔ = 2N4393

± 15V for analog circuitry is fully floating

** Vishay S-102 precision resistor

* Metal film resistor—RN60C

† Teflon—Component Research Corp.

⊣⊢ = 1N4148

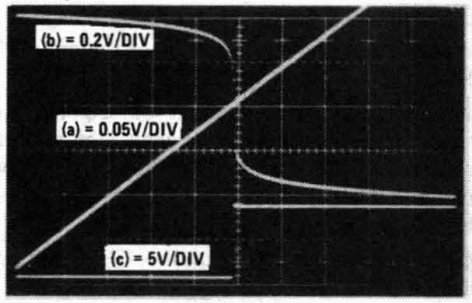
TL/H/5625–2

FIGURE 2

Another FET is used to reset the integrator and is biased by a "brute-force" level shifting-edge speed-up network formed by the 2N2222-2N2369 pair. A 4N28 opto-isolator biases this network when it receives the reset signal from the INS8070 processor. A1, an LF356, has its "+" input biased at about negative 1V, ensuring that the ramp will start far enough below ground to determine a true zero signal.

The requirement for a comparator with 1 ppm (1 LSB at 20 bits = 1 ppm) of trip point noise cannot be met by any standard device. At 10V full-scale this is only a 10 μV LSB. The 50 ms-10V ramp's relatively slow slew rate means that the gain-bandwidth and noise characteristics of a standard differential input comparator will cause considerable uncertainty at the trip point. Also, as the common-mode voltage at which the ramp vs EX crossing occurs changes, the trip point of the comparator will shift, introducing overall non-linearity.

These problems are addressed by the A2-A3 configuration, which forms a high precision comparator. A4's negative output is resistively summed with the positive output of the A1 ramp at A2. A2 normally operates at a low gain due to the diode bounding in its feedback loop. When the currents produced by the ramp potential and A4's output very nearly balance the potential at A2's summing junction will go low enough so that A2 comes out of bound and operates at a gain determined by the 499k feedback resistor (about 100). A2 remains in this high-gain state as long as the ramp and A4 output caused currents are nearly equal. As the ramp continues in its positive going direction the current into A2's summing junction will go to zero and then move positive until the A2 output bounds negative. The output of A2 drives A3, an LM311 comparator which is set up as a zero crossing detector. The components in the positive feedback path at A3 insure a sharp transition. *Figure 3* shows the waveforms of operation. The ramp (a) is shown in highly expanded form. The A2 output (b) can be seen to come cleanly out of diode-bound just before the ramp balances A4's output and then return to bound after the crossing occurs. Waveform (c) is A3's output. The A2 pre-amplifier makes the A3 comparator's job much easier in a number of ways. It amplifies the voltage difference of the two signals to be compared by a factor of 100. This knocks down the effect of A3's input uncertainties. It also produces an apparent 100 fold increase in the ramp slew rate at the trip point. This means A3 spends that much less time with its inputs nearly balanced in an uncertain and noise sensitive condition. Finally, A2 presents the difference signal as a single ended zero crossing signal. This eliminates errors due to changing common-mode voltages that a differential comparator's input would face. Such errors would manifest themselves as overall converter non-linearity.



HORIZ = 200 μs/DIV

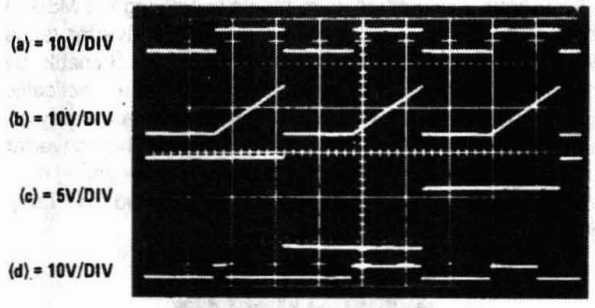
TL/H/5625–3

FIGURE 3

The output of the A3 comparator feeds a 2N2369 transistor, which functions as a level shifter-gate. This transistor gates out that portion of the width output pulse which would be due to the length of the integrator reset pulse. The 2N2369, a low storage capacitance device, provides high speed, even in the relatively slow common emitter configuration. The HP-2602 high speed opto-coupler transmits the width information to the digital circuitry.

Converter Performance and Testing

Figure 4 shows the convert at work. A complete conversion cycle is captured in the photograph. Waveform (a) is the integrator reset out of the INS8070. (b) is the ramp at A1's output. Waveform (c) is the multiplexer output at A4, showing the zero, full-scale reference and EX states. For each state ample time is allowed before the ramp begins. The width output is shown in waveform (d).

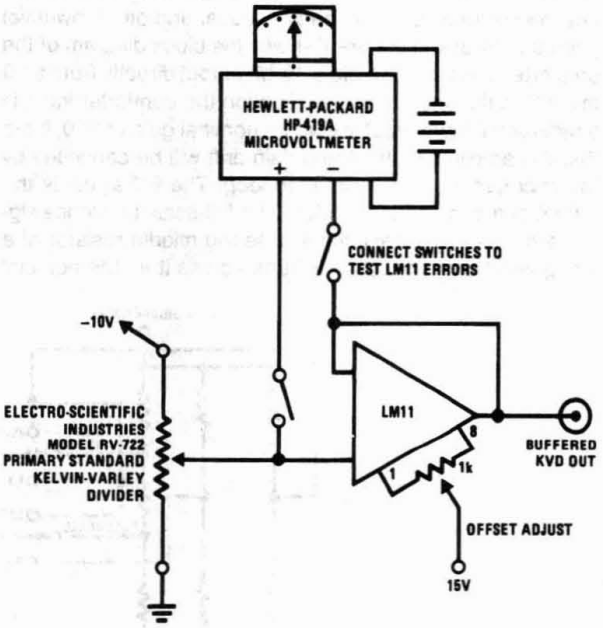


HORIZ = 50 ms/DIV (UNCALIBRATED)

TL/H/5625–4

FIGURE 4

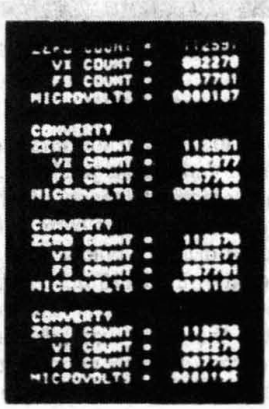
The converter was tested with the arrangement shown in *Figure 5*. The Kelvin-Varley voltage divider, a primary standard type, has a guaranteed linearity of within 1 ppm. The LM11 op amp provides a low bias current, low drift follower to unload the Kelvin divider's output impedance. Because the LM11 gives greater than 120 dB common-mode rejection, its voltage output should track the linearity of the Kelvin divider. To test this the LM11 was adjusted for offset null and a battery-powered μV meter connected between its inputs. 20-bit linear (1 ppm) transfer characteristics were verified by running the Kelvin divider through its range and noting less than 10 μV (1 LSB at 10V full-scale) shift under all conditions. Then, the converter reference was used to drive the Kelvin divider input and the LM11 output to the EX input of the A/D converter.



TL/H/5625–5

FIGURE 5

A typical output on the Hewlett-Packard 2644A CRT terminal display is shown in *Figure 6.* For each convert command to the INS8070 the number of counts of zero, full-scale reference and EX are shown along with the final computed answer. Note that the final count is computed to one part in ten million and the last digit is insignificant. Note also that the 4 final counts are all within ± 1 ppm . . . despite the fact that they were individually spaced almost 1 hour apart in a varying thermal environment. Linearity of the converter over a 10V range was verified at 10 points by varying the MSB of the Kelvin divider. Although the prototype converter takes 300 ms to complete a cycle, faster speed is attainable by increasing the 20 MHz clock rate. Perhaps more practically, higher conversion speeds at lower resolutions are easily attainable by simply shortening the ramp time. The converter output word length and conversion time may be varied over a wide dynamic range by juggling clock speed and ramp time.



TL/H/5625–6

FIGURE 6

Although demonstrating a 20-bit converter is useful, there are other applications which do not require this degree of precision. The basic technique is readily adaptable to the practical solution of common transducer and other low-level interface problems. *Figure 7* shows the block diagram of the converter used to generate a 15-bit output directly from a 30 mV full-scale input. In this application the converter input is a differential input amplifier with a nominal gain of 300. Note that the amplifier's offset and gain drift will be cancelled by the microprocessor's calibration loop. The EX signal is the output of the transducer bridge. The full-scale reference signal is derived by measuring across the middle resistor of a string which has the same voltage across it as the nominal bridge output for a given bridge drive level. In this manner, even if the bridge drive varies, the gain of the system remains calibrated by ratiometric error cancellation. The zero signal is derived by shorting both amplifier inputs to the common-mode voltage at the bridge output. This system has been built and has maintained 15-bit accuracy over a 75°F temperature range.

Prospective constructors of this converter are advised that construction technique is extremely critical. In order for the converter to operate properly, the greatest care must be taken in grounding, guarding and shielding techniques. Useful sources of information are listed in the References

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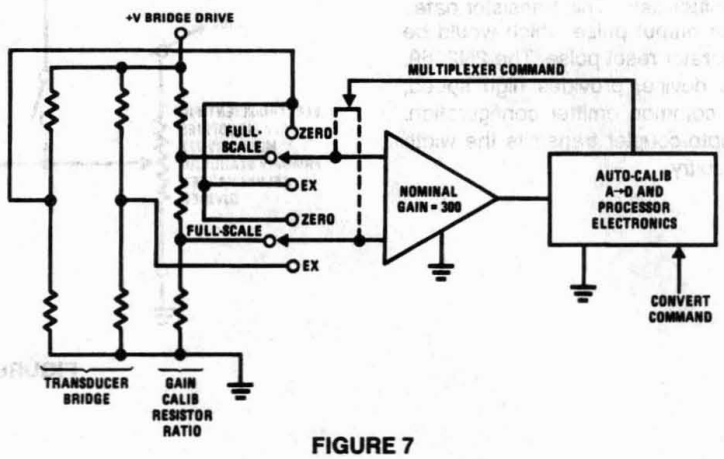

TL/H/5625–7

FIGURE 7

About Integrating Converters and Capacitors

The simplest form of integrating converter is the single-slope type (*Figure A*). In the single-slope unit shown, a linear reference ramp is compared against the unknown input, EX. When the switch across the integrator capacitor is opened, the ramp begins. The time interval between the opening of the integrator reset switch and the comparator changing state (when $E_{RAMP} = EX$) is directly proportional to the value of EX. This converter requires that the integrating capacitor and the clock used to measure the time interval be stable over time and temperature ... a significant drawback under normal circumstances.

The dual-slope integrator (*Figure B*) overcomes these problems by effectively normalizing the capacitor value and clock rate each time a conversion is made. It does this by integrating the EX input for a pre-determined time. Then, the voltage reference is switched to the integrator input which proceeds to integrate in a negative going direction from the EX slope. The length of time the reference slope requires to get back to zero is proportionate to the EX signal value. These slopes are both established with the same integrating capacitor and measured with the same clock, so both parameters need only be stable over one conversion cycle.

Both of these converters are dependent to varying degrees on capacitor characteristics. The single-slope type requires stability in the capacitor over time and temperature while the dual-slope gets around this limitation. The effects of a phenomenon in capacitors called dielectric absorption, however, have direct impact on dual-slope performance. Dielectric absorption is due to the capacitor dielectric's unwillingness to accept or give up charge instantaneously. It is commonly and simply modeled as a parasitic series RC (*Figure C*) across the terminals of the main capacitor.

If a charged capacitor is discharged, even through a dead short, some degree of time will be required to remove all of the charge in the parasitic capacitance due to the parasitic series resistance. Conversely, some amount of charge will be absorbed by the parasitic capacitor after a charging of the main capacitor has ceased unless the charge source is maintained for many parasitic RC time constants. Various dielectrics offer differing performance with respect to dielectric absorption. Teflon, polystyrene and polypropylene are quite good, while paper, mylar and glass are relatively poor. Electrolytics are by far the worst offenders. Anyone who has received a shock after discharging a high voltage electrolytic in a television set has experienced the effect of dielectric absorption.

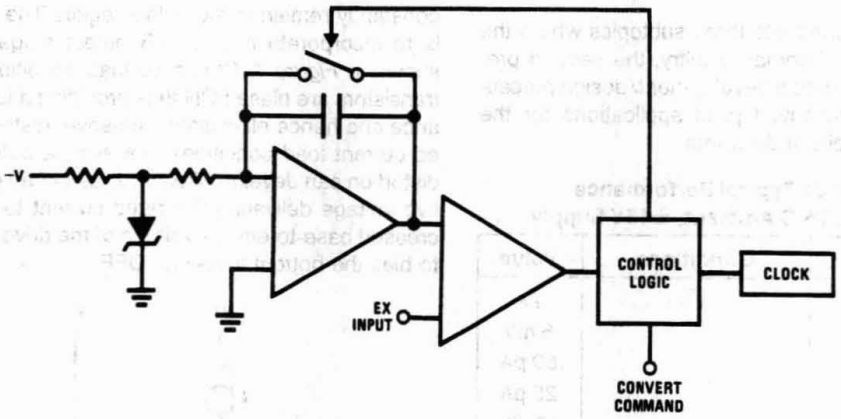

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FIGURE A

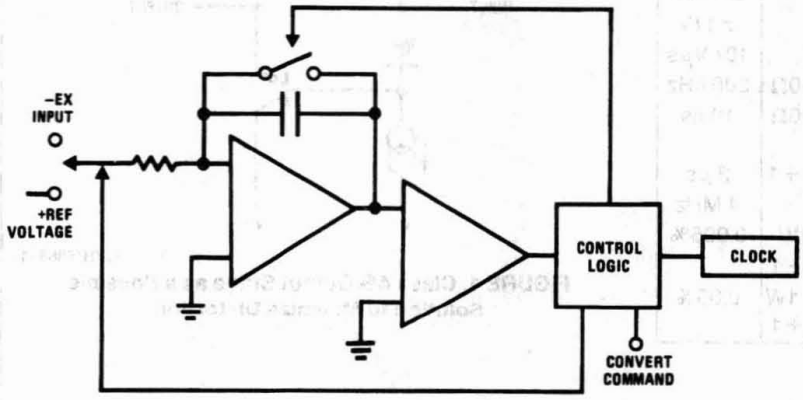
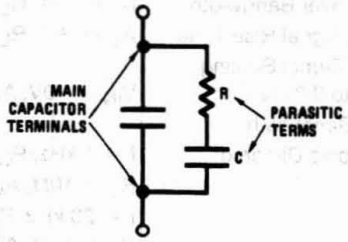


FIGURE B



TL/H/5625–8

FIGURE C

Low Distortion Wideband Power Op Amp

National Semiconductor
Application Note 261

The LH0101 is a power operational amplifier capable of delivering a high-current low-distortion output. The device is conservatively rated at 2 amps continuous current. A novel design technique is used to eliminate the crossover distortion often plaguing power op amps. Additional features include a frequency response from DC to greater than 4 MHz. Excellent DC performance is attained by using FET input devices, and the unity gain frequency compensation has been performed internally. Finally, the device is hermetically sealed in a standard 8-pin TO-3 power package.

The initial LH0101 design goal was to develop an easy to use wideband operational amplifier capable of driving a variety of loads. This requirement focused a major portion of the design effort in the power output stage where considerable emphasis was placed on eliminating crossover distortion. Another consideration was to remove the ground connection typically associated with power amplifiers in order to ease the usage with single or dual power supply configurations.

Our discussion is sectioned into three subtopics where the first details the LH0101 internal circuitry, the second presents a variety of user product development/design precautions, and the third presents typical applications for the LH0101, supported by circuit diagrams.

TABLE I. LH0101 Typical Performance Characteristics at 25°C Ambient, ±15V Supply

Parameter	Conditions	Value
Output Current		2A
Input Offset Voltage		5 mV
Input Bias Current		50 pA
Input Offset Current		25 pA
Input Resistance		$10^{12}\Omega$
Large Signal Voltage Gain		200V/mV
Output Voltage Swing	$R_L = 100\Omega$	±12.5V
	$R_L = 10\Omega$	±11.6V
	$R_L = 5\Omega$	±11V
Slew Rate	$A_V = +1$	10/ Vμs
Full Power Bandwidth	$A_V = +1, R_L = 10\Omega$	300 kHz
Small Signal Rise Time	$A_V = +1, R_L = 10\Omega$	10 ns
Small Signal Settling Time to 0.01%	$V_{IN} = 10V, A_V = +1$	2 μs
Gain Bandwidth		4 MHz
Harmonic Distortion	f = 1 kHz, P_O = 1W	0.005%
	$R_L = 10\Omega, A_V = +1$	
	f = 20 kHz, P_O = 1W	0.05%
	$R_L = 10\Omega, A_V = +1$	

CIRCUIT TOPOLOGY

The LH0101 consists of 3 essential stages, an operational amplifier, a buffer, and a power output stage.

Selection of a BI-FET operational amplifier was prompted by a balance between the desired AC and DC performance. This decision was made in order to take advantage of the high performance BI-FET series' slew rate, settling time, and low bias current characteristics. The added feature of internal frequency compensation aided in making it an ideal amplifier upon which to build.

The zero-crossing distortion associated with high current and high frequency conditions is an age-old problem of class B and class AB power amplifiers. In order to minimize the distortion at crossover, the amplifier must maintain a low output impedance throughout zero crossing. This requires the push-pull output transistors to smoothly alternate current sourcing and sinking duty during the crossover.

To obtain a low output resistance the output stage must constantly remain in the active region. The usual approach is to incorporate a class AB output stage similar to that shown in *Figure 1.* During no load conditions, both output transistors are biased ON thus providing a low output resistance and hence eliminating crossover distortion. Under rated current load conditions, however, a potential source of distortion can develop. Take the case of an output at a positive voltage delivering the rated current to a load. The increased base-to-emitter voltage of the drive transistor tends to bias the bottom transistor OFF.

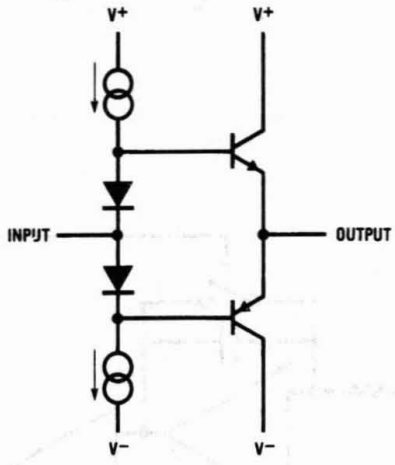


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FIGURE 1. Class AB Output Stage as a Possible Solution to Minimize Distortion

As the output swings negative, crossover distortion can be seen to depend upon how quickly the bottom transistor can turn ON to assume its drive portion of the duty cycle. This condition becomes more acute at higher frequencies.

Of even greater concern is the risk of thermal runaway. An internal rise in temperature decreases transistor junction voltages which in turn increase the collector operating current. Typically emitter degeneration resistors can be used to compensate for this effect, but prove themselves inadequate under rated current load conditions. In order to minimize the junction voltage temperature effect a large resistor value must be selected. At the same time this limits the output drive current and, hence, the output voltage swing. On the other hand, if a small resistor value is selected, the output drive current is maintained but the voltage drop across this small resistance is inadequate to compensate for a decrease in junction voltage. This result brings the problem back to one of thermal runaway and clarifies the shortcomings of *Figure 1.*

Another commonly used technique is a pseudo-class B output stage found in many integrated power op amps, (see *Figure 2*). In this configuration, the limited output swing problem of class AB amplifiers is eliminated. The output swings to within one or two volts of either supply.

The obvious problem with this type of circuit is that it has significant crossover distortion. Distortion occurs when both output transistors are biased completely OFF during zero crossing, thus exhibiting relatively high resistance at the amplifier output. In addition, the minor loop feedback between the base drive of the transistors and the output almost always induces an abrupt change in the response. This further aggravates the amplifier distortion.

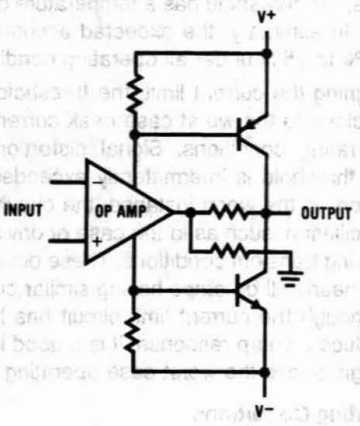

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FIGURE 2. Class B Output Stage

The new op amp successfully combines both techniques to achieve remarkably smooth crossover transitions under most demanding conditions. The complete schematic is shown in *Figure 3.*

The buffer stage, which consists of transistors Q3, Q5, Q10, and Q11 is a current amplifier with unity voltage gain. Connected as a class AB amplifier, its function is to provide distortion-free drive during zero crossing. Bandwidth is in excess of 50 MHz to ensure no bandwidth-induced distortion.

The buffer stage output is current limited by transistors Q7 and Q8 to no more than 50 mA. However, the power stage transistors Q1 and Q2 are designed to turn ON as the load current reaches about 25 mA. Any additional current demanded is sustained by these two output transistors right up to the rated output limit. Thus, the reserve drive of the buffer stage is used only to "smooth" the turn-on delay of the output Darlington transistors.

Q6 and Q9 base-to-emitter junctions are used as current limit sense to protect the output stage. Current sense resistors connected between the supply pins and the SC pins program the limit threshold. In operation, an approximate 0.6V differential turns ON either transistor Q6 or Q9, which in turn drives Q12 and Q4 respectively, starving any excess base current from driving the output beyond the preset limit.

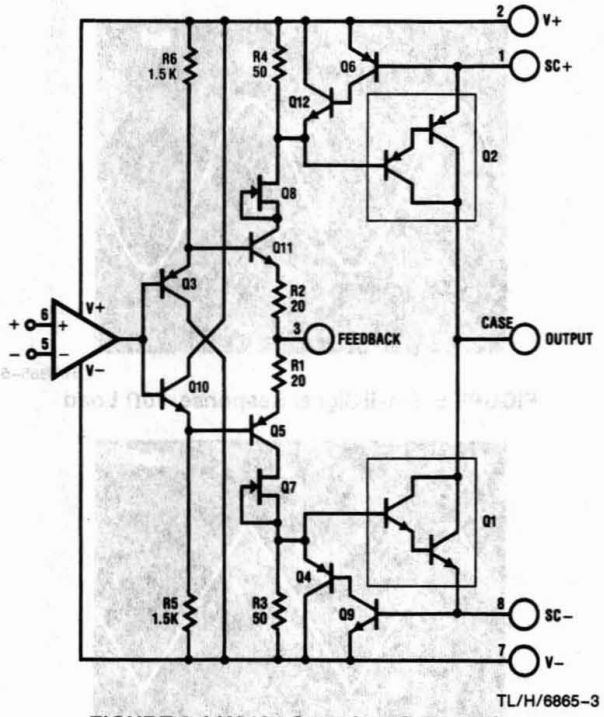

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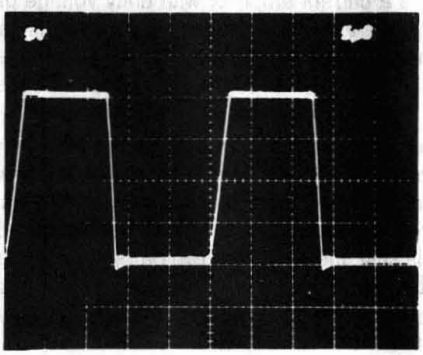
FIGURE 3. LH0101 Complete Schematic

RESULT

The performance of the LH0101 is best demonstrated in the following photographs. *Figure 4* shows the large signal slew response of the LH0101 into a 10Ω load. No crossover distortion is evident.



TL/H/6865–4

FIGURE 4. Large Signal Pulse Response, 10Ω Load

Generally, crossover distortion occurs within a small region near zero crossing. In order to amplify its effect, a signal of small amplitude is used. *Figures 5* and *6* show a signal amplitude of 2 volts peak, and loads of 10Ω and 1Ω respectively. Notice that a slight distortion is observed in *Figure 6,* but only under the extreme condition imposed by the 1Ω load!

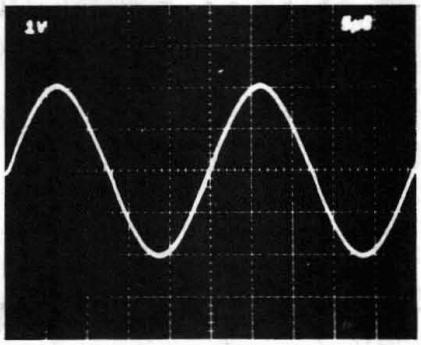


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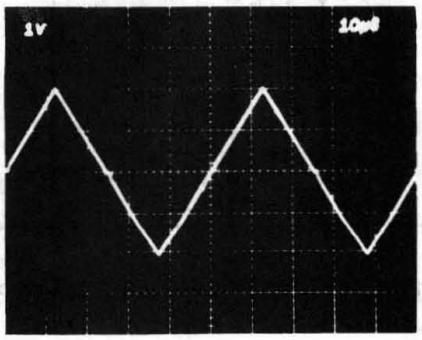
FIGURE 5. Small Signal Response, 10Ω Load



TL/H/6865–6

FIGURE 6. Small Signal Triangular Wave Response, 1Ω Load

DESIGN PRECAUTIONS

Circuit Layout Considerations

In high power applications, one must pay close attention to the trace connections in which high current is carried. Critical connections should be short to minimize line drop. For example, a 10 mΩ PC trace carrying 2 amps develops 20 mV of error voltage. It is important to be aware of where this error is generated and how it impacts accuracy.

Ground connections are probably the most important, if not the most troublesome. Not only can they contribute to circuit error, but in many situations the circuit can become unstable if the layout induces excessive phase error. *Figure 7* shows one correct technique for circuit grounding. The heavy lines represent high current paths. The analog signal ground is returned to the supply common.

Output Current Limit

As described in the previous section, current sense resistors may be inserted between the supply pins and the SC pins to limit excessive load currents. A voltage of 0.6V developed across the sense resistor triggers the limiting circuit. *Figure 8* illustrates the usage.

In cases where the chosen R_{SC} is small ($<1\Omega$), the contact resistances from solder connections and socket ohmic contacts become important and must not be overlooked. A good solder joint typically exhibits 5 mΩ of resistance and socket contacts have about 10 mΩ. Even interconnecting traces will become significant if they are long.

Consider the circuit in *Figure 8*; a pair of good solder joints on the 0.3Ω current sense resistors contribute more than 3% error. Also, one can expect the current sense transistor threshold to vary as much as 10% from device to device. Furthermore, this threshold has a temperature coefficient of −2 mV/°C. In summary, the expected accuracy is on the order of 20% to 25% under all operating conditions.

When designing the current limit, the threshold should not be set too close to the worst case peak current under any normal operating conditions. Signal distortion will occur even if the threshold is intermittently exceeded for a very short duration. In the worst instance, the circuit can trigger spurious oscillation, such as in the case of driving a capacitive load during transient conditions. These occurrences are very real in nearly all op amps having similar current sense circuits. Although the current limit circuit has high enough gain to produce a sharp response, it is a good idea to allow a 20% margin above the worst case operating condition.

Safe Operating Conditions

In order to preserve the reliable performance of the LH0101, the device must not operate beyond the boundary defined in the Safe Operating Area curve in the data sheet. Because of its importance, it has been reproduced in *Figure 9.*

Power Dissipation Considerations

Probably the single most important gauge of reliability is the operating temperature of this device. The derating curve, which has again been reproduced in *Figure 10,* must be followed faithfully. Similar to the Safe Operating Area curve, under no circumstances should the boundary be exceeded.

The curves relate operating and junction temperature, power dissipation and thermal resistance. The general relationship is expresed as follows.

$$P_{DISS} = \frac{T_{J(MAX)} - T_{A(MAX)}}{R_{\theta JC} + R_{\theta CS} + R_{\theta SA}} \quad (1)$$

where: P_{DISS} = the power dissipated by the device in watts.

$T_{J(MAX)}$ = the maximum junction temperature allowed, for the LH0101, $T_{J(MAX)}$ = 150°C.

$T_{A(MAX)}$ = the maximum ambient temperature in °C under which the device must operate.

$R_{\theta JC}$ = thermal resistance from the junction to case in °C/W, for the LH0101, $R_{\theta JC}$ = 2.5°C/W.

$R_{\theta CS}$ = thermal resistance from case to surface of heat sink in °C/W.

$R_{\theta SA}$ = thermal resistance from heat sink to free air ambient in °C/W.

In simple terms, the expression is a measure of how well the internally generated heat is removed such that the power dissipated will not give rise to a maximum permissible junction temperature of 150°C. Thus, the sum of all the thermal resistance represents the thermal efficiency of the mechanical design. The lower the sum, the more efficient the thermal conductivity.

In a typical design, first and foremost is to calculate the maximum power dissipation that the device is designed to handle. There are two components, which are related by the following equation:

$$P_{DISS} = P_Q + P_O \quad (2)$$

The first part of the equation is the quiescent power at which the device operates under no load. The second term is the power dissipated by the output transistors due to the load. This is calculated as the average voltage difference between the supply voltage and the output voltage multiplied by the maximum rms load current the amplifier is required to deliver.

Once the power dissipation is calculated, the next step is to determine the maximum ambient temperature in which the device must operate.

To complete the thermal design, all contributions of thermal resistances must be summed per equation (1) above. First, the junction-to-case thermal resistance for the LH0101 is given in the data sheet; it is typically 2.5°C/W.

The metal case of the LH0101 is electrically connected to the output of the amplifier. Unless the application permits direct mounting to a heat sink, a sheet of insulation should be sandwiched between the case and the mounting surface for isolation purposes. Many types of insulators are available. The most popular of these is mica film. Its thermal resistance is listed in Table II along with other types.

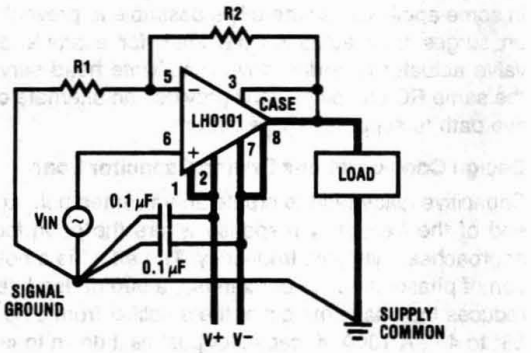


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FIGURE 7. Proper Supply Connection

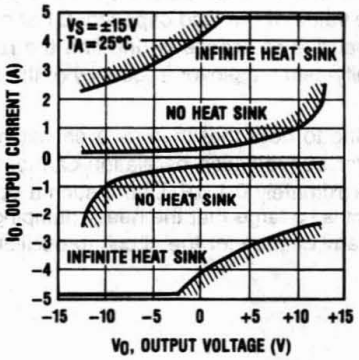

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FIGURE 9. Safe Operating Area

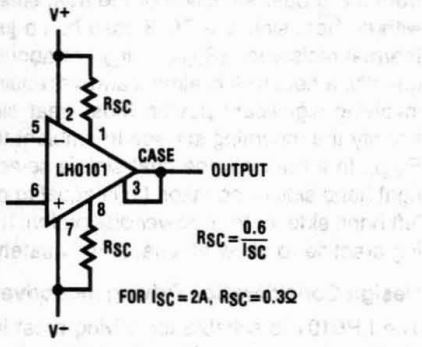

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FIGURE 8. Current Limit Protection

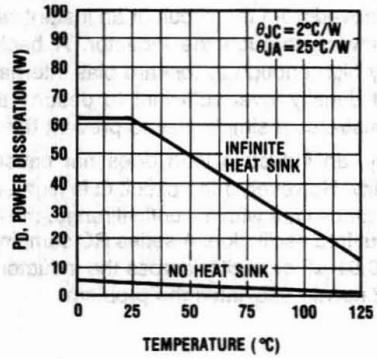

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FIGURE 10. Power Derating Curve

TABLE II. Thermal Resistance (Note 1)

Insulator Material Type	W/O Thermal Joint Compound	W/Thermal Joint Compound	Sources
Mica	1.3°C/W @ 0.003″ thick	0.25°C/W	Thermalloy Inc.
	1.2°C/W @ 0.002″ thick	0.33°C/W	Keystone Electronics Mod. #4658
Thermalfilm I[2]	1.5°C/W @ 0.002″ thick	0.52°C/W	Thermalloy Inc.
Aluminum Oxide[2]	1.0°C/W @ 0.062°C	0.3°C/W	
Beryllium Oxide[2-3]	0.6°C/W @ 0.062″ thick	0.15°C/W	
Insul-Cote[2]	0.5°C/W @ 0.002″ thick		Thermalloy Inc.

Note 1: Mounting bolts torqued to 6 oz.-in.

Note 2: Consult manufacturer on availability for 8-lead TO-3 package style.

Note 3: Particle, dust, or fumes present health hazards when inhaled. Grinding, sanding, and pulverizing the material should be avoided.

In critical applications, thermal-joint compound should be used to maximize heat transfer across the case to the heat sink. With air being a poor heat conduction medium, the use of thermal joint compound eliminates air gaps between mounting surfaces, thus providing more than 3 times improvement in thermal efficiency over those cases without.

The remaining unknown, $R_{\theta SA}$, can now be determined from the proper selection of the heat sink. By itself, that is, with no heat sink, the TO-3 case has a junction-to-ambient thermal resistance ($R_{\theta JA}$ or θ_{JA}) of about 25°C/W. Consequently, a heat sink is almost always required in applications involving significant power. Most heat sink manufacturers specify the mounting-surface to ambient thermal resistance $R_{\theta SA}$. In a nutshell, the heat sink is selected such that the right hand side of equation (1) is equal to or greater than the left hand side, or total power dissipation. It is good engineering practice to allow at least a 10% safety margin.

Design Consideration Driving Inductive Load

The LH0101 is suitable for driving most inductive loads including voice-coils and motors. However, in many situations the device should be protected from the harmful effects of energy stored in the inductor. Such a condition exists when power is removed from the circuit at an instant when a high current is flowing through the inductor. A back-emf may have energy high enough to forward bias internal junctions at a current density level sufficient to destroy the device. *Figure 11* illustrates a simple way to prevent this.

Theoretically, an inductive load does not cause amplifier loop instability. However, if the circuit Q is high enough and stray capacitances are within a critical range, the load circuit can break out into oscillation. A series RC damping circuit of 10Ω and a 0.01 μF capacitor across the inductor as shown in *Figure 12* usually alleviates the problem.

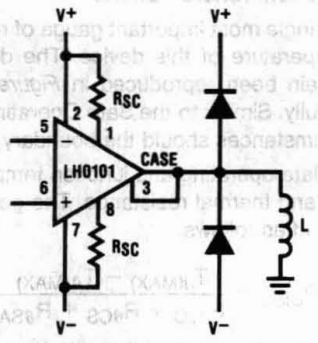

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FIGURE 11. Back EMF Suppression Technique

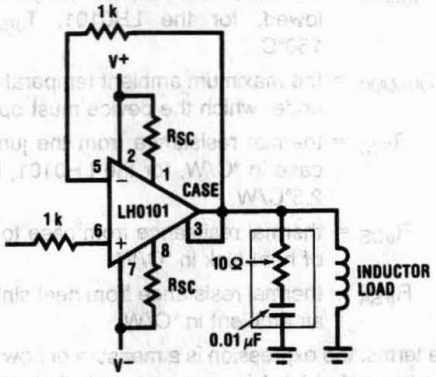

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FIGURE 12. RC Damping to Compensate Inductor Load

In some applications where it is desirable to prevent power-on surges from actuating the load, for example a motor valve actuator or a disk drive read/write head servo loop, the same RC damping circuit provides an alternate conductive path to suppress surge current.

Design Considerations Driving Capacitor Load

Capacitive loads tend to create an unwanted pole at the tail end of the frequency response where the open loop gain approaches unity gain frequency. The effect is a net reduction of phase margin. For example, a 500 pF load capacitor reduces the phase margin of the amplifier from a no load of 58° to 45°. A 1000 pF capacitor pushes it down to 40°. With a large 0.01 μF capacitor, the amplifier has a mere 22° phase margin. The latter cases are susceptible to oscillation. *Figure 13* shows a compensation technique to restore stability. The value of the lead capacitor C1 should be such that the capacitive reactance is one-fifth the resistance of R2 at the unity-gain crossover frequency of the amplifier, or 4 MHz.

It is interesting to note that there is a critical value for the load capacitor above which oscillation cannot occur. That value is approximately 0.1 μF. Under such a condition, the time constant is so large that the heavy damping effectively suppresses any chance for the circuit to oscillate.

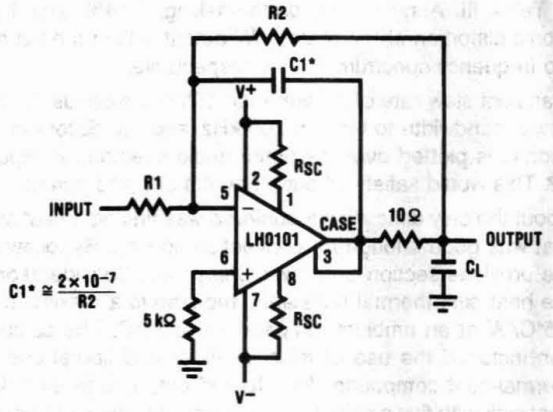

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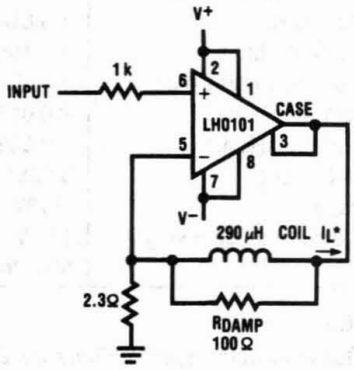
FIGURE 13. Compensation for Capacitance Load

TYPICAL APPLICATIONS

CRT Yoke Driver

One of the most natural applications for the LH0101 op amp is the deflection yoke driver for high resolution CRTs. The low distortion characteristics allow virtually unrestricted use in any circuit configuration. A typical design is shown in *Figure 14.*



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*Coil Current I_L Measured with
Tektronix Current Probe Model P6042.

FIGURE 14. CRT Yoke Driver Circuit

A 500 mV peak-to-peak triangular waveform about ground is input to the amplifier, giving rise to a 100 mA peak current to the inductor. As shown in *Figures 15* and *16,* the responses were recorded at 60 Hz and 20 kHz respectively. At higher frequencies, R_{DAMP} becomes important. The value should be selected to yield the cleanest waveform.

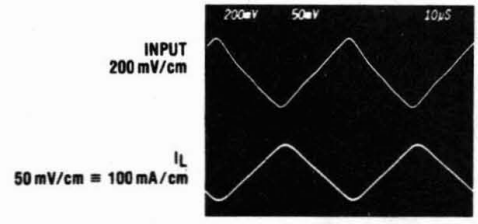

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FIGURE 15. 60 Hz Current Drive Waveform of CRT Deflection Coil

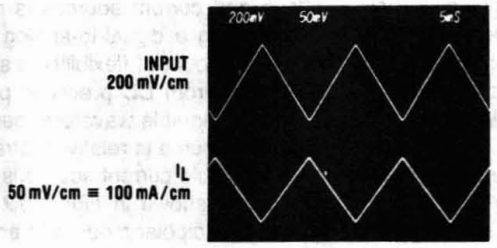

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FIGURE 16. 20 kHz Current Drive Waveform of CRT Deflection Coil

Servo Motor Amplifier

A typical motor driver circuit is shown in *Figure 17.* The amplifier will deliver the rated current into the motor. Again, care should be taken to keep power dissipation within the permitted level.

A variation of the same servo design is shown in *Figure 18.* This precision speed regulation circuit employs rate feedback for constant motor current at a given input voltage.

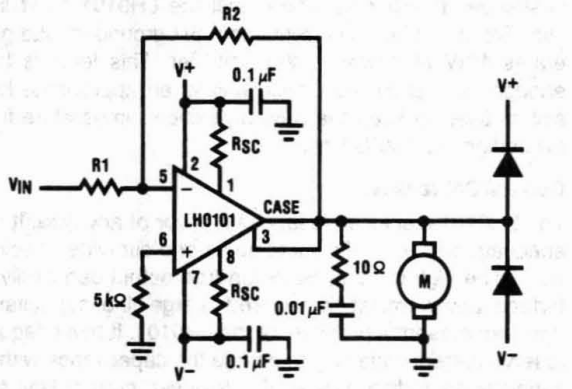

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FIGURE 17. Servo Motor Amplifier

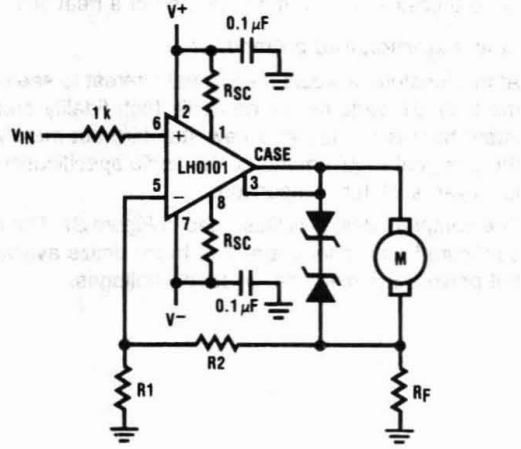

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FIGURE 18. Rate Feedback Servo Motor Amplifier

Digitally Programmable Power Source

Designing precision voltage and current sources is made simple using the LH0101. Adding a digital-to-analog converter provides a tremendous amount of flexibility in speed and control. Applications range from DC precision power supplies to sophisticated programmable waveform generators. The design of the voltage source is relatively straightforward, whereas the programmable current source is a bit more involved. Such a circuit is shown in *Figure 19.* The DAC is configured to operate in a bipolar mode with an output range of ±10.000V. With 12 bits, the DAC outputs an equivalent of 4.88 mV per bit-weight. Consequently, the resolution at the current source is 0.488 μA/bit.

The output sources and sinks current only to ground referenced loads. A negative full-scale code (all digital inputs low) effects a negative (source) 1 amp current output. A zero scale (MSB low and all other bits high) gives zero current. And a positive full scale code (all digital inputs high) forces a positive (sink) 1 amp current at the output.

The versatility of this circuit configuration is not without limitation. Because the output voltage is dependent upon the ground referred load, one must be aware of the potentially destructive power dissipation level the LH0101 must sustain. For example, 1A current into a 5Ω grounded load generates 10W of power in the amplifier. This level is high enough to destroy the device unless an appropriate heat sink is used to keep the device junction temperature from exceeding the 150°C limit.

Coaxial Cable Driver

The LH0101 makes an ideal cable driver of any type. It has adequate bandwidth for most audio and sub-video applications. The high current, distortion free output can easily interface any termination required. Large line capacitance does not present a problem for the LH0101. It has adequate reserve current capability to charge the capacitance without seriously degrading bandwidth. However, current limit protection against cable shorts is recommended. A typical interface circuit is shown in *Figure 20.* The op amp can drive up to 6 coaxial lines without the use of a heat sink.

Low Distortion Audio Amplifier

At this juncture, it would be of great interest to see how well the LH0101 performs in the audio high fidelity arena. The intent here is not to set a new standard but merely to use the stringent requirements of the audio specifications as an ideal yardstick for comparison.

The complete design is illustrated in *Figure 21.* The circuit is configured as a bridge amplifier to maximize available output power for a given set of supply voltages.

The result is an impressive set of specifications summarized in Table III. Although not earth-shaking, 0.14% total harmonic distortion at the rated 40W output, within the full audio frequency spectrum, is very respectable.

Transient slew rate of greater than 10V/μs extends the full power bandwidth to beyond 200 kHz, and the distortion response is plotted over the entire audio spectrum in *Figure 22.* This would satisfy all but a handful of audio purists.

About the only difficulty encountered was finding a heat sink that was good enough for convection cooling. By following the previous section on Power Dissipation Considerations, the heat sink thermal resistance required is a maximum of 3.5°C/W at an ambient temperature of 25°C. The calculation included the use of mica insulator and liberal use of thermal-coat compound. As it turned out, a large extruded heat sink with fins similar to the Thermalloy type 6141 did an excellent job of keeping the junctions cool.

TABLE III. Bridge Audio Amplifier Specifications

A_V (Voltage Gain)	3
Z_{IN} (Input Impedance)	10 kΩ
I_q (Quiescent Current)	60 mA
P_O (Output Power)	40 Watts into 8Ω
—RMS Continuous 20 Hz–20 kHz	28 Watts into 16Ω
Full Power Bandwidth	DC to >100 kHz
THD (Total Harmonic Distortion)	
1W 20–20,000 Hz	<0.8%
40W 20–20,000 Hz	<0.15%
IMD (Intermodulation Distortion)	
1W 60 Hz/100 kHz 4:1	<0.01%
40W 60 Hz/100 kHz 4:1	<0.002%
Peak Output Current	3.125A into 8Ω
Supply Voltage	±18V
Maximum Output Voltage Swing	21.2V rms
	30V Peak

REFERENCES

1. National Semiconductor, *Special Functions Databook.*
2. National Semiconductor, *Linear Applications Handbook.*
3. J. Wong, J. Sherwin, "Applications of Wide-Band Buffer Amplifier", National Semiconductor AN-227, October 1979.
4. National Semiconductor "LH0101 Power Operational Amplifier" data sheet.

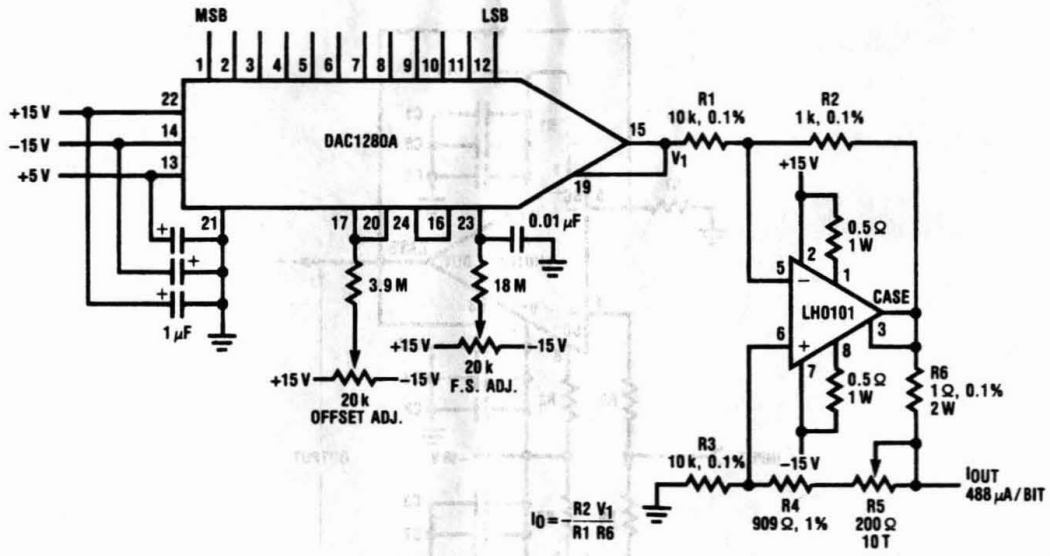

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FIGURE 19. Digitally Programmable Current Source

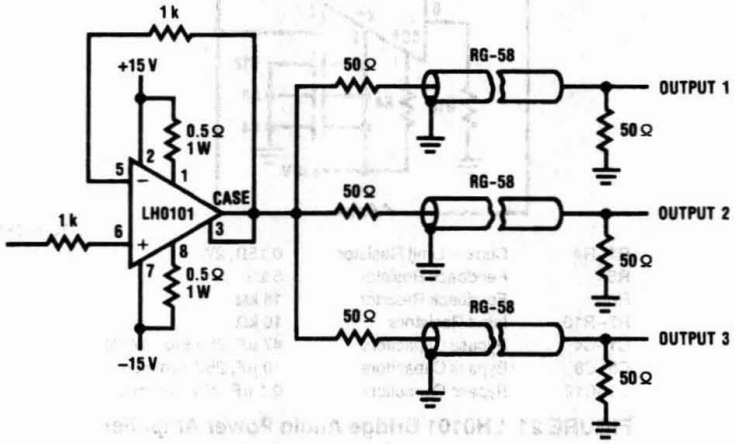

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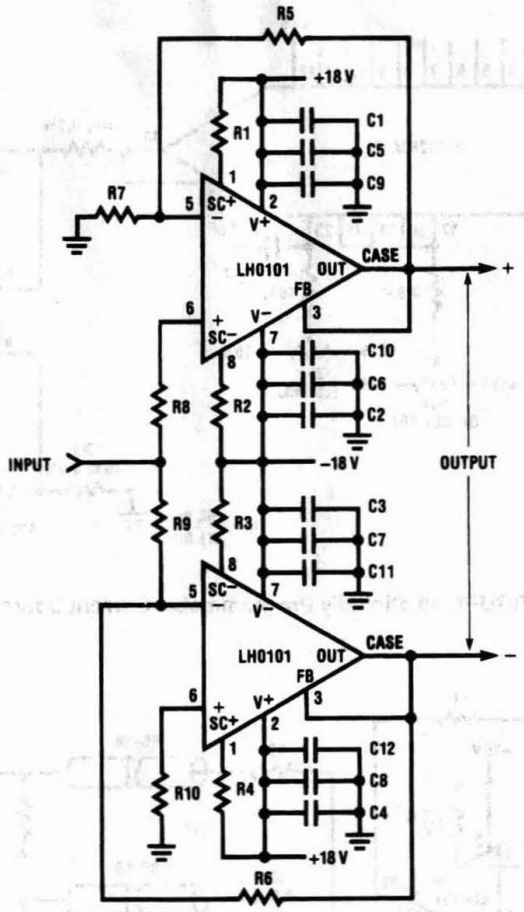
FIGURE 20. Multi-Line Coaxial Cable Driver



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R1–R4	Current Limit Resistor	0.15Ω, 2W
R5	Feedback Resistor	5 kΩ
R6	Feedback Resistor	15 kΩ
R7–R10	Input Resistors	10 kΩ
C1–C4	Bypass Capacitors	47 μF, 25V Electrolytic
C5–C8	Bypass Capacitors	10 μF, 25V Tantalum
C9–C12	Bypass Capacitors	0.1 μF, 25V Ceramic

FIGURE 21. LH0101 Bridge Audio Power Amplifier

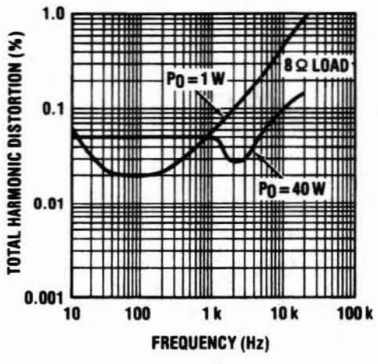

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FIGURE 22. Total Harmonic Distortion vs Frequency of Bridge Power Amplifier

Applying Dual and Quad FET Op Amps

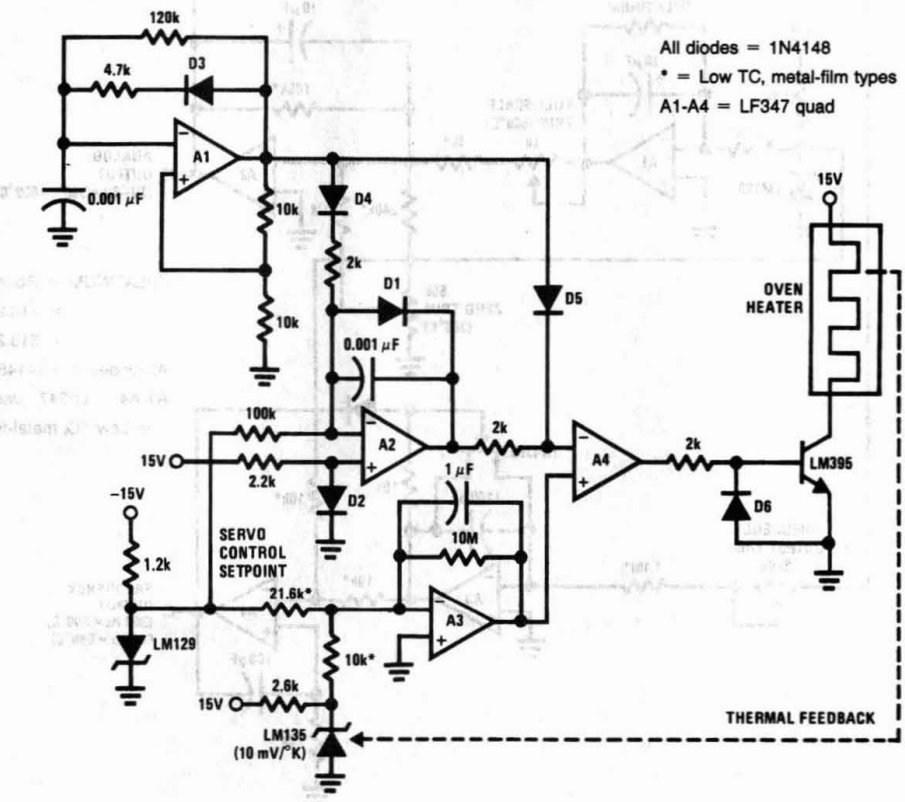
National Semiconductor
Application Note 262

The availability of dual and quad packaged FET op amps offers the designer all the traditional capabilities of FET op amps, including low bias current and speed, and some additional advantages. The cost-per-amplifier is lower because of reduced package costs. This means that more amplifiers are available to implement a function at a given cost, making design easier. At the same time, the availability of more amplifiers-per-dollar means that relatively self contained and sophisticated functions can be designed around a single FET dual or quad package. In addition, duals and quads require less board space, fewer bypass capacitors and less power supply bussing. An inventive designer can capitalize on all of these advantages to produce complex circuit functions at low cost. An example is shown in *Figure 1*.

HIGH EFFICIENCY PRECISION OVEN TEMPERATURE CONTROLLER

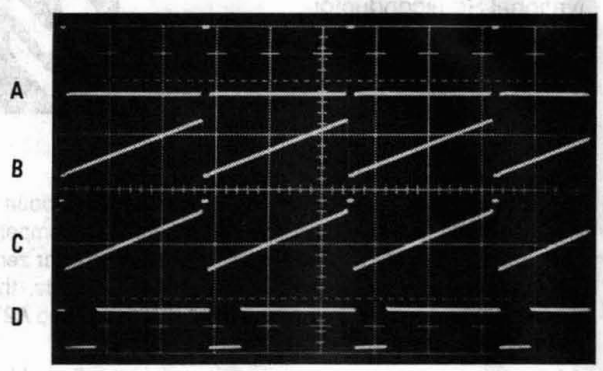
In this circuit, a complete, high efficiency pulse width modulating temperature controller is built around a single LF347 package. In *Figure 1*, A1 functions as an oscillator whose output (Trace A, *Figure 2*) periodically resets the A2 integrator output (Trace B, *Figure 2*) back to zero volts. Each time A1's output goes high, a large positive current is forced into A2's summing junction, overcoming the negative current that flows through the 100 kΩ resistor into the LM129 reference. This forces A2's output to head in a negative-going direction ultimately limited by the diode feedback-bound. Another diode provides bias at A2's "+" input to compensate the bound diode and A2's output settles very near zero volts. When the positive output pulse from A1 ends, the positive current into A2's summing junction ceases and A2's output ramps linearly until the next reset pulse.

A3 functions as a current summing servo-amplifier which compares the currents derived from the LM135 temperature sensor and the LM129 reference. In this example A3 operates at a gain of 1000 with a 1 μF capacitor providing 0.1 Hz servo response. A3's output represents the amplified difference between the LM135's temperature and the desired control setpoint, which may be varied by altering the 21.6k value. In this circuit the 21.6k resistor provides a setpoint of 49°C. A3's output is compared to the ramp output of A2 and A4, which is set up as a comparator. A4's output will only be high during the time A3's output is greater than the ramp voltage. The ramp reset pulse is diode-summed with the ramp output (Trace C, *Figure 2*) at A4 to prevent A4's output from going high during the period of the reset pulse. A4's output biases the LM395 power transistor which switches power to the heater (Trace D, *Figure 2*). If the LM135 sensor is tightly coupled to the heater and the oven is well insulated, this controller will easily hold 0.05°C over wide excursions of ambient temperature.



TL/H/6932–1

FIGURE 1. Connecting appropriate components to an LF347 quad FET op amp IC produces a high efficiency precision oven temperature controller. This design can hold a temperature within 0.05°C despite wide ambient temperature fluctuations.



TL/H/6932–2

Trace	Vertical	Horizontal
A	20V/Div	
B	10V/Div	50 μs/Div
C	10V/Div	
D	20V/Div	

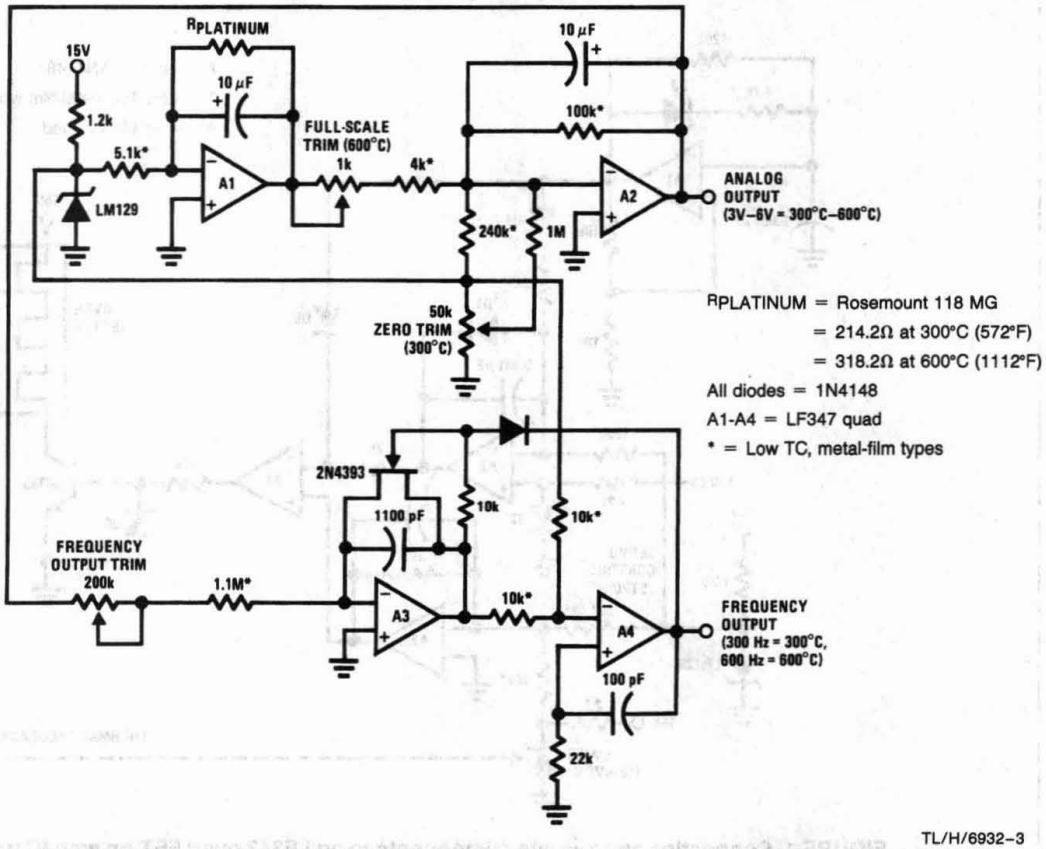
FIGURE 2. Oven-controller waveforms from *Figure 1's* circuit show A1's oscillator output (Trace A) and A2's integrator output (B) as the latter resets periodically to 0V. Trace C displays A4's ramp input, and (D) indicates the LM395's power input to the oven heater.

PLATINUM RTD HIGH TEMPERATURE THERMOMETER WITH ANALOG AND DIGITAL OUTPUTS

Another temperature related circuit appears in *Figure 3*. In this circuit an LF347 is used to signal condition a Platinum RTD and provide simultaneous analog and frequency outputs. These outputs are accurate to ±1°C over a range of 300°C–600°C (572°F–1112°F). Although the circuit maintains linearity over a much wider range the non-linear response of the RTD over wide range is the limitation to accurate, wide range operation (see graph, *Figure 4*).

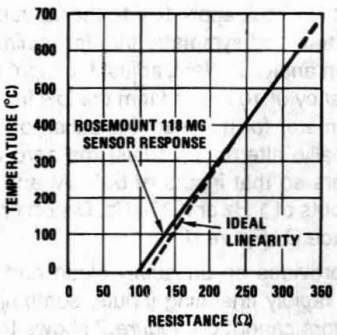
A1 functions as a negative gain inverter to drive a constant current through the platinum sensor. The LM129 and the 5.1k resistor provide the current reference. Because A1 operates at negative gain the voltage across the sensor is extremely low and self-heating induced errors are eliminated. A1's output potential, which varies with the platinum sensor's temperature, is fed to A2. A2 provides scaled gain and offsetting so that its output will swing from 3.00V to 6.00V for a 300°C to 600°C temperature swing at the platinum sensor.

A3 and A4 form a voltage-to-frequency converter which generates a 300 Hz to 600 Hz output from A2's 3V to 6V analog output. A3 integrates in a negative-going direction at a slope which is linearly dependent upon A2's output voltage. A4 compares A3's negative ramp to the LM129's positive reference voltage by current summing in the 10 kΩ resistors. When the negative value of the ramp just exceeds the LM129 voltage A4's output goes positive, turning on the 2N4393 FET and resetting the A3 integrator. AC feedback at A4 causes it to "hang up" in the positive state long enough to completely discharge the integrator capacitor.



TL/H/6932–3

FIGURE 3. Generate simultaneous analog level and frequency outputs using one LF347 package by signal-conditioning a platinum RTD sensor. You can calibrate this high temperature (300°C to 600°C) measuring circuit to ±1°C by using three trimming pots.



TL/H/6932–4

Temperature(°C)	Resistance(Ω)
600	318.2
500	284.7
400	249.8
300	219.2
200	177.3
100	139.2
0	100.0

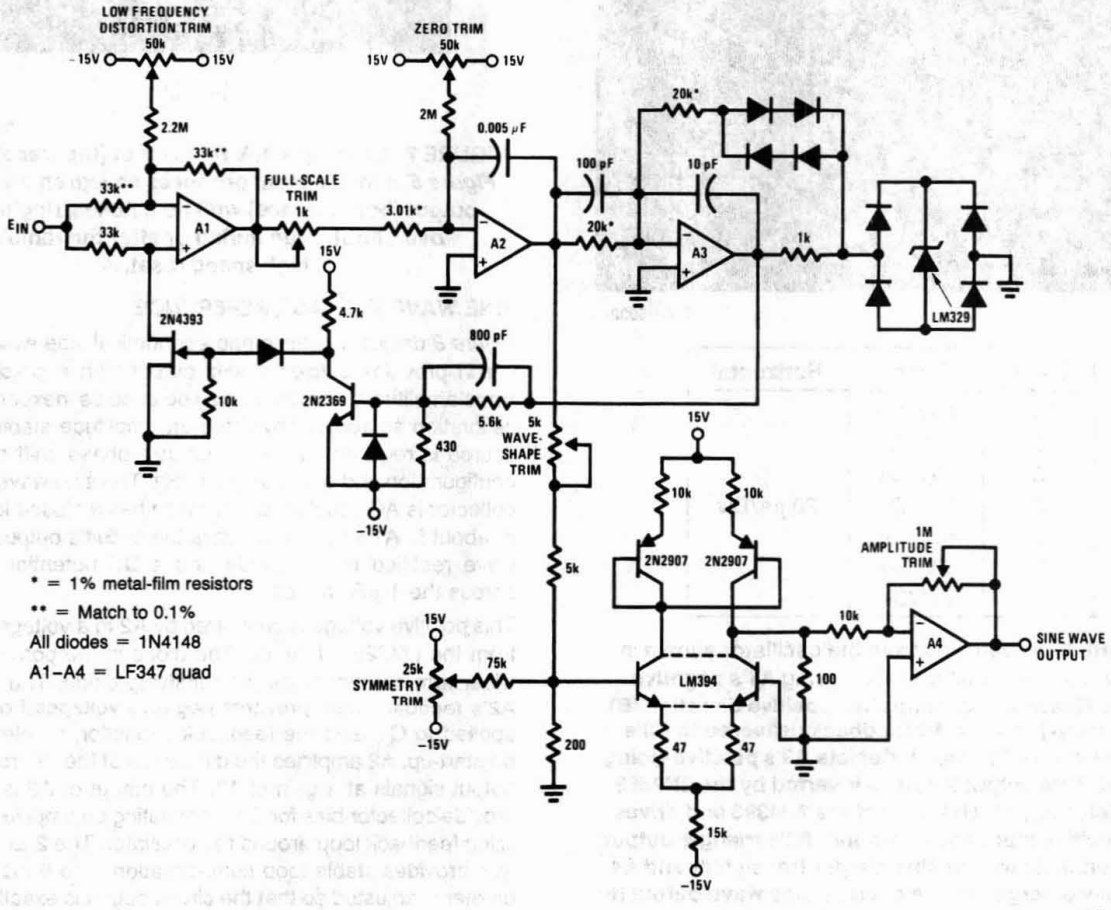
FIGURE 4. A platinum RTD sensor's resistance decreases linearly from 600°C to 300°C. Then, from 300°C to 0°C, the sensor's resistance deviates from a straight line slope and degrades the *Figure 3* circuit's accuracy beyond ± 1°C.

To calibrate this circuit, substitute a high quality decade box (e.g., General Radio #1432-K) for the sensor. Alternately adjust the zero (300°C) and full-scale (600°C) potentiometers for the resistance values noted in *Figure 4* until A2's output is calibrated. Next, adjust the 200 kΩ frequency output trim so the frequency output corresponds to the analog value at A2's output.

VOLTAGE CONTROLLED SINE WAVE OSCILLATOR

Figure 5 diagrams a very high performance voltage controlled sine wave oscillator which uses a single LF347 package. For a 0V–10V input the circuit produces sine wave outputs of 1 Hz to 20 kHz with better than 0.2% linearity. In addition, distortion is about 0.4% and the sine wave output frequency and amplitude settle instantaneously to a step input change. The circuit's sine wave output is achieved by non-linearly shaping the triangle wave output of a voltage-to-frequency converter.

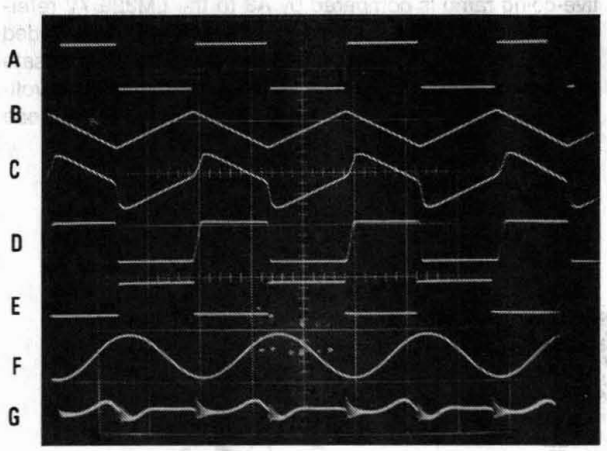
Assume the 2N4393 FET is on and A1's output has just gone low. With the FET on, A1's "+" input is grounded and A1 functions as a unity gain inverter. In this state its output will be equal to $-E_{IN}$ (Trace A, *Figure 6*). This negative voltage is applied to the A2 integrator which responds by ramping in a positive direction (Trade B, *Figure 6*). This positive-going ramp is compared by A3 to the LM329 7V reference which is contained within its symmetrically bounded positive feedback loop. The paralleled diodes compensate the diodes in the bridge. When the positive-going ramp voltage just nulls out the −7V produced by the LM329, diode



TL/H/6932–5

FIGURE 5. An LF347-based voltage-controlled sine wave oscillator combines high performance with versatility. For 0V to 10V inputs, this circuit generates 1 Hz to 20 kHz outputs with better than 0.2% linearity and only 0.4% distortion.

bound A3's output goes positive (Trace D, *Figure 6*). The 100 pF capacitor provides a frequency adaptive trim to A3's trip point, aiding V/F linearity at high frequencies by compensating A3's relatively slow response time when used as a comparator. The 10 pF capacitor provides AC positive feedback to A3's positive input (Trace C, *Figure 6*). The positive output of A3 is inverted by the 2N2369 transistor which also has the effect of further shortening A3's response time. It does this by using a heavy feed-forward capacitor in its base drive line. This allows the transistor to complete switching just barely after the A3 output has begun to move! (Trace E, *Figure 6*). The 2N2369's negative output turns off the 2N4393 FET. This lifts A1's "+" input from ground and causes A1 to become a unity gain follower. This forces A1's output to immediately slew to the value of E_{IN}. This causes the A2 integrator to reverse in direction, forming a triangle wave. When A2 ramps far enough negative A3 will again switch and the entire cycle will repeat. The triangle output at A2 is fed to the discrete transistors which form a sine shaper. This configuration uses the logarithmic relationship between collector current and V_{BE} in transistors to smooth the triangle wave. The last amplifier in the quad package provides gain and buffering and furnishes the sine wave output (Trace F, *Figure 6*).



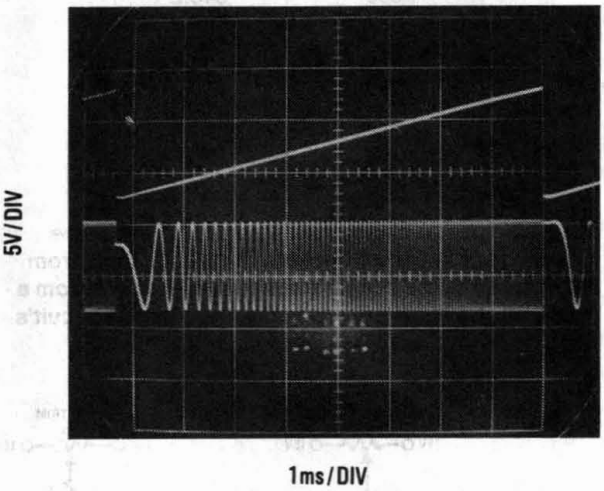
TL/H/6932-6

Trace	Vertical	Horizontal
A	20V/Div	
B	20V/Div	
C	10V/Div	
D	20V/Div	20 μs/Div
E	50V/Div	
F	2V/Div	
G	0.2VDiv	

FIGURE 6. Waveforms from the oscillator shown in *Figure 5* show that upon receiving A1's negative voltage (Trace A), A2 ramps in a positive direction (B). This ramp joins the AC feedback delivered to A3's positive input (C); Trace D depicts A3's positive-going output. This output in turn is inverted by the 2N2369 transistor (E), which turns off the 2N4393 and drives A1's positive input above ground. A2's triangle output also connects to four sine-shaper transistors and A4 and finally emerges as the circuit's sine wave output (F). A distortion analyzer's output (G) shows the circuit's minimum distortion products after trimming.

To calibrate the circuit apply 10V to the input and adjust the wave shape trim and symmetry trim for minimum distortion on a distortion analyzer. Next, adjust the input voltage for an output frequency of 10 Hz and trim the low frequency distortion potentiometer for minimum indication on the distortion analyzer. Finally, alternately adjust the zero and full-scale potentiometers so that inputs of 500 μV and 10V yield respective outputs of 1 Hz and 20 kHz. Distortion products are shown in Trace G, *Figure 6*.

This circuit provides an unusually clean and wide ranging response to rapidly changing inputs, something most sine wave oscillators cannot do. *Figure 7* shows the circuit's response to a 10V ramp applied to the input. The output is singularly clean, with no untoward dynamics, even during or following the high speed reset of the ramp.



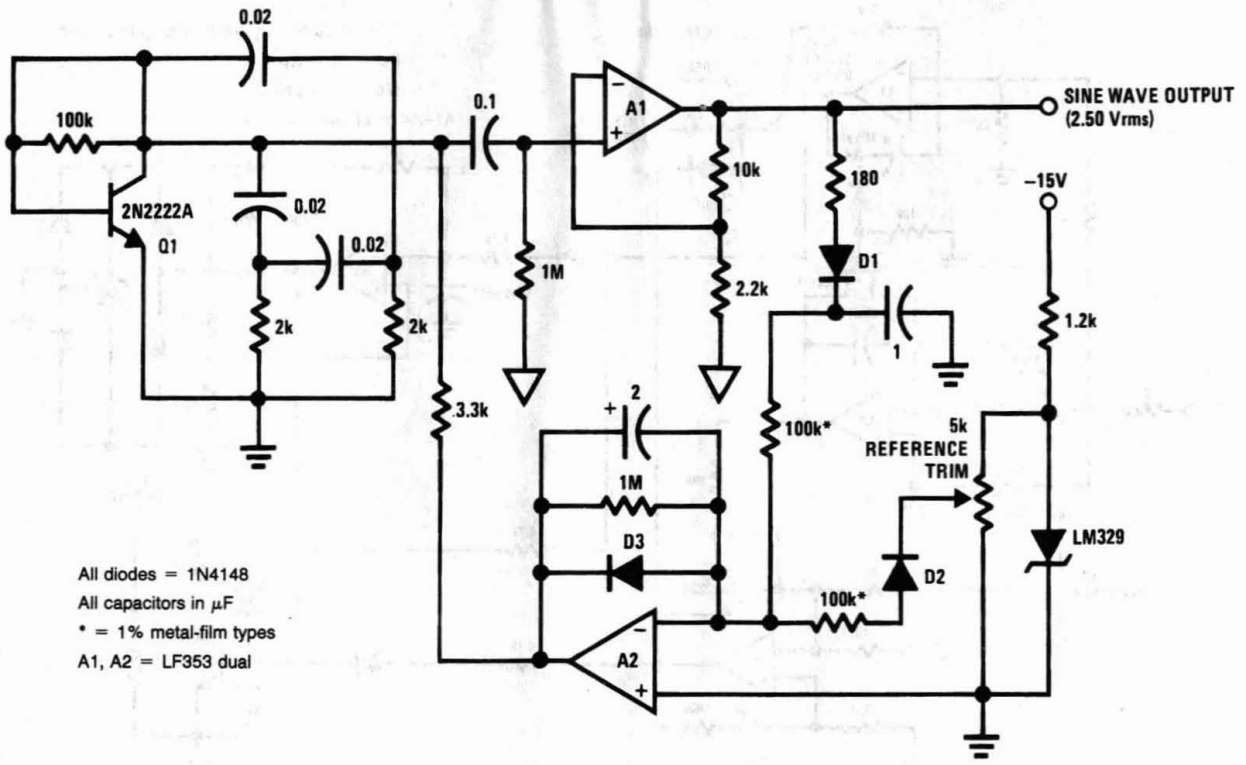
TL/H/6932-7

FIGURE 7. Applying a 10V ramp input (top trace) to the *Figure 5* circuit's input produces an extremely clean output (bottom trace) with no glitches, ringing or overshoot, even during or after the ramp's high speed reset.

SINE WAVE VOLTAGE REFERENCE

Figure 8 depicts a simple and economical sine wave circuit which provides a fixed 1 kHz output with a precise 2.50 Vrms amplitude. The circuit may be used as inexpensive AC calibration source or anywhere an amplitude stabilized AC source is required. Q1 is set up in a phase shift oscillator configuration and oscillates at 1 kHz. The sine wave at Q1's collector is AC coupled to A1, which has a closed loop gain of about 5. A1's output, which is the circuit's output, is half-wave rectified by the diode and a DC potential appears across the 1 μF capacitor.

This positive voltage is compared by A2 to a voltage derived from the LM329 reference. The diode in the potentiometer wiper arm compensates the rectifying diode. The diode in A2's feedback loop prevents negative voltages from being applied to Q1 (and the feedback capacitor, an electrolytic) on start-up. A2 amplifies the difference of the reference and output signals at a gain of 10. The output of A2 is used to provide collector bias for Q1, completing an amplitude stabilizing feedback loop around the oscillator. The 2 μF electrolytic provides stable loop compensation. The 5 kΩ potentiometer is adjusted so that the circuit output is exactly 2.50V. This output will show less than 1 mV shift for ±5V variation in either supply. Drift is typically 250 μV/°C and distortion is inside 1%.



TL/H/6932-8

FIGURE 8. Reduce parts count and save money by basing this precision sine wave voltage reference on an LF353 dual FET op amp IC. This circuit generates a 1 kHz sine wave at 2.50 Vrms. The 2N2222A transistor functions as a phase-shift oscillator. The A1, A2 combination amplifies and amplitude stabilizes the circuit's sine wave output.

ANALOG-TO-DIGITAL CONVERTER

An extremely versatile integrating analog-to-digital converter appears in *Figure 9*. A single LF347 quad implements the A/D converter which can be either internally or externally triggered. As shown, the converter provides a 10-bit serial output word with a 10 ms full-scale conversion time.

To understand this circuit assume the mode select switch is in the "free run with delay" position and the 2N4393 FET has just been turned off. The A2 integrator, biased from the LM129 reference, begins to ramp in a negative-going direction (Trace B, *Figure 10*). The 2N2222A transistor provides a −0.6V or a +7V feedback output bound for A4, keeping its output from saturating and aiding high speed response. AC positive feedback assures clean transitions. A3 is set up as a 100 kHz oscillator. The LM329 and the diodes provide a temperature compensated bipolar switching threshold reference for the oscillator. During the time A4 is low the pulses from A3's output are passed by the 2N3904 transistor. When A4 goes high the 2N3904 is biased on and no more pulses appear (Trace D, *Figure 10*). Since A2's output ramp is linear the length of time A4 spends low is directly proportional to the value of E_{IN}. The number of pulses at the 2N3904 output provides a digital indication of this information. A2's ramp continues to run after A4 goes high and the actual conversion ends. When the time constant associated with the "free run with delay" mode charges to 2V A1's output goes high (Trace A, *Figure 10*), turning on the 2N4393 FET, which resets the integrator. A1 stays high until the AC feedback provided by the 150 pF capacitor decays below 2V. At this point A1 goes low, A2 begins to ramp and a new conversion cycle starts. False data at the converter output is prevented during the time A1 is high by resistor diode gating at the 2N3904 base.

Normally, a ±1 count uncertainty at the output will be introduced because the 100 kHz clock runs asynchronously with the conversion cycle. This problem is eliminated by the diode and 4.7k resistor which run between A1's output and the A3 negative input. These components force the oscillator to synchronize to the conversion cycle at each falling edge of A1's output. The length of time between conversions in the "free run with delay" mode is adjustable by varying the RC combination associated with this switch position. The converter may be triggered externally by any source with a greater than 2V amplitude. In the "free run" mode the converter self triggers immediately after A4 goes high. Thus, the conversion time will vary with the input voltage.

This is graphically illustrated in the photo of *Figure 11*. Here, a positive biased sine wave (Trace B, *Figure 11*) is fed into the A/D input. Because the A/D resets and self triggers immediately after converting, the A2 ramp output shapes a ramp constructed envelope of the input signal (Trace C, *Figure 11*). Trace A shows this in time expanded form. Note that the −120 ppm/°C temperature coefficients of the Polystyrene capacitors in the integrator and oscillator will tend to track, aiding drift performance in this circuit. From 15°C to 35°C this circuit achieves 10-bit absolute accuracy. To calibrate this circuit apply 10.00V to the input and adjust the FS trim for 1000 pulses out per conversion. Next, apply 0.05V and adjust zero trim for 5 pulses out per conversion. Repeat this procedure until the adjustments converge.

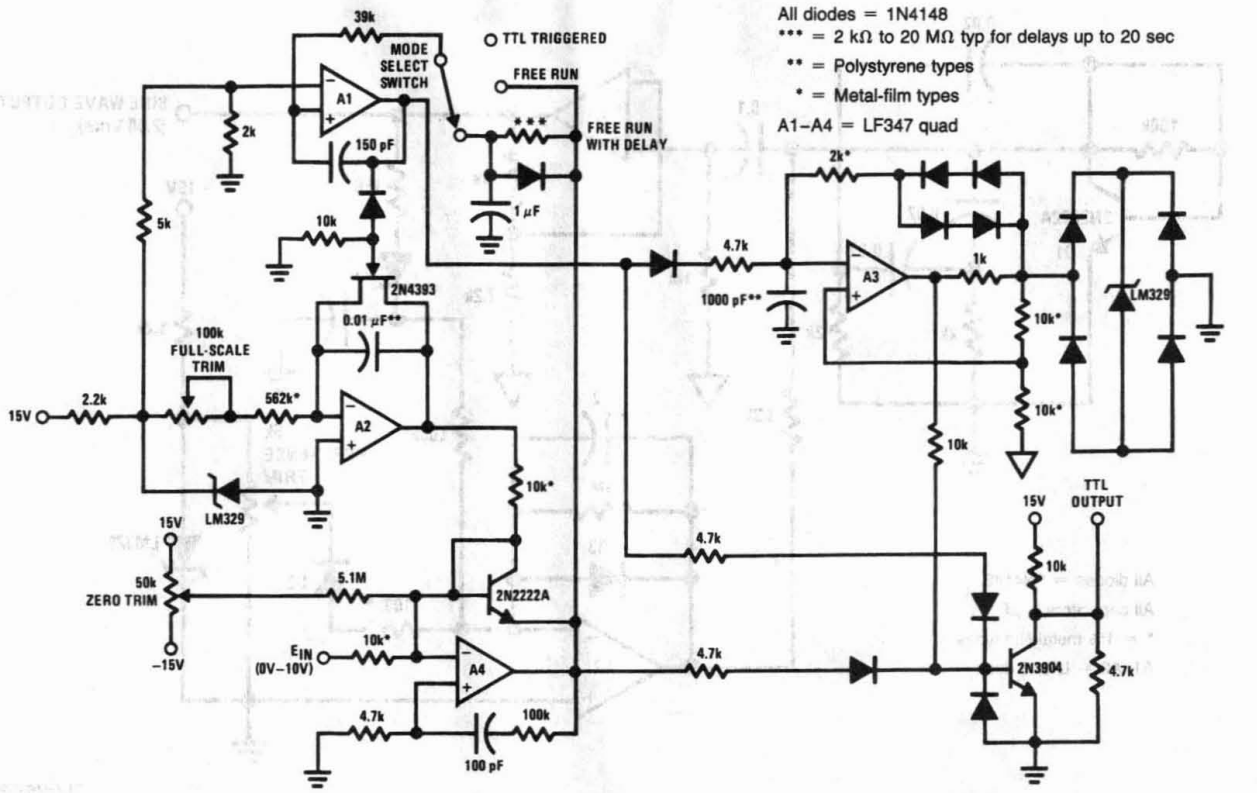
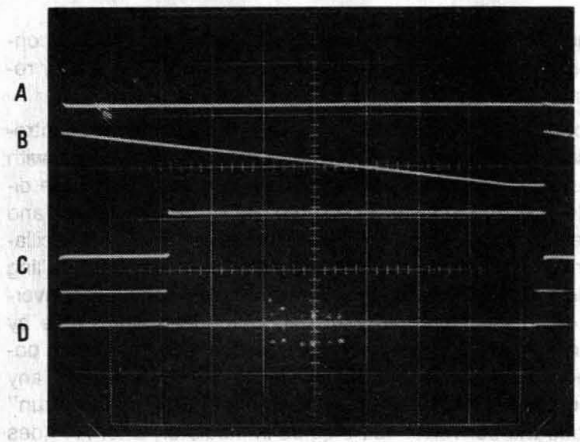


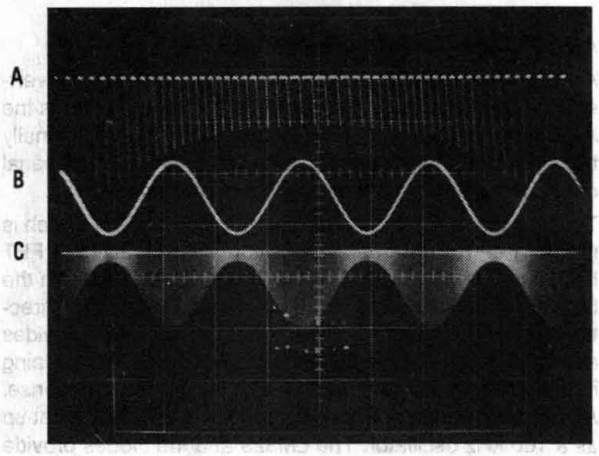
FIGURE 9. Three mode select switch positions offer a choice of internal or external trigger conditions for this integrating A/D converter. Over 15°C to 35°C, this trimmable converter provides a 10-bit serial output, converts in 10 ms and accepts 0V to 10V inputs.



TL/H/6932–10

Trace	Vertical	Horizontal
A	5V/Div	1 ms/Div
B	10V/Div	
C	10V/Div	
D	5V/Div	

FIGURE 10. Depicting the operation of *Figure 9's* A/D circuit in "free run with delay" mode, Trace A shows A1's output low. In this state, integrator A2 starts to ramp in a negative-going direction (Trace B). When A2's ramp potential barely exceeds the input voltage's negative value, A4's output goes high (C). This transition turns on the 2N3904 transistor, which shuts off the TTL output pulse train (D).



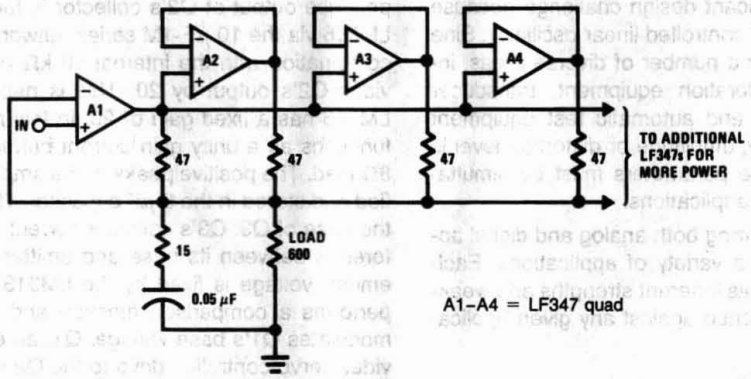
TL/H/6932–11

Trace	Vertical	Horizontal
A	1V/Div	2 ms/Div
B	5V/Div	20 ms/Div
C	5V/Div	20 ms/Div

FIGURE 11. Illustrating the A/D converter's operation in the "free run" mode, Trace B shows a positively biased sine wave input. Because reset and self trigger occur instantly after conversion. A2's output produces a ramp-constructed envelope of the input (Trace C). Trace A shows a time expanded form of the envelope waveform.

HIGH OUTPUT CURRENT AMPLIFIER

Figure 12 shows a scheme for obtaining high output current into a load by using all 4 amplifiers in an LF347 to supply output power. It operates on the principle that all the amplifiers have to supply the same current as A1, whether that current is plus, minus or zero. A single LF347 can be used to drive a 600Ω load to ±11V in this fashion. Two LF347 packages permit ±40 mA of output current. The series RC damper prevents oscillations. The circuit of *Figure 13* is similar but features a gain of 10 and output to a floating load. A1 amplifies the signal and A2 helps it drive the load. A3 operates as a unity gain inverter and A4 helps it to drive the load. This circuit will easily drive a 2000Ω floating load to ±20V.



TL/H/6932–12

FIGURE 12. Utilizing current-amplifying capabilities, one LF347 can drive a 600Ω load to ±11V. For additional power, two LF347's can supply an output current of ±40 mA.

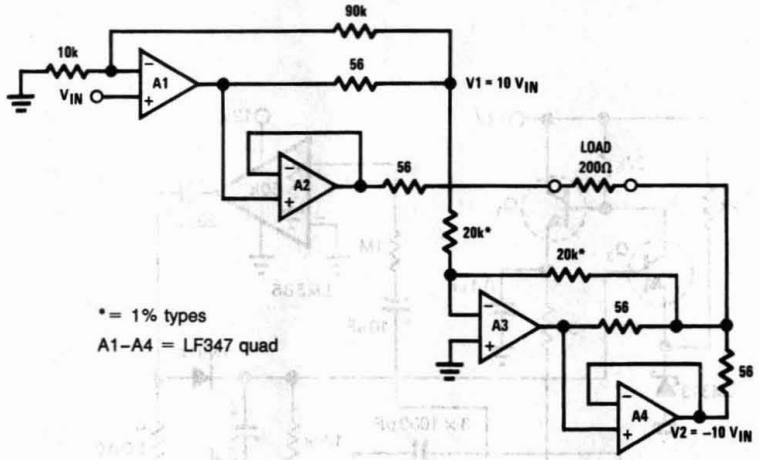


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FIGURE 13. Configured as a high output current amplifier with a gain of 10, this LF347 circuit can drive a 200Ω floating load to ±20V.

Sine Wave Generation Techniques

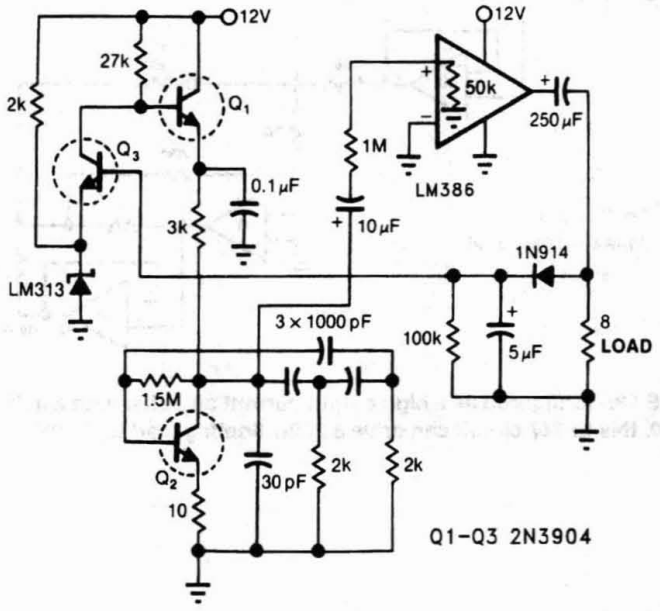
National Semiconductor
Application Note 263

Producing and manipulating the sine wave function is a common problem encountered by circuit designers. Sine wave circuits pose a significant design challenge because they represent a constantly controlled linear oscillator. Sine wave circuitry is required in a number of diverse areas, including audio testing, calibration equipment, transducer drives, power conditioning and automatic test equipment (ATE). Control of frequency, amplitude or distortion level is often required and all three parameters must be simultaneously controlled in many applications.

A number of techniques utilizing both analog and digital approaches are available for a variety of applications. Each individual circuit approach has inherent strengths and weaknesses which must be matched against any given application (see table).

PHASE SHIFT OSCILLATOR

A simple inexpensive amplitude stabilized phase shift sine wave oscillator which requires one IC package, three transistors and runs off a single supply appears in *Figure 1*. Q2, in combination with the RC network comprises a phase shift configuration and oscillates at about 12 kHz. The remaining circuitry provides amplitude stability. The high impedance output at Q2's collector is fed to the input of the LM386 via the 10 μF-1M series network. The 1M resistor in combination with the internal 50 kΩ unit in the LM386 divides Q2's output by 20. This is necessary because the LM386 has a fixed gain of 20. In this manner the amplifier functions as a unity gain current buffer which will drive an 8Ω load. The positive peaks at the amplifier output are rectified and stored in the 5 μF capacitor. This potential is fed to the base of Q3. Q3's collector current will vary with the difference between its base and emitter voltages. Since the emitter voltage is fixed by the LM313 1.2V reference, Q3 performs a comparison function and its collector current modulates Q1's base voltage. Q1, an emitter follower, provides servo controlled drive to the Q2 oscillator. If the emitter of Q2 is opened up and driven by a control voltage, the amplitude of the circuit output may be varied. The LM386 output will drive 5V (1.75 Vrms) peak-to-peak into 8Ω with about 2% distortion. A $\pm$3V power supply variation causes less than $\pm$0.1 dB amplitude shift at the output.



TL/H/7483–1

FIGURE 1. Phase-shift sine wave oscillators combine simplicity with versatility. This 12 kHz design can deliver 5 Vp-p to the 8Ω load with about 2% distortion.

Sine-Wave-Generation Techniques

Type	Typical Frequency Range	Typical Distortion (%)	Typical Amplitude Stability (%)	Comments
Phase Shift	10 Hz–1 MHz	1–3	3 (Tighter with Servo Control)	Simple, inexpensive technique. Easily amplitude servo controlled. Resistively tunable over 2:1 range with little trouble. Good choice for cost-sensitive, moderate-performance applications. Quick starting and settling.
Wein Bridge	1 Hz–1 MHz	0.01	1	Extremely low distortion. Excellent for high-grade instrumentation and audio applications. Relatively difficult to tune—requires dual variable resistor with good tracking. Take considerable time to settle after a step change in frequency or amplitude.
LC Negative Resistance	1 kHz–10 MHz	1–3	3	Difficult to tune over wide ranges. Higher Q than RC types. Quick starting and easy to operate in high frequency ranges.
Tuning Fork	60 Hz–3 kHz	0.25	0.01	Frequency-stable over wide ranges of temperature and supply voltage. Relatively unaffected by severe shock or vibration. Basically untunable.
Crystal	30 kHz–200 MHz	0.1	1	Highest frequency stability. Only slight (ppm) tuning possible. Fragile.
Triangle-Driven Break-Point Shaper	< 1 Hz–500 kHz	1–2	1	Wide tuning range possible with quick settling to new frequency or amplitude.
Triangle-Driven Logarithmic Shaper	< 1 Hz–500 kHz	0.3	0.25	Wide tuning range possible with quick settling to new frequency or amplitude. Triangle and square wave also available. Excellent choice for general-purpose requirements needing frequency-sweep capability with low-distortion output.
DAC-Driven Logarithmic Shaper	<1 Hz–500 kHz	0.3	0.25	Similar to above but DAC-generated triangle wave generally easier to amplitude-stabilize or vary. Also, DAC can be addressed by counters synchronized to a master system clock.
ROM-Driven DAC	1 Hz–20 MHz	0.1	0.01	Powerful digital technique that yields fast amplitude and frequency slewing with little dynamic error. Chief detriments are requirements for high-speed clock (e.g., 8-bit DAC requires a clock that is 256 × output sine wave frequency) and DAC glitching and settling, which will introduce significant distortion as output frequency increases.

LOW DISTORTION OSCILLATION

In many applications the distortion levels of a phase shift oscillator are unacceptable. Very low distortion levels are provided by Wein bridge techniques. In a Wein bridge stable oscillation can only occur if the loop gain is maintained at unity at the oscillation frequency. In *Figure 2a* this is achieved by using the positive temperature coefficient of a small lamp to regulate gain as the output attempts to vary. This is a classic technique and has been used by numerous circuit designers* to achieve low distortion. The smooth limiting action of the positive temperature coefficient bulb in combination with the near ideal characteristics of the Wein network allow very high performance. The photo of *Figure 3* shows the output of the circuit of *Figure 2a*. The upper trace is the oscillator output. The middle trace is the downward slope of the waveform shown greatly expanded. The slight aberration is due to crossover distortion in the FET-input LF155. This crossover distortion is almost totally responsible for the sum of the measured 0.01% distortion in this

*Including William Hewlett and David Packard who built a few of these type circuits in a Palo Alto garage about forty years ago.

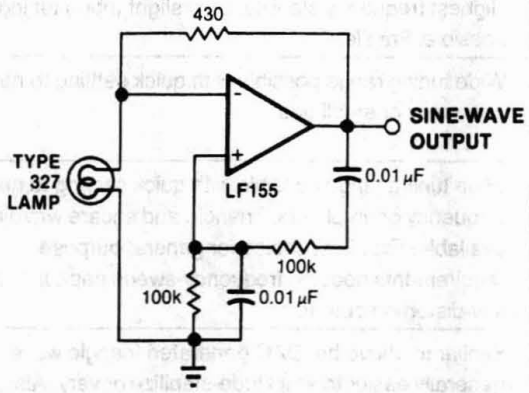
oscillator. The output of the distortion analyzer is shown in the bottom trace. In the circuit of *Figure 2b*, an electronic equivalent of the light bulb is used to control loop gain. The zener diode determines the output amplitude and the loop time constant is set by the 1M-2.2 μF combination.

The 2N3819 FET, biased by the voltage across the 2.2 μF capacitor, is used to control the AC loop gain by shunting the feedback path. This circuit is more complex than *Figure 2a* but offers a way to control the loop time constant while maintaining distortion performance almost as good as in *Figure 2a*.

HIGH VOLTAGE AC CALIBRATOR

Another dimension in sine wave oscillator design is stable control of amplitude. In this circuit, not only is the amplitude stabilized by servo control but voltage gain is included within the servo loop.

A 100 Vrms output stabilized to 0.025% is achieved by the circuit of *Figure 4*. Although complex in appearance this circuit requires just 3 IC packages. Here, a transformer is used to provide voltage gain within a tightly controlled servo loop. The LM3900 Norton amplifiers comprise a 1 kHz amplitude controllable oscillator. The LH0002 buffer provides low impedance drive to the LS-52 audio transformer. A voltage gain of 100 is achieved by driving the secondary of the transformer and taking the output from the primary. A current-sensitive negative absolute value amplifier composed of two amplifiers of an LF347 quad generates a negative rectified feedback signal. This is compared to the LM329 DC reference at the third LF347 which amplifies the difference at a gain of 100. The 10 μF feedback capacitor is used to set the frequency response of the loop. The output of this amplifier controls the amplitude of the LM3900 oscillator thereby closing the loop. As shown the circuit oscillates at 1 kHz with under 0.1% distortion for a 100 Vrms (285 Vp-p) output. If the summing resistors from the LM329 are replaced with a potentiometer the loop is stable for output settings ranging from 3 Vrms to 190 Vrms (542 Vp-p!) with no change in frequency. If the DAC1280 D/A converter shown in dashed lines replaces the LM329 reference, the AC output voltage can be controlled by the digital code input with 3 digit calibrated accuracy.



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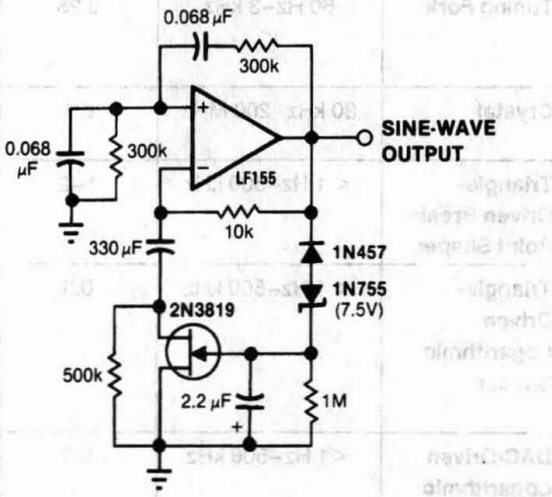
(a)



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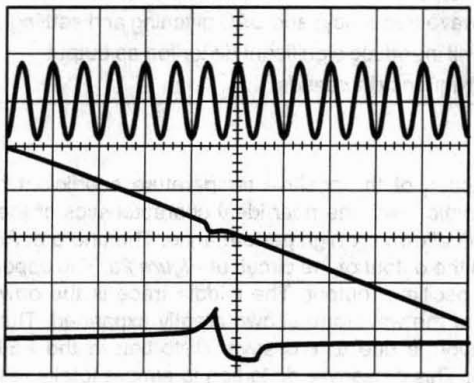
(b)

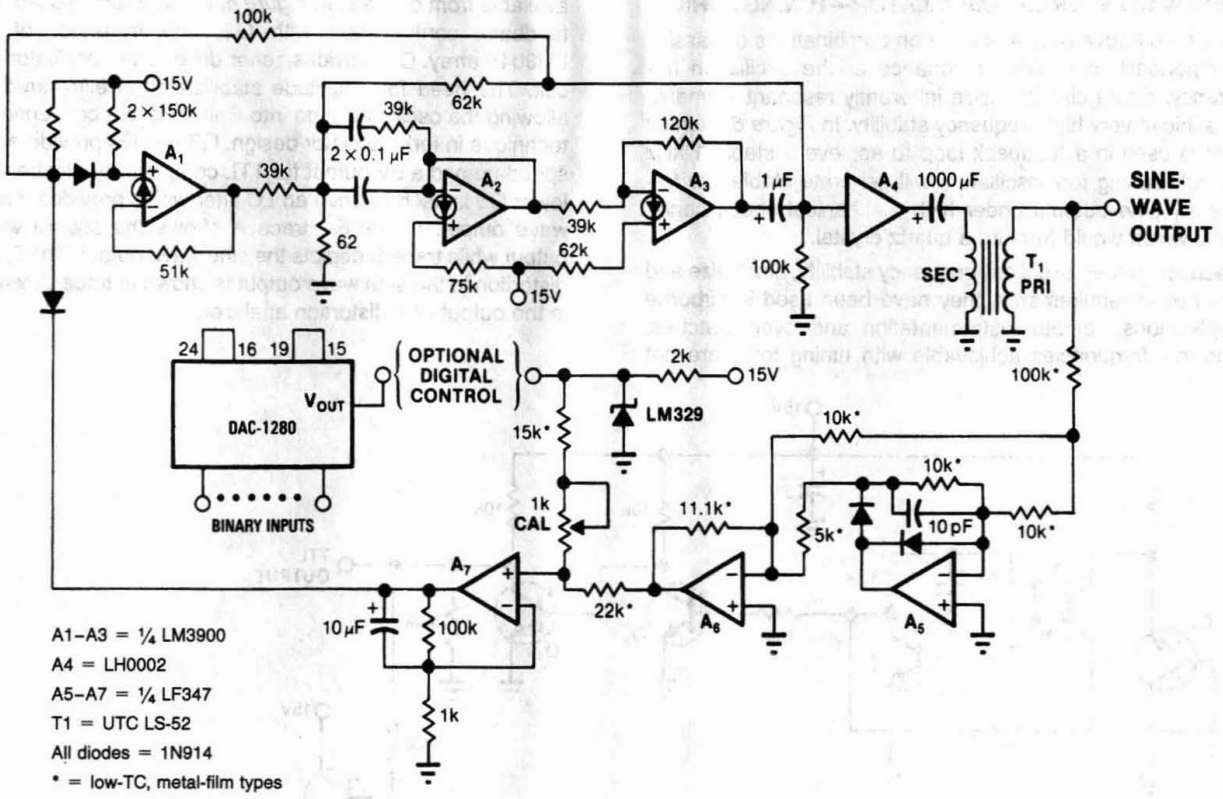
FIGURE 2. A basic Wein bridge design (a) employs a lamp's positive temperature coefficient to achieve amplitude stability. A more complex version (b) provides the same feature with the additional advantage of loop time-constant control.



TL/H/7483–4

Trace	Vertical	Horizontal
Top	10V/DIV	10 ms/DIV
Middle	1V/DIV	500 ns/DIV
Bottom	0.5V/DIV	500 ns/DIV

FIGURE 3. Low-distortion output (top trace) is a Wein bridge oscillator feature. The very low crossover distortion level (middle) results from the LF155's output stage. A distortion analyzer's output signal (bottom) indicates this design's 0.01% distortion level.



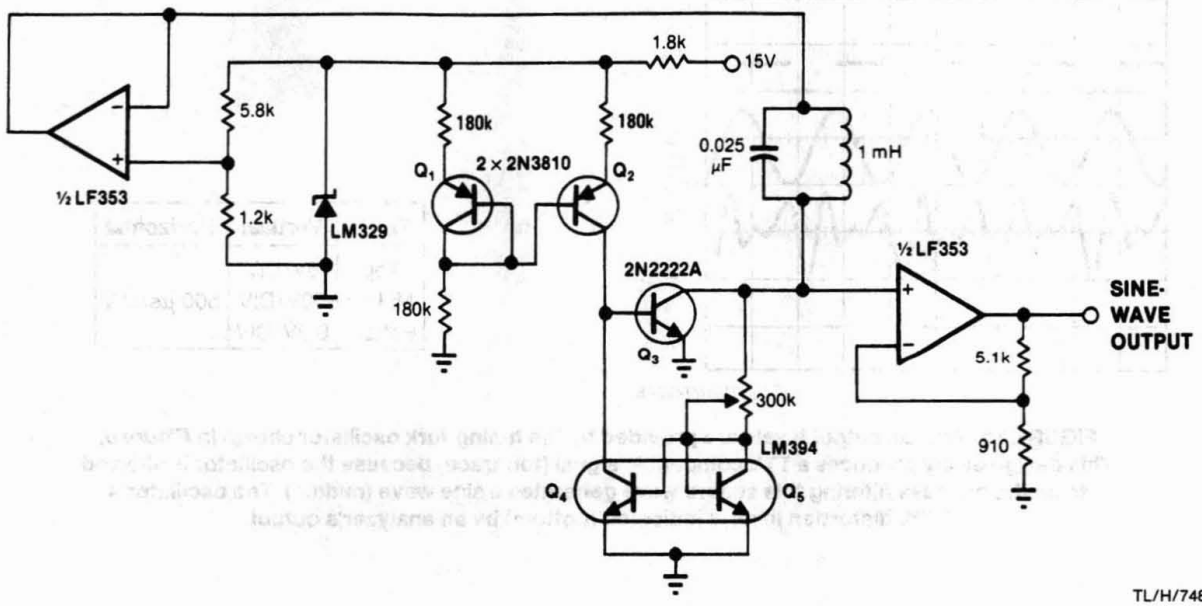
TL/H/7483–5

FIGURE 4. Generate high-voltage sine waves using IC-based circuits by driving a transformer in a step-up mode. You can realize digital amplitude control by replacing the LM329 voltage reference with the DAC1287.

NEGATIVE RESISTANCE OSCILLATOR

All of the preceding circuits rely on RC time constants to achieve resonance. LC combinations can also be used and offer good frequency stability, high Q and fast starting.

In *Figure 5* a negative resistance configuration is used to generate the sine wave. The Q1-Q2 pair provides a 15 μA current source. Q2's collector current sets Q3's peak collector current. The 300 kΩ resistor and the Q4-Q5 LM394 matched pair accomplish a voltage-to-current conversion that decreases Q3's base current when its collector voltage rises. This negative resistance characteristic permits oscillation. The frequency of operation is determined by the LC in the Q3-Q5 collector line. The LF353 FET amplifier provides gain and buffering. Power supply dependence is eliminated by the zener diode and the LF353 unity gain follower. This circuit starts quickly and distortion is inside 1.5%.



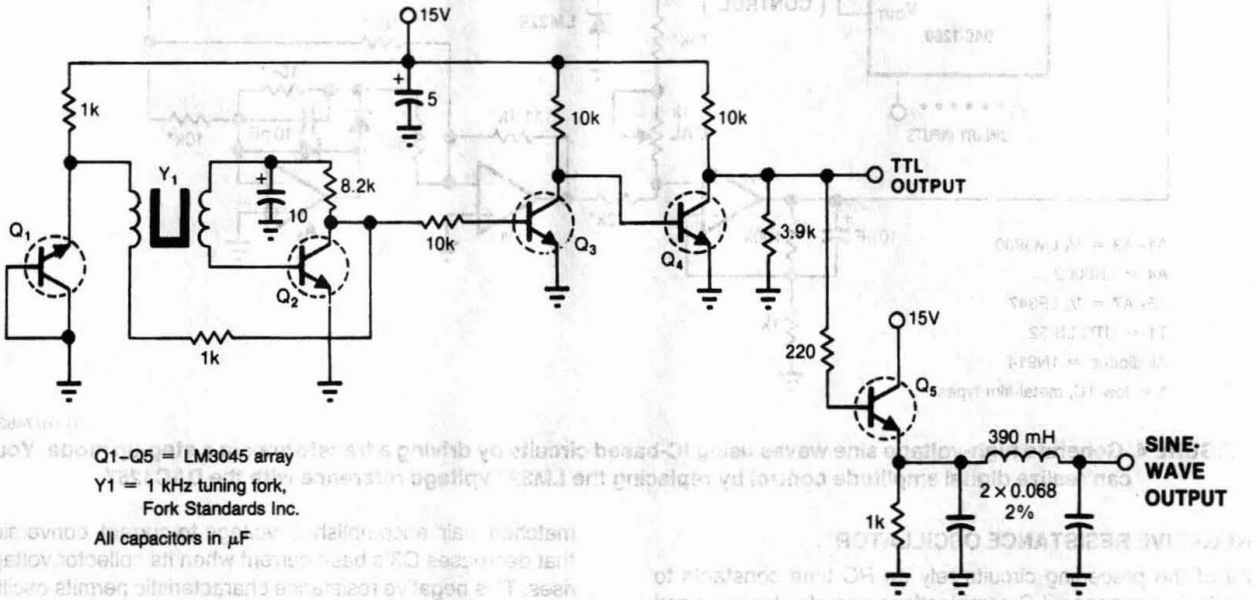
TL/H/7483–6

FIGURE 5. LC sine wave sources offer high stability and reasonable distortion levels. Transistors Q1 through Q5 implement a negative-resistance amplifier. The LM329, LF353 combination eliminates power-supply dependence.

RESONANT ELEMENT OSCILLATOR—TUNING FORK

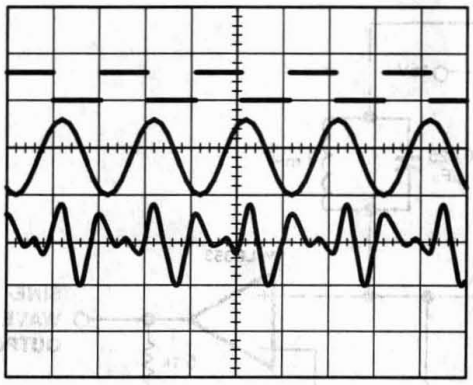
All of the above oscillators rely on combinations of passive components to achieve resonance at the oscillation frequency. Some circuits utilize inherently resonant elements to achieve very high frequency stability. In *Figure 6* a tuning fork is used in a feedback loop to achieve a stable 1 kHz output. Tuning fork oscillators will generate stable low frequency sine outputs under high mechanical shock conditions which would fracture a quartz crystal.

Because of their excellent frequency stability, small size and low power requirements, they have been used in airborne applications, remote instrumentation and even watches. The low frequencies achievable with tuning forks are not available from crystals. In *Figure 6*, a 1 kHz fork is used in a feedback configuration with Q2, one transistor of an LM3045 array. Q1 provides zener drive to the oscillator circuit. The need for amplitude stabilization is eliminated by allowing the oscillator to go into limit. This is a conventional technique in fork oscillator design. Q3 and Q4 provide edge speed-up and a 5V output for TTL compatibility. Emitter follower Q5 is used to drive an LC filter which provides a sine wave output. *Figure 6a*, trace A shows the square wave output while trace B depicts the sine wave output. The 0.7% distortion in the sine wave output is shown in trace C, which is the output of a distortion analyzer.



TL/H/7483–7

FIGURE 6. Tuning fork based oscillators don't inherently produce sinusoidal outputs. But when you do use them for this purpose, you achieve maximum stability when the oscillator stage (Q1, Q2) limits. Q3 and Q4 provide a TTL compatible signal, which Q5 then converts to a sine wave.



Trace	Vertical	Horizontal
Top	5V/DIV	
Middle	50V/DIV	500 μs/DIV
Bottom	0.2V/DIV	

TL/H/7483–8

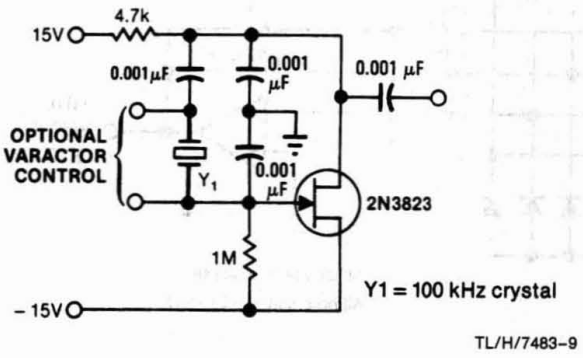
FIGURE 6a. Various output levels are provided by the tuning fork oscillator shown in *Figure 6*. This design easily produces a TTL compatible signal (top trace) because the oscillator is allowed to limit. Low-pass filtering this square wave generates a sine wave (middle). The oscillator's 0.7% distortion level is indicated (bottom) by an analyzer's output.

RESONANT ELEMENT OSCILLATOR—QUARTZ CRYSTAL

Quartz crystals allow high frequency stability in the face of changing power supply and temperature parameters. *Figure 7a* shows a simple 100 kHz crystal oscillator. This Colpitts class circuit uses a JFET for low loading of the crystal, aiding stability. Regulation will eliminate the small effects ($\sim$ 5 ppm for 20% shift) that supply variation has on this circuit. Shunting the crystal with a small amount of capacitance allows very fine trimming of frequency. Crystals typically drift less than 1 ppm/°C and temperature controlled ovens can be used to eliminate this term (*Figure 7b*). The RC feedback values will depend upon the thermal time constants of the oven used. The values shown are typical. The temperature of the oven should be set so that it coincides with the crystal's zero temperature coefficient or "turning point" temperature which is manufacturer specified. An alternative to temperature control uses a varactor diode placed across the crystal. The varactor is biased by a temperature dependent voltage from a circuit which could be very similar to *Figure 7b* without the output transistor. As ambient temperature varies the circuit changes the voltage across the varactor, which in turn changes its capacitance. This shift in capacitance trims the oscillator frequency.

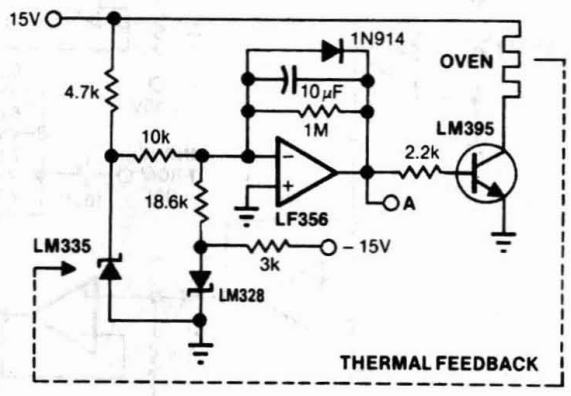
APPROXIMATION METHODS

All of the preceding circuits are *inherent* sine wave generators. Their normal mode of operation supports and maintains a sinusoidal characteristic. Another class of oscillator is made up of circuits which *approximate* the sine function through a variety of techniques. This approach is usually more complex but offers increased flexibility in controlling amplitude and frequency of oscillation. The capability of this type of circuit for a digitally controlled interface has markedly increased the popularity of the approach.



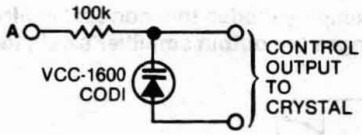
TL/H/7483–9

(a)



TL/H/7483–10

(b)



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(c)

FIGURE 7. Stable quartz-crystal oscillators can operate with a single active device (a). You can achieve maximum frequency stability by mounting the oscillator in an oven and using a temperature-controlling circuit (b). A varactor network (c) can also accomplish crystal fine tuning. Here, the varactor replaces the oven and retunes the crystal by changing its load capacitances.

SINE APPROXIMATION—BREAKPOINT SHAPER

Figure 8 diagrams a circuit which will "shape" a 20 Vp-p wave input into a sine wave output. The amplifiers serve to establish stable bias potentials for the diode shaping network. The shaper operates by having individual diodes turn on or off depending upon the amplitude of the input triangle. This changes the gain of the output amplifier and gives the circuit its characteristic non-linear, shaped output response. The values of the resistors associated with the diodes determine the shaped waveform's appearance. Individual diodes in the DC bias circuitry provide first order temperature compensation for the shaper diodes. *Figure 9* shows the circuit's performance. Trace A is the filtered output (note 1000 pF capacitor across the output amplifier). Trace B shows the waveform with no filtering (1000 pF capacitor removed) and trace C is the output of a distortion analyzer. In trace B the breakpoint action is just detectable at the top and bottom of the waveform, but all the breakpoints are clearly identifiable in the distortion analyzer output of trace C. In this circuit, if the amplitude or symmetry of the input triangle wave shifts, the output waveform will degrade badly. Typically, a D/A converter will be used to provide input drive. Distortion in this circuit is less than 1.5% for a filtered output. If no filter is used, this figure rises to about 2.7%.

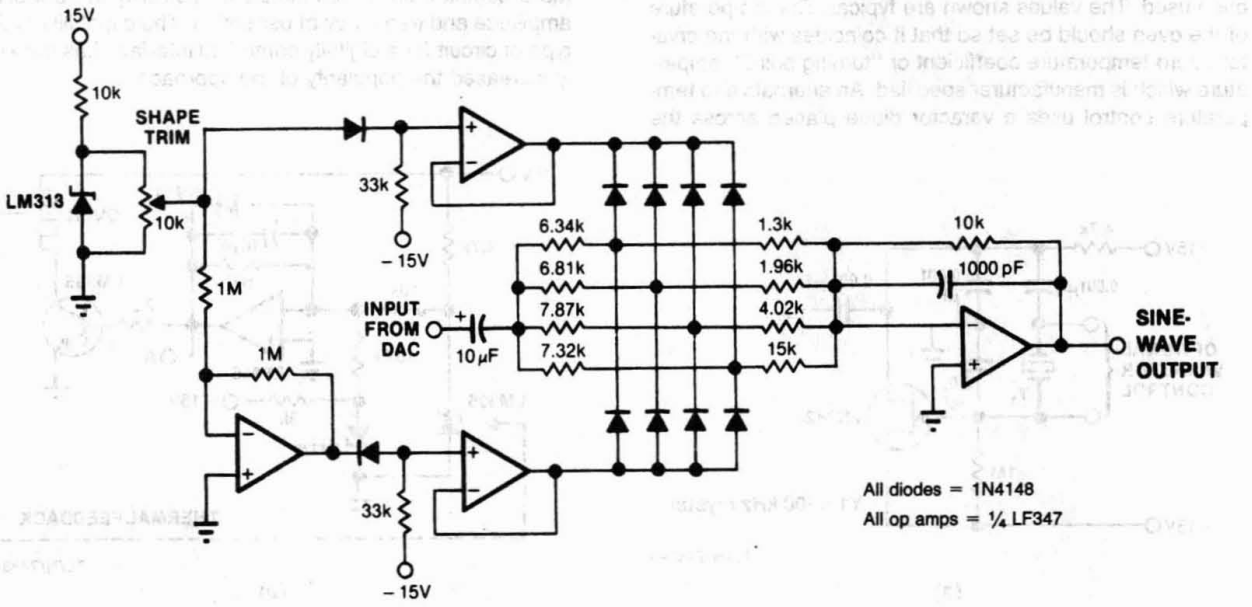

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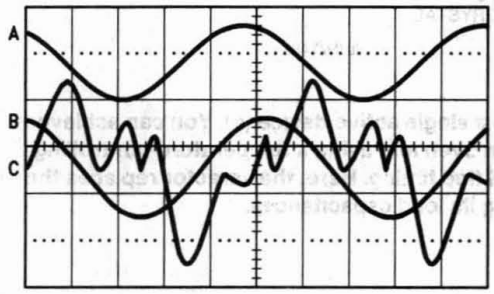
FIGURE 8. Breakpoint shaping networks employ diodes that conduct in direct proportion to an input triangle wave's amplitude. This action changes the output amplifier's gain to produce the sine function.



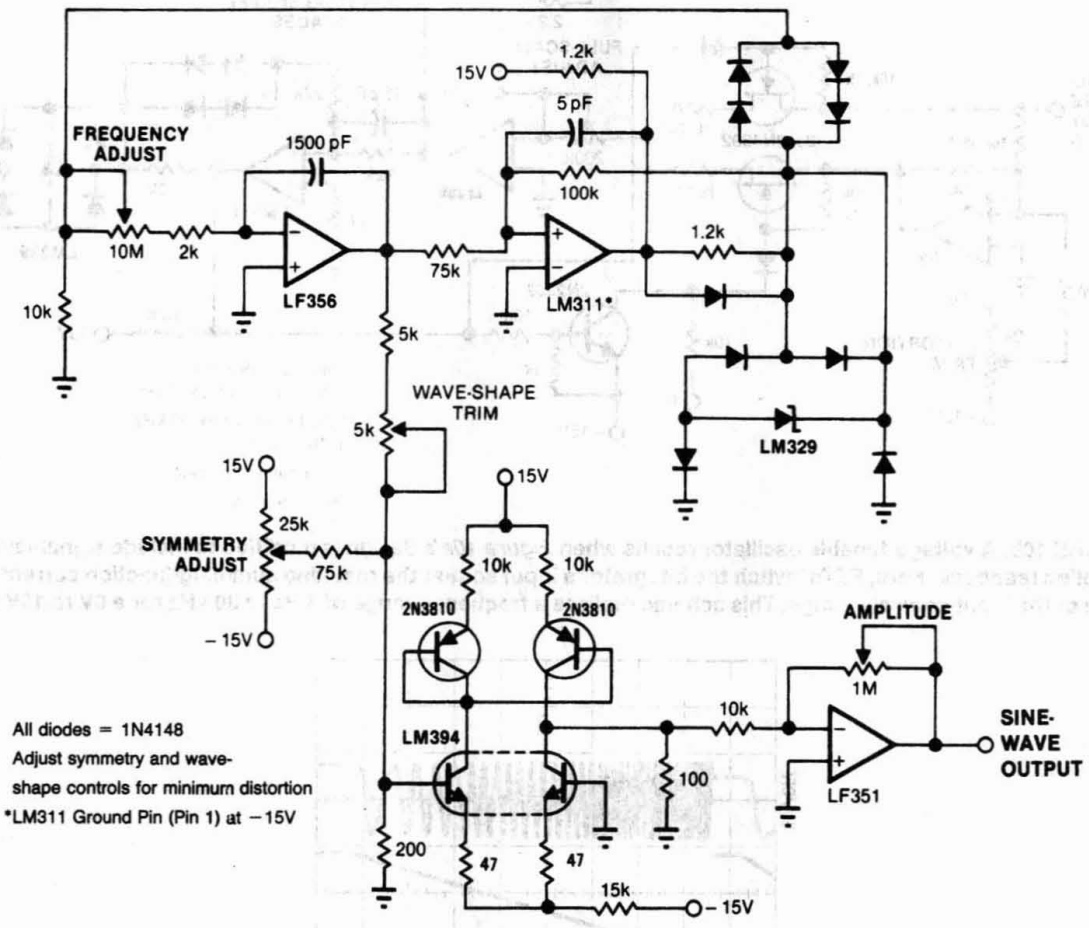
TL/H/7483–13

Trace	Vertical	Horizontal
A	5V/DIV	
B	5V/DIV	20 µs/DIV
C	0.5V/DIV	

FIGURE 9. A clean sine wave results (trace A) when *Figure 8's* circuit's output includes a 1000 pF capacitor. When the capacitor isn't used, the diode network's breakpoint action becomes apparent (trace B). The distortion analyzer's output (trace C) clearly shows all the breakpoints.

SINE APPROXIMATION—LOGARITHMIC SHAPING

Figure 10 shows a complete sine wave oscillator which may be tuned from 1 Hz to 10 kHz with a single variable resistor. Amplitude stability is inside 0.02%/°C and distortion is 0.35%. In addition, desired frequency shifts occur instantaneously because no control loop time constants are employed. The circuit works by placing an integrator inside the positive feedback loop of a comparator. The LM311 drives symmetrical, temperature-compensated clamp arrangement. The output of the clamp biases the LF356 integrator. The LF356 integrates this current into a linear ramp at its output. This ramp is summed with the clamp output at the LM311 input. When the ramp voltage nulls out the bound voltage, the comparator changes state and the integrator output reverses. The resultant, repetitive triangle waveform is applied to the sine shaper configuration. The sine shaper utilizes the non-linear, logarithmic relationship between V_{be} and collector current in transistors to smooth the triangle wave. The LM394 dual transistor is used to generate the actual shaping while the 2N3810 provides current drive. The LF351 allows adjustable, low impedance, output amplitude control. Waveforms of operation are shown in *Figure 11*.



TL/H/7483–14

FIGURE 10a. Logarithmic shaping schemes produce a sine wave oscillator that you can tune from 1 Hz to 10 kHz with a single control. Additionally, you can shift frequencies rapidly because the circuit contains no control-loop time constants.

SINE APPROXIMATION—VOLTAGE CONTROLLED SINE OSCILLATOR

Figure 10b details a modified but extremely powerful version of *Figure 10*. Here, the input voltage to the LF356 integrator is furnished from a control voltage input instead of the zener diode bridge. The control input is inverted by the LF351. The two complementary voltages are each gated by the 2N4393 FET switches, which are controlled by the LM311 output. The frequency of oscillation will now vary in direct proportion to the control input. In addition, because the amplitude of this circuit is controlled by limiting, rather than a servo loop, response to a control step or ramp input is almost instantaneous. For a 0V–10V input the output will run over 1 Hz to 30 kHz with less than 0.4% distortion. In addition, linearity of control voltage vs output frequency will be within 0.25%. *Figure 10c* shows the response of this circuit (waveform B) to a 10V ramp (waveform A).

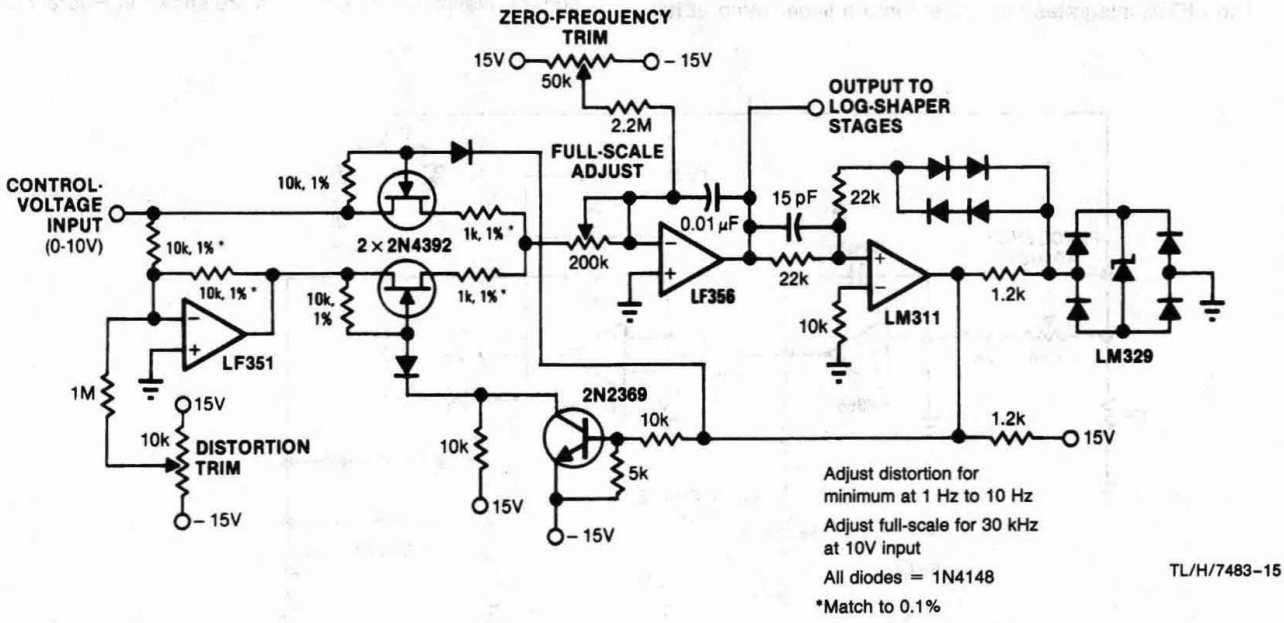
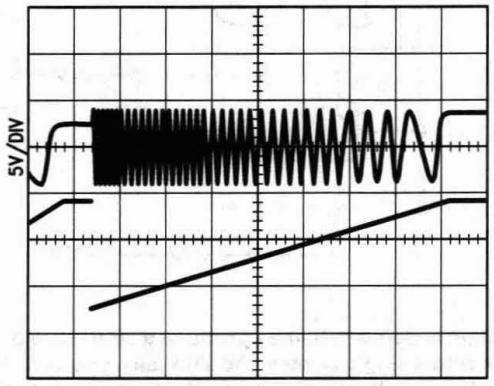


FIGURE 10b. A voltage-tunable oscillator results when *Figure 10a's* design is modified to include signal-level-controlled feedback. Here, FETs switch the integrator's input so that the resulting summing-junction current is a function of the input control voltage. This scheme realizes a frequency range of 1 Hz to 30 kHz for a 0V to 10V input.

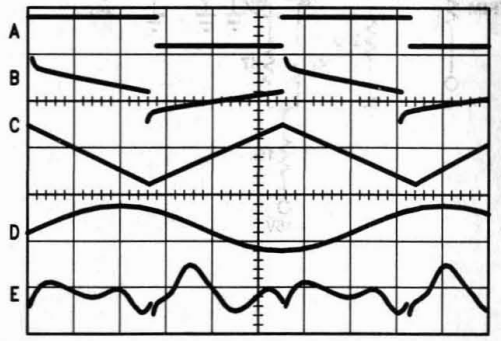


TL/H/7483–16

FIGURE 10c. Rapid frequency sweeping is an inherent feature of *Figure 10b's* voltage-controlled sine wave oscillator. You can sweep this VCO from 1 Hz to 30 kHz with a 10V input signal; the output settles quickly.

SINE APPROXIMATION—DIGITAL METHODS

Digital methods may be used to approximate sine wave operation and offer the greatest flexibility at some increase in complexity. *Figure 12* shows a 10-bit IC D/A converter driven from up/down counters to produce an amplitude-stable triangle current into the LF357 FET amplifier. The LF357 is used to drive a shaper circuit of the type shown in *Figure 10*. The output amplitude of the sine wave is stable and the frequency is solely dependent on the clock used to drive the counters. If the clock is crystal controlled, the output sine wave will reflect the high frequency stability of the crystal. In this example, 10 binary bits are used to drive the DAC so the output frequency will be 1/1024 of the clock frequency. If a sine coded read-only-memory is placed between the counter outputs and the DAC, the sine shaper may be eliminated and the sine wave output taken directly from the LF357. This constitutes an extremely powerful digital technique for generating sine waves. The amplitude may be voltage controlled by driving the reference terminal of the DAC. The frequency is again established by the clock speed used and both may be varied at high rates of speed without introducing significant lag or distortion. Distortion is low and is related to the number of bits of resolution used. At the 8-bit level only 0.5% distortion is seen (waveforms, *Figure 13*; graph, *Figure 14*) and filtering will drop this below 0.1%. In the photo of *Figure 13* the ROM directed steps are clearly visible in the sine waveform and the DAC levels and glitching show up in the distortion analyzer output. Filtering at the output amplifier does an effective job of reducing distortion by taking out these high frequency components.



TL/H/7483–17

Trace	Vertical	Horizontal
A	20V/DIV	
B	20V/DIV	20 μs/DIV
C	10V/DIV	
D	10V/DIV	
E	0.5V/DIV	

FIGURE 11. Logarithmic shapers can utilize a variety of circuit waveforms. The input to the LF356 integrator (*Figure 10*) appears here as trace A. The LM311's input (trace B) is the summed result of the integrator's triangle output (C) and the LM329's clamped waveform. After passing through the 2N3810/LM394 shaper stage, the resulting sine wave is amplified by the LF351 (D). A distortion analyzer's output (E) represents a 0.35% total harmonic distortion.

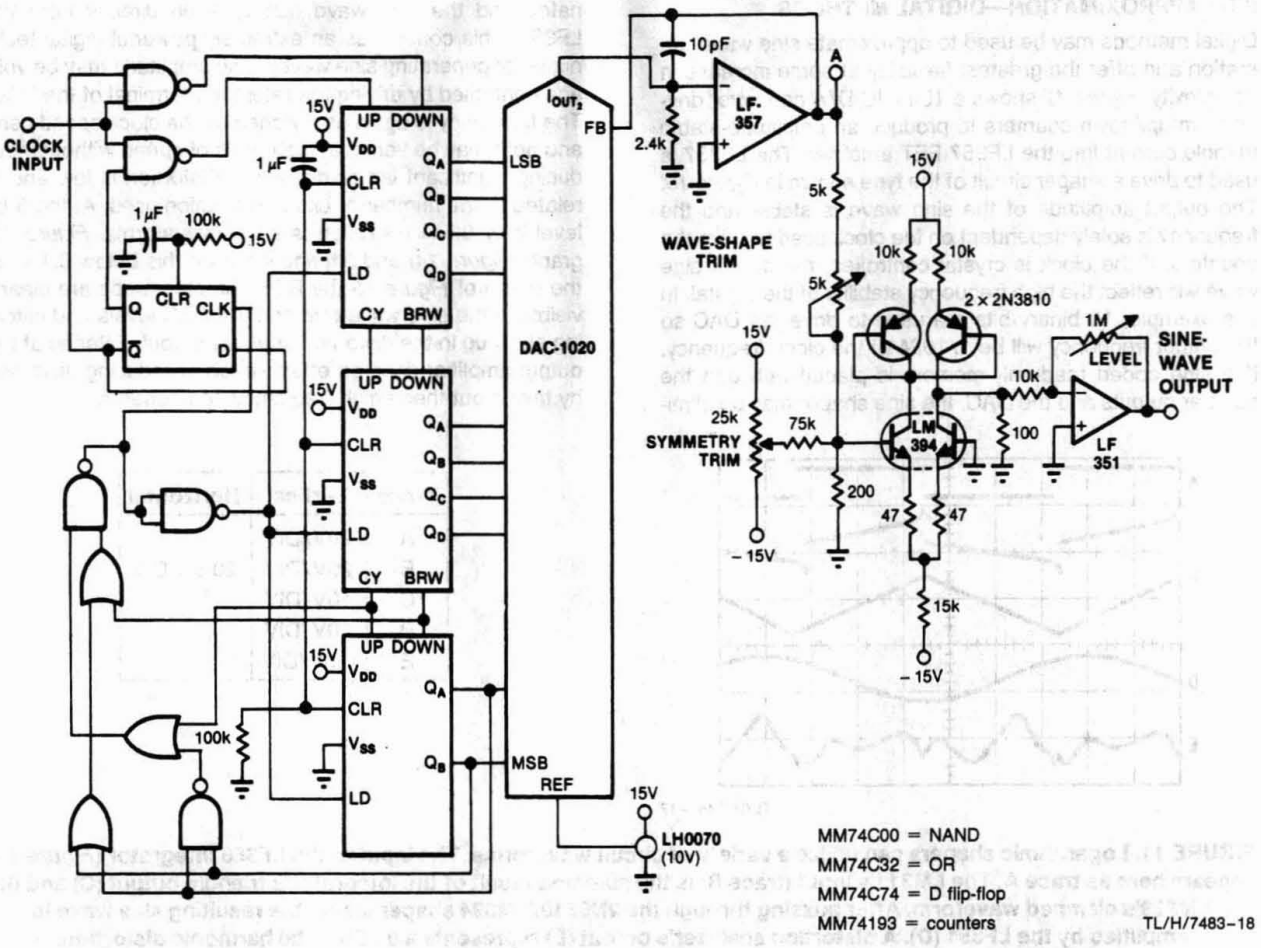
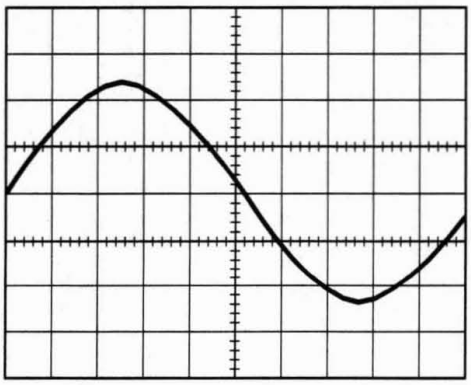


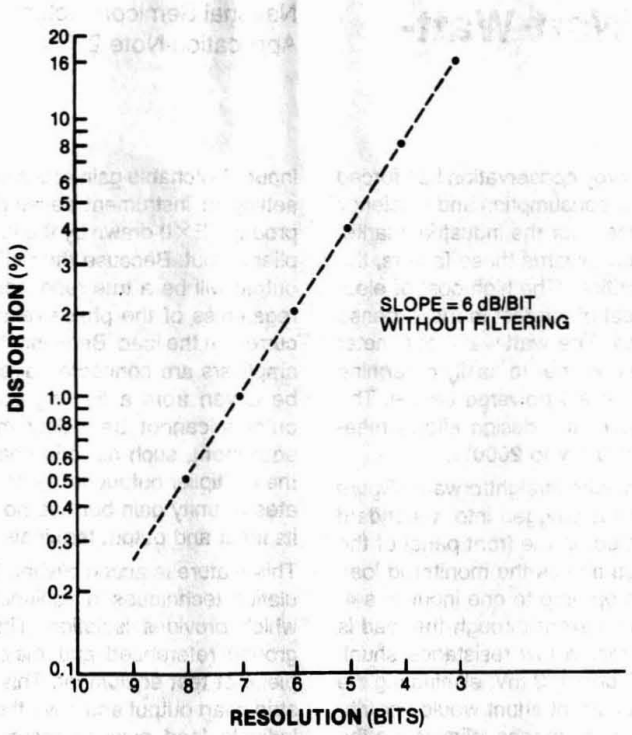
FIGURE 12. Digital techniques produce triangular waveforms that methods employed in *Figure 10a* can then easily convert to sine waves. This digital approach divides the input clock frequency by 1024 and uses the resultant 10 bits to drive a DAC. The DAC's triangular output—amplified by the LF357—drives the log shaper stage. You could also eliminate the log shaper and place a sine-coded ROM between the counters' outputs and the DAC, then recover the sine wave at point A.



TL/H/7483–19

Trace	Vertical	Horizontal
Sine Wave	1V/DIV	200 μs/DIV
Analyzer	0.2V/DIV	

FIGURE 13. An 8-bit sine coded ROM version of *Figure 12's* circuit produces a distortion level less than 0.5%. Filtering the sine output—shown here with a distortion analyzer's trace—can reduce the distortion to below 0.1%.



TL/H/7483–20

FIGURE 14. Distortion levels decrease with increasing digital word length. Although additional filtering can considerably improve the distortion levels (to 0.1% from 0.5% for the 8-bit case), you're better off using a long digital word.

An Electronic Watt-Watt-Hour Meter

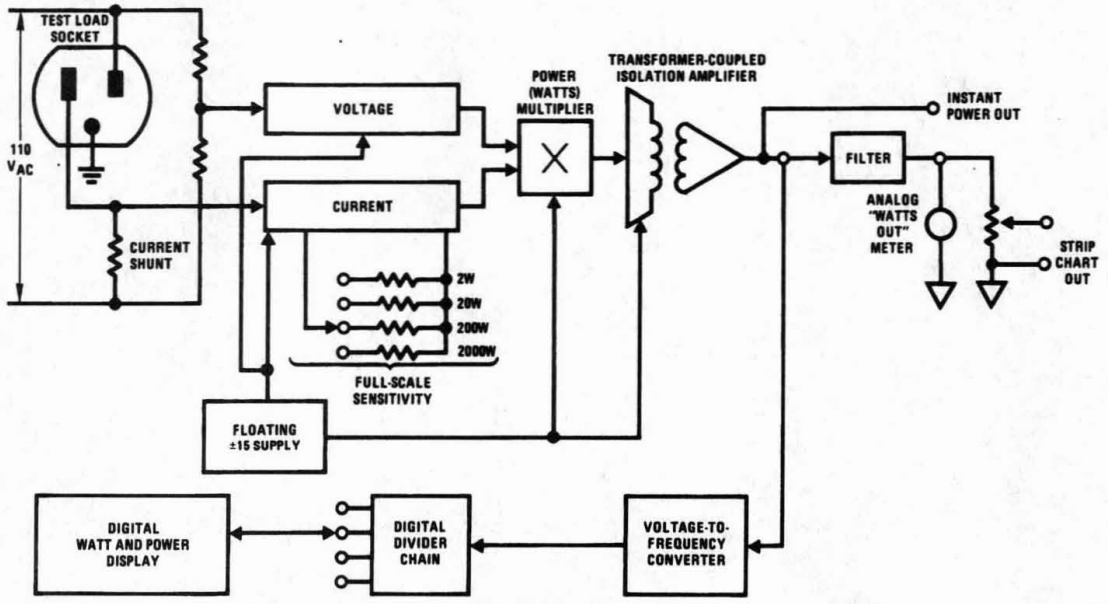
National Semiconductor
Application Note 265

The continued emphasis on energy conservation has forced designers to consider the power consumption and efficiency of their products. While equipment for the industrial market must be designed with attention towards these factors, the consumer area is even more critical. The high cost of electricity has promoted a great deal of interest in the expense of powering various appliances. The watt-watt-hour meter outlined in *Figure 1* allows the designer to easily determine power consumption of any 115V AC powered device. The extremely wide dynamic range of the design allows measurement of loads ranging from 0.1W to 2000W.

Conceptually, the instrument is quite straightforward *(Figure 1).* The device to be monitored is plugged into a standard 110V AC outlet which is mounted on the front panel of the instrument. The AC line voltage across the monitored load is divided down and fed via an op amp to one input of a 4-quadrant analog multiplier. The current through the load is determined by the voltage across a low resistance shunt. Even at 20A the shunt "steals" only 133 mV, eliminating the inaccuracies a high resistance current shunt would contribute. This single shunt is used for all ranges, eliminating the need to switch in high impedance shunts to obtain adequate signal levels on the high sensitivity scales.

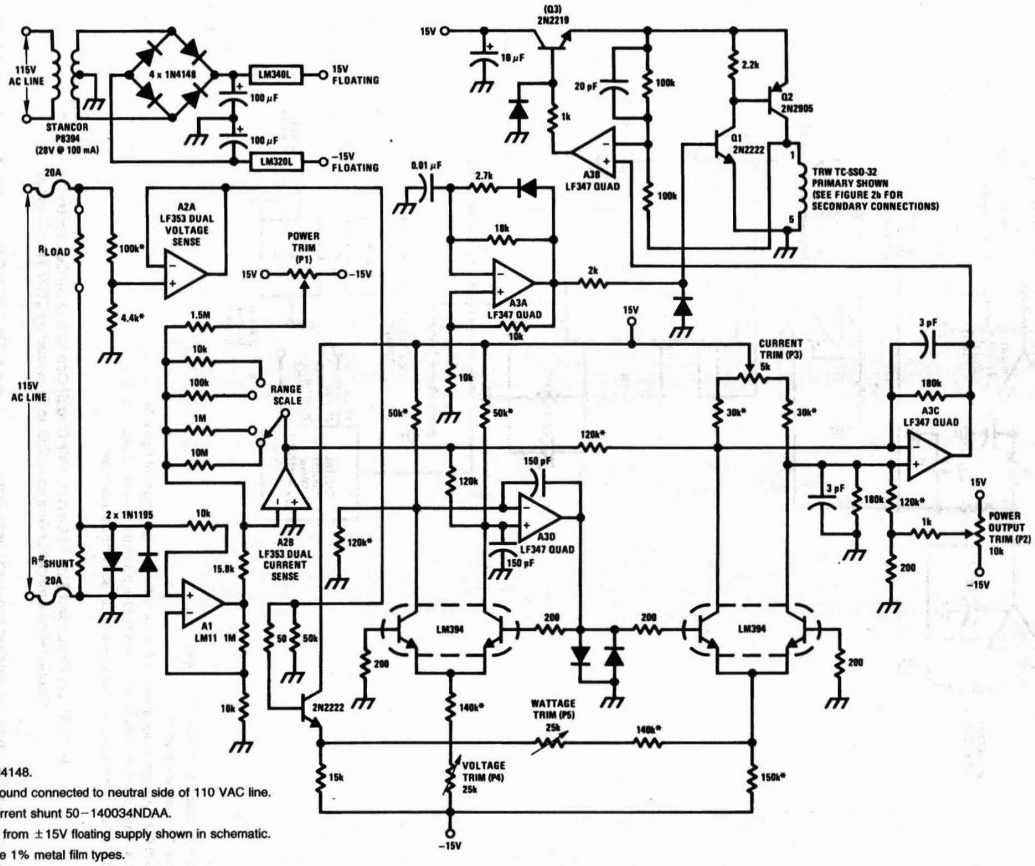
This provision is made possible by low uncertainty in the current amplifier, whose output feeds the other multiplier input. Switchable gain at the current amplifier allows decade setting of instrument sensitivity. The instantaneous power product (E×I) drawn by the load is represented by the multiplier output. Because the multiplier is a 4-quadrant type, its output will be a true reflection of load power consumption, regardless of the phase relationship between voltage and current in the load. Because the multiplier and its associated amplifiers are connected directly to the AC line, they must be driven from a floating power supply. In addition, their outputs cannot be safely monitored with grounded test equipment, such as strip chart recorders. For this reason, the multiplier output drives an isolation amplifier which operates at unity gain but has no galvanic connection between its input and output terminals.

This feature is accomplished through pulse amplitude modulation techniques in conjunction with a small transformer, which provides isolation. The isolated amplifier output is ground referenced and may safely be connected to any piece of test equipment. This output is filtered to provide a strip chart output and drive the readout meter, both of which indicate load power consumption. The isolation amplifier output also biases a voltage-to-frequency converter which combines with digital counters to form a digital integrator. This allows power over time (watt-hours) to be integrated and displayed. Varying the divide ratio of the counters produces ranging of the watt-hour function.



TL/H/5626–1

FIGURE 1



Note 1: All diodes 1N4148.

Note 2: ⏚ floating ground connected to neutral side of 110 VAC line.

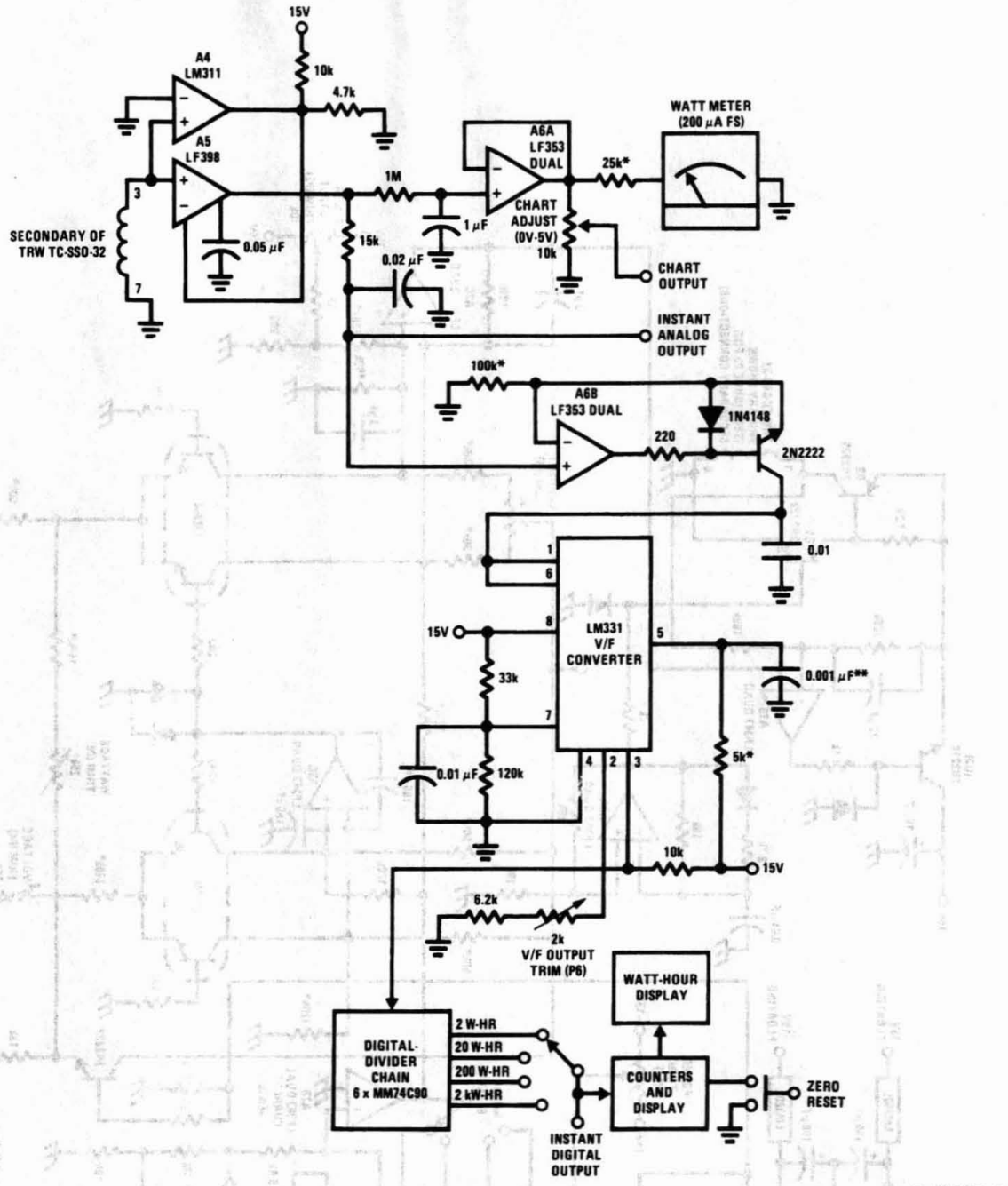
Note 3: R# = G.E. current shunt 50−140034NDAA.

Note 4: Circuit power from ±15V floating supply shown in schematic.

Note 5: *Resistors are 1% metal film types.

TL/H/5626–2

FIGURE 2a. Floating Half of Circuit is Connected Directly to the AC Line. Always Use Caution when Working with this Circuitry.



Note 1: *Resistors are 1% metal film types.

Note 2: **Polystyrene capacitor.

Note 3: DO NOT connect (⏚) ground of this half of circuit to (⏚) ground of *Figure 2a.*

Note 4: ±15V power must come from a source other than floating supply of *Figure 2a.*

Note 5: *Figure 2a* and *Figure 2b* must be electrically isolated from each other.

FIGURE 2b. Grounded Side of Circuit. This Circuit Can Safely Be Connected to a Chart Recorder or Computer Due to Isolation Provided by TRW Transformer.

Figures 2a and *2b* show the detailed schematic, with *Figure 3* giving the waveforms of operation. The AC line is divided down by the 100 kΩ − 4.4 kΩ resistor string. ½ of A2 (amplifier A) serves as a buffer and feeds one input of an analog multiplier configuration. A1 monitors the voltage across the current shunt at a fixed gain of 100. The other half of A2 (B) provides additional gain and calibrated switching of wattage sensitivities from 2W to 2000W full-scale over four decade ranges. The 1N1195 diodes and the 20A fuses protect A1 and the shunt in the event a short appears across the load test socket. The voltage and current signals are multiplied by a multiplier configuration comprised of amplifiers A3, C and D, and the LM394 dual transistors. The multiplier is of the variable transconductance type and works by using one input to vary the gain of an amplifier whose output is the other input of the multiplier.

The output of the multiplier *(Figure 3,* Trace A) represents the instantaneous power consumed by the load. This information is used to bias a pulse amplitude modulating isolation amplifier. The isolation amplifier is made up of A3 (A and B) and the discrete transistors. The A3 (A) oscillator output *(Figure 3,* Trace B) biases the Q1-Q2 switch, which drives a pulse transformer. A3 (B) measures the amplitude of the pulses at the transformer and servo controls them to be the same amplitude as its "+" input, which is biased from the multiplier output. Q3 provides current drive capability and completes the feedback path for A3 (B). *Figure 3,* Trace D shows the pulses applied to the transformer. Note that the amplitude of the pulses applied to the transformer forms an envelope whose amplitude equals the multiplier output. *Figure 3,* Trace C shows Q3's emitter voltage changing to meet the requirements of the servo loop.

The amplitude modulated pulses appear at the transformer's secondary, which is referenced to instrument ground. The amplitude of each pulse is sampled by A5, a sample-hold amplifier. The sample command is generated by A4. The output of A5 is lightly filtered by the 15 kΩ−0.02 μF combination and represents a sampled version of the instantaneous power consumed in the load *(Figure 3,* Trace E). Heavy filtering by the 1 MΩ−1 μF time constant produces a smoothed version of the power signal, which drives the watts meter and the strip chart output via the A6 (A) buffer. The watt-hour time integration function is provided by an LM331 voltage-to-frequency converter and a digital divider chain which form a digital integrator. The lightly filtered A5 output is fed to A6 (B) which is used to bias the V/F converter. The V/F output drives a divider chain. The ratio of the divider chain sets the time constant of the integrator and is used to switch the scale factor of the watt-hours display. The additional counters and display provide the digital readout in watt-hours. A zero reset button allows display reset.

INSTRUMENT CALIBRATION

To calibrate the instrument, pull the 20A fuses from their holders. Next, adjust P1 for 0.00V out at A2 (B) with the watts range switch in the 2 watt position. Then, disconnect both multiplier input lines and connect them to floating ("⏚") instrument ground. Adjust P2 for 0V out at A6 (A). Next, apply a 10 Vp-p 60 Hz waveform to the current input of the multiplier (leave the voltage input grounded) and adjust P3 for zero volts out at A6 (A). Then, reverse the state of the multiplier inputs and adjust P4 for zero volts out at A6 (A). Reconnect the multiplier input into the circuit. Read the AC line voltage with a digital voltmeter. Plug in a known load (e.g., 1% power resistor) to the test socket and adjust P5 until the meter reads what the wattage should be (wattage = line voltage^2/resistance of load). Finally, lift A6's (B's) "+" input line, apply 5.00V to it, and adjust P6 until the LM331V/F output (pin 3) runs at 27.77 kHz. Reconnect A6's (B's) input. This completes the calibration.

APPLICATIONS

Once calibrated, the watt-watt-hour meter provides a powerful measurement capability. A few simple tests provide some surprising and enlightening results. The strip chart of *Figure 4a* shows the measured power a home refrigerator draws over 3½ hours at a temperature set-point of 7°C. Each time the compressor comes on, the unit draws about 260W. Actually, the strip chart clearly shows that as the compressor warms up over time, the amount of power drawn drops off a bit. The watt-hour display was used to record the total watt-hours consumed during this 3½ hour period. The data is summarized in the table provided. With the temperature control in the refrigerator set to maintain 5°C, just 2°C colder, it can be seen that the compressor duty cycle shifts appreciably *(Figure 4b),* over 6%! This factor is directly reflected in the kW-H/cycle and yearly operating cost columns. If you want your milk 2°C colder you will have to pay for it!

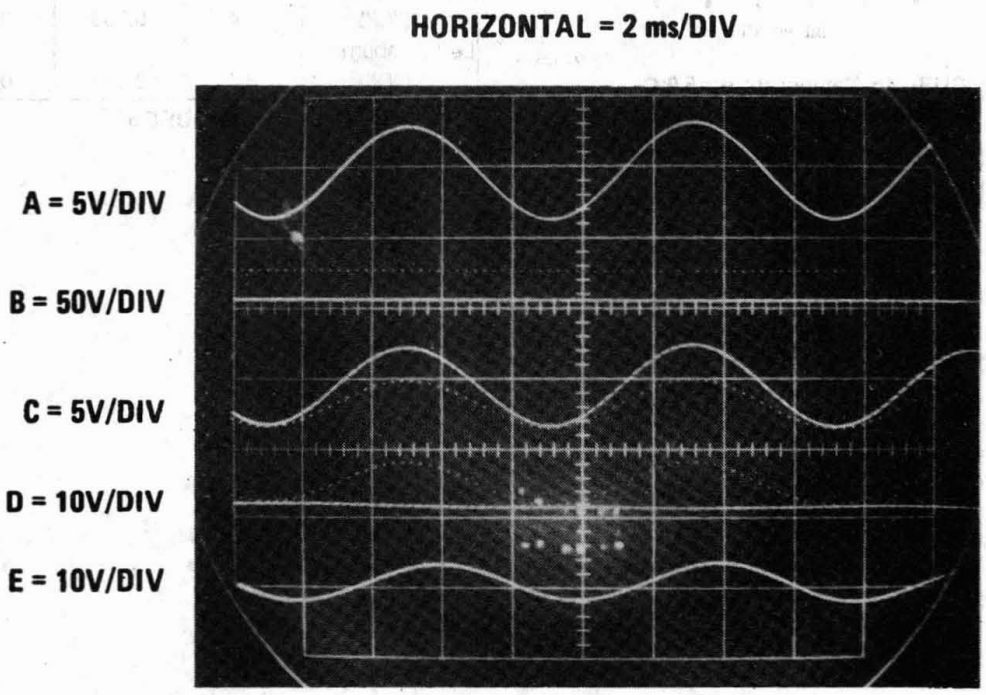


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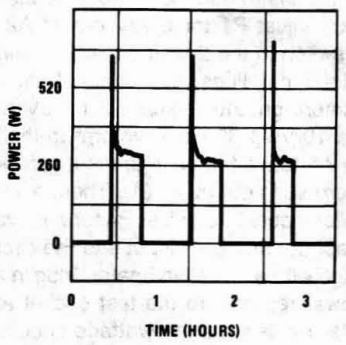
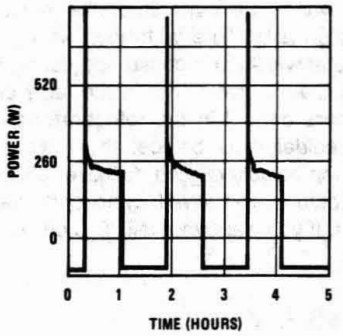
FIGURE 3



TL/H/5626–5

Temperature	Watts	Kilowatt-Hours/Cycle	Cost/Day	Cost/Year
5°C	260	0.119	$0.1147	$41.89
7°C	260	0.104	$0.0998	$36.44

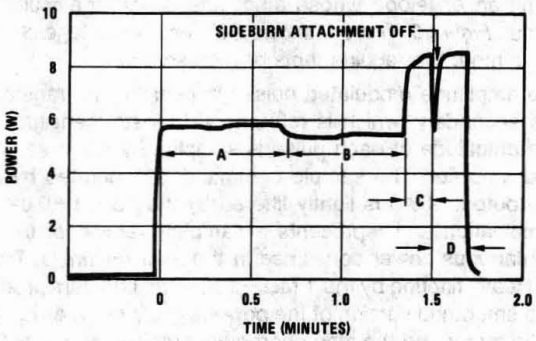
FIGURE 4a. Temperature = 7.0°C Compressor Duty Cycle = 40%



TL/H/5626–6

FIGURE 4b. Temperature = 5.0°C Compressor Duty Cycle = 46%

The strip chart of *Figure 5* is somewhat less depressing but no less informative. In this example, the watt-watt-hour meter was used to record power consumption during morning shaving with an electric razor. From the strip chart and the table it can be seen that various facial areas cost more to shave than others. The high power drawn by the sideburn attachment on the razor is somewhat compensated for by the relatively short period of time it is in use. A complete shave, including the 4 areas listed, costs 0.00692 cents/day or 8.68 cents per year. If this is too high, you can economize by growing a beard.



TL/H/5626–7

Facial Area	Power (W)	Watt-Hours	Cost (at 4¢ Kilowatt-Hours) Per Shave
Cheeks ("A")	5.8	0.173	0.00692¢
Upper/Lower Lip ("B")	5.4	0.123	0.00492¢
Right Sideburn ("C")	8.4	0.063	0.00252¢
Left Sideburn ("D")	8.4	0.061	0.00244¢

FIGURE 5

Circuit Applications of Sample-Hold Amplifiers

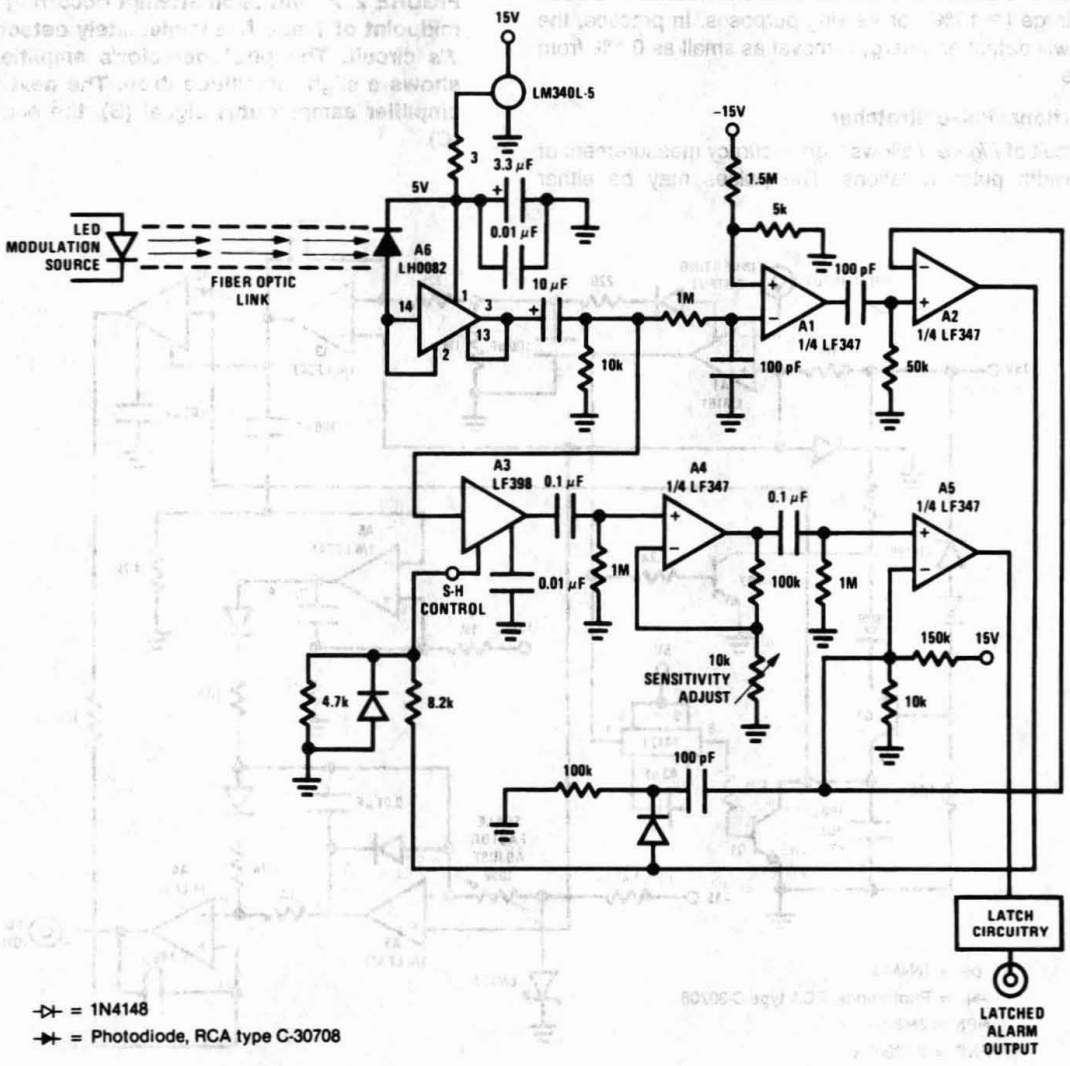
National Semiconductor
Application Note 266

Most designers are familiar with the sample-hold amplifier as a *system* component which is utilized in high speed data acquisition work. In these applications, the sample-hold amplifier is used to store analog data which is then digitized by a relatively slow A/D converter. In this fashion, high speed or multiplexed analog data can be digitized without resorting to complex and expensive ultra-high speed A/D converters.

The use of sample-hold amplifiers as *circuit* oriented components is not as common as the class of application described above. This is unfortunate, because sampling techniques allow circuit functions which are sophisticated, low cost and not easily achieved with other approaches. An excellent example is furnished by the fiber optic data link intrusion alarm of *Figure 1.*

Fiber Optic Data Link Intrusion Alarm

The circuit of *Figure 1* will detect an attempt to tap a fiber optic data link. It may be used with any fiber optic communication system which transmits data in pulse coded form. The circuit works by detecting any short-term change in the loss characteristics of the fiber optic line. Long term changes due to temperature and component aging do not affect the circuit. The amplitude of the pulses at the LH0082 fiber optic receiver IC (A6) will depend upon the characteristics of the photocomponents and the losses in the optical line. Any attempt to tap the fiber optic will necessitate removal of some amount of light energy. This will cause an instantaneous drop in the pulse amplitude at A6's output. The amplitude of each of A6's output pulses is sampled by the LF398 sample-hold amplifier (A3), A1 and A2 provide a delayed

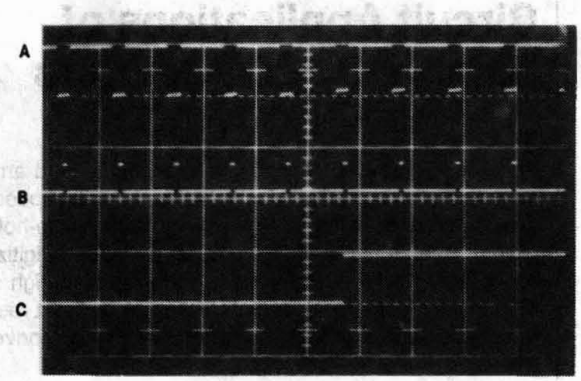


TL/H/5627–1

FIGURE 1. Fiber optic link eavesdropping attempts are immediately detected by this design. Working on a pulse-by-pulse comparison basis, A3 samples each input pulse and holds its output amplitude value at a DC level. Anything that disturbs the next input's amplitude causes a jump in this level; because A4 is an AC-coupled amplifier, the comparator and latch then activate.

sample-hold control pulse to A3, which insures that A6's output is sampled well after its output has settled. Under normal conditions, the pulse-to-pulse amplitude variations at A6's output will be negligible, and the output of A3 will be at a DC level. A4 is AC coupled and its output will be zero. During an intrusion attempt, energy will be removed from the line and A6's output will shift, causing A3 to jump to a new DC level. This shift will be AC amplified by A4 and the A5 comparator will trip, activating the latch circuitry.

Note that the circuit is not affected by slow drifts in circuit components over time and temperature because it is only sensitive to AC disturbances on the line. In addition, the frequency and pulse widths of the data may vary over wide ranges. The photo of *Figure 2* shows the circuit in operation. Trace A is A6's output. Trace B is the sample-hold control pin at A3 and Trace C is the latch-alarm output. In this figure, a disturbance on the fiber optic line has occurred just past the midpoint of the photo. This is reflected by the reduced amplitude of A6's output at this point. The latch-alarm output goes high just after the sample command rises, due to the sample-hold amplifier jumping to the new value at A6's output. In the photo, the disturbance has been made large (≅10%) for viewing purposes. In practice, the circuit will detect an energy removal as small as 0.1% from the line.



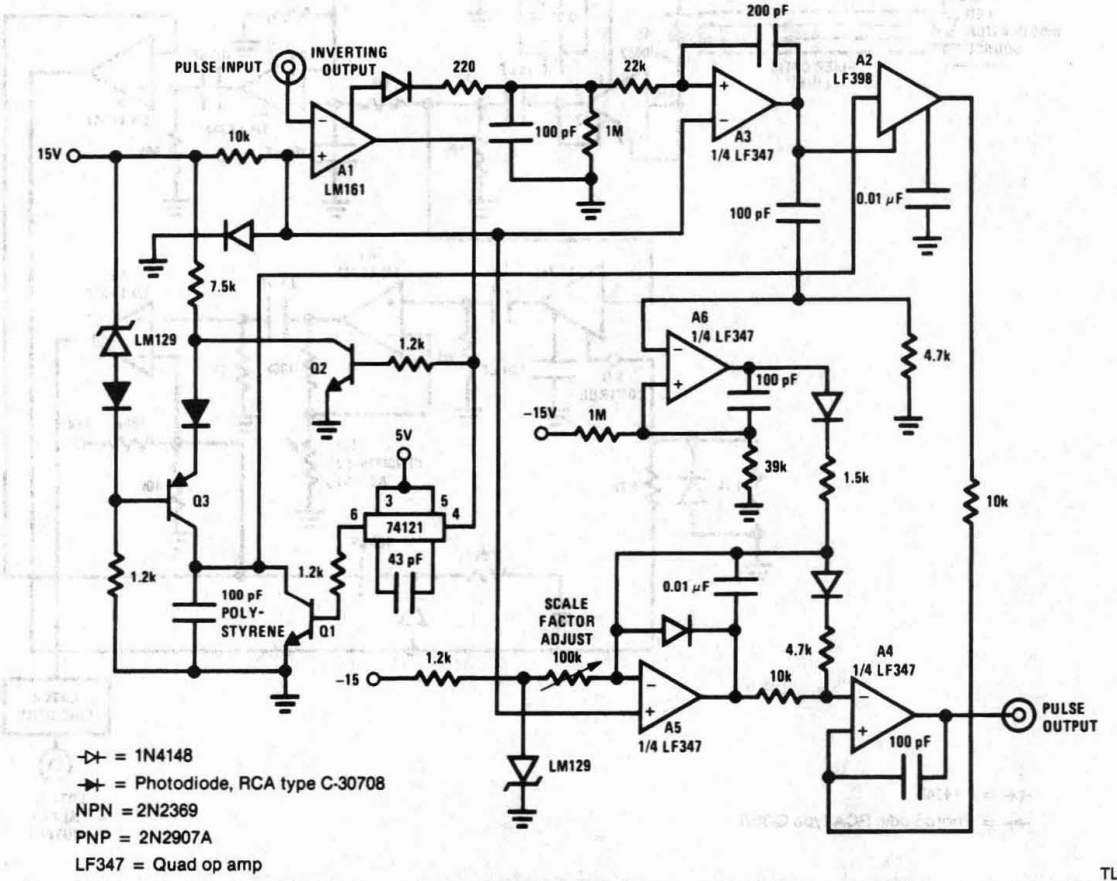
TL/H/5627–2

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 mSEC/DIV
B	10V/DIV	1 mSEC/DIV
C	10V/DIV	1 mSEC/DIV

FIGURE 2. An intrusion attempt occurring just past the midpoint of Trace A is immediately detected by *Figure 1's* circuit. The photodetector's amplifier output (A) shows a slight amplitude drop. The next time the S-H amplifier samples this signal (B), the alarm latch sets (C).

Proportional Pulse Stretcher

The circuit of *Figure 3* allows high accuracy measurement of short width pulse durations. The pulses may be either



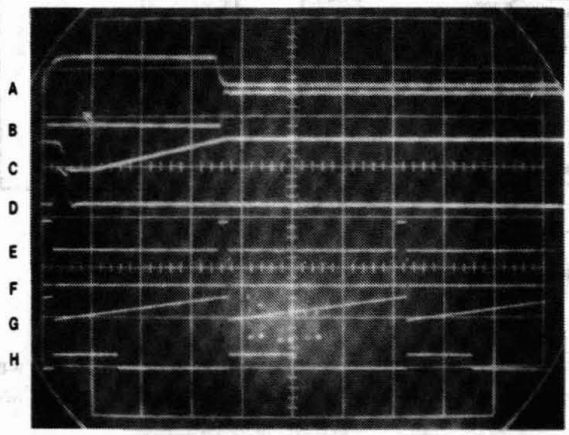
TL/H/5627–3

FIGURE 3. Pulse width measurement accuracy is enhanced by this pulse stretching circuit. A short input pulse triggers the 74121 one-shot and (via Q1) discharges the 100 pF capacitor while concurrently turning on the recharging current source, Q3. So long as the input pulse is present, the capacitor charges; when the pulse ends, the capacitor's voltage is proportional to the pulse's width. S-H amplifier A2 samples this voltage, and the resultant DC level controls the ON duration of the A4/A5 pulse width modulator.

repetitive or single-shot events. Using digital techniques, a 1% width measurement of a 1 μs event requires a 100 MHz clock. This circuit gets around this requirement by linearly amplifying the width of the input pulse with a time multiplying factor of 1000 or more. Thus, a 1 μs input event will yield a 1 ms output pulse which is easy to measure to 1%. This measurement capability is useful in high energy physics and nuclear instrumentation work, where short pulse width signals are common.

Figure 4, Trace A shows a 350 ns input pulse applied to the circuit of *Figure 3.* The A1 comparator output goes low (*Figure 4,* Trace B), triggering the DM74121 one shot, which resets the 100 pF capacitor to 0V via Q1 with a 50 ns pulse (Trace C). Concurrently, Q2 is turned off, allowing the A3 current source to charge the 100 pF capacitor in a linear fashion (*Figure 4,* Trace C). This charging continues until the circuit input pulse ends, causing A1's output to return high and cutting off the current source. The voltage across the 100 pF capacitor at this point in time is directly proportional to the width of the circuit input pulse. This voltage is sampled by the LF398 sample-hold amplifier (A2) which receives its sample-hold command from A3 (*Figure 4,* Trace E—note horizontal scale change at this point). A3 is fed from a delay network which is driven by A1's inverting output. The output of A2 is a DC voltage, which represents the width of the most recently applied pulse to the circuit's input. This DC potential is applied to A4, which along with A5 comprises a voltage controlled pulse width modulator. A5 ramps positive (*Figure 4,* Trace G) until it is reset by a pulse from A6, which goes high for a short period (*Figure 4,* Trace F) each time A3's output (Figure 4, Trace E) goes low. The ramps at A6's output are compared to A2's output voltage by A4, which goes high for a period linearly dependent on A2's output value (*Figure 4,* Trace H). This pulse is the circuit's output.

In this particular circuit, the time amplification factor is about 2000 with a 1 μs full-scale width giving a 1.4 ms output pulse. Absolute accuracy of the time expansion is 1% (10 ns) referred to input with resolution down to 2 ns. The 50 ns DM74121 reset pulse limits the minimum pulse width the circuit can measure.



TL/H/5627–4

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV
C	5V/DIV	100 nSEC/DIV
D	5V/DIV	100 nSEC/DIV
E	50V/DIV	500 μSEC/DIV
F	50V/DIV	500 μSEC/DIV
G	20V/DIV	500 μSEC/DIV
H	100V/DIV	500 μSEC/DIV

FIGURE 4. A sequence of events in *Figure 3's* circuit stretches a 350 ns input pulse (A) by a factor of 2000. When triggered, comparator A1 goes low (B). This action starts the recharging of a capacitor (C) after its previously stored charge has been dumped (D). When the input pulse ends, the capacitor's voltage is sampled under control of a delayed pulse (E) derived from the input amplifier's inverting output (F). The sampled and held voltage then turns off a voltage controlled pulse width modulator (G), and a stretched output pulse results (H).

Controlled Amplitude Pulser

Figure 5 depicts a circuit which converts an input pulse train into an amplitude stabilized pulse output which will drive a 20Ω load. The output pulse amplitude is adjustable from 0V to 10V and is stable over time, temperature and load changes. This circuit function is useful in automatic test equipment and general laboratory applications.

The circuit works by storing the sampled amplitude of the output pulse as a DC level, and supplying this information to a feedback loop which controls the voltage applied to the output switch. Each time a pulse is applied at the circuit input, the Q2-Q3 combination turns on and drives the load. Simultaneously, the A1 sample-hold amplifier is placed in the sample mode. When the pulse ends, A1's output is at a DC level equal to the amplitude of the output pulse. This level is compared to the amplitude set DC reference by A2, whose output drives Q1. Q1's emitter provides the DC supply level to the Q2-Q3 switch. This servo action forces the amplitude of the output pulse to be the same as the DC potential at the amplitude set potentiometer wiper, regardless of Q3 switch losses or loading. In *Figure 6,* Trace A is the circuit output. Traces B and C detail the rising and falling edges of the output (note horizontal sweep time change for B and C) with clean 50 ns transitions into the 20Ω load.

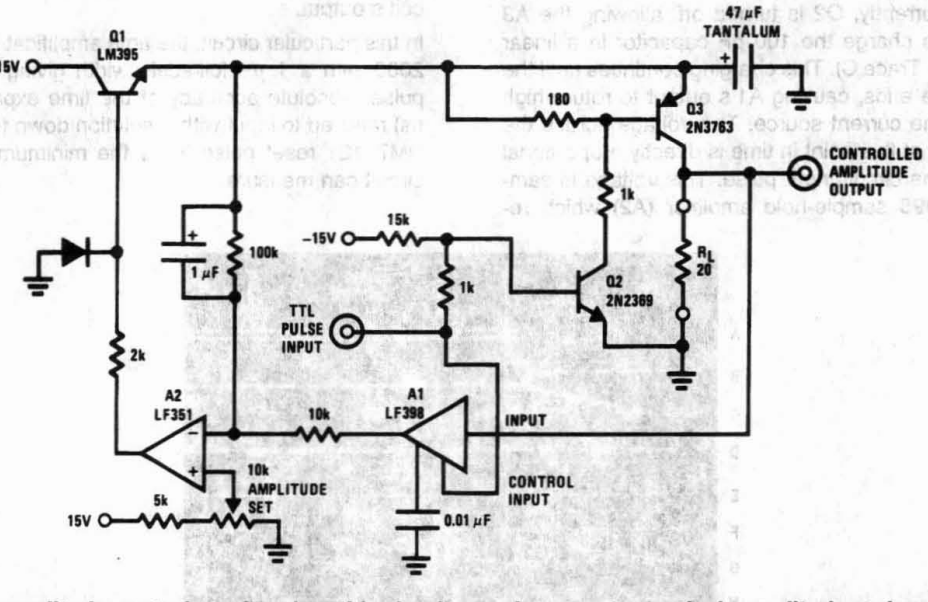


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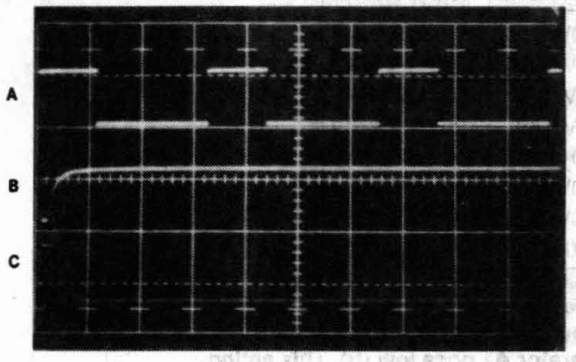
FIGURE 5. Pulse amplitude control results when this circuit samples an output pulse's amplitude and compares it with a preset reference level. When the output exceeds this reference, A2 readjusts switching transistor Q3's supply voltage to the correct level.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 mSEC/DIV
B	10V/DIV	100 nSEC/DIV
C	10V/DIV	100 nSEC/DIV

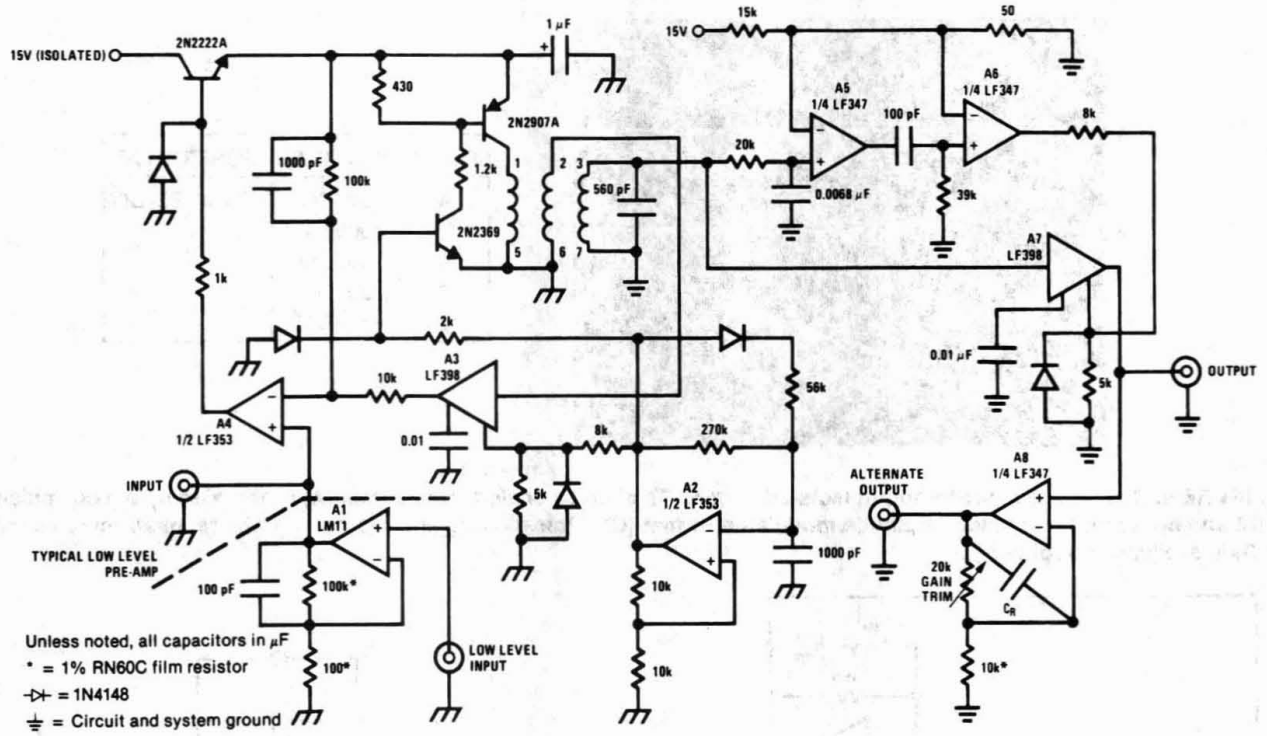
TL/H/5627–6

FIGURE 6. A 10V, 0.5A pulse (A) is amplitude stabilized by the S-H technique depicted in *Figure 5.* Note the clean 50 ns rise (B) and fall (C) times.

Isolated Input Signal Conditioning Amplifier

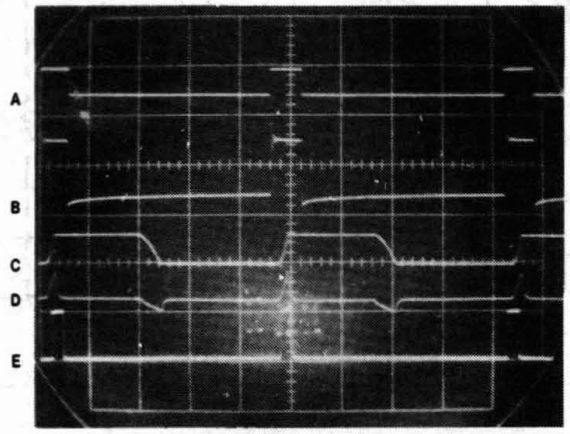
Figure 7 is a logical and very powerful extension of the controlled amplitude pulser shown in *Figure 5.* This circuit permits measurement of a small amplitude signal, e.g., thermocouples, in the presence of common-mode noise or voltages as high as 500V. This is a common requirement in industrial control systems. Despite the fact that the input terminals are fully galvanically isolated from the output, a transfer accuracy of 0.1% may be expected. With the optional low-level pre-amplifier shown, inputs as low as 10 mV full-scale may be measured.

The circuit works by converting the input signal into a pulse train whose amplitude is linearly dependent on the input signal value. This pulse train drives a transformer which provides total galvanic isolation of the input circuitry from ground. The transformer output is then demodulated back to a DC level to provide the circuit's system ground referenced output. The amplitude of the pulse train which drives the transformer is controlled by a loop very similar to the one described in *Figure 5.* The amplitude set potentiometer has been deleted, and the servo amplifier's "+" input becomes the circuit input. A1, a low drift *X1000* amplifier, may be employed for boosting low-level inputs. The pulse train is supplied by A2, which is set up as an oscillator (A2 output shown in *Figure 8,* Trace A). The feedback to the pulse amplitude stabilizing loop is taken from an isolated



TL/H/5627–7

FIGURE 7. Obtain input signal isolation using this circuit's dual S-H scheme. Analog input signals amplitude modulate a pulse train using a technique similar to that employed in *Figure 5*'s design. This modulated data is transformer coupled, and thereby isolated, to a DC filter stage, where it is resampled and reconstructed.



TL/H/5627–8

TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	100 µSEC/DIV
B	1V/DIV	100 µSEC/DIV
C	50V/DIV	100 µSEC/DIV
D	10V/DIV	100 µSEC/DIV
E	5V/DIV	100 µSEC/DIV

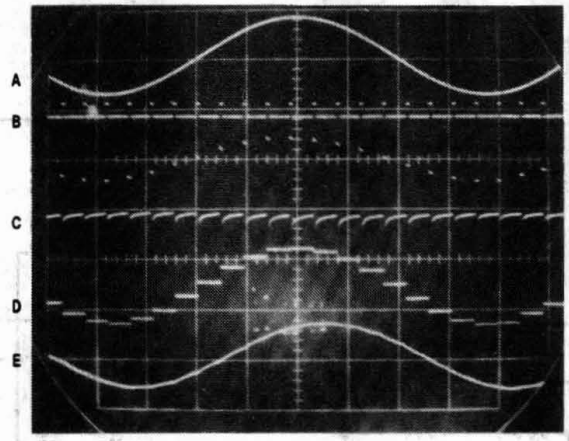
FIGURE 8. *Figure 7's* in-circuit oscillator (A2) generates both the sampling pulse (A) and the switching transistor's drive. Modulated by the analog input signal, Q2's (and therefore T1's) output (B) is demodulated by S-H amplifier A7. A5's output (C) and A6's input (D) and output (E) provide a delayed sample command.

secondary of the transformer, which insures high accuracy amplitude information transfer. The amplitude coded information at the transformer's secondary (*Figure 8,* Trace B) is demodulated back to a DC level by sample-hold amplifier, A7. A5 (output, *Figure 8,* Trace C) and A6 ("+" input, *Figure 8,* Trace D; output, *Figure 8,* Trace E) provide a delayed sample command to A7, ensuring accurate acquisition of the transformer's output pulse amplitude. A8 provides gain trimming and filtering capability.

Figure 9 provides very graphic evidence of the circuit at work. Here, a DC biased sine wave (*Figure 9,* Trace A) is fed into the circuit input. Trace B is the clock from A2's output. Trace C is the transformer secondary (input of A7 sample-hold amplifier) and Trace D is A7's output. Trace E shows the filter's output at A8.

Precision, High Efficiency Temperature Controller

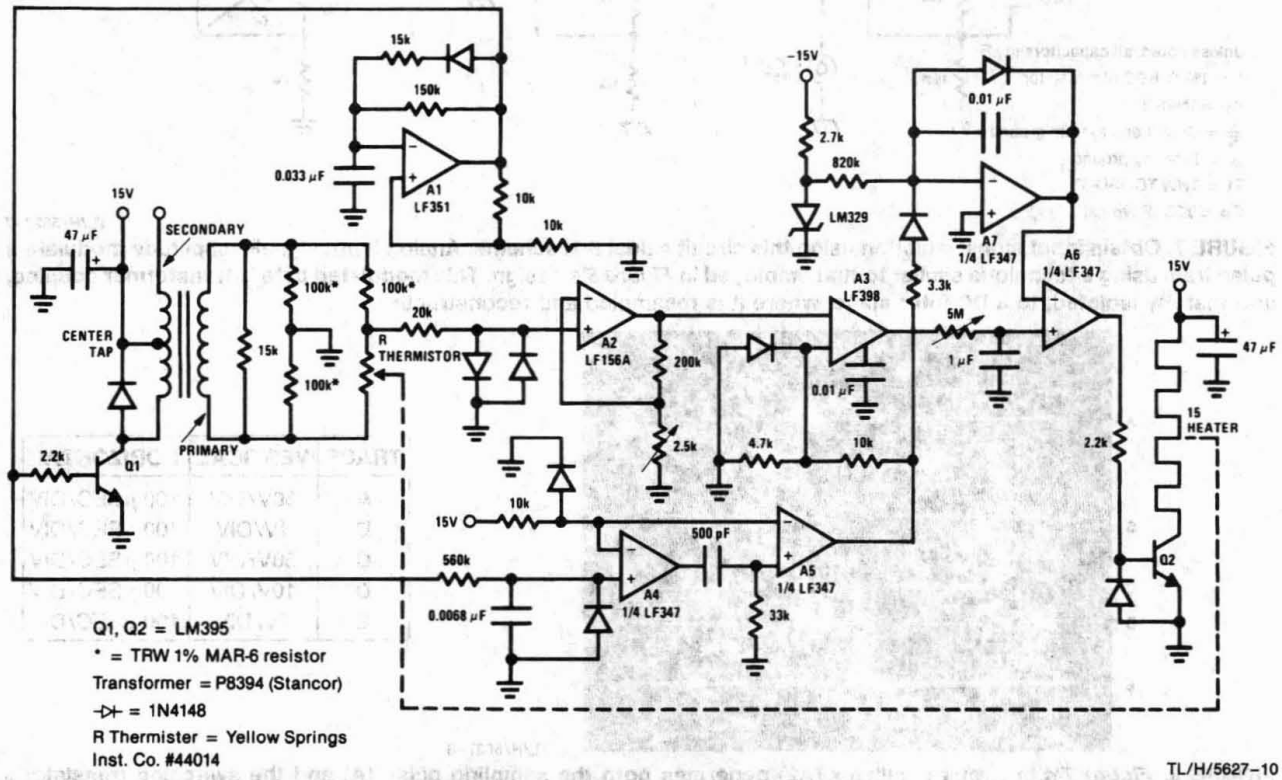
The sample-hold amplifier in *Figure 10* is used to provide very high stability in an oven temperature control circuit. In this circuit, the output signal of the pulse driven thermistor-bridge is ten times greater than the usual DC driven bridge. In thermistor-bridges, power dissipation in the resistors and thermistor is the limiting factor in how much DC bridge drive may be used. However, if the bridge drive is applied in the form of high voltage pulses at very low duty cycle, average power dissipation will be low and a high bridge output signal will result.



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 mSEC/DIV
B	100V/DIV	
C	5V/DIV	
D	5V/DIV	
E	5V/DIV	

TL/H/5627–9

FIGURE 9. Completely input-to-output isolated, *Figure 7's* circuit's analog input signal (A) is sampled by a clock pulse (B) and converted to a pulse amplitude modulated format (C). After filtering and resampling, the reconstructed signal (D) is available smoothed (E).

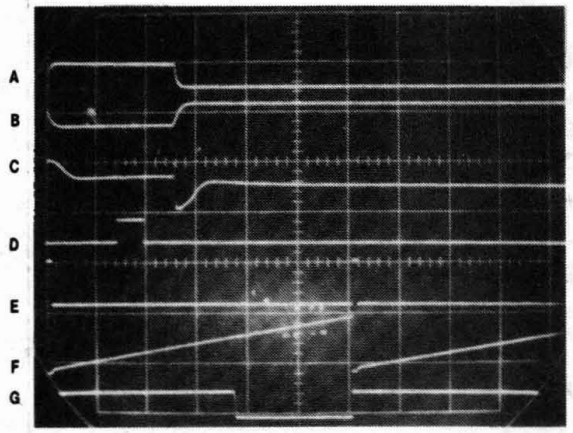


TL/H/5627–10

FIGURE 10. Tight temperature control results when high voltage pulses synchronously drive a thermistor-bridge—a trick that increases signal level—and are then sampled and used to control a pulse width modulated heater driver.

In *Figure 10,* this operation is implemented by having the A1 oscillator drive Q1 to energize a common 24V transformer used "backwards". The transformer's floated output is a 100V pulse which is applied directly across the thermistor-bridge. With one side of the bridge output grounded, the bridge drive with respect to ground appears as complementary 50V pulses (*Figure 11,* Traces A and B). A2 provides amplification of the bridge's pulsed output (*Figure 11,* Trace C). A3, a sample-hold amplifier, samples the middle of A2's output pulses and has a DC output equal to the amplitude of these pulses. Proper timing for A3's sample command (*Figure 11,* Trace D) is provided by the A4-A5 pair and their associated RC networks. The DC output of A3 is low-pass filtered and fed to A6, which combines with A7 to form a simple pulse width modulator. The output of A7 is a ramp (*Figure 11,* Trace F—note horizontal scale change) which is periodically reset by A5's output (*Figure 11,* Trace E). This ramp is compared at A6 to A3's output, and the resultant pulse at A6's output (*Figure 11,* Trace G) is used to drive the Q2 heater control switch. In this fashion, the ON time of the pulse applied to the heater will be proportional to the sensed offset at the thermistor-bridge. Thermal feedback from the heater to the thermistor completes a loop around the circuit. The 5 MΩ potentiometer is used to adjust the time constant of this loop, and the 2.5k potentiometer at A2 sets the gain.

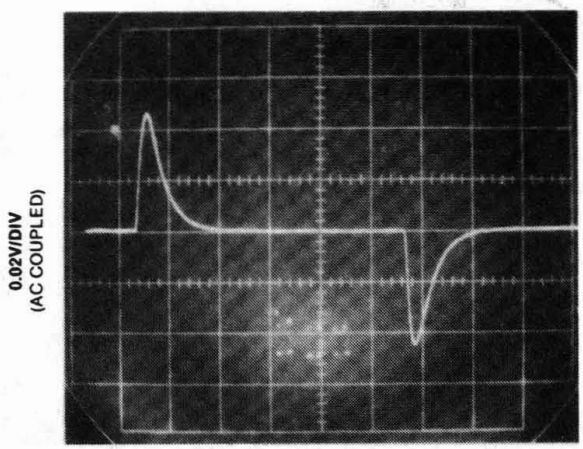
In operation, with the thermistor and heater tightly coupled, the time constant of the loop is adjusted by applying small step changes in the temperature setpoint. This is done by alternately opening and closing a switch across a 100Ω resistor in series with one of the bridge resistors. For the thermistor shown, this represents a 0.02°C step. The response of the loop to these steps can be monitored at A3's output. With the loop time constant and gain properly adjusted, A3's output will settle in a minimum amount of time in response to the steps. *Figure 12* shows settling for both "+" and "−" steps, with settling inside 2 seconds for either polarity step.



TRACE	VERTICAL	HORIZONTAL
A	100V/DIV	200 μSEC/DIV
B	100V/DIV	200 μSEC/DIV
C	5V/DIV	200 μSEC/DIV
D	10V/DIV	200 μSEC/DIV
E	5V/DIV	1 mSEC/DIV
F	10V/DIV	1 mSEC/DIV
G	50V/DIV	1 mSEC/DIV

TL/H/5627–11

FIGURE 11. Driving a thermistor-bridge with complementary high voltage pulses (A and B) permits high gain amplification without drift problems (C). Driven by a delayed sample command (D), a S-H amplifier converts the bridge's error signal to a DC level (E) that controls a pulse width modulated heater driver (F and G).



TL/H/5627–12

FIGURE 12. Tight heater to thermistor coupling and careful calibration can provide rapid temperature restabilization. Here the controlled oven recovers within 2 seconds after ±0.002°C steps.

Once adjusted, and driving a well insulated and designed oven, the circuit's control stability can be monitored. The high output signal levels from the bridge, in combination with the gain provided by A2, yield extremely good performance.

Sample-Hold Amplifier Terms

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Time: The delay required between hold command and an input analog transition, so that the transition does not affect the held output.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the hold logic command.

Hold Step: The voltage step at the output of the sample-hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is specified, usually 5V.

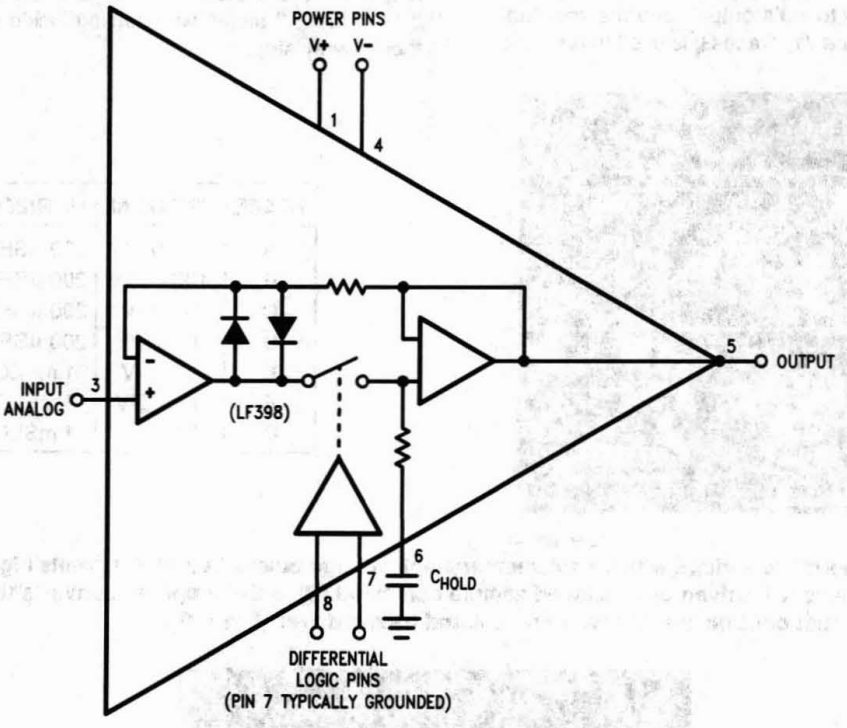


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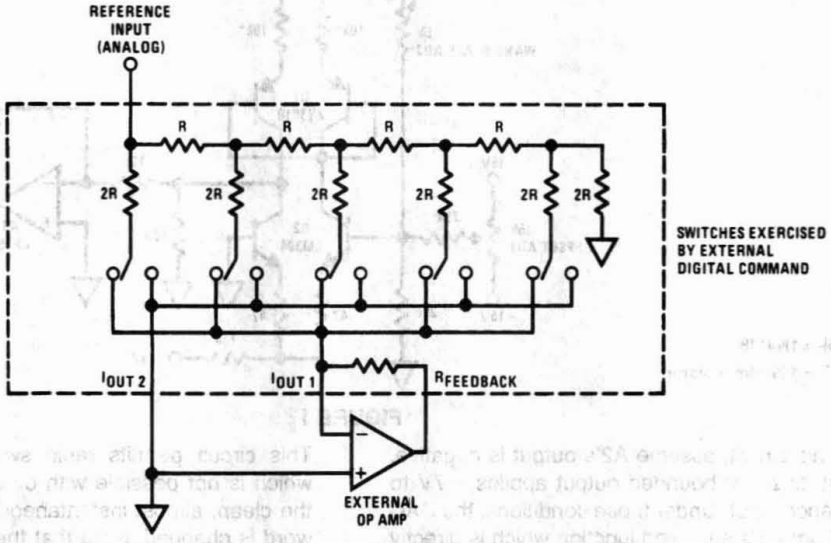
FIGURE 13. Typical Sample-Hold IC Amplifier

Circuit Applications of Multiplying CMOS D to A Converters

National Semiconductor
Application Note 269

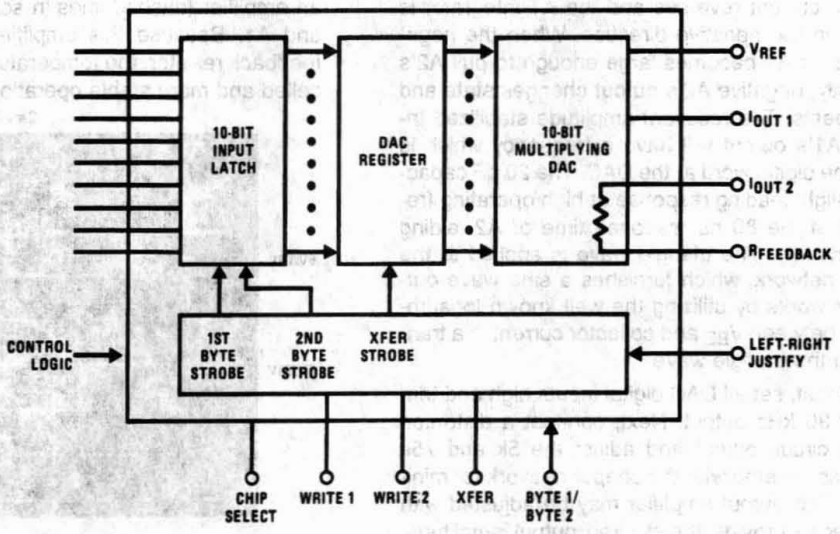
The 4-quadrant multiplying CMOS D to A converter (DAC) is among the most useful components available to the circuit designer. Because CMOS DACs allow a digital word to operate on an analog input, or vice versa, the output can represent a sophisticated function. Unlike most DAC units, CMOS types permit true bipolar analog signals to be applied to the reference input of the DAC (see shaded area for CMOS DAC details).

This feature is one of the keys to the CMOS DAC's versatility. Although D to A converters are usually thought of as system data converters, they can also be used as circuit elements to achieve complex functions. Some CMOS DACs contain internal logic which makes interface with microprocessors and digital systems easy. In circuit oriented applications, however, the "bare bones" DACs will usually suffice. As an example, *Figure 1* shows a 0 kHz–30 kHz variable frequency sine wave generator which has essentially instantaneous response to digital commands to change frequency. This capability is valuable in automatic test equipment and instrumentation applications and is not readily achievable with normal sine wave generation techniques. The linearity of output frequency to digital code input is within 0.1% for each of the 1024 discrete output frequencies the 10-bit DAC can generate.



Details (Simplified) of CMOS DAC1020—Last 5 Bits Shown

Other CMOS DACs are similar in the nature of operation but also include internal logic for ease of interface to microprocessor based systems. Typical is the DAC1000 shown below.



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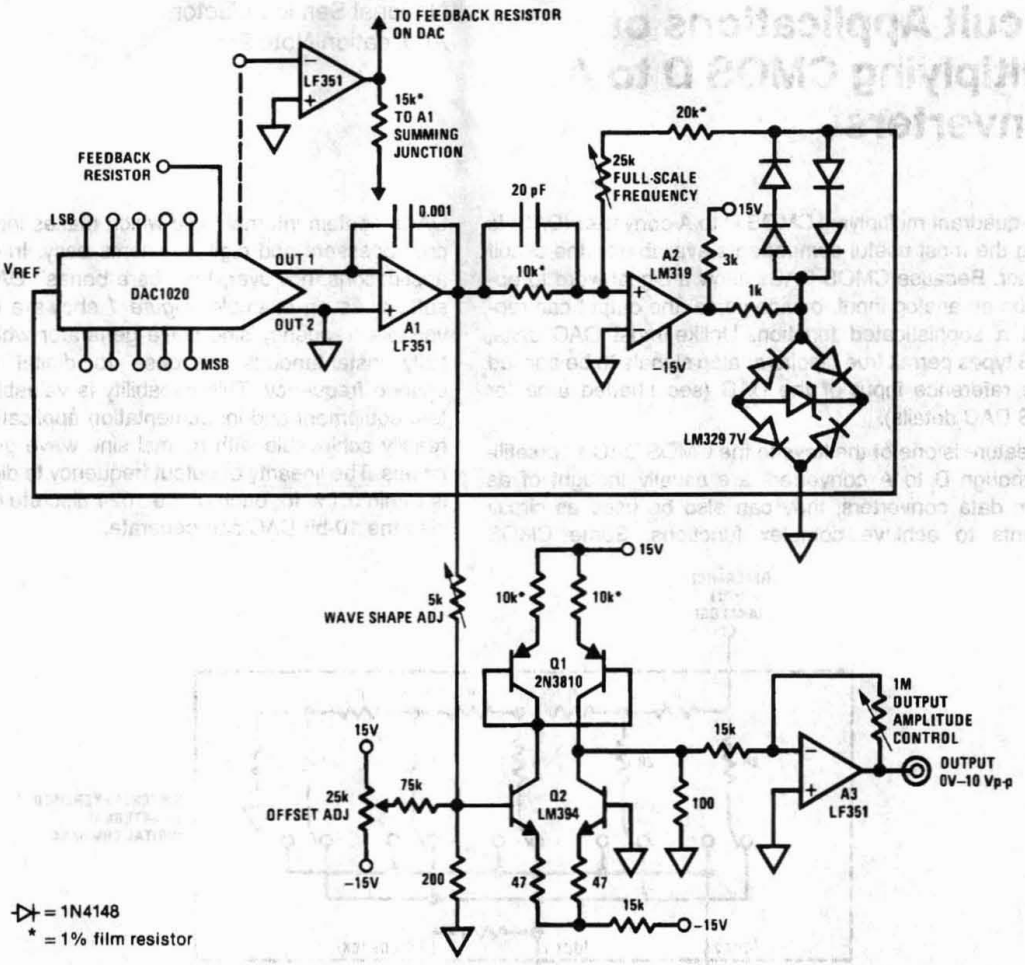

TL/H/5628–2

FIGURE 1

To understand this circuit, assume A2's output is negative. This means that its zener bounded output applies −7V to the DAC's reference input. Under these conditions, the DAC pulls a current from A1's summing junction which is directly proportional to the digital code applied to the DAC. A1, an integrator, responds by ramping in the positive direction. When A1 ramps far enough so that the potential at A2's "+" input just goes positive, A2's output changes state and the potential at the DAC's reference input becomes +7V. The DAC output current reverses and the A1 integrator is forced to move in the negative direction. When the negative-going output of A1 becomes large enough to pull A2's "+" input slightly, negative A2's output changes state and the process repeats. The resultant amplitude stabilized triangle wave at A1's output will have a frequency which is dependent on the digital word at the DAC. The 20 pF capacitor provides a slight leading response at high operating frequencies to offset the 80 ns response time of A2, aiding overall circuit linearity. The triangle wave is applied to the Q1–Q2 shaper network, which furnishes a sine wave output. The shaper works by utilizing the well known logarithmic relationship between V_{BE} and collector current in a transistor to smooth the triangle wave.

To adjust this circuit, set all DAC digital inputs high and trim the 25k pot for 30 kHz output. Next, connect a distortion analyzer to the circuit output and adjust the 5k and 75k potentiometers associated with the shaper network for minimum distortion. The output amplifier may be adjusted with its potentiometer to provide the desired output amplitude.

This circuit permits rapid switching of output frequency which is not possible with other methods. *Figure 2* shows the clean, almost instantaneous response when the digital word is changed. Note that the output frequency shifts immediately by more than an order of magnitude with no untoward dynamics or delays. If operation over temperature is required, the absolute change in resistance in the DAC's internal ladder network may cause unacceptable errors. This can be corrected by reversing A2's inputs and inserting an amplifier (dashed lines in schematic) between the DAC and A1. Because this amplifier uses the DAC's internal feedback resistor, the temperature error in the ladder is cancelled and more stable operation results.

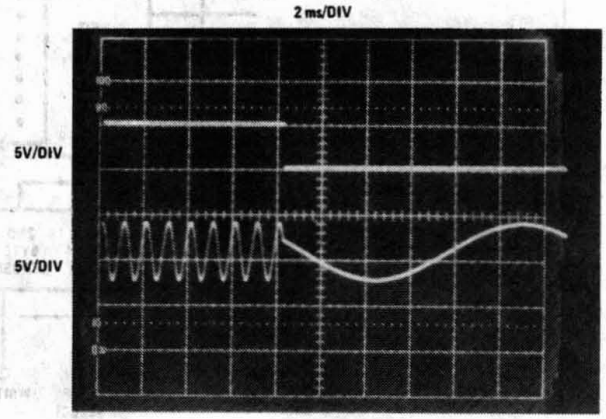

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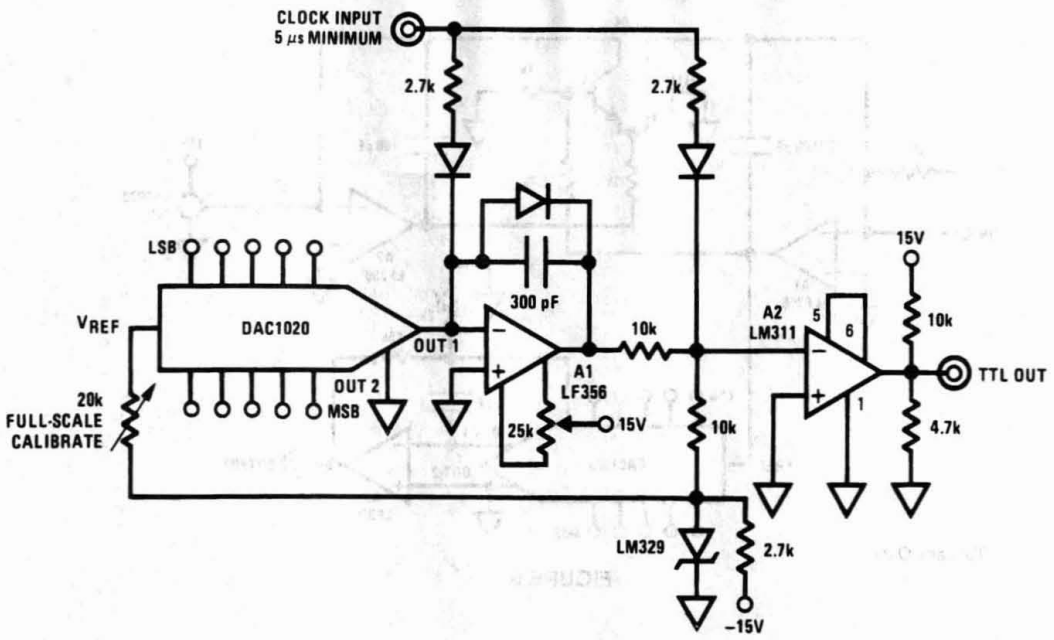
FIGURE 2



TL/H/5628–4

FIGURE 3

Digitally Programmable Pulse Width Modulator

The circuit of *Figure 3* allows the DAC inputs to control a pulse width. This capability has been used in automatic testing of secondary breakdown limits in switching transistors. The high resolution of control the DAC exercises over the pulse width is useful anywhere wide range, precision pulse width modulation is necessary. In this circuit, the length of time the A1 integrator requires to charge to a reference level is determined by the current coming out of the DAC. The DAC output current is directly proportional to the digital input code. Both the DAC analog input and the reference trip point are derived from the LM329 voltage reference. During the time the integrator output (*Figure 4*, Trace A) is below the trip point, the A2 comparator output remains high (*Figure 4*, Trace B). When the trip point is exceeded, A2's output goes low. In this fashion, the DAC input code can vary the output pulse width over a range determined by the DAC resolution. Traces C, D and E show the fine detail of the resetting sequence (note expanded horizontal scale for these traces). Trace C is the 5 μs clock pulse. When this pulse rises, the A1 integrator output (Trace D) is forced negative until it bounds against the diode in its feedback loop. During the time the clock pulse is high, the current through the 2.7k diode path forces A2's output low. When the clock pulse goes low, A2's output goes high and remains high until the A1 integrator output amplitude exceeds the trip point. To calibrate this circuit set all DAC bits high and adjust the "full-scale calibrate" potentiometer for the desired full-scale pulse width. Next, set only the DAC LSB high and adjust the A1 offset potentiometer for the appropriate length pulse, e.g., 1/1024 of the full-scale value for a 10-bit DAC. If the 2.2mV/°C drift of the clamp diode in A1's feedback loop is objectionable it can be replaced with an FET switch.

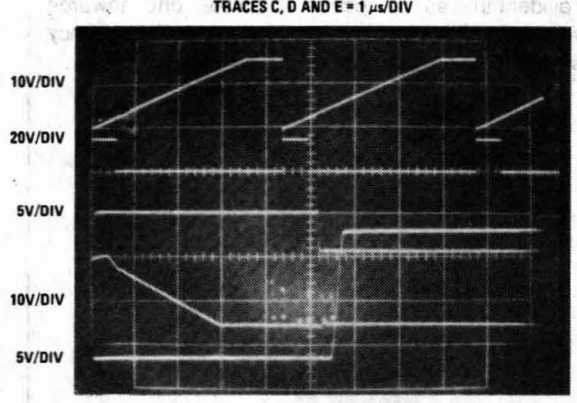


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FIGURE 4

Digitally Controlled Scale Factor Logarithmic Amplifier

Wide dynamic measurement range is required in many applications, such as photometry. Logarithmic amplifiers are commonly employed in these applications to achieve wide measurement range. In such applications it is often required to be able to set the scale factor of the logarithmic amplifier. A DAC controlled circuit permits this to be done under digital control. *Figure 5* shows a typical logarithmic amplifier circuit. Q1 is the actual logarithmic converter transistor, while Q2 and the 1 kΩ resistor provide temperature compensation. The logarithmic amplifier output is taken at A3. The digital code applied to the DAC will determine the overall scale factor of the input voltage (or current) to output voltage ratio.

Digitally Programmable Gain Amplifier

Figure 6 shows how a CMOS DAC can be used to form a digitally programmable amplifier which will handle bipolar input signals. In this circuit, the input is applied to the amplifier via the DAC's feedback resistor. The digital code selected at the DAC determines the ratio between the fixed DAC feedback resistor and the impedance the DAC ladder presents to the op amp feedback path. If no digital code (all zeros) is applied to the DAC, there will be no feedback and the amplifier output will saturate. If this condition is objectionable, a large value (e.g. 22 MΩ) resistor can be shunted across the DAC feedback path with minimal effect at lower gains. It is worth noting that the gain accuracy of this circuit is directly dependent on the open loop gain of the amplifier employed.

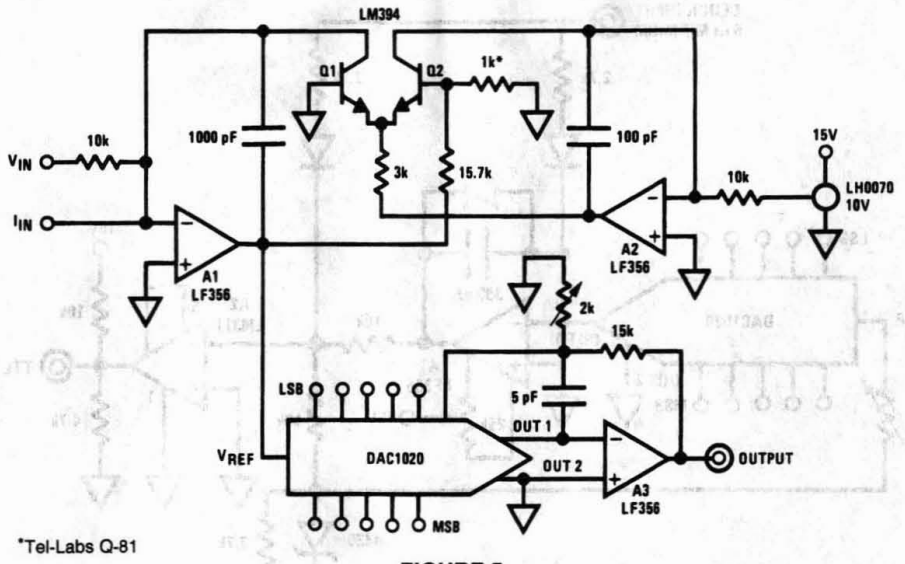

FIGURE 5

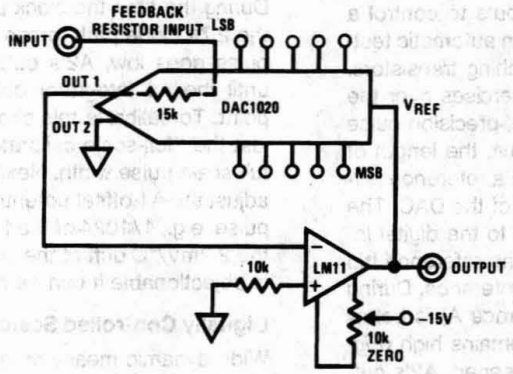

FIGURE 6

Digitally Controlled Filter

In *Figure 7* the DAC is used to control the cutoff frequency of a filter. The equation given in the figure governs the cutoff frequency of the circuit. In this circuit, the DAC allows high resolution digital control of frequency response by effectively varying the time constant of the A3 integrator. *Figure 8* dramatically demonstrates this. Here, the circuit is driven from the test circuit shown in *Figure 7*.

As each input square wave is presented to the filter the one-of-ten decoder sequentially shifts a "one" to the next DAC digital input line. Trace A is the input waveform, while Trace B is the waveform at A1's output (the reference input of the DAC). The circuit output at A3 appears as Trace C. It is clearly evident that as the decoder shifts the "one" towards the lower order DAC inputs the circuit's cutoff frequency decays rapidly.

Test Circuit

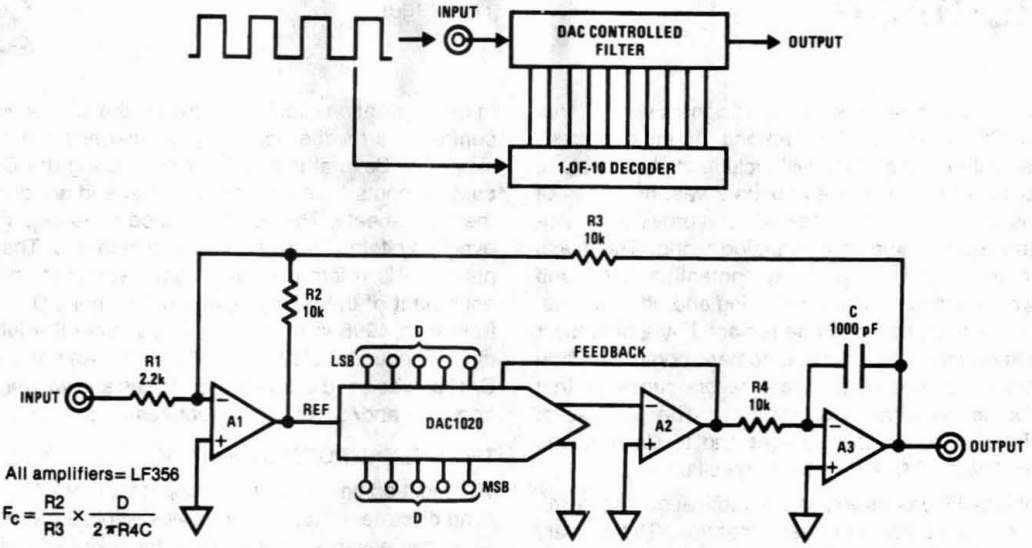

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FIGURE 7

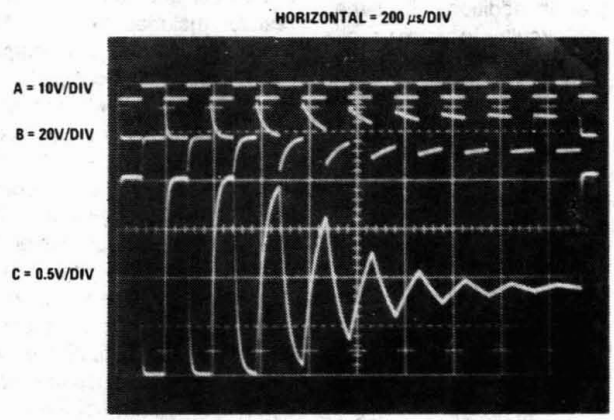

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FIGURE 8

AN-271

Applying the New CMOS MICRO-DAC™

National Semiconductor
Application Note 271
Tim Regan

Most microprocessor based systems designers will find that the new CMOS MICRO-DAC are among the most interesting and versatile devices they will include in their system. The availability of these devices opens a vast new area of applications where the microprocessor can provide an intelligent controlling function in the analog world. Traditional analog control devices, primarily potentiometers and switches which require a time-consuming and often erroneous human interface, can often be replaced by a processor and DACs to perform precise and automatic controls. A little creative thinking can easily generate several functions that could be better performed automatically. The purpose of this note is to stimulate this thought and to illustrate the versatility of CMOS DACs to achieve results.

The use of CMOS processing in the fabrication of the MICRO-DAC offers several important features. The primary advantage is that the current switching R-2R ladder network, used for the actual D to A conversion, can conduct current in both directions (sourcing or sinking current at its analog output) to control either a positive or negative fixed voltage reference or an AC signal. In addition, all of the necessary digital input conditioning circuitry to permit a direct microprocessor interface with no additional logic devices needed is included with minimal device power requirements. All of the MICRO-DAC can be controlled from an 8-bit data bus regardless of the number of digital inputs for a particular device. The operation of the R-2R ladder and the digital interface signal requirements are explained in detail on the actual device data sheets.

Resolution and linearity are the most important characteristics of the analog output of any D to A. Linearity is important to insure that each and every analog output quantity is predictable within a given tolerance (specified as a percent of the full-scale range) for any applied digital word. Resolution defines the number of possible analog output quantities available within a given range. Higher resolution in a DAC serves to minimize the gaps in the analog output inherent in digitally-based controls. The new line of MICRO-DAC offers a wide variety of converters to fit the accuracy and resolution requirements of a great number of applications. The device part numbers are summarized in *Figure 1*.

In the application circuits that follow, the connections for the control pins for the actual digital interface are omitted for simplicity. Several methods of configuring the DAC to accept its inputs from a processor exist and are described on the data sheets. The actual method used depends on the overall system provisions and requirements. The digital input code is referred to as D and represents the decimal equivalent of the binary input. For example, D would range from 0 to 4095 in steps of 1 to describe the full range of digital inputs for a 12-bit MICRO-DAC. Any of the MICRO-DAC can be used in any of the circuits shown, depending on accuracy and/or resolution requirements.

THE DIGITAL POTENTIOMETER

The most common and basic application of a DAC is generating discrete voltage output levels within a given span, and serving in essence as an attenuator (*Figure 2*). The applied digital input word multiplies the applied reference voltage, and the output voltage is this product normalized to the DAC's resolution. The op amp shown is used to convert the output current from the DAC to a voltage via a feedback resistor included in the DAC (R_{fB}). This output current ranges from a near zero output leakage (on the order of 10 nA) for an applied code of all zeros (D = 0), to a full-scale value ($D = 2^n - 1$, where n is the DAC's bits of resolution) of V_{REF} divided by the R value of the internal R-2R ladder network (nominally 15 kΩ). The current at $I_{OUT\ 2}$ is equal to that caused by the one's complement of the applied digital input, so while $I_{OUT\ 1}$ is at full-scale, $I_{OUT\ 2}$ will be zero. Note that the output voltage is the opposite polarity of the applied reference voltage, but since CMOS DACs can accept bipolar reference voltages, if a positive output is needed, a negative reference can be applied. To preserve the linearity of the output, the two current output pins of the DAC must be as close to 0V as possible, which requires the input offset voltage of the op amp to be nulled. The amount of linearity error degradation is approximately $V_{OS} \div V_{REF}$. For AC signal attenuation, in audio applications for example, the DAC's linearity over the full range of the applied reference voltage, even as it passes through zero, is sufficiently good enough to distort a 10V peak sine wave by only 0.004%.

Linearity Error (% of Full-Scale)	Resolution		
	8 Bits 256 Output Steps	10 Bits 1024 Output Steps	12 Bits 4096 Output Steps
±0.012%			DAC1208, DAC1230
±0.024%			DAC1209, DAC1231
±0.05%	DAC0830	DAC1000, DAC1006	DAC1210, DAC1232
±0.1%	DAC0831	DAC1001, DAC1007	
±0.2%	DAC0832	DAC1002, DAC1008	

FIGURE 1. The MICRO-DAC Family

The feedback capacitor shown in *Figure 2* is added to improve the settling time of the output as the input code is changed. With no compensation, a fair amount of overshoot and ringing appears at the output due to a feedback pole formed by the feedback resistor, and the output capacitance of the DAC, which appears from the (−) input of the op amp ground.

It is most desirable to select an op amp for use with the MICRO-DAC which combines good DC characteristics, primarily low V_{OS} and low V_{OS} drift, with fast AC characteristics such as slew rate, settling time and bandwidth. Such a combination is difficult to find in a single op amp for use with the higher accuracy 12-bit DACs. *Figure 3* shows an op amp configuration which combines the excellent DC input characteristics of the LM11 with the fast response of an LF351 BI-FET™ op amp.

The low cost, high resolution, and stability with time and temperature of the MICRO-DAC allow precise output levels that rival the capability of the best multiple turn potentiometers, and can automatically be adjusted, as required, by a controlling microprocessor.

LEVEL SHIFTING THE OUTPUT RANGE

As shown in *Figure 4*, the zero code output of the DAC can be shifted, if desired, to any level by summing a fixed current to the DAC's current output terminal, offsetting the output voltage of the op amp. The applied reference voltage now serves as the output span controller and is fractionally added to the output as a function of the applied code.

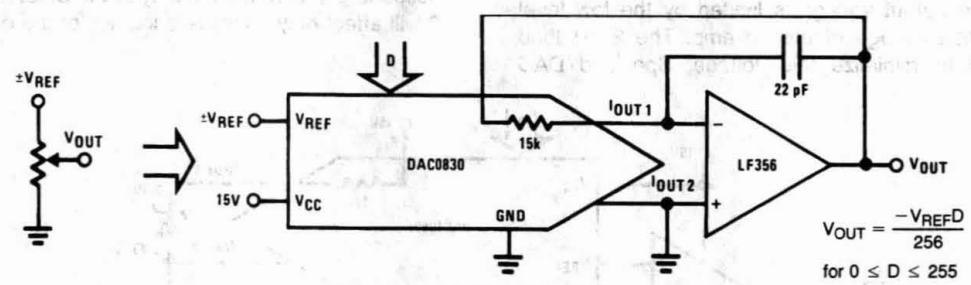

FIGURE 2. The Digital Pot

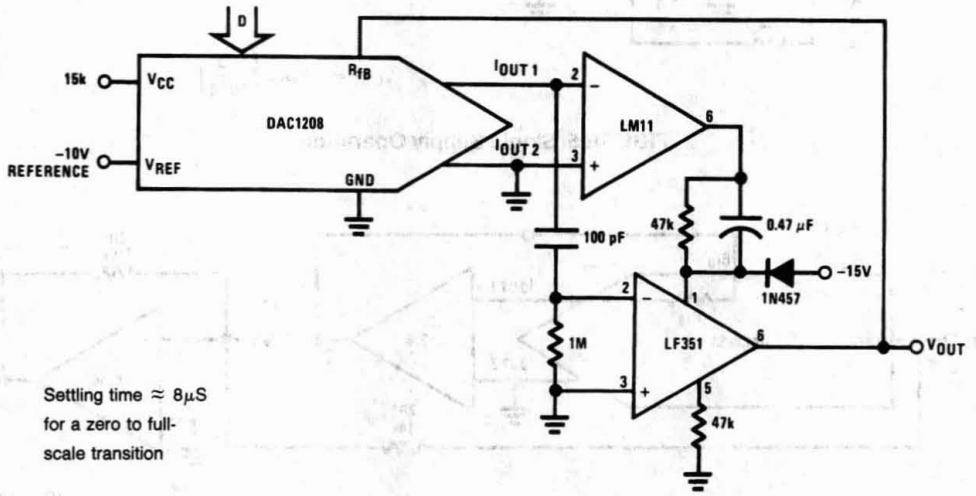

FIGURE 3. Composite Amplifier for Good DC Characteristics and Fast Output Response

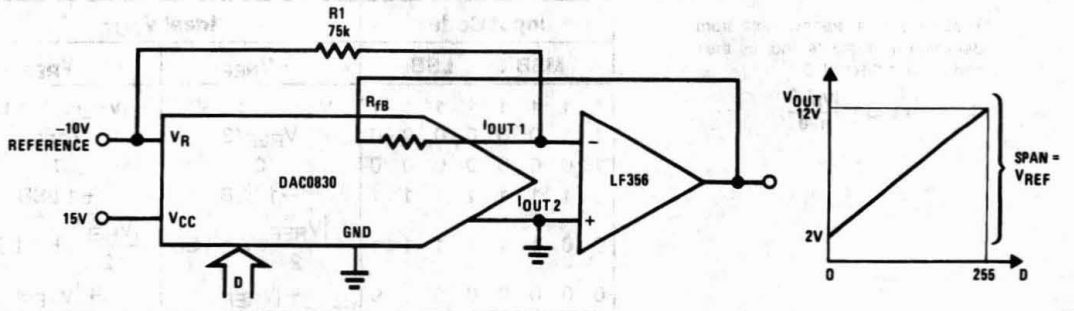

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FIGURE 4. Level Shifted Output

$$V_{OUT} = -V_{REF}\left[\frac{R_{fB}}{R1} + \frac{D}{256}\right]$$

SINGLE SUPPLY OPERATION

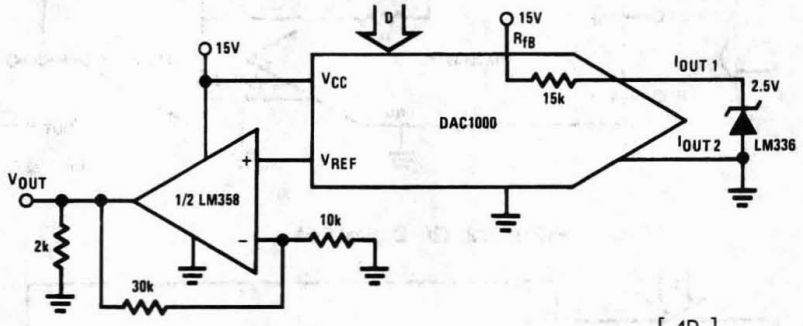
The R-2R ladder can be operated as a voltage switching network to circumvent the output voltage inversion inherent in the current switching mode. This allows single supply operation. In *Figure 5*, the reference voltage is applied to the $I_{OUT\ 1}$ terminal, and is attenuated by the R-2R ladder in proportion to the applied code, and output to the V_{REF} terminal with no phase inversion. To insure linear operation in this mode, the applied reference voltage must be kept less than 3V for the 10-bit DACs or less than 5V for the 8-bit DACs. The applied supply voltage to the DAC must be at least 10V more positive than the reference voltage to insure that the CMOS ladder switches have enough voltage overdrive to fully turn on. An external op amp can be added to provide gain to the DAC output voltage for a wide overall output span.

The zero code output voltage is limited by the low level output saturation voltage of the op amp. The 2 kΩ load resistor helps to minimize this voltage. Specified DAC linearity can be obtained in this circuit with the 8 and 10-bit MICRO-DAC, but is difficult because of the very low value reference required with the 12-bit parts. The resistance to ground of the V_{REF} terminal is nominally 15 kΩ, independent of the digital input code.

BIPOLAR OUTPUT FROM A FIXED REFERENCE VOLTAGE

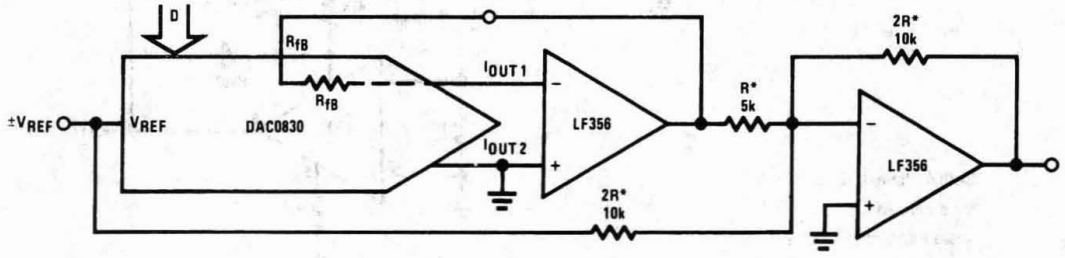
The use of a second op amp in the analog output circuitry can provide a bipolar output swing from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word to allow 2-quadrant multiplication of the reference voltage. The polarity of the reference can still be reversed or be an AC signal to realize full 4-quadrant multiplication. This circuit is shown in *Figure 6*.

Only the input offset voltage of amplifier OA 1 needs to be nulled to preserve the linearity of the DAC. The offset of OA 2 will affect only absolute accuracy of the output voltage.



$$V_{OUT} = +V_{REF}\left[\frac{4D}{1024}\right]$$

FIGURE 5. Single Supply Operation



TL/H/5629–2

$$V_{OUT} = V_{REF}\frac{(D - 128)}{128}$$

*These resistors are available from Beckman Instruments, Inc. as their part no. 694-3-R10K-Q

$$1\ LSB = \frac{|V_{REF}|}{128}$$

Input Code MSB . . . LSB								Ideal V_{OUT} $+V_{REF}$	Ideal V_{OUT} $-V_{REF}$
1	1	1	1	1	1	1	1	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
1	1	0	0	0	0	0	0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	-1 LSB	$+1$ LSB
0	0	1	1	1	1	1	1	$-\frac{\lvert V_{REF}\rvert}{2} - 1$ LSB	$\frac{\lvert V_{REF}\rvert}{2} + 1$ LSB
0	0	0	0	0	0	0	0	$-\lvert V_{REF}\rvert$	$+\lvert V_{REF}\rvert$

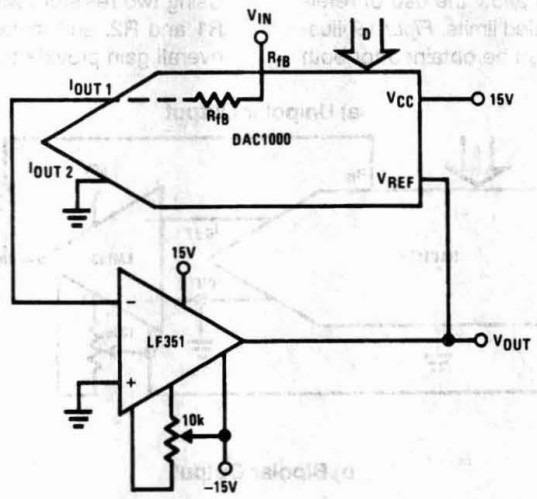
FIGURE 6. Bipolar Output from a Fixed Reference Voltage

DAC CONTROLLED AMPLIFIER

In the circuit of *Figure 7*, the DAC is used as the feedback element for an inverting amplifier configuration. The R–2R ladder digitally adjusts the amount of output signal fed back to the amplifier's summing junction. The feedback resistance can be thought of as varying from ≅ 15 kΩ to ∞ as the input code changes from full-scale to zero. The internal R_{fB} is used as the amplifier's input resistor. It is important to note that when the input code is all zeros the feedback loop is opened and the op amp output will saturate.

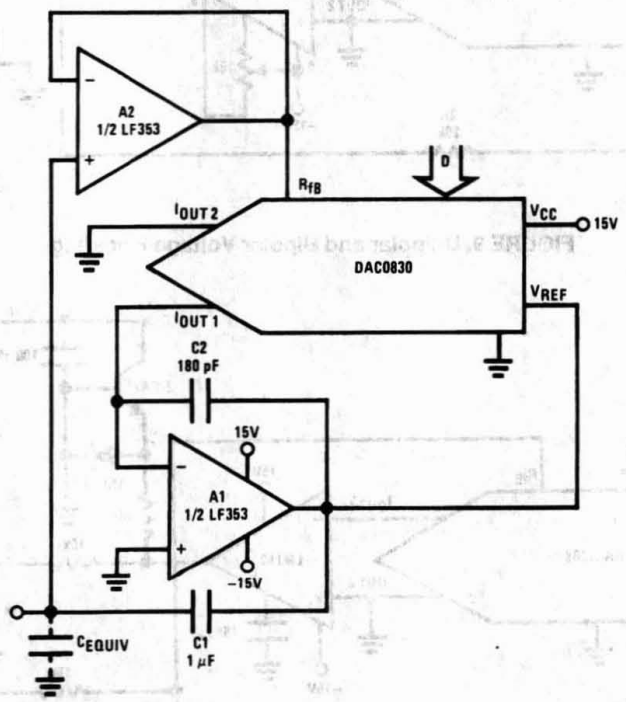
CAPACITANCE MULTIPLIER

The DAC controlled amplifier can be used in a capacitance multiplier circuit to give a processor control of a system's time or frequency domain response. The circuit in *Figure 8* uses the DAC to adjust the gain of a stage with a fixed capacitive feedback, creating a Miller equivalent input capacitance of the fixed capacitance times 1 + the amplifier's gain. The voltage across the equivalent input capacitance to ground is limited to the maximum output voltage of op amp A1, divided by 1 + $2^n/D$, where n is the DAC's bits of resolution.



$$V_{OUT} = \frac{-V_{IN}(1024)}{D}$$

FIGURE 7. DAC Controlled Amplifer



TL/H/5629–3

$$C_{EQUIV} = C1\left(1 + \frac{256}{D}\right)$$

FIGURE 8. Capacitance Multiplier

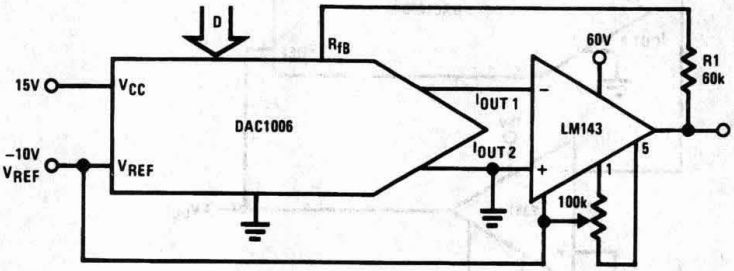
HIGH VOLTAGE OUTPUT

Many DAC applications involve the generation of high voltage levels to be used for deflection plate driving, high voltage motor speed, or position control. All of the MICRO-DAC can control as much as ±25V applied to the reference terminal, but guaranteed performance is specified at no more than ±10V. Since the output amplifier serves as a current-to-voltage converter, increasing the effective feedback resistance directly increases the amplifier's output voltage for a given DAC output current. Use of a high voltage op amp, the LM143 with 80V supply capability for example, can accommodate this increased gain and allow the use of reference voltage within the DAC's specified limits. *Figure 9* illustrates how higher voltage outputs can be obtained for both unipolar and bipolar requirements.

The output current of these circuits is limited to that of the LM143, typically 20 mA. If higher voltage and/or higher output current is needed, a discrete power stage can be used, as shown in *Figure 10*.

To insure accuracy with these high voltage circuits, concern for the power dissipation and temperature coefficients of the resistors used to increase the output voltage is necessary. The T-network configuration shown in *Figure 10* reduces the dependence of the output voltage to temperature changes by reducing the significance of the tracking requirements of the external resistors to the internal R_{fB} resistor. Using two resistors with similar temperature coefficients for R1 and R2, and making their ratio dominant in setting the overall gain provide the most stable results.

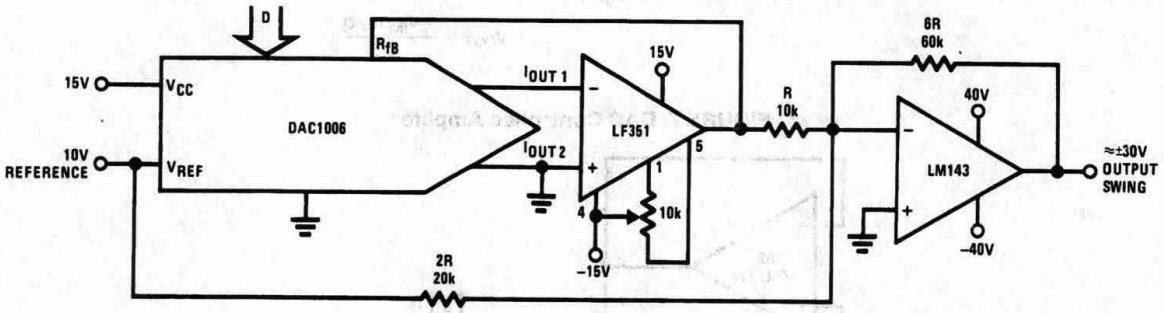
a) Unipolar Output



$$V_{OUT} = \frac{-V_R D}{1024}(R_{fB} + R1)$$

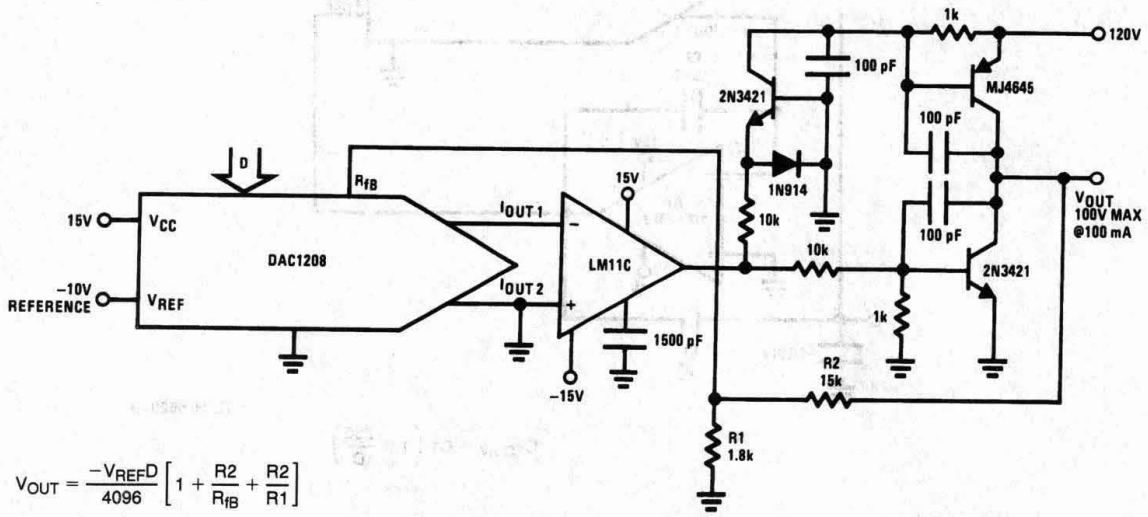
$$0 \le V_{OUT} \le 50V$$

b) Bipolar Output



$$V_{OUT} = \frac{(D - 512)\,3\,V_R}{512}$$

FIGURE 9. Unipolar and Bipolar Voltage Boosting



$$V_{OUT} = \frac{-V_{REF} D}{4096}\left[1 + \frac{R2}{R_{fB}} + \frac{R2}{R1}\right]$$

TL/H/5629–4

FIGURE 10. High Voltage Power DAC

HIGH CURRENT CONTROLLER

The MICRO-DAC can also be used to linearly control current flow useful in applications such as automatic test systems, stepper-motor torque compensation, and heater controls. *Figure 11* illustrates the use of a DAC1230 controlling a 0A to 1A current sink. The largest source of nonlinearity in this circuit is the stability of the current sensing resistance with changes in its power dissipation. To minimize this effect, the sensing resistance should be kept as low as possible. To maintain the output current range, the reference voltage to the DAC must be reduced. The flexible reference requirements of the MICRO-DAC permit the application of a lower reference with no degradation in linearity. A triple Darlington is used to minimize the base current term flowing through the sense resistor, but not into the collector terminal.

4 ma to 20 mA CURRENT LOOP CONTROLLER

The standard 4 mA−20 mA industrial process current loop controller is an application where automatic, microprocessor directed operation is often required, and is a natural application for D to A converters. The low power requirements of the CMOS MICRO-DAC allow the design of a controller that is powered directly from the loop it is controlling. *Figure 12* illustrates a 2-terminal floating 4 mA to 20 mA controller.

In this circuit, the output transistor will conduct whatever current is necessary to keep the voltage across R3 equal to the voltage across R2. This voltage, and therefore the total loop current, is directly proportional to the output current from the DAC. the net resistance of R1 is used to set the zero code loop current to 4 mA, and R2 is adjusted to provide the 16 mA output span with a full-scale DAC code.

The entire circuit "floats" by operating at whatever ground reference potential is required by the total loop resistance and loop current. To insure proper operation, the voltage differential between the input and output terminals must be kept in the range of 16V to 55V, and the digital inputs to the DAC must be electrically isolated from the ground potential of the controlling processor. This isolation can best be achieved with opto-isolators switching the digital inputs to the ground potential of the DAC for a logic low level.

In a non-microprocessor based system where the loop controlling information comes from thumbwheel switches, the digital input data for the DAC can be derived from BCD to binary CMOS logic circuitry, which is ground referenced to the ground potential of the DAC. The total supply current requirements of all circuits used must, of course, be less than 4 mA, and the value of R1 could be adjusted accordingly.

TARE COMPENSATION/AUTO-ZEROING

Probably the most popular application of D to A converters is in auto-zeroing or auto-referencing. In these systems the DAC is called upon to hold an output voltage used to offset the analog input range of an A to D converter. This is done to reserve the full input range of the A to D for analog voltages starting from reference potential to a full-scale value relative to that reference voltage. A common example of this is Tare Compensation in a weighing system where the weight of the scale platform, and possibly a container, is subtracted automatically from the total weight being measured. This, in effect, expands the range of weight that could be measured by preventing a premature full-scale reading, and allows an automatic indication of the actual unknown quantity.

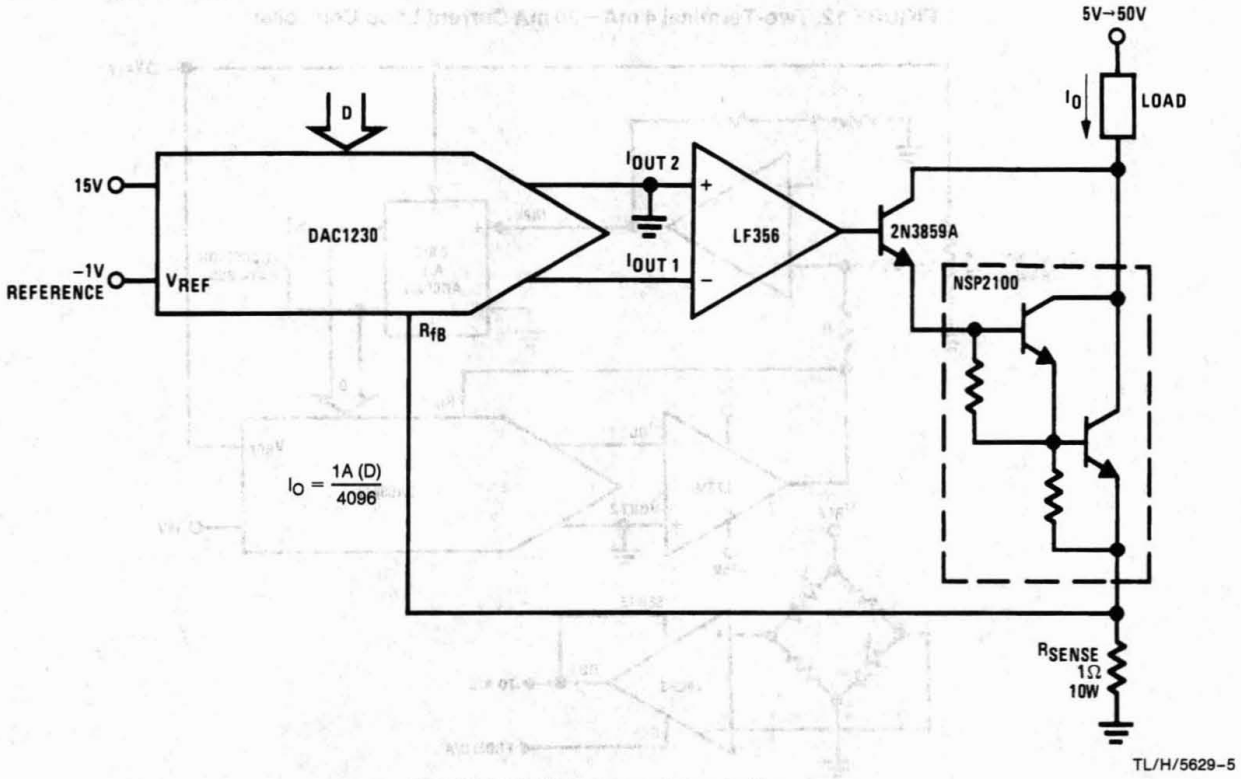
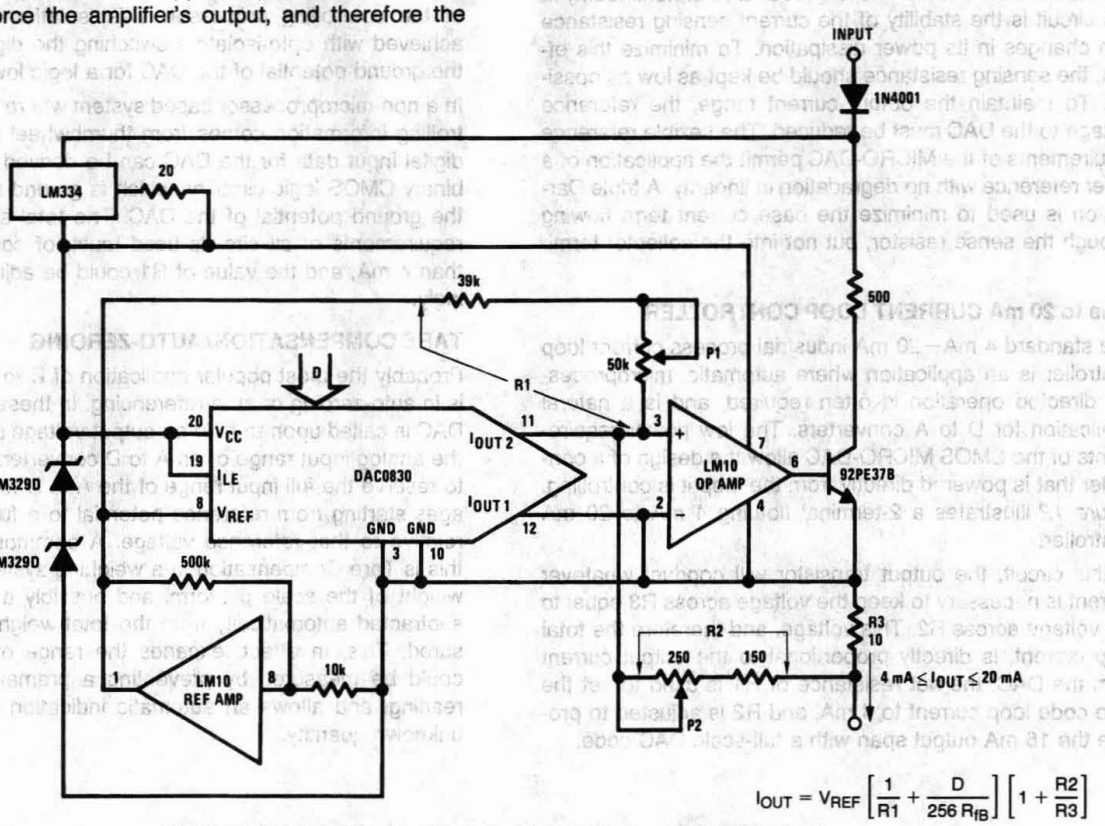


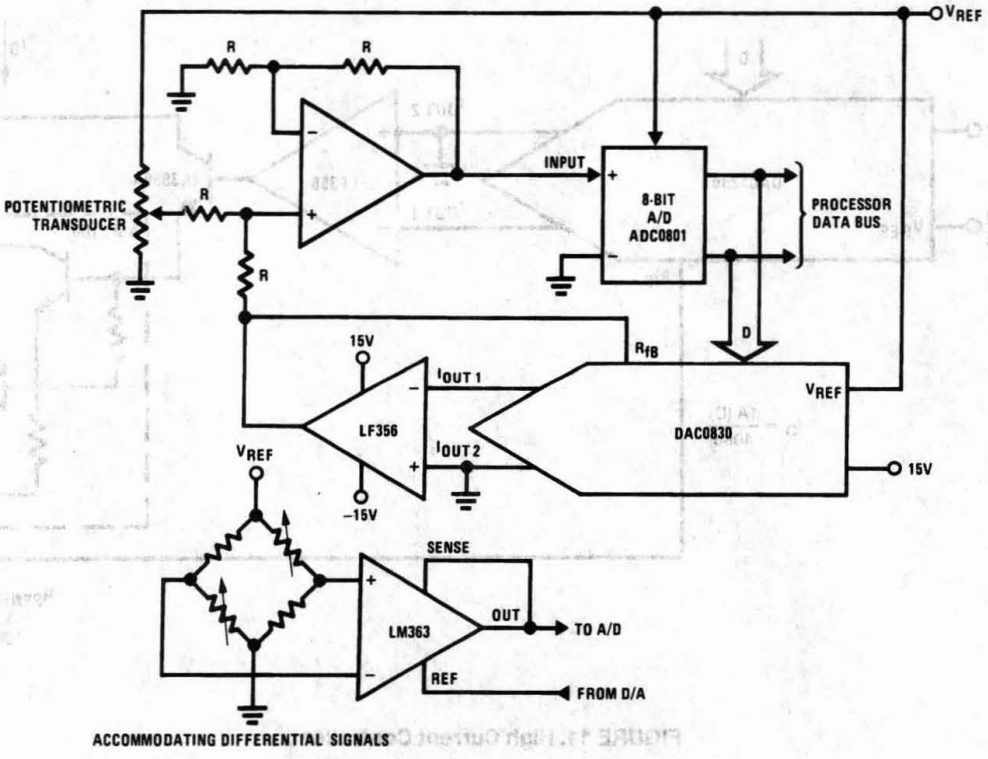
FIGURE 11. High Current Controller

Figure 13 illustrates this basic technique. In this system the DAC would initially be given a zero code and the system's input would be set to some reference quantity. A conversion of this input would be performed, then the corresponding code would be applied to the DAC. The output of the DAC will be equal to and of the opposite polarity as the input voltage to force the amplifier's output, and therefore the A/D's input, to zero. The DAC's output is held constant so that any subsequent A/D conversions will yield a value relative in magnitude to the initial reference quantity. To insure that the output code from the A to D generates the proper DAC output voltage, the two devices should be driven from the same reference voltage.



$$I_{OUT} = V_{REF}\left[\frac{1}{R1} + \frac{D}{256\,R_{fB}}\right]\left[1 + \frac{R2}{R3}\right]$$

FIGURE 12. Two-Terminal 4 mA – 20 mA Current Loop Controller



TL/H/5629–6

FIGURE 13. Basic Tare Compensation

For differential input signals, an instrumentation amplifier such as the LM363 can be used. The output reference pin of this amplifier can be driven directly by the DAC's output amplifier to offset the A to D input.

Auto-zeroing is the unique case of auto-referencing where the reference input is the zero or null condition. This technique essentially shorts out or electrically simulates a balance of the system's input device, and uses a DAC to correct for offset errors contributed by the signal conditioning amplification stage. Since amplifier errors are generally much lower in magnitude than the signal after being amplified, and can be of either polarity when applied to the A/D, a bipolar output configuration utilizing a CMOS DAC (*Figure 6*) driven from a reduced reference voltage can null the offset errors to within microvolts of zero. This is illustrated in *Figure 14* for an LM363 differential amplification stage.

The auto-zeroing routine performed by the processor is essentially a successive approximation routine which utilizes the A/D converter as a high resolution comparator, a feature unique to the ADC0801 A/D shown. When the routine is completed, the voltage at the reference pin of the instrumentation amplifier will be equal to and of the opposite polarity of the amplifier's offset voltage, multiplied by the gain. Details of the A/D's operation in this mode and an example of a microprocessor successive approximation routine can be found on the ADC0801 data sheet.

D TO A CONVERTER WITH A VERNIER ADJUSTMENT

In many systems it is required that an analog voltage be generated as a controlling function by a processor, when only an approximate value is known, with the exact value dependent on feedback from the controlled device. In this case, the processor could output an 8-bit "coarse" word to the 8 MSBs of a 12-bit DAC. Then the 4 LSBs could be incremented or decremented by an up/down counter to serve as a 16 LSB dither or vernier, which would stop when external sensing circuitry detected the actual desired value. The DAC1208 can be used in just such a system, as shown in *Figure 15*. The digital input circuitry of this device

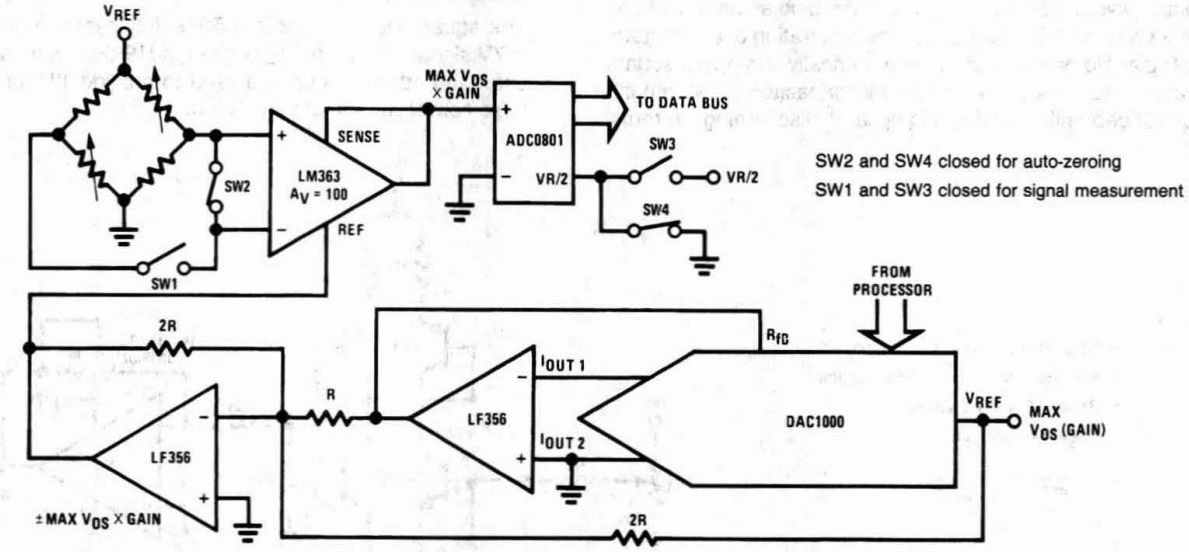
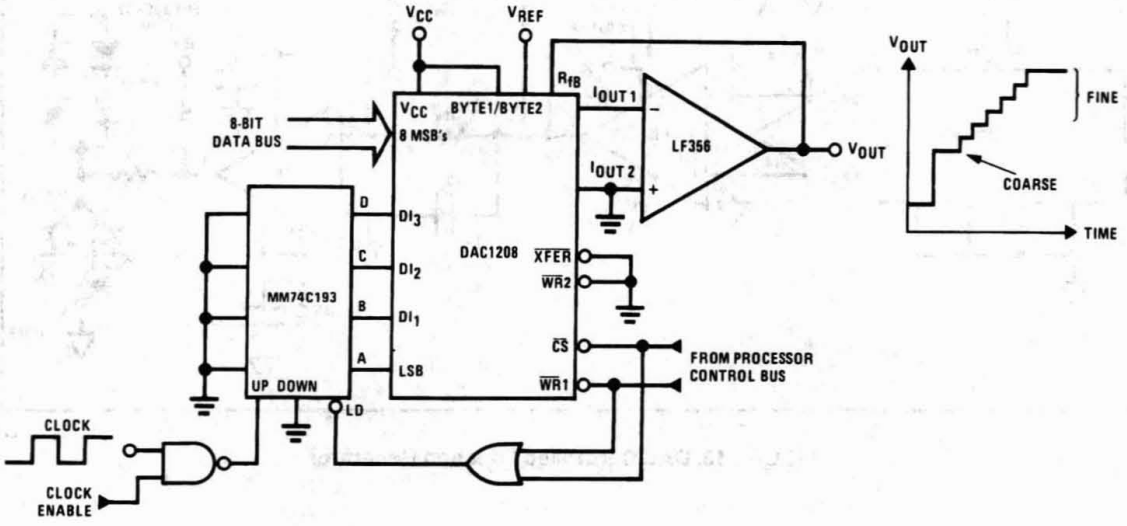


FIGURE 14. Auto-Zeroing



TL/H/5629–7

FIGURE 15. 8-Bit Coarse, 4-Bit Vernier DAC

provides all 12 input lines with separate registers for the 8 MSBs and the 4 LSBs. The register for the 4 LSBs can be configured to flow through so that the output will always reflect the state of the counter's output.

DAC CONTROLLED FUNCTION GENERATOR

CMOS DACs find wide use in the synthesis of periodic waveforms from digital information primarily for their precision and flexibility in controlling magnitude and timing parameters. If the signal generated is used as an excitation for a system, the data is readily available for a processor to know precisely where the input is to enable it to interpret the output response of the system. Typically, the data required to generate the amplitude information resides in the system ROM and the frequency is controlled by the rate at which the DAC is updated. Some of the more typical waveforms include sin, square, sawtooth ramps or staircases, and triangles.

Figure 16 shows the implementation of a MICRO-DAC providing frequency control of a sine, square and triangle function generator. The DAC is used as a digitally programmable input resistor for an integrator. The bipolar nature of the reference input is important to the generation of a symmetrical triangle wave and a symmetrically clamped square wave. This allows the integrating capacitor to be ground referenced with equal charging and discharging currents. Linearity of the output frequency versus the applied digital input code is as good as the DAC up to 30 kHz, where the propagation delay through the LM319 comparator starts adding non-linearity.

Integrating capacitor, C1, is selected for the maximum output frequency which occurs with a full-scale input code when the DAC provides its maximum output current. A problem in selecting this capacitor is that the R value of the internal R-2R ladder can vary over the range of 10 kΩ to 20 kΩ. This can be accommodated by adjusting the amount of positive feedback around the comparator to provide the desired maximum frequency for a given capacitor. This adjustment also alters the amplitude of the triangle wave, but this can be attenuated or amplified as required to achieve any desired amplitude.

The sine wave output is derived from the triangle wave by virtue of the non-linear conduction characteristics of the transistors used in the shaper circuit. The wave-shape adjustment is used to obtain minimum distortion of the sine wave output and should be adjusted after the triangle wave output is established.

The square wave output is a 50% duty cycle, symmetrical ±7V signal. Since only ½ of the LM319 dual comparator is used, the other side can be used to provide TTL or CMOS logic compatible output if needed.

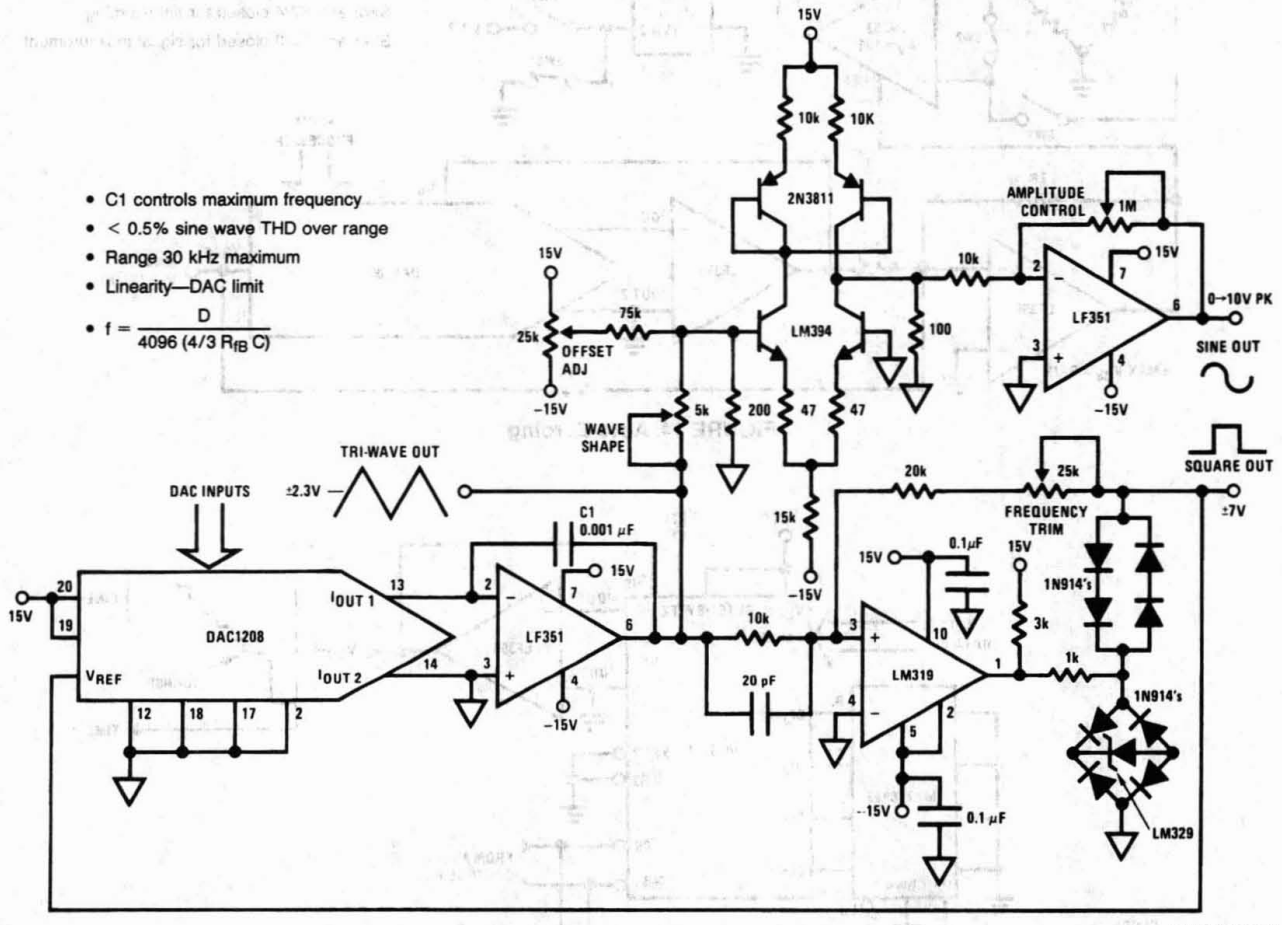


FIGURE 16. DAC Controlled Function Generator

For DAC controlled amplitude versatility, the basic unipolar configuration (*Figure 2*) can be used at any or all of the outputs.

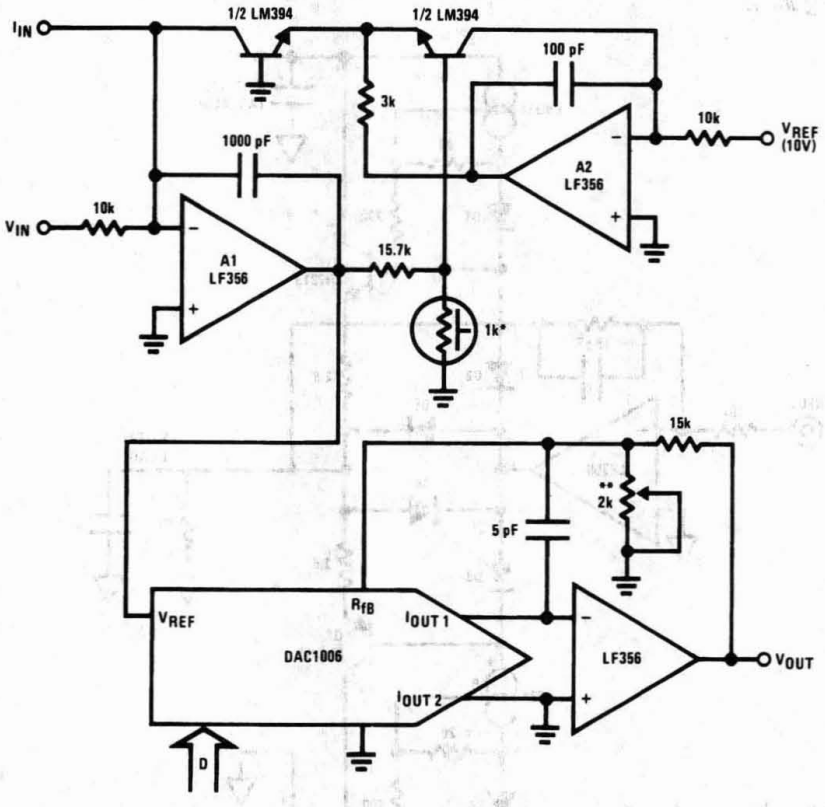
LOGARITHMIC AMPLIFIER WITH A PROGRAMMABLE SCALE FACTOR

Sensors that operate over a wide dynamic range, such as photomultiplier tubes, often require signal compression via logarithmic amplifiers. *Figure 17* shows a logging amplifier with a digitally programmable output scale factor from 10 mV/decade to 10V/decade over an input voltage range of 100 μV to 10V, or an input current range of 10 nA to 1 mA. The DAC1006 is used as the scaling element to attenuate or amplify the logarithmic output.

SUMMARY

The circuits described in this note illustrate only a very small percentage of possible MICRO-DAC applications. The key points to remember when considering the use of one of these devices are summarized below.

1. The reference voltage can be a bipolar AC or DC signal within the range of 25V with specified linearity guaranteed at $\pm$10V and $\pm$1V.
2. Low power consumption CMOS circuitry (20 mW typ).
3. Direct microprocessor interface with the necessary controlling logic designed in. All parts are 8-bit bus compatible.
4. TTL compatible digital input thresholds independent of the DAC's V_{CC} supply.
5. Linearity is guaranteed over temperature following a simple zero and full-scale adjustment procedure.
6. The current outputs, $I_{OUT\ 1}$ and $I_{OUT\ 2}$, want to be at ground potential.
7. $I_{OUT\ 1}$ should always be used in conjunction with the internally provided feedback resistor, as this resistor matches and tracks with temperature the resistors used in the R-2R ladder network.
8. The internal R value can vary over a 10 kΩ to 20 kΩ range.
9. The 12-bit MICRO-DAC are not recommended for use in the voltage switching mode.



TL/H/5629–9

*Tel Labs Q81 (+0.3%/°C)

**Adjust for 10V/dec output sensitivity at full-scale input code

$$V_{OUT} = \frac{10D}{1024} \log \frac{V_{IN}}{V_{REF}}$$

FIGURE 17. Logarithmic Amplifier with Digitally Programmable Scale Factor

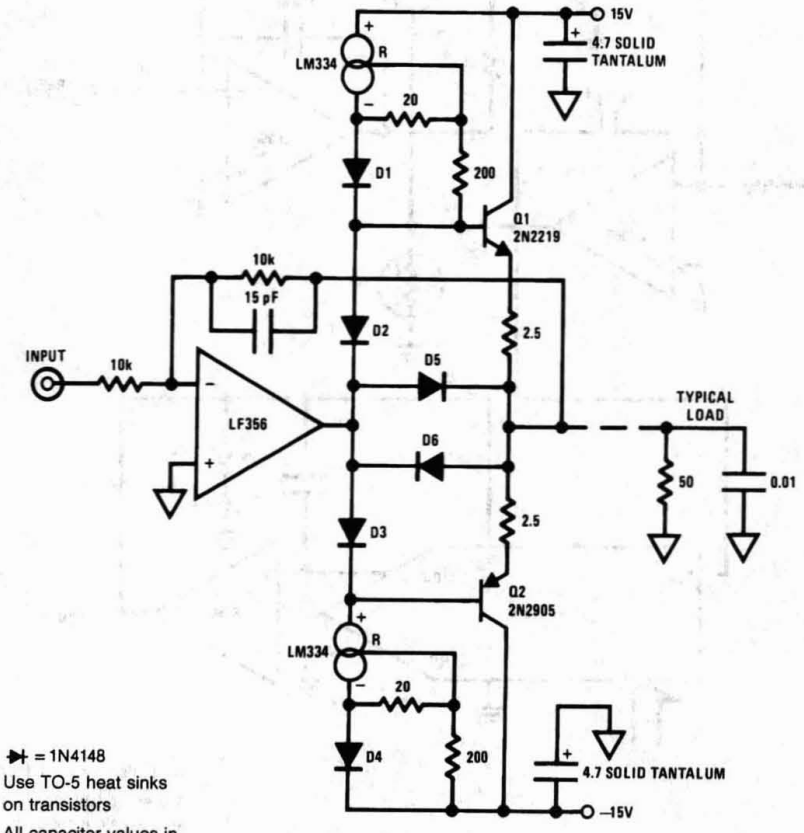
Op Amp Booster Designs

National Semiconductor
Application Note 272

Although modern integrated circuit operational amplifiers ease linear circuit design, IC processing limits amplifier output power. Many applications, however, require substantially greater output voltage swing or current (or both) than IC amplifiers can deliver. In these situations an output "booster," or post amplifier, is required to achieve the needed voltage or current gain. Normally, this stage is placed within the feedback loop of the operational amplifier so that the low drift and stable gain characteristics of the amplifier are retained. Because the booster is a gain stage with its own inherent AC characteristics, the issues of phase shift, oscillation, and frequency response cannot be ignored if the booster and amplifier are to work well together. The design of booster stages which achieve power gain while maintaining good dynamic performance is a difficult challenge. The circuitry for boosters will change with the application's requirements, which can be very diverse. A typical current gain stage is shown in *Figure 1.*

200 mA CURRENT BOOSTER

The circuit of *Figure 1* boosts the LF356 unity gain inverter amplifier's output current to a ±200 mA level while maintaining a full ±12V output swing. The LM334 current sources are used to bias complementary emitter-followers. The 200Ω resistors and D1-D4 diodes associated with the LM334s provide temperature compensation for the current sources, while the 20Ω resistor sets the current value at 3.5 mA. Q1 provides drive for positive LF356 output swings, while Q2 sinks current for negative amplifier outputs. Crossover distortion is avoided by the D2-D3 diodes which compensate the V_{BE}s of Q1 and Q2. For best results, D2 and D3 would be thermally coupled to the TO-5 type heat sinks used for Q1 and Q2. Amplifier feedback is taken from the booster output and returned to the LF356 summing junction. D5 and D6 achieve short circuit protection for the output by shunting drive from Q1 or Q2 when output current exceeds

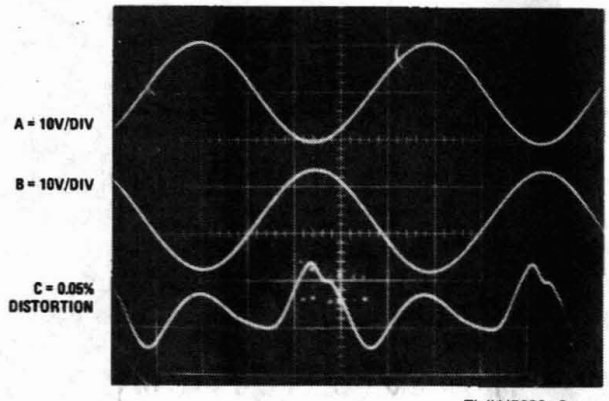


= 1N4148
Use TO-5 heat sinks on transistors
All capacitor values in μF unless otherwise noted

FIGURE 1

TL/H/5630–1

about 275 mA. This value is derived from the output 2.5Ω resistors value divided by the 0.7V drop across the diodes. The 15 pF-10k feedback values provide a roll-off above 2 MHz. *Figure 2* shows the circuit at work driving a 100 kHz 20 Vp-p sine wave into a 50Ω load paralleled by 10,000 pF/ Trace A is the input, while Trace B is the output. Despite the heavy load, response is clean below and quick with overall circuit distortion 0.05% (Trace C).

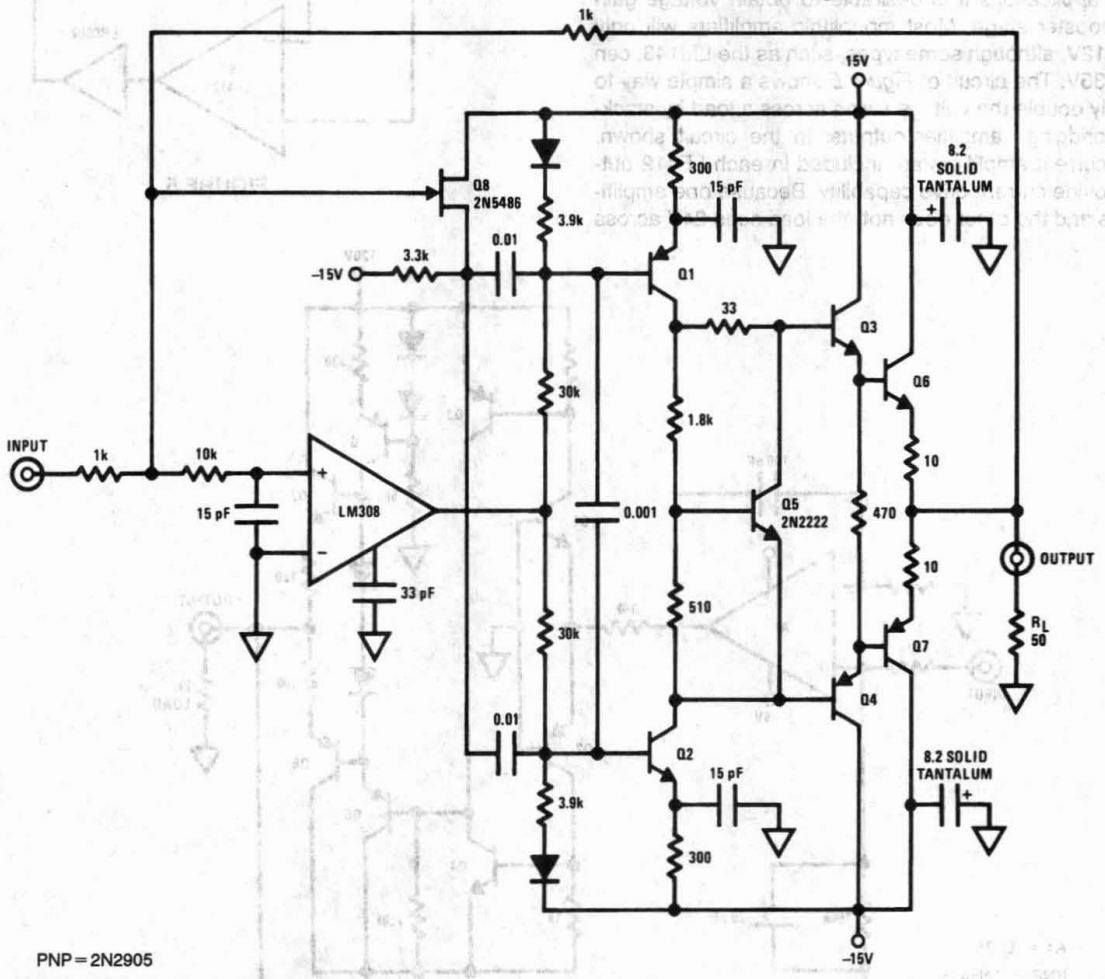


TL/H/5630–2

FIGURE 2

ULTRA HIGH SPEED FED-FORWARD CURRENT BOOSTER

The schematic of *Figure 3* features the same output specifications as the previous current booster, but provides much greater speed. The speed of the booster in *Figure 1* is limited by the response of the op amp which drives it. Because that booster resides in the op amp's feedback loop, it cannot go any faster than the op amp, even though it has inherently greater bandwidth. In *Figure 3* we employ a feed-forward network which allows AC signals to bypass the LM308 op amp and directly drive a very high bandwidth current boost stage. At DC and low frequencies the LM308 provides the signal path to the booster. In this fashion, a very high speed, high current output is achieved without sacrificing the DC stability of the op amp. The output stage is made up of the Q1 and Q2 current sources which bias complementary emitter-followers, Q3-Q6 and Q4-Q7. Because the stage inverts, feedback is returned to the non-inverting input of the LM308. The actual summing junction for the circuit is the meeting point of the 1k resistors and the 10k unit at the LM308. The 10k-15 pF combination prevents the LM308 from seeing high frequency inputs. Instead, these inputs are source-followed by the Q8 FET and fed directly to the output stage via the two 0.01 μF capacitors. The LM308, therefore, is used to maintain loop stability only at DC and low frequencies. Although this arrangement is substantially more complex than *Figure 1,* the result is a breathtaking

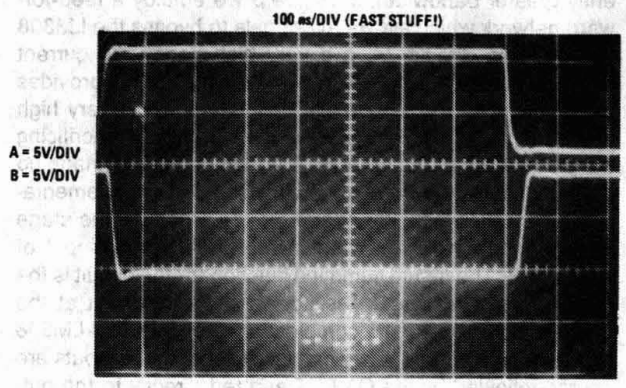


PNP = 2N2905
NPN = 2N2219 unless noted
TO-5 heat sinks for Q6-Q7

TL/H/5630–3

FIGURE 3

increase in speed. This boosted amplifier features a slew rate of 750V per microsecond, a full power bandwidth over 6 MHz and a 3 dB point beyond 11 MHz while retaining a ±12V, 200 mA output. *Figure 4* shows the amplifier-booster at work. Trace A is the input, while Trace B is the output. The booster drives a 10V pulse into 50Ω, with rise and fall times inside 15 ns and clean settling characteristics.



TL/H/5630–4

FIGURE 4

VOLTAGE-CURRENT BOOSTER

In many applications it is desirable to obtain voltage gain from a booster stage. Most monolithic amplifiers will only swing ±12V, although some types, such as the LM143, can swing ±35V. The circuit of *Figure 5* shows a simple way to effectively double the voltage swing across a load by stacking or "bridging" amplifier outputs. In the circuit shown, LF0002 current amplifiers are included in each LF412 output to provide current drive capability. Because one amplifier inverts and the other does not, the load sees 24V across it for ±12V swings from each amplifier. With the LH0002 current buffers, 24V can be placed across a 250Ω load. Although this circuit is simple and no high voltage supplies are needed, it requires that the load float with respect to ground.

±120V SWING BOOSTER

In *Figure 6* the load does not have to float from ground to be driven at high voltage. This booster will drive a 2000Ω load to ±100V with good speed. In this circuit, voltage gain is

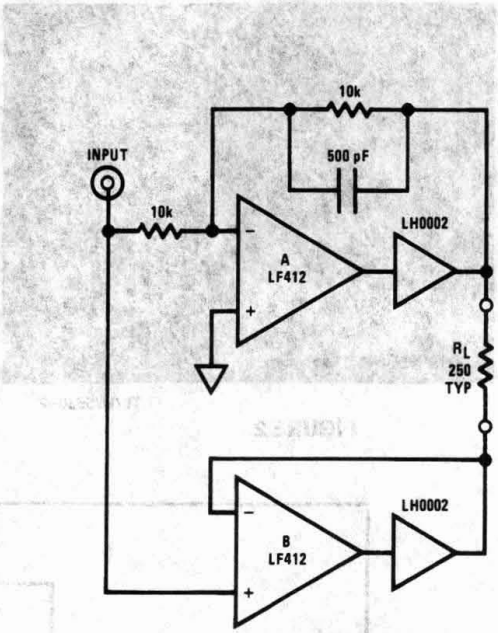
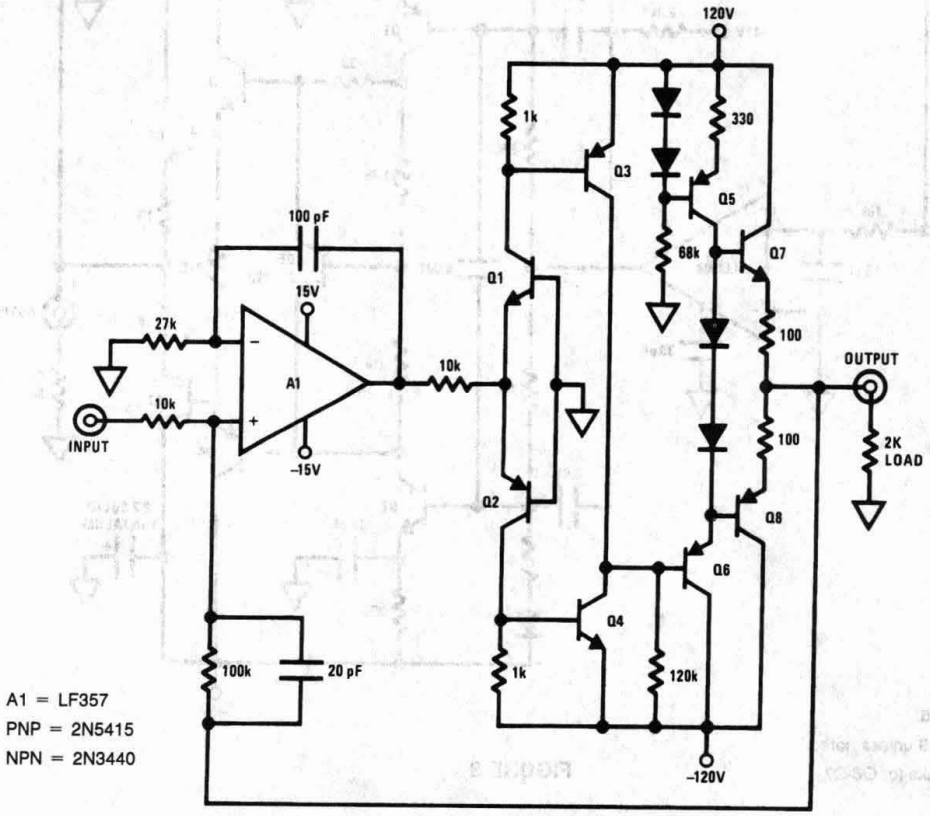


FIGURE 5



A1 = LF357
PNP = 2N5415
NPN = 2N3440

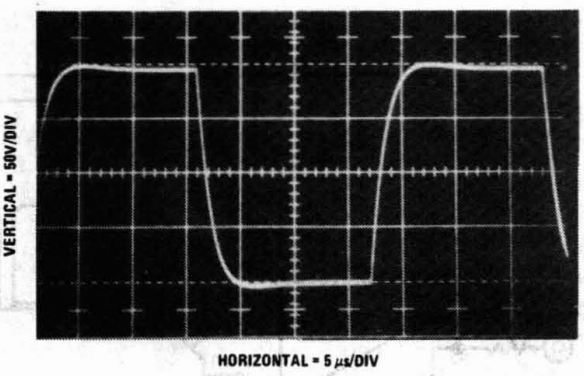
TL/H/5630–5

FIGURE 6

obtained from the complementary common base stage, Q1-Q2. Q3 and Q4 provide additional gain to the Q7-Q8 complementary emitter-follower output stage. Q5 and Q6 provide bias, and crossover distortion is minimized by the diodes in Q5's collector line. For ±10V input signals, A1 must operate at a minimum gain of 10 to achieve a ±100V swing at the output. In this case, 10k-100k feedback values are used for a gain of ten, and the 20 pF capacitor provides loop roll-off. Because the booster contains an inverting stage (Q3-Q4), overall feedback is returned to A1's positive input. Local AC feedback at A1's negative input provides circuit dynamic stability. With its ±50 mA output, this booster yields currents as well as voltage gain. In many applications, such as CRT deflection plate driving, this current capability is not required. If this is the case, Q5 through Q8 and their associated components can be eliminated and the output and feedback taken directly from the Q3-Q4 collector line. Under these conditions, resistive output loading should not exceed 1 MΩ or significant crossover distortion will appear. Since deflection plates are a pure capacitive load, this is usually not a problem. *Figure 7* shows the boosted amplifier driving a ±100V square wave into a 2000Ω load at 30 kHz.

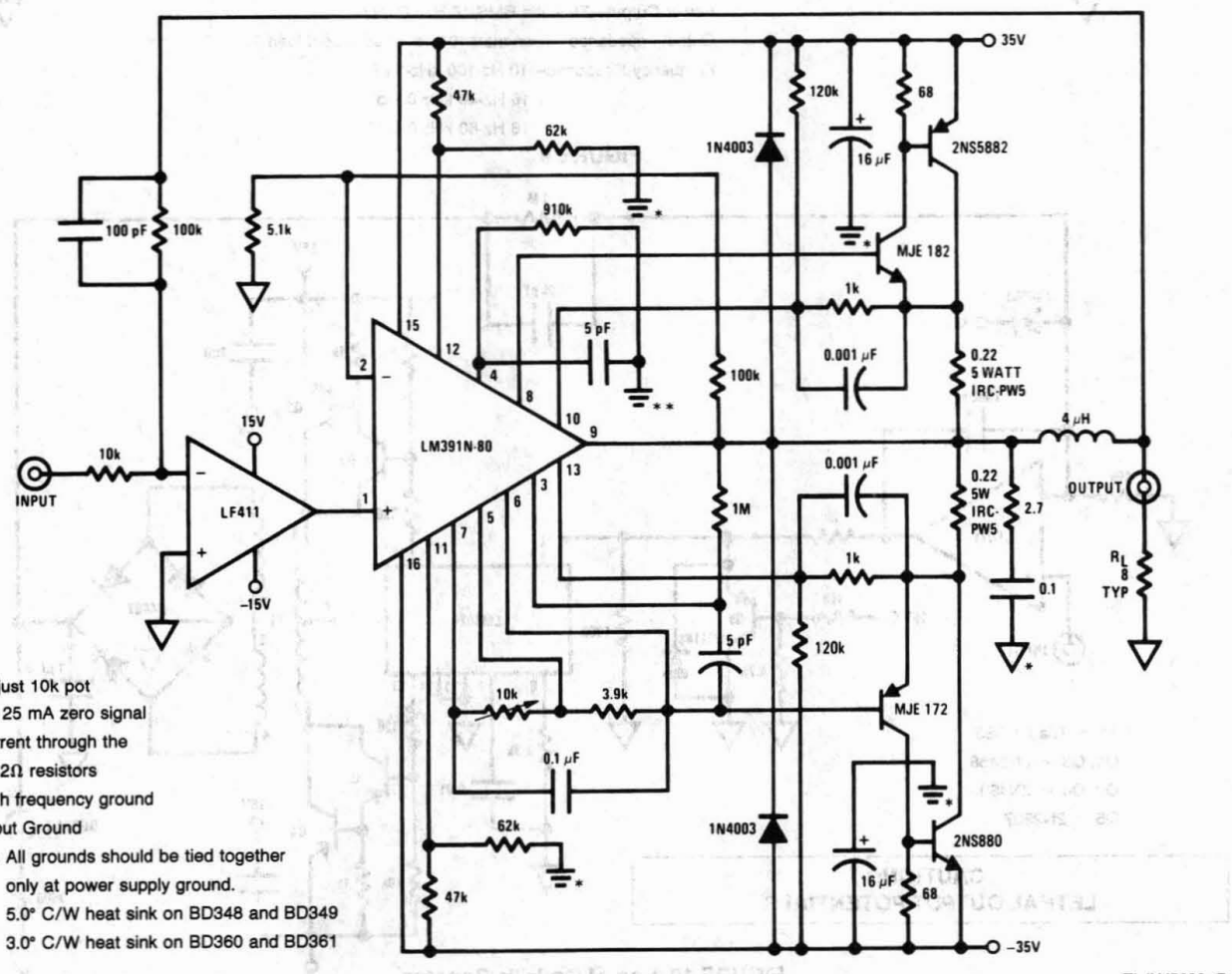
HIGH CURRENT BOOSTER

High current loads are well served by the booster circuit of *Figure 8*. While this circuit does provide voltage gain, its ability to drive 3A of current into an 8Ω load at 25V peak makes it useful as a current booster. In this circuit, the LM391-80 driver chip and its associated power transistors are placed inside the LF411's feedback loop. The 5 pF capacitor at pin 3 of the LM391-80 sets the booster bandwidth well past 250 kHz. The 100k-10k feedback resistors set a gain of ten, and the 100 pF feedback capacitor rolls off the loop gain at 100 kHz to insure stability for the amplifier-booster combination. The 2.7Ω-0.1 μF damper network and the 4 μH inductor prevent oscillations. The zero signal current of the output stage is set with the 10k potentiometer (pins 6-7 at the LM391) while a DVM is monitored for 10 mV across the 0.22Ω output resistors.



TL/H/5630–6

FIGURE 7



Adjust 10k pot for 25 mA zero signal current through the 0.22Ω resistors

* High frequency ground

** Input Ground

Note: All grounds should be tied together only at power supply ground.

5.0° C/W heat sink on BD348 and BD349

3.0° C/W heat sink on BD360 and BD361

TL/H/5630–7

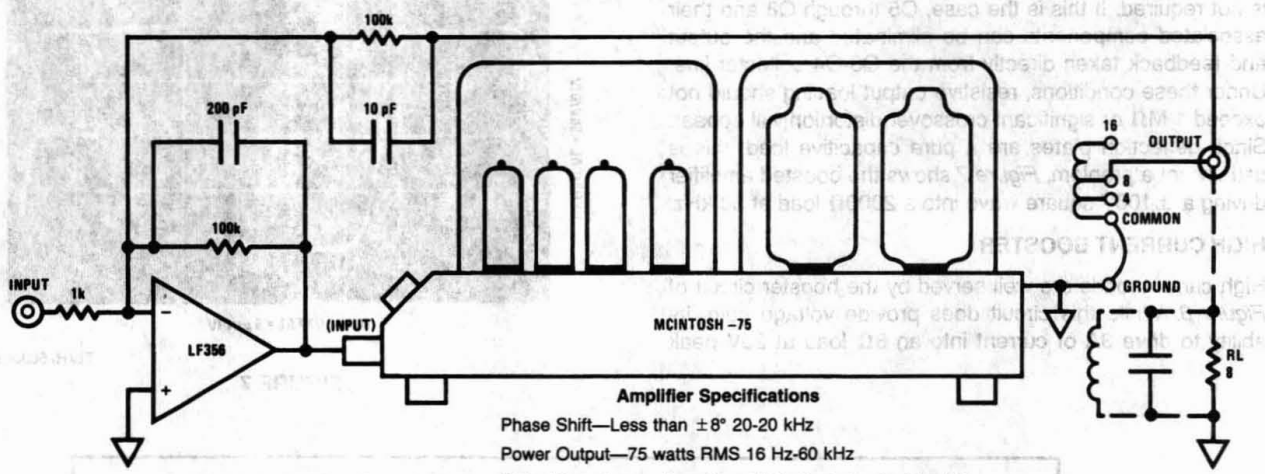
FIGURE 8

INDESTRUCTIBLE, FLOATING OUTPUT BOOSTER

Figure 9 shows how a high quality audio amplifier can be used as a current-voltage booster for AC signals. The audio amplifier, specified as the booster, is a venerable favorite in research labs, due to its transformer isolated output and clean response. The LF356 op amp's loop is closed locally at a DC gain of 100, and rolled off at 50 kHz by the 200 pF capacitor. The audio amplfier booster's output is fed back via the 100k resistor for an overall AC gain of 100 with respect to the booster amplifier output. The arrangement is ideal for laboratory use because the vacuum tube driven transformer isolated output is extremely forgiving and almost indestructible. AC variable frequency power supplies, shaker table drives, motors and gyro drives, as well as other difficult inductive and active loads, can be powered by this booster. Power output is 75W into 4Ω-16Ω, although loads of 1Ω can be driven at reduced power output.

1000V-300 mA BOOSTER

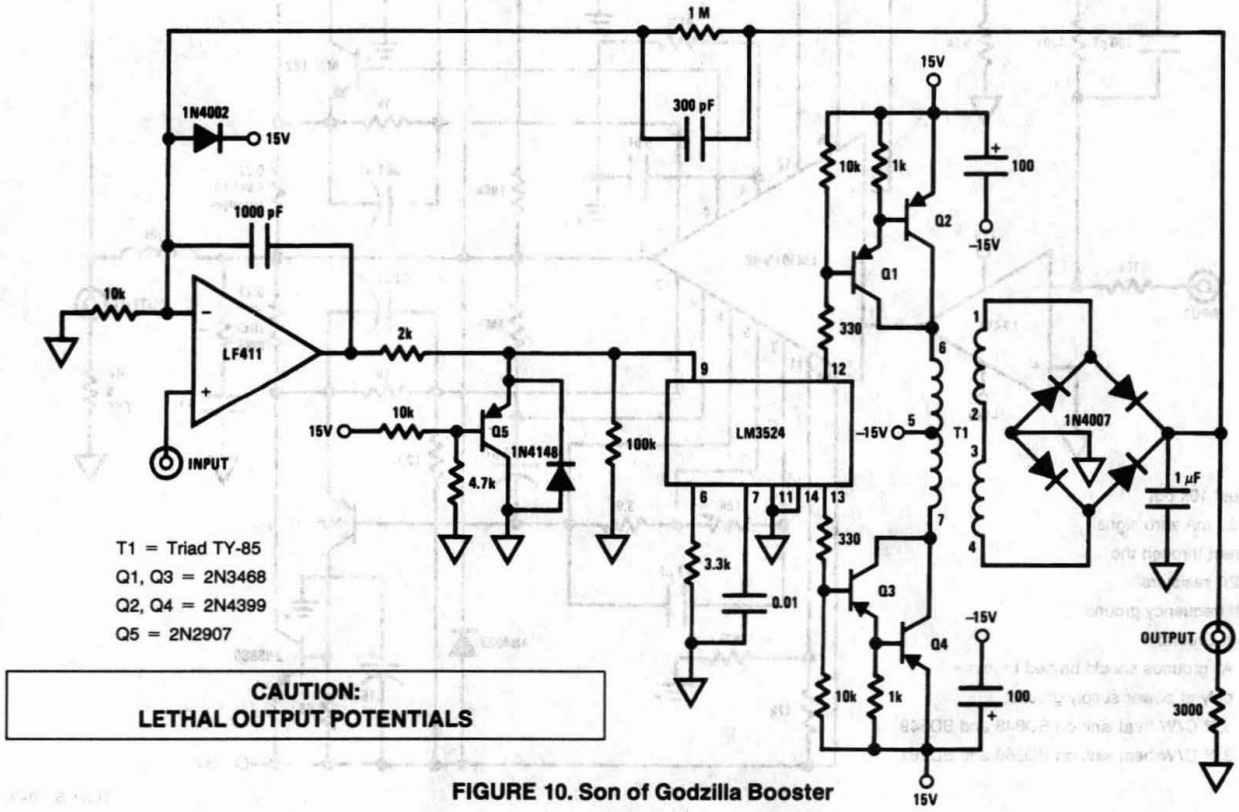
Figure 10 diagrams a very high voltage, high current booster which will allow an op amp to control up to 300W for positive outputs up to a staggering 1000V. This performance is achieved without sacrificing efficiency because this booster, in contrast to all the others shown, operates in a switching



Amplifier Specifications

Phase Shift—Less than ±8° 20-20 kHz
Power Output—75 watts RMS 16 Hz-60 kHz
Output Impedance—Less than 10% of rated output load Z.
Frequency Response—10 Hz-100 kHz-1 dB.
16 Hz-40 kHz-0.1 dB.
16 Hz-60 kHz-0.5 dB.

FIGURE 9



T1 = Triad TY-85
Q1, Q3 = 2N3468
Q2, Q4 = 2N4399
Q5 = 2N2907

CAUTION:
LETHAL OUTPUT POTENTIALS

FIGURE 10. Son of Godzilla Booster

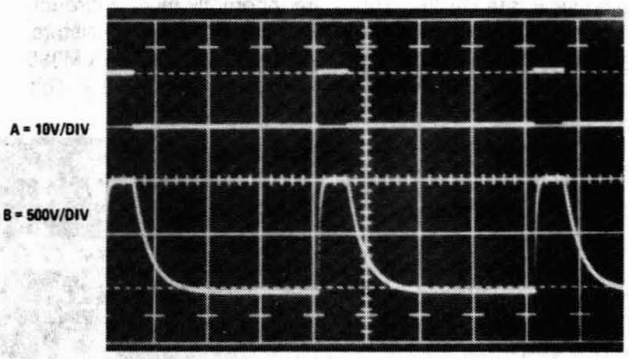
TL/H/5630–8

mode. In addition, this booster runs off ±15V supplies and has the highly desirable property of *not* requiring a high voltage power supply to achieve its high potential outputs. The high voltage required for the output is directly generated by a switching DC-DC converter which forms an integral part of the booster. The LM3524 switching regulator chip is used to pulse width modulate the transistors which provide switched 20 kHz drive to the TY-85 step-up transformer. The transformer's rectified and filtered output is fed back to the LF411, which controls the input to the LM3524 switching regulator. In this manner, the high voltage booster, although operating switched mode, is controlled by the op amp's feedback action in a similar fashion to all the other designs. Q5 and the diode act as clamps to prevent the LF411's output swing from damaging the LM3524's 4V input on start-up. The diode at the LF411 swing junction prevents high voltage transients coupled through the feedback capacitor from destroying the amplifier. The 1 MΩ-10k feedback resistors set the gain of the amplifier at 100 so that a 10V input will give a 1000V output. Although the 20 kHz torroid switching rate places an upper limit on how fast information can be transmitted around the loop, the 1 μF filter capacitor at the circuit output restricts the bandwidth. For the design shown, full power sine wave output frequency is 55H. *Figure 11* shows the response of the boosted LF411 when a 10V pulse (Trace A) is applied to the circuit input. The output (Trace B) goes to 1000V in about 1 ms, while fall time is about 10 ms because of capacitor discharge time. During the output pulse's rise time the booster is slew rate limited and the switching action of the torroid is just visible in the leading edge of the pulse.

The reader is advised that the construction, testing and use of this circuit must be approached with the greatest care. The output potentials produced are many times above the level which will kill. Repeating, the output of this circuit is lethal.

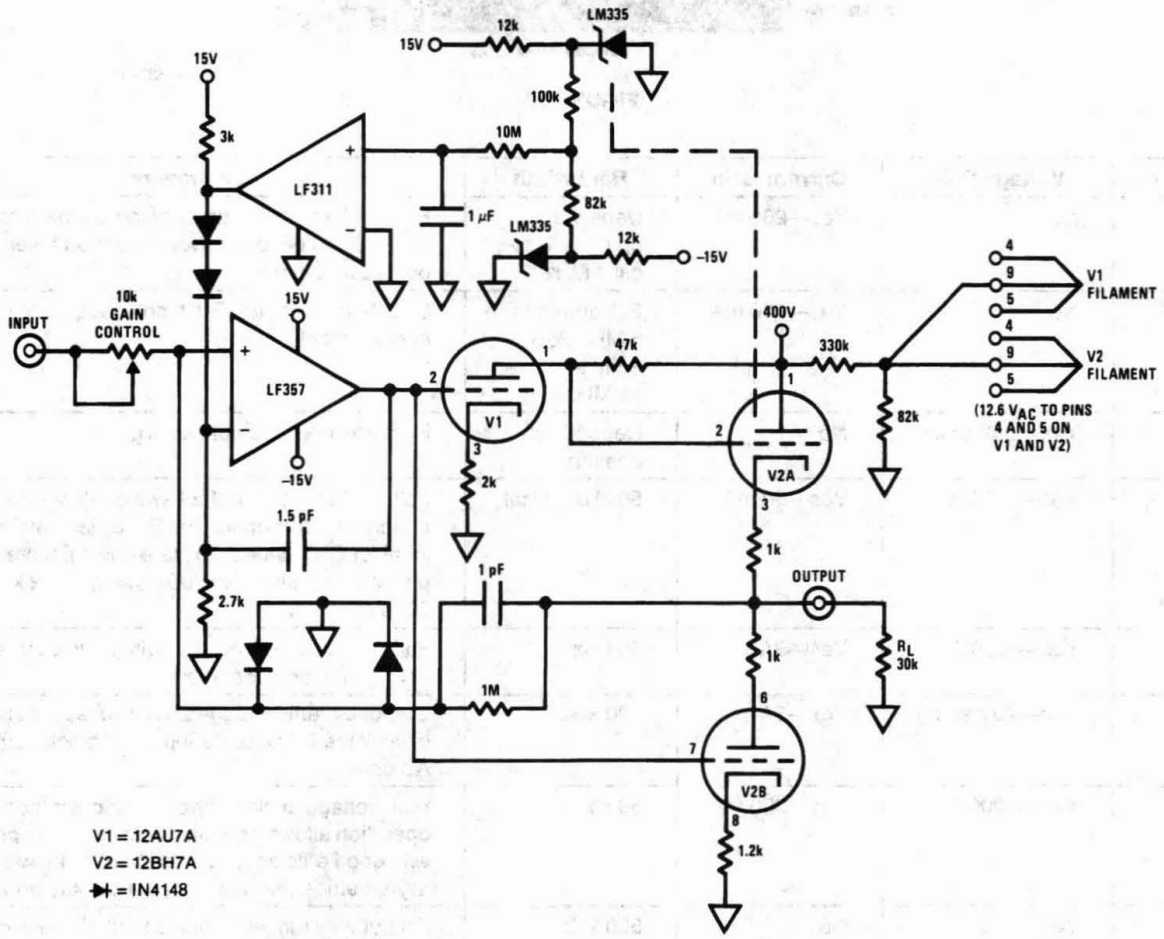
300V OUTPUT BOOSTER

The circuit of *Figure 12* is another high voltage booster, but will only provide 10 mA of output current. This positive-output-only circuit will drive 350V into a 30k load, and is almost



TL/H/5630–9

FIGURE 11

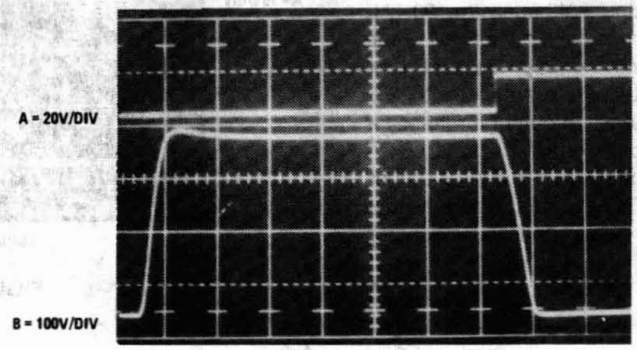


TL/H/5630–10

FIGURE 12

immune to load shorts and reverse voltages. A solid state output requires substantial protection against these conditions. Although the circuit shown has a 350V limit, tubes (remember them?) with higher plate voltage ratings can extend the output capacity to several kilovolts. In this circuit, our thermionic friends are arranged in a common cathode (V2B) loaded-cathode-follower (V2A) output, driven from a common cathode gain stage (V1). The booster output is fed back to the LF357 via the 1 MΩ resistor. Local feedback is used to stabilize the LF357, while the pF-1 MΩ pair rolls off the loop at 1 MHz. Because the V1 stage inverts, the feedback summing junction is placed at the LF357 positive input. The parallel diodes at the summing junction prevent high voltage from destroying the amplifier during circuit start-up and slew rate limiting. Tubes are inherently much more tolerant of load shorts and reverse voltages than transistors, and are much easier to protect. In this circuit, an LM335 temperature sensor is in contact with V2. This sensor's output is compared with another LM335 which senses ambient temperature. Under normal operating conditions, V2 operates about 45°C above ambient and the "+" input of the LF311 is about −100 mV, causing its output to be low. When a load fault occurs, V2's plate dissipation increases, causing its associated LM335's output to rise with respect to ambient temperature. This forces the LF311's output high, which makes the LF357 output go low, shutting down the output stage. Adequate hysteresis is provided by the thermal time constant of V2 and the 10 MΩ-1 μF delay in the LF311 input line. *Figure 13* shows the response of this amplifier booster at a gain of about 25. With a 15V input pulse (Trace A), the output (Trace B) goes to 350V in 1 μs, and settles within 5 μs. The falling edge slews equally fast and settling occurs within 4 μs.

Figure 14 is a table which summarizes the information in this article and will help you to pick the right booster for your particular application.



TL/H/5630–11

FIGURE 13

Figure	Voltage Gain	Current Gain	Bandwidth	Comments
1	No	Yes—200 mA	Depends on op amp. Typical 1 MHz	Full "+" and "−" output swing. Stable into 50Ω-10,000 pF load. Inverting or non-inverting operation. Simple.
3	No	Yes—200 mA	Full output to 5 MHz-3dB. Point at 11 MHz.	Ultra fast. 750V/μs. Full bipolar output. Inverting operation only.
5	Yes—24V swing	No	Depends on op amp.	Requires that load float from ground.
6	Yes—±100V	Yes—50 mA	50 kHz typical.	Full "+" and "−" output swing. Allows inverting or non-inverting operation. Simplified version ideal for CRT deflection plate driving. More complex version drives full 200V swing into 2 kΩ and 1000 pF.
8	Yes—±30V	Yes—3A	50 kHz	Full "+" and "−" output swing. Allows inverting or non-inverting operation.
9	Yes—70V swing	Yes—3A	100 kHz	Output extremely rugged. Well suited for driving difficult loads in lab. Set-ups. Full bipolar output. AC only.
10	Yes—1000V	Yes—300 mA	50 Hz	High voltage at high current. Switched mode operation allows operation from ±15V supplies with good efficiency. Limited bandwidth with asymmetrical slewing. Positive outputs only.
12	Yes—350V	No	500 kHz	Output very rugged. Good speed. Positive outputs only.

FIGURE 14

CMOS A/D Converter Interfaces Easily with Many Microprocessors

National Semiconductor
Application Note 274

With a span accommodation down to 180 mV, this 8-bit unit can also replace a 12-bit analog-to-digital device in some applications.

To help meet the rising demand for easier interfacing between analog-to-digital converters and microprocessors, the complementary MOS, 8-bit ADC0801-05 has been designed to accommodate almost all of today's popular microprocessors. It requires only a single 5V supply and is low power to boot.

Housed in a 20-pin dual-in-line package, the successive approximation device includes a Schmitt trigger circuit that allows it to be driven from a system clock, as well as an external RC network. At a clock frequency of 640 kHz, conversion time is 100 μs. What's more, its guaranteed linearity error of $\pm 1/4$ least significant bit (typically $\pm 1/16$ LSB) can encode an analog signal span as small as 180 mV—a performance that allows it to replace 9, 10, and even 12-bit converters in many applications.

Constantly decreasing converter prices raise the comparative cost of the interface electronics and increase the demand for simplicity of interfacing. The growing emphasis on simpler systems for higher levels of reliability has also pushed this demand, as has a trend toward lower levels of power dissipation. And with the success of the 5V power supply standard of logic circuits, linear circuits have been pressed for 5V operation. Supporting the ADC0801-05 A/D converter are such special operational amplifiers as the LM358 dual and the LM324 and LM3900 quad op amps that run off 5V supplies; also useful are voltage comparators such as the LM393 dual and LM339 quad devices. Perhaps the most versatile of such 5V linear devices is the LM392, comprising an op amp and a comparator.

MORE COMPLICATIONS

Complicating the interfacing are the ever higher levels of resolution in monolithic converters, with 8 and 10-bit types readily available and 12-bit devices ready to emerge soon. Yet, despite their greater resolution, 10 and 12-bit monolithic A/D converters are not only more expensive than 8-bit designs, but also require more careful attention to system noise problems and management of grounding.

For simple interfacing, an A/D converter must operate directly with the signals available on a microprocessor control bus. The converter is generally given an address that can be mapped into memory or input/output space, depending on the type of microprocessor employed. On 6800 microprocessors and their derivatives, no special input/output addressing or strobes are available, so the converter must appear as a memory location to these processors. Z80® microprocessors, on the other hand, not only provide special I/O interfacing, but also automatically insert a wait state during I/O selection to increase the width of the read and write strobe signals. This eases interface requirements considerably, since slower I/O devices can operate with much faster microprocessor units. The automatic wait state for I/O devices will loom larger in importance as the next generation of higher speed microprocessors evolves.

COMPATIBILITY CRITERIA DIFFER

Microprocessor compatibility has a wide range of meanings—at least according to the various converter data sheets. True compatibility, however, involves meeting electrical specifications like proper logic voltage levels with adequate loading capability. For example, true TTL compatibility means the ability to maintain a 0.4V low potential (or less) at the A/D converter logic outputs while sinking 1.6 mA of current. And the high state must be maintained at a minimum of 2.4V while supplying at least 360 μA.

Furthermore, all interface protocols must be met. This not only means operating with the proper signals, but also meeting all necessary timing requirements, so the converter must have valid data on the microprocessor bus within the access time of the memory system with which it happens to be working.

The protocols for interfacing are not at all standardized. Some A/D converters make use of the standard chip select signal ($\overline{CS}$) to start a conversion. But decoding voltage glitches can cause an A/D converter to begin conversion when it is not desirable. Both the standard $\overline{CS}$ signal and a write strobe signal ($\overline{WR}$) must therefore be used, so that the former signal qualifies the latter and prevents unwanted conversions due to address decoding glitches. Care must also be taken when using some A/D converters that are designed to act as bus controllers; problems can arise when the central processor is not in control of the bus.

DIFFERENT STANDARDS

The 8080 and 6800 microprocessors (and their derivatives) use different control bus standards. Microprocessors based on the 8080, for example, make use of read and write strobe signals to specify the operation (read or write) requested. Working with these microprocessors, A/D converters start the conversion cycle upon the microprocessor's issuance of a chip select signal (decoded from the address bus) and a write strobe signal. At the end of conversion (EOC), the converter issues an EOC signal. When dealing with older A/D converters where the EOC signal is typically low during the conversion process and high at the end of it, microprocessors have difficulty because the EOC signal is not available on the data bus. Furthermore, the EOC signal does not reset when the converter is serviced by the central processing unit (that is, when data has been read).

Complications can also occur when microprocessors interface with older A/D devices during read operations. For proper interfacing, such converters must have valid data on the bus within the memory access time.

Interfacing requirements differ for 6800-type microprocessors, like the 6502 and 68000, which use read/write (R/$\overline{W}$) control lines instead of read and write strobe signals and obtain timing information from the system clock signal. In addition, they include a valid memory address signal to qualify the address that is placed on the bus. Such features make interfacing for these microprocessors different from that for earlier 8080 types.

For an A/D converter to be most useful in a microprocessor-based system, it must have such desirable analog features as differential inputs, and it should adjust to accommodate various analog input signal ranges. The ADC0801-05 offers differential analog inputs, but it is the converter's span accommodation that allows many unusual and useful analog applications.

The availability of differential analog voltage inputs eliminates the problem of poor analog grounds, since both inputs can be connected directly across the analog signal source.

The negative (normally grounded) analog input lead can be referenced to any desired DC offset voltage to accommodate an input signal range that does not swing down to ground. A DC offset can thus be used at this input to cause a digital output of all 0s at any desired input voltage.

FLEXIBLE SPAN

Finally, the ability to accommodate an arbitrary span or input dynamic voltage range is desirable in an A/D converter. This can easily be achieved in the ADC0801-05 by selecting the magnitude of the converter's reference input.

An example might be to permit an analog input voltage range of 0.5V to 3.5V. This is accomplished by tying the converter's negative input lead to a 0.5 V_{DC} offset voltage and supplying a reference voltage that is equal to half the 3V span. This application provides the 00 output code for V_{IN} = 0.5 V_{DC} and the FF output code for V_{IN} = 3.5 V_{DC}.

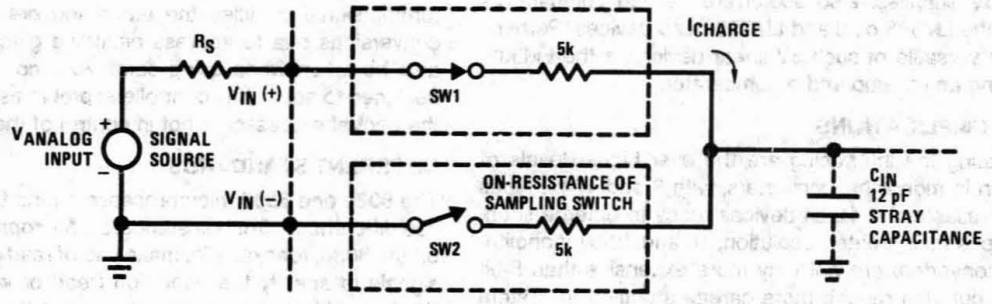
In many applications (such as weighing cans on a production line), 14, or even 16-bit converters are often called upon for the needed high levels of resolution. For those reduced-span applications, an 8-bit A/D converter can be used instead—at considerble savings.

A SAMPLED-DATA INPUT

The ADC0801-05 makes use of a sampled-data comparator. Sampled-data circuits cancel the offset voltage, provide essentially temperature-independent performance, and cancel low frequency MOS 1/f noise. They do, however, provide some differences in application, since there is an input stray capacitance to ground, as shown in *Figure 1*.

When switch S1 is closed, stray input capacitance, C_{IN}, is charged to the input analog potential, V_{ANALOG}. Note that with a stray capacitance of approximately 12 pF and a 5 kΩ MOS switch resistance, the time constant, τ, is only 60 ns. Thus, C_{IN} becomes charged to the necessary accuracy level (within $\pm 1/4$ LSB) in 6.9τ, or about 0.4 μs. Since the input switches are operating at one eighth the input clock frequency of 640 kHz, there is ample time for C_{IN} to settle, as comparisons are made only at the end of the clock period. Note that the switch at the (−) analog input discharges the stray capacitance; this event causes input displacement currents to flow.

Input bypass capacitors, when placed directly at the analog inputs, cause full-scale errors, since they average the current which will flow through the source resistance of the analog input signal generator. Input capacitors are not required; but if they are used, a full-scale adjustment will eliminate any system errors.



TL/H/8721–1

FIGURE 1. Equivalent. Because it has a sampled-data comparator input, the 8-bit ADC0801-05 monolithic analog-to-digital converter looks capacitive to an input signal source. The sampling switches operate at one eighth the rate of the clock frequency.

The ADC0801-05 monolithic 8-bit CMOS A/D converter can be operated with a wide range of $V_{REF}/2$ voltages that facilitates its use in many different circuit applications. Inexpensive ratiometric transducers, such as potentiometers, can be tied across the converter's 5V supply voltage with the wiper fed directly to the converter's V_{IN}^+ input pin. The $V_{REF}/2$ pin, which will now bias at 2.5V, can be tied to a second potentiometer that is also hooked across the supply voltage to provide a full-scale adjustment.

When the $V_{REF}/2$ is grounded, the converter then functions as a comparator, yielding a digital output of all 1s when V_{IN}^+ is greater than V_{IN}^-, and of all 0s when V_{IN}^+ is less than V_{IN}^-. The $V_{REF}/2$ feature is also useful for low level analog voltage systems where an operational amplifier is normally used to boost the input signal prior to digitization. In a circuit with an analog input voltage of 250 mV maximum, for example, the signal can be fed directly to the A/D device, saving the cost of the amplifier. The $V_{REF}/2$ pin would thus be biased at 125 mV.

CAREFUL GROUNDING

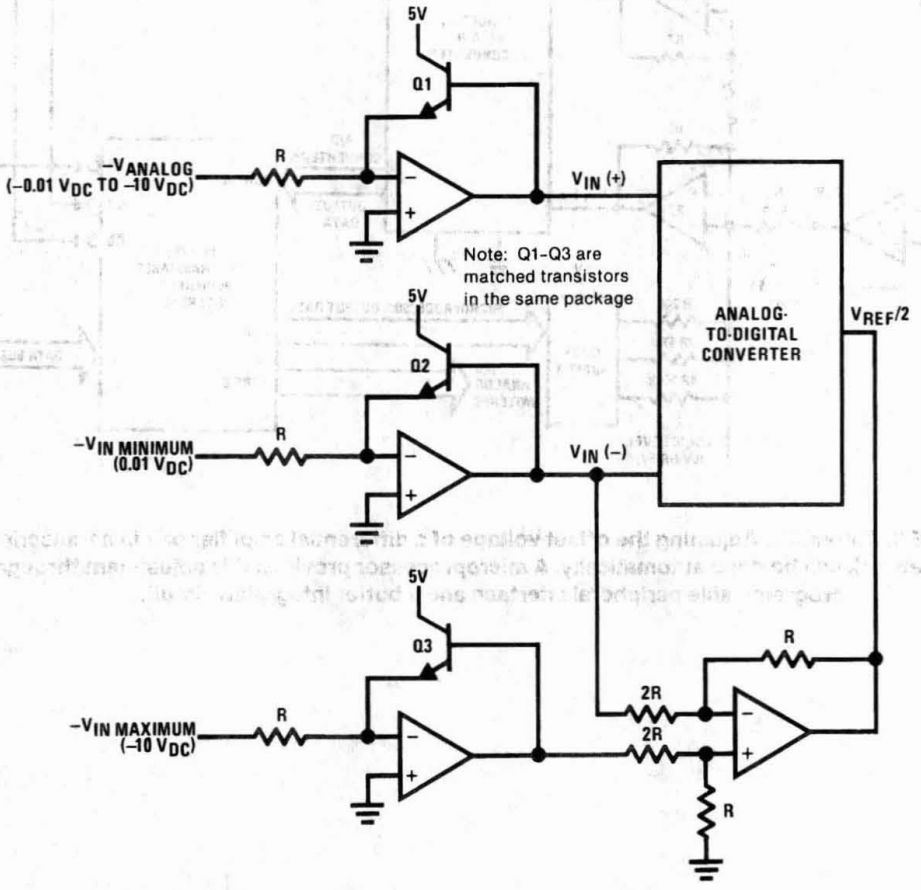
A minor drawback is that this extra analog resolution leaves the circuit more susceptible to noise, and the $V_{REF}/2$ voltage requires a low initial tolerance and must be stable over temperature changes. Grounding problems become more critical and careful grounding is a must.

The ADC0801-05 can also be used as a logarithmic converter to extend the input voltage dynamic range to cover three decades. Three input logging circuits (*Figure 2*) are provided by the NPN transistors in the feedback loops of operational amplifiers. With these at the same temperature (all three on a common chip), there are no thermal problems with this circuit. To keep costs at their lowest, the three transistors in the LM389 audio amplifier IC can be used.

The fourth operational amplifier in *Figure 2* is used to supply the proper $V_{REF}/2$ voltage to the A/D converter. Its DC output voltage is half that of the logarithmically compressed analog input voltage span.

OFFSET ADJUSTING

Yet another application for the ADC0801-05 is in automatically adjusting the offset voltage of an op amp under microprocessor control. This is useful in transducer bridge networks where a pair of amplifiers is normally used to amplify the differential signal. Such an output signal can be fed directly to the A/D converter's inputs without requiring a more costly instrumentation amplifier. The bridge network's arms will thus be biased at approximately $V_{CC}/2$.



TL/H/8721–2

FIGURE 2. Logarithmic. The ADC0801-05 monolithic A/D converter's $V_{REF}/2$ pin allows its use as a three-decade logarithmic circuit. The three NPN transistors in the feedback loops of the operational amplifiers give better accuracy with changing temperature than the diodes normally used.

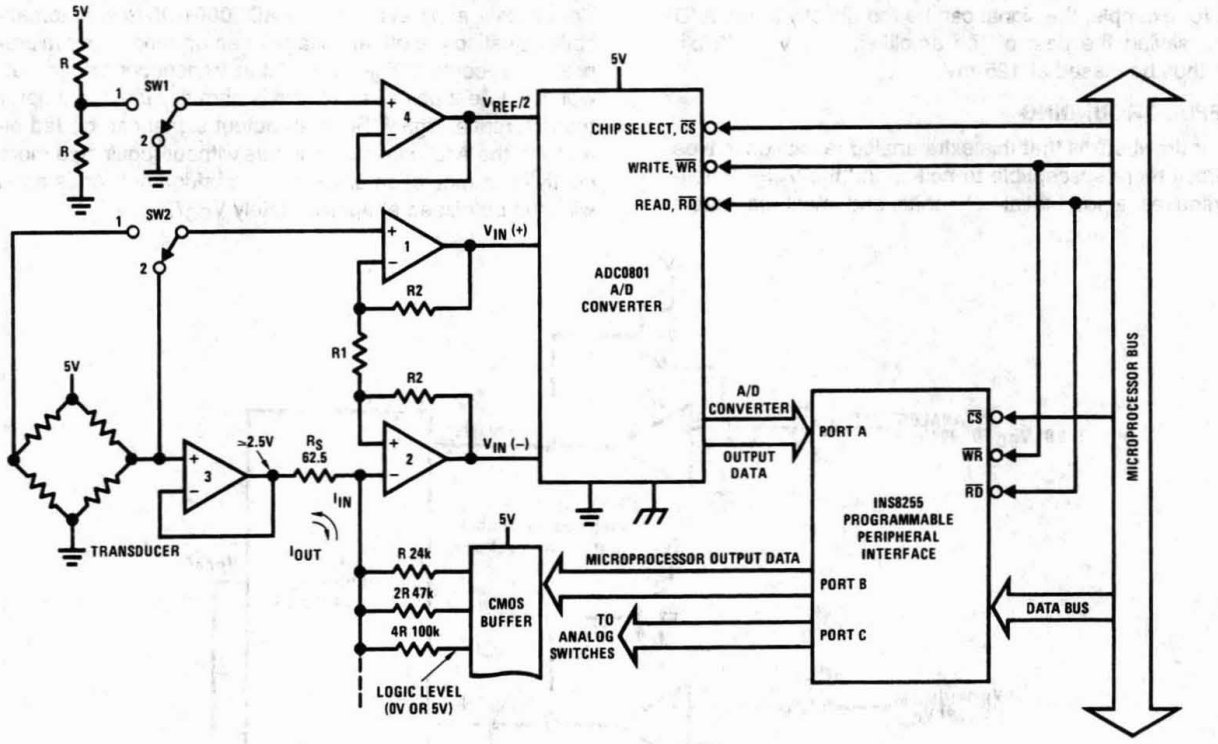
Figure 3 shows such a circuit, where the microprocessor takes the digital output of the A/D device and automatically adjusts the output voltage of operational amplifier 2. This amplifier is used to isolate the bridge network from the offset adjustment circuit. The INS8255 programmable peripheral interface controls the offset voltage adjustment and analog switches 1 and 2. The CMOS buffer provides ideal analog level swings of either 0V or 5V to the binary resistor network. The binary resistor network extracts and injects a current from and into op amp 3, causing a small voltage drop across R_S. This corrects for offset voltage that is introduced anywhere in the system.

AUTO ADJUSTMENT

Electrically actuated switches 1 and 2 allow the automatic adjustment of the offset voltage. It should be noted that op amp 1 is referenced to one side of the bridge network in order to cancel any common-mode offset voltage effects.

The A/D converter acts as a high gain comparator because a 0V $V_{REF}/2$ is provided by the voltage follower (amplifier 4) and switch 1 circuits. This allows the microprocessor to perform a successive approximation routine to null the offset voltage of the system. Resolution is thus considerably better than the normal + 1LSB obtainable with a conventional A/D converter.

The ADC0801-05 combines linear and digital features in an A/D converter that is flexible and easy to tie to microprocessor-based systems. The benefits of a sampled-data comparator and an unusual ladder now make an A/D converter actually easier to fabricate than a digital-to-analog converter.



TL/H/8721–3

FIGURE 3. Automatic. Adjusting the offset voltage of a differential amplifier pair in a transcript bridge network can be done automatically. A microprocessor provides this adjustment through a programmable peripheral interface and a buffer integrated circuit.

CMOS D/A Converters Match Most Microprocessors

National Semiconductor
Application Note 275
James B. Cecil

With double buffering, 8, 9, and 10-bit multiplying units are useful for microprocessor control of gain and attenuation.

A new family of complementary MOS multiplying digital-to-analog converters has arrived on the scene and promises to make microprocessor interfacing truly universal. The double-buffered MICRO-DAC™ units eliminate many common problems, bridging the way to a host of new applications that include microprocessor-controlled gain, attenuation, and multiplication.

The proliferation of the microprocessor in electronic circuits has brought with it an equal proliferation of microprocessor-compatible D/A converters. Many of these converters, however, have shortcomings in that they often require additional external components to be truly microprocessor-compatible. Furthermore, depending on a converter's resolution and data format, a designer is sometimes forced to adopt additional interfacing circuitry for total microprocessor compatibility. Transient output voltage errors can occur during the updating of a 10-bit D/A converter from an 8-bit microprocessor bus, when the two words are transferred to the converter. Left-justified (fractional binary) and right-justified (positionally weighted binary) D/A converter data formats require different interfacing schemes. All of these problems must be considered in interfacing a microprocessor and a D/A unit.

TWO LEVELS OF BUFFERING

The MICRO-DAC family of multiplying D/A converters consists of 8, 9, and 10-bit accurate units designed to interface directly with the 8080, 8048, 8085, Z-80, and other popular microprocessors. The converters appear to the microprocessor as a memory location or as an input/output port and require no interfacing logic. Each has two levels of input buffers—an input latch and a register (*Figure 1*).

The converter's register holds the digital data undergoing conversion, while the input latch is kept busy acquiring new input data. The digital input data is used to update the D/A converter. The double buffering feature allows 10 bits of microprocessor data to be assembled from 2 data bytes. It also prevents the analog output from changing while the digital input word is updated.

Even when used with 16-bit microprocessors, the double buffering feature is necessary for the simultaneous updating of many D/A converters. Double buffering establishes the proper conditions for the next test or lets new system parameters be set up at the same time.

Two groups of MICRO-DAC converters are available. The DAC1000, DAC1001, and DAC1002 are 24-pin units with 10, 9, and 8-bit accuracy levels, respectively. Each contains all of the necessary logic functions for interfacing with right-justified and left-justified microprocessor data. The DAC1006, DAC1007, and DAC1008 20-pin units are designed for left-justified data at accuracy levels of 10, 9, and 8 bits, respectively.

All the members of this family of multiplying D/A converters feature standard chip select (CS) and write (WR) microprocessor control signals. Data on the microprocessor bus can be written into the D/A converter in a standard write cycle.

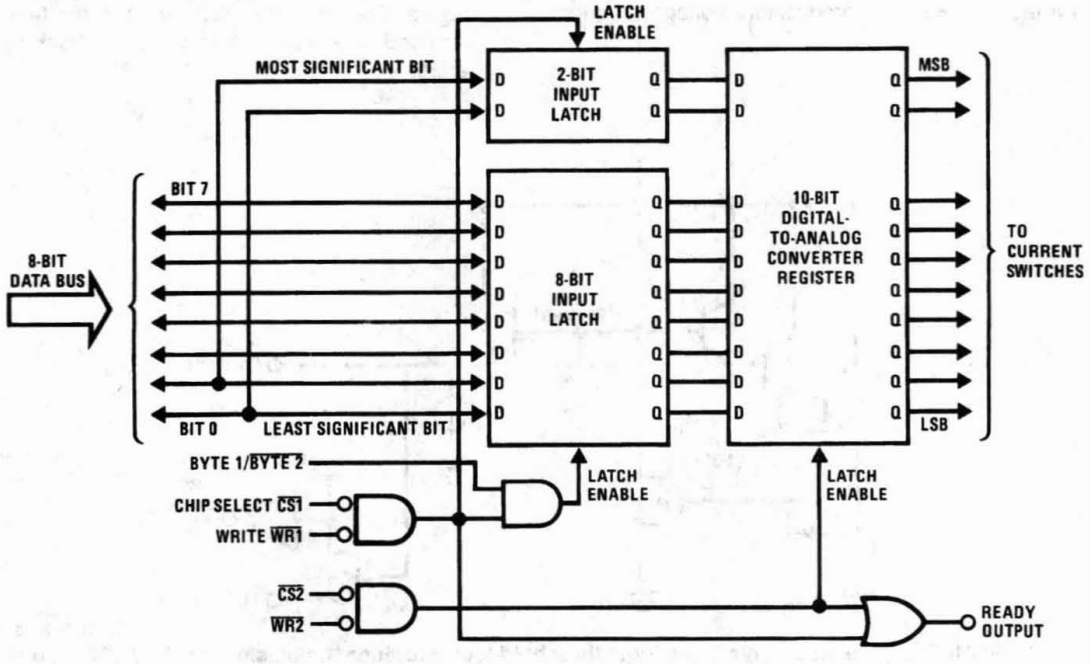


FIGURE 1. Double buffered. The MICRO-DAC family of 8, 9, and 10-bit digital-to-analog converters has two levels of input buffers—an input latch and a register. They are designed to interface with 8080-, 8048, 8085, Z-80, and other popular microprocessors, with no interfacing logic.

HANDLING THE DIFFERENT DATA FORMATS

Different data formats exist for many D/A converter products, all of which must be readily handled when interfacing with a microprocessor. Left-justified (fractional number × V_{REF}) and right-justified (positional number × $V_{REF}/1,024$) are the main ones. Initially, converter manufacturers favored a left-justified approach in which the most significant bit was labeled bit 1. Newer converters have changed to the right-justified approach to match the data format of microprocessor data buses. Nevertheless, the left-justified approach is still widely used. As previously mentioned, the MICRO-DAC family can readily handle left- and right-justified data formats with no additional interfacing circuitry.

When a MICRO-DAC converter uses either an 8-bit (two write cycles) or a 16-bit (one write cycle) data bus, all 10 locations of the converter's input latch are enabled on the first write cycle from the microprocessor. Depending on the data format, the next write cycle, if used, overwrites 2 of the 10 locations at the proper data rate.

Digital data is transferred from the input latch to the register internally in one of three ways: automatically when the second write byte occurs; through microprocessor control, which allows the updating of several D/A converters if this is necessary; and through the use of an external strobe.

The converter's CMOS logic levels are made compatible with those of TTL by a special biasing circuit that uses the parasitic NPN bipolar transistor available on a CMOS chip. The bipolar transistor supplies a base-emitter voltage (V_{BE}) that acts as a reference for the converter's digital inputs. It supplies an input threshold voltage of 2 V_{BE} that has the same amplitude as that of TTL devices.

Details of the biasing circuit are shown in *Figure 2*. Note that the reference N-channel field-effect transistor, Q1, is tied in a feedback loop so as to have its gate voltage biased at a level of V_{THN}, causing it to conduct the 60 μA shown in its drain circuit. The three NPN transistors in the loop add a voltage of 3 V_{BE} to V_{THN}. The output emitter-follower, Q2, causes a loss of V_{BE}, thus producing a voltage reference of 2 V_{BE} + V_{THN} for use by all of the logic input circuits. Each of the input stages has FETs like Q3, whose source has the digital input applied to it and whose geometry is the same as that of FET Q1. Like Q1, Q3 also has 60 μA of current feeding its drain. When the logic input voltage equals 2 V_{BE}, Q3 conducts, thereby pulling the input of a standard CMOS inverter to a low level. This 2 V_{BE} threshold continues to be independent of the D/A converter's supply voltage. 2 V_{BE} is the logic threshold voltage of standard TTL gates.

ACHIEVING HIGH ACCURACY

The design of the MICRO-DAC's resistor network is simple, even though it provides high levels of converter accuracy. *Figure 3* shows the current switching inverted R-2R ladder used, which consists of passive components.

The operation of the ladder network requires that all of the 2R legs connect to a 0V, or ground, level. This means that the external operational amplifier shown must have a minimal offset voltage. Only 1 mV of offset voltage can introduce a 0.01% linearity error into the converter's operation. Operational amplifiers like National's LM308A series are available with low offset voltages, and they require no zero adjustments.

When zero adjustment of the operational amplifier's offset voltage is required, a 1 kΩ resistor can be temporarily switched in between the converter's $I_{OUT\ 1}$ terminal (which is tied to the amplifier's negative input terminal) and ground. No DC balancing resistance should be used in the operational amplifier's grounded positive input terminal, since it may create errors. The operational amplifier, a BI-FET™ LF356 (made with bipolar and field-effect transistors), has a low input bias current which makes it an ideal choice for use as a current-to-voltage converter. The amplifier's offset voltage should be adjusted with a digital input of all zeros to force $I_{OUT\ 1}$ of the converter to a zero current level. The manually switched-in resistor provides a DC gain of about 15 to the offset voltage and makes the zeroing easier to sense. The converter chip provides the feedback resistor for good initial matching as well as for tracking over temperature.

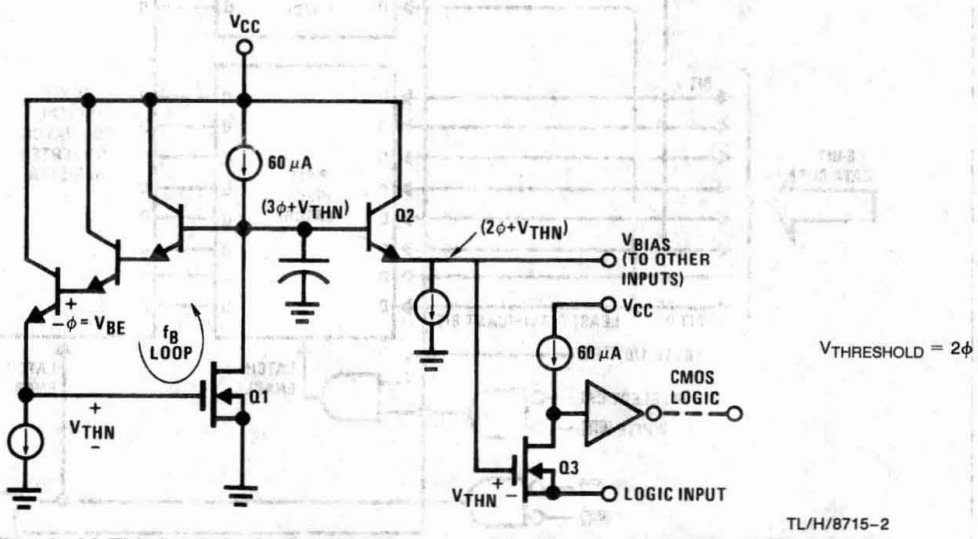


FIGURE 2. Threshold. This basic logic threshold loop provides the biasing for the MICRO-DAC family of MOS D/A converters to interface with TTL voltage levels. This circuit uses the parasitic bipolar structure, which delivers an input threshold of 2 V_{BE} to the biasing circuit.

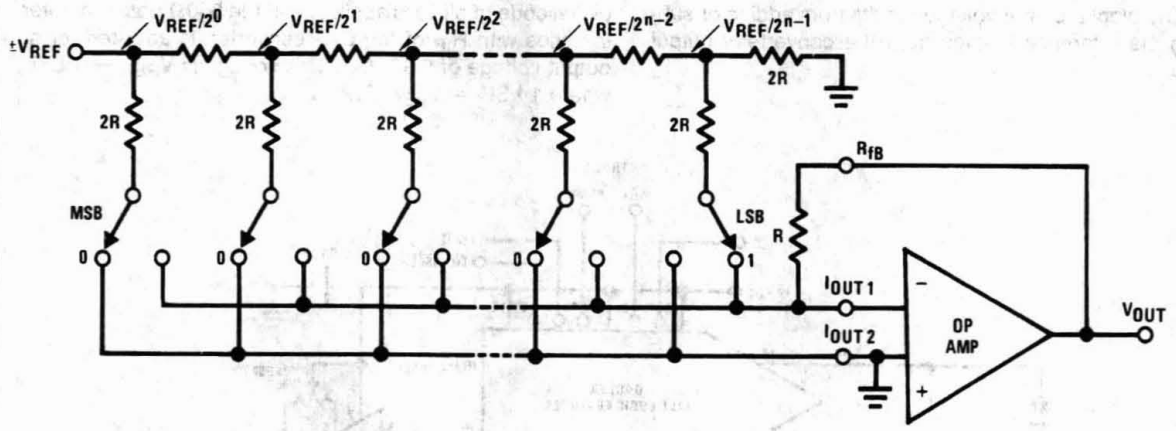
LOOKING AT THE INSIDE

An examination of the internal details of the single-pole, double-throw current-mode switches employed in the converters shows that the N-channel FETs' gates are driven from the D/A converter's supply voltage. In contrast to a 5V supply, a 15V level reduces the FETs' on-resistances and thereby improves the converter's performance.

MICRO-DAC converters are relatively stable in gain and linearity during variations in the 15V supply voltage. For example, a drop in supply voltage all the way down to 5V results in a gain error of only −0.1%. Even smaller is the change in linearity error for the same supply voltage swing—just −0.005%.

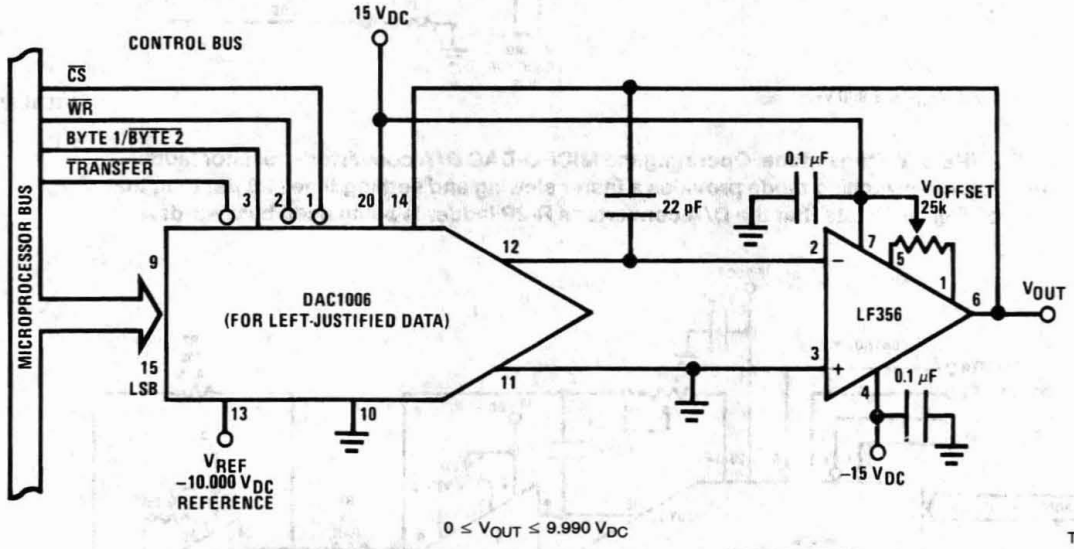
The usefulness of a D/A converter can be determined by the magnitude of the linearity errors resulting from changes in the reference voltage. For applications, like multiplication, that require small values of reference voltage, small linearity errors are essential. In the case of the MICRO-DAC converters, reducing the reference voltage from 10V to 1V results in a worst-case linearity error change of approximately 0.005%.

Figure 4 shows a typical application of a MICRO-DAC as a unipolar voltage output device. This circuit inverts the negative reference voltage to a positive output, with a maximum value of 1,023/1,024 of the reference voltage multiplied by V_{REF}. The BI-FET operational amplifier used is an LF356 that slews and settles within 3 μs.



TL/H/8715–3

FIGURE 3. Ladder. The current-switching, current-mode R-2R resistor ladder of the MICRO-DAC family of D/A converters is simple, yet provides high levels of converter accuracy. The external operational amplifier is chosen for minimal offset voltage for the least converter linearity error.



TL/H/8715–4

FIGURE 4. Unipolar. In a typical unipolar application, a MICRO-DAC D/A converter inverts the negative reference voltage to a positive one. The positive output is 1,023/1,024 of the negative reference voltage multiplied by 9.990 V_{DC}. The output amplifier slews within 3 μs.

Operating the MICRO-DAC's R-2R resistor ladder in a voltage switching mode as shown in *Figure 5* gives a faster slewing and settling time—1.8 μs. The ladder is being used backwards. The reference voltage that is derived from the LM336 reference diode is applied to the $I_{OUT\ 1}$ pin. An output voltage is produced at the converter's pin 15 where the reference voltage was previously located in *Figure 4*. This output voltage ranges from 0 to (1,023/1,024) (2.49 V_{DC}). The LF356 operational amplifier used supplies a gain of a little more than 4 for an overall output voltage ranging from 0 to 1 LSB less than 10V (or 9.990 V_{DC}). The two compensating diodes at the ends of the full-scale adjustment potentiometer on the LM336 reference improve the temperature stability of the reference voltage.

For a bipolar output voltage, the circuit in *Figure 6* may be used. The bipolar output voltage results from adding or subtracting the reference voltage from the converter's output voltage.

The output of operational amplifier 1 ranges from 0 to $-1{,}023/1{,}024 \times V_{REF}$ (or $-9.990\ V_{DC}$). This voltage is then applied to operational amplifier 2, where a gain of -2 doubles the voltage range. A $-10\ V_{DC}$ offset voltage at the output of operational amplifier 2 is provided by adding the converter's reference voltage to the amplifier's input. Resistors R1, R2, and R3 in the circuit of operational amplifier 2 must stay matched even during temperature changes for the circuit of *Figure 6* in order to work properly.

The bipolar converter of *Figure 6* is adjusted by first entering a digital code composed of all zeros into the D/A converter. Next, the offset potentiometer of operational amplifier 1 is adjusted for a zero amplifier output voltage and then the offset potentiometer of operational amplifier 2 is adjusted for an amplifier output voltage of $-10{,}000\ V_{DC}$. Finally, a digital code of all 1s is applied, and the 500Ω potentiometer, in series with R_{fB} of the D/A converter, is adjusted for an output voltage of 9.98 V_{DC}. This voltage is $V_{REF} - 1$ LSB, where 1 LSB = $V_{REF}/512$.

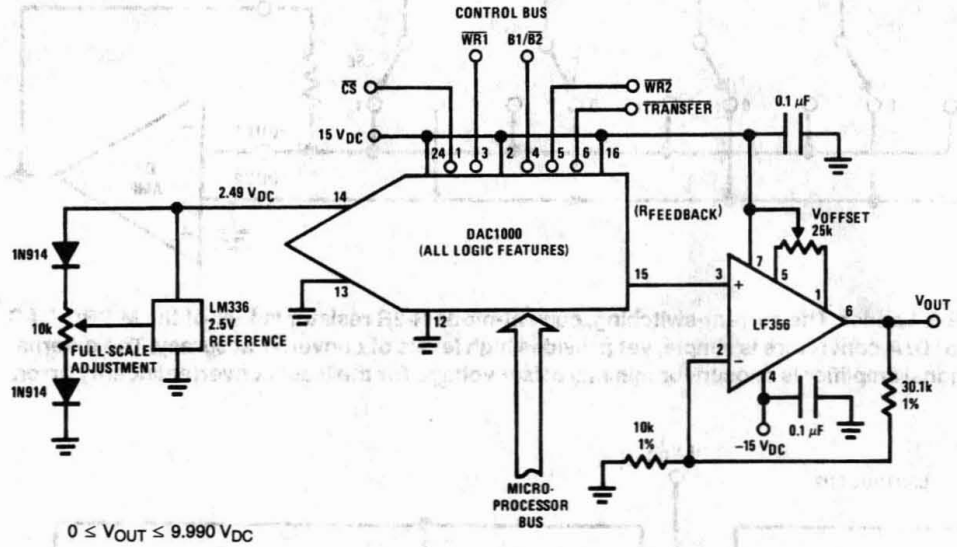


FIGURE 5. Voltage mode. Operating the MICRO-DAC D/A converter's resistor ladder in a voltage-switching mode provides a faster slewing and settling time (1.8 μs) than that of *Figure 4*. Note that the D/A converter's R-2R ladder is being used backwards.

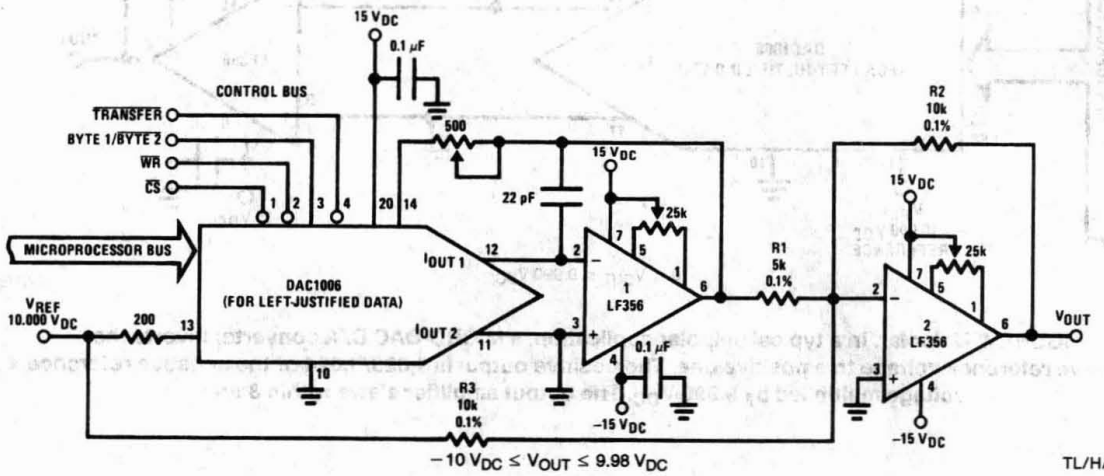


FIGURE 6. Bipolar. By adding and subtracting the MICRO-DAC D/A converter's reference voltage from its output voltage, a bipolar output results. For this circuit to work properly, however, resistors R1, R2, and R3 in the circuit of op amp 2 must stay matched during temperature changes.

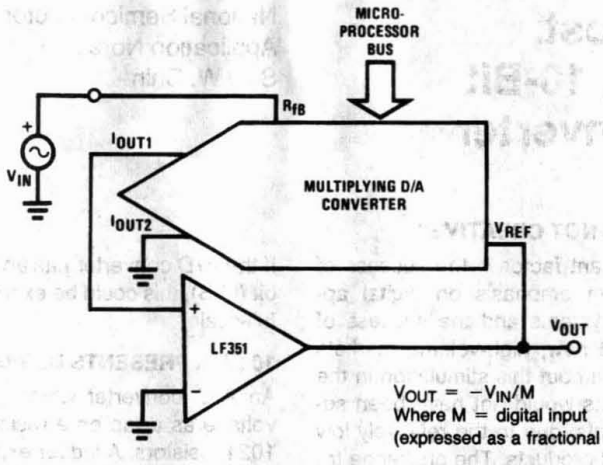


FIGURE 7. Control. A MICRO-DAC D/A converter can be used for microprocessor control of an amplifier circuit. Since the converter has 4-quadrant multiplication capability, AC and DC signals can be handler. The feedback resistors referred to but not shown is in the converter.

USING THE MICROPROCESSOR FOR CONTROL

The MICRO-DAC multiplying D/A converter can be used in a microprocessor-controlled amplifier circuit as the feedback element for the amplifier *(Figure 7)*. Since the converter has 4-quadrant multiplication capability, both AC and DC signals can be handled. The feedback resistor (not shown) is the internal one on the D/A converter's chip.

The D/A converter in *Figure 7* automatically provides an output voltage that causes the current from the converter's $I_{OUT\ 1}$ terminal to the V_{REF} terminal to equal the input current, $V_{IN}R_{fB}$. Note that when the microprocessor provides data to the D/A converter with the LSB set to a 1, a relatively large value of the reference voltage is needed to balance the input current. This value corresponds to the maximum gain of $-1{,}024$. The minimum gain of $-1{,}024/1{,}023$ is obtained for a D/A converter digital input of all 1s. In all, 1,023 gain steps are provided.

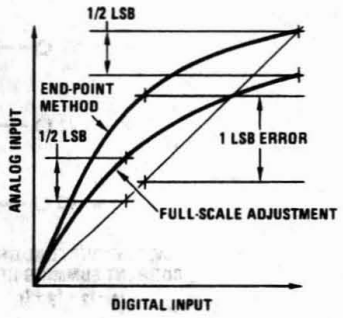
The addition of another amplifier in the converter's $I_{OUT\ 2}$ leg produces a microprocessor-controlled amplifier and attenuator. Compared with the gain of the circuit that appears in *Figure 7*, the gain here is noninverted and ranges from 0 to 1,022.

END POINT VS BEST-STRAIGHT-LINE

To maximize their product yields, manufacturers of digital-to-analog converters like to use a best-straight-line linearity guarantee. Unfortunately, this method is based on iteration of the zero and full-scale converter adjustments, so that errors are optimally split and equidistant from a straight line. To the converter user, a best-straight-line specification means that the D/A converter must undergo a sophisticated adjustment procedure for its linearity to be proven. Furthermore, each D/A converter has a different best-straight-line fit, making it necessary to adjust every one of them individually.

Another way to specify converter linearity is by an end-point method. For a current output converter, the offset voltage of the current-to-voltage output amplifier is first adjusted for 0V output. Then the converter is adjusted with a full-scale input digital code to produce a full-scale output voltage. This simple technique ensures that each of the 10-bit unit's 1,024 steps are within the stated linearity specification. Further, a pretrimmed output amplifier can be used to eliminate the zero offset adjustment, leaving only the full-scale adjustment.

The differences between the best-straight-line and end-point specification techniques are shown in the illustration (below), where a D/A converter with an error of 1 least significant bit is shown failing the end-point linearity test. Note that by readjusting the converter's full-scale output, the D/A converter's error is optimally split on either side of the ideal line in a best-straight-line fit, which is a time-consuming procedure, particularly when done on a large number of individual converters. For many an application where the D/A converter is already mounted on a printed circuit board, the end-point adjustment of zero and full-scale is much less time-consuming. Furthermore, this end-point procedure is a more stringent guarantee of converter linearity than the best-straight-line approach. The end-point method is used for D/A converters in the MICRODAC family.



TL/H/8715–8

A New, Low-Cost, Sampled-Data, 10-Bit CMOS A/D Converter

National Semiconductor
Application Note 276
Sing W. Chin

"IF IT'S NOT LOW COST, IT'S NOT CREATIVE"

Cost is the single most important factor in the success of any new product. The current emphasis on digital approaches to build electronic systems and the success of microprocessors have created new, high-volume markets for low cost A/D converters. Without this stimulation in the marketplace, converter products would not have been selected as monolithic components, due to the relatively low volume usage of the traditional products. The challenge today, therefore, is to find new design solutions which will reduce costs of A/Ds without sacrificing the performance specifications.

HOW MANY BITS ARE NEEDED?

The question of how many bits are needed in the A/D converter for a particular system is not always easy to answer. This is further complicated because of the distinction which must first be made between resolution and accuracy. For example, your digital bathroom scale may have graduations which indicate each pound over a range which extends from zero to 300 pounds maximum. This means you are capable of "resolving" one pound over this complete dynamic range or "span." The next question is, "What do I really weigh, say, on my doctor's scale?" You may find that his scale indicates you are actually three pounds heavier than your scale indicates: this is the accuracy problem.

A 10-bit A/D is capable of resolving 2^{10}, or 1024, minimum voltage levels over the range from 0 to V_{REF} volts. To put this into the physical world we live in, this degree of resolution is capable of differentiating each single sheet of paper, which is only 0.004 inches (4 mils) thick in a stack of paper 4 inches high. In any stack of paper up to this maximum limit, a 10-bit A/D could be used in an electronic system which would sound an alarm if a sheet was added to or removed from the stack. (For simplicity, this assumes we have a perfect height transducer and perfect analog signal conditioning circuitry between this transducer and the input to the A/D.)

If the A/D converter has an accuracy of ±1 least significant bit (LSB), this could be expressed as ±1/1024 or ±0.1% of full-scale.

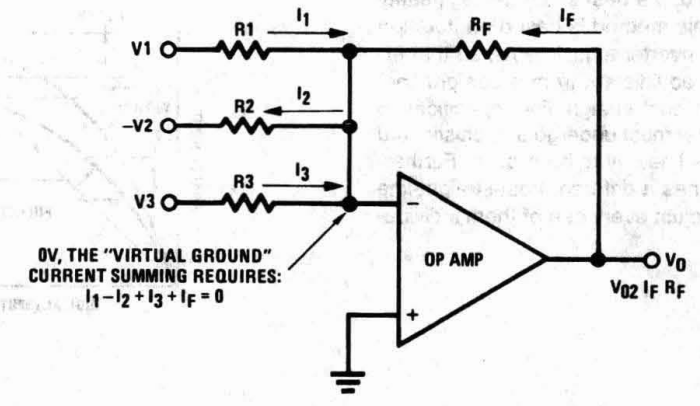
10 BITS PRESENTS DESIGN PROBLEM

An A/D converter which provides every possible analog voltage as a tap on a resistor ladder would require 2^{10}, or 1024 resistors. A ladder expansion technique has been previously developed which has greatly reduced the number of resistors. This technique has been used to provide an 8-bit A/D (the ADC0804 family) which uses a theoretical minimum of only 7 resistors. (In practice, extra resistors are typically used to improve matching by making use of unit resistors.)

This 8-bit A/D design was the starting point for developing this 10-bit converter. A new idea, which is key to the 10-bit design, is a novel way to, in effect, use the previous 8-bit circuit four times to increase the resolution to 10 bits†. This was achieved by adding 2 MSBs to the 8-bit design. We will first review the 8-bit A/D operation as a basis for understanding the new 10-bit design.

THE BASIC 8-BIT DESIGN

The essential part of the ADC0804 8-bit A/D family is a novel, multiple input, voltage comparator. This circuit allows a new feature for a comparator: multiple, differential voltages can be accepted as simultaneous inputs to the comparator, and each differential input can be weighted by scaling the size of the associated input capacitor. The traditional op amp summing circuit, *Figure 1*, is similar, but accepts single-ended voltage inputs, and first converts each input voltage to an input current by making use of a scaled or weighted input resistor. These input currents are then algebraically summed at the "virtual ground" or summing junction (the (−) input of an op amp which has the (+) input grounded). The current surplus (or deficiency) is supplied through the feedback resistor to produce the output voltage.



TL/H/8716–1

FIGURE 1. The Traditional Op Amp Summing Circuit

†This design concept was proposed and implemented by John Connolly.

A more useful voltage comparator results from a sampled-data approach, which involves switches and capacitors. Now, input voltages are converted to input charges by the use of input capacitors, and the resulting charges are then algebraically added at a "charge summing" node.

A multiple, differential input, sampled-data comparator is shown in *Figure 2* with the switches in the zeroing cycle. The input-output short, which is accomplished with SW5 around the inverting gain block (provided by a logic inverter), causes this stage to bias at a fixed DC voltage. For example, a standard CMOS inverter will bias at approximately one half of the power supply voltage. Notice that at this time the input switches, SW2 and SW4, are precharging the input capacitors with the (−) input voltages of the differential inputs. These input capacitors will serve as storage elements to remember both of the (−) input voltages and the biasing voltage of the gain stage.

These zeroing switches are then opened. The gain stage is now active and will respond to any deviations in the input voltage. An input voltage results when the switches SW1 and SW3 are subsequently both closed. As shown in the figure, ΔV1 is positive, which inputs a charge, Q1, proportional to the value of C1, (Q1 = ΔV1C1). If ΔV2 is negative, a charge, Q2, will be removed from the charge summing node. If the charges Q1 and Q2 are balanced, there is no net change in the input voltage of the inverting gain block.

These switches are dynamically cycled by a clock and the system is zeroed prior to each measuring interval. This is the same operating mode as has been used years ago by the auto-zeroed or chopper-stabilized op amps. A sufficient number of these stages are capacitor-coupled to provide an adequate overall gain for the comparator.

MAKING AN 8-BIT A/D

This sampled-data comparator was made the heart of an 8-bit A/D converter, as shown in *Figure 3*. The comparator now has four differential voltage inputs; one for the analog inputs and three for the DAC. The first 4 MSBs of the 8-bit A/D are supplied by the DAC switches, S1 and S2. As shown, the positions of S1 and S2 correspond to the digital code, "10 00," for the first 4 bits of the 8-bit word. This should input $V_{REF}/2$ from the DAC. Note that S1 is selecting $\frac{3}{4}$ V_{REF} and S2 is selecting $\frac{1}{4}$ V_{REF}, and these voltages are the first differential pair which is sampled by SW1 and SW2 at the start of a successive approximation search. This provides ($\frac{3}{4}$ $V_{REF} - \frac{1}{4}$ V_{REF}) or $\frac{1}{2}$ V_{REF} as required from the DAC.

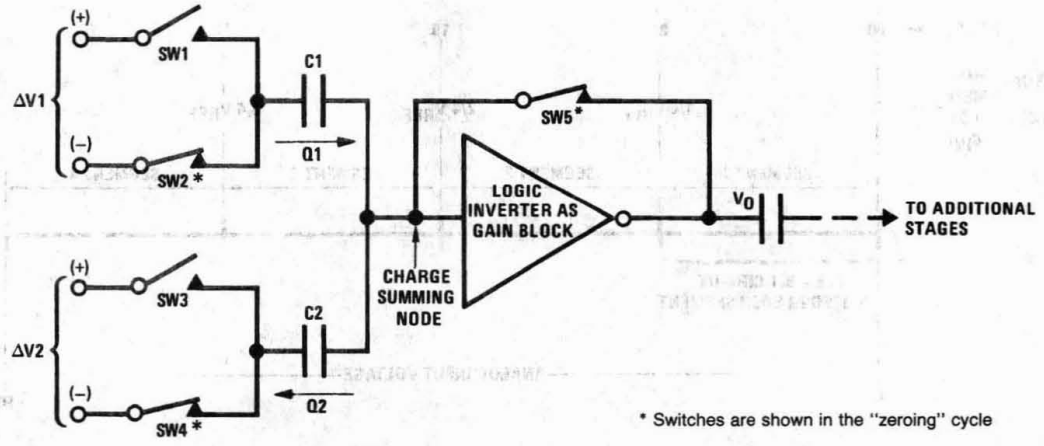
The differential input feature of this comparator has allowed an unusual resistor ladder to be used for the DAC. Notice that the top three resistors (each labeled "R") have $\frac{1}{4}$ V_{REF} across them and the lower resistors (each labeled "R/4") have $\frac{1}{16}$ V_{REF} across them. The comparator, therefore, allows the increased resolution of the S2 selected voltages to be "fitted into" each section of the upper or S1 selected voltages. In this way, the first 4 bits of this differential DAC, or "DDAC," are realized.

This same 4-bit trick is used again via the left side decoding switches, S3 and S4. These same voltage values provide charge which is reduced in significance by 16:1, making the input capacitor for this section a factor of 16 smaller. This now provides the least significant 4-bit group. The additional capacitor, C, and the lowermost two resistors (labeled "R/8") supply a $\frac{1}{2}$ LSB overall DAC offset voltage. This is used in A/Ds to center the natural $\pm\frac{1}{2}$ LSB quantization uncertainty of the A/D about the integer LSB values of analog input voltage. (This is $\frac{1}{2}$ LSB voltage is added to the analog input to cause the 00_{HEX} to 01_{HEX} code change of the A/D to occur at any analog input voltage value of only $\frac{1}{2}$ LSB.)

If we are to use this basic 8-bit design for a 10-bit converter, we must make these 8 bits the least significant of the 10-bit data word. This can easily be done by again scaling the capacitor sizes. Further, 2 additional MSBs must be added: here is where another trick comes in.

A NOVEL WAY OF ADDING 2 MSBs

The 2 MSBs of the DAC will control 2^2, or 4, voltages. If these are chosen as V_{REF}, ground, $\frac{1}{3}$ V_{REF} and $\frac{2}{3}$ V_{REF} we have an unusually beneficial situation. Notice that the differential voltage input feature of the sampled-data comparator allows picking up the two intermediate voltages ($\frac{1}{3}$ and $\frac{2}{3}$ V_{REF}) from a resistor divider with only one tap, as shown in *Figure 4*. These odd voltage values ($\frac{1}{3}$ and $\frac{2}{3}$ V_{REF}) from this 2 MSB DAC are "cleaned up" simply by scaling the size of the input capacitor which is used for this DAC section by a factor of $\frac{3}{4}$. This will, therefore, provide the $\frac{1}{4}$ V_{REF} increments 0, $\frac{1}{4}$ V_{REF}, $\frac{2}{4}$ V_{REF} and $\frac{3}{4}$ V_{REF}, which are necessary for the 2 MSBs. Now the basic 8-bit circuit can be used a total of 4 times, with each referenced to one of these $\frac{1}{4}$ V_{REF} values. This will cover the analog input voltage range of 0 to V_{REF} with 10 bits of resolution, as shown in *Figure 5*.



* Switches are shown in the "zeroing" cycle

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FIGURE 2. A Multiple, Differential Input Sampled-Data Comparator or Charge Summing Circuit

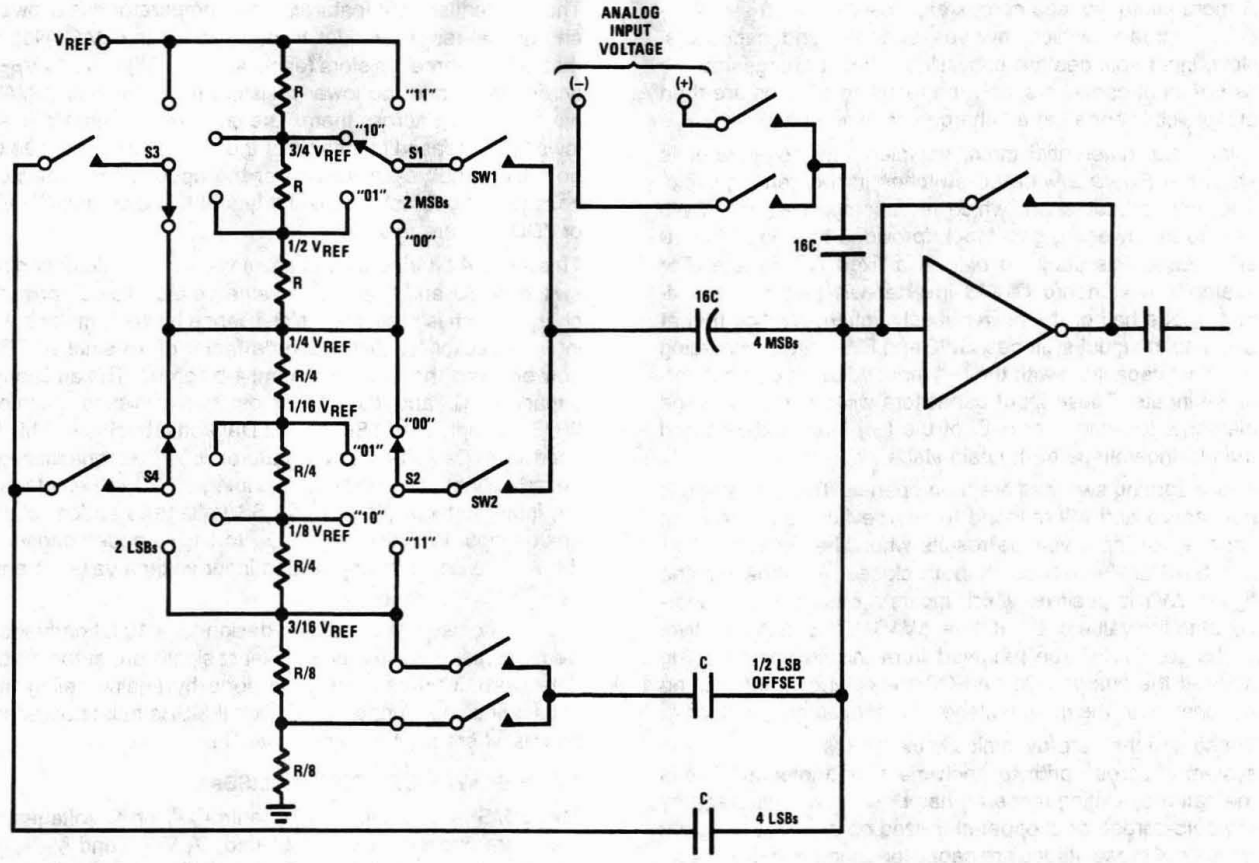

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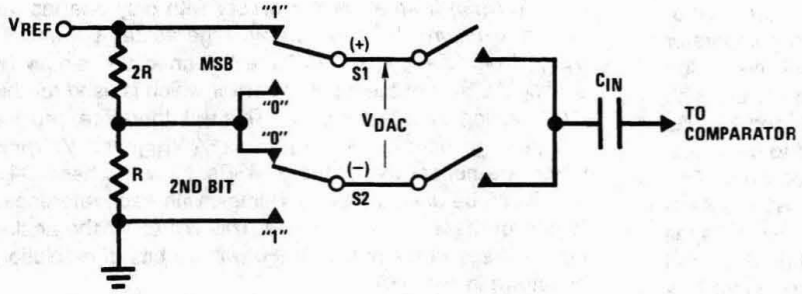
FIGURE 3. Basic DAC Ladder of 8-Bit A/D Converter



S1 (MSB)	S2 (2nd Bit)	V_{DAC}
0	0	0
0	1	$\frac{1}{3} V_{REF}$
1	0	$\frac{2}{3} V_{REF}$
1	1	V_{REF}

TL/H/8716–4

FIGURE 4. Providing the 2 MSBs of a 10-Bit A/D

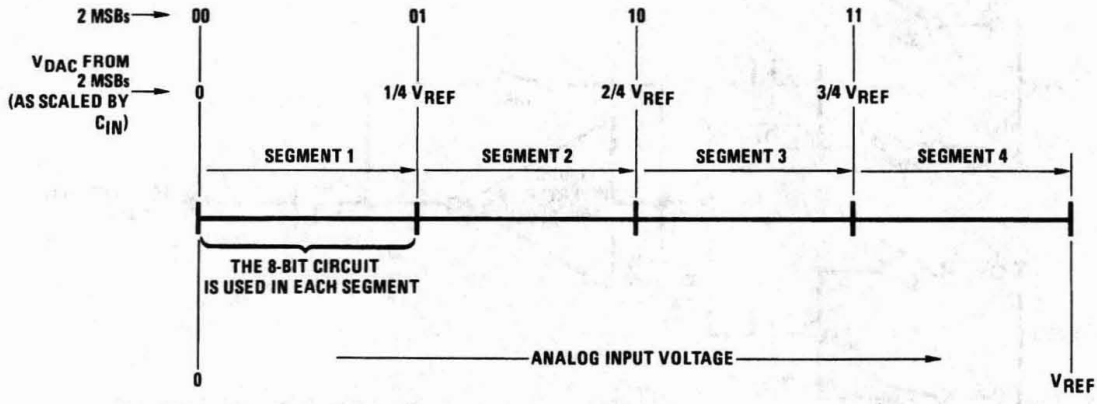


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FIGURE 5. How the 2 MSBs Extend the 8-Bit Circuit to 10 Bits

This 2 resistor ladder will produce linearity errors in only 2 of the segments of the overall A/D transfer characteristic, because there will be no errors in the first segment (2 MSBs = 0), because V_{DAC} for this code is 0V. Similarly, if we assume that the input capacitors ratio properly, there will be no linearity errors in the last segment, because the full V_{REF} is sampled (then is weighed to produce $\frac{3}{4}$ V_{REF} as compared to the analog input voltage, via C_{IN}). Any mismatch between the C_{IN} of the analog differential input voltage and the C_{IN} of the DACs will cause a full-scale error, not a linearity error.

The two end segments are therefore both free of linearity errors and an additional benefit is that any error in the exact value of the tap voltage on a 2 resistor divider has the natural characteristic that the error is the same magnitude on the $\frac{1}{3}$ V_{REF} and $\frac{2}{3}$ V_{REF} voltages, and is simply of opposite sign. Thus, a linearity trim must provide a single magnitude of correcting charge, then this same charge is introduced into the comparator summing mode in one polarity for the "01" 2 MSB code, and then the opposite polarity for the "10" code (a correcting charge is not used for the "00" or "11" codes).

THE ADC1001, A 10-BIT A/D

In keeping with the similarity to the previous 8-bit A/D, a 10-bit product was designed to fit in the same 20 pin (0.3" wide) package and to use the same pinouts. Now a customer can easily interchange from an 8 to a 10-bit A/D. This allows for a range of performance variation in his end products while using the same PC board.

The problem of getting the 10-bit output of the A/D onto an 8-bit data bus is handled by reading two 8-bit bytes. The data is left-justified and transferred, most significant byte first. This allows a single read cycle to pick up a valid 8-bit representation (the 8 MSBs) and can save time if this is all the resolution that is required on a particular analog channel. A second read cycle will pick up the 2 LSBs of the 10-bit data word. The 6 LSB positions are set to zero in this second byte. An internal byte counter keeps track of the byte sequencing so multiple, double-read cycles can be made, if desired.

The problem of properly biasing a 5 V_{DC} reference circuit when operating from only a single 5 V_{DC} power supply voltage was handled on the 8-bit part by reducing the operating reference voltage for the internal DAC to only 2.5 V_{DC}. This can be designed to still provide a 5V full-scale for the A/D by simply doubling the sizes of all of the DAC input capacitors to the comparator. This technique was also used for this 10-bit product. The reference voltage can also be further reduced in magnitude to increase the analog resolution over a reduced analog input voltage span, if desired.

A basic diagram of the DAC and the comparator input section of the 10-bit A/D are shown in *Figure 6*. A simplified schematic representation has been used for the 8 LSB section. This has been shown in more detail in *Figure 3* without the V_{REF} reduction to $V_{REF}/2$.

To understand the scaling shown for the input capacitors, keep in mind that it is the input charge which is balanced. This means that a maximum differential analog input voltage of 5V would produce an input charge of 5 x 32C or 160C

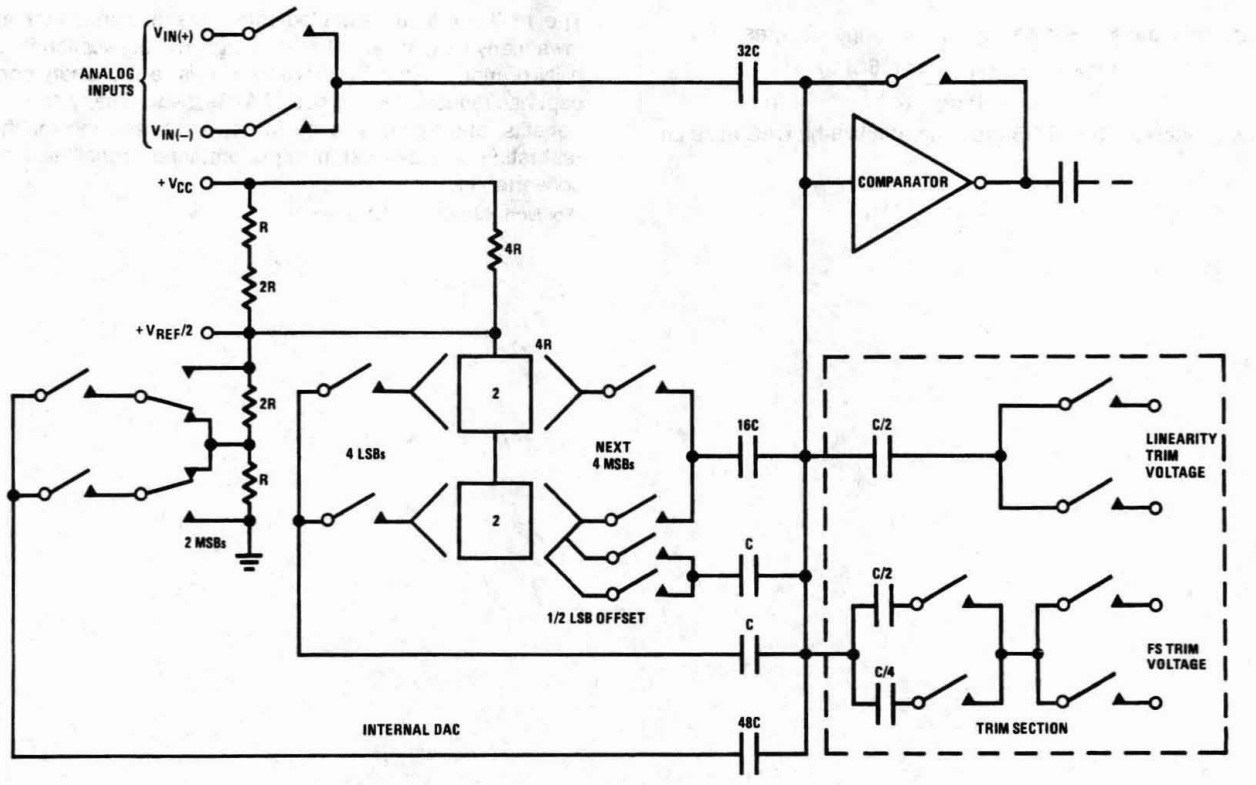

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FIGURE 6. The DAC and Comparator Input Section

coulombs. If the DAC were forced to a "11 0000 0000" or 300_{HEX} code, the voltage, which is output from the 2 MSB section, would be $V_{REF}/2$. This is converted to an input charge via the 48C capacitor, so this charge, $Q300_{HEX}$, becomes:

$$Q300_{HEX} = \frac{V_{REF}}{2} \times 48C$$

and as $V_{REF}/2 = 2.5V$

then

$$Q300_{HEX} = 2.5\,(48)C$$

or

$$Q300_{HEX} = 120C$$

which ratios to the analog full-scale charge, Q_{AFS} as

$$\frac{Q300_{HEX}}{Q_{AFS}} = \frac{120C}{160C} = \frac{3}{4}\,FS$$

which is the proper weight for the 300_{HEX} code.

Similarly, the "00 1000 0000" or 080_{HEX} code should require $\frac{1}{8}$ (V_{REF}) at the analog input (neglecting the effects of the $\frac{1}{2}$ LSB offset voltage shift) to balance. This is the output of the 8 LSB section with a binary code of "1000 0000" input to this DAC section. The charge from the analog input, Q_A, which corresponds to an analog input voltage of $\frac{1}{8}$ V_{REF}, is given by:

$$Q_A = \frac{1}{8}(V_{REF})\,(32C)$$

The output voltage of the 8-bit DAC section for 080_{HEX} code is $\frac{1}{2}$ $(V_{REF})/2$, so the charge input by this DAC, Q_{DAC}, is given by

$$Q_{DAC} = \frac{1}{2}\frac{(V_{REF})}{2}\,(16C),$$

and this ratios to the analog input change, Q_{A1}, as

$$\frac{Q_{DAC}}{Q_A} = \frac{\frac{1}{2}\,(V_{REF}/2)\,(16C)}{\frac{1}{8}\,(V_{REF})\,(32C)} = 1$$

as expected. The 4 LSB grouping of this 8-bit DAC uses an input capacitor $\frac{1}{16}$ smaller in value to properly reduce the significance of the last 4 bits.

FULL-SCALE TRIM

Full-scale (or "gain") errors are trimmed by introducing an additional correcting charge into the summing node of the comparator. This is done in steps; for example, no full-scale correction is used on the first $\frac{1}{4}$ of the analog input voltage range (near zero). The next range receives $\frac{1}{3}$ of the total FS correcting charge, then $\frac{2}{3}$, and finally the full charge is introduced in the last section. This sequencing of the FS trim is achieved by dynamically altering the input capacitance from no capacitance to C/2, to C/4, and finally to 3C/4. This is the reason for the extra input capacitor and the added switches, which are shown in the FS trim section of *Figure 6*.

APPLICATIONS

The standard applications of the 8-bit ADC0804 series* can now easily be extended to 10 bits by simply plugging in the new ADC1001 10-bit part. In addition, a 24 pin product (ADC1021) is also available, which brings all 10 bits out for a 16-bit data bus application.

The zero offsetting (by introducing a DC shifting voltage into the $V_{IN(-)}$ pin) can be used to accommodate analog input voltages which do not swing to ground. The $V_{REF}/2$ input voltage can also be reduced to accommodate a reduced span of analog input voltages. Finally, system designers can use the same PC board for either an 8-bit or a 10-bit product to take advantage of the standard pinouts used for these A/D converters.

CONCLUSIONS

The multiple, input, sampled-data voltage comparator allows many benefits in both the design and application flexibility of monolithic A/D converters. This revolutionary concept has reduced the die size of A/Ds, allows many product benefits, and appears to be the optimum solution for the realization of a low cost, high performance, monolithic A/D converter line.

*For further details see data sheet.

The New MICRO-DAC™ Product Line for Microprocessor Systems

National Semiconductor
Application Note 277
James B. Cecil

A second generation of the popular MDAC (or multiplying DAC) is now available which has been designed to provide an easy interface to microprocessor systems. These new MICRO-DAC products are low power drain CMOS converters, which typically require only 0.5 mA supply current (2 mA max) and draw only approximately 600 μA from a 10 V_{DC} reference supply.

The basic problems which are inherent in bipolar designs are not present in this CMOS product. CMOS devices have nearly infinite current gain, therefore there are no β or α errors in the design. Also, there is no analogous term to offset voltage in these products, rather, an ON CMOS switch is nothing more than a small resistor which can be controlled by device geometry. To avoid the temperature coefficient and piezoresistive problems of diffused resistors, silicon chromium thin-film resistors are used.

These resistors track within 1 ppm/°C, which insures excellent temperature tracking characteristics. Also, the feedback resistor, which is needed with an external op amp, is provided on the chip, which insures a low temperature coefficient of the gain or full-scale reading of the DAC.

Bipolar designs in the 10-bit region can have a power dissipation of 300 mW. Unless extreme care is taken to insure an almost perfect thermal die layout, it is very possible to have a 1°C temperature gradient on the die. If a diffused resistor ladder were to be used in the presence of this gradient, it will cause a 0.15% error. This means that all of the allowable error in a 10-bit DAC will be used up due to this thermal gradient. From this, it is obvious that the CMOS DAC, with its combination of a low temperature coefficient thin-film resistor ladder and an on-chip power dissipation of 30 mW max, will overcome one of the major problems in bipolar designs.

DATA FORMATS AND DATA BUFFERS

From the digital viewpoint, a DAC seems little more than a *write only memory* where the information in the memory is made available as the analog output voltage. Problems arise concerning data formatting. Is the data to be left-justified (fractional binary) or right-justified (positionally weighted binary)? Also, updating a 10-bit DAC from an 8-bit bus can cause transient output voltage errors until the complete new word has been transferred.

The data format options are shown in *Figure 1*. Early converter manufacturers favored fractional binary, and this has caused the MSB to be labeled as "Bit 1" on DAC products. As may be expected, this convention has been changed in the new converter products to match the notation of the bits on the data bus of μPs. People supplying converter products still favor the fractional binary format, but it appears that the user groups are approximately split on the question of which to use.

MSB									**LSB**
1	0	1	0	1	0	1	0	2	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}
1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512	1/1024

V_{OUT} = (fractional binary number) × V_{REF}

a) Left-Justified Data

MSB									**LSB**
1	0	1	0	1	0	1	0	1	0
2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
512	256	128	64	32	16	8	4	2	1

V_{OUT} = (positionally weighted binary number) × V_{LSB}
where $V_{LSB} = V_{REF}/1024$

b) Right-Justified Data

FIGURE 1. Data Formats for a 10-Bit Converter

Both of these problems go away with the addition of flexible input digital data buffers (latches) which allow complete applications flexibility (*Figure 2*). For example, with two levels of input buffers (double buffering), the DAC Register has the job of holding the current digital data which is being converted, and the other, the Input Latch, is then available to acquire new digital data which will eventually be used to update the DAC. This allows 10 bits to be assembled with two data bytes from the μP and prevents the transient output error at updating time. Further, even with 16-bit μPs, double buffering is necessary to allow many DACs to be updated simultaneously. This is useful to establish the proper conditions for a next test, or to allow new system parameters to be set up at the same time.

Data formatting is handled by providing flexibility in the way the digital data is entered into the Input Latch. To allow operation with either an 8-bit (two write cycles) or a 16-bit (one write cycle) data bus, all 10 locations of the Input Latch are enabled on the first write cycle from the μP. Then, depending on the data format, the next write cycle, if used, will overwrite two of these locations with the proper data.

Two product options are offered, as shown in the matrix of *Figure 3*. Each of the 2 functional options is offered in accuracies of 8, 9 or 10 bits. The 20 pin 0.3" wide packages are used for fixed left-justified data format. The 24 pin part is pin programmable for either right- or left-justified data.

All of these options make use of the standard μP control signals, such as $\overline{CS}$ and $\overline{WR}$, and the data on the bus can be read by the converter in a standard write cycle. As expected, the internal CMOS logic is faster for higher supply voltages, and this effect on the write strobe width is shown in *Figure 4*.

The internal transfer of the digital data from the Input Latch to the DAC Register can be controlled in three ways: 1) automatic transfer when the second byte occurs, 2) use the μP to control the transfer—this signal can update several DACs, if desired, or 3) use an external strobe to cause the transfer.

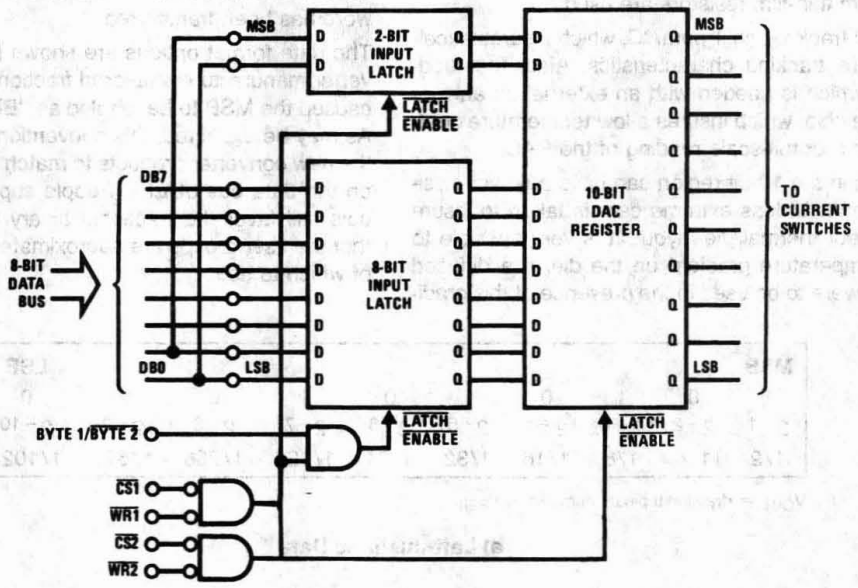

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FIGURE 2. Double-Buffering the Digital Input Data

Part #	Accuracy (Bits)	Pin	Description
DAC1000	10	24	Has All Logic Features
DAC1001	9		
DAC1002	8		
DAC1006	10	20	For Left-Justified Data
DAC1007	9		
DAC1008	8		

FIGURE 3. MICRO-DAC Product Options

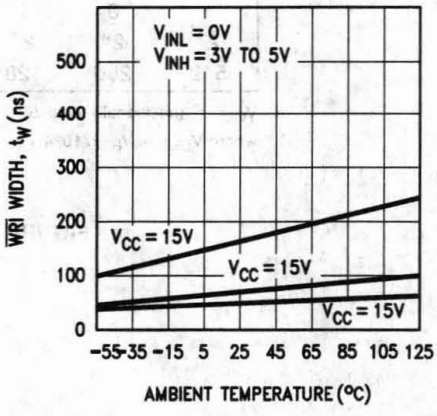

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FIGURE 4. Write Strobe as a Function of the V_{CC} Supply Voltage and Temperature

MEETING T²L INPUT VOLTAGE SPECS WITH CMOS

Logic compatibility is aided by having the CMOS logic inputs meet T²L voltage level specs. A special biasing circuit makes use of the parasitic NPN bipolar transistors which are available on the CMOS chip (*Figure 5*). These bipolar devices will supply base-emitter voltage, V_{BE}, references for the digital inputs. By using this circuit, these CMOS MICRO-DAC products have the same input voltage threshold, 2 V_{BE}, as exists with standard T²L!

The details of this bias referencing circuit are shown in *Figure 6*. Notice that the reference N-channel transistor, Q1, is tied in a feedback loop, which forces it to conduct the 60 μA which is supplied to its drain. The gate voltage of the transistor thus biases at V_N, the voltage which is necessary for Q1 to conduct the 60 μA. The three NPN transistors add 3 V_{BE} to this voltage. The output emitter-follower, Q2, causes a loss of 1 V_{BE} and produces a voltage reference of 2 V_{BE} + V_N to be used by all of the logic input circuits. One of these input stages, Q3, is also shown on this figure. Note that the digital input is applied to the source of Q3. This transistor has the same geometry as Q1, and also has a 60 μA current source feeding its drain. Due to device matching, Q3 will therefore conduct when the logic input voltage is equal to 2 V_{BE}, and this is the logic threshold *voltage of standard T²L logic gates.* The variation of this logic threshold with supply voltage and temperature is shown in *Figure 7*. This input circuitry may surprise a new user because here is a CMOS part which outputs 60 μA of current at the digital input leads when pulled to the low voltage state!

ON THE ANALOG SIDE

Conceptually, it is easiest to think of DACs which use binary weighted resistors. Unfortunately, the large resistance ratios which result have limited this design approach to 4-bit converters where the ratio is 16 to 1.

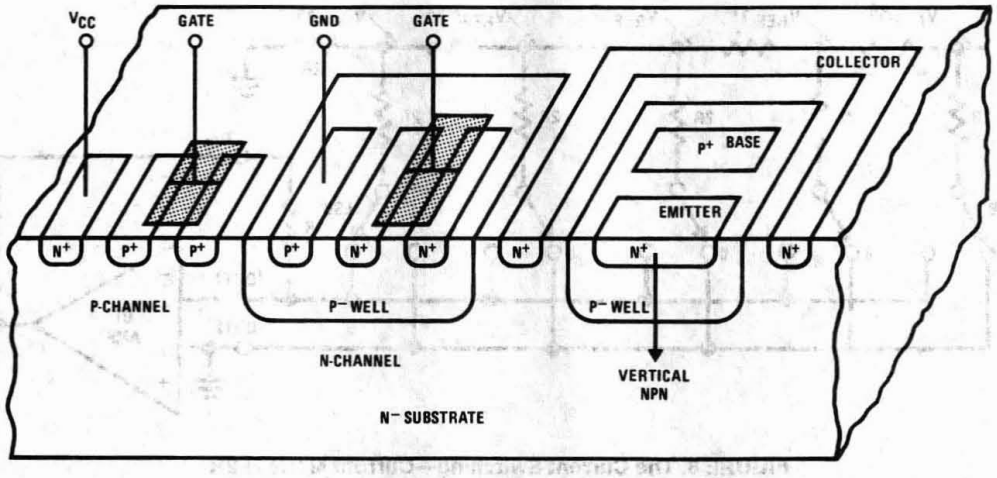

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FIGURE 5. A Simplified Wafer Cross Section Showing the CMOS FETs and the NPN Bipolar Transistor

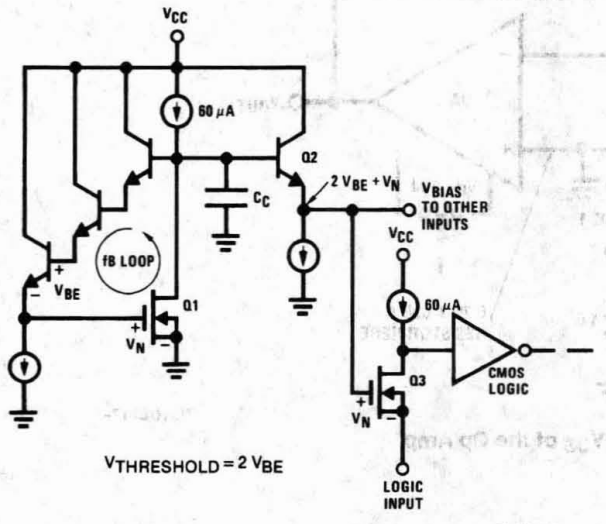

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FIGURE 6. Basic Logic Threshold Loop

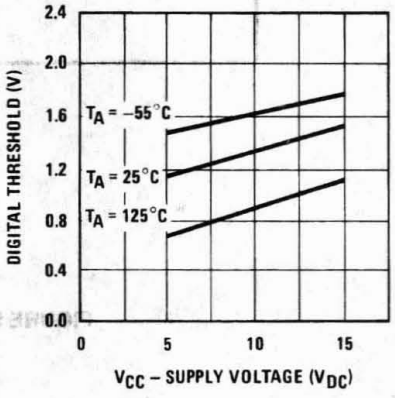

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FIGURE 7. Digital Input Threshold vs Supply Voltage

The R-2R resistor ladder is an old trick to keep the resistors always in a 2:1 ratio, independent of the resolution of the converter. Three variations on the use of these ladders exist which depend on whether voltages or currents are being switched, and whether the output from the ladder is a current or a voltage. The current-switching, current-mode, R-2R ladder is used in the MICRO-DAC products and is shown in *Figure 8*. This is the heart of the analog section of the DAC and, as can be seen, it consists of all passive components. This inherent simplicity is the strong point of this design approach. The main DAC design problem is to provide a relatively straightforward function—but to do it with a very high accuracy!

Proper operation of the ladder requires that all of the 2R legs always go to exactly 0 V_{DC} (ground). Therefore, offset voltage, V_{OS}, of the external op amp cannot be tolerated, as every millivolt of V_{OS} will introduce 0.01% of added linearity error. At first this seems unusually sensitive, until it becomes clear that 1 mV is 0.01% of the 10V reference!

High resolution converters of high accuracy require attention to every detail in an application to achieve the available performance which is inherent in the part.

Also note that no "DC balancing" resistance should be used in the grounded positive input lead of the op amp, *Figure 9*. This resistance and the input current of the op amp can also create errors. The low input biasing current of the BI-FET™ op amps makes these ideal for use in DAC current-to-voltage applications. The V_{OS} of the op amp should be adjusted with a digital input of all zeros to force I_{OUT1} = 0 mA. A 1 kΩ resistor can be temporarily connected from the inverting input to ground (*Figure 9*) to provide a DC gain of approximately 15 to the V_{OS} of the op amp and make the zeroing easier to sense. Note also that the feedback resistor for the op amp is provided on the chip and should always be used. This guarantees both a good initial matching and this resistor will match the R-2R ladder over temperature changes.

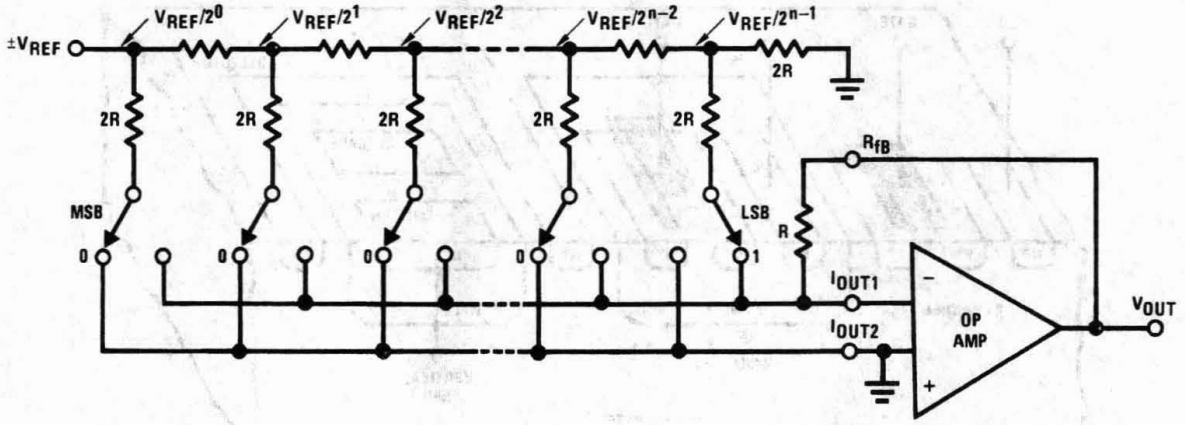

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FIGURE 8. The Current Switching—Current Mode R-2R Ladder of the MICRO-DAC Products

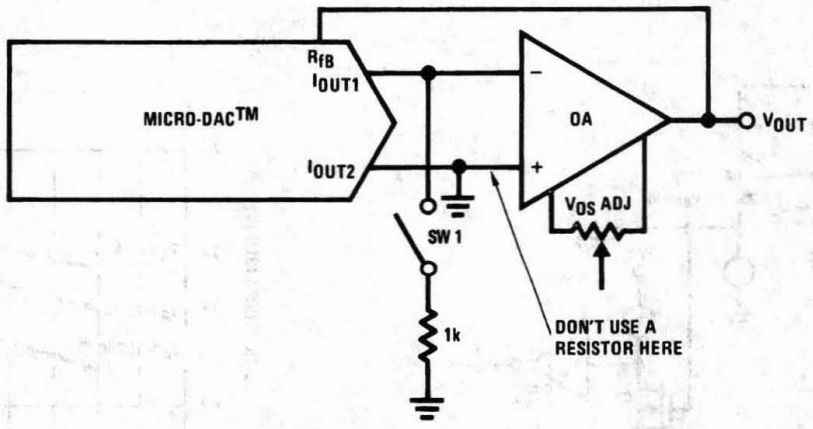

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FIGURE 9. Adjusting the V_{OS} of the Op Amp

The internal details of the SPDT current-mode switches are shown in *Figure 10*. The N-channel transistors are driven by the V_{CC} supply voltage which is used for the part. Operation at 15 V_{DC} reduces the switch ON resistance as compared to the use of a 5 V_{DC} supply and, therefore, improves the performance of the DAC. The change in gain and linearity errors as a function of the supply voltage are shown in *Figure 11*. These curves are normalized to the performance with a 15 V_{DC} power supply and show the degradation as the supply voltage is reduced.

The usefulness of a DAC can be determined by noting the linearity errors which result as the magnitude of the reference voltage is reduced. This is important for multiplication applications and other uses which require small values of reference voltage. In the case of the MICRO-DAC converters, reducing the reference voltage from 10V to 1V results in a linearity error change of approximately 0.005%.

END POINT GUARANTEE VS BEST-STRAIGHT-LINE

Suppliers of DACs like to use a Best-Fit Straight-Line linearity guarantee to increase yields. Unfortunately, this technique is based upon iterating the zero and the full-scale adjustments to optimumly split the errors to be equidistant from a straight line. To the user, this means that each DAC has to go through a rather sophisticated adjustment procedure to home in on this best approximation—which is different for each part.

The alternative specification is called an End Point Spec. This means that after a standard zeroing of the V_{OS} of the op amp (the DAC itself doesn't require a zero adjustment, so a pre-trimmed low V_{OS} op amp can eliminate this adjustment) and a standard full-scale adjustment, the linearity of *each of the 1024 steps* is within spec! This is a large benefit to the DAC user.

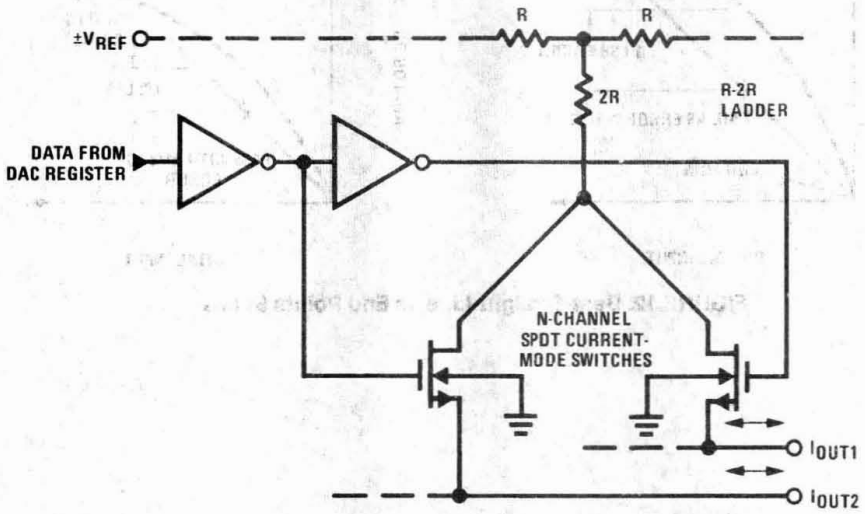

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FIGURE 10. The Basic DAC Circuit

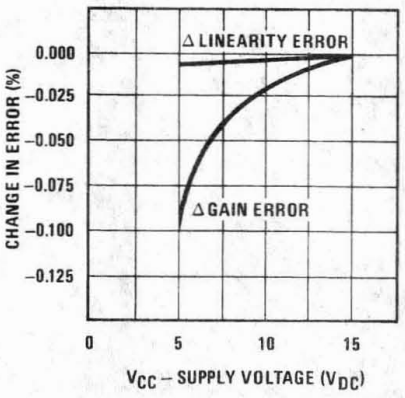

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FIGURE 11. Effects of Supply Voltage on Linearity and Gain Error

The differences between these specification techniques are shown in *Figure 12*. A DAC with an error of 1 LSB and failing the end point test is shown in *Figure 12*. Notice that by readjusting the full-scale, the error of this DAC can be optimumly split to be symmetrically located about a Best-Fit Straight-Line. This search for the optimum end point readjustments has to be done by the user for each individual DAC. The end point spec allows standard zero and full-scale adjustment procedures to be used in PC board assembly, and no time-consuming searching or special readjusting techniques need to be used. Further, it can be seen that the end point spec is a more stringent requirement on the linearity of the DAC.

SUMMARY

The CMOS current-switching DACs have evolved from the unbuffered MDACs to the μP compatible double-buffered MICRO-DAC products. Many non-DAC applications have been generated for the MDACs and we now have the new possibility of μP controlled gain, attenuators and multipliers—all of which easily interface to a μP system. These new low cost monolithic DACs will open up many new applications in the modern electronic systems.

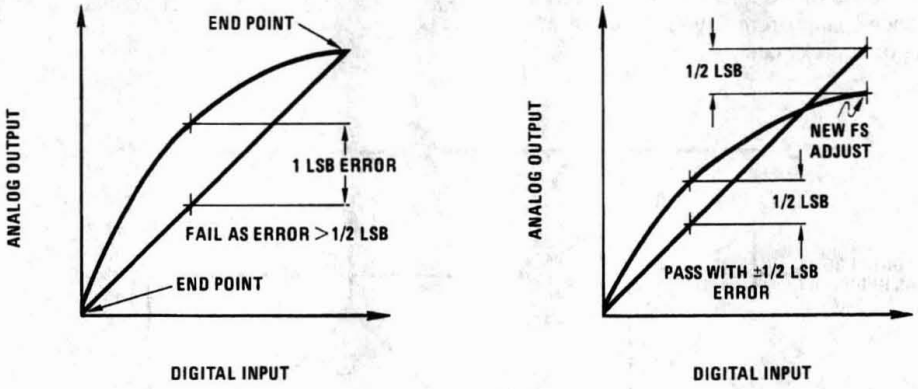

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FIGURE 12. Best-Straight-Line vs End Points Specs

Designing with a New Super Fast Dual Norton Amplifier

National Semiconductor
Application Note 278
Timothy T. Regan

WHY ANOTHER NORTON AMPLIFIER?

The current differencing Norton amplifier has been widely applied over the last 5 years because of the versatility and availability of quad Norton amplifiers (the LM3900). These low cost quads are found today in a wide variety of analog systems, but primarily in medium frequency and single supply AC applications. Today, a brand new dual current differencing amplifier, the LM359, offers spectacular speed improvements which can be used in circuits operating well beyond the video frequencies.

How the speed is improved: The speed improvement of the new Norton amplifier is due to the cascode circuit (*Figure 1*). Cascode circuits are used in high frequency single-ended amplifier designs because there is no Miller effect on the collector-to-base capacitance of the input transistor. Also, there is no collector-to-emitter parasitic feedback in the common base configured transistor, Q2, so the high frequency signal appearing at the output of the cascode does not reflect back into the input. Furthermore, note that band-limiting PNP transistors are eliminated from the signal path; here PNPs are used only for collector loads, so not only is high speed maintained, but high gain is also obtained without additional amplification stages.

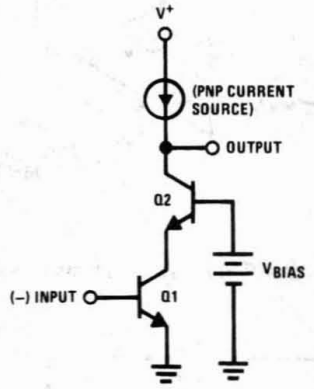

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FIGURE 1. Basic Cascode Circuit

Adding a mirror to get differential inputs: To make the high frequency single-ended amplifier more versatile differential inputs should be provided. An easy way is to add a current mirror across the negative (inverting) input terminal (*Figure 2*). This method provides current differencing, as the current entering the non-inverting input is extracted from the inverting input current. The LM359 is then a current differencing, as opposed to a voltage differencing, op amp.

The programmable features extend versatility: An additional feature of the LM359 is the programmability of its speed, its input impedance, and its output current sinking capability for line driver applications and for control of overall power consumption (*Figure 3*). An internal compensation capacitor is adequate compensation for all inverting applications where the gain is 10 or higher. An additional compensation capacitor can be added externally to reduce undesired bandwidth or to fit any particular application, as will be discussed later. The following sections illustrate some new design ideas using this fast Norton amplifier.

A NEW HIGH FREQUENCY ACTIVE FILTER STRUCTURE

Multiple op amp active filter building blocks are very popular because of their low sensitivities and their tunability. The basic element of such a filter is the inverting integrator. Usually two inverting integrators are cascaded and a third inverter allows closing the overall loop with the proper phase. This is the idea behind the state variable and bi-quad filter structures which today are fully available in low cost hybrid forms.

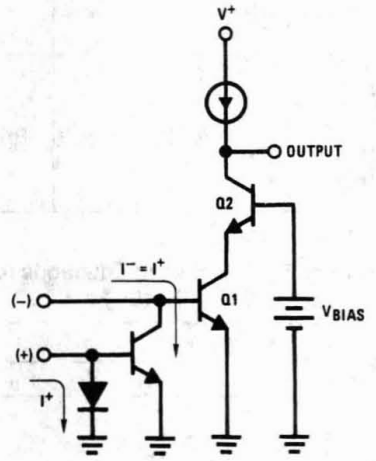

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FIGURE 2. Adding a Current Mirror to Provide Current Differencing Inputs

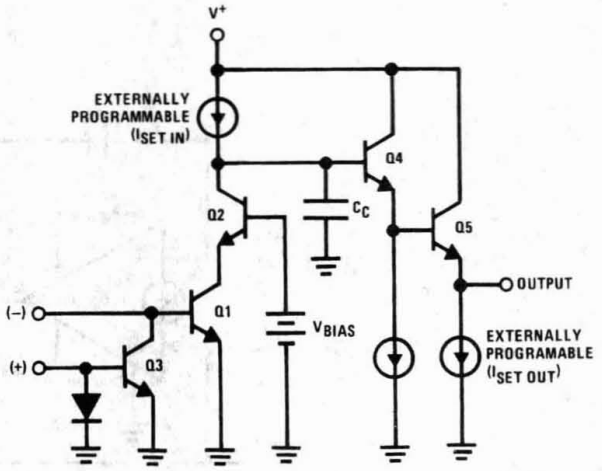

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FIGURE 3. A Simplified Schematic of the LM359, a High Speed, Current Differencing Amplifier. The Input, Output and Speed Characteristics are Externally Programmable.

The op amp count in these filters could be reduced by one (allowing use of a dual op amp instead of 3 op amps or a quad) if a true non-inverting integrator could be built with a single op amp. Unfortunately, this cannot be done with standard op amps but is a trivial task with current differencing amplifiers (*Figure 4*). Combining a non-inverting integrator with an inverting one, a new high frequency and low sensitivity active filter building block can be made (*Figure 5*). Table I shows the 3 particular filter structures, together with their design equations, which are derived from *Figure 5*. The frequency compensation for the 2 amplifiers is asymmetric to optimize performance. Also, since the LM359 is a wide bandwidth amplifier, high frequency circuit layout is strongly recommended. The circuit works with a single supply, and the output DC biasing of each filter type is provided with 2 resistors, R1 and R_b, which should be chosen according to Table II.

TABLE I. Analysis and Design Equations

Type	V_{O1}	V_{O2}	C_i	R_{i2}	R_{i1}	f_o	Q_o	f_Z (Notch)	H_o (LP)	H_o (BP)	H_o (HP)
I	BP	LP	O	R_{i2}	∞	$\frac{1}{2\pi RC}$	$\frac{R_Q}{R}$	–	$\frac{R}{R_{i2}}$	$\frac{R_Q}{R_{i2}}$	–
II	HP	BP	C_i	∞	∞	$\frac{1}{2\pi RC}$	$\frac{R_Q}{R}$	–	–	$\frac{R_Q C_i}{RC}$	$\frac{C_i}{C}$
III	Notch or Band-Reject	–	C_i	∞	R_{i1}	$\frac{1}{2\pi RC}$	$\frac{R_Q}{R}$	$\frac{1}{2\pi RR_i CC_i}$	–	–	$\frac{C_i}{C}$ as $f \rightarrow \infty$ $\frac{R}{R_1}$ as $f \rightarrow 0$

TABLE II. DC Biasing Equations for $V_{O1}(DC) \cong V_{O2}(DC) \cong V^+/2$

Type I	$\frac{2V_{IN}(DC)}{V^+(R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type II	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type III	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; \frac{1}{R1} = \frac{V_{IN}(DC)}{V^+(R_{i1})} + \frac{1}{2R}$

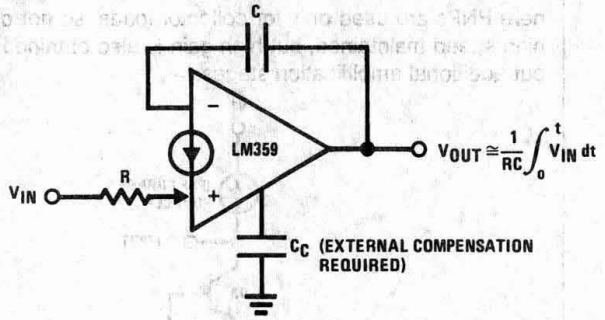

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FIGURE 4. A True Non-Inverting Integrator

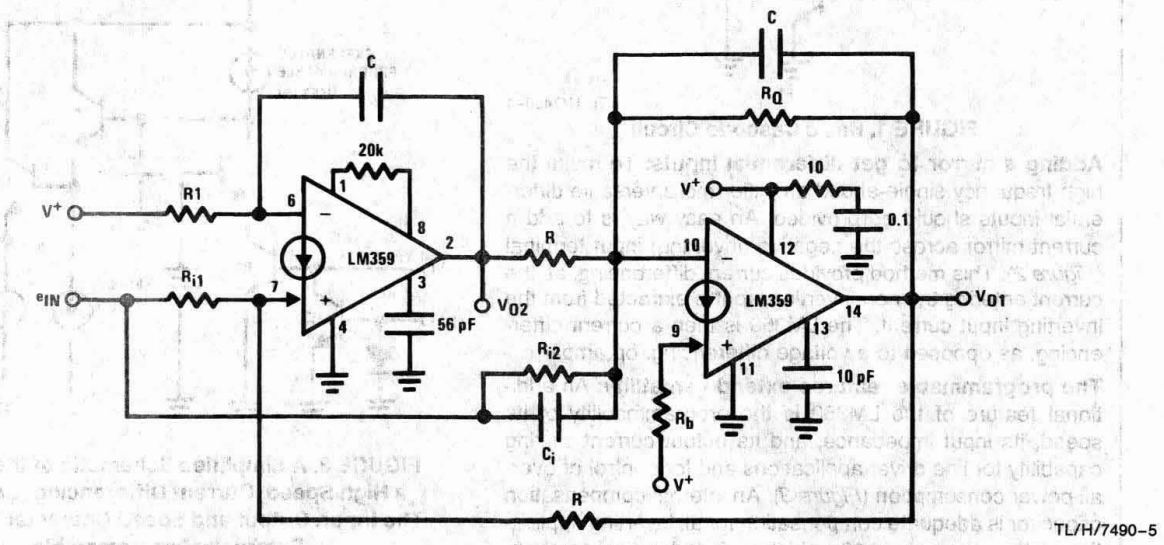

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Table I and Table II relate to *Figure 5*

FIGURE 5. High Performance 2 Amplifier Bi-Quad Filter. Half of the LM359 Acts as a Non-Inverting Integrator and the Other Half Acts as an Inverting One. No Extra Inversion is Necessary to Provide Proper Phase.

The operating range of an active filter can be estimated by comparing its Q_o, center frequency product ($f_o \times Q_o$), with the gain bandwidth product (GBW) of its active elements. The $f_o \times Q_o$ should be less than the active element GBW by a factor of at least 20; a higher factor will yield less sensitive filters. For instance, with a 5 MHz op amp, the $f_o \times Q_o$ product of the filter should not exceed 250 kHz, and in reality should be even less. The filters tested with the LM359 could extend their $f_o \times Q_o$ product up to 2 MHz.

VOLTAGE-CONTROLLED LOW PASS FILTER

A most unique feature of the LM359 is that it provides the user with complete control of its frequency response over a very wide range. The combination of both programmable input stage current and external compensation capability is the key to this flexibility.

One of the most simple, yet illustrative, examples of the usefulness of this capability is the voltage-controlled low pass filter shown in *Figure 6*. The corner frequency of this filter is determined by the closed loop corner frequency of the inverting, gain of 100 amplifier. This frequency is directly controlled by the frequency of the dominant pole of the amplifier's open loop response, which can be approximated by the expression:

$$f_p \cong \frac{3\, I_{SET\ IN}}{2\,\pi\, C_{COMP}\, A_{VOL}\, V_T}$$

where A_{VOL} is the amplifier's DC open loop gain, V_T is equal to KT/q or 0.026V at room temperature, $I_{SET\ IN}$ is the input stage programming current, and C_{COMP} is the total compensation capacitance.

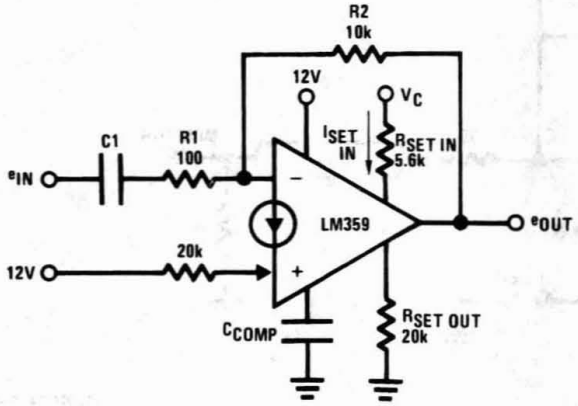

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FIGURE 6. Voltage-Controlled Low Pass Filter. Minimum Input Frequency is Determined by C1 and R1.

The closed loop corner frequency, which, as stated is also the corner frequency of the filter, is:

$$f_c = \beta \bullet GBW = \beta \bullet A_{VOL} \bullet f_p$$

where β is the feedback factor, R1/(R1 + R2), and a single pole open loop frequency response is assumed. Combining these two expressions, the corner frequency is:

$$f_c = \frac{3\, I_{SET\ IN} \bullet \beta}{2\,\pi\, C_{COMP}\, V_T}.$$

The simplest method to dynamically control f_c is to vary $I_{SET\ IN}$ through a control voltage, V_C, where:

$$I_{SET\ IN} = \frac{V_C - V_{BE}}{R_{SET\ IN} + 500\Omega}.$$

In this manner, C_{COMP} should be chosen for the highest desired corner frequency at maximum $I_{SET\ IN}$. Two curves illustrating the dependence of the corner frequency on $I_{SET\ IN}$ for two different compensation capacitors are shown in *Figure 7*.

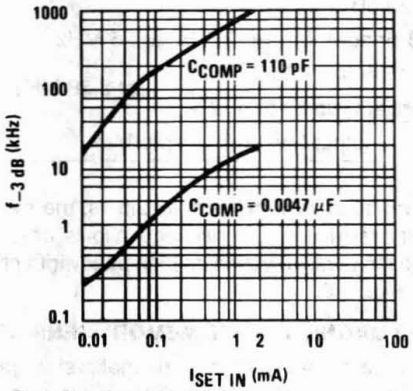

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FIGURE 7. Amplifier Closed Loop Corner Frequency vs $I_{SET\ IN}$

It should be noted that as the compensation capacitor is increased, or $I_{SET\ IN}$ is decreased, the maximum slew rate of the amplifier is decreased. To prevent slew rate induced distortion of sinusoidal input signals, the following restriction applies:

$$\text{Slew rate max} = \frac{3\, I_{SET\ IN}}{C_{COMP}} \geq \omega\, V_o \text{ peak},$$

where V_o peak is the peak output voltage of the filter and ω is $2\,\pi\, f_{IN}$, where f_{IN} is the signal frequency. The output voltage for signal frequencies less than the corner frequency of the filter (within the passband) should then be restricted to:

$$V_o \text{ peak} \leq \frac{V_T}{\beta}.$$

VIDEO AMPLIFIERS

The basic principle behind the design of the LM359 is to provide amplification of high frequency signals with the ease of using standard operational amplifiers. The most obvious application area for this amplifier is in the video area where a fair amount of gain is required at frequencies much higher than monolithic op amps can provide.

A specific application is the amplification or buffering of a composite video signal for a distributed monitor system.

Figure 8 shows a typical connection for a non-inverting video amplifier whose signal source may be either detected video from a receiver, or possibly a camera signal. The output stage of the LM359 can be programmed, as shown, to drive a terminated 75Ω cable to 4 Vp-p for use as a video line driver. For color signals, the differential phase error and differential gain error at 3.58 MHz are desirably low, as noted in Table III.

TABLE III. Typical Video Amplifier Performance

A_V = 20 dB
−3 dB Bandwidth → 2.5 Hz to 25 MHz
Differential Phase Error <1° } at 3.58 MHz
Differential Gain Error < 2% } at 3.58 MHz
Amplifier Output Swing = 4 Vp-p Max

For general purpose wideband amplifiers, the availability of two amplifiers in a single package allows cascading two gain stages to achieve very high gain bandwidth products as shown in *Figure 9*.

DISC AND MAGNETIC TAPE MEMORY SENSING

In digital data recovery from a magnetic storage medium, such as a disc or magnetic tape, there exists a need for high gain bandwidth amplifiers to convert the low level voltage transients from the output of the playback head (caused by a magnetic flux reversal on the tape or disc) to digital pulses that can be processed by data separating or decoding circuitry. The two amplifiers in a single LM359 package can be combined in a variety of ways to provide the basic blocks of a playback channel.

a) For very high bit rates and low level signals they can be cascaded to optimize overall gain bandwidth product, as already shown in *Figure 9*.

b) For single-ended playback signals (non center-tapped head), one amplifier can be used as a gain stage and the other as a differentiating stage to convert recovered signal peaks into bi-directional zero crossing signals, and then properly drive a comparator with regard to direction of flux changes on the disc or tape; this simplifies decoding of phase-encoded data.

c) For differential playback signals (center-tapped head), one amplifier can be used to provide gain for each output signal individually to retain the differential signal, or a single amplifier difference amp can perform a differential to single-ended conversion and the other amplifier can perform differentiation of the single-ended signal. For multichannel, parallel recorded data, the overall component count of the playback system can be minimized by using one amplifier of the LM359 per channel.

Combining gain with constant delay filtering: Another important application of the LM359 in data recovery systems is that of filtering. It is most desirable to prevent high frequency noise spikes from being coupled through the sensing stage causing erroneous readings, but the low

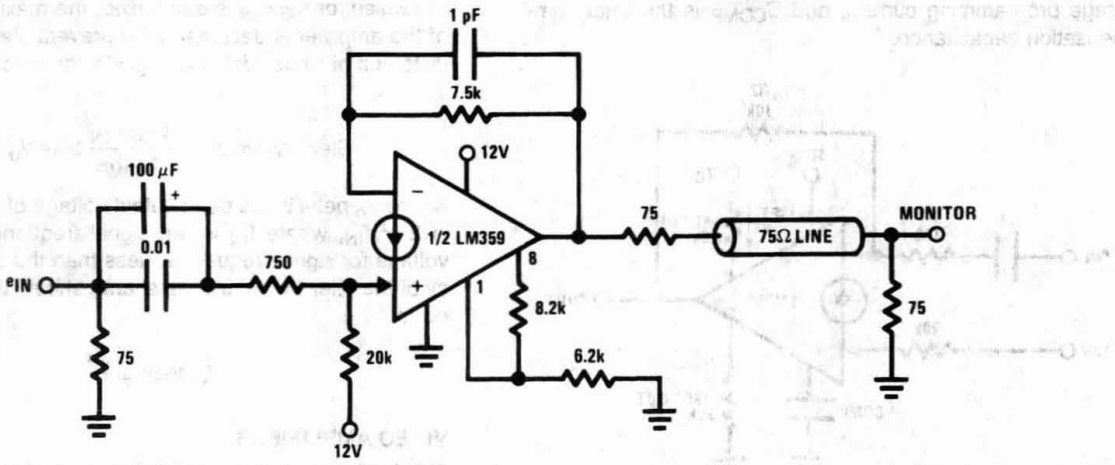

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FIGURE 8. A Typical Application of this Fast Norton Amplifier as a High Perfomance Video Amplifier Driving a 75Ω Line

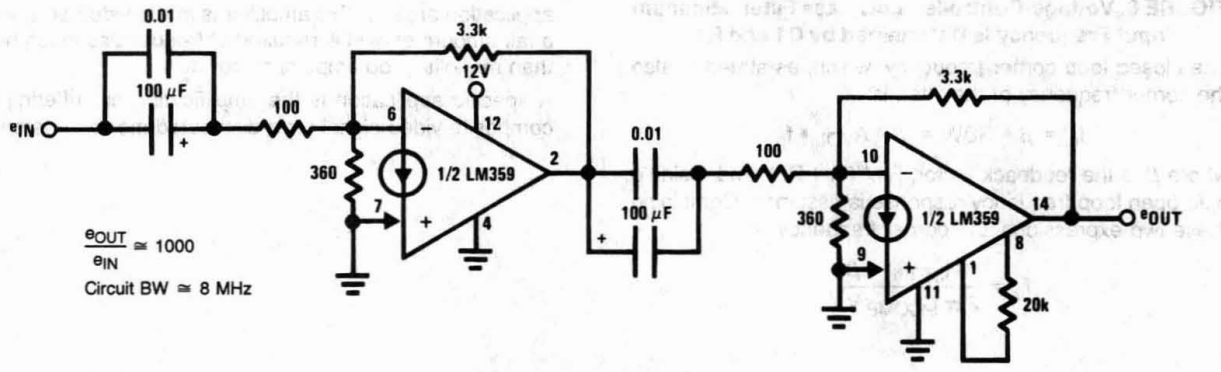

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FIGURE 9. General Purpose, High Gain, Wideband Amplifiers Can Be Obtained by Cascading the 2 Norton Amplifiers Available on a Single Chip

pass filter used must not induce time delays to valid data signals which will be decoded by their time relationship to each other. This immediately implies a constant group delay low pass filter or a Bessel filter approximation which, if implemented with active components, can also provide signal gain. *Figure 10* shows a fourth order, 250 kHz, gain of 100 Bessel filter. Here, because of the low Q_0 requirements of the Bessel filter, a simple (Sallen-Key) filter structure has been chosen over the previously discussed higher performance structures. Note, however, that constant group delay filtering and amplification are performed with a single package.

A HANDLE ON INPUT NOISE

The programmability of the amplifier's input stage current and the ability to "shut off" the non-inverting input current mirror allows significant improvements of the noise characteristics. For an inverting application where the non-inverting input would only be used for DC biasing purposes, an alternate biasing scheme, the nV_{BE} biasing, can be used, as shown in *Figure 11*. This allows "shutting off" the input current mirror which, in itself, will reduce the input noise by a factor of two.

In addition, the input stage programming current can be increased to further reduce the noise voltage at the expense of an increase in input noise current and low frequency 1/f noise, which are not a problem in low input impedance, wideband amplifiers. The typical effect on noise vs input stage current is illustrated in *Figure 12*.

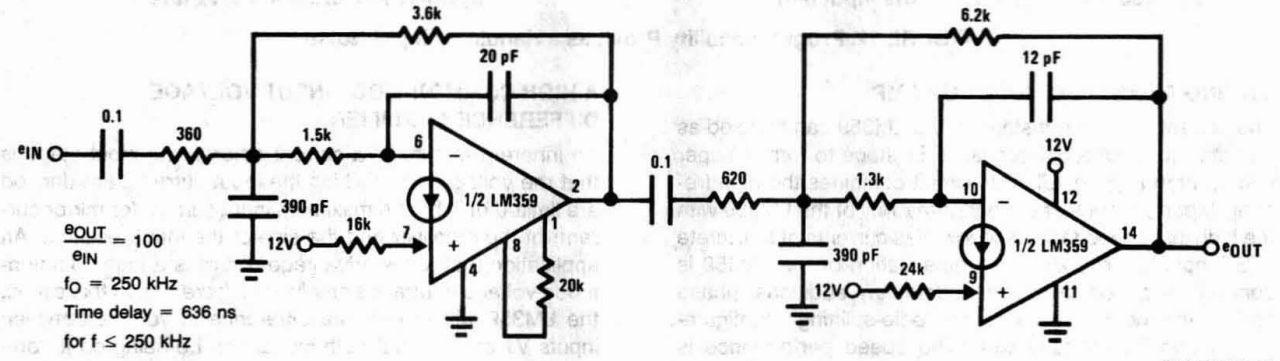

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FIGURE 10. A Fourth Order, 250 kHz Bessel Filter for Data Recovery Systems. The Filtering Function is Done with a Single Package.

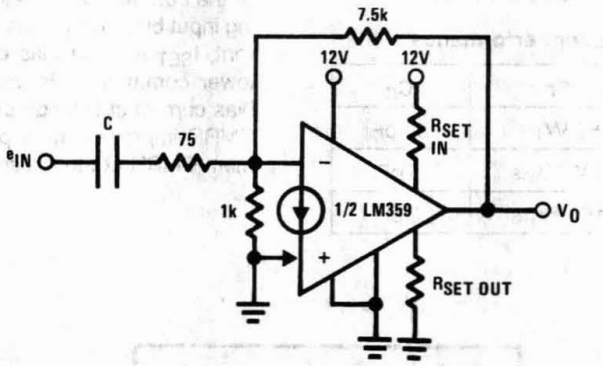

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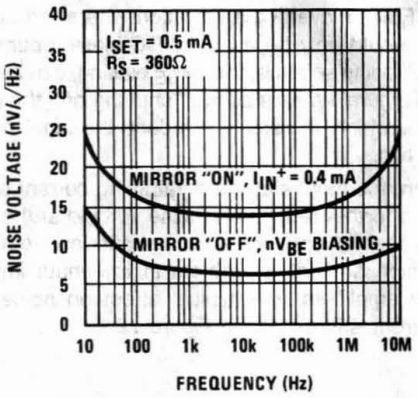
FIGURE 11. nV_{BE} Biasing Can Reduce Input Noise Voltage



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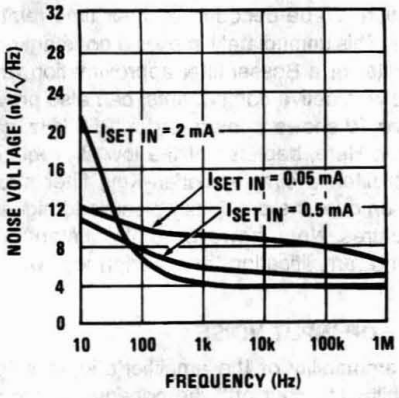
a) Effect of "Shutting Off" the Input Mirror



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b) Noise Performance of *Figure 11*

FIGURE 12. Programmability Provides a Handle on Input Noise

MAKING A FAST JFET INPUT OP AMP

The current mirror input stage of the LM359 can be used as an active load for a differential JFET stage to form a super fast op amp (*Figure 13*). This circuit combines the high frequency performance and programmability of the LM359 with the high input impedance and low bias currents of a discrete JFET input stage. External compensation of the LM359 is generally required to accommodate any additional phase shift of the input stage, and the "pole-splitting" configuration shown works quite well. The speed performance is shown in Table IV. Note that this op amp should be mainly used for very high speed, single supply AC coupled circuits. This is because the op amp DC input offset voltage depends mainly on the matching of 2 discrete JFETs.

TABLE IV. Typical Amplifier Performance

A_V	BW	Sr	C_C
1	40 MHz	60 V/μs	51 pF
10	24 MHz	130 V/μs	5 pF
100	4.5 MHz	150 V/μs	2 pF

A HIGH COMMON-MODE INPUT VOLTAGE DIFFERENCE AMPLIFIER

An inherent feature of a current differencing input stage is that the voltages from which the input currents are derived are limited only by the maximum input current (or mirror current) of the amplifier and the size of the input resistors. An application that takes advantage of this is a high common-mode voltage difference amplifier (*Figure 14*). In this circuit, the LM359 will amplify the difference in voltage between inputs V1 and V2, but both inputs can be riding on a common-mode level as high as approximately 250 V_{DC} without exceeding the maximum mirror current of 10 mA.

The addition of resistor R1 in *Figure14* allows an adjustment of the common-mode rejection ratio by adjusting the inverting input bias current, via the programmable input stage current, $I_{SET\ IN}$. This bias current error is most significant at lower common-mode input voltage levels. By making the bias current directly proportional to the input level, a 20 dB CMRR improvement is possible by adjusting R1 for maximum CMRR at the maximum input common-mode voltage.

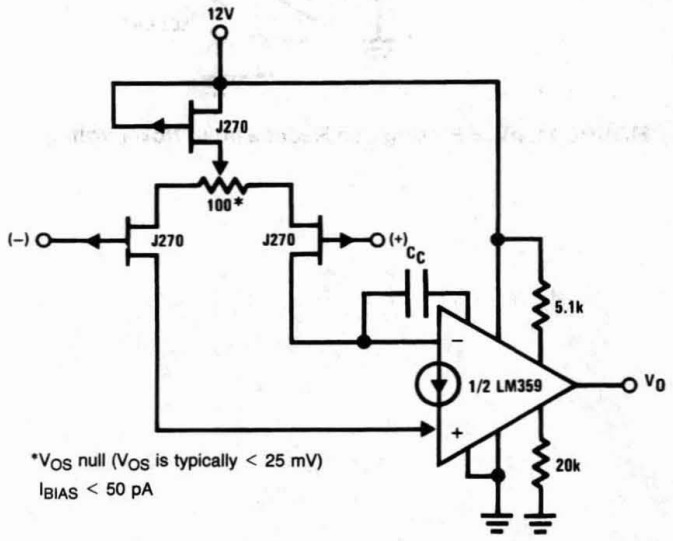

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FIGURE 13. Combining the Norton Amplifier with Discrete P-Channel JFETs to Make a Fast Voltage Mode Op Amp

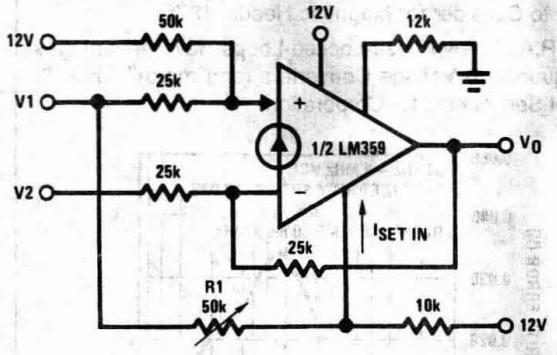

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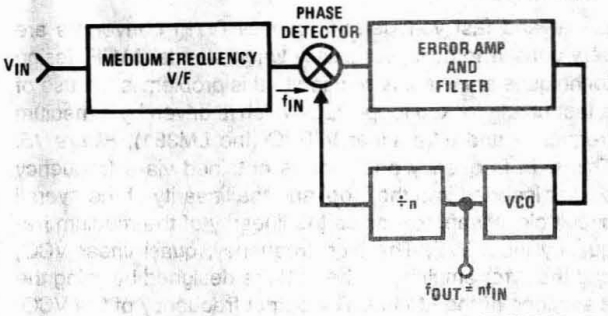
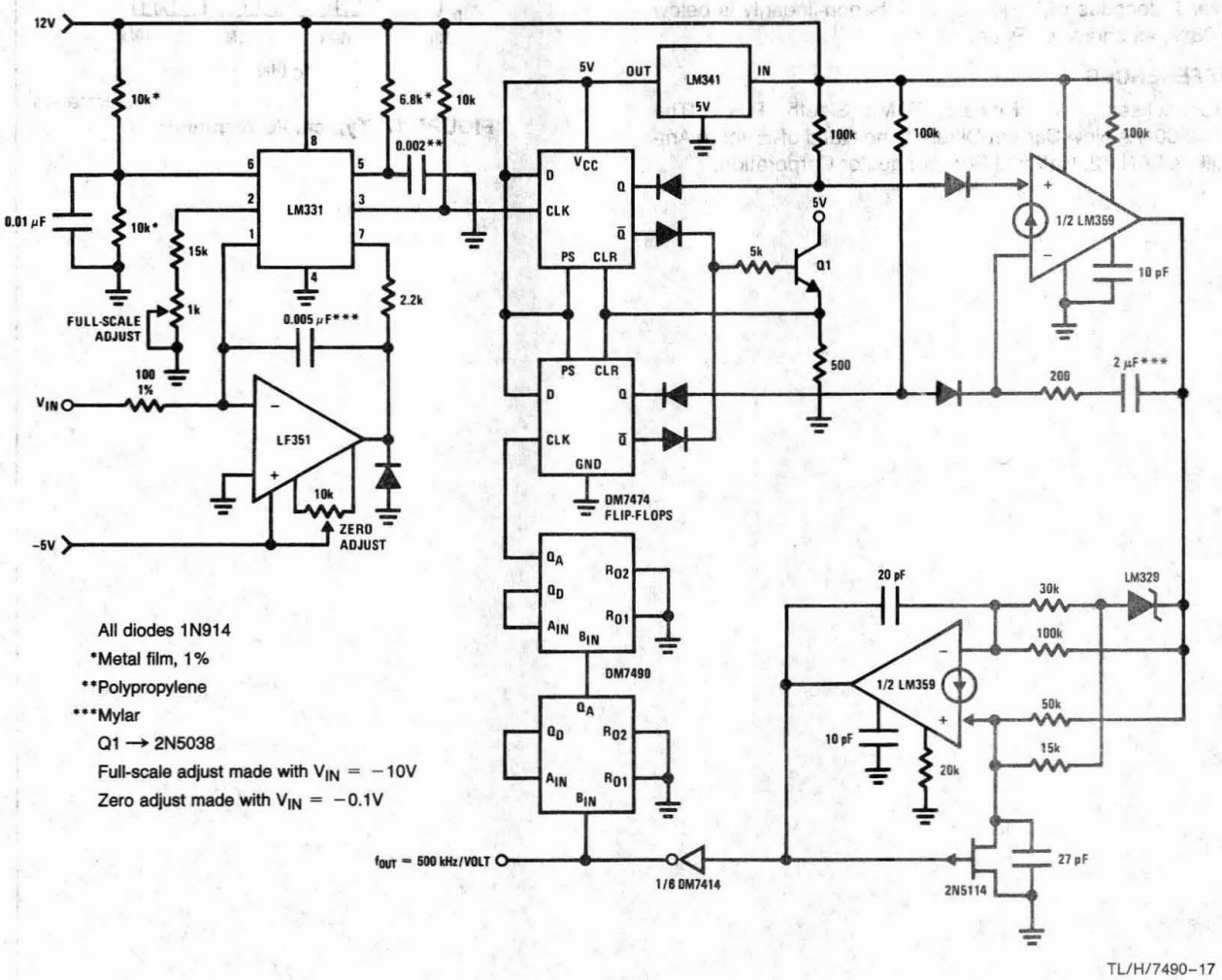
FIGURE 14. A High Input Common-Mode Voltage Difference Amplifier



TL/H/7490–15

FIGURE 15. Using a Fast PLL to Make a High Frequency, Ultra Linear V/F



All diodes 1N914
*Metal film, 1%
**Polypropylene
***Mylar
Q1 → 2N5038
Full-scale adjust made with $V_{IN} = -10V$
Zero adjust made with $V_{IN} = -0.1V$

TL/H/7490–17

FIGURE 16. Complete Schematic of an Ultra Linear, Two Decade (50 kHz → 5 MHz) VCO

BUILDING A FAST AND ULTRA LINEAR V/F CONVERTER

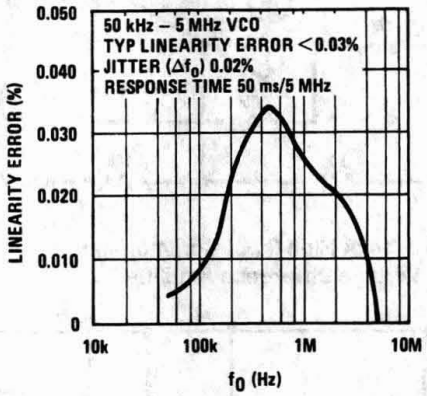
Linear and fast voltage-to-frequency (V/F) converters are very difficult to build, especially when standard V/F design techniques are used. A solution to this problem is the use of a fast phase locked loop (PLL) which is driven by a medium frequency and ultra linear V/F IC (the LM331), *Figure 15*. This high frequency operation is obtained via a frequency divider inserted into the loop, and the linearity of the overall circuit closely approximates the linearity of the medium frequency input V/F. The high frequency, quasi linear VCO, and the error amplifier of the PLL are designed by using the 2 sections of the LM359. The output frequency of the VCO, which is also the output of the system, is divided by 100 and is compared with the output of the driving V/F via a digital phase detector. The overall circuit is shown in *Figure 16*. Following a zero and a full-scale adjust, the V/F works well over 2 decades of frequency and its non-linearity is below 0.03%, as shown in *Figure 17*.

REFERENCES

Fredericksen, T.M.; Howard, W.M.; Sleeth, R.S., "The LM3900—A New Current-Differencing Quad of ± Input Amplifiers" AN-72, National Semiconductor Corporation.

Nortronics Design Digest on Digital Recording, Application Factors to Consider for Magnetic Heads, 1976.

Pease, R.A., "New Phase-Locked-Loops Have Advantages as Frequency to Voltage Converters (and more)" AN-210, National Semiconductor Corporation.



TL/H/7490–16

FIGURE 17. Typical Performance

A/D Converters Easily Interface with 70 Series Microprocessors

National Semiconductor
Application Note 280

Abstract: *This application note describes techniques for interfacing parallel I/O and serial I/O 8-bit A/D converters to the INS8070 series of microprocessors. A detailed hardware and software interface example is provided for each type of A/D.*

As examples, the INS8073 is used to interface with the parallel I/O ADC0804, and the INS8072 is used with the serial I/O ADC0833.

INTRODUCTION

The INS8070 series of microprocessors is designed for compact, low cost control, data acquisition, and processing applications. Up to 2.5k-bytes of ROM and 64 bytes of RAM are available on-chip. The INS8073 is a programmed version of the INS8072 with a Tiny Basic microinterpreter on-chip. The microinterpreter executes source code directly, thus avoiding the need to translate the source code into machine language. This approach allows users to develop system software without using a development system and gives a greater flexibility for design changes.

The ADC0801 series, the ADC0808 series, and the ADC0816 series are CMOS 8-bit successive approximation A/D converters that include TRI-STATE® latched outputs and control logic for parallel I/O. These A/Ds can be mapped into memory space or they can be controlled as I/O devices. The ADC0801 series includes a differential input and span adjust pin, while the ADC0808 and ADC0816 series include an 8- or 16-channel multiplexer with latched control logic.

The ADC0831 series, on the other hand, are CMOS 8-bit successive approximation A/D converters with serial I/O. In addition to the single analog input ADC0831 in an 8-pin miniDIP, they offer 8, 4, or 2-channel analog multiplexed inputs. Serial output data can be selected as either MSB or LSB first. The channel assignment of the multiplexers is accomplished with a 4-bit serial input word preceded by a leading "1" start bit.

The ADC0801, ADC0802, ADC0803, ADC0804 parallel I/O A/Ds and the ADC0833 serial I/O A/D are designed to work with a 2.5V fixed reference for a 0V to 5V analog input range. The full 8 bits of resolution can be encoded over any smaller analog voltage range by applying one half of the desired full-scale analog input voltage value to the $V_{REF}/2$ pin.

The ADC0805, ADC0808, ADC0809, ADC0816, ADC0817 parallel I/O A/D converters and the ADC0831, ADC0832, ADC0834, and ADC0838 serial I/O A/D converters are designed to operate ratiometrically with the system transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full-scale value. The actual value of the transducer's output is not important, but the ratio of this output to the full-scale reference is important. Also, these parts are designed to use a 5V fixed reference.

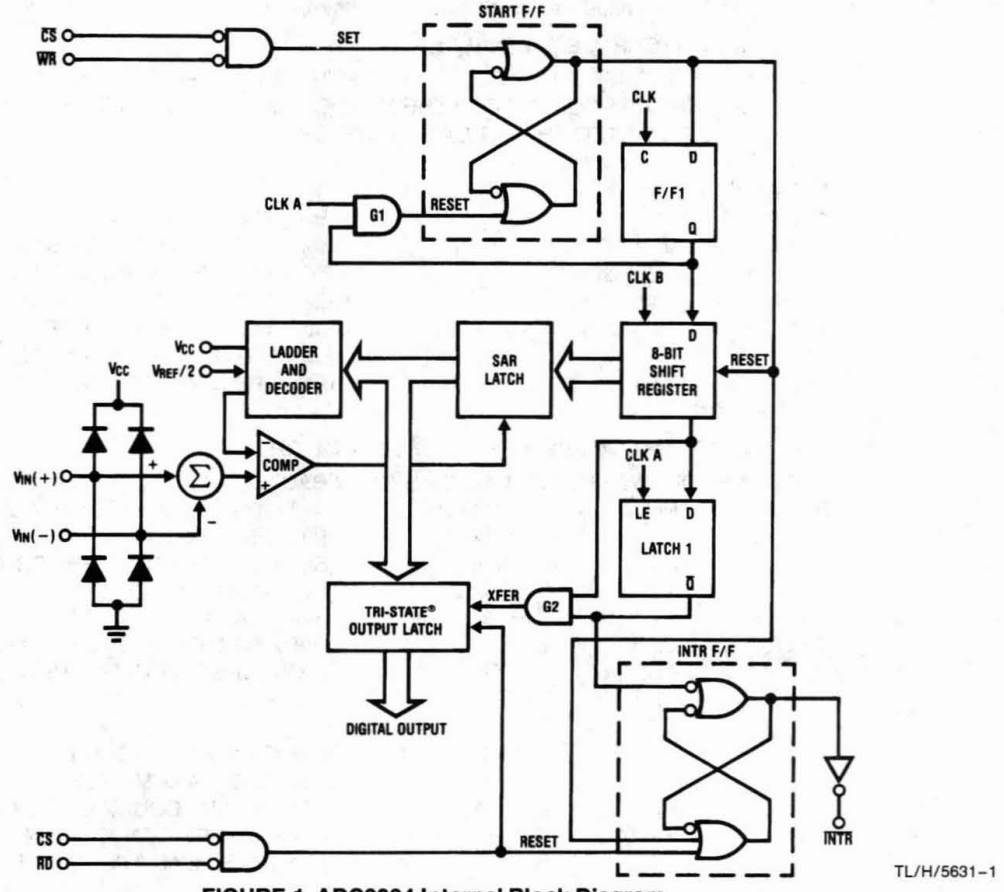


FIGURE 1. ADC0804 Internal Block Diagram

All of these A/D converters operate from a standard 5V power supply, and are available in accuracies over the temperature range of ±½ LSB or ±1 LSB including full-scale, zero scale, and non-linearity errors.

ADC0804 IMPLEMENTATION EXAMPLE

Theory of Operation

The converter is started by forcing $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) (see *Figure 1*) which resets the 8-bit shift register, resets the INTR F/F and sets F/F1, which is at the input end of the 8-bit shift register. When the set signal of the start F/F goes low (either $\overline{WR}$ or $\overline{CS}$ is high), the 8-bit shift register then shifts in a "1" from F/F1, which starts the conversion process. After the "1" is clocked through the 8-bit shift register, it appears as the input to Latch 1. The "1" output from the shift register causes the 8-bit output of the SAR latch to transfer to the TRI-STATE output latches. When Latch 1 is subsequently enabled, the Q output makes a high-to-low transition which sets the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal. When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will reset the INTR F/F and will enable the TRI-STATE buffer latch output onto the 8-bit data bus.

1k-byte of external RAM is provided in the INS8073 system, in which the first 256 bytes are used to store the microinterpreter's variables, stacks and buffers. The remainder of the RAM is used to store data and the interface program. The A/D is mapped into the memory space of the INS8073 system at address 3000 HEX. External RAMs are located from 1000 HEX to 13FF HEX. A DM74LS138 address decoder is used to generate the chip select signals for the A/D and the RAM. It also provides a signal to enable a DM74LS368 TRI-STATE HEX buffer which provides the baud rate setting at location FD00 HEX. The read and write strobe signals of the A/D and the processor are tied together, and the $\overline{INTR}$ signal of the A/D is tied to the SENSE B input of the INS8073.

The microinterpreter has built-in I/O routines to serially interface with an RS-232 terminal. The INS8073 F1 flag should be inverted and buffered to provide an RS-232 level. Similarly, the INS8073 will accept serial input data, buffered to TTL level without inversion, on its SA input. DS1488/DS1489 quad line driver/receiver chips are used for TTL/RS-232 buffering. Baud rate can be selected by matching the two jumpers, J1 and J2, (see *Figure 2*), with the table below. A "0" signifies that the jumper is missing, and a "1" means that it is installed.

J1	J2	Baud Rate
0	0	4800
0	1	1200
1	0	300
1	1	110

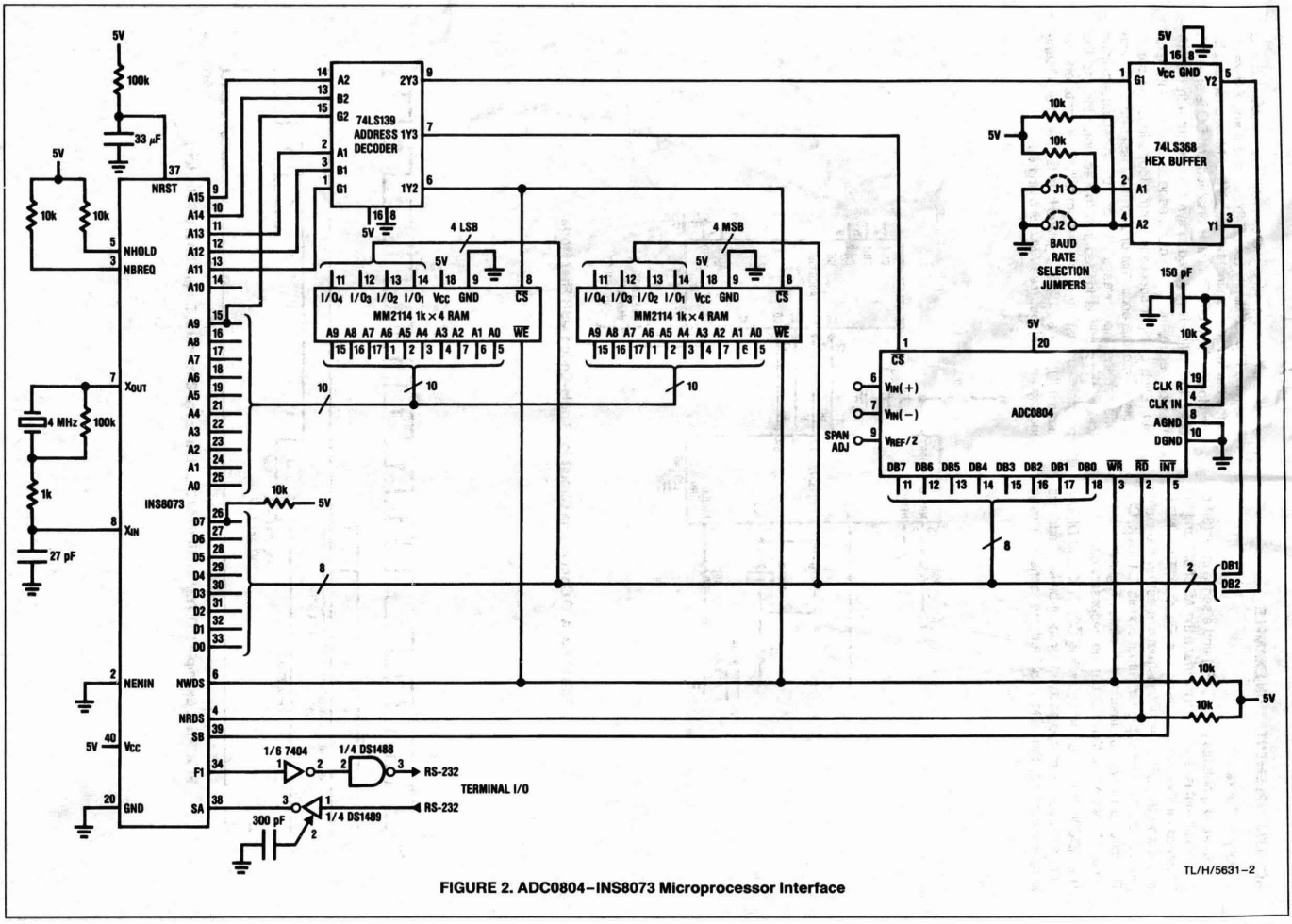
Details of both hardware and software interface are given below and in *Figure 2*. A Tiny Basic subroutine, along with an Assembly Language subroutine, are illustrated. The microprocessor starts the A/D, reads, and stores the results of 16 successive conversions. The 16 data bytes are stored at location 13D0 HEX to 13DF HEX. The Assembly Language subroutine can be called by issuing a "LINK" statement in Tiny Basic. It performs the same function as the Tiny Basic subroutine, except it will execute faster. The Tiny Basic subroutine takes about 60 ms to execute; the Assembly Language subroutine takes only 96 μs (plus conversion time).

TINY BASIC INTERFACE SUBROUTINE

```
100 REM   SUBROUTINE TO START A/D AND STORE DATA INTO MEMORY
110 REM   C IS THE COUNTER FOR THE NUMBER OF DATA BYTES STORED
120 REM   D POINTS TO THE 1ST DATA ADDRESS
130 C=16
140 D=#13D0
150 @ #3000=A                          :REM  START A/D
160 A=STAT AND #20                     :REM  LOOP UNTIL SENSE B GOES LOW
170 IF A<>0 THEN GO TO 160             :REM  (CONVERSION COMPLETED)
180 @ D=@ #3000                        :REM  INPUT CONVERTED DATA
190 D=D+1                              :REM  INCREMENT DT ADDRESS
200 C=C-1                              :REM  CHECK WHETHER 16 CONVERSIONS
210 IF C>0 THEN GO TO 150              :REM  ARE DONE OR NOT
220 RETURN
```

INS8072 ASSEMBLY CODE INTERFACE SUBROUTINE

```
; THIS SUBROUTINE IS TO BE CALLED BY TINY BASIC THROUGH A "LINK" STATEMENT
BEGIN:   PLI    P2,=13DOH      ;P2 POINTS TO A 1ST BYTE ADDRESS
         PLI    P3,=3000H      ;P3 POINTS TO A/D
         LD     A,=0FH         ;SET CONVERSION COUNTER TO 15
         ST     A, COUNT       ;COUNTER ADDRESS
START:   ST     A, 0, P3       ;START A/D
WAIT:    LD     A, S           ;WAIT FOR SENSE B INPUT TO GO LOW
         AND    A,=20H         ;(CONVERSION COMPLETED)
         BNZ    WAIT
         NOP
         LD     A, 0, P3       ;INPUT CONVERTED DATA
         ST     @ 1, P2        ;STORE DATA IN MEMORY
         DLD    A, COUNT       ;DECREMENT COUNTER. IF NOT DONE,
         BP     START          ;DO ANOTHER CONVERSION
         POP    P3             ;RESTORE P2 AND P3 FOR TINY BASIC
         POP    P2
         RET                   ;RETURN TO TINY BASIC
```



TL/H/5631–2

FIGURE 2. ADC0804–INS8073 Microprocessor Interface

ADC0833 IMPLEMENTATION EXAMPLE

Theory of Operation

The three flag outputs (F1, F2, F3) and a sense input (SA or SB) are all that is required to interface the ADC0833 and the 70 series family microprocessor (see *Figure 3*). The AND S, = XX and the OR S, = XX instructions set up the status register to produce the proper output signals (D1, CLK, $\overline{CS}$). The input is derived by loading the status register into the accumulator and masking all but the necessary bit.

The ADC0833 is selected by setting $\overline{CS}$, CLK, and DI low. After setting a counter to account for the 4-bit MUX address and the start bit, the data is shifted out, serially. This is accomplished by testing the carry bit after each shift and modifying FI accordingly (see Tables I and II and *Figure 4*). Once the leading sentinel bit and all four MUX address bits are clocked in, the A/D input is disabled and DO is enabled. One clock pulse is required to sync the output with the falling clock edge; the falling clock edge is used to clock data out. Each of eight successive input loops load the status register into the accumulator and the masks to determine whether the input was a "1" or "0". After ascertaining which, the result is loaded into the accumulator and the program successively shifts left (for a "0"), or shifts left and adds a "1" (for a "1"). A digitized byte is formed representing the analog input (see *Figures 5* and *6*).

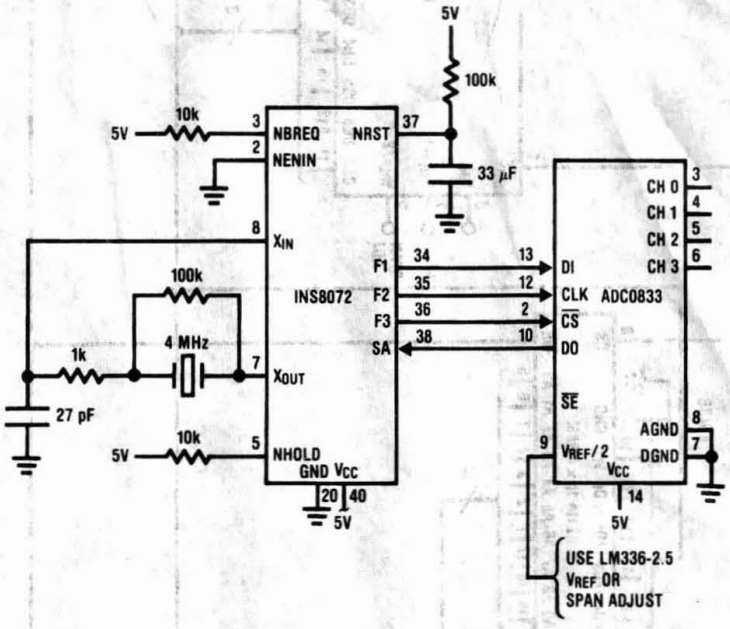
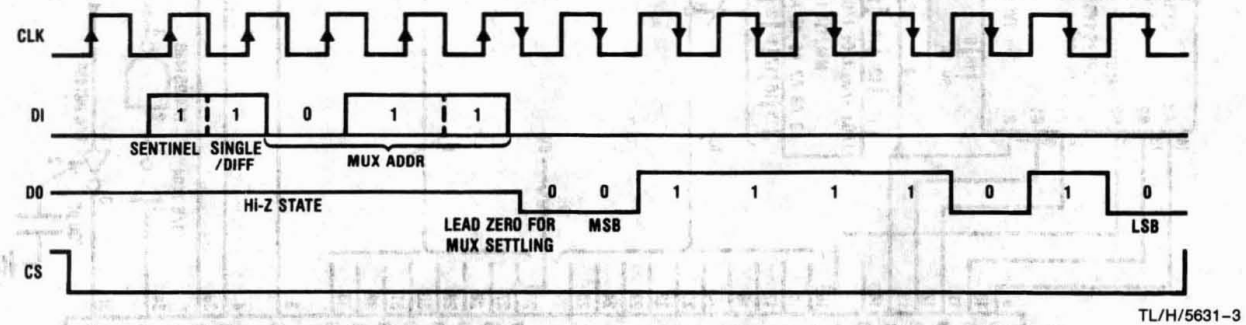


FIGURE 3. A/D Conversion Circuit for Single-Ended MSB First Mode



TL/H/5631–3

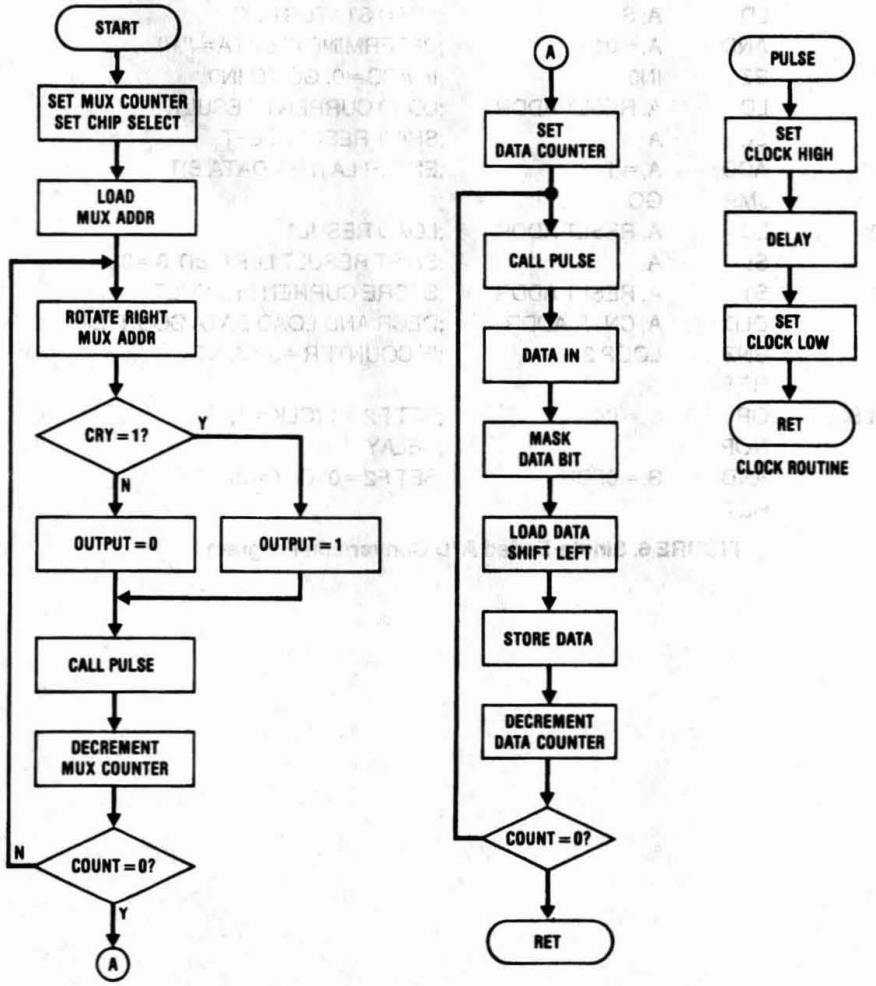
FIGURE 4. Example I/O Transaction (A/D Output = 7A; Channel 2, Single-Ended Selected)

TABLE I. SINGLE-ENDED MUX MODE

LSB		MSB	S/D	Start	Single-Ended 0	1	2	3	HEX Code
1	0	0	1	1	+				13
1	1	0	1	1			+		1B
1	0	1	1	1		+			17
1	1	1	1	1				+	1F

TABLE II. DIFFERENTIAL MUX MODE

LSB		MSB	S/D	Start	Differential 0	1	2	3	HEX Code
1	0	0	0	1	+	−			11
1	1	0	0	1			+	−	19
1	0	1	0	1	−	+			15
1	1	1	0	1			−	+	1D



TL/H/5631–4

FIGURE 5. A/D Conversion Flow Chart

```
START:  AND   S, = 0F0H      ;SET CS = 0, CLK = 0
        LD    A, = 5
        ST    A, CNTR ADDR   ;SET UP MUX ADDR COUNTER
        LD    A, = 0
        ST    A, RESLT ADDR  ;CLEARS RESULT LOCATION
        LD    A, = MUX ADDR  ;LOAD MUX ADDR AND SENTINEL BIT
        JMP   LOOPS
LOOP 1: XCH   A, E           ;RESTORE MUX ADDR REMAINDER
LOOP 5: RRL   A              ;ROTATE BIT 0 INTO CARRY
        XCH   A, E           ;SAVE MUX ADDR REMAINDER
        LD    A, S           ;LOAD STATUS REG
        BP    ZERO           ;IF CARRY NOT SET, OUTPUT = "0"
ONE:    OR    S, = 02        ;SET F1 = 1 (D1 = 1)
        JMP   CONT
ZERO:   AND   S, = 0F0H      ;SET F1 = 0 (DI = 0)
CONT:   CALL  PULSE          ;PULSE CLK 0 → 1 → 0
        DLD   A1 CNTR ADDR   ;DECR AND LOAD COUNTER
        BNZ   LOOP 1         ;BRANCH IF COUNT = 0
        LD    A, = 08        ;SET UP DATA BIT COUNTER
LOOP 2: CALL  PULSE          ;PULSE CLOCK 0 → 1 → 0
        LD    A, S           ;LOAD STATUS REG
        AND   A, = 01        ;DETERMINE IF DATA = "1"
        BZ    IN0            ;IF ACC = 0, GO TO IN0
        LD    A, RESLT ADDR  ;LOAD CURRENT RESULT
        SL    A              ;SHIFT RESULT LEFT
        ADD   A, = 1         ;ENTER LATEST DATA BIT
        JMP   GO             ;
IN0:    LD    A, RESLT ADDR  ;LOAD RESULT
        SL    A              ;SHIFT RESULT LEFT, BIT 0 = 0
GO:     ST    A, RESLT ADDR  ;STORE CURRENT RESULT
        DLD   A, CNTR ADDR   ;DECR AND LOAD DATA COUNTER
        BNZ   LOOP 2         ;IF COUNTER ≠ 0, CONT
        RET
PULSE:  OR    S, = 04        ;SET F2 = 1 (CLK = 1)
        NOP                  ;DELAY
        AND   S, = 0FBH      ;SET F2 = 0 (CLK = 0)
        RET
```

FIGURE 6. Single-Ended A/D Conversion Program

Data Acquisition Using INS8048

National Semiconductor
Application Note 281
Daniel Hagerty

Abstract: *This application note describes techniques for interfacing National Semiconductor's ADC0833 serial I/O, and ADC0804 parallel I/O A/D converters to the INS8048 family of microprocessors. A hardware and software interface example is provided for each A/D, along with a brief theory of operation.*

INTRODUCTION

Since the INS8048 series microprocessors are single-chip, multiple I/O line, high speed devices designed as efficient controllers, the capacity to interface with analog peripherals is obvious. That the conversion be fast, inexpensive and easily expanded to accommodate a number of I/O devices is desirable.

The INS8048 is a self-contained, 8-bit processor in a 40-pin dual-in-line package. It contains its own system timing, control logic and memory. All parts contain RAM (64, 128, 256 bytes) and offer the option of on-board ROM (1k, 2k, 4k depending on part). It provides extensive bit-handling capabilities, 97 instructions, and offers easy expansion for I/O and memory.

The ADC0833 A/D converter is an 8-bit successive-approximation device with serial I/O and conversion time of 25 μs. This family of converters offers various configurations of multiplexed analog inputs which can be software programmed as single-ended, or as differential inputs, or both. Single-ended inputs are referenced to a common pin which is either referred to analog ground or to a fixed reference voltage. Like the INS8048 family, a single 5V power supply is all that is needed. The inputs will accept a 0V-5V range. No zero adjust is necessary. It is compatible with TTL and MOS at both input and output. The output can be selected as either MSB or LSB first.

The ADC0804 is a CMOS 8-bit successive-approximation A/D converter with parallel I/O. This A/D can be mapped into memory space or can be controlled as an I/O device. No external logic is needed to interface with the INS8048. A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding smaller voltage spans to the full 8 bits of resolution.

ADC0833 IMPLEMENTATION

Before explaining the system configuration, it is worthwhile for one to understand the operation of the INS8048 processor's I/O ports. Ports 1 and 2 are quasi-bidirectional; that is, they can be used as inputs or outputs while being statically latched. If a "1" is written into any port bit, that bit can function as an input or as a high level output. If a "0" is written into any port bit, that bit can function only as a low level output. Outputs are latched until changed and inputs are unlatched and must be read immediately. When used with the ANL Pp,A (AND accumulator to port) or the ORL Pp,A (OR accumulator to port) instructions, these ports provide an efficient means of handling single line inputs and outputs. Port expansion, if anticipated, is handled via the lower four bits of Port 2. These four bits fulfill three distinct functions:

(1) A quasi-bidirectional static port

(2) The four high order address bits for external memory

(3) An expander port interface

Only four pins of the processor's Port 1 or Port 2 are needed for physical interfacing (see *Figure 1*). The ANL or ORL instructions set up the port pins to produce the proper outputs (CS, CLK, and the multiplex address) or to allow for data input from the A/D converter.

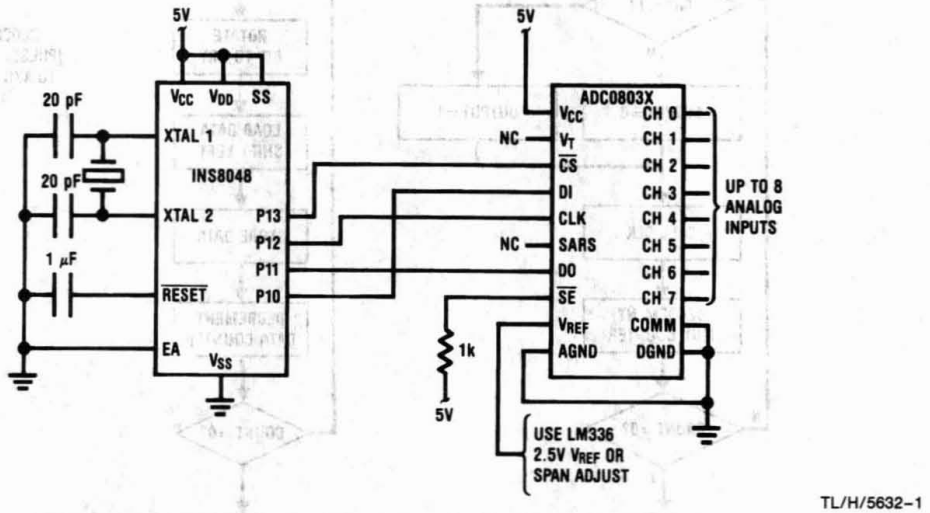


FIGURE 1. A/D Conversion Circuit for Single-Ended MSB First Mode

The following description of the program can be used with the listing or flow chart to understand the procedure. To begin conversion, the processor must drive CS low, resetting the multiplex address shift register, the successive-approximation register and the 9-bit shift register. After the A/D converter has been selected, the multiplexer address is shifted out serially to the converter. The 4-bit multiplexer address is always preceded by a start bit, a "1". The program loads the multiplexer address, start bit and mode bit into the accumulator as a single byte which is processed and shifted out to the converter. By shifting this byte into the carry, each bit is tested and the appropriate "1" or "0" is output to the port. After five such operations, the start bit is shifted on the rising edge of the clock pulse through the A/D's 5-bit shift register (see *Figures 2* and *3*, Tables 1 and 2). At this point, the digital data input is disabled, and the digital data output enabled. One more clock pulse is needed to synchronize the output on the falling edge of the clock pulse. On each successive clock pulse, data is shifted serially to the processor. The data bits are then shifted, upon reception, into the accumulator to form the digitized analog input.

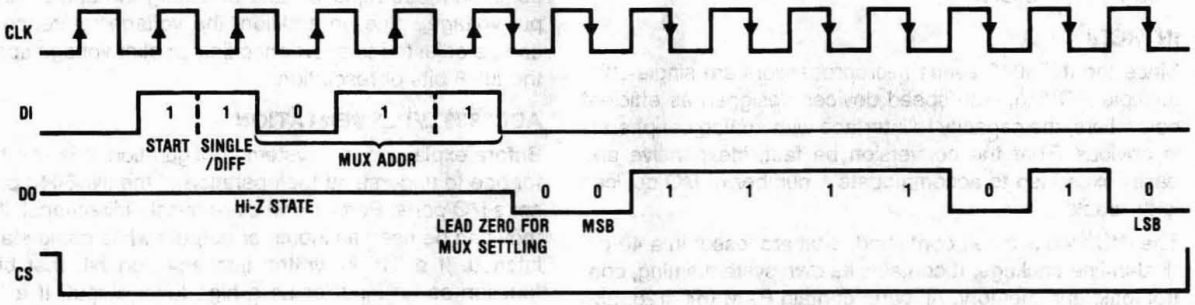
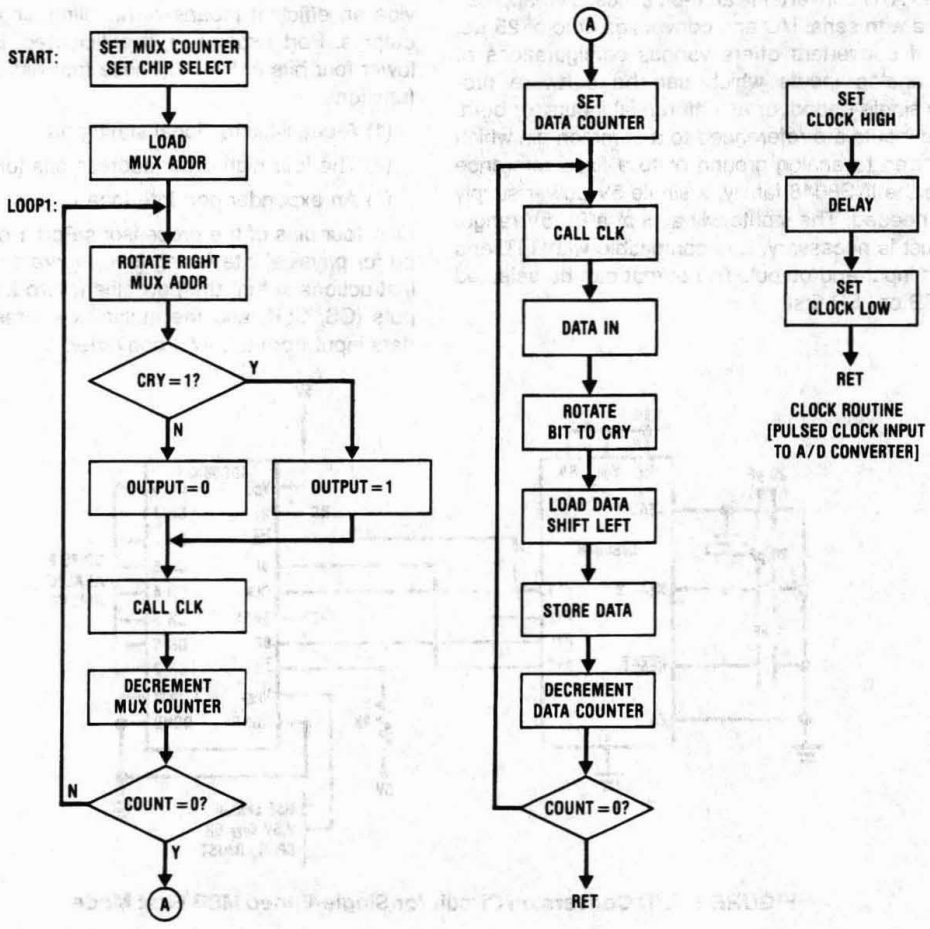


FIGURE 2. Example I/O Transaction (A/D Output = 7A; Channel 2, Single-Ended Selected)



TL/H/5632-2

FIGURE 3. A/D Conversion Flow Chart

TABLE I. Single-Ended Mux Mode

LSB		MSB	S/D	Start	Single-Ended 0	1	2	3	HEX Code
1	0	0	1	1	+				13
1	1	0	1	1			+		1B
1	0	1	1	1		+			17
1	1	1	1	1				+	1F

TABLE II. Differential Mux Mode

LSB		MSB	S/D	Start	Differential 0	1	2	3	HEX Code
1	0	0	0	1	+	−			11
1	1	0	0	1			+	−	19
1	0	1	0	1	−	+			15
1	1	1	0	1			−	+	1D

```
START:    ANL     P1, #0F3H       ;SELECT A/D, SET CS0 to 0
          MOV     R2 #5           ;BIT COUNTER ← 5
          MOV     A, #DATA        ;A ← MUX ADDR
          MOV     R3, #0          ;CLEAR R3
LOOP 1:   RRC     A               ;CY ← ADDR BIT
          JC      ONE             ;IF CY = 1 GO TO ONE
ZERO:     ANL     P1, #0FEH       ;SET DI = 0
          JMP     CONT            ;CONTINUE IF 0
ONE:      ORL     P1, #1          ;SET DI = 1
CONT:     CALL    PULSE           ;PULSE CLK 0 → 1 → 0, CLK IN DATA
          DJNZ    R2, LOOP 1      ;LOOP, TO SHIFT AND OUTPUT MUX
                                  ;ADDR AND SENTINEL
          MOV     R2, #8          ;BIT COUNTER ← 8, FOR SERIAL IN
LOOP2:    CALL    PULSE           ;PULSE CLK 0 → 1 → 0
          IN      A, P1           ;A ← (D0), BIT SHIFTED TO CARRY
          RRC     A
          RRC     A
          MOV     A, R3           ;A ← RESULT
          RLC     A               ;A(0) ← CY, SHIFT LEFT
          MOV     R3, A           ;R1 ← RESULT
          DJNZ    R2, LOOP 2      ;LOOP THRU FOR ALL 8 BITS
          RETR
PULSE:    ORL     P1, #04         ;CLK ← 1
          NOP                     ;DELAY
          ANL     P1, #0FBH       ;CLK ← 0
          RET
          END     START
```

FIGURE 4. Single-Ended A/D Conversion Routine

Easy expansion, mentioned earlier, has not been forgotten. With the addition of the one chip (see *Figure 5*), the number of peripherals can be expanded TEN-FOLD! The INS8243 I/O expander consists of five 4-bit bidirectional ports. One port provides the interface with the processor, the other four provide the I/O expansion. The INS8243 I/O expander serves as a direct extension for the resident I/O port of the INS8048 family of processors. The INS8048 instruction set provides four instructions solely for use with this chip. They are:

MOVD Pp,A—Shift accumulator data to addressed port

MOVD A,Pp—Shift addressed port data to accumulator

ANLD Pp,A—ANDing accumulator data to addressed port

ORLD Pp,A—ORing accumulator data to addressed port

The last two instructions can be used in the same way as the ANL and ORL instructions in the first example. It should be noted that only one pin can be used in Port 7, since the INS8243, unlike the INS8048 series, has true bidirectional ports and thus requires that each port be either input or output. *Figure 5* shows how 10 A/D converters could be connected to allow up to 80 analog inputs to be monitored at the expense of only four I/O pins on the INS8048 itself.

ADC0804 IMPLEMENTATION

The ADC0801/2/3/4/5 A/D converters have been designed to directly interface with processors similar to the INS8048 family. The A/D is memory mapped into the external data memory space of the INS8048 system. The RD, WR and INTR signals of the A/D, and the processor are tied directly. In the example circuit, an arbitrarily chosen address, E0, is assigned to the A/D, and CS is decoded by a bus comparator, the DM8131. Since the address and the data of the INS8048 processor are multiplexed on the same bus, an inverted ALE signal from the INS8048 is tied to the strobed input of the bus comparator in order to latch the address output from the processor. If no other devices are attached to the INS8048's bus, this decoding can be left off and the CS input to the ADC0804 is simply grounded.

A sample program is shown in *Figure 6*. The processor starts the A/D, reads and stores the result of an analog-to-digital conversion through an interrupt service routine. This subroutine starts at address 30H, and the external interrupt vector is located at address 03H. The converted data word is stored at on-chip RAM location, 10H. The following is a line by line description of the parallel A/D conversion subroutine.

BEGIN: This is where the program starts execution after having been reset. R0 and R1 are set up with addresses to point to the A/D converter and the address where data is to be stored.

AGAIN: Interrupts are enabled to allow the A/D to signal that it has completed its conversion; arbitrary data is written to the device to start its conversion process.

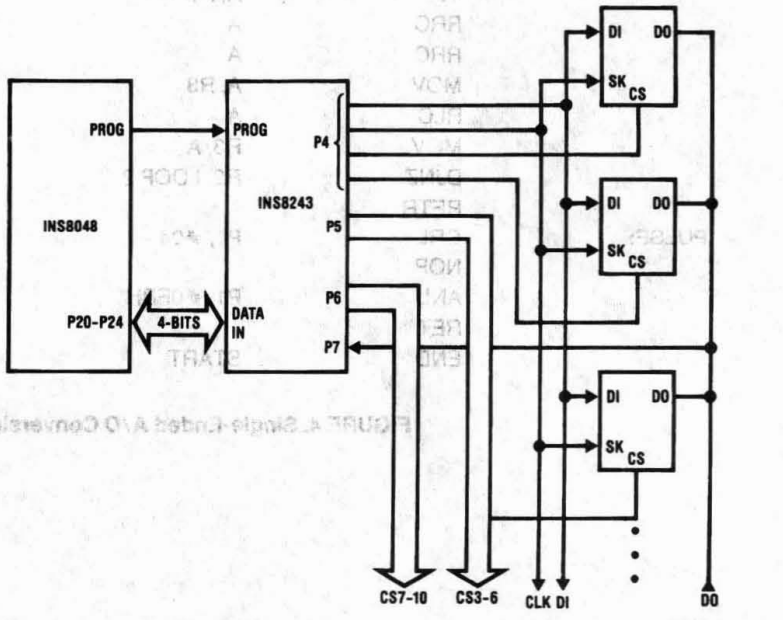
LOOP: The processor waits here for an interrupt to occur. The interrupt service routine returns with a zero in the accumulator to allow the program to continue at CONT.

CONT: This is where the analog input received earlier is processed.

INDATA: Upon the occurrence of an interrupt, this routine is entered. It reads data from the A/D converter (with a MOVX A,@R0) and puts it into the RAM location pointed to by R1 (MOV @R1, A). The accumulator is cleared in order to pass location LOOP:, (see *Figure 6*) and control is returned to the user's program.

Upon inspection, it can be seen that each system has its strengths and limitations. Because of the need to handle serial data with loops for input and output, the ADC0833 is approximately five times slower than the ADC0804. Therefore, for raw speed, the ADC0804, at 100 μs conversion time plus minimal processor service time, is preferable. Faster processors can be used to decrease the response time from any given analog input. All INS8048 series devices are available with clock rates up to 11 MHz. Though slower, the ADC0833 provides up to eight multiplexed inputs configurable in single-ended or differential modes, and uses only four processor I/O pins. In either case, the implementation is not formidable and, with only 2 or 3 chips per system, not expensive.

Expander	Outputs
Port 4	DI
	SK
	$\overline{CS}1$
	$\overline{CS}2$
Port 5	$\overline{CS}3$
	$\overline{CS}4$
	$\overline{CS}5$
	$\overline{CS}6$
Port 6	$\overline{CS}7$
	$\overline{CS}8$
	$\overline{CS}9$
	$\overline{CS}10$
Port 7	D0



TL/H/5632–3

FIGURE 5. I/O Expansion

```
                    ;TEST ROUTINE FOR INTERFACING INS8048 WITH ADC0804
                    ;PROGRAM STARTS AT MEMORY LOCATION 10H
                    ;INTERRUPT SUBROUTINE STARTS AT LOCATION 30H
                    ;DATA WILL BE STORED IN MEMORY LOCATION AT 20H
                    ;
ADDRESS   OBJECT CODE
                              ORG     0H
0000      04 10               JMP     10H       ;PROGRAM STARTS AT 10H
                              ORG     3H        ;INTERRUPT VECTOR
0003      04 30               JMP     30H
                              ORG     10H       ;MAIN PROGRAM
0010      B8 E0     BEGIN:    MOV     R0, #0E0H ;R0 POINTS TO A/D
0012      B9 20               MOV     R1, #20H  ;R1 POINTS TO DATA ADDRESS
0014      05        AGAIN:    EN I
0015      23 FF               MOV     A, #0FFH  ;SET THE ACC FOR INTR LOOP
0017      90                  MOVX    @R0, A    ;START A/D
0018      96 18     LOOP:     JNZ     LOOP      ;LOOP UNTIL INTR FROM A/D
001A      00                  NOP               ;GO TO USER'S PROGRAM
                              ;
001B      00        CONT:     NOP               ;USER'S PROGRAM TO PROCESS
                              ;CONVERTED DATA
                              ;
                              ;INTERRUPT ROUTINE STARTS
                              ORG     30H       ;AT 30H
0030      80        INDATA:   MOVX    A, @R0    ;INPUT CONVERTED DATA
0031      A1                  MOV     @R1, A    ;STORE IN DATA ADDRESS
0032      27                  CLR     A         ;CLEAR ACC TO GET OUT OF
0033      93                  RETR              ;THE INTERRUPT LOOP
                              END
```

FIGURE 6. A/D Conversion Routine

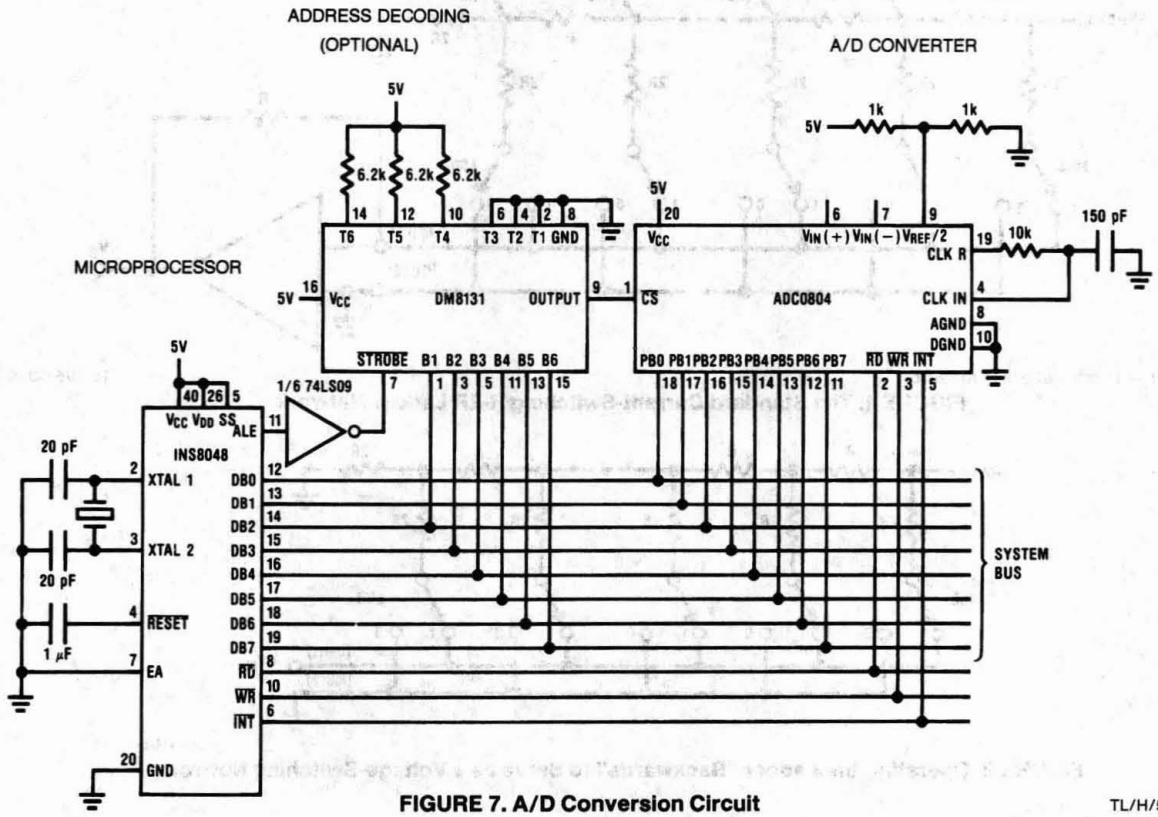


FIGURE 7. A/D Conversion Circuit

TL/H/5632–4

Single-Supply Applications of CMOS MICRODACs

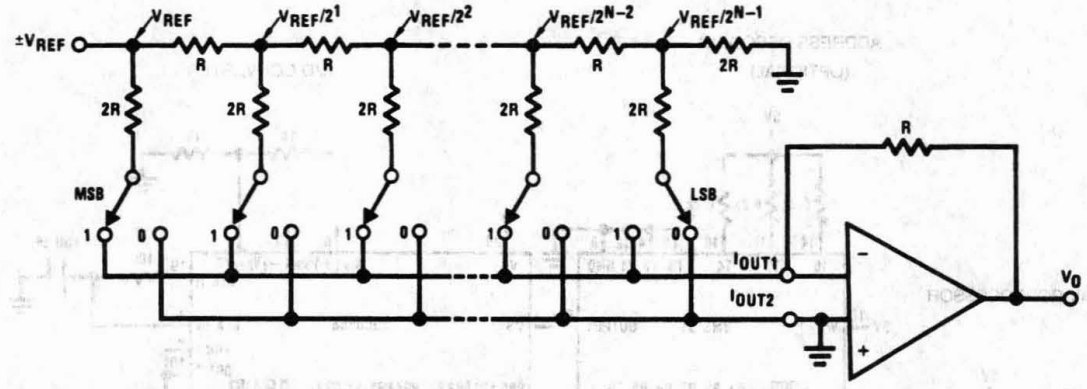
National Semiconductor
Application Note 284
Tim Regan

CMOS data acquisition and conversion products are becoming the ideal choice for microprocessor controlled analog systems. The use of CMOS allows the addition of more digital logic functionality on to the same die as the analog circuitry to minimize external parts requirements. The inherently low power consumption is also a big factor for battery operation and low heat generation in large scale systems.

National's MICRODAC™ family of 8, 10 and 12-bit D to A converters all feature on-chip data latches to permit direct interface to 8 or 16-bit data busses. These devices were designed to provide the most versatility from an analog standpoint. By utilizing a current switching R-2R ladder network *(Figure 1),* the applied reference voltage can be either a stable DC voltage or an AC voltage within the wide range of ±10V. However, output linearity requires that the two current output terminals be biased to 0V. This is accomplished by using an external op amp to serve as a current-to-voltage converter. Negative feedback via the feedback resistor included in the DAC keeps the I_{OUT1} terminal at a virtual ground potential. A drawback to this technique is that the output amplifier inverts and outputs a voltage of the opposite polarity of the applied reference. This then requires the output amplifier to have a negative supply voltage if the reference were positive. To operate with only a single-supply by biasing the ground pin of the DAC and the inputs of the op amp to ½ the supply does not work, as the digital inputs are no longer TTL compatible.

All hope is not lost, however, if single-supply operation is essential. By taking a somewhat backwards view of the DAC ladder network, only a single positive supply is necessary. In *Figure 2* the R-2R ladder network is used to switch voltages rather than currents.[1] By applying the reference to the normal current output terminal (I_{OUT1}) and grounding I_{OUT2} the voltage at the reference terminal will be a fraction of the reference voltage and a function of the applied digital input code.

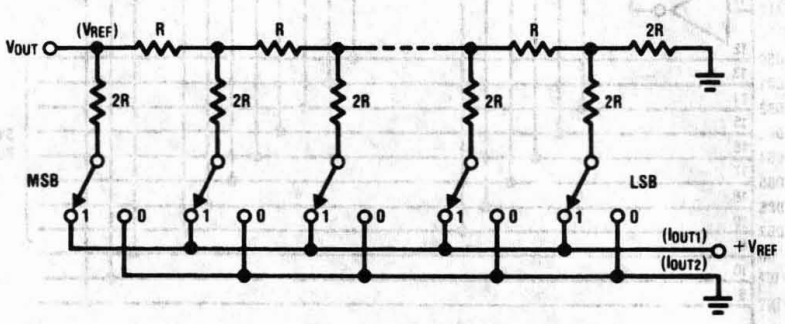
There are two important considerations when using this voltage-switching approach. The applied reference voltage must be positive since there are internal parasitic diodes from the I_{OUT} terminals to ground which would turn on if the reference were to be negative. This, of course, is of no concern with single-supply applications. There is also a dependence of converter linearity and gain error on the voltage difference between the DAC's V_{CC} supply and the applied reference voltage. This is a result of the voltage drive requirement of the CMOS ladder switches. To ensure that all of the switches can turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) an 8-bit DAC should not have a reference greater than 5V and the V_{CC} supply should be at least 9V more positive than the reference. This would keep linearity and gain error degradation less than 0.1%. A 10-bit DAC is a bit more stringent. For a 0.005% or less error degradation, the reference should be less than 3 V_{DC} and V_{CC} should be 10V more positive. The typical effects of bringing V_{REF} and V_{CC} closer together,



N = Number of bits of resolution

TL/H/5633–6

FIGURE 1. The Standard Current-Switching R-2R Ladder Network



TL/H/5633–1

FIGURE 2. Operating the Ladder "Backwards" to Serve as a Voltage-Switching Network

as well as temperature performance, are shown graphically in *Figure 3* for the 8-bit DAC0830 series.

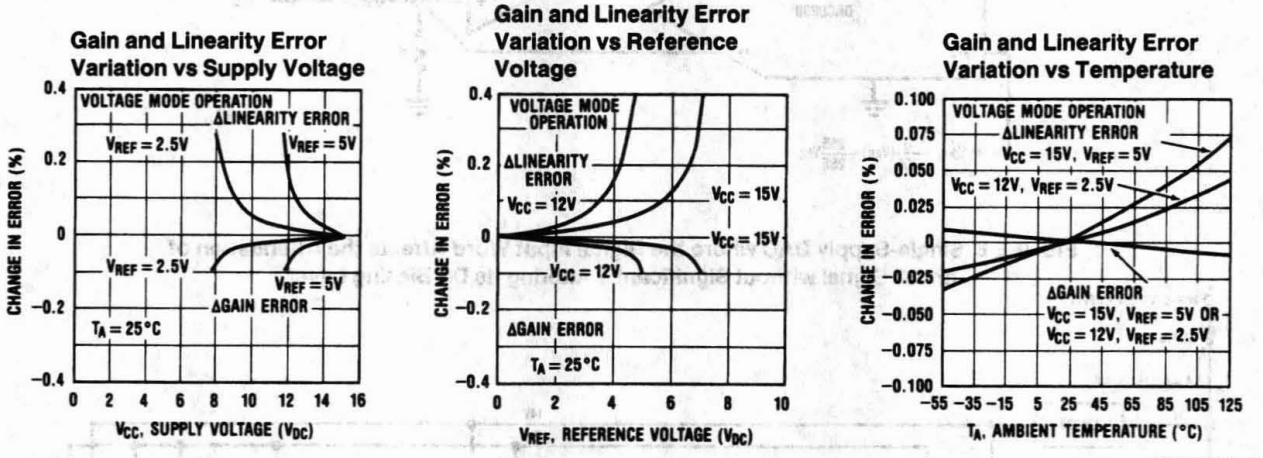
Since the output is now a voltage rather than a current, an output op amp is not necessarily required, but the DAC's output impedance is fairly high (equal to its specified reference input resistance of 10k to 20k), so an op amp may be required for buffering purposes. *Figure 4* shows a single-supply DAC with an output amplifier providing buffering and gain for a more useful 0V to 10V output from a 2.5V reference. The LM336 reference diode is biased through the internal feedback resistor between the I_{OUT1} pin and the R_{fb} pin. The zero-code output voltage is limited by the lower output saturation voltage of the LM358 op amp. The 2k pull-down load resistor helps to reduce this voltage to 10 mV or ¼ of an output LSB. Even with a 15V DAC supply, the digital inputs remain T^2L compatible.

Closer inspection of *Figure 2* shows that both I_{OUT1} and I_{OUT2} drive the ladder network in an identical manner. Each leg is connected to either I_{OUT1} or I_{OUT2} as controlled by the logic state of each digital input. If each I_{OUT} terminal is biased to separate reference potentials, the circuit of *Figure 5* results. This is a single-supply DAC with an adjustable zero-code output offset voltage and adjustable output span to reserve the full resolution of the DAC for a range of voltages other than 0V to full-scale. An important point to note is that for an all ones code applied, only the voltage at I_{OUT1} is connected to the ladder and sets the output to 255/256 times the voltage of I_{OUT1}. With an all zeros code applied, only the voltage at I_{OUT2} drives the ladder, setting the output to 255/256 times this voltage. This non-interaction of the two inputs at the end-points makes calibration a breeze. The incremental analog output steps are automatically set to $(V_{MAX} - V_{MIN})/256$.

The buffers at the two reference inputs in *Figure 5* isolate the code-dependent resistance to ground at I_{OUT1} and I_{OUT2} from the resistive string used to set V_{MAX} an V_{MIN}. The output responds in accordance to the following expression.

(1) $V_{OUT} = D/256\,(V_{MAX} - V_{MIN}) + 255/256\,V_{MIN}$

Where D is the decimal equivalent of the 8-bit binary control word.


Gain and Linearity Error Variation vs Supply Voltage
VOLTAGE MODE OPERATION
ΔLINEARITY ERROR
VREF = 2.5V
VREF = 5V
ΔGAIN ERROR
TA = 25°C
CHANGE IN ERROR (%)
VCC, SUPPLY VOLTAGE (VDC)
Gain and Linearity Error Variation vs Reference Voltage
VOLTAGE MODE OPERATION
ΔLINEARITY ERROR
VCC = 12V
VCC = 15V
ΔGAIN ERROR
TA = 25°C
CHANGE IN ERROR (%)
VREF, REFERENCE VOLTAGE (VDC)
Gain and Linearity Error Variation vs Temperature
VOLTAGE MODE OPERATION
ΔLINEARITY ERROR
VCC = 15V, VREF = 5V
VCC = 12V, VREF = 2.5V
ΔGAIN ERROR
VCC = 15V, VREF = 5V OR
VCC = 12V, VREF = 2.5V
CHANGE IN ERROR (%)
TA, AMBIENT TEMPERATURE (°C)

TL/H/5633–2

Note: For these curves, V_{REF} is the voltage applied to the I_{OUT1} terminal and I_{OUT2} is grounded.

FIGURE 3. The Effects of Bringing the V_{CC} Supply and V_{REF} Closer Together and Temperature Performance Using the DAC in the Voltage-Switching Mode

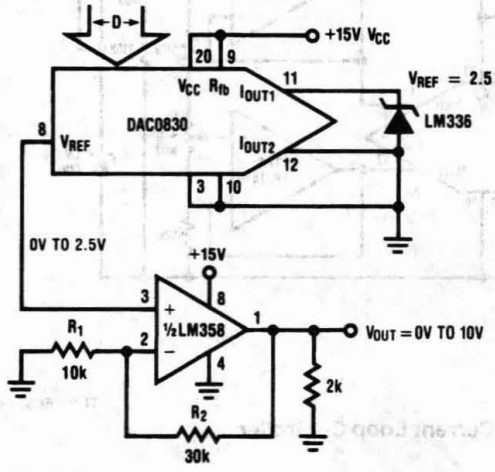
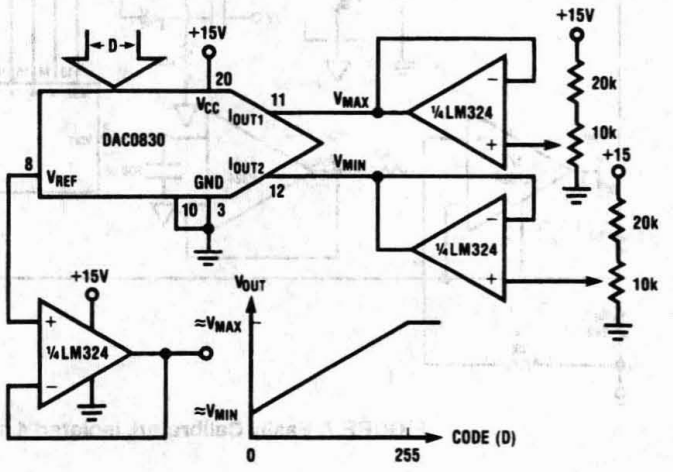


FIGURE 4. Obtaining 0V to 10V Output from a 2.5V Reference



TL/H/5633–3

FIGURE 5. A Single-Supply DAC with Level Shift and Span Adjustable Output

A common requirement of single-supply systems is that the outputs of signal-conditioning amplifiers must be DC biased, typically to ½ of the V_{CC} supply, to provide maximum unclipped AC signal swing. The circuit of *Figure 6* shows how this dual-input voltage-switching DAC configuration can allow the digital input code to control the attenuation of an AC signal without significantly affecting the DC biasing level. If the voltage at I_{OUT2} is set to the DC level of the voltage at I_{OUT1}, then the term in equation (1) which is controlled by the digital input code, D, reduces to just the AC signal at I_{OUT1}. The DC level at the output is 255/256 times the DC level at the input.

The circuit of *Figure 7* combines the advantages of low power consumption of the CMOS MICRODACs together with the non-interactive zero and full-scale adjustability of this voltage-switching technique. This circuit is an isolated 4 mA-20 mA current loop controller where the DAC sets the amount of current that flows through the loop, yet receives its own power from the very same loop.

Digital control and isolation are provided by a single optoisolator and a CMOS counter. The controlling processor must generate a clock and keep track of the number of clock pulses issued to the circuit to know what the loop current is at any time. On power-up the counter is reset to all zeros to give the processor a starting point, as well as to inherently provide a calibration point. When calibrating, potentiometer P1 would be set for the zero-code loop current of 4 mA. The processor would then issue exactly 255 clock pulses to the opto-isolator. Potentiometer P2 can then adjust the full-scale current value to 19.92 mA. If one more clock pulse is issued, the DAC input code returns to all zeros and the previously set value of 4 mA will flow, as this setting was unaffected by the full-scale adjustment.

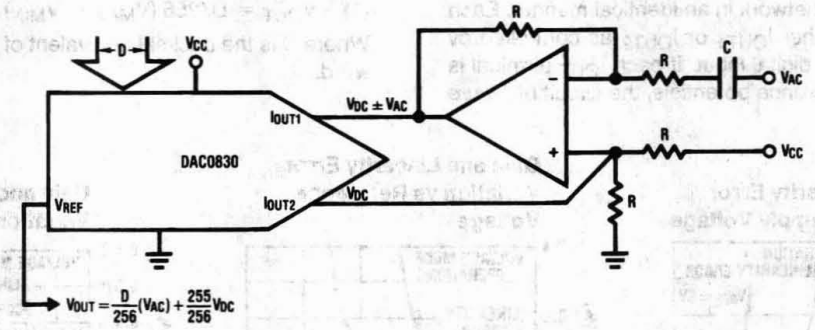
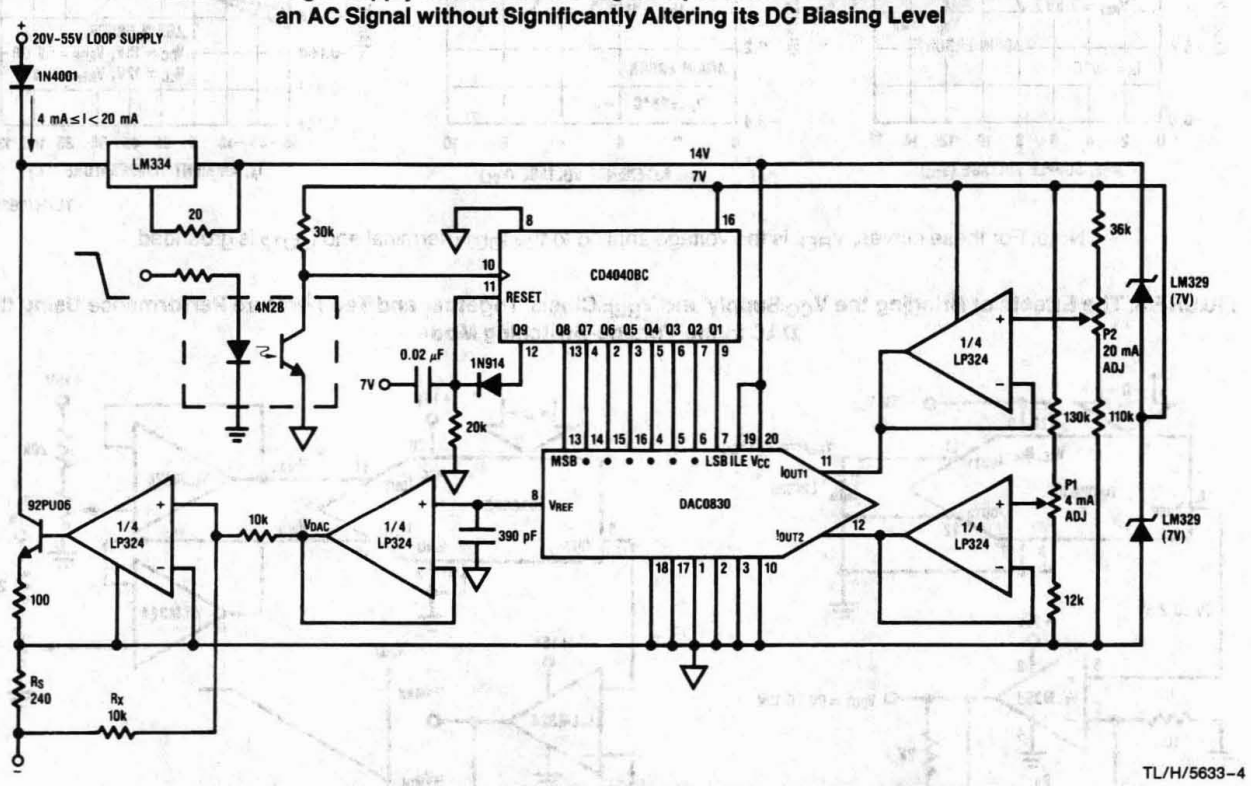


FIGURE 6. Single-Supply DAC where the Digital Input Word Affects the Attenuation of an AC Signal without Significantly Altering its DC Biasing Level



TL/H/5633–4

FIGURE 7. Easily Calibrated, Isolated 4 mA-20 mA Current Loop Controller

The NPN emitter-follower will conduct whatever level of current necessary to keep the voltage across resistor R_S equal to the voltage across resistor R_X. This voltage is equal to the output voltage at the V_{REF} pin of the DAC which can be determined from equation (1). The actual loop current is:

(2) $I_{LOOP} = V_{DAC}(1/R_S + 1/R_X)$

The second LM329 reference diode is used to bias the DAC V_{CC} supply higher than the voltages at I_{OUT1} and I_{OUT2} to preserve linearity.

Finally, what if a D to A function is required, but only a single 5V supply is available and minimal supply current is a primary concern (battery powered instrumentation is a good example)? The voltage-switching techniques previously described are not suitable because not enough voltage is available to properly bias the DAC. A CMOS DAC is still attractive for its low supply current requirements and if it can be operated in the standard current switching configuration, a single 5V supply is sufficient. But how about the voltage inversion and the requirement for negative supply potential? By taking advantage of an age-old technique of clocking a diode-capacitor network connected as a DC to DC voltage inverter, a low current negative supply can be generated. In the circuit of *Figure 8,* 2 diodes and 2 capacitors are clocked by a CMOS Schmitt trigger oscillator and connected in such a fashion as to generate a −3.8V supply potential. This negative supply is used only to bias a low current LM385-2.5V reference diode to provide the DAC with a stable negative reference. Now the inversion of the output current-to-voltage converter will generate a positive output ranging from 0V to 2.5V as a function of the digital input code.

The amount of ripple that may appear at the reference input is a function of the dynamic impedance of the LM385, the clock frequency and the size of the switching capacitors. For the component values shown, the clock frequency is approximately 1 kHz and the ripple on the reference is 7 mV peak to peak. This ripple is cleanly filtered by the bypass cap around the feedback resistor of the output amplifier. The output op amp is part of a new low power quad, the LP324, which is ideal for its ability to common-mode to ground on the inputs and swing very close to ground at its output. If an extra CMOS Schmitt inverter is not readily available, the oscillator function can be implemented with another of the amplifiers in the op amp package. The total supply current of this single-supply DAC is on the order of 1.5 mA with no output load.

With this technique even the 12-bit DAC1230 can be used with no linearity degradation which would be apparent in the voltage-switching techniques.

REFERENCE

1. Sevastopoulos, N.; Cecil, J.; and Fredericksen, T., *"An Unusual Circuit Configuration Improves CMOS-MDAC Performance",* EDN Magazine, March 5, 1979, pg. 77.

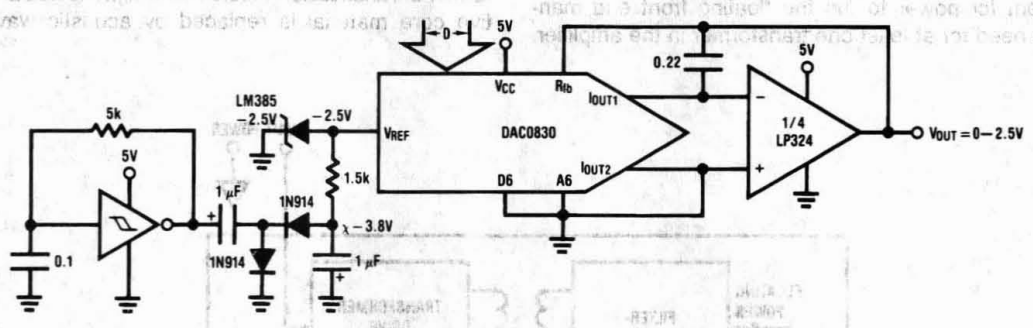


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FIGURE 8. Single 5V Supply, 8-Bit CMOS DAC

An Acoustic Transformer Powered Super-High Isolation Amplifier

National Semiconductor
Application Note 285

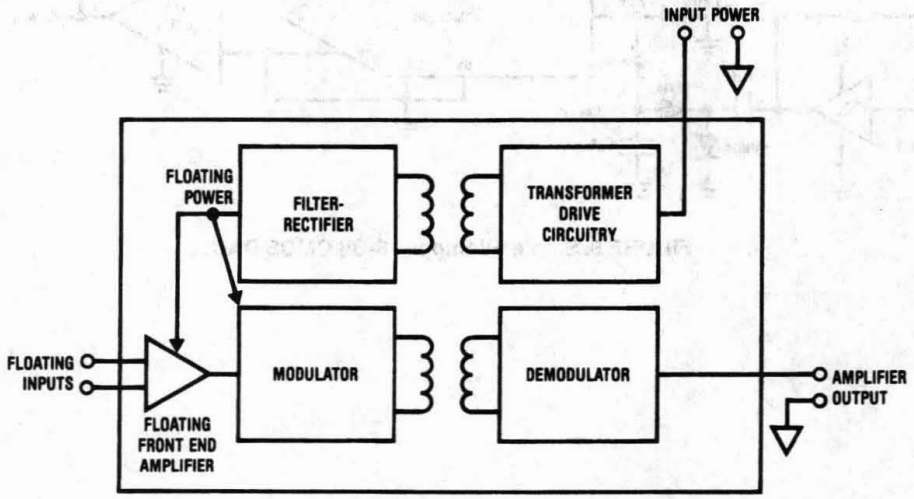
A number of measurements require an amplifier whose input terminals are galvanically isolated from its output and power terminals. Such devices, often called parametric or isolation amplifiers, are employed in situations that call for measurements in the presence of high common-mode voltages or require complete ground path isolation for safety reasons. Although commercial devices are available to meet these needs, the method of power transfer used to supply power to the floating input circuitry has limited the common-mode voltage capability to about 2500V. In addition, leakage currents can run as high as 2 μA.

Present devices (*Figure 1)* employ transformers to transmit power to the floating front end of the amplifier. The output of the floating amplifier is then modulated onto a carrier which is transmitted via a transformer or opto-isolator to the output of the amplifier. Modulation schemes employed include pulse width and pulse amplitude as well as frequency and light intensity coding. The limitation on common-mode voltage breakdown and leakage in this type of device is the breakdown rating of the transformers employed. Even when opto-isolators are used to transmit the modulated signal, the requirement for power to run the floating front end mandates the need for at least one transformer in the amplifier.

Although other methods of transmitting electrical energy with high isolation are available (e.g., microwaves, solar cells) they are expensive, inefficient and impractical. Batteries present and obvious choice but have drawbacks due to maintenance and reliability. What is really needed to achieve extremely high common-mode capability and low leakage is a method for transferring electrical energy which is relatively efficient, easy to implement and offers almost total input-to-input isolation.

ACOUSTIC TRANSFORMERS

A technique which satisfies the aforementioned requirements is available by taking advantage of the piezoelectric characteristics of certain ceramic materials. Although piezoelectric materials have long been recognized as electrical-to-acoustic or acoustic-to-electrical transducers (e.g., buzzers and microphones) their capability for electrical-to-acoustic-to-electrical energy conversion has not been employed. This technique, which capitalizes on the non-conducting nature of ceramic materials, is the key to a super-high isolation electrical transformer. In this device the conventional transformer's transmission medium of magnetic flux and conductive core material is replaced by acoustic waves and a



TL/H/5634–1

FIGURE 1

non-conducting piezoceramic core. *Figure 2* shows a photograph of typical acoustic transformers, fabricated by Channel Industries, Santa Barbara, California. Two physical configurations are shown, although many are possible. In each case the transformer is constructed by simply bonding a pair of leads to each end of the piezoceramic material. Insulation resistance exceeds $10^{12}\Omega$ and primary-to-secondary capacitance is typically a few pF. The nature of the piezoceramic material employed and the specific physical configuration determines the resonant frequency of the transformer. *Figure 3* shows a plot of the output of an acoustic transformer driven at resonance. From the data it can be seen that transfer efficiency can exceed 75%, depending upon loading conditions. Output short circuit current for the device tested was 35 mA.

APPLYING THE TRANSFORMER—A 20,000V ISOLATION AMPLIFIER

Figure 4 shows a basic but working design for an isolation amplifier using the acoustic transformer. This design will easily stand off common-mode voltages of 20,000V and versions that operate at 100 kV potentials have been constructed. In this design the acoustic transformer's HI-Q characteristics are used to allow it to self resonate in a manner similar to a quartz crystal. This eliminates the requirement to drive the transformer with a stable oscillator.

The Q1 configuration provides excitation to the transformer primary, while the diodes and capacitor rectify and filter the secondary's output. *Figure 5* shows the collector waveform at Q1 (Trace A) while Trace B, *Figure 5* shows the secondary output. Despite the distorted drive waveform the transformer's secondary output is a clean sinusoid because of the extremely Hi-Q of the device. An LM331 V/F converter is used to convert the amplitude input to a frequency output. The V/F output drives an LED, whose output is coupled to a length of fiber-optic cable. Trace A, *Figure 6* shows the LM331's output, while Trace B indicates the current through the LED. Each time the LM331 output goes low, a short 20 mA current spike is passed through the LED via the 0.01 μF capacitor. Because the duty cycle is low, the average current out of the transformer's secondary is small and power requirements are minimized. At the amplifier output a photodiode is used to detect the light encoded signal and another LM331 serves as an F/V converter to demodulate the frequency encoded signal.

APPLICATIONS

An excellent application for the high isolation amplifier is shown in *Figure 7.* Here, the winding temperature of an electric utility transformer operating at 10,000V is monitored by the LM135 temperature transducer. The LM135 output biases the isolation amplifier input and the temperature information comes out at the amplifier output, safely referenced to ground.

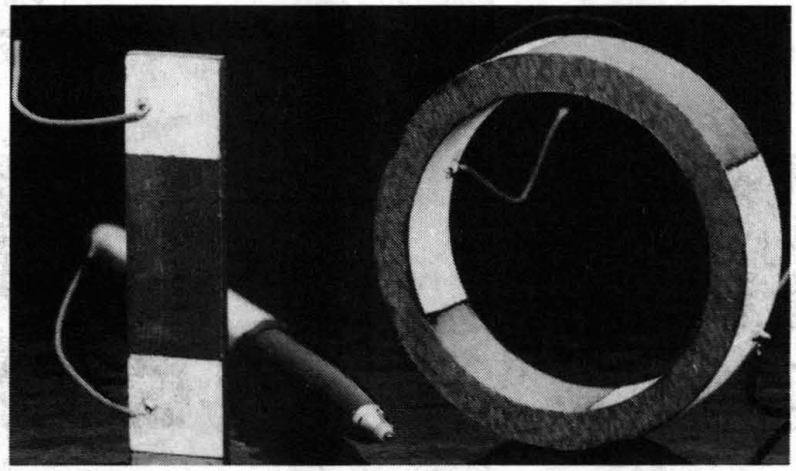


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FIGURE 2

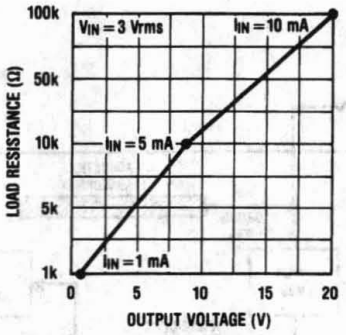

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FIGURE 3

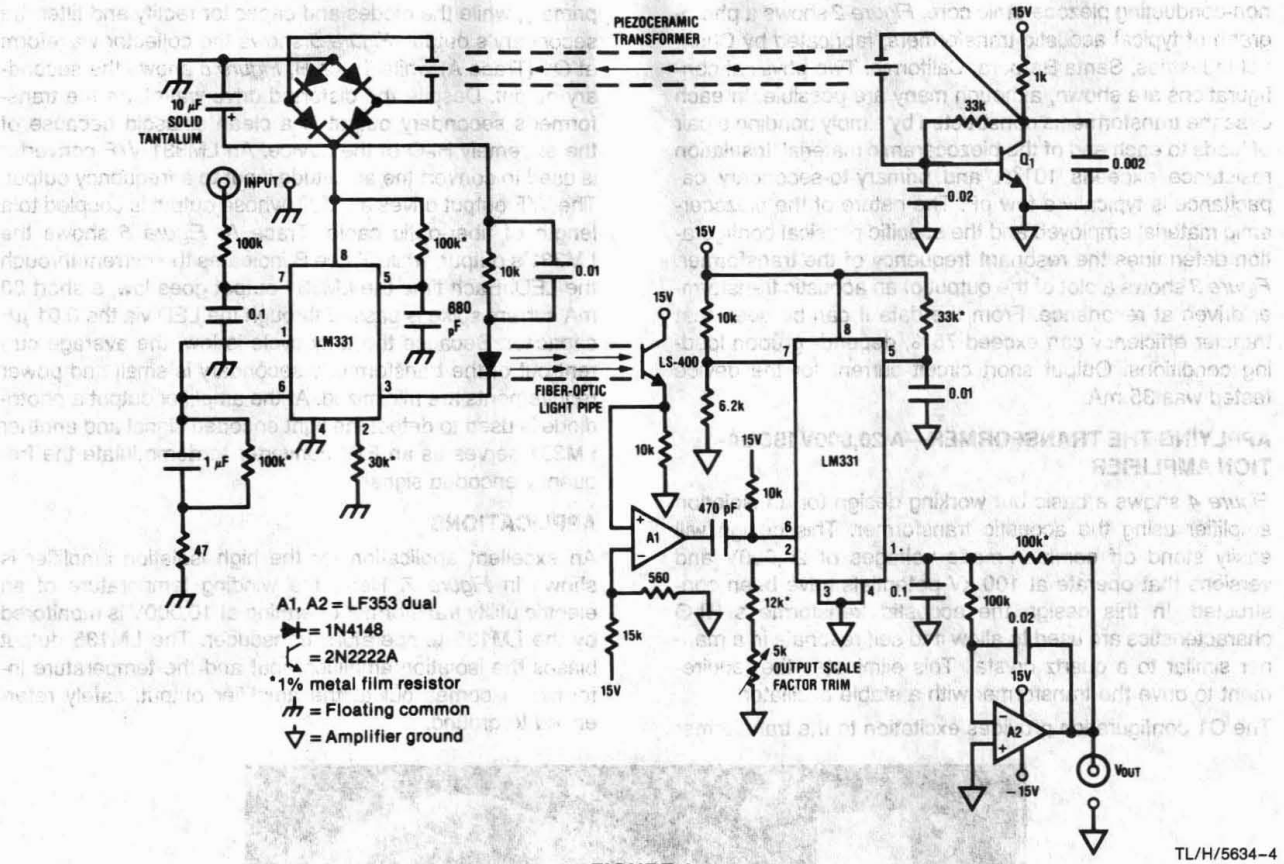

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FIGURE 4

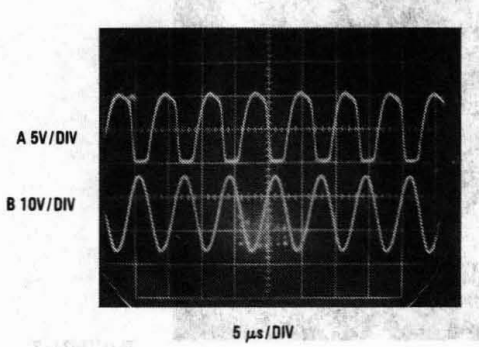

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FIGURE 5

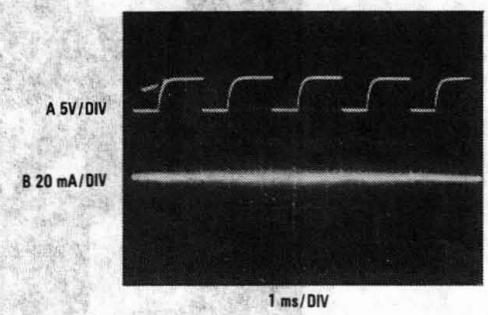

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FIGURE 6

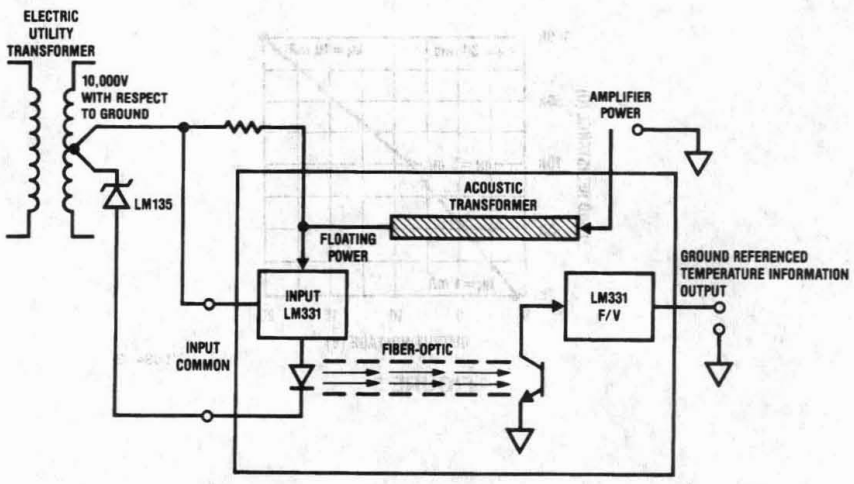

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FIGURE 7

Figure 8 shows another application where the high common-mode voltage capability allows a 5000V regulated power supply to have a fully floating output. Here, a push-pull type DC-DC converter generates the 5 kV output. The piezo-isolation amplifier provides a ground referenced output feedback signal to A1, which controls the transformer drive, completing a feedback loop.

In *Figure 9,* the piezo-isolation amplifier is used to provide complete and fail-safe isolation for the inputs of a piece of test equipment to be connected into a CMOS IC production line. This capability prevents any possibility of static discharge damage, even when the equipment may have accumulated a substantial charge.

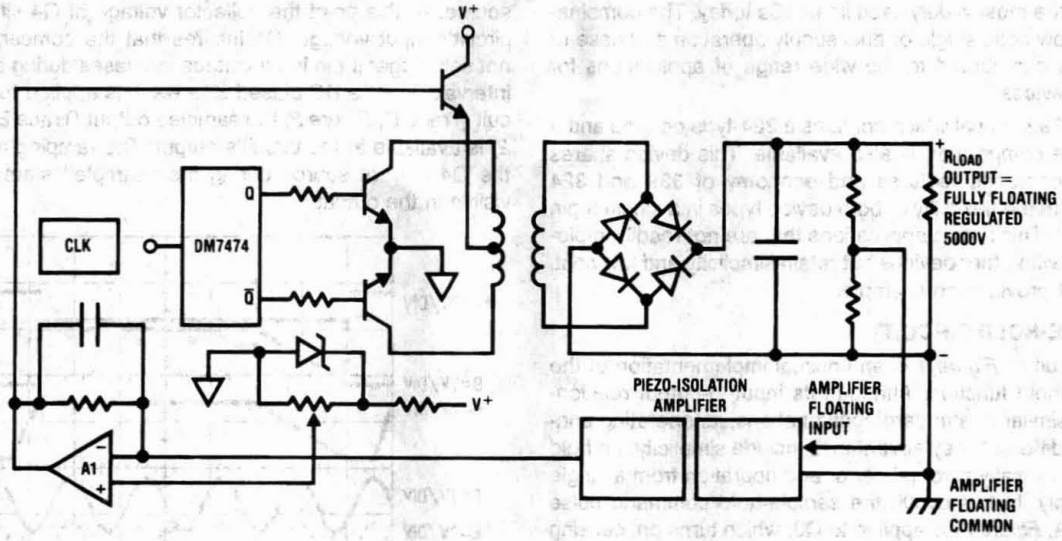
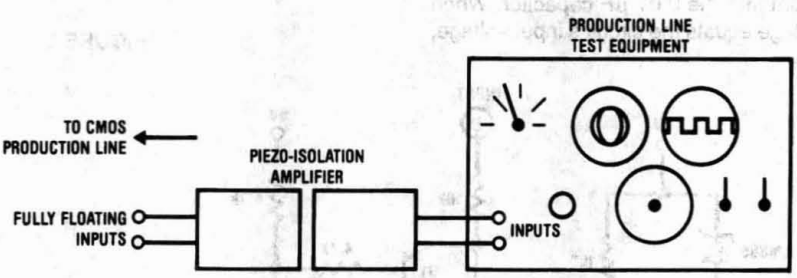


FIGURE 8



TL/H/5634–8

FIGURE 9

Applications of the LM392 Comparator Op Amp IC

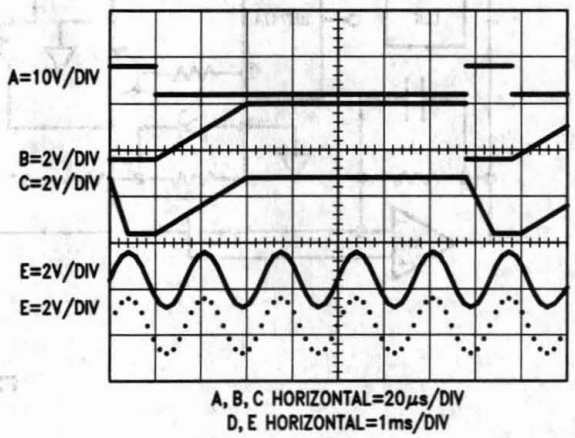
National Semiconductor
Application Note 286

The LM339 quad comparator and the LM324 op amp are among the most widely used linear ICs today. The combination of low cost, single or dual supply operation and ease of use has contributed to the wide range of applications for these devices.

The LM392, a dual which contains a 324-type op amp and a 339-type comparator, is also available. This device shares all the operating features and economy of 339 and 324 types with the flexibility of both device types in a single 8-pin mini-DIP. This allows applications that are not readily implemented with other devices but retain simplicity and low cost. *Figure 1* provides an example.

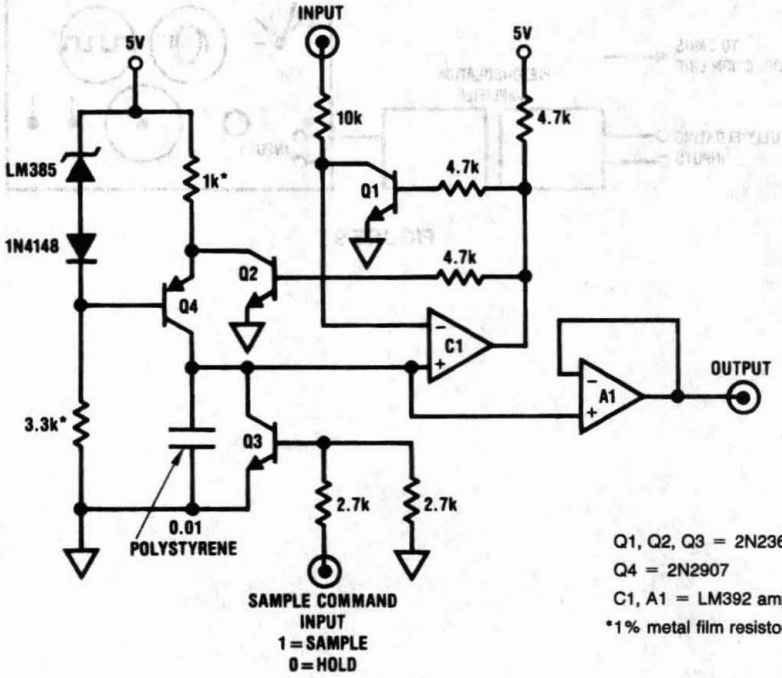
SAMPLE-HOLD CIRCUIT

The circuit of *Figure 1* is an unusual implementation of the sample-hold function. Although its input-to-output relationship is similar to standard configurations, its operating principle is different. Key advantages include simplicity, no hold step, essentially zero gain error and operation from a single 5V supply. In this circuit the sample-hold command pulse (Trace A, *Figure 2*) is applied to Q3, which turns on, causing current source transistor Q4's collector (Trace B, *Figure 2*) to go to ground potential. Amplifier A1 follows Q4's collector voltage and provides the circuit's output (Trace C, *Figure 2*). When the sample-hold command pulse falls, Q4's collector drives a constant current into the 0.01 μF capacitor. When the capacitor ramp voltage equals the circuit's input voltage, comparator C1 switches, causing Q2 to turn off the current source. At this point the collector voltage of Q4 sits at the circuit's input voltage. Q1 insures that the comparator will not self trigger if the input voltage increases during a "hold" interval. When a DC biased sine wave is applied to the circuit (Trace D, *Figure 2*) the sampled output (Trace E, *Figure 2*) is available at the circuit's output. The ramping action of the Q4 current source during the "sample" states is just visible in the output.



TL/H/7493–1

FIGURE 2



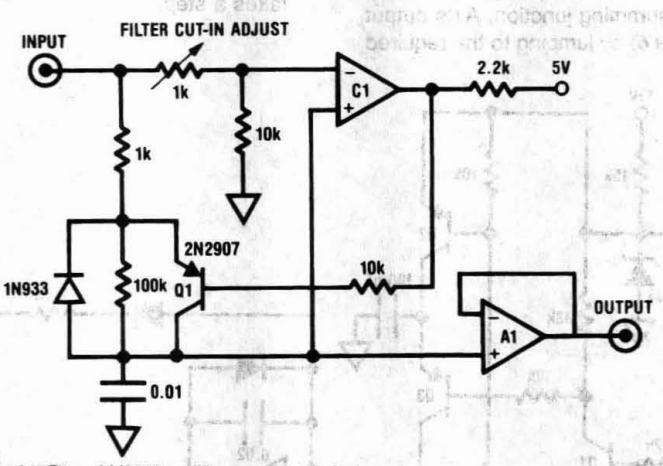
Q1, Q2, Q3 = 2N2369
Q4 = 2N2907
C1, A1 = LM392 amplifier-comparator dual
*1% metal film resistor

TL/H/7493–2

FIGURE 1

"FED-FORWARD" LOW-PASS FILTER

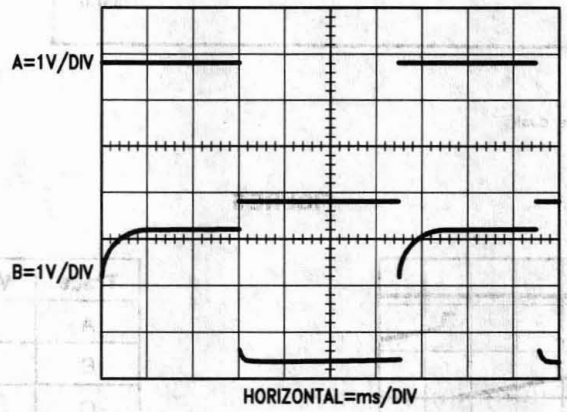
In *Figure 3* the LM392 implements a useful solution to a common filtering problem. This single supply circuit allows a signal to be rapidly acquired to final value but provides a long filtering constant. This characteristic is useful in multiplexed data acquisition systems and has been employed in electronic infant scales where fast, stable readings of infant weight are desired despite motion on the scale platform. When an input step (Trace A, *Figure 4*) is applied, C1's negative input will immediately rise to a voltage determined by the 1k pot-10 kΩ divider. C1's "+" input is biased through the 100 kΩ-0.01 μF time constant and phase lags the input. Under these conditions C1's output will go low, turning on Q1. This causes the capacitor (Waveform B, *Figure 2*) to charge rapidly towards the input value. When the voltage across the capacitor equals the voltage at C1's positive input, C1's output will go high, turning off Q1. Now, the capacitor can only charge through the 100k value and the time constant will be long. Waveform B clearly shows this. The point at which the filter switches from short to long time constant is adjustable with the 1 kΩ potentiometer. Normally, this is adjusted so that switching occurs at 90%–98% of final value, but the photo was taken at a 70% trip point so circuit operation is easily discernible. A1 provides a buffered output. When the input returns to zero the 1N933 diode, a low forward drop type, provides rapid discharge for the capacitor.



A1, C1 = LM392 amplifier-comparator dual

TL/H/7493–3

FIGURE 3



TL/H/7493–4

FIGURE 4

VARIABLE RATIO DIGITAL DIVIDER

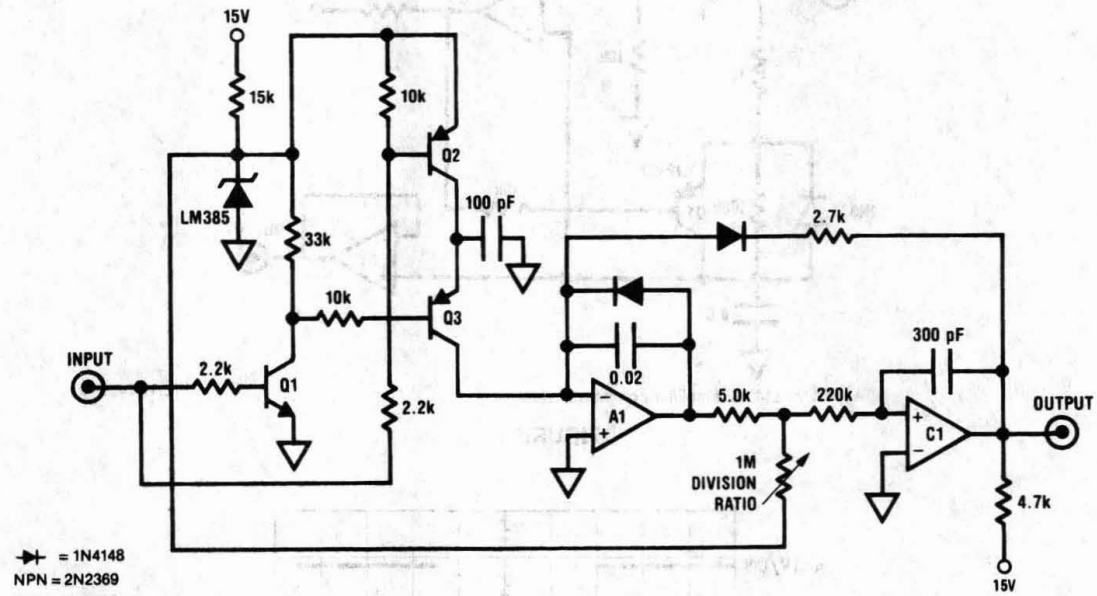
In *Figure 5* the circuit allows a digital pulse input to be divided by any number from 1 to 100 with control provided by a single knob. This function is ideal for bench type work where the rapid set-up and flexibility of the division ratio is highly desirable. When the circuit input is low, Q1 and Q3 are off and Q2 is on. This causes the 100 pF capacitor to accumulate a quantity of charge (Q) equal to

$Q = CV$

where $C = 100$ pF

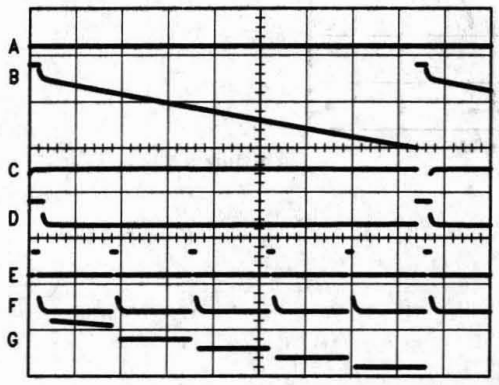
and $V =$ the LM385 potential (1.2V) minus the $V_{CE(SAT)}$ of Q2.

When the input goes high (Trace A, *Figure 6*) Q2 goes off and Q1 turns on Q3. This causes Q3 to displace the 100 pF capacitor's charge into A1's summing junction. A1's output responds (Waveform B, *Figure 6*) by jumping to the required value to maintain the summing junction at 0V. This sequence is repeated for every input pulse. During this time A1's output will form the staircase shape shown in Trace B as the 0.02 μF feedback capacitor is pumped up by the charge dispensing action into A1's summing junction. When A1's output is great enough to just bias C1's "+" input below ground, C1's output (Trace C, *Figure 6*) goes low and resets A1 to 0V. Positive feedback to C1's "+" input (Trace D, *Figure 6*) comes through the 300 pF unit, insuring adequate reset time for A1. The 1 MΩ potentiometer, by setting the number of steps in the ramp required to trip C1, controls the circuit input-output division ratio. Traces E–G expand the scale to show circuit detail. When the input (Trace E) goes high, charge is deposited into A1's summing junction (Trace F) and the resultant staircase waveform (Trace G) takes a step.



TL/H/7493–5

FIGURE 5



TL/H/7493–6

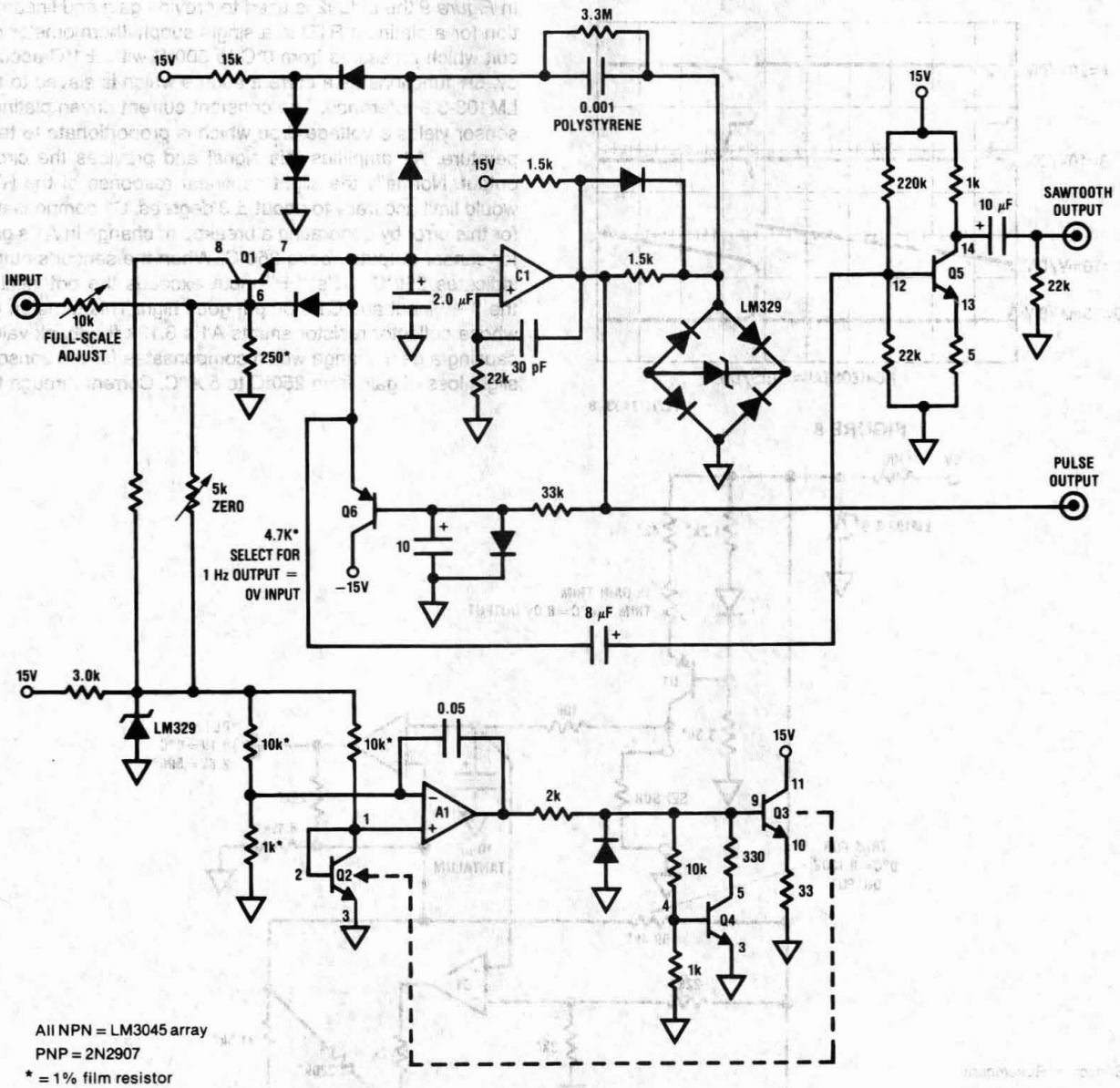
FIGURE 6

Trace	Vertical	Horizontal
A	10V	500 μs
B	1V	500 μs
C	50V	500 μs
D	50V	500 μs
E	10V	50 μs
F	10 mA	50 μs
G	0.1V	50 μs

EXPONENTIAL V/F CONVERTER FOR ELECTRONIC MUSIC

Professional grade electronic music synthesizers require voltage controlled frequency generators whose output frequencies are exponentially related to the input voltages. *Figure 7* diagrams a circuit which performs this function with 0.25% exponential conformity over a range from 20 Hz to 15 kHz using a single LM392 and an LM3045 transistor array. The exponential function is generated by Q1, whose collector current will vary exponentially with its base-emitter voltage in accordance with the well known relationship between BE voltage and collector current in bipolar transistors. Normally, this transistor's operating point will vary wildly with temperature and elaborate and expensive compensation is required. Here, Q1 is part of an LM3045 transistor array. Q2 and Q3, located in the array, serve as a heater-sensor pair for A1, which servo controls the temperature of Q2. This causes the entire LM3045 array to be at constant temperature, eliminating thermal drift problems in Q1's operation. Q4 acts as a clamp, preventing servo lock-up during circuit start-up.

Q1's current output is fed into the summing junction of a charge dispensing I/F converter. C1's output state is used to switch the 0.001 μF capacitor between a reference voltage and C1's "−" input. The reference voltage is furnished by the LM329 zener diode bridge. The comparator's output pulse width is unimportant as long as it permits complete charging and discharging of the capacitor. In operation, C1 drives the 30 pF-22k combination. This RC provides regenerative feedback which reinforces the direction of C1's output. When the 30 pF-22k combination decays, the positive feedback ceases. Thus, any negative going amplifier output will be followed by a positive edge after an amount of time



All NPN = LM3045 array
PNP = 2N2907
* = 1% film resistor
A1, C1 = LM392 amplifier-comparator dual
▶|◀ = 1N4148

FIGURE 7

TL/H/7493–7

governed by the 30 pF-22k time constant (Waveforms A and B, *Figure 8*). The actual integration capacitor in the circuit is the 2 μF electrolytic. This capacitor is never allowed to charge beyond 10 mV–15 mV because it is constantly being reset by charge dispensed from the switching of the 0.001 μF capacitor (Waveform C, *Figure 8*). Whenever the amplifier's output goes negative, the 0.001 μF capacitor dumps a quantity of charge (Waveform D) into the 2 μF capacitor, forcing it to a lower potential. The amplifier's output going negative also causes a short pulse to be transferred through the 30 pF capacitor to the "+" input. When this negative pulse decays out so that the "+" input is higher than the "−" input, the 0.001 μF capacitor is again able to receive a charge and the entire process repeats. The rate at which this sequence occurs is directly related to the current into C1's summing junction from Q1. Since this current is exponentially related to the circuit's input voltage, the overall I/F transfer function is exponentially related to the input voltage. This circuit can lock-up under several conditions. Any condition which would allow the 2 μF electrolytic to charge beyond 10 mV–20 mV (start-up, overdrive at the input, etc.) will cause the output of the amplifier to go to the negative rail and stay there. The 2N2907A transistor prevents this by pulling the "−" input towards −15V. The 10 μF-33k combination determines when the transistor will come on. When the circuit is running normally, the 2N2907 is biased off and is effectively out of the circuit. To calibrate the circuit, ground the input and adjust the zero potentiometer until oscillations just start. Next, adjust the full-scale potentiometer so that frequency output exactly doubles for each volt of input (e.g., 1V per octave for musical purposes). Repeat these adjustments until both are fixed. C1 provides a pulse output while Q5 AC amplifies the summing junction ramp for a sawtooth output.

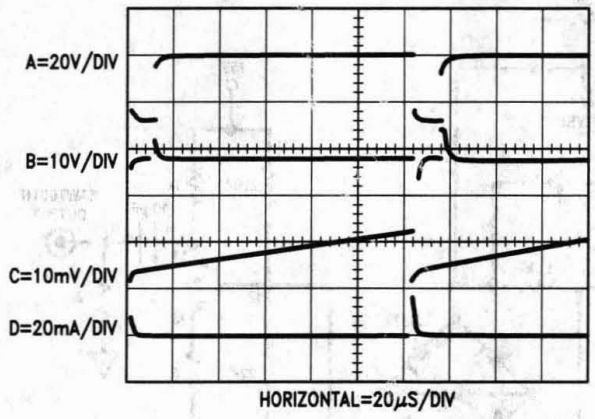


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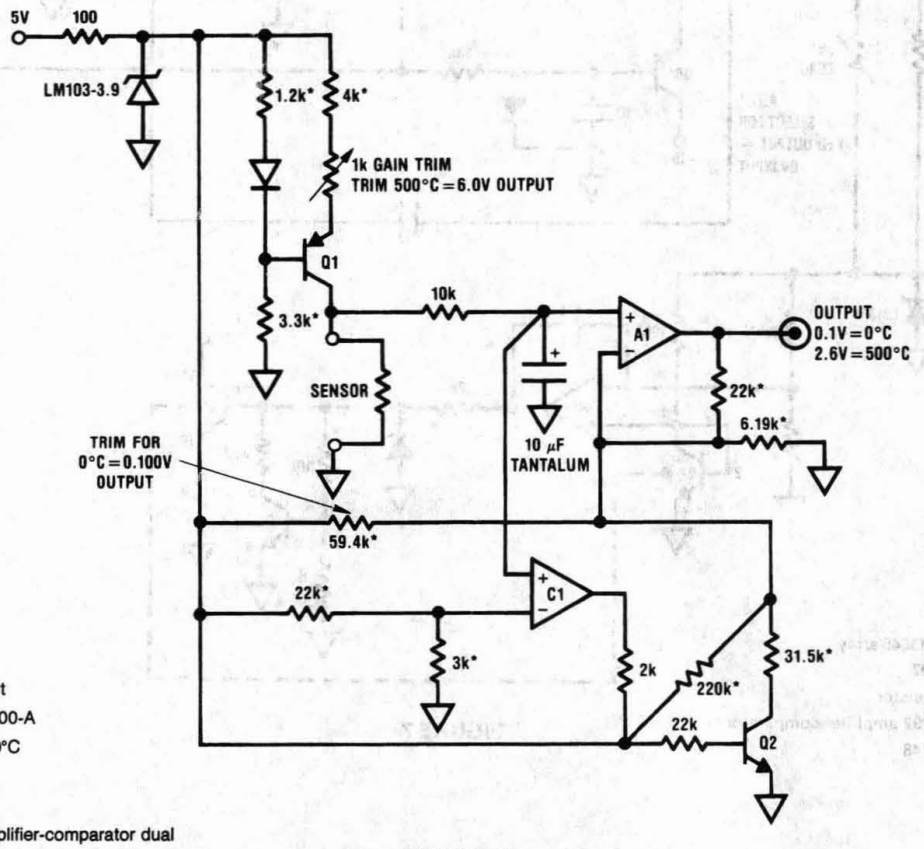
FIGURE 8

LINEARIZED PLATINUM RTD THERMOMETER

In *Figure 9* the LM392 is used to provide gain and linearization for a platinum RTD in a single supply thermometer circuit which measures from 0°C to 500°C with ±1°C accuracy. Q1 functions as a current source which is slaved to the LM103-3.9 reference. The constant current driven platinum sensor yields a voltage drop which is proportionate to temperature. A1 amplifies this signal and provides the circuit output. Normally the slight nonlinear response of the RTD would limit accuracy to about ±3 degrees. C1 compensates for this error by generating a breakpoint change in A1's gain for sensor outputs above 250°C. When the sensor's output indicates 250°C, C1's "+" input exceeds the potential at the "−" input and C1's output goes high. This turns on Q2 whose collector resistor shunts A1's 6.19k feedback value, causing a gain change which compensates for the sensor's slight loss of gain from 250°C to 500°C. Current through the



Sensor = Rosemount
118 MF-1000-A
1000Ω at 0°C
Q1 = 2N2907
Q2 = 2N2222A
A1, C1 = LM392 amplifier-comparator dual
*metal film resistor

TL/H/7493–9

FIGURE 9

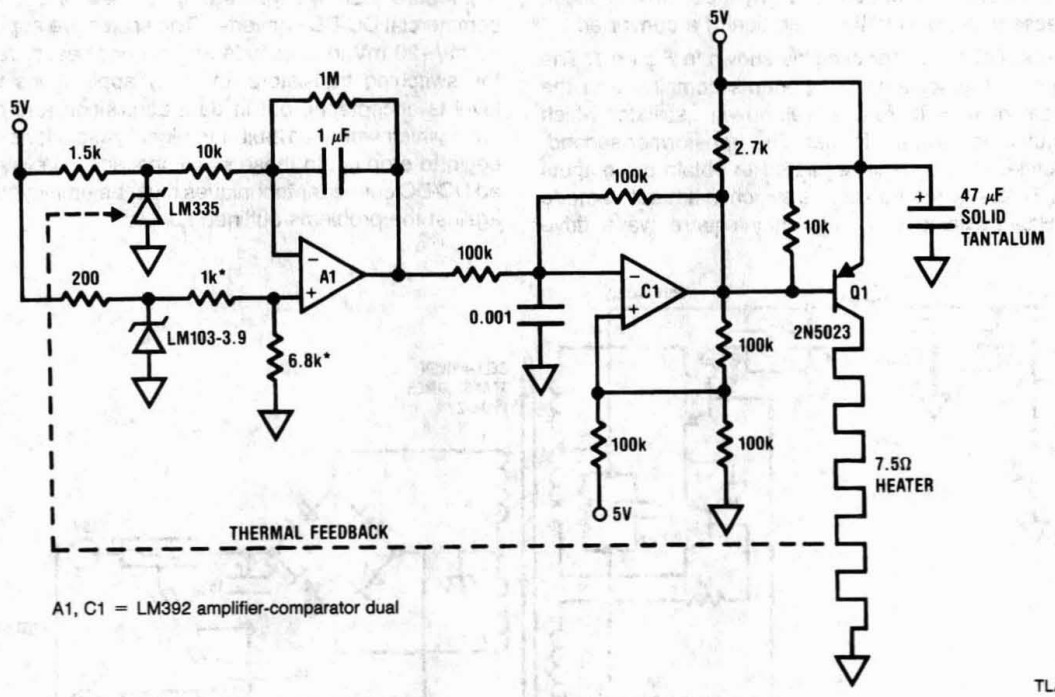
220k resistor shifts the offset of A1 so no "hop" occurs at the circuit output when the breakpoint is activated. A precision decade box is used to calibrate this circuit. With the box inserted in place of the sensor, adjust 0°C for 0.10V output for a value of 1000Ω. Next dial in 2846Ω (500°C) and adjust the gain trim for an output of 2.60V. Repeat these adjustments until both zero and full-scale are fixed at these points.

TEMPERATURE CONTROLLER

Figure 10 details the LM392 in a circuit which will temperature-control an oven at 75°C. This is ideal for most types of quartz crystals. 5V single supply operation allows the circuit to be powered directly from TTL-type rails. A1, operating at a gain of 100, determines the voltage difference between the temperature setpoint and the LM335 temperature sensor, which is located inside the oven. The temperature setpoint is established by the LM103-3.9 reference and the 1k-6.8k divider. A1's output biases C1, which functions as a pulse width modulator and biases Q1 to deliver switched-mode power to the heater. When power is applied, A1's output goes high, causing C1's output to saturate low. Q1 comes on and delivers DC to the heater. When the oven warms to the setpoint, A1's output falls and C1 begins to pulse width modulate the heater in servo control fashion. In practice the LM335 should be in good thermal contact with the heater to prevent servo oscillation.

REFERENCES

1. *Transducer Interface Handbook,* pp. 220–223; Analog Devices, Inc.
2. "A New Ultra-Linear Voltage-to-Frequency Converter", Pease, R. A.; *1973 NEREM Record* Volume 1, page 167.



A1, C1 = LM392 amplifier-comparator dual

TL/H/7493–10

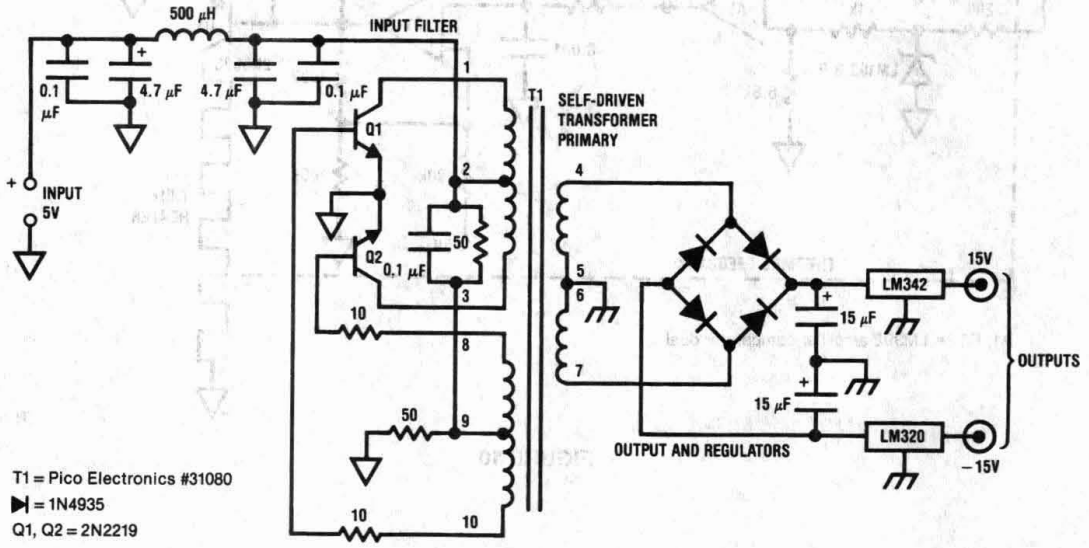
FIGURE 10

System-Oriented DC-DC Conversion Techniques

National Semiconductor
Application Note 288

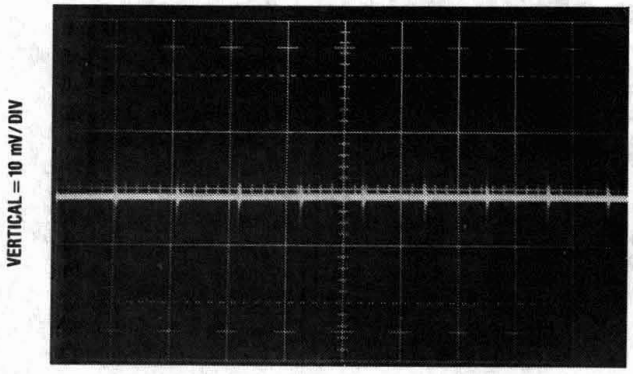
In many electronic systems, the need arises to generate small amounts of power at voltages other than the main supply voltage. This is especially the case in digital systems where a relatively small amount of analog circuitry must be powered. A number of manufacturers have addressed this requirement by offering modular DC-DC converters which are PC mountable, offer good efficiency and are available in a variety of input and output voltage ranges. These units are widely applied and, in general, are well engineered for most applications. The sole problem with these devices is noise, in the form of high frequency switching spikes which appear on the output lines. To understand why these spikes occur, it is necessary to examine the operation of a converter.

A typical DC-DC converter circuit is shown in *Figure 1*. The transistors and associated components combine with the transformer primary to form a self-driven oscillator which provides drive to the transformer. The transformer secondary is rectified, filtered and regulated to obtain the outputs required. Typically, the transistors switch in saturated mode at 20 kHz, providing high efficiency square wave drive to the transformer. The output filter capacitors are relatively small compared to sine wave driven transformers and overall losses are quite low. The high speed, saturated switching of the transistors does, however, generate high frequency noise components. These manifest themselves as short duration current spikes drawn from the converter's input supply and as high speed spikes which appear on the output lines. In addition, the transformer can radiate noise in RF fashion. Manufacturers have dealt with these problems through careful converter design, including attention to input filter design, transformer construction and package shielding. *Figure 2* shows typical output noise of a good quality commercial DC-DC converter. The spikes are approximately 10 mV–20 mV in amplitude and occur at each transition of the switching transistors. In many applications this noise level is acceptable, but in data acquisition and other systems which work at 12-bit and higher resolutions, problems begin to crop up. In these situations, special system-oriented DC-DC converter techniques must be employed to insure against the problems outlined above.



TL/H/7495–1

FIGURE 1



TL/H/7495–2

FIGURE 2

BLANK PULSE CONVERTER

Figure 3 shows a converter which will supply 100 mA at ±15V from a 5V input. This design attacks the noise problem in two ways. The LM3524 switching regulator chip provides non-overlapping drive to the transistors, eliminating simultaneous conduction which helps keep input current spiking down. The LM3524 operates open loop. Its feedback connection (pin 9) is tied high, forcing the chip's outputs to full duty cycle. Internal logic in the LM3524 prevents the transistors from conducting at the same time. The components at pins 6 and 7 set the switching frequency. The LM3524's timing ramp biases the LM311 comparator to generate a blank pulse which "brackets" the output noise pulse. *Figure 4* shows the switching transistor waveforms (trace A and B) and the blank pulse (trace C) which is issued at each switching transition. The converter's output noise is shown in trace D. The blank pulse is used to alert the system that a noise spike is imminent. In this fashion, a critical A/D conversion or sample-hold operation can be delayed until the converter's noise spike has settled. This technique is quite effective, because it does not allow the system to "see" noise spikes during critical periods. This not only insures good system performance, but also means that a relatively simplistic converter design can be employed. The expense associated with low output noise (e.g., shielding, special filtering, etc.) can be eliminated in many cases. *Figure 5* details a converter design which uses a different approach to solving the same problem.

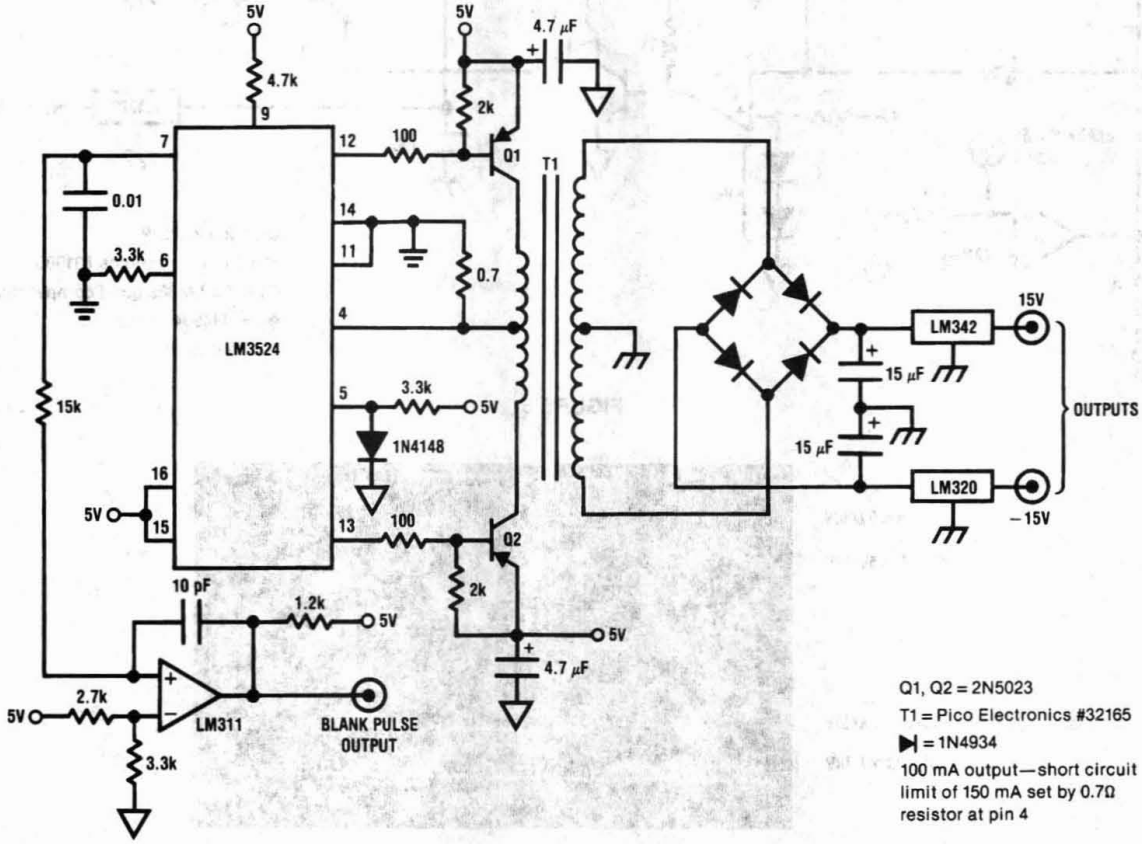


FIGURE 3

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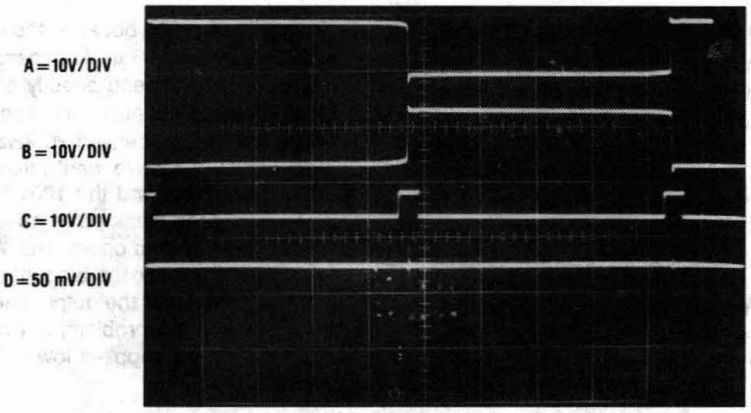


FIGURE 4

TL/H/7495–4

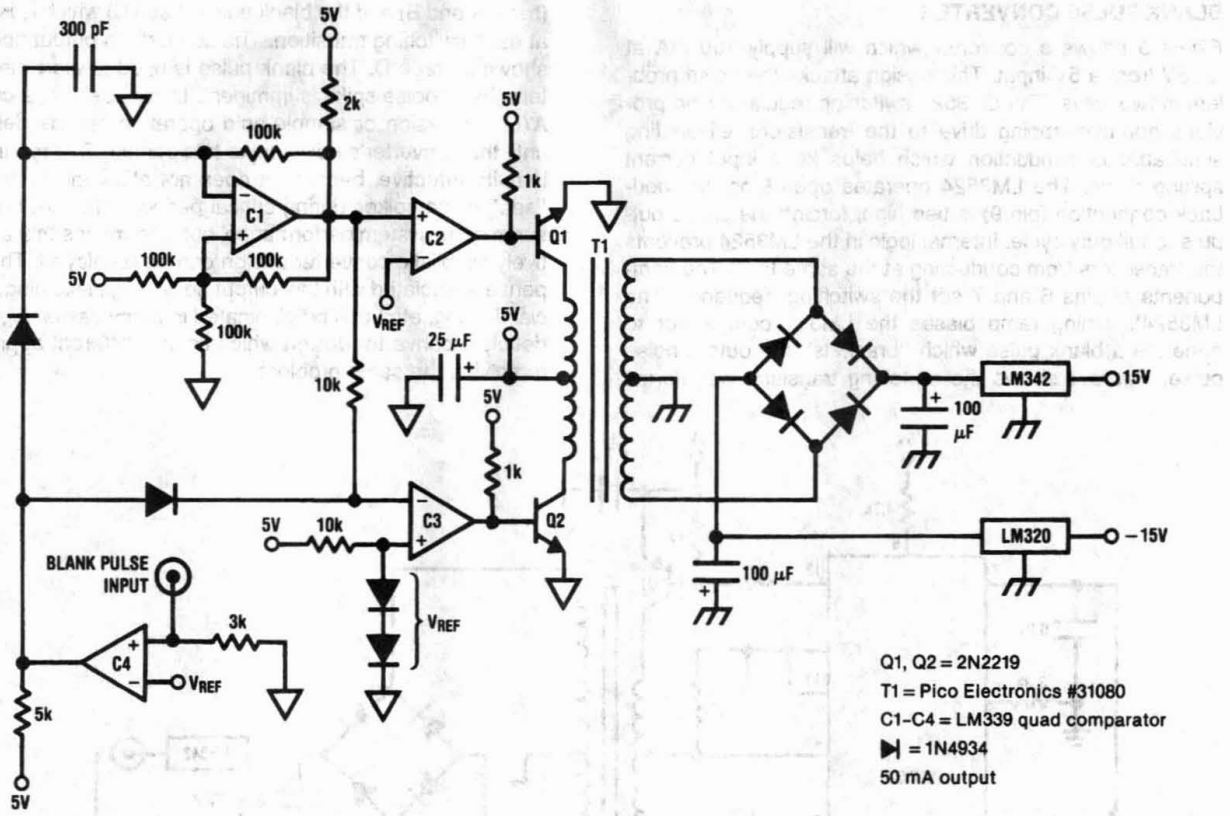
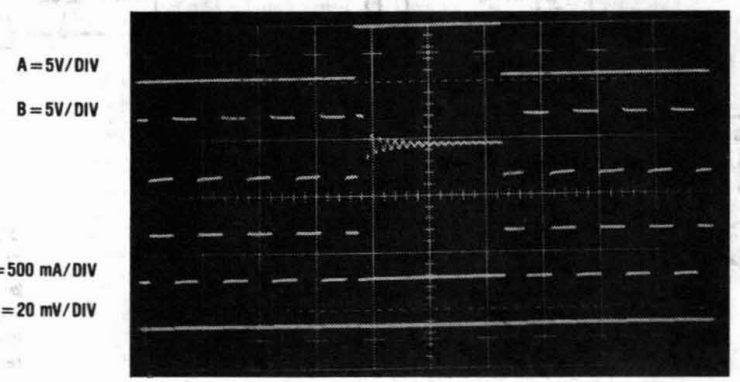


FIGURE 5

TL/H/7495–5



TL/H/7495–6

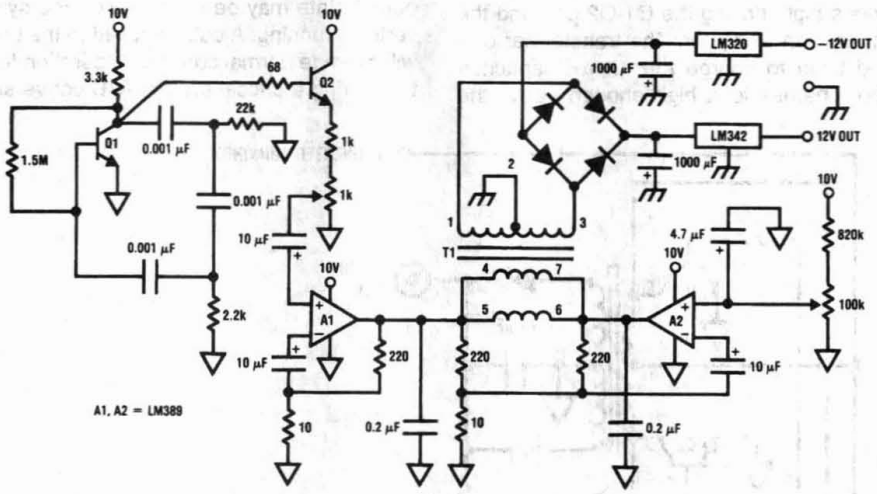
FIGURE 6

EXTERNALLY STROBED CONVERTER

In *Figure 5* the system controls the converter, instead of the converter issuing blank commands. This arrangement uses an LM339 quad comparator to provide the necessary drive to the converter. C1 functions as a clock which provides drive to C2 and C3. These comparators drive the transistors (trace B, *Figure 6* is Q1's collector voltage waveform, while trace C details its current) to provide power to the transformer. When a critical system operation must occur, an external blank pulse (trace A) is applied to C4. C4's output goes high, shutting off all transformer drive. Under these conditions, the transformer current ceases (note voltage ringing on turn-off in trace B) and output noise (trace D) virtually disappears because the output regulators are powered only by the 100 µF filter capacitors. The value of these capacitors will depend directly on the output load and the length of the blank pulse. If synchronization to the system is desired, a system-derived 20 kHz square wave may be applied at C1's negative input through 2k, after removing the 300 pF capacitor and the 100k feedback resistor. The low noise during the blank pulse period affords ideal conditions for sensitive system operations. Although this approach allows great flexibility, the amount of off time is limited by the storage capacity of the output filter capacitors. In most systems this is not a problem, but some cases may require a converter which supplies low noise outputs at 100% duty cycles.

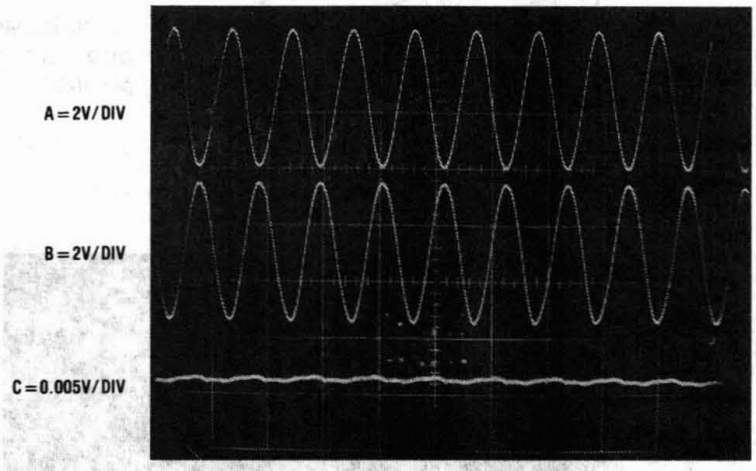
SINE WAVE DRIVEN CONVERTER

Figure 7 diagrams a converter which sacrifices the efficient saturated-switch mode of operation to achieve an inherently low noise output at a 100% duty cycle. In this converter, sine wave drive is used to power the transformer. Q1 functions as a 20 kHz phase shift oscillator with Q2 providing an emitter-followed output. A1 and A2 are used to drive the transformer in complementary-bridge fashion (traces A and B, *Figure 8*). The high current output capability of the amplifiers, in combination with the transformer's paralleled primaries, results in a high power transformer drive. The transformer output is rectified, filtered and regulated in the usual fashion. Because the sine wave drive contains little harmonic content and current spiking, output noise is well below 1 mV (trace C, *Figure 8*). To adjust this circuit, ground the wiper arm of the 1k potentiometer and adjust the 100k value for minimum power supply drain. Next, unground the 1k potentiometer wiper arm and adjust it so that both A1 and A2's outputs are as large as possible without clipping. This circuit yields a low noise output on a 100% available basis but efficiency degrades to about 30%. In relatively low power converters such as this one (e.g., 50 mA output current) this is often acceptable.



TL/H/7495–7

FIGURE 7

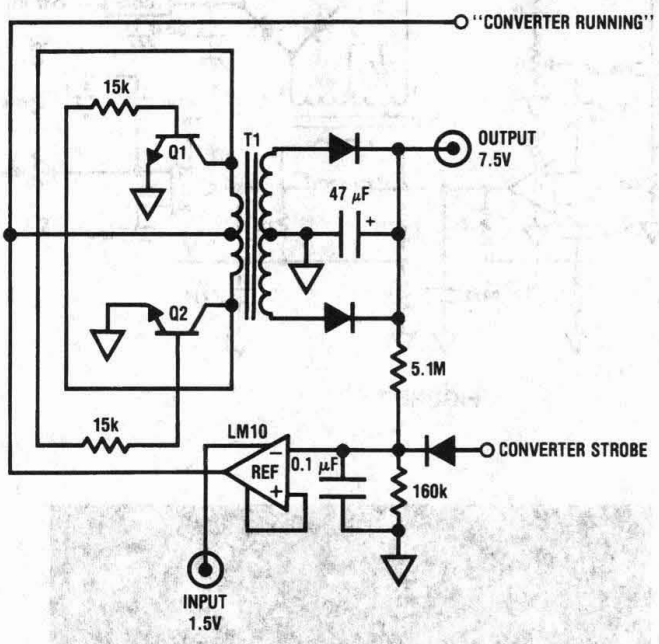


TL/H/7495–8

FIGURE 8

LOW POWER CONVERTER

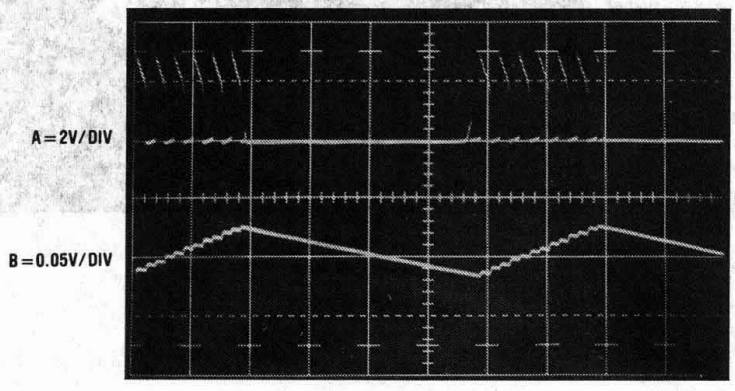
Figure 9 shows a converter which operates from very low power. This circuit will provide 7.5V output from a 1.5V D cell battery. With a 125 μA load current (typically 20 CMOS ICs) it will run for 3 months. It may be externally strobed off during periods where lowest output noise is desired and it also issues a "converter running" pulse. This circuit is unusual in that the amount of time required for Q1 and Q2 to drive the transformer is directly related to the load resistance. The converter's output voltage is sensed by an LM10 op amp reference IC, which compares the converter output to its own internal 200 mV reference via the 5.1M-160k voltage divider. Whenever the converter output is below 7.5V, the LM10 output goes high, driving the Q1-Q2 pair and the transformer which form an oscillator. The transformer output is rectified and used to charge the 47 μF capacitor. When the capacitor charges to a high enough value, the LM10 output goes low and oscillation ceases. Trace A, *Figure 10* shows the collector of Q1, while trace B shows the output voltage across the 47 μF capacitor (AC coupled). It can be seen that each time the output voltage falls a bit the LM10 drives the oscillator, forcing the voltage to rise until it is high enough to switch the LM10 output to its low stage. The frequency of this regulating action is determined by the load on the converter output. To prevent the converter from oscillating about the trip point, the 0.1 μF unit is used to provide hysteresis of response. Very low loading of the converter will result in almost no on time for the oscillator while large loads will force it to run almost constantly. Loop operating frequencies of 0.1 Hz to 40 Hz are typical. The LM10 output state may be used to alert the system that the converter is running. A pulse applied to the LM10 negative input will override normal converter operation for low noise operation during a critical system A/D conversion.



T1 = Stancor #PCT-39
Q1, Q2 = 2N2222A
▶| = 1N4148

TL/H/7495–9

FIGURE 9



TL/H/7495–10

FIGURE 10

Applications of the LM3524 Pulse-Width-Modulator

National Semiconductor
Application Note 292

The LM3524 Regulating Pulse-Width-Modulator is commonly used as the control element in switching regulator power supplies. This is in keeping with its intended purpose. Engineers closely associate this part with switching power supplies. Nevertheless, the flexible combination of elements (see box) within the LM3524 also allows it to be used in a number of other applications outside the power supply area. Because the device is inexpensive and operates off a single-sided supply, it can considerably reduce component count and circuit complexity in almost any application. The constant light intensity servo of *Figure 1* furnishes a good example.

CONSTANT LIGHT INTENSITY SERVO

The circuit of *Figure 1* uses a photodiode's output to control the intensity of a small light bulb. The constant intensity output of the light bulb is useful in a number of areas, including opto-electronic component evaluation and quality control of photographic film during manufacture. In this circuit, the photodiode pulls a current out of the LF356 summing junction, which is directly related to the amount of light that falls on the photodiode's surface. The LF356 output swings positive to maintain the summing junction at zero and represents the photodiode current in amplified voltage form. This potential is compared at the LM3524 to the voltage coming from the 2.5k "intensity" potentiometer wiper. A stable voltage for the "intensity" control is taken from the LM3524's internal five-volt regulator. The difference between the LF356 output and the "intensity" potentiometer output is amplified at a gain of about 70 dB, which is set by the 1 MΩ value at pin 9. The LM3524 output transistors are paralleled and provide drive to the 2N2219 switch transistor. The 5.6k and .01 μF values set the switching frequency at about 30 kHz. Because the LM3524 forms a switched mode feedback loop around the light bulb and photodiode, the average power delivered to the light bulb will be controlled by the photodiode output, which is directly proportional to the lamp's output. Frequency compensation for this feedback loop is provided by the .001 μF capacitor, which rolls off the loop gain at a 1 ms time constant. *Figure 2* shows the wave-

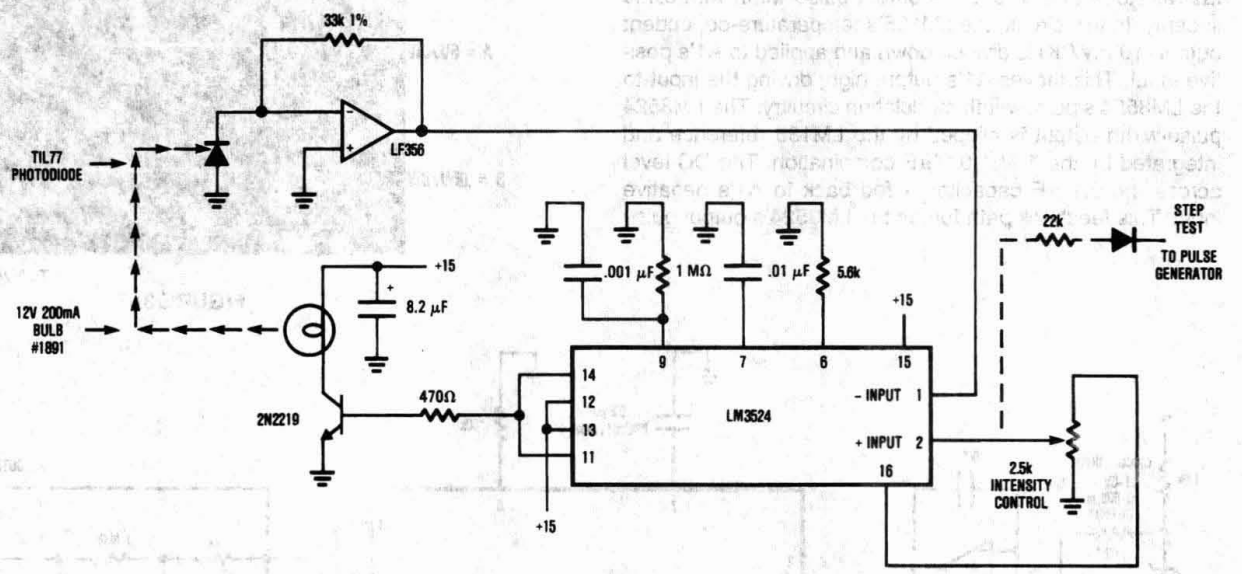


FIGURE 1

TL/H/6890–1

forms in the circuit. Trace A is the 2N2219 collector and trace B is the AC-coupled LF356 output. Each time the 2N2219 collector goes low, power is driven into the lamp. This is reflected in the positive going ramp at the LF356's output. When the 2N2219 goes off, the lamp cools. This is shown in the negative going relatively slow ramp in trace B. It is interesting to note that this indicates the bulb is willing to accept energy more quickly than it will give it up. *Figure 3a* elaborates on this. Here, trace A is the output of a pulse generator applied to the "step test" input and trace B is the AC-coupled LF356 output. When the pulse generator is high, the diode blocks its output, but when it goes low, current is drawn away from the "intensity" control wiper through the 22k resistor. This forces the servo to control bulb intensity at a lower value. This photo shows that the bulb servos to a higher output almost three times as fast as it takes to go to the lower output state, because the bulb more readily accepts energy than it gives it up. Surprisingly, at high intensity levels, the situation reverses because the increased incandescent state of the bulb makes it a relatively efficient radiator (*Figure 3b*).

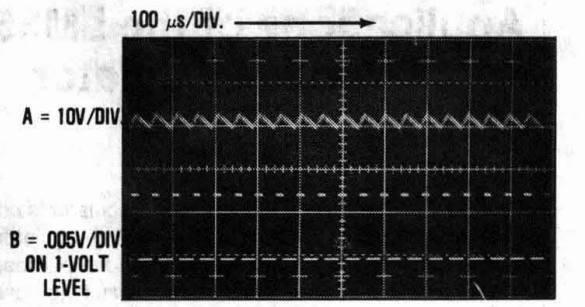


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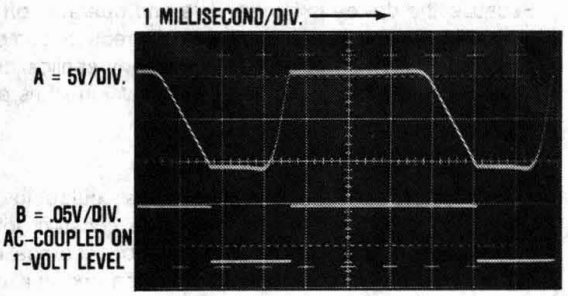
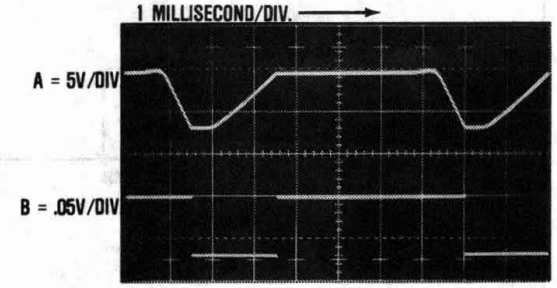
FIGURE 2



TL/H/6890–3

FIGURE 3a

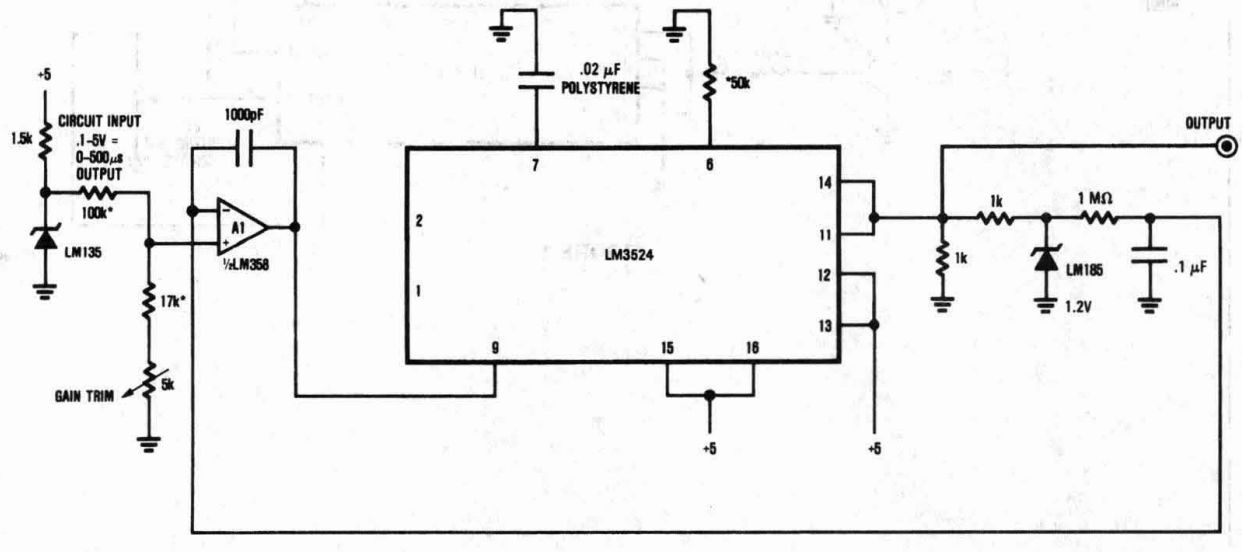


TL/H/6890–4

FIGURE 3b

TEMPERATURE-TO-PULSE-WIDTH CONVERTER

The circuit in *Figure 4* uses the LM3524 to convert the output of an LM135 temperature transducer into a pulse width which can be measured by a digital system, such as a microprocessor-controlled data acquisition system. Although this example uses the temperature transducer as the input, the circuit will convert any 0.1 to 5V input applied to the 100 kΩ resistor into a 0–500 ms output pulse width with 0.1% linearity. In this circuit, the LM135's temperature-dependent output (10 mV/°K) is divided down and applied to A1's positive input. This moves A1's output high, driving the input to the LM3524's pulse-width modulation circuitry. The LM3524 pulse-width output is clipped by the LM185 reference and integrated by the 1 MΩ-0.1 μF combination. The DC level across the 0.1 μF capacitor is fed back to A1's negative input. This feedback path forces the LM3524's output pulse



*Metal Film Resistor

TL/H/6890–5

FIGURE 4

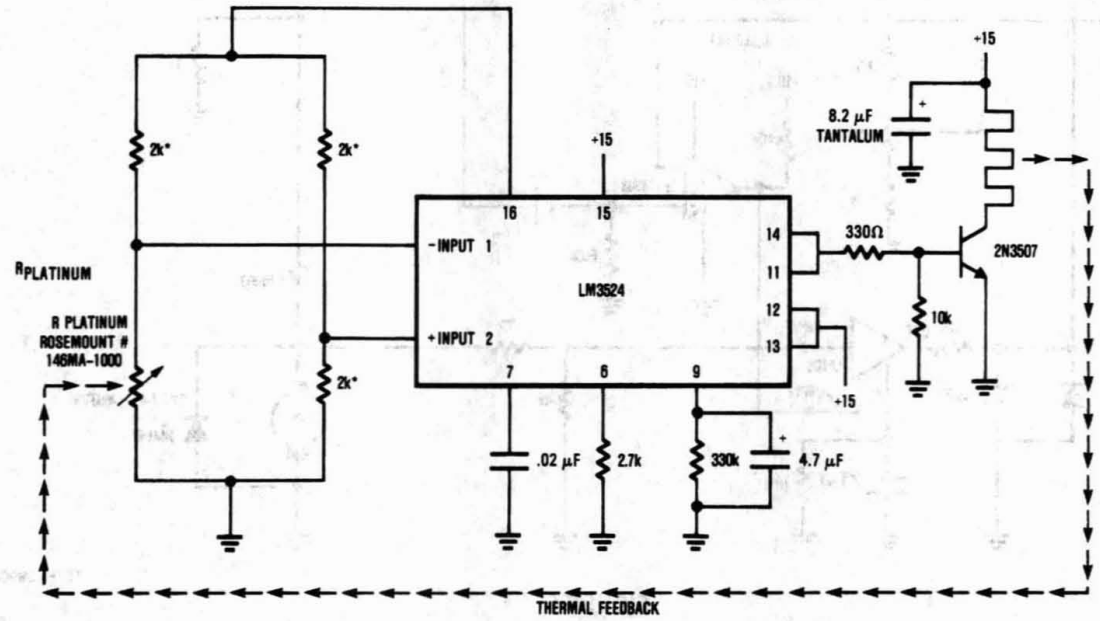
width to vary in a highly linear fashion according to the potential at A1's positive input. The overall temperature-to-pulse width scale factor is adjusted with the "gain trim" potentiometer. The 1000 pF capacitor provides stable loop compensation. A1, an LM358, allows voltages very close to ground to be sensed. This provides greater input range than the LM3524's input amplifier, which has a common mode range of 1.8–3.4V. The oscillator output pulse at pin 3 may be used to reset counters or other digital circuitry because it occurs just before the output pulse width begins.

RTD TEMPERATURE CONTROLLER

Figure 5 is another temperature circuit which uses the LM3524 to control the temperature of a small oven. Here, a platinum RTD is used as a sensor in a bridge circuit made up of the 2 kΩ resistors. When power is applied, the positive temperature coefficient platinum sensor is at a low value and the LM3524's positive input is at a higher potential than its negative input. This forces the output to go high, turning on the 2N3507 and driving the heater. When the servo point is reached, the duty cycle of the heater is reduced from 90% (full on) to whatever value is required to keep the oven at temperature. The 330k-4.7 μF combination at the internal input amplifier's output sets the servo gain at about 55 dB at 1 Hz, more than adequate for most thermal-control applications. The 0.02 μF-2.7k combination sets the pulse frequency at about 15 kHz, far above the 1 Hz pole of the servo gain. If the sensor is maintained in close thermal contact with the heater, this circuit will easily control to .1°C stability over widely varying ambients.

"SENSORLESS" MOTOR SPEED CONTROL

Figure 6 shows the LM3524 in an arrangement which controls the speed of a motor without requiring the usual tachometer or other speed pick-off. This circuit uses the back EMF of the motor to bias a feedback loop, which controls motor speed. When power is applied, the positive input of the LM3524 is at a higher potential than the negative input. Under these conditions, the output of the LM3524 is biased full on (90% duty cycle). The output transistors, paralleled in the common emitter configuration, drive the 2N5023 and the motor turns. (LM3524 output is waveform A, *Figure 7*; waveform B is the 2N5023 collector.) The LM3524 output pulse is also used to drive a 1000 pF-500 kΩ differentiator network whose output is compared to the LM3524's internal 5V reference. The result is a delayed pulse (*Figure 7*, waveform D), which is used to trigger an LF398 sample-hold IC. As the waveforms show, the sample-hold is gated high (ON) just as the 2N5023 collector stops supplying current to the



*TRW Type MAR-60 .1%

TL/H/6890–6

FIGURE 5

motor. At this instant, the motor coils produce a flyback pulse, which is damped by the shunt diode. (Motor waveform is *Figure 7*, trace C). After the flyback pulse decays, the back EMF of the motor remains. This voltage is "remembered" by the sample-hold IC when the sample trigger pulse ceases and is used to complete the speed control loop back at the LM3524 input. The 10k-4k divider at the motor output insures the LF398's output will always be within the common range of the LM3524's input. The 10k-1 μF combination provides filtering during the time the LF398 is sampling. The diode associated with this time constant prevents any possible LF398 negative output from damaging the LM3524. The 10 MΩ resistor paralleling the 0.01 μF sampling capacitor prevents the servo from "hanging up" if this capacitor somehow manages to charge above the motor's back EMF value. The 39k-100 μF pair sets the loop frequency response. The maximum pulse-width-modulator duty cycle is clamped by the 2k-2k divider and diode at 80%, thus avoiding overshoot and aiding transient response at turn-on and during large positive step changes. The 60k-0.1 μF values at pins 6 and 7 set the pulse modulation frequency at 300 Hz.

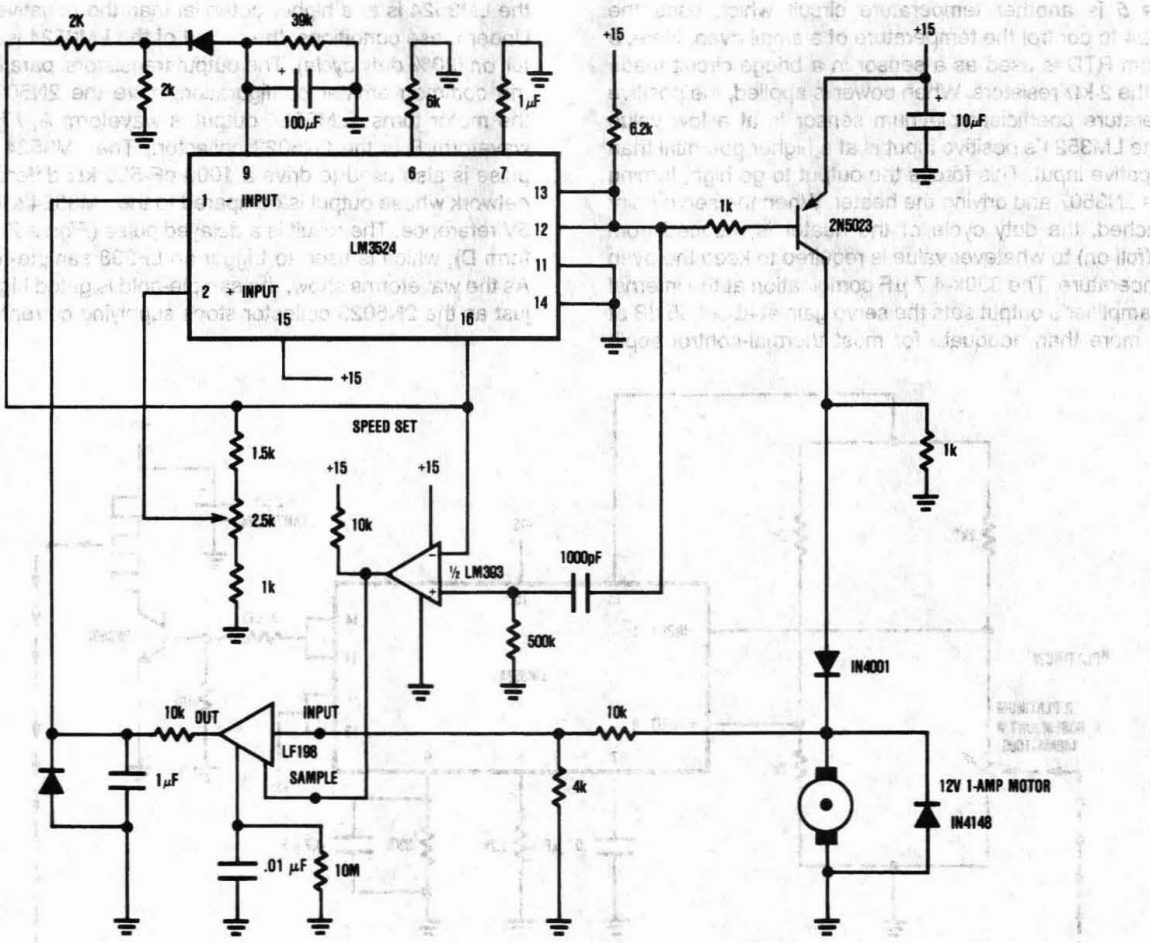


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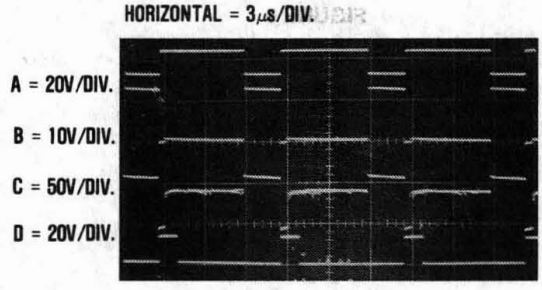
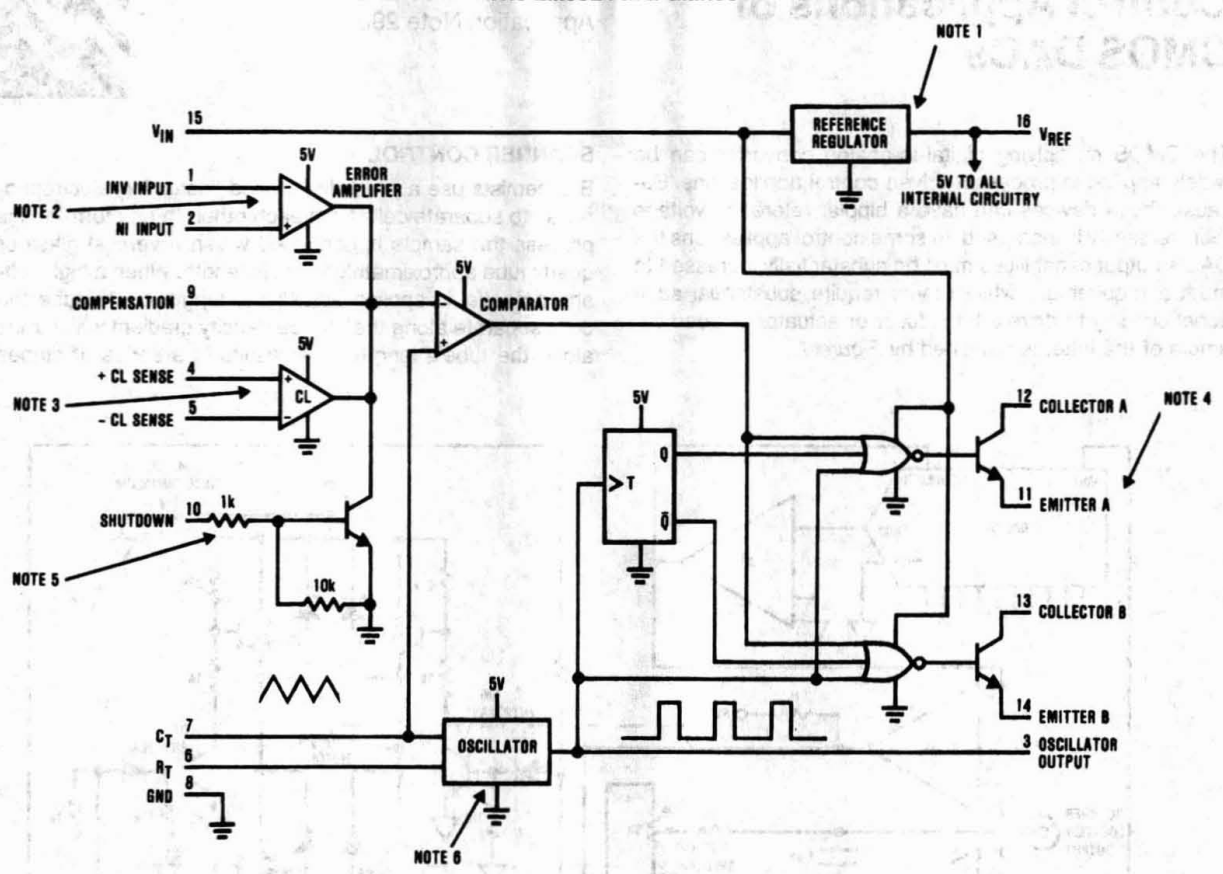
FIGURE 6



TL/H/6890–8

FIGURE 7

The LM3524 at a Glance



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Note 1: 5V 50 mA regulator available to user.

Note 2: Transconductance diff. input amplifier. Gains from 40–80 dB available by resistor loading of output. 1.8–3.4V common mode input range.

Note 3: Over current sense comparator −0.7 to 1V common mode input range.

Note 4: Output transistors switch out of phase and may be paralleled. Up to 100 mA maximum output current.

Note 5: Transistor may be used to strobe LM3524 into an off state at its outputs.

Note 6: Oscillator typically frequency programmable for up to 100 kHz.

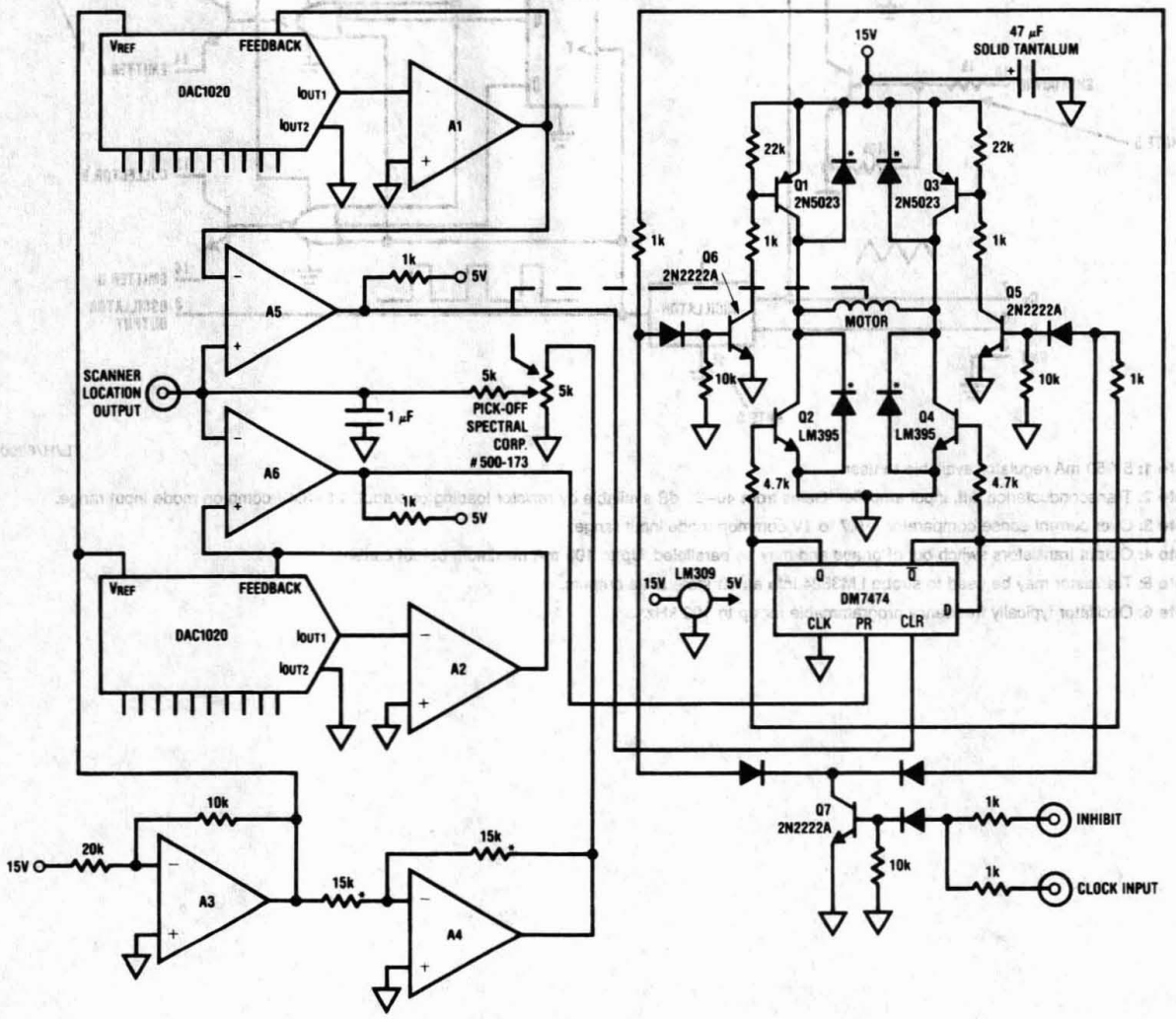
Control Applications of CMOS DACs

National Semiconductor
Application Note 293

The CMOS multiplying digital-to-analog converter can be widely applied in processor-driven control applications. Because these devices can have a bipolar reference voltage their versatility is increased. In some control applications the DAC's output capabilities must be substantially increased to meet a requirement while others require substantial additional circuitry to drive a transducer or actuator. A good example of the latter is furnished by *Figure 1*.

SCANNER CONTROL

Biochemists use a procedure called "scanning electrophoresis" to separate cells from each other. In one form of this process the sample is contained within a vertical glass or quartz tube approximately 1 foot in length. When a high voltage potential is applied across the length of the tube the cells separate along the charge density gradient which runs along the tube's length. This results in a series of stripes



= 1N4148
= 1N4001
= 1% metal film, match 0.5%

Motor = Motordyne, Inc. #1150-1

A1, A2 = LF356

A3, A4 = LF353 dual

A5, A6 = LM393 dual

FIGURE 1

TL/H/5636–1

or bands within the tube as the individual cells, under the influence of the charge gradient, collect together. When separation is complete, the tube is mechanically scanned along its length by a photometer for optical density characteristics of each band. This information yields useful biochemical information to the experimenter. The scanner must be fully programmable so that it can be run between any two limits at a variety of speeds. In *Figure 1* the two DAC1020 D/A converters establish the limits of the scan. The 5k pick-off potentiometer furnishes scanner location information and the motor drives the scanner (via a gear-train). A5 and A6 are comparators, one of whose outputs goes low when either the high limit (A6 and its associated DAC) or low limit (A5 and its associated DAC) is exceeded. A1 and A2 furnish voltage outputs from the current output of the DACs. A3 and A4 are used to provide suitable reference voltages for the 5k pick-off potentiometer and the DAC reference inputs.

The DM7474 flip-flop is configured in a set-reset arrangement which changes output state each time either A5 or A6 goes low. When the lower limit of the scan is reached, A5 goes low, setting the DM7474's Q output too high. This turns on Q2, Q5 and Q3 resulting in current flow through the motor from Q3 to Q2. This forces the scanner to run towards its high limit. When this limit is reached, A6 goes low and the flip-flop changes state. This turns off the Q2, Q5, Q3 combination and the Q4, Q6, Q1 trio come on, forcing current through the motor in the opposite direction via the Q1-Q4 path. This causes the motor to reverse and proceed toward the lower limit. Q7 is driven by a width-modulated pulse train from the processor which is used to control the scanner's speed via Q5 and Q6. The diodes across Q1, Q2, Q3 and Q4 provide motor spike suppression and the internal current limiting in the LM395s (Q2-Q4) assures short circuit protection.

HIGH VOLTAGE OUTPUT FOR ATE

Testing high voltage components with automatic test equipment (ATE) is often inconvenient because a source of stable, controllable high voltage is required. Adding this capability to a piece of equipment can be expensive and time consuming if standard techniques are used. In *Figure 2* a circuit is shown which has been employed in the testing

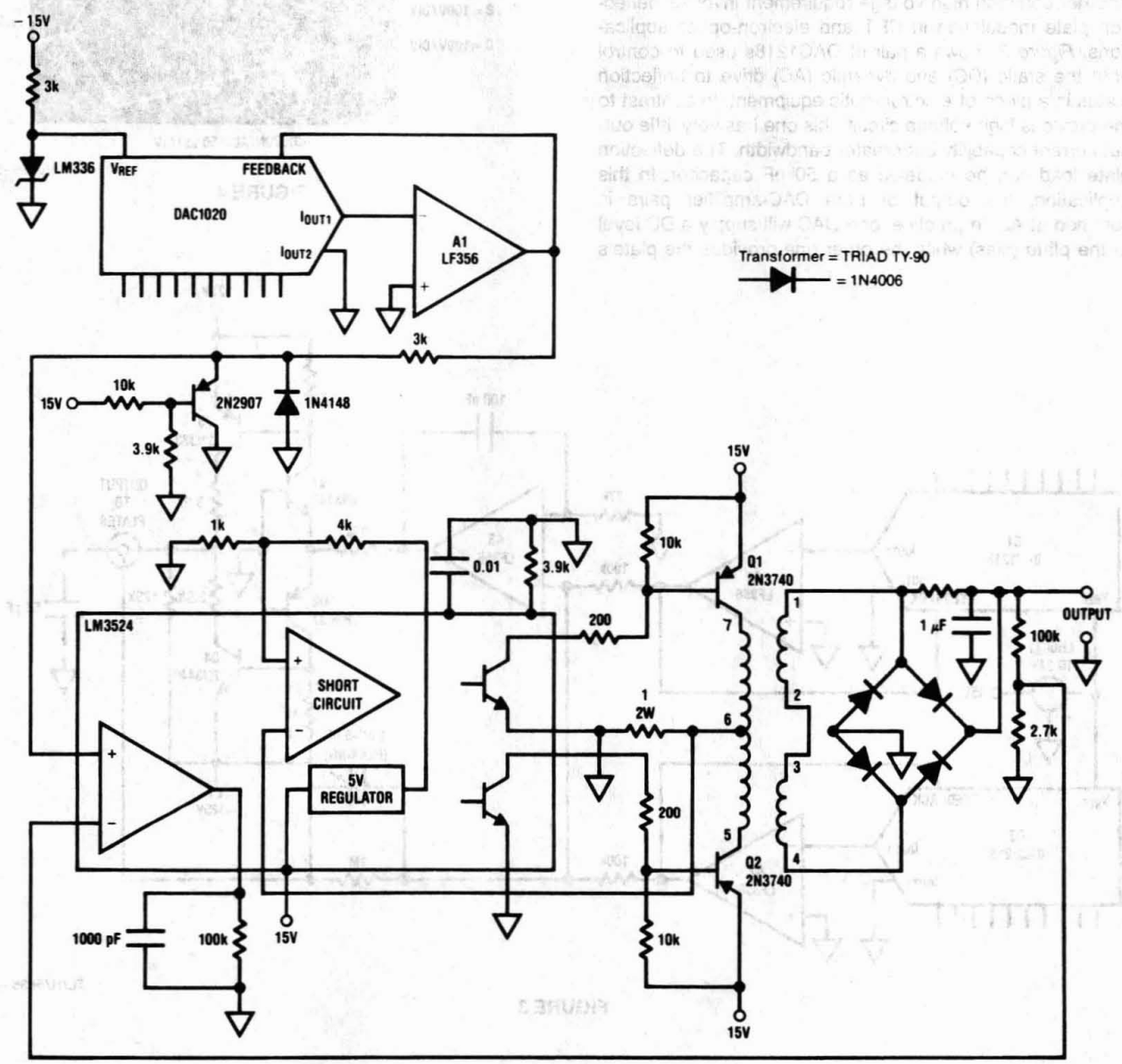


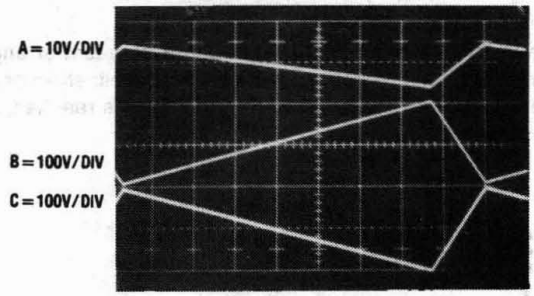
FIGURE 2

TL/H/5636–2

of high voltage transistors and zeners as well as fuse link blowing in PROMs. In this circuit, a high voltage output is developed by using a Toroidal DC-DC converter within a DAC-controlled pulse-width modulated feedback loop to obtain high voltage. The DAC1020 in conjunction with A1 supplies a setpoint to the LM3524 regulating pulse-width modulator. This set point needs to be within the LM3524's common mode input voltage range of 1.8V to 3.5V. The LM3524's outputs are used to drive the TY-90 toroid via Q1 and Q2. The high voltage square-wave transformer output is rectified and filtered and divided down by the 100k-2.7k string. This potential is fed back to the LM3524, completing a loop. Loop gain and frequency compensation are set by the 1000 pF-100k parallel combination, and the 1Ω resistor at pin 6 of the transformer is used to sense current for short circuit protection. Although the update rate into the DAC can be very fast, the 20 kHz switching of the transformer and the loop time constants determine the available bandwidth at the circuit's output. In practice, a full output sine wave swing of 100V into 1000Ω is available at 250 Hz.

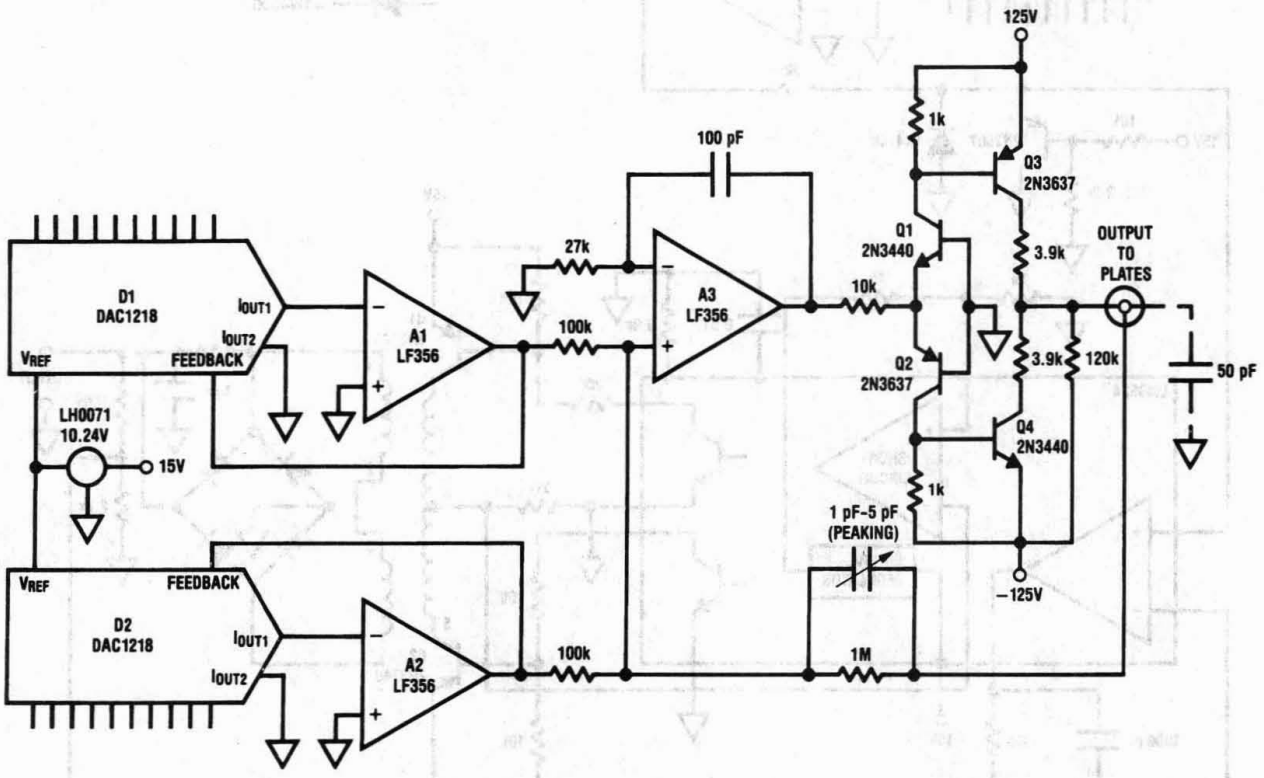
PLATE-DRIVING DEFLECTION AMPLIFIER

Another common high voltage requirement involves deflection plate modulation in CRT and electron-optics applications. *Figure 3* shows a pair of DAC1218s used to control both the static (DC) and dynamic (AC) drive to deflection plates in a piece of electron-optic equipment. In contrast to the previous high voltage circuit, this one has very little output current capability but greater bandwidth. The deflection plate load can be modeled as a 50 pF capacitor. In this application, the output of both DAC-amplifier pairs is summed at A3. In practice, one DAC will supply a DC level to the plate (bias) while the other one provides the plate's AC signal, typically a ramp. The high voltage plate drive is furnished by the Q1, Q2, Q3, Q4 configuration which is a complementary common-base-driven common-emitter output stage. Because the output current requirements are low, the usual crossover distortion problems may be avoided by returning the circuit's output to negative supply via the 120 kΩ resistor. This eliminates notch compensation circuitry and results in a simplified design. Because the high voltage stage inverts, overall negative feedback is achieved by returning the 1 MΩ feedback resistor to A3's positive input. The point now becomes the summing junction for both DAC-driven inputs and the feedback signal. The output of this circuit is clean and quick, as shown in *Figure 4.* In this figure, 2 complete DAC-driven amplifiers were used to produce the traces. Trace A is the output of A1, while the complementary high voltage outputs are shown in B and C.



TL/H/5636–3

FIGURE 4



TL/H/5636–4

FIGURE 3

TEMPERATURE LIMIT CONTROLLER

Certain biochemical reactions occur only within very specific temperature limits. The behavior of these reactions within and at the edges of these limits is of interest to biochemists. In order to study these reactions, a special temperature control scheme is required. To meet this requirement, the circuit of *Figure 5* has been employed. In this circuit A1, A3, A4 and A5 comprise a simple pulse-width modulating temperature controller. A4 is an integrator that generates a ramp which is periodically reset to zero by the 10 kHz clock pulse. This ramp is compared to A3 output by A5, which biased the LM395 switch to control the heater. A3's output will be determined by the difference between the temperature setpoint current through the 22.6 kΩ resistor and the current driven by the LM135 temperature sensor through the 10 kΩ resistor. Thermal feedback from the heater to the LM135 completes the loop. The 10M-1 μF values at A3 set loop response at 0.1 Hz.

Up to this point, the circuit functions as a fixed point temperature controller to provide a stable thermal baseline. To meet the application's requirement, however, the DAC1218 is driven by a slow digitally-coded triangle waveform. The DAC's output is fed to A2, whose output drives the 2 MΩ summing resistor. This causes the controller setpoint to vary slowly and predictably through the desired temperature excursion. This characteristic is observable on a strip-chart recording of the oven's temperature (*Figure 6*) over many hours.

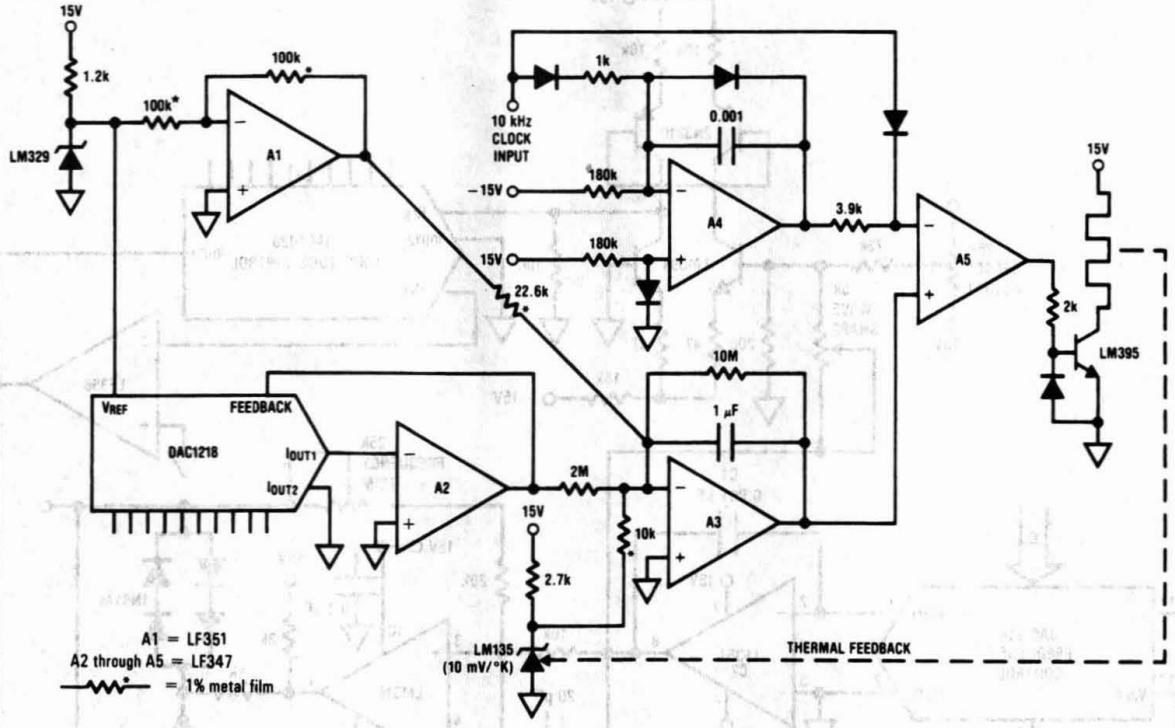
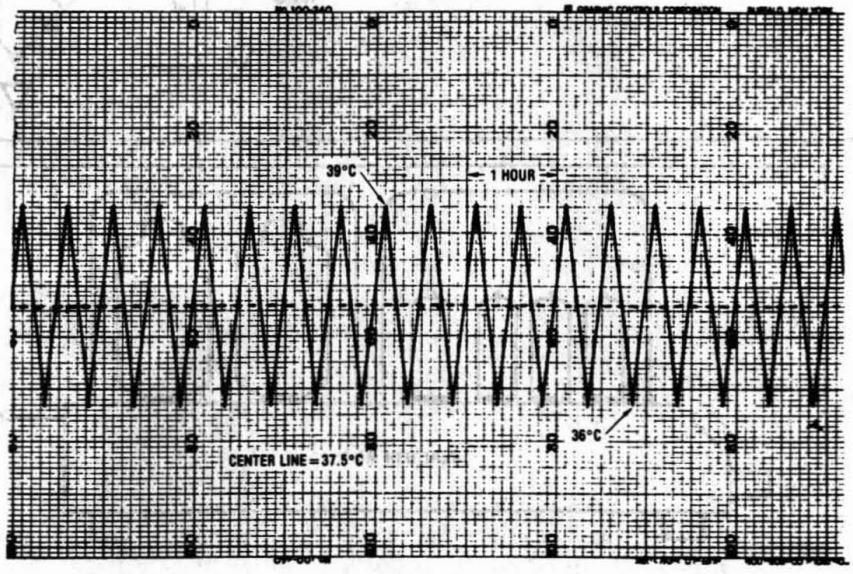


FIGURE 5

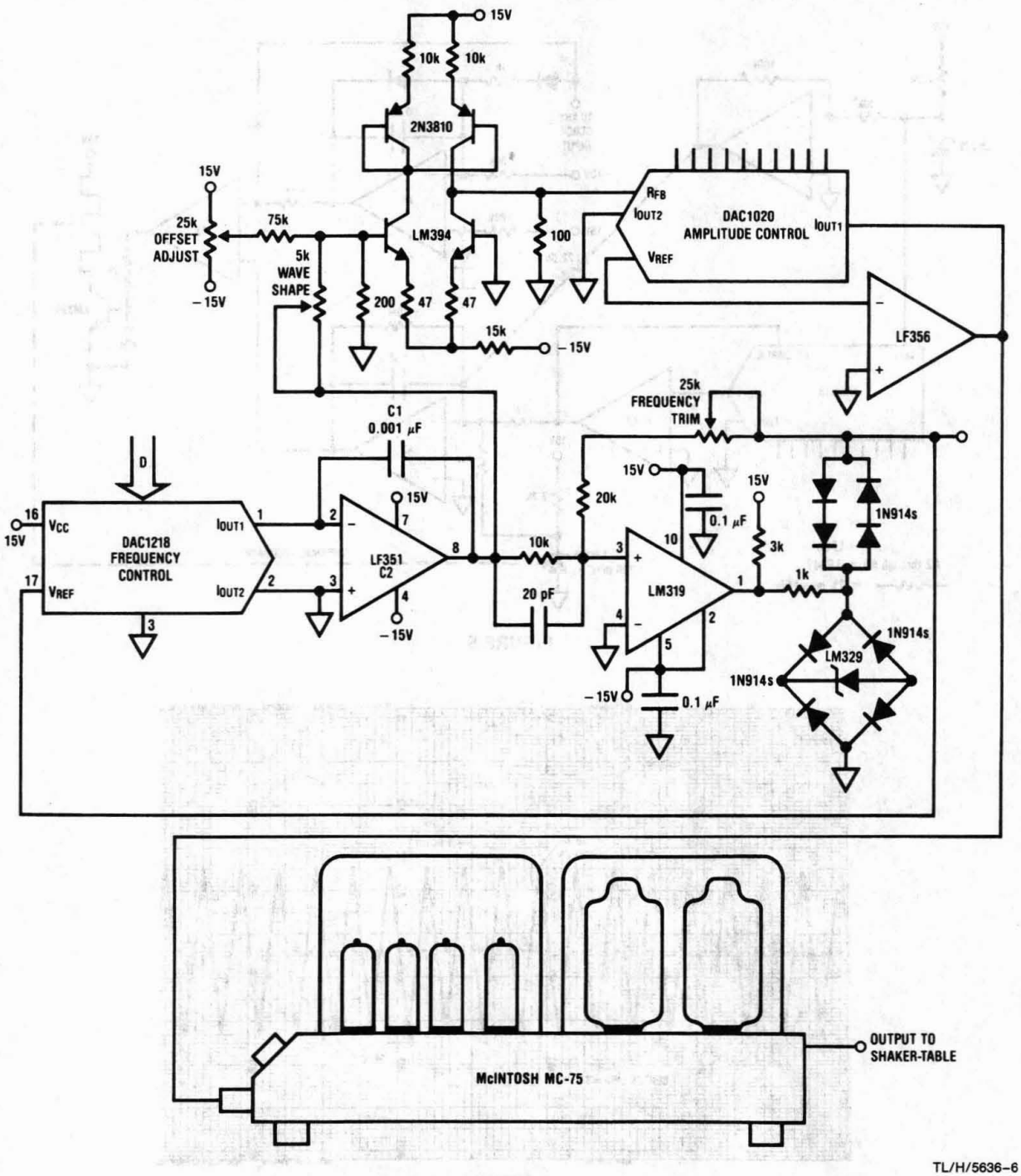


TL/H/5636–5

FIGURE 6

PROCESSOR CONTROLLED SHAKER-TABLE DRIVE

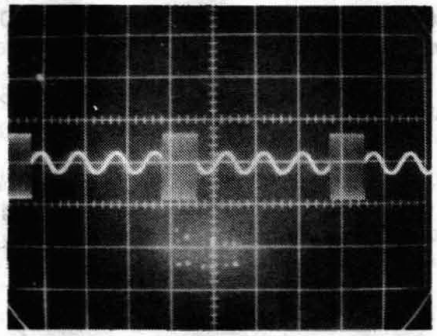
Shaker-tables are frequently employed to test finished assemblies for vibration induced failures under various conditions of frequency and amplitude. It is often desired to simulate vibration patterns which can greatly vary with duration, frequency and amplitude. In addition, it is useful to be able to vary both amplitude and frequency with precise control over wide dynamic ranges so that narrow resonances in the assembly under test may be observed. The circuit of *Figure 7* provides these capabilities. The DAC1218 is used to drive the LF351 integrator. The LF351's output ramps until the current through the 10k resistor just balances the current through the 20k resistor at pin 3 of the LM319 comparator. At this point the comparator changes state, forcing the zener diode bridge and associated series diode to put an equal but opposite polarity reference voltage. This potential is used as the DAC's reference input as well as the feedback signal to the LM319 "+" input. In this fashion, the integrator output forms a triangle waveform whose output is centered around ground. The DAC input coding controls the frequency, which may vary from 1 Hz to 30 kHz. Calibration is accomplished with the "frequency trim" potentiometer. The triangle waveform is shaped by the 2N3810-LM394 configuration which relies on the logarithmic relationship between V_{BE} and collector current in the LM394 to smooth the triangle into a sine wave. The two potentiometers associated with the



TL/H/5636–6

FIGURE 7

shaper are adjusted for minimum indicated distortion on a distortion analyzer. The DAC1020 and the LF356 are arranged in a DAC-controlled gain configuration which allows the amplitude of the sine wave to be varied over a range from millivolts to volts at the LF356 output. The low input impedance and high inductance of a typical shaker-table presents a difficult load for a solid state amplifier to drive, and vacuum tube amplifiers are frequently employed to avoid output stage failures. In this example, the amplifier specified is a well-known favorite for the job because its transformer-isolated input is immune to the inductive flyback spikes a shaker-table can generate. *Figure 8* shows the output waveform when both DACs are simultaneously updated. The output waveform changes in frequency and amplitude with essentially instantaneous response.



TL/H/5636–7

FIGURE 8

Special Sample and Hold Techniques

National Semiconductor
Application Note 294

Although standard devices (e.g., the LF398) fill most sample and hold requirements, situations often arise which call for special capabilities. Extended hold times, rapid acquisition and reduced hold step are areas which require special circuit techniques to achieve good results. The most common requirement is for extended hold time. The circuit of *Figure 1* addresses this issue.

EXTENDED HOLD TIME SAMPLE AND HOLD

In this circuit, extended hole time is achieved by "stacking" two sample and hold circuits in a chain. In addition, rapid acquisition time is retained by use of a feed-forward path. When a sample command is applied to the circuit (trace A, *Figure 2*), A1 acquires the input very rapidly because its 0.002 μF hold capacitor can charge very quickly. The sample command is also used to trigger the DM74C221 one-shot (trace B, *Figure 2*), which turns on the FET switch, S1. In this fashion, A1's output is fed immediately to the A3 output buffer. During the time the one-shot is high, A2 acquires the value of A1's output. When the one-shot drops low, S1 opens, disconnecting A1's output from A3's input. At this point A2's output is allowed to bias A3's input and the circuit output does not change from A1's initial sampled value. Trace C details what happens when S1 opens. A small glitch, due to charge transfer through the FET, appears but the steady state output value does not change. This circuit will acquire a 10V step in 10 μs to 0.01% with a droop rate of just 30 μV/second.

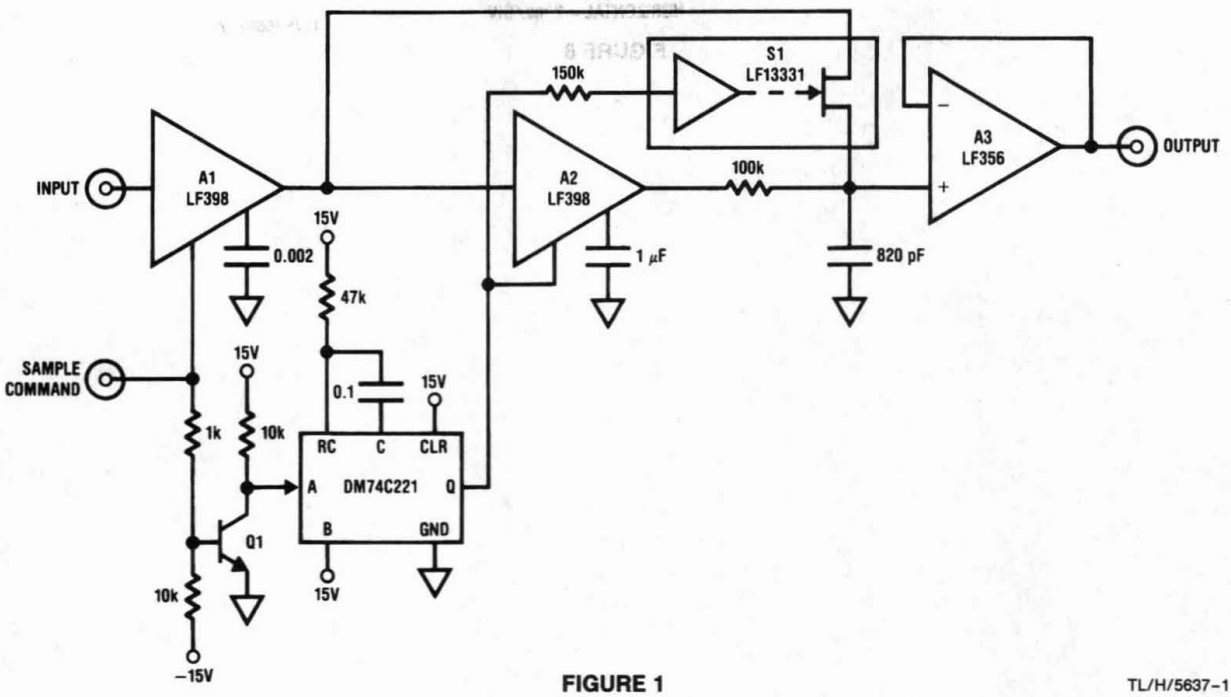


FIGURE 1

TL/H/5637–1

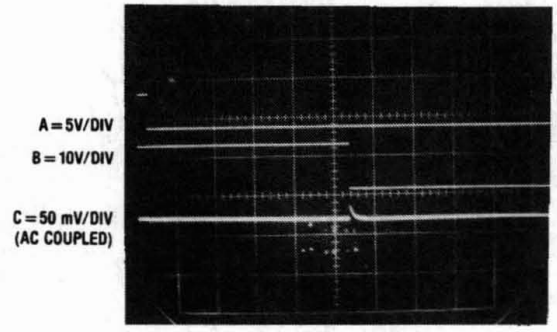


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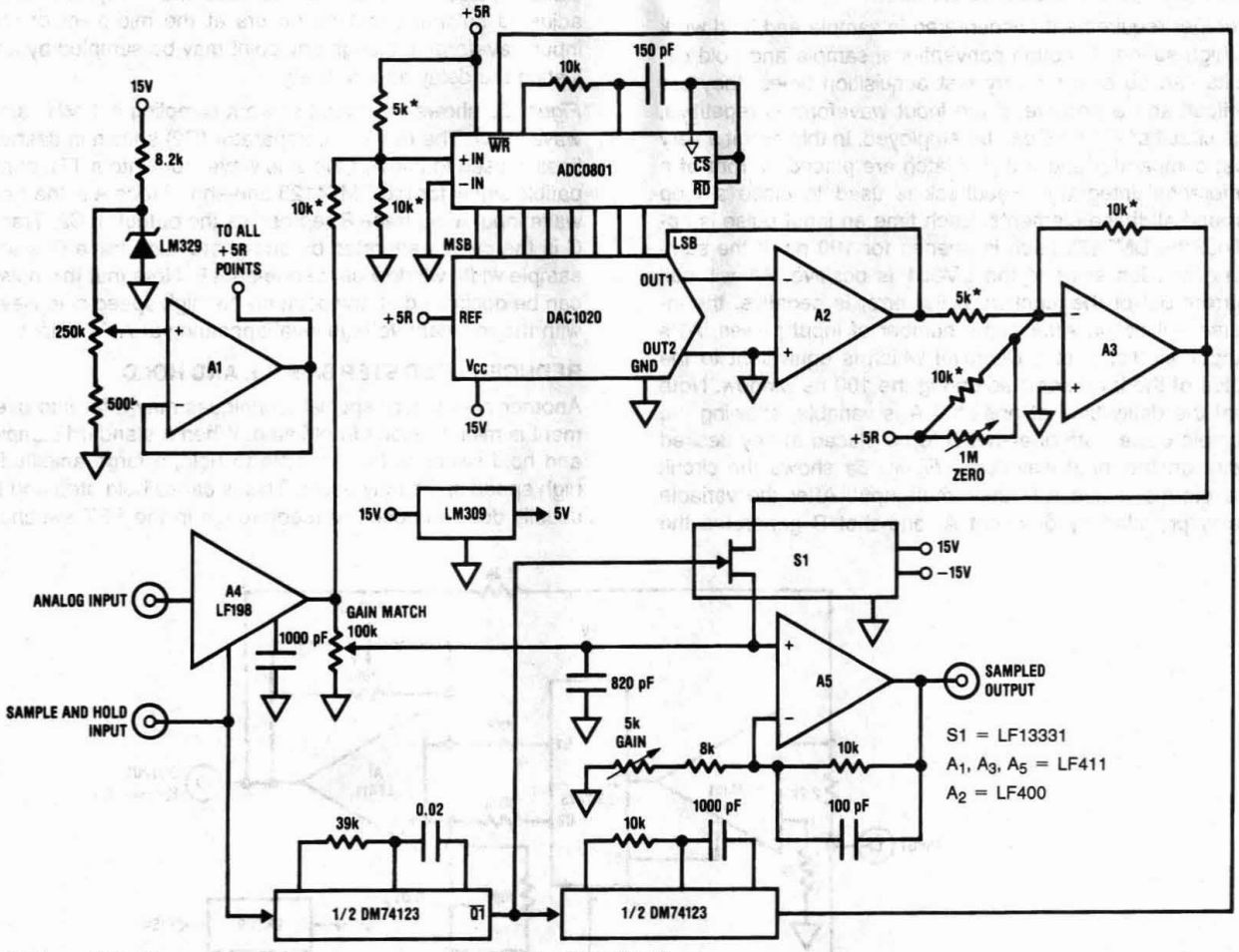
FIGURE 2



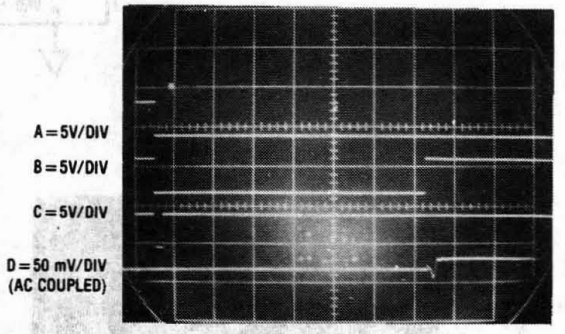
*Ratio match 0.1%

FIGURE 3

TL/H/5637–3

INFINITE HOLD SAMPLE AND HOLD

Figure 3 details a circuit which extends the hold time to infinity with an acquisition time of 10 μs. Once a signal has been acquired, this circuit will hold its output with no droop for as long as is desired. If this arrangement, A4's divided down output is fed directly to the circuit output via A5 as soon as a sample command (trace A, *Figure 4)* is applied. The sample command is also used to trigger the DM74123 one-shots. The first one-shot (trace B, *Figure 4)* is used to bias the FET switch OFF during the time it is low. The second one-shot (trace C, *Figure 4)* delivers a pulse to the ADC0801 A/D converter which then performs an A/D conversion on A4's output. The DAC1020, in combination with A2 and A3, converts the A/D output back to a voltage. The A/D/A process requires about 100 μs. When the one-shot (trace B) times out, its output goes high, closing the FET switch. This action effectively connects A3's output to A5 while disconnecting A4's output. In this manner, the circuit output will remain at the DC level that was originally determined by A4's sampling action. Because the sampled value is stored digitally, no droop error can occur. The precision resistors noted in the circuit provide offsetting capability for the unipolar A/D output so that a −10V to +10V input range can be accommodated. To calibrate this circuit, apply 10V to the input and drive the sample command input with a pulse generator. Adjust the gain match potentiometer so that minimum "hop" occurs at the circuit output when S1 closes. Next, ground the input and adjust the zero potentiometer for 0V output. Finally, apply 10V to the input and adjust the gain trim for a precise 10V circuit output. Once adjusted, this circuit will hold a sampled input to within the 8-bit quantization level of the A/D converter over a full range of +10V to −10V. Trace D, *Figure 4* shows the circuit output in great detail. The small glitch is due to parasitic capacitance in the FET switch, while the level shift is caused by quantization in the A/D. An A/D with higher resolution could be used to minimize this effect.



A, B, C HORIZONTAL = 20 μs/DIV
D HORIZONTAL = 2 μs/DIV

TL/H/5637–4

FIGURE 4

HIGH SPEED SAMPLE AND HOLD

Another requirement encountered in sample and hold work is high speed. Although conventional sample and hold circuits can be built for very fast acquisition times, they are difficult and expensive. If the input waveform is repetitive, the circuit of *Figure 5* can be employed. In this circuit a very fast comparator and a digital latch are placed in front of a differential integrator. Feedback is used to close a loop around all these elements. Each time an input pulse is applied, the DM7475 latch is opened for 100 ns. If the summing junction error at the LM361 is positive, A1 will pull current out of the junction. If the error is negative, the inverse will occur. After some number of input pulses, A1's output will settle at a DC level which is equivalent to the value of the level sampled during the 100 ns window. Note that the delay time of one-shot A is variable, allowing the sample pulse from one-shot B to be placed at any desired point on the input waveform. *Figure 6a* shows the circuit waveforms. Trace A is the circuit input. After the variable delay provided by one-shot A, one-shot B generates the sample pulse (trace B). In this case the delay has been adjusted so that sampling occurs at the mid-point of the input waveform, although any point may be sampled by adjusting the delay appropriately.

Figure 6b shows the circuit at work sampling a 1 MHz sine wave input. The optional comparator (C2) shown in dashed lines is used to convert the sine wave input into a TTL compatible signal for the DM74123 one-shot. Trace A is the sine wave input while trace B represents the output of C2. Trace C is the delay generated by one-shot A and trace D is the sample width window out of one-shot B. Note that this pulse can be positioned at any point on the high speed sine wave with the resultant voltage level appearing at A1's output.

REDUCED HOLD STEP SAMPLE AND HOLD

Another area where special techniques may offer improvement is minimization of hold step. When a standard sample and hold switches from sample to hold, a large amplitude high speed spike may occur. This is called hold step and is usually due to capacitive feedthrough in the FET switches

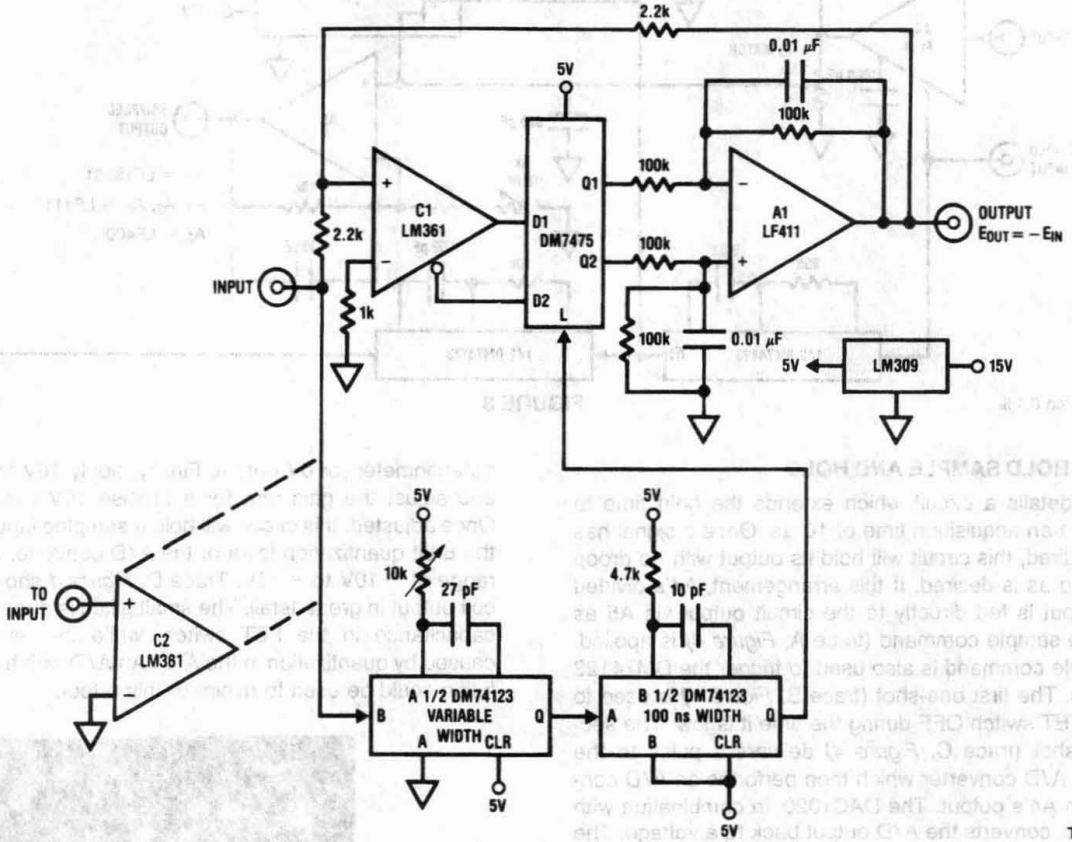
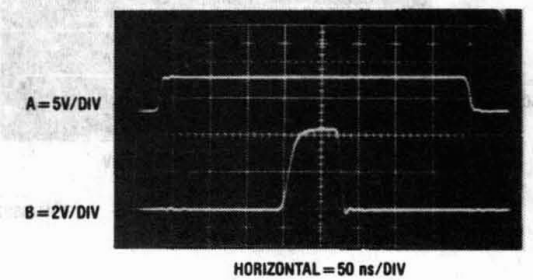
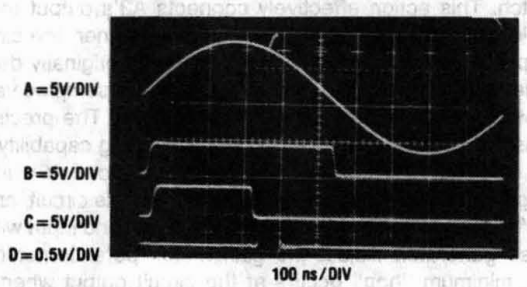


FIGURE 5



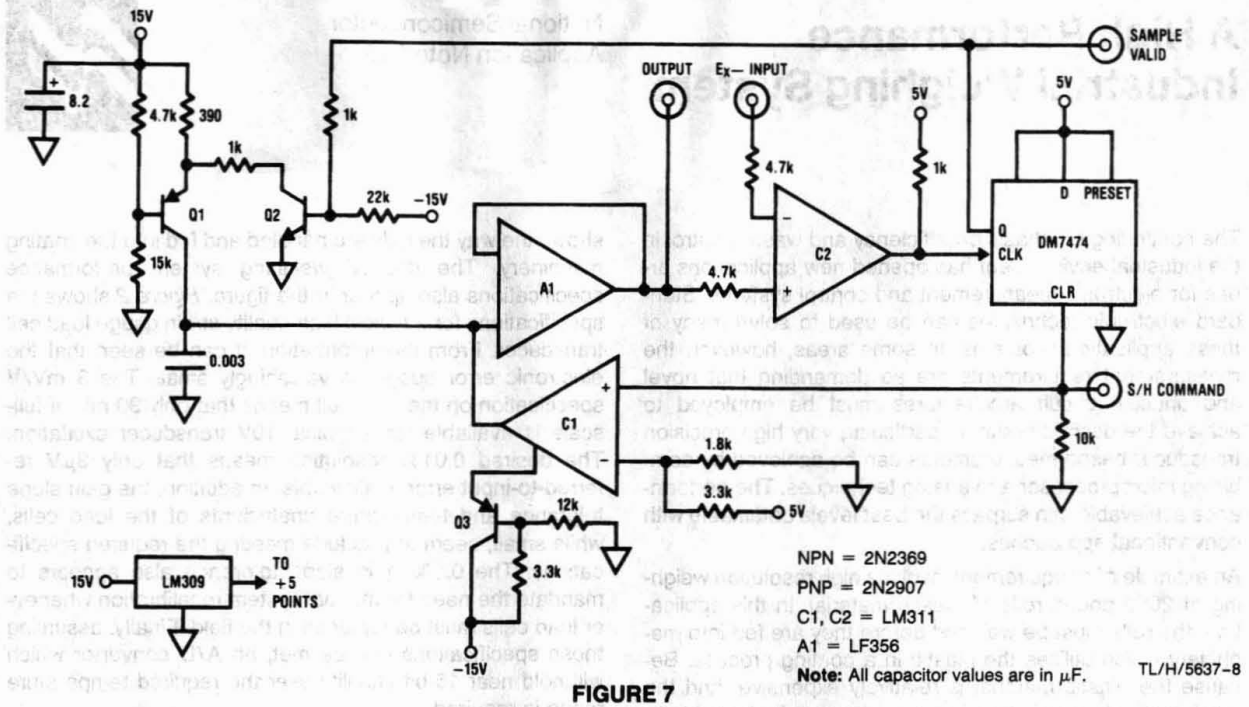
TL/H/5637–6

FIGURE 6a



TL/H/5637–7

FIGURE 6b



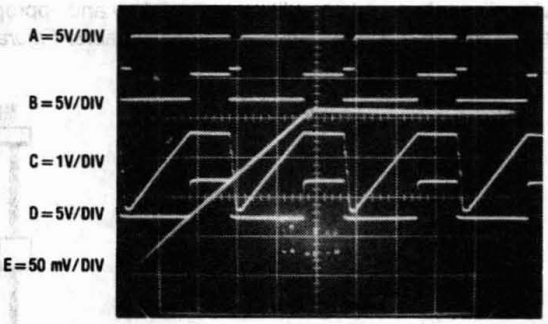
TL/H/5637–8

FIGURE 7

used in the circuit. The circuit of *Figure 7* greatly reduces hold step by using an unusual approach to the sample and hold function. In this circuit sampling is started when the sample and hold command input goes low (trace A,*Figure 8*). This action also sets the DM7474 flip-flop low (trace B, *Figure 8*). At the same time, C1's output clamps at Q3's emitter potential of −12V (trace C, *Figure 8*). When the sample pulse returns high, C1's output floats high and the 0.003 μF capacitor is linearly charged by current source Q1. This ramp is followed by A1, which feeds C2. When the ramp potential equals the circuit's input voltage, C2's output (trace D, *Figure 8*) goes high, setting the flip-flop high. This turns on Q2, very quickly cutting off the Q1 current source. This causes the ramp to stop and sit at the same potential at the circuit's input. The hold step generated when the circuit goes into hold mode (e.g., when the flip-flop output goes high) is quite small. Trace E, a greatly enlarged version of trace C, details this. Note the hold step is less than 10 mV high and only 30 ns in duration. Acquisition time for this circuit is directly dependent on the input value, at a rate of 5 μs/V.

REFERENCE

One IC Makes Precision Analog Sampler, S. Dendinger; EDN May 20, 1977.



A, B, C, D HORIZONTAL = 5 μs/DIV
E HORIZONTAL = 100 ns/DIV

TL/H/5637–9

FIGURE 8

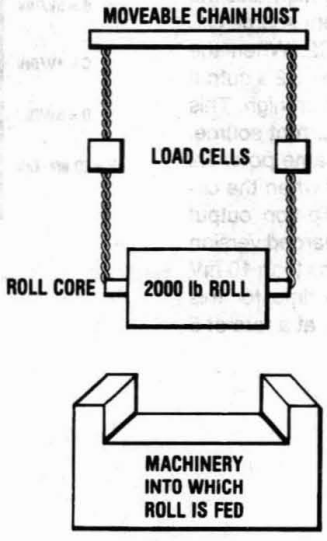
A High Performance Industrial Weighing System

National Semiconductor
Application Note 295

The continuing emphasis on efficiency and waste control in the industrial environment has opened new applications areas for electronic measurement and control systems. Standard electronic techniques can be used to solve many of these application problems. In some areas, however, the measurement requirements are so demanding that novel and unusual circuit architectures must be employed to achieve the desired result. In particular, very high precision transducer-based measurements can be achieved by combining microprocessor and analog techniques. The performance achievable can surpass the best levels obtainable with conventional approaches.

An example of a requirement involves high resolution weighing of 2000 pound rolls of plastic material. In this application, the rolls must be weighed before they are fed into machinery which utilizes the plastic in a coating process. Because the plastic material is relatively expensive, and the number of rolls used over time quite large, it is desirable to keep close tabs on the amount of material actually used in production. This involves weighing the roll before it is used and then weighing the amount of material left on the roll core after it has unwound. In this fashion, the losses accumulated over hundreds of rolls can be tracked and appropriate action taken if the losses are unacceptable. *Figure 1* shows the way the rolls are handled and fed into the coating machinery. The desired weighing system performance specifications also appear in the figure. *Figure 2* shows the specifications for a typical high quality strain gauge load cell transducer. From this information, it can be seen that the electronic error budget is vanishingly small. The 3 mV/V specification on the load cell means that only 30 mV of full-scale is available for a typical 10V transducer excitation. The desired 0.01% resolution means that only 3μV referred-to-input error is allowable. In addition, the gain slope tolerance and temperature coefficients of the load cells, while small, seem to preclude meeting the required specifications. The 0.1% gain slope tolerance also appears to mandate the need for manual system recalibration whenever load cells must be replaced in the field. Finally, assuming these specifications can be met, an A/D converter which will hold near 15-bit stability over the required temperature range is required.

The key to achieving the desired performance is in the realization that the system must be designed as an *integrated* function instead of a group of interconnected signal conditioning blocks. Traditional approaches which rely on "brute force" high stability amplifiers and data converters cannot be successfully used to meet the required specifications.



TL/H/5638–1

FIGURE 1

Desired System Specifications

Accuracy, 0.03%
Stable Resolution, 0.01%
Operating Temperature Range, 10°C to 45°C
Full Load Cell Field Interchangeability
20,000 Count Display

FIGURE 2

Typical Load Cell Specifications

Gain Slope—3 mV/V Excitation ±0.1%
Recommended Excitation—10V
Gain Tempco—±0.0008%/°F
Zero Tempco—±0.0015/°F

The approach utilized is diagrammed in *Figure 3*. In this arrangement a microprocessor is used to effectively close an analog loop around the load cells with an instrumentation amplifier and an A/D converter. In this system, four discrete measurements are continuously performed on each load cell to determine its error corrected output. Corrections are made for zero and gain drift and a first-order temperature error correction is also made. The actual load cell output voltage is read to complete the measurement cycle. The start of a measurement cycle is initiated by the microprocessor commanding the LF13509 differential input multiplexer A to position 1 (See *Figure 4*). In this position, the amplifier inputs are connected to one side of the transducer bridge. This determines the electrical zero in the system at the common-mode output voltage of the bridge. Physical zero information (e.g., "tare weight") is fed to the microprocessor via a pushbutton which is depressed when no load is in the chain hoist. This operation need only be carried out when the system is first turned on. The multiplexer is then switched to position 2.

In this position, the LM163 inputs are connected across the middle resistor in a string of resistors. The voltage across this resistor represents the precise full-scale output voltage of the load cell transducer. Although the transducers are specified for only 0.1% interchangeability, the precise value of gain slope is furnished with each individual device. This information allows the system to determine the gain slope of the transducer. In practice, the middle resistor in the string is physically located within the load cell connector. When any such equipped load cell is plugged into the system, the value of this resistor allows immediate and precise gain slope compensation and eliminates the usual manual calibration requirements. When this measurement is completed, the multiplexer is switched to position 3. In this position the output of strain gage bridge A is connected to the LM163 instrumentation amplifier. This signal, which represents the transducer output, is amplified by the LM163, converted by the A/D and stored in memory. The fourth multiplexer operation is used to read the temperature of the load cell. In this position, the output of the LM335 temperature sensor, which is located inside the load cell transducer, is determined and stored in memory. The relatively high level LM335 output is resistively divided by 100 so the LM163 does not saturate. Two separate temperature terms, zero and gain TC, affect the load cell. Although the LM335 provides the absolute cell temperature, the sign of each temperature term in any individual cell will vary. Thus, not only the cell's temperature but the sign for both zero and gain terms must be furnished. This is accomplished by a pin strapping code inside the load cell's connector. This sequence of operations is also performed by multiplexer B for load cell B. When all the information for both transducers has been collected, the microprocessor can determine the actual weight of the roll. The temperature information provides a first-order correction for the relatively small effect of ambient temperature on the load cell's gain and zero terms.

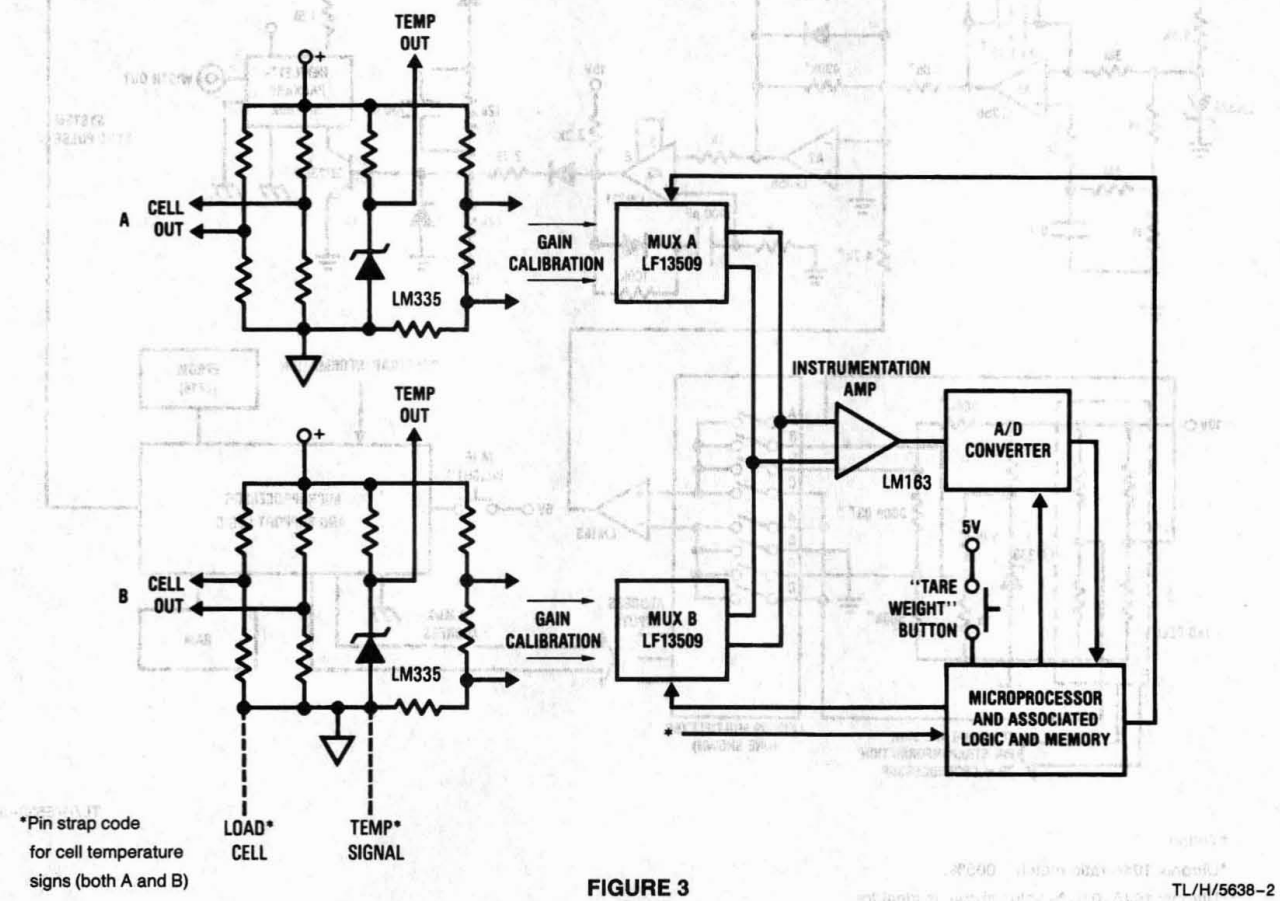
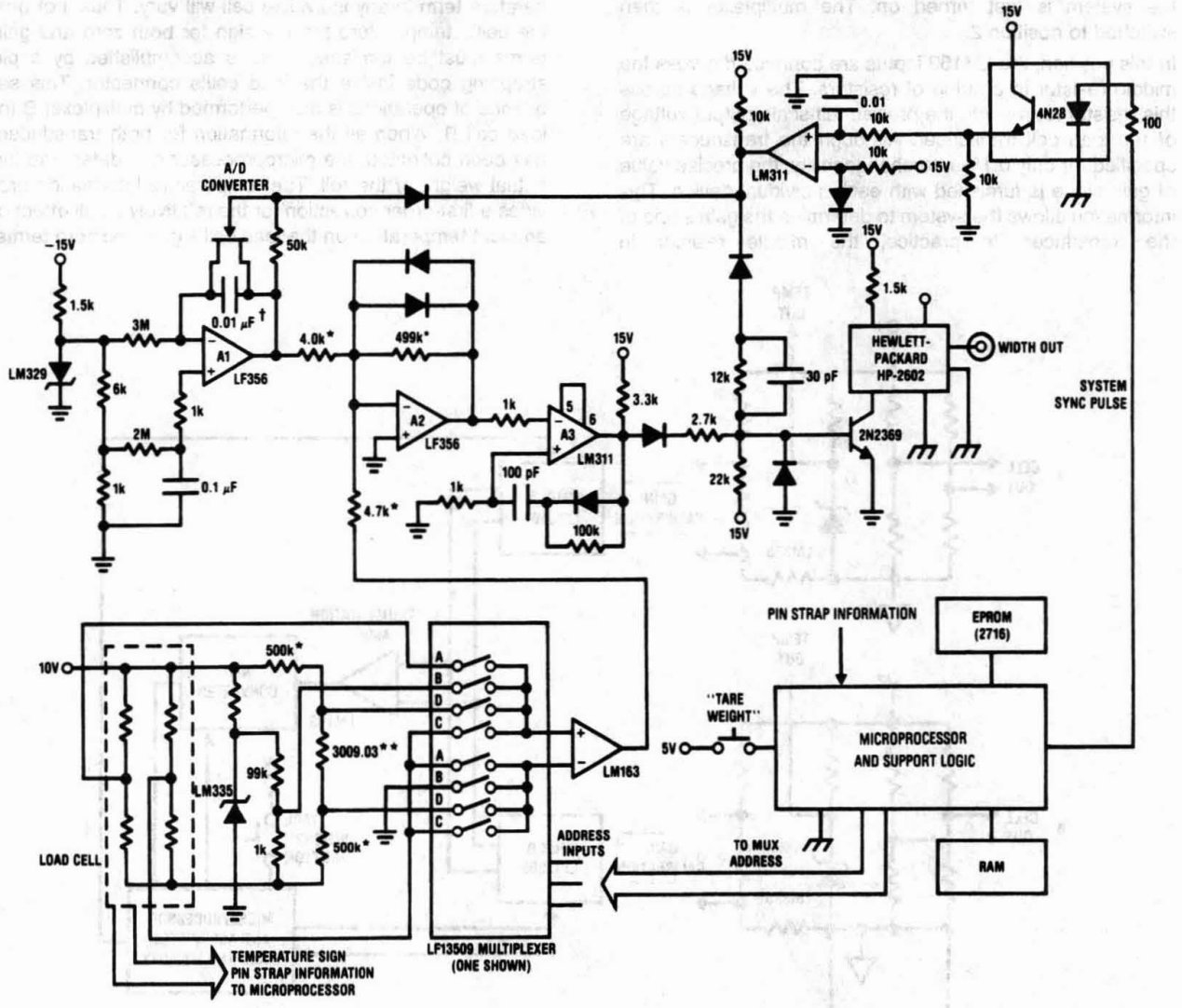


FIGURE 3

TL/H/5638–2

The gain calibration resistor string inside the load cell allows complete field interchangeability with no manual field calibration required. In practice, the load cell connector heads are modified by the addition of the resistor string, temperature sensor and temperature sign pin strapping after the cells have been purchased from the manufacturer. Connector types with the appropriate extra number of pins are substituted for the originals and the completed modified transducer is furnished as a unit to the end user. The stability of this approach is entirely dependent on the resistors in the gain calibration string. The voltage drive to the bridge need not be stable because it is common to the gain calibration string and ratiometrically cancels. Low pass filtering of electrical and mechanical noise is achieved by displaying the digitally-averaged value of a number of measurement cycles. It is worth noting that zero and gain drifts in the instrumentation amplifier and the A/D converter are continuously compensated for by the closed loop action of the microprocessor. The sole requirement for these components is that they be linear and have noise limits within the required measurement precision. In this manner, the zero and gain drifts of all active electronic components in the system are eliminated, which considerably simplifies the selection and design of these components.

A schematic diagram of the system appears in *Figure 4*. For purposes of clarity only, one load cell and its associated multiplexer are shown. Details of the microprocessor are also not included. The LF11509 multiplexer feeds the LM163 instrumentation amplifier. The LM163's output is routed to the A/D converter section which is composed of a ramp generator (A1) and a precision comparator circuit (A2-A3). The output of the A/D is a pulse width which varies with the LM163's output amplitude. This pulse width is fed to the microprocessor which uses it to gate a high speed clock. A



TL/H/5638–3

†Teflon

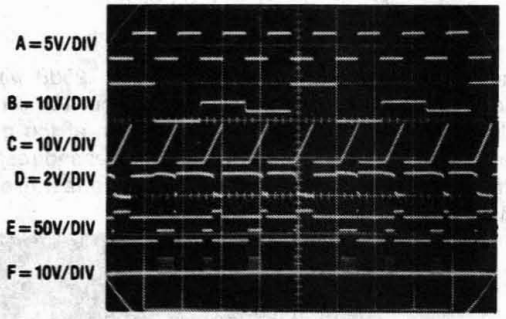
*Ultronix 104A ratio match 0.005%.

**Ultronix 104A, 0.01% value shown is ideal for precise 30 mV output load cell and must be selected at load cell test.

FIGURE 4

loop is completed by using the microprocessor to control the LF11509 multiplexer address inputs. Operation of the system is best understood by referring to *Figure 5*. Trace A is a system synchronizing pulse which is generated by the microprocessor. Trace B is the output of the LM163, which is connected to the multiplexer. Each time the synchronizing pulse goes low, the multiplexer advances one state. The leftmost multiplexer state in the photograph is the zero signal. The next state is the gain calibration, which is followed by the strain gage bridge output and then the temperature signal. The next 4 multiplexer states repeat this pattern for the other load cell. Each time the multiplexer changes state, the LM163 output is compared to the A1 ramp generator output (trace C) by the A2-A3 comparator. A2 acts as a preamplifier for the A3 comparator, insuring a low noise trip point. When the ramp is very close to balancing the current being pulled out of A2's summing junction by the LM163, A2 comes out of diode bound (trace D, *Figure 5*) and trips A3. The rapid slewing, high level signal from A2 allows A3 to have a noise free transition (trace E, *Figure 5*). This output is used to turn off a high speed clock (trace F, *Figure 5*) which was started at the beginning of the ramp (comparator-ramp-high speed clock detail shown in *Figure 6*). The waveforms show that the number of high speed pulses which occur at each multiplexer state varies with the LM163's output. Because the ramp is highly linear and the comparator very stable, a direct relationship between the number of high speed pulses and the LM163 output is assured. The final computed answer at which the microprocessor controlled loop arrives will nullify the effects of drift in the A/D converter and instrumentation amplifier.

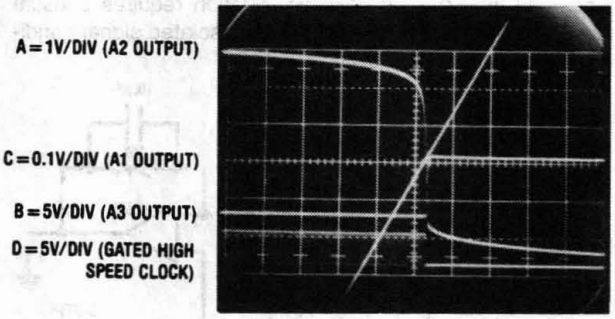
In practice, this system has met specifications in the industrial environment for which it was designed. It furnishes a good example of the type of intelligence which is becoming typical in industrial measurement and control apparatus. The interlocking of analog and digital techniques to solve a difficult measurement problem will become even more common in future applications.



TL/H/5638–4

*System operation normally occurs at a 2 Hz rate but has been sped up for photographic convenience.

FIGURE 5



TL/H/5638–5

Details of comparator-ramp-high speed clock interaction:

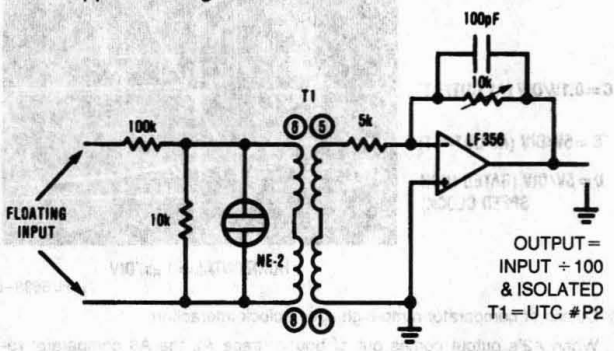
When A2's output comes out of bound (trace A), the A3 comparator responds with a clean, noise-free transition (trace B), causing the high speed clock burst to cease (trace D). Trace C shows the ramp, greatly expanded. A2-A3 trip point occurs just after the ramp passes center screen.

FIGURE 6

Isolation Techniques For Signal Conditioning

National Semiconductor
Application Note 298

Industrial environments present a formidable challenge to the electronic system designer. In particular, high electrical noise levels and often excessive common mode voltages make safe, precise measurement difficult. One of the best ways to overcome these problems is by the use of isolated measurement techniques. Typically, these approaches utilize transformers or opto isolators to galvanically isolate the input terminals of the signal conditioning amplifier from its output terminal. This breaks the common ground connection and eliminates noise and dangerous common mode voltages. The conflicting requirements for good accuracy and total input/output galvanic isolation requires unusual circuit techniques. A relatively simple isolated signal conditioner appears in *Figure 1*.



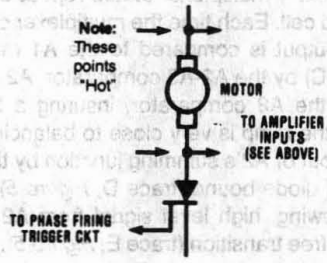
TL/H/5639–2

TO AC LINE FROM FULL WAVE BRIDGE

FIGURE 1

FLOATING INPUT HIGH VOLTAGE MOTOR MONITOR

In this inexpensive circuit, a wideband audio transformer permits safe, ground referenced monitoring of a motor which is powered directly from the 115VAC line. *Figure 1A* details the measurement arrangement. The floating amplifier inputs are applied directly across the brush-type motor. The 100k-10k string, in combination with the transformer ratio, provides a nominal 100:1 division in the observed motor voltage while simultaneously allowing a ground referenced output. The NE-2 bulb suppresses line transients while the 10k potentiometer trims the circuit for a precise 100:1 scale factor. To calibrate the circuit, apply a 10-volt RMS 1kHz sine wave to the floating inputs, and adjust the potentiometer for 100 millivolts RMS output. Full power

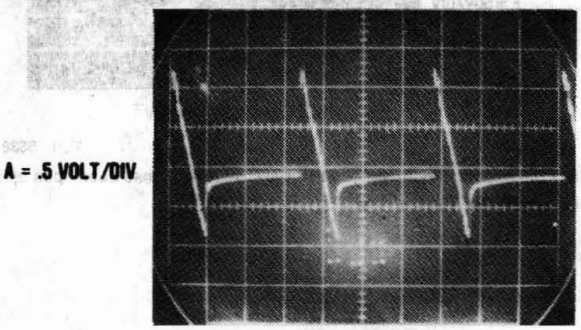


TL/H/5639–1

AC LINE FROM FULL WAVE BRIDGE

FIGURE 1A

bandwidth extends from 15Hz to 45kHz ± .25dB with the −3dB point beyond 85kHz. Risetime is about 10 microseconds. *Figure 2* shows the motor waveform at the ground referenced circuit output. The isolated, wideband response of the circuit permits safe monitoring of the fast rise SCR turn-on as well as the motor's brush noise.

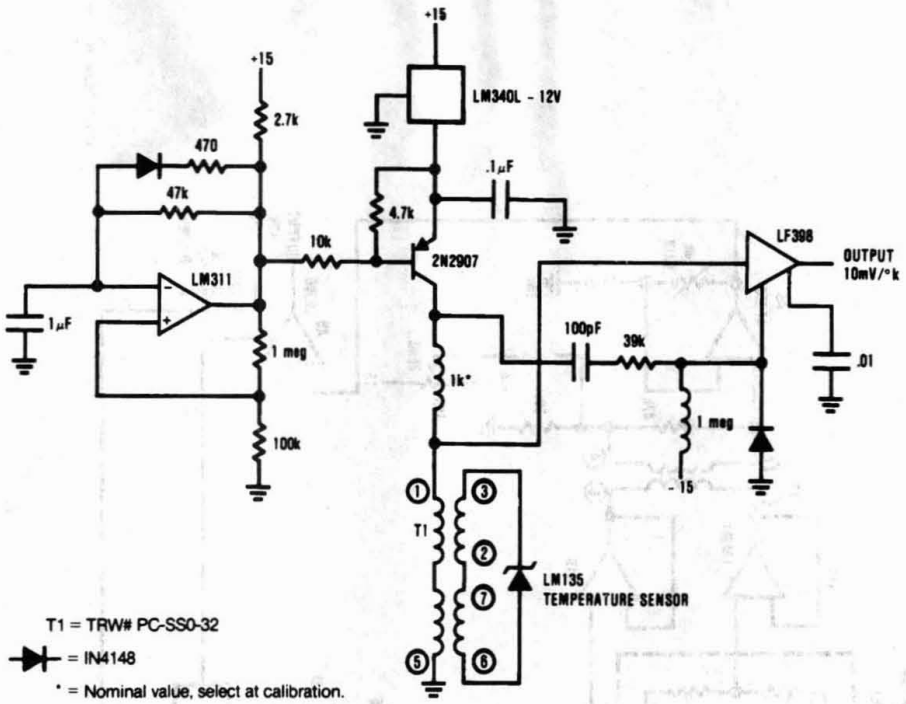


TL/H/5639–3

FIGURE 2

ISOLATED TEMPERATURE MEASUREMENT

Figure 3 shows a scheme which allows an LM135 temperature sensor to operate in a fully floating fashion. In this circuit, the LM311 puts out a 100 microsecond pulse at about 20Hz. This signal biases the PNP transistor, whose collector load is composed of the 1kΩ unit and the primary of T1. The voltage that develops across T1's primary (waveform A, *Figure 4)* will be directly dependent upon the value that the LM135 temperature sensor clamps the secondary at. Waveform B, *Figure 4* details the transformer primary current.



TL/H/5639–4

FIGURE 3

This voltage value, of course, varies with the temperature of the LM135 in accordance with its normal mode of operation. The LF398 sample-and-hold IC is used to sample the transformer primary voltage and presents the circuit output as a DC level. The 100 pF-39k-1MΩ combination presents a trigger pulse (waveform C, *Figure 4)* to the LF398, so that the sampling period does not finish until well after the LM135 has settled. The LM340 12-volt regulator provides power supply rejection for the circuit. To calibrate, replace the LM135 with an LM336 2.5-volt diode of known breakdown potential. Next, select the 1kΩ valve until the circuit output is the same as the LM336 breakdown voltage. Replace the LM336 with the LM135 and the circuit is ready for use.

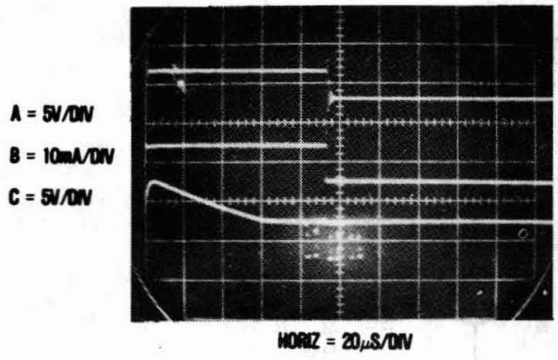


FIGURE 4 TL/H/5639–5

FULLY ISOLATED PRESSURE TRANSDUCER MEASUREMENT

Strain gauge-based transducers present special difficulties if total isolation from ground is required. They need excitation power in addition to their output signal. Some industrial measurement situations require that the transducer must be physically connected to a structure which is floating at a high common mode voltage. This means that the signal conditioning circuitry must supply fully floating drive to the strain gauge bridge, while also providing isolated transducer output signal amplification. *Figure 5* details a way to accomplish this. Here, the strain bridge is excited by a transformer which generates a pulse of servo-controlled amplitude. The pulse is generated by storing the sampled amplitude of the output pulse as a DC level, and supplying this information to a feedback loop which controls the voltage applied to the output switch. A2 functions as an oscillator which simultaneously drives Q2-Q3 and the LF398 (A3) sample mode pin. When A2's output pulse ends, A3's output is a DC level equal to the amplitude of the output pulse which drives the strain bridge. The dual secondary of T1 allows accurate magnetic sampling of the strain bridge output pulse without sacrificing electrical isolation. A3's output is compared to the LH0070 10-volt reference by A4, whose output drives Q1. Q1's emitter provides the DC supply level to the Q2-Q3 switch. This servo action forces the pulses applied to the strain gauge transducer (waveform A, *Figure 6)* to be of constant amplitude and equal to the 10-volt LH0070 reference output. Some amount of the pulse's energy is stored in the 100μF capacitor and used to power the LM358 dual (A1) followers. These devices unload the output of the transducer bridge and drive the primary of T2. T2's secondary output amplitude (waveform B, *Figure 6)* represents the transducer output value. This potential is amplified by A5 and fed to A6, a sample-and-hold circuit. A6's sample command is a shortened version of the A2 oscillator pulse. The 74C221 generates this pulse (waveform C, *Figure 6*).

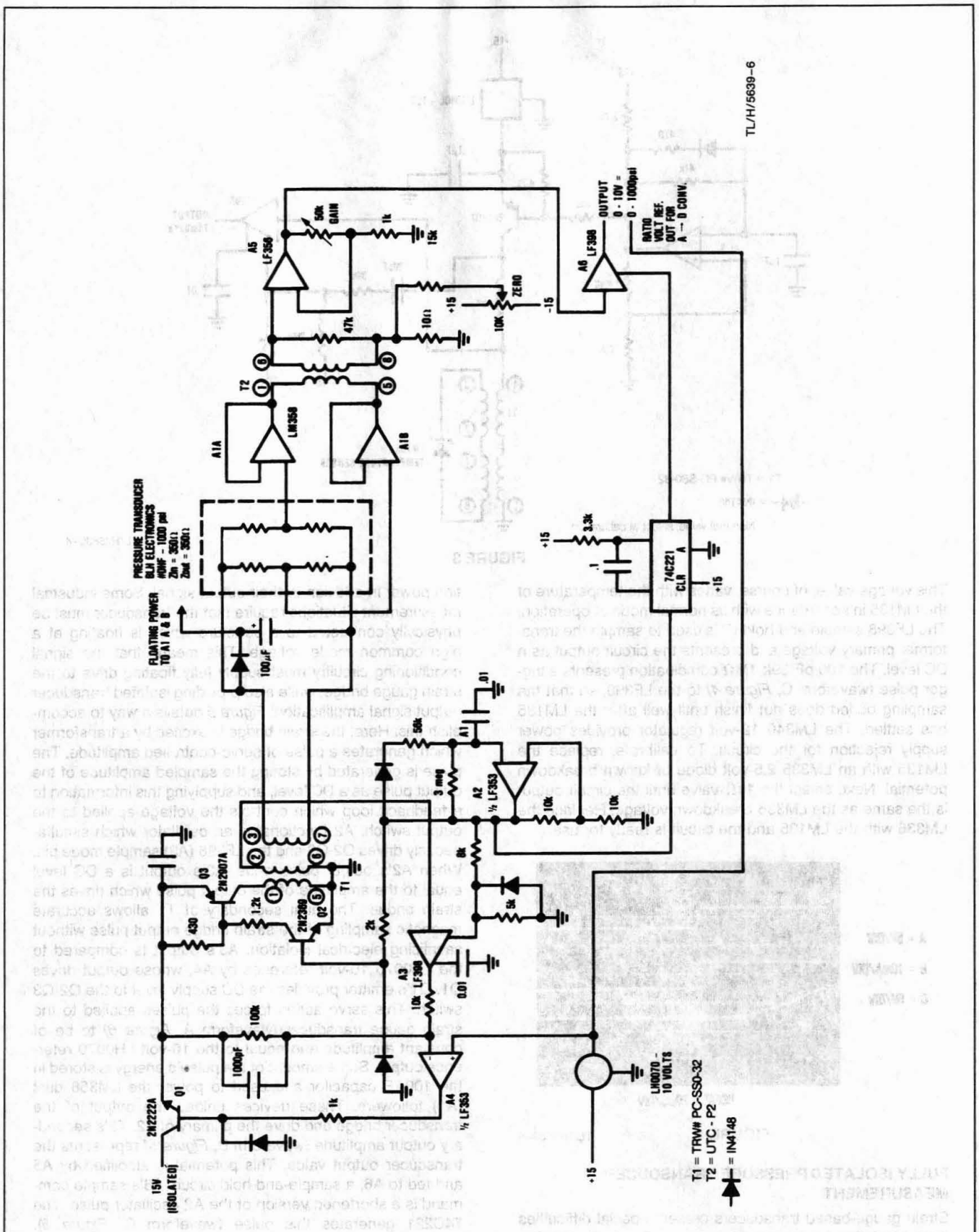

TL/H/5639–6
A5 LF356
50k GAIN
1k
15k
A6 LF398
OUTPUT 0 - 10V = 0 - 1000psi
RATIO VOLT REF. OUT FOR A → D CONV.
+15
ZERO
-15
10K
47k
10Ω
T2
A1A
LM358
A1B
PRESSURE TRANSDUCER BLH ELECTRONICS #UNF - 1000 psi Zin = 350Ω Zout = 350Ω
FLOATING POWER TO A1 A B
100µF
+15
3.3k
.1
74C221
CLR A
+15
.01
A1
50k
3 meg
A2 ½ LF353
10k
10k
8k
5k
Q3 2N2907A
Q2 2N2369
T1
1.2k
430
2k
A3 LF398
10k
0.01
100k
1000pF
Q1 2N2222A
15V (ISOLATED)
1k
A4 ½ LF353
LM0070 - 10 VOLTS
-15
T1 = TRW# PC-SSO-32
T2 = UTC - P2
= IN4148

FIGURE 5

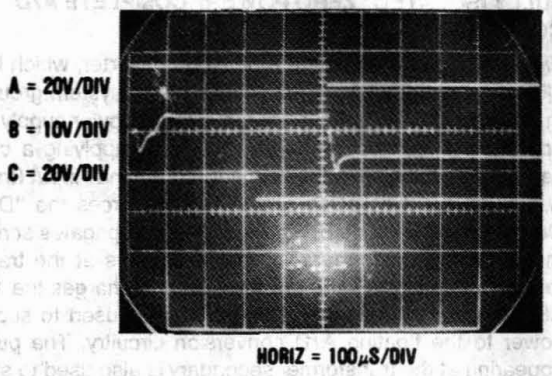
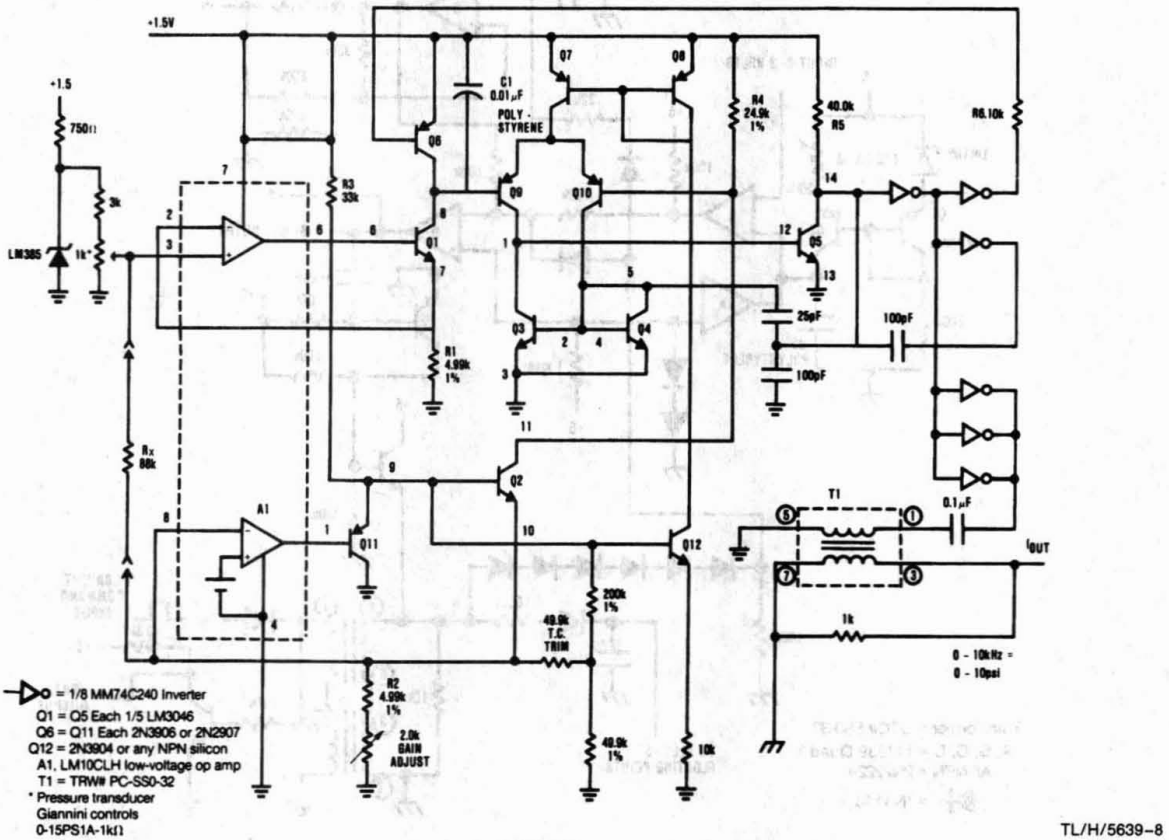


FIGURE 6 TL/H/5639–7

Because the A6 sample command falls during the settled section of T2's output pulse, A6's output will be a DC representation of the amplified strain gauge pressure transducer output. The LH0070 output may be used to ratiometrically reference a monitoring A/D converter. To calibrate this circuit, insert a strain bridge substitution box (e.g., BLH model 625) in place of the transducer and dial in the respective values for zero and full-scale output (which are normally supplied with the individual transducer). Adjust the circuit "zero" and "gain" potentiometers until a 0- to 10-volt output corresponds to a 0 to 1000psi pressure input.

1.5-VOLT POWERED ISOLATED PRESSURE MEASUREMENT

Figure 7 diagrams another pressure measurement circuit. This circuit presents a frequency output which is fully isolated by the transformer indicated. The entire circuit may be powered from a 1.5-volt supply, which may be derived from a battery or solar cells. The potentiometer output of the pressure transducer used is fed to a voltage-to-frequency converter circuit. In this V-F circuit, an LM10 op amp acts as an input amplifier, and forces the collector current of Q1 to be linearly proportional to V_{IN} for a range of 0 to +400 millivolts. Likewise, the reference amplifier of the LM10 causes Q2's output current to be stable and constant under all conditions. The transistors Q3-Q10 form a relaxation oscillator, and every time the voltage across C1 reaches



TL/H/5639–8

FIGURE 7

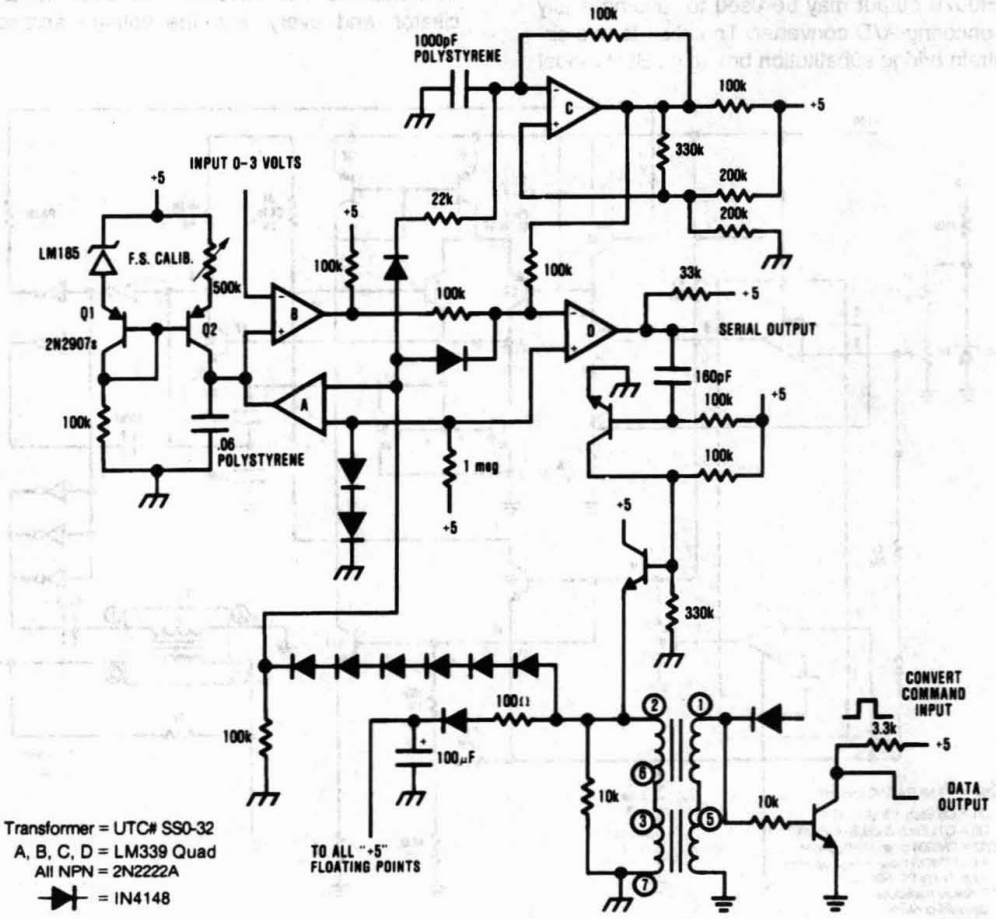
0.8-volt, Q6 is commanded to reset it to zero volts differential. This basic circuit is not normally considered a very accurate technique, because the dead time, while Q6 is saturated, will cause a large (1%) nonlinearity in the V-tc-F transfer curve. However, the addition of R_X causes the reference current flowing through Q2 to include a term which is linearly proportional to the signal, which corrects the transfer nonlinearity.

The NSC MM74C240 inverters are employed because this IC has the only uncommitted inverters with such a low (0.6 to 0.8V) threshold that they can operate on a supply as low as 1.2 volts.

The 49.9k resistors which feed into Q2's emitter act as a gain tempco trim, as Q12's Vbe is used as a temperature sensor. If the output frequency is 100ppm/C too fast/hot, you can cut the resistor to 20k. If f is too slow/hot, add more resistance in series with the 49.9k. Total current drain for this circuit is about 1 milliampere.

FULLY ISOLATED "ZERO POWER" COMPLETE A/D CONVERTER

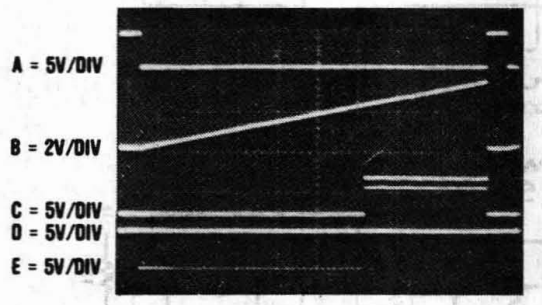
Figure 8 shows a complete 8-bit A/D converter, which has all input and output lines fully floating from system ground. In addition, the A/D converter requires *no* power supply for operation! Circuit operation is initiated by applying a convert-command pulse to the "convert-command" input (trace A, *Figure 9B).* This pulse simultaneously forces the "Data Output" line low (trace B, *Figure 9B)* and propagates across the isolation transformer. The pulse appears at the transformer secondary *(Figure 9A,* trace A) and charges the 100 μF capacitor to five volts. This potential is used to supply power to the floating A/D conversion circuitry. The pulse appearing at the transformer secondary is also used to start the A/D conversion by biasing comparitor A's negative input low. This causes comparitor A's output to go low, discharging the .06μF capacitor (waveform B, *Figure 9A).* Simultaneously, the 10kHz oscillator (*Figure 9A,* trace D), formed by



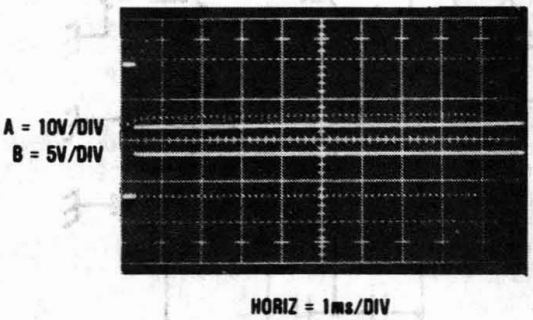
TL/H/5639–9

FIGURE 8

comparator D and its associated components, is forced off via the 22k diode path. A second diode path also forces comparator D's output low (*Figure 9A,* trace E). Note the cessation of oscillation during the time the convert command pulse is high. When the convert command pulse falls, the Q1-Q2 current source begins to charge the .06 μF capacitor. During this time, the 10 kHz comparator C oscillator runs, and comparator D's output is a stream of 10 kc clock pulses. When the ramp (trace B, *Figure 9A)* across the .06 μF capacitor exceeds the circuit input voltage, comparator B's output goes high (trace C, *Figure 9A),* forcing comparator D's output low. The number of pulses which appeared at comparator D's output is directly proportional to the value of the circuit's input voltage. These pulses are amplified by the two NPN transistors which are used to modulate the data pulse stream back across the transformer. The six series diodes insure that the modulated data does not appear at comparator A's input and trigger it. The pulses appear at the primary (*Figure 9B,* trace A) as small amplitude spikes and are then amplified by the data output transistor, whose collector waveform is trace B or *Figure 9B.* In this example a 0- to 3-volt input produces 0- to 300 pulses at the output. The 22k diode path averts a +1 count uncertainty error by synchronizing the 10kHz clock to the conversion sequence at the beginning of each conversion. The 500k potentiometer in the current source adjusts the scale factor. The circuit drifts less than 1LSB over 25°C ± 20°C and requires 45 milliseconds to complete a full scale 300 count conversion.



TL/H/5639–10



TL/H/5639–11

FIGURE 9

COMPLETE, FLOATING MULTIPLEXED THERMOCOUPLE TEMPERATURE MEASUREMENT

Figure 10 shows a complete , fully floating multiplexed thermocouple measurement system. Power to the floating system is supplied via T2, which runs in a self oscillating DC-DC converter configuration with the 2N2219 transistors. T2's output is rectified, filtered, and regulated to ±15 volts. An eight channel LF13509 multiplexer is used to sequentially switch 7 inputs and a ground reference into the LM11 amplifier. The LM11 provides gain and cold junction compensation for the thermocouples. The multiplexer is switched from the 74C93 counter, which is serially addressed via the 4N28 opto isolator. The ground referenced channel prevents monitoring instrumentation from losing track of the multiplexer state. The LM11's output is fed into a unity gain isolation amplifier. Oscillator drive for the isolation amplifier is derived by dividing down T2's pulsed output, and shaping the 74C90's output with A4 and its associated components. This scheme also prevents unwanted interaction between the T2 DC-DC converter and the isolation amplifier. This circuit, similar to the servo-controlled amplitude pulser described in *Figure 5,* puts a pulse across T1's primary. The amplitude of the pulse is directly dependent on the LM11's output value. T1's secondary receives the pulse and feeds into an LF398 sample-hold-amplifier. The LF398 is supplied with a delayed trigger pulse, so that T1's output is sampled well after settling occurs. The LF398 output equals the value of the LM11. In this fashion, the fully floating thermocouple information may be connected to grounded test equipment or computers. Effective cold-junction compensation results when the thermocouple leads and the LM335 are held isothermal. To calibrate the circuit, first adjust R3 for an LM11 gain of 245.7. Next, short the "+" input of the LM11 and the LM329 to floating common, and adjust R1 so that the circuit output is 2.982 volts at 25°C. Then, remove the short across the LM329 and adjust R2 for a circuit output of 246 millivolts at 25°C. Finally, remove the short at the LM11 input, and the circuit is ready for use.

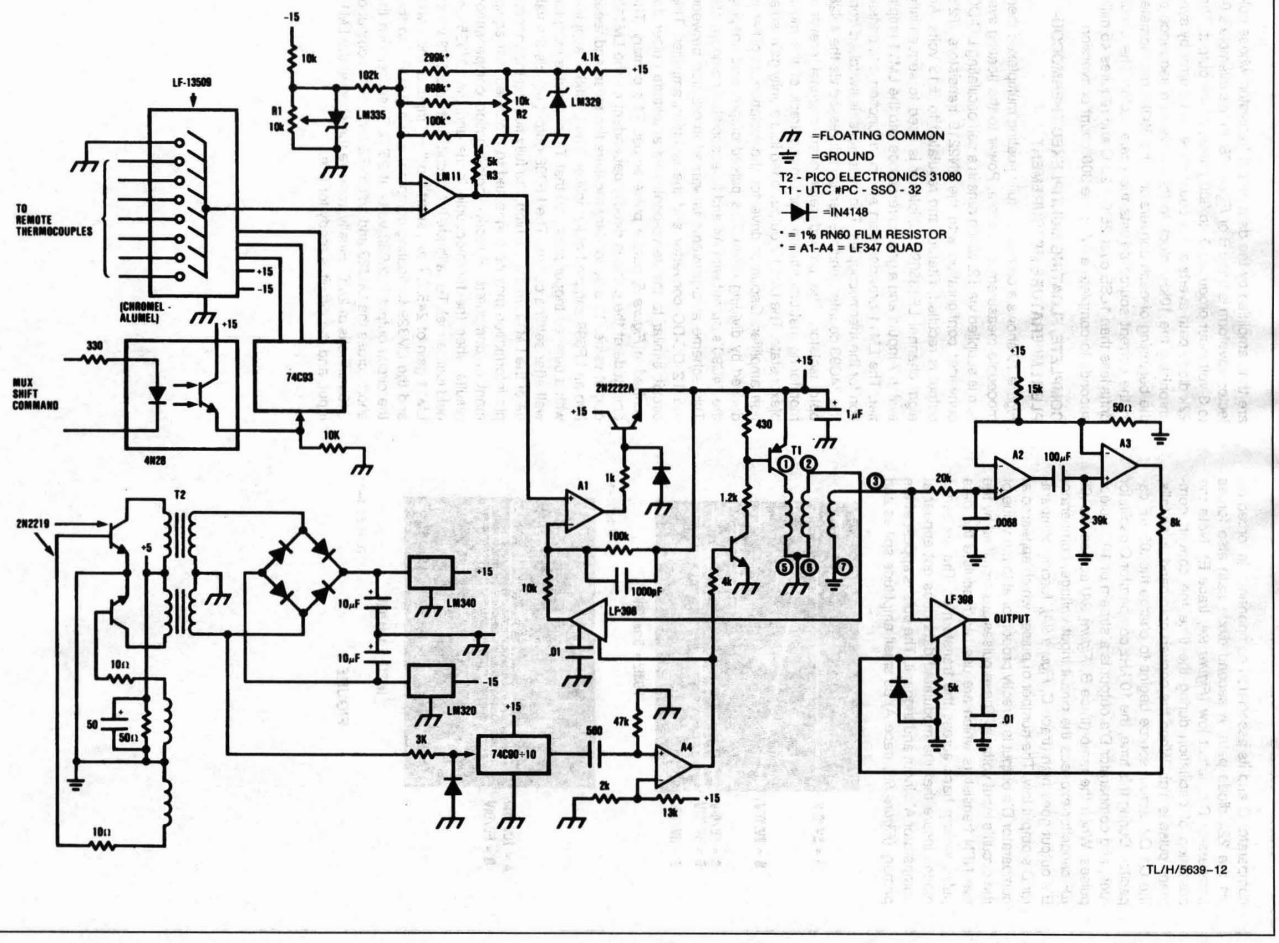

=FLOATING COMMON
=GROUND
T2 - PICO ELECTRONICS 31080
T1 - UTC #PC - SSO - 32
=IN4148
* = 1% RN60 FILM RESISTOR
* = A1-A4 = LF347 QUAD
LF-13509
TO REMOTE THERMOCOUPLES
(CHROMEL - ALUMEL)
MUX SHIFT COMMAND
4N28
74C93
LM11
LM335
LM329
LM340
LM320
74C90÷10
2N2222A
2N2219
LF-398
OUTPUT
TL/H/5639–12

FIGURE 10

Audio Applications of Linear Integrated Circuits

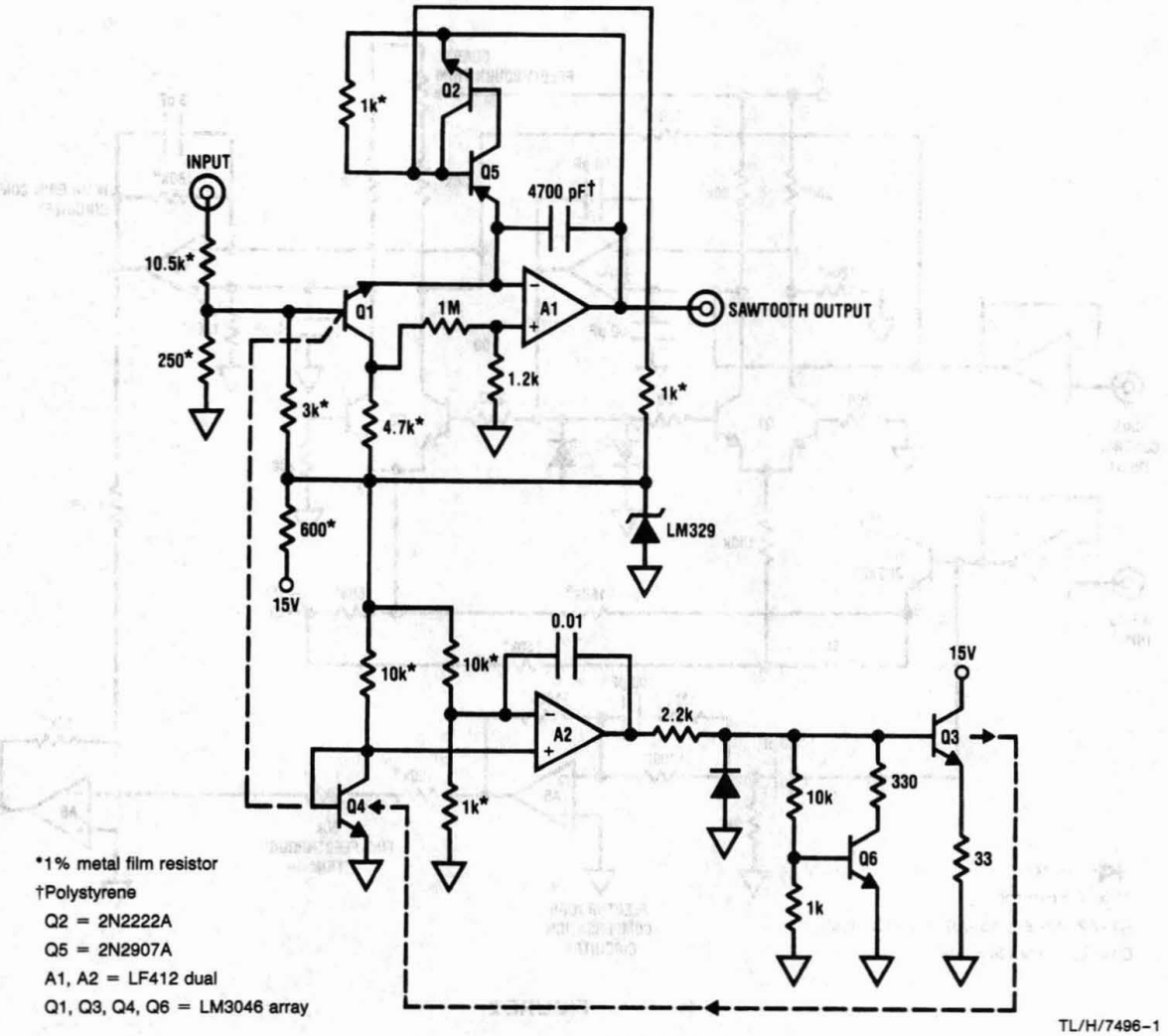
National Semiconductor
Application Note 299

Although operational amplifiers and other linear ICs have been applied as audio amplifiers, relatively little documentation has appeared for other audio applications. In fact, a wide variety of studio and industrial audio areas can be served by existing linear devices. The stringent demands of audio requirements often mean that unusual circuit configurations must be used to satisfy a requirement. By combining off-the-shelf linear devices with thoughtful circuit designs, low cost, high performance solutions are achievable. An example appears in *Figure 1*.

EXPONENTIAL V-F CONVERTER

Studio-type music synthesizers require an exponentially responding V-F converter with a typical scale factor of 1V in per octave of frequency output. Exponential conformity requirements must be within 0.5% from 20 Hz–15 kHz. Almost all existing designs utilize the logarithmic relationship between V_{BE} and collector current in a transistor.

Although this method works well, it requires careful attention to temperature compensation to achieve good results. *Figure 1* shows a circuit which eliminates all temperature compensation requirements. In this circuit, the current into A1's summing junction is exponentially related to the circuit input voltage because of the logarithmic relationship between Q1's V_{BE} and its collector current. A1's output integrates negatively until the Q2-Q5 pair comes on and resets A1 back to 0V. Note that opposing junction tempcos in Q2 and Q5 provide a temperature compensated switching threshold with a small (100 ppm/°C) drift. The −120 ppm/°C drift of the polystyrene integrating capacitor effectively cancels this residual term. In this fashion, A1's output provides the sawtooth frequency output. The LM329 reference stabilizes the Q5-Q2 firing point and also fixes Q1's collector bias. The 3k resistor establishes a 20 Hz output frequency for 0V input, while the 10.5k unit trims the gain to 1V in per octave frequency doubling out. Exponential conformity is within 0.25% from 20 Hz to 15 kHz.



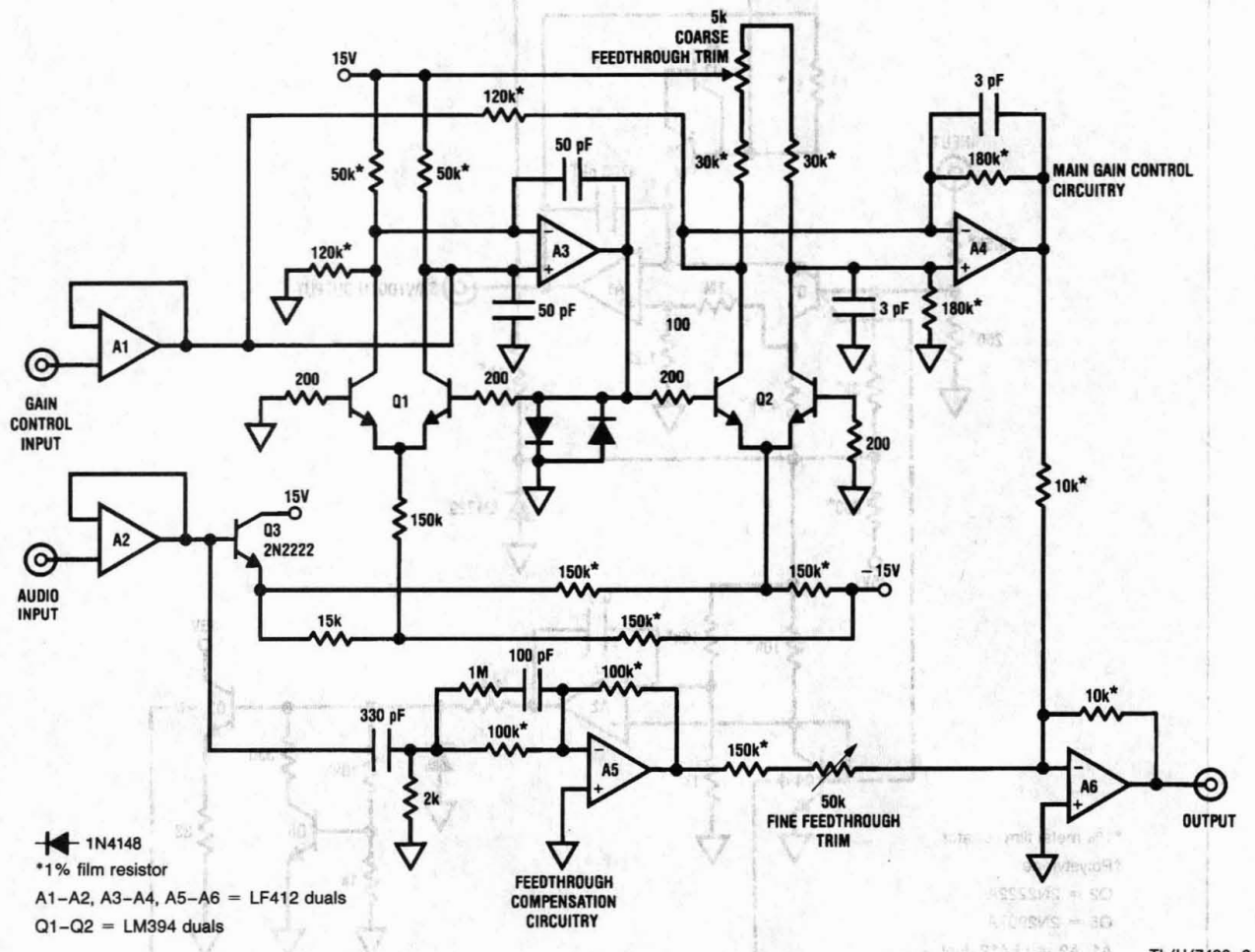
TL/H/7496–1

FIGURE 1

The 1M–1.2k divider at A1's "+" input achieves first order compensation for Q1's bulk emitter resistance, aiding exponential conformity at high frequencies. A2 and its associated components are used to "brute-force" stabilize Q1's operating point. Here, Q3, Q4 and A2 form a temperature-control loop that thermally stabilizes the LM3046 array, of which Q1 is a part. Q4's V_{BE} senses array temperature while Q3 acts as the chip's heater. A2 provides servo gain, forcing Q4's V_{BE} to equal the servo temperature setpoint established by the 10k–1k string. Bias stabilization comes from the LM329. The Q6 clamp and the 33Ω emitter resistor determine the maximum power Q3 can dissipate and also prevent servo lock-up during circuit start-up. Q1, operating in this tightly controlled environment, is thus immune from effects of ambient temperature shift.

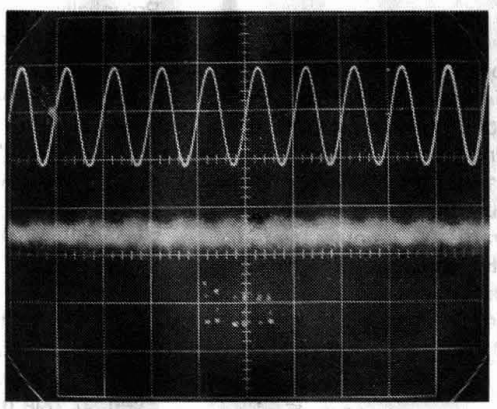
ULTRA-LOW FEEDTHROUGH VOLTAGE-CONTROLLED AMPLIFIER

A common studio requirement is a voltage-controlled gain amplifier. For recording purposes, it is desirable that, when the gain control channel is brought to 0V, the signal input feedthrough be as low as possible. Standard configurations use analog multipliers to achieve the voltage-controlled gain function. In *Figure 2*, A1–A4, along with Q1–Q3, comprise such a multiplier, which achieves about −65 dB of feedthrough suppression at 10 kHz. In this arrangement, A4 single ends a transconductance type multiplier composed of A3 along with Q1 and Q2. A1 and A2 provide buffered inputs. The −65 dB feedthrough figure is typical for this type of multiplier. A5 and A6 are used to further reduce this feedthrough figure to −84 dB at 20 kHz by a nulling technique. Here, the circuit's audio input is inverted by A5 and then summed at A6 with the main gain control output, which comes from A4. The RC networks at A5's input provide phase shift and frequency response characteristics which are the same as the main gain control multipliers feedthrough characteristics. The amount of feedthrough compensation is adjusted with the 50k potentiometer. In this way, the feedthrough components (and only the feedthrough components) are nulled out and do not appear at A6's output. From 20 Hz to 20 kHz, feedthrough is less than −80 dB. Distortion is inside 0.05%, with a full power bandwidth of 60 kHz. To adjust this circuit, apply a 20 Vp-p sine wave at the audio input and ground the gain control input. Adjust the 5k coarse feedthrough trim for minimum output at A4. Next, adjust the 50k fine feedthrough trim for minimum output at A6. For best performance, this circuit must be rigidly constructed and enclosed in a fully shielded box with attention give to standard low noise grounding techniques. *Figure 3* shows the typical remaining feedthrough at 20 kHz for a 20 Vp-p input. Note that the feedthrough is at least −80 dB down and almost obscured by the circuit noise floor.



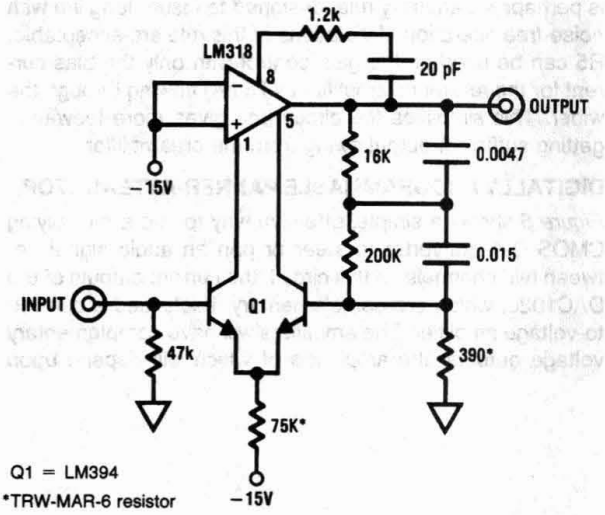
TL/H/7496–2

FIGURE 2



TL/H/7496–3

FIGURE 3



TL/H/7496–4

Frequency	Total Harmonic Distortion				
20	<0.002	<0.002	<0.002	<0.002	<0.002
100	<0.002	<0.002	<0.002	<0.002	<0.002
1000	<0.002	<0.002	<0.002	<0.002	<0.002
10000	<0.002	<0.002	<0.002	<0.0025	<0.003
20000	<0.002	<0.002	<0.004	<0.004	<0.007
Output Amplitude (Vrms)	0.03	0.1	0.3	1.0	5.0

FIGURE 4

ULTRA-LOW NOISE RIAA PREAMPLIFIER

In *Figure 4*, an LM394 is used to replace the input stage of an LM118 high speed operational amplifier to create an ultra-low distortion, low noise RIAA-equalized phono preamplifier. The internal input stage of the LM118 is shut off by tying the unused input to the negative supply. This allows the LM394 to be used in place of the internal input stage, avoiding the loop stability problems created when extra stages are added. The stability problem is especially critical in an RIAA circuit where 100% feedback is used at high frequencies. Performance of this circuit exceeds the ability of most test equipment to measure it. As shown in the accompanying chart, harmonic distortion is below the measurable 0.002% level over most of the operating frequency and amplitude range. Noise referred to a 10 mV input signal is −90 dB down, measuring 0.55 μVrms and 70 pArms in a 20 kHz bandwidth. More importantly, the noise figure is less than 2 dB when the amplifier is used with standard phono cartridges, which have an equivalent wideband (20 kHz) noise of 0.7 μV. Further improvements in amplifier noise characteristics would be of little use because of the noise generated by the cartridge itself. A special test was performed to check for transient intermodulation distortion. 10 kHz and 11 kHz were mixed 1:1 at the input to give an rms output voltage of 2V (input = 200 mV). The resulting 1 kHz intermodulation product measured at the output was 80 μV. This calculates to 0.0004% distortion, quite a low level, considering that the 1 kHz has 14 dB (5:1) gain with respect to the 10 kHz signal in an RIAA circuit. Of special interest also is the use of all DC coupling. This eliminates the overload recovery problems associated with coupling and bypass capacitors. Worst-case DC output offset voltage is about 1V with a cartridge having 1 kΩ DC resistance.

MICROPHONE PREAMPLIFIER

Figure 5 shows a microphone preamplifier which runs from a single 1.5V cell and can be located right at the microphone. Although the LM10 amplifier-reference combination has relatively slow frequency response, performance can be considerably improved by cascading the amplifier and reference amplifier together to form a single overall audio amplifier. The reference, with a 500 kHz unity-gain bandwidth, is used as a preamplifier with a gain of 100. Its output is fed through a gain control potentiometer to the op amp, which is connected for a gain of 10. The combination gives a 60 dB gain with a 10 kHz bandwidth, unloaded, and 5 kHz, loaded with 500Ω. Input impedance is 10 kΩ.

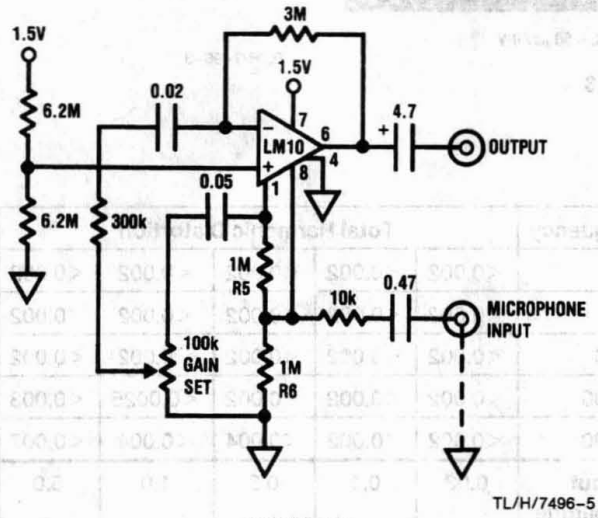


FIGURE 5

Potentially, using the reference as a preamplifier in this fashion can cause excess noise. However, because the reference voltage is low, the noise contribution which adds root-mean-square, is likewise low. The input noise voltage in this connection is 40 nV − 50 nV/$\sqrt{\text{Hz}}$, approximately equal to that of the op amp.

One point to observe with this connection is that the signal swing at the reference output is strictly limited. It cannot swing much below 150 mV, nor closer than 800 mV to the supply. Further, the bias current at the reference feedback terminal lowers the output quiescent level and generates an uncertainty in this level. These facts limit the maximum feedback resistance (R5) and require that R6 be used to optimize the quiescent operating voltage on the output. Even so, one must consider the fact that limited swing on the preamplifier can reduce maximum output power with low settings on the gain control.

In this design, no DC current flows in the gain control. This is perhaps an arbitrary rule, designed to insure long life with noise-free operation. If violations of this rule are acceptable, R5 can be used as the gain control with only the bias current for the reference amplifier (<75 nA) flowing through the wiper. This simplifies the circuit and gives more leeway in getting sufficient output swing from the preamplifier.

DIGITALLY PROGRAMMABLE PANNER-ATTENUATOR

Figure 6 shows a simple, effective way to use a multiplying CMOS D-A converter to steer or pan an audio signal between two channels. In this circuit, the current outputs of the DAC1020, which are complementary, each feed a current-to-voltage amplifier. The amplifiers will have complementary voltage outputs, the amplitude of which will depend upon

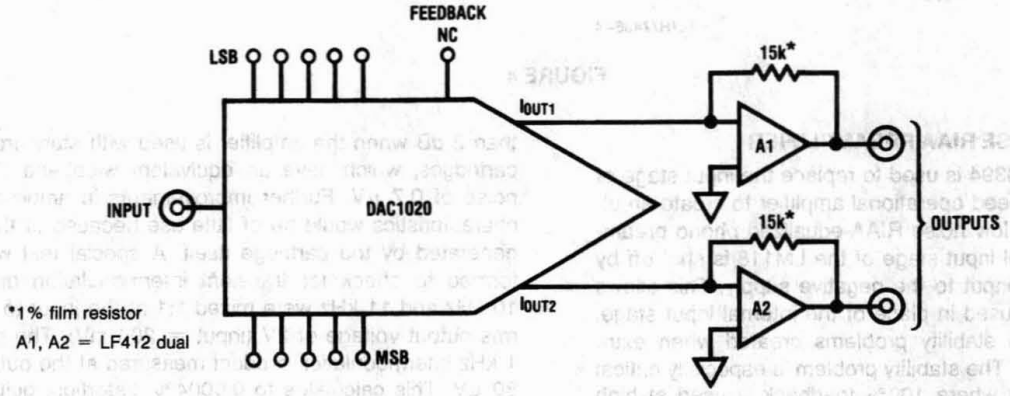


FIGURE 6

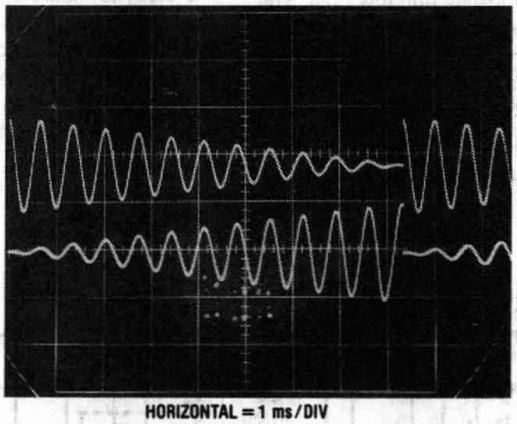
the address code to the DAC's digital inputs. *Figure 7* shows the amplifier outputs for a ramp-count code applied to the DAC digital inputs. The 1.5 kHz input appears in complementary amplitude-modulated form at the amplifier outputs. The normal feedback connection to the DAC is not used in this circuit. The use of discrete feedback resistors facilitates gain matching in the output channels, although each amplifier will have a $\approx$300 ppm/°C gain drift due to mismatch between the internal DAC ladder resistors and the discrete feedback resistors. In almost all cases, this small error is acceptable, although two DACs digitally addressed in complementary fashion could be used to totally eliminate gain error.

DIGITALLY PROGRAMMABLE BANDPASS FILTER

Figure 8 shows a way to construct a digitally programmable first order bandpass filter. The multiplying DAC's function is to control cut-off frequency by controlling the gain of the A3–A6 integrators, which has the effect of varying the integrators' capacitors. A1–A3 and their associated DAC1020 form a filter whose high-pass output is taken at A1 and fed to an identical circuit composed of A4–A6 and another DAC. The output of A6 is a low-pass function and the final circuit output. The respective high-pass and low-pass cut-off frequencies are programmed with the DAC's digital inputs. For the component values shown, the audio range is covered.

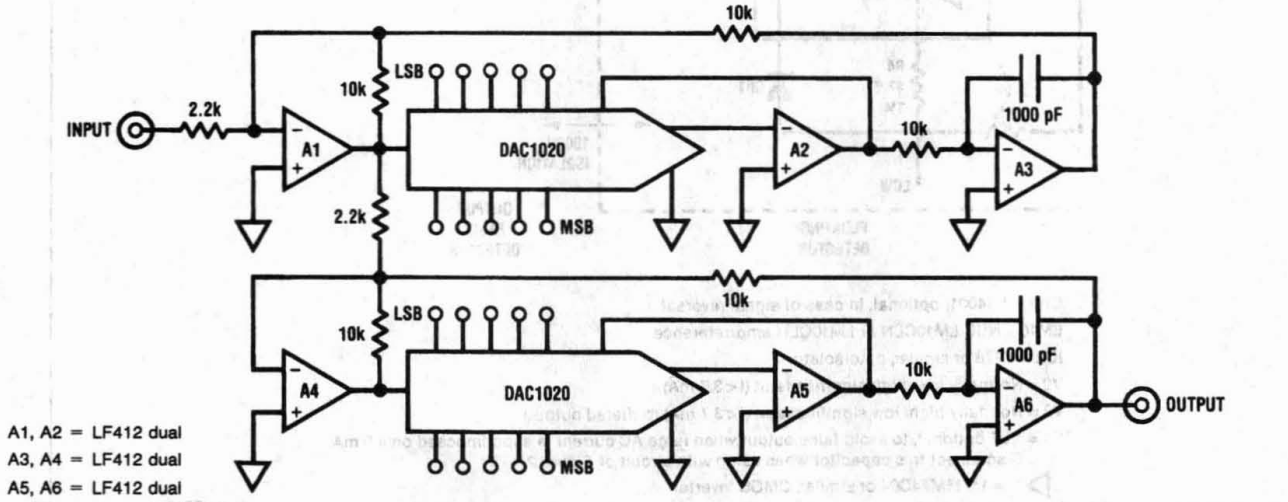
REFERENCES

Application Guide to CMOS Multiplying D-A Converters, Analog Devices, Inc. 1978



TL/H/7496–7

FIGURE 7



TL/H/7496–8

FIGURE 8

Simple Circuit Detects Loss of 4-20 mA Signal

National Semiconductor
Application Note 300
Robert A. Pease

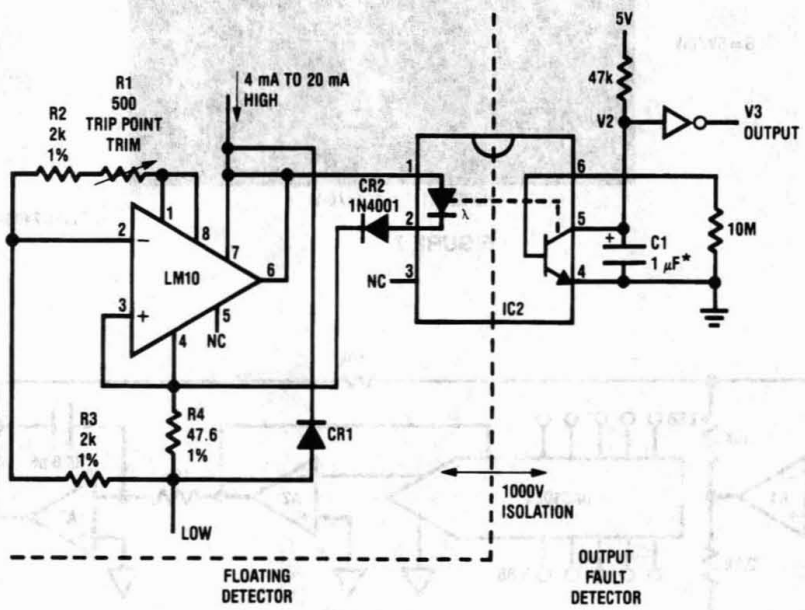
Four-to-twenty milliampere current loops are commonly used in the process control industry. They take advantage of the fact that a remote amplifier can be powered by the same 4-20 mA current that it controls as its output signal, thus using a single pair of wires for signal and power. Circuits for making 4-20 mA transmitters are found in the LM10, LM163, and LH0045 data sheets.

In general, an expensive isolation amplifier would be required to detect the case of a 4 mA signal falling out of spec (e.g., 3.7 mA) without degrading the isolation of the 4-20 mA current loop.

But this new circuit (*Figure 1*) can detect a loss or degradation of signal below 4 mA, with simplicity and low cost. The LM10 contains a stable reference at pins 1 and 8, 200 mV positive referred to pin 4. As long as the loop current is larger than 4 mA, the I × R drop across the 47.6Ω resistor, R4, is sufficient to pull the LM10's amplifier input (pin 2) below pin 3 and keep its output (pin 6) turned *OFF*.

The 4-20 mA current will flow through the LED in the optoisolator and provide a *LOW* output at pin 5 of the optoisolator.

When the current loop falls below 3.7 mA, the LM10's input at pin 2 will rise and cause the pin 6 output to fall and steal all the current away from the LED in the optoisolator. Pin 5 of the 4N28 will rise to signify a *fault* condition. This *fault* flag will fly for any loop current between 3.7 mA and 0.0 mA (and also in case of reversal or open-circuit). R1 is used to trim the threshold point to the desired value. CR2 is added in series with the LED to make sure it will turn OFF when the LM10's output goes *LOW*. (While the LM10 is guaranteed to saturate to 1.2V, the forward drop of the LED in the 4N28 may be as low as 1.0V, so a diode is added in series with the LED, to insure that it can be shut off.) Note that most operational amplifiers will not respond in a reasonable way if the output pin (6) is connected to the positive supply pin (7), but the LM10 was specifically designed and is specified to perform accurately in this "shunt" mode. (Refer to AN-211 application note, TP-14 technical paper, and the LM10 data sheet.)



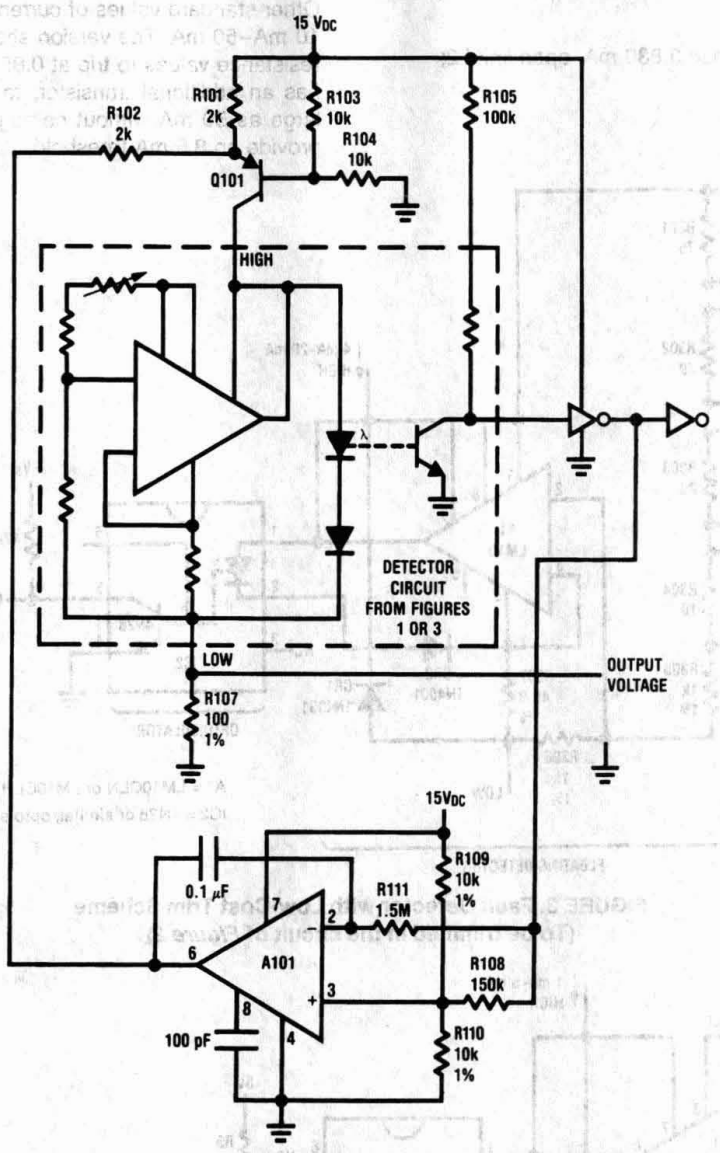
CR1 = 1N4001, optional, in case of signal reversal
LM10 = NSC LM10CLN or LM10CLH amp/reference
IC2 = 4N28 or similar, optoisolator
V2 = Normally low; high signifies fault (I < 3.7 mA)
V3 = Normally high; low signifies fault (I < 3.7 mA) (buffered output)
*C1 = 1 μF optional, to avoid false output when large AC current is superimposed on 4.0 mA. Disconnect this capacitor when using with circuit of *Figure 2*.
▷o = 1/6 MM74C04 or similar, CMOS inverter

TL/H/5640–1

FIGURE 1. Current Loop Fault Detector

While you could manually adjust R1 while observing the status of V3 output, this would be a coarse and awkward trim procedure. *Figure 2* shows an improved test circuit which servos the current through the detector circuit, forcing it to be at the threshold value. Then that current can be monitored continuously, and the circuit can be trimmed easily. If the current through R107 starts out too small, the output of the 4N28 will be *HIGH* too much of the time, and the op amp output will integrate upwards until the current is at the actual threshold of the detector. The integrator's output will stop at the value where the duty cycle of the 4N28 output is exactly 50%. This occurs when the current through R107 is straddling the threshold value.

The positive feedback via R108 assures that the loop oscillates at approximately 50 cycles per second, with a small, well-controlled sawtooth wave at its output. This mode of operation was chosen to insure that the loop does not oscillate at some high, uncontrolled frequency, as it would be difficult in that case to be sure the duty cycle was exactly 50%. This test circuit is advantageous, because you can measure the trip point directly.



TL/H/5640–2

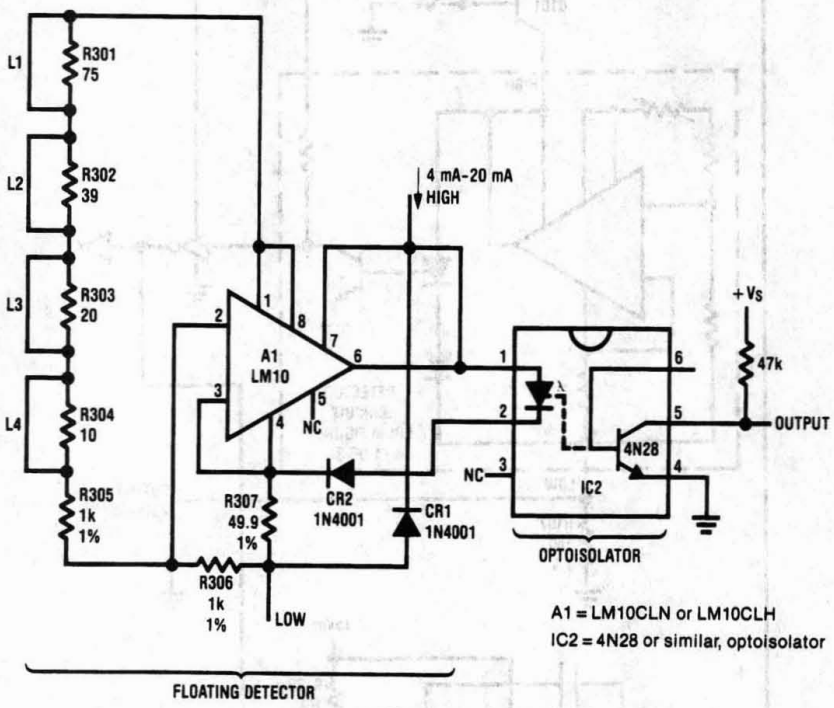
FIGURE 2. Test Circuit for Threshold Detector

The test circuit of *Figure 2* is necessary for trimming the detector in *Figure 3*. This circuit does not have a trim pot, and thus avoids the problem of someone mis-adjusting the circuit after it is once trimmed correctly. It also avoids the compromises between good but expensive trim pots and cheap but unreliable, drifty trim pots. By opening one or more of the links, L1–L4, according to the following procedure, it is easy to trim the threshold level to be within 1% of 3.70 mA (or as desired).

- Observe the DC current through R107 in *Figure 2*
- If $I_{THRESHOLD}$ is larger than 3.950 mA, open link L1; —if not, don't
- If $I_{THRESHOLD}$ is larger than 3.830 mA, open link L2; —if not, don't
- If $I_{THRESHOLD}$ is larger than 3.760 mA, open link L3; —if not, don't
- Then, if $I_{THRESHOLD}$ is larger than 3.720 mA, open link L4;—if not, don't

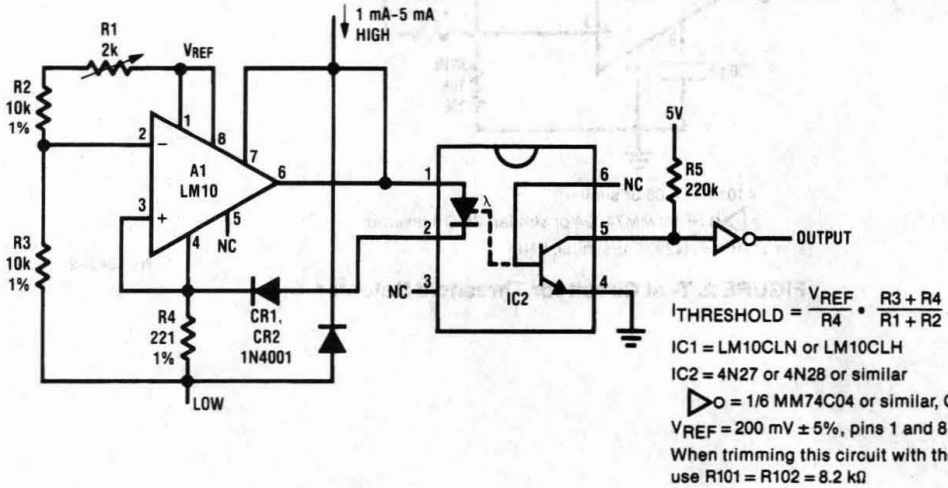
This procedure provides a circuit trimmed to much better than 1% of 3.70 mA, without using any trim pots. Of course, this circuit can be used to detect drop-out of regulation of other floating signals, while maintaining high isolation from ground, good accuracy, low power dissipation (2 mA × 2.5V typical) and low cost.

Other standard values of current loop are 1 mA–5 mA and 10 mA–50 mA. The version shown in *Figure 4* uses higher resistance values to trip at 0.85 mA. The circuit in *Figure 5* has an additional transistor, to accommodate currents as large as 50 mA without damage or loss of accuracy, and provide an 8.5 mA threshold.



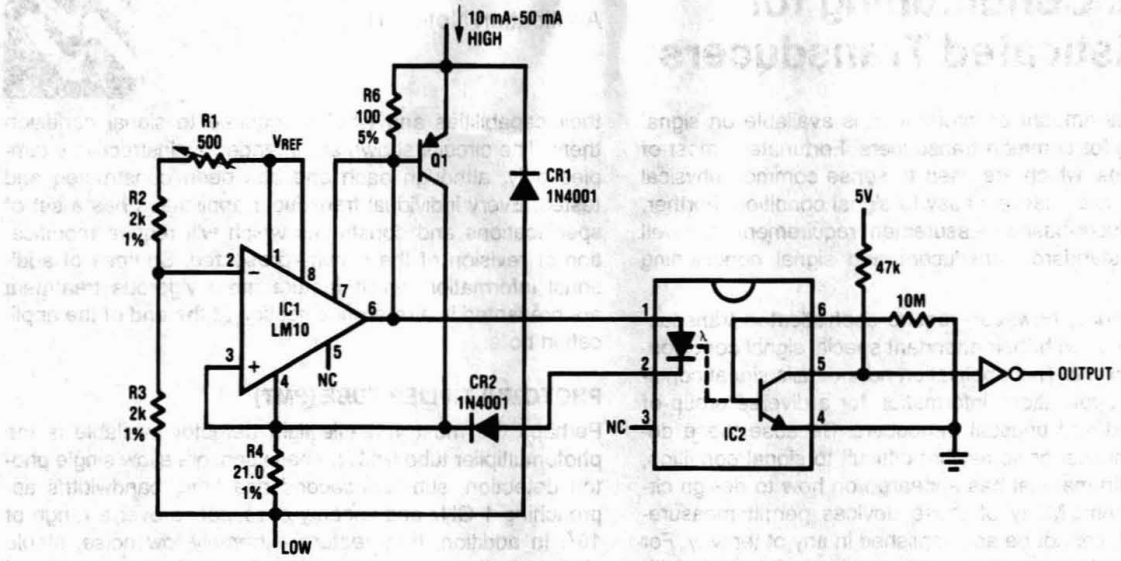
TL/H/5640–3

FIGURE 3. Fault Detector with Low-Cost Trim Scheme (To be trimmed in the circuit of *Figure 2*)



TL/H/5640–4

FIGURE 4. Current Loop Fault Detector ($I_{THRESHOLD}$ = 0.85 mA for 1 mA–5 mA Current Loops)



$$-I_{THRESHOLD} = \frac{V_{REF}}{R4} \bullet \frac{R3 + R4}{R1 + R2}$$

IC1 = LM10CLH or LM10CLN op amp and reference

V_{REF} = 200 mV ± 5%, pins 1 and 8 referred to pin 4

IC2 = 4N28 or similar, optoisolator

▷o = 1/6 MM74C04 or similar, CMOS inverter

Q1 = 2N2904 or 2N2907, any silicon PNP

When trimming this circuit with the circuit of *Figure 2*, use R101 = R102 = 820Ω

TL/H/5640–5

FIGURE 5. Current Loop Fault Detector ($I_{THRESHOLD}$ = 8.5 mA, for 10 mA–50 mA Current Loops)

Signal Conditioning for Sophisticated Transducers

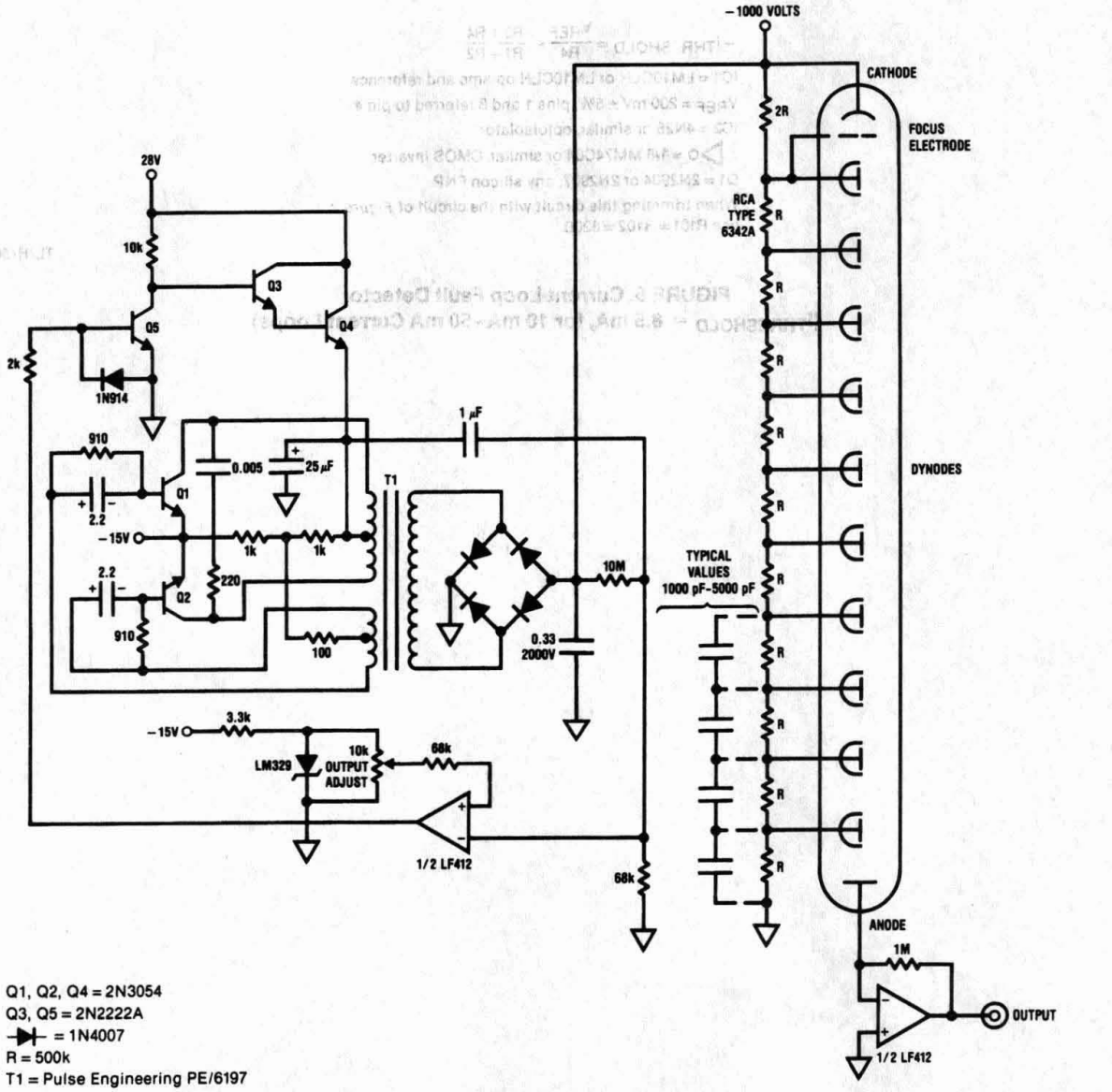
National Semiconductor
Application Note 301

A substantial amount of information is available on signal conditioning for common transducers. Fortunately, most of these devices, which are used to sense common physical parameters, are relatively easy to signal condition. Further, most transducer-based measurement requirements are well served by standard transducers and signal conditioning techniques.

Some situations, however, require sophisticated transduction techniques with their attendant special signal conditioning requirements. This application note details signal conditioning and applications information for a diverse group of sophisticated and unusual tranducers. Because these devices are unusual or somewhat difficult to signal condition, relatively little material has appeared on how to design circuitry for them. Many of these devices permit measurements which cannot be accomplished in any other way. For this reason it is worthwhile to have a basic familiarity with their capabilities and what is required to signal condition them. The circuits shown are intended as instructive examples only, although each one has been constructed and tested. Every individual transducer application has a set of specifications and constraints which will require modification or revision of the circuits presented. Sources of additional information which feature more vigorous treatment are presented in a reference section at the end of the application note.

PHOTOMULTIPLIER TUBE (PMT)

Perhaps the most versatile light detector available is the photomultiplier tube (PMT). These sensors allow single photon detection, sub-nanosecond rise time, bandwidths approaching 1 GHz and linearity of response over a range of 10^7. In addition, they feature extremely low noise, stable characteristics and very long life. *Figure 1a* details a typical



Q1, Q2, Q4 = 2N3054
Q3, Q5 = 2N2222A
→|← = 1N4007
R = 500k
T1 = Pulse Engineering PE/6197

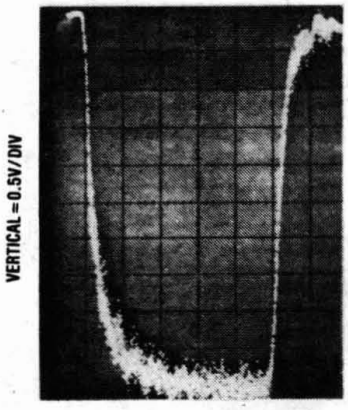
FIGURE 1a

TL/H/5641–1

PMT along with a signal conditioning circuit. The tube is composed of a photosensitive cathode, an anode, a focusing electrode and ten dynode stages. In operation, the photocathode, which is high voltage biased with respect to the dynodes, emits photoelectrons when it is struck by light. These are focused into a beam and directed to the first dynode stage by the focus electrode. These arriving electrons impinge on the dynode, causing secondary emission to occur. As a result, a greater number of electrons leave the dynode and are then directed to the second dynode. In this fashion, a number (e.g.,10) of dynode stages are used to achieve overall gains of 10^6 to 10^8. The electrons from the final dynode are collected by the anode, which provides the output current of the tube. In contrast to other vacuum tubes, the PMT does not use a filament to thermionically generate electrons. Instead, the photocathode, in combination with incident light, initiates the electrons. The absence of a filament means there are no degradation, heat or outgassing problems and the life of a PMT is very long.

Signal conditioning involves generating a stable high voltage supply and accomplishing a low noise current-to-voltage conversion at the anode. In this example, a DC-DC converter is used to supply the dynode potentials to the tube. The supply is stabilized by the LF412 amplifier which drives the Q3-Q5 combination to complete a feedback loop around the Q1-Q2 driven transformer. The LM329 provides a stable servo reference. In general, the regulation of a PMT supply should be at least ten times greater than the required measurement gain stability because of the relationship between a PMT's gain slope and the high voltage applied. The cathode and dynodes are biased from the high voltage supply via divider resistors. The resistors distribute the dynode potentials in proportion to a ratio which is specified for each tube type. To prevent non-linear response, the current through the divider string should be at least ten times the maximum expected current out of the tube. Some high speed pulse applications can generate transient high tube currents which may require the small capacitors shown in dashed lines. The anode is the tube output and appears as an almost ideal current source. The LF412 amplifier performs a current-to-voltage conversion with the 1 MΩ resistor setting the output scale factor.

The PMT's combination of high speed and extreme sensitivity suits it to a variety of difficult light measurement chores. The remarkable photograph of *Figure 1b* shows the actual rise and fall time characteristics (inverted) of a fast pulse of light produced by an LED. This photo was taken with a high speed PMT which was terminated directly into a 1 GHz bandwidth, 50Ω sampling oscilloscope.

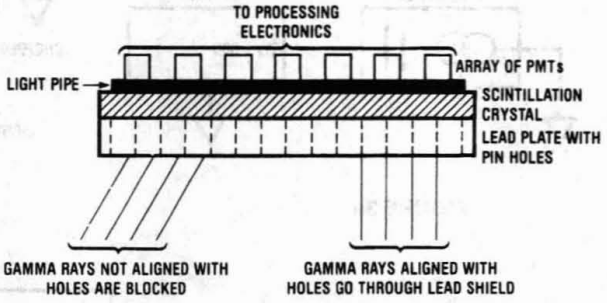


TL/H/5641–2

FIGURE 1b

Another PMT application exchanges speed for sensitivity in a nuclear medical instrument, the Gamma camera.

The Gamma camera operates by using the scintillation properties of special crystals which are placed in front of an array of PMTs. Small quantities of radioactive isotopes are introduced into the patient either by oral ingestion or injection. Specific isotopes collect at certain organs within the body. As the radioactive isotopes decay, gamma rays are emitted from the isotope concentration area. These rays are collimated by a lead plate containing many small holes which forms the front of the camera (*Figure 2a*). This collimator allows only those rays which are at right angles to pass through the plate. The rest are absorbed in the lead. In this fashion the geometric shape of the gamma source is preserved and is presented to the scintillation crystal. The array of PMTs is located behind the crystal. The individual tubes respond to any given scintillation anywhere in the crystal with a distribution of signal strengths. This distribution is used by a processor to determine the precise point of scintillation in the crystal. Each of these scantillation locations is recorded on a CRT. After a length of time, this counting-integration process produces a picture of the organ on the CRT. *Figure 2b* shows 7 such pictures of a pair of human lungs, taken 30 seconds apart over a 150 second period. In photo A, the administered radioactive isotope begins to collect in the lungs. In photo B, the lungs are saturated. During photos C, D, E, F and G, the isotope progressively decays. Normally, human lungs will clear after 120 seconds. This particular sequence shows evidence of an obstructive pulmonary disease which is most pronounced in the lower right lung.


TO PROCESSING ELECTRONICS
ARRAY OF PMTs
LIGHT PIPE
SCINTILLATION CRYSTAL
LEAD PLATE WITH PIN HOLES
GAMMA RAYS NOT ALIGNED WITH HOLES ARE BLOCKED
GAMMA RAYS ALIGNED WITH HOLES GO THROUGH LEAD SHIELD

TL/H/5641–3

FIGURE 2a

PYROELECTRIC DETECTOR

The pyroelectric detector represents another class of sophisticated photodetector. These ceramic-based radiation detectors feature an extraordinary light sensitivity range from microwatts to watts with excellent linearity. Their bandwidth is flat from the ultraviolet to the far infrared. Response is sub-nanosecond and the devices may be operated at room temperature; no cooling is required. A major difficulty and source of confusion with signal conditioning pyroelectrics is that they do not respond at DC. This limitation, which is in keeping with all ceramic-based transducers, is surmounted by using a light chopper in front of the detector. In this fashion, DC light inputs to the detector appear as a modulated carrier. These devices are used in industrial temperature measurement, spectroscopy and laser power meters. They are also used to measure high speed laser pulse characteristics.

For signal conditioning purposes, pyroelectrics can be modeled as either a current source with parallel capacitance or a voltage source with series capacitance. Because there is no resistive component, there is no resistive Johnson noise. *Figure 3a* shows a simple voltage mode set-up which can be used for fast pulses of high energy. In this circuit, the detector is terminated directly into a high speed 50Ω oscilloscope. In *Figure 3b*, a slower detector terminates into 1 MΩ and is unloaded by the LH0052 low bias FET amplifier. For response time much longer than a few milliseconds, the optical chopper provides a modulated light signal to the detector. The amplifier output may be rectified to recover the DC component of the signal. *Figure 3c* shows a current mode signal conditioning circuit. The optical chopper is retained, but the detector is loaded directly into the summing junction of a low bias op amp composed of an LF411 and a pair of sub-picoamp bias FETs. The low bias current allows low energy light measurement.

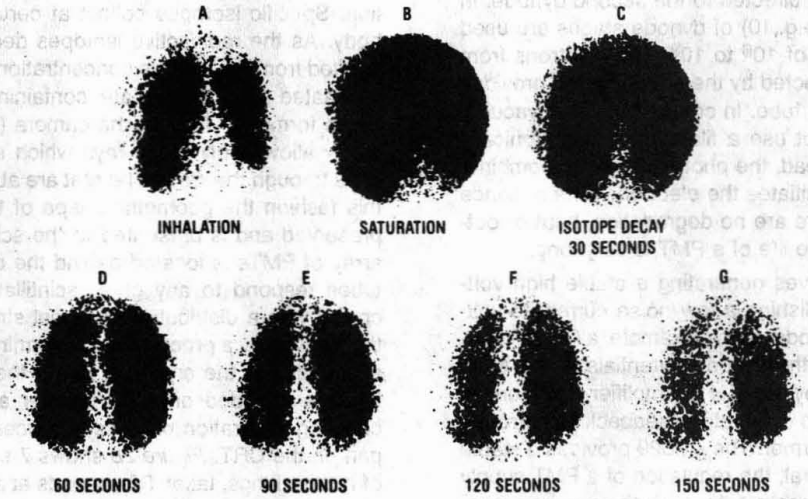


FIGURE 2b

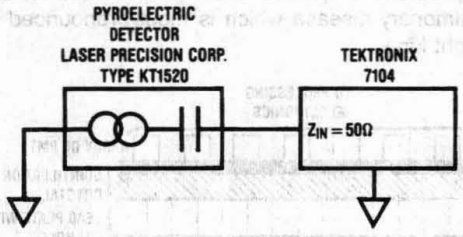
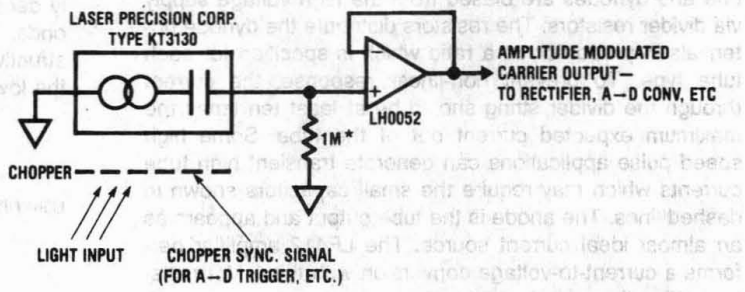
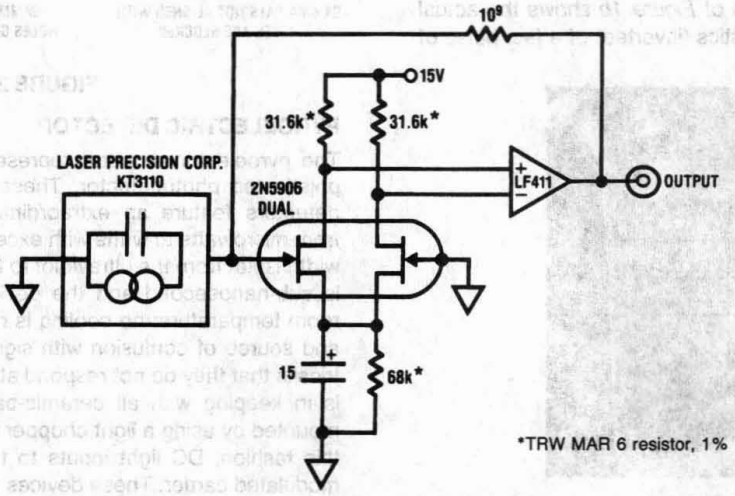


FIGURE 3a



*TRW MAR 6 resistor, 1%

FIGURE 3b



*TRW MAR 6 resistor, 1%

TL/H/5641–4

FIGURE 3c

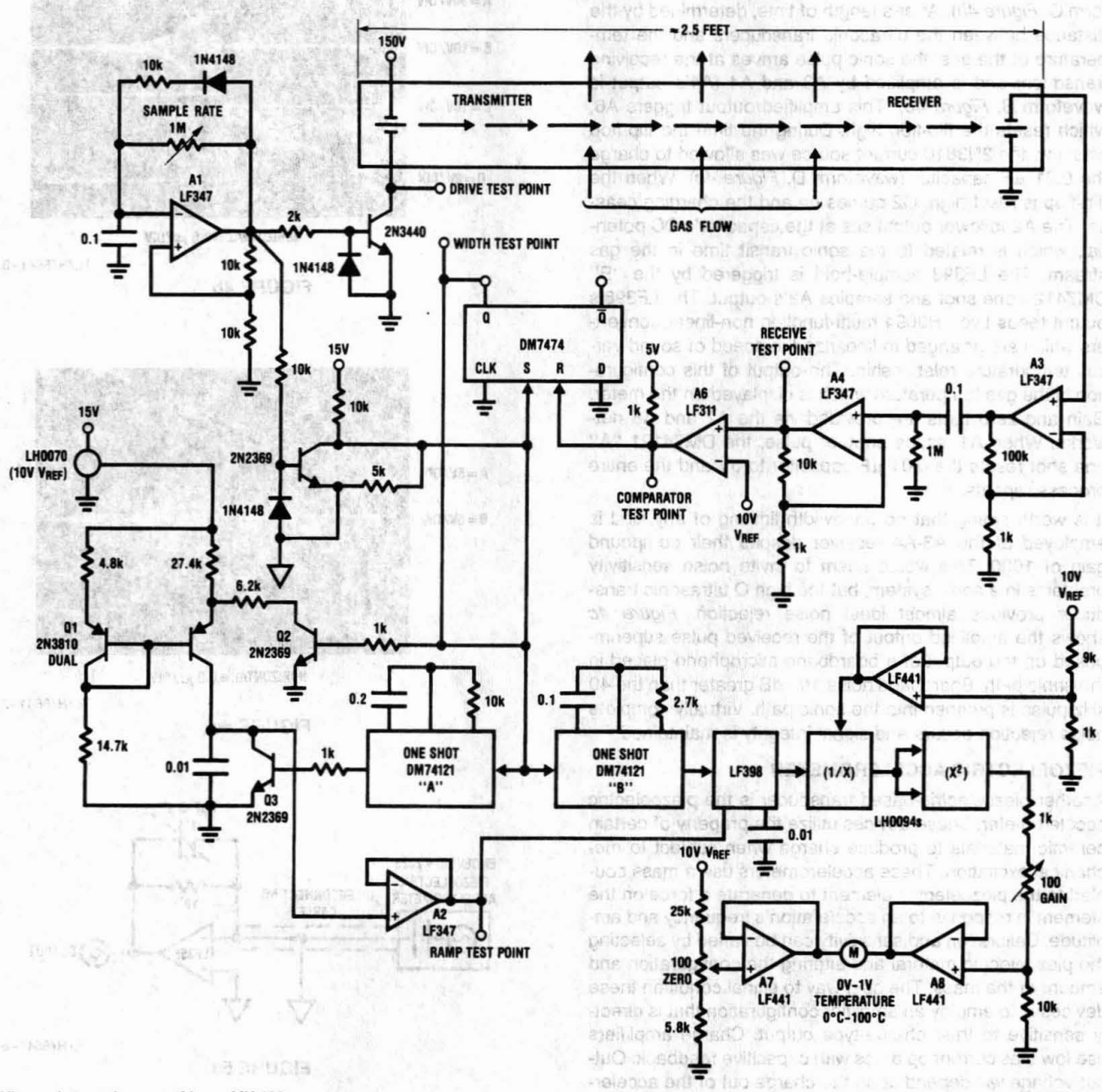
PIEZOELECTRIC ULTRASONIC RESONATORS

Piezoelectric ultrasonic tranducers are generically related to pyroelectrics in that they are also ceramic-based. These devices are used for both generation and reception of narrow band ultrasonic information. The characteristic resonance of these transducers, in a similar fashion to quartz crystals, is extremely narrow, allowing high Q, noise rejecting systems to be built around them. As transmitters, they are often driven very hard by steps several hundred volts high at low duty cycles. This permits substantial ultrasonic power to be generated and eases the burden of the receiver in the system (which could be the same transducer as the transmitter). Ultrasonic resonators are used in a wide variety of applications including liquid level detection, intrusion alarms, automatic camera focusing, cardiac ultrasonic profiling (echocardiography) and distance measuring equipment. *Figure 4a* shows a signal conditioning circuit which capitalizes on the high Q, noise rejection characteristics and fast response of ultrasonic transducers to accomplish a difficult thermal measurement. This circuit is similar to a type developed to measure high speed temperature shifts in a gas medium.

In contrast to almost all other temperature sensors, it does not rely on its sensing element to come into thermal equality with the measurand. Instead, the relationship between the speed of sound and the temperature of the medium in which the sound is propagating is utilized to determine temperature. The speed of response is therefore very fast and the measurement is also non-invasive. The relationship between the speed of sound in any medium and temperature may be described by equations. As an example, the relationship in dry air is:

$$C = 331.5\sqrt{\frac{T}{273}} \text{ meters/second,}$$

where C = speed of sound.



Ultrasonic transducers = Massa MK-109

TL/H/5641–5

FIGURE 4a

For any given value of C the absolute temperature is:

$$T = \frac{273}{(331.5)^2} \times C^2.$$

It is clear that because sound speed and the medium in which it travels have a predictable relationship, a temperature transducer can be composed of the medium itself. If the characteristics of the medium can be defined (e.g., its make up) the transmit time of a sonic pulse through it can be used to determine its temperature. If narrow band ultrasonic transducers are used, they will reject sonic noise that may be occurring in the medium.

A1 periodically generates a short pulse (waveform A, *Figure 4b*) that drives the 2N3440 into conduction, forcing the ultrasonic 40 kHz transducer to emit a short burst at its resonant frequency. The 150V pulse amplitude allows substantial ultrasonic energy to be coupled into the medium. As this pulse is generated, the DM7474 flip-flop is set low (waveform C, *Figure 4b*). After a length of time, determined by the distance between the ultrasonic transducers and the temperature of the gas, the sonic pulse arrives at the receiving transducer and is amplified by A3 and A4 (A4's output is waveform B, *Figure 4b*). This amplified output triggers A6, which resets the flip-flop high. During the time the flip-flop was low, the 2N3810 current source was allowed to charge the 0.01 μF capacitor (waveform D, *Figure 4b*). When the flip-flop is reset high, Q2 comes on and the charging ceases. The A2 follower output sits at the capacitor's DC potential, which is related to the sonic transit time in the gas stream. The LF398 sample-hold is triggered by the "B" DM74121 one shot and samples A2's output. The LF398's output feeds two LH0094 multi-function non-linear converters which are arranged to linearize the speed of sound versus temperature relationship. The output of this configuration is the gas temperature which is displayed on the meter. Gain and zero trims are provided via the A7 and A8 networks. When A1 issues another pulse, the DM74121 "A" one shot resets the 0.01 μF capacitor to 0V and the entire process repeats.

It is worth noting that no bandwidth limiting of any kind is employed at the A3-A4 receiver despite their compound gain of 1000. This would seem to invite noise sensitivity problems in a sonic system, but the high Q ultrasonic transducer provides almost ideal noise rejection. *Figure 4c* shows the amplified output of the received pulse superimposed on the output of a boardband microphone placed in the sonic path. Boardband noise 100 dB greater than the 40 kHz pulse is pumped into the sonic path. Virtually complete noise rejection occurs and signal integrity is maintained.

PIEZOELECTRIC ACCELEROMETER

Another piezoelectric-based transducer is the piezoelectric accelerometer. These devices utilize the property of certain ceramic materials to produce charge when subject to mechanical excitation. These accelerometers use a mass coupled to the piezoelectric element to generate a force on the element in response to an acceleration's frequency and amplitude. Calibration and sensitivity can be varied by selecting the piezoelectric materal and altering the configuration and amount of the mass. The best way to signal condition these devices is to employ an amplifier configuration that is directly sensitive to their charge-type output. Charge amplifiers use low bias current op amps with capacitive feedback. Output voltage will depend upon the charge out of the accelerometer which is related to the applied acceleration.

In *Figure 5a*, the transducer looks directly into the ground potential summing junction of an op amp. Because of this, there is no voltage difference between the interconnecting cable center conductor and its shield. This eliminates cable capacitance effects on the transducer output and allows long cable runs. It is advisable to use cable specified for low triboelectric charge effects for best performance, although this is usually only a factor with relatively low output devices. The $10^{11}\Omega$ resistor provides a DC feedback path, while the variable capacitor sets the sensitivity of the charge-to-voltage conversion. When the accelerometer shown is mounted on a hand-held voltmeter and dropped on the floor, the instantaneous acceleration to which the voltmeter is subjected can be determined. In *Figure 5b,* the stored trace display

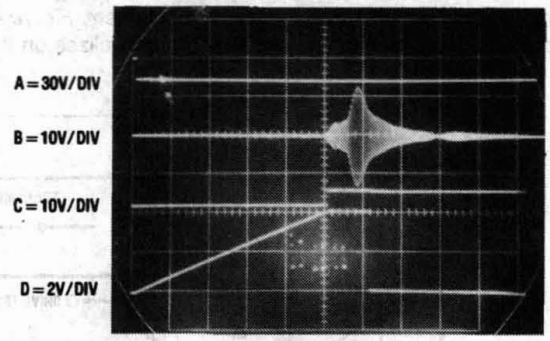


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FIGURE 4b

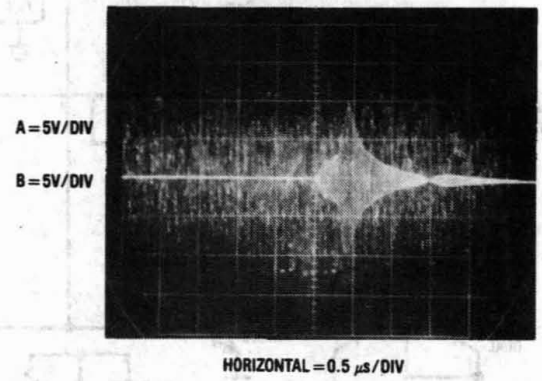

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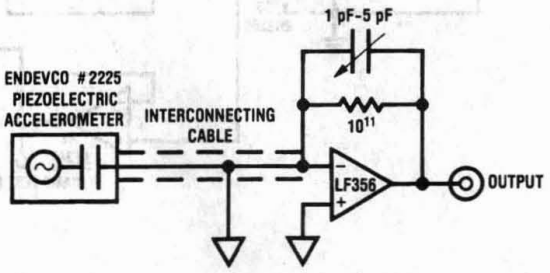
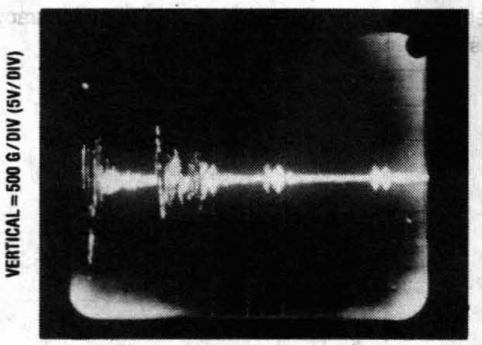
FIGURE 4c



TL/H/5641–8

FIGURE 5a

shows an instantaneous force of almost 1000G with smaller forces generated as the voltmeter bounces 3 times over 60 ms. (It is recommended that this experiment be performed with a borrowed voltmeter.)

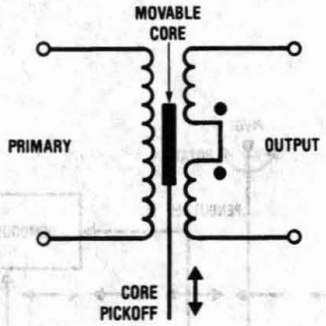


TL/H/5641–9

FIGURE 5b

LINEAR VARIABLE DIFFERENTIAL TRANSFORMER (LVDT)

The linear variable differential transformer (LVDT) offers zero-friction position sensing with good precision. Although potentiometers are easy to signal condition and allow high precision they cannot match the nearly infinite life and zero-friction of the LVDT approach. LVDTs are available in both rotary and stroke mechanical configurations. The LVDT is basically a transformer (*Figure 6a*) with a movable core. The primary is driven with a sine wave which is usually amplitude stabilized. The two matched secondaries are connected in series-opposed fashion. When the movable core is positioned in the magnetic (and usually geometric) center of the transformer, the secondaries' outputs cancel and no net secondary voltage appears. This is called the null position. As the core is moved from null, the differential in flux coupled to the two secondaries produces a net voltage difference across them.



TL/H/5641-10

FIGURE 6a

This is the output of transducer. Good transducer performance (e.g., null cancellation characteristics, linearity, etc.) requires manufacturer attention to winding techniques, magnetic shielding, material choices and other issues. Rectifying and filtering the output signal will yield only amplitude information. Optimum signal conditioning requires a phase sensitive demodulation scheme. This gives the amplitude and also polarity information necessary to determine on which side of null the LVDT core is.

Figure 6b shows a circuit which does this. Waveforms of operation are given in *Figure 6c*. In this circuit, Q1 and its associated components from a phase shift oscillator which runs at 2.5 kHz, the manufacturer's specified transducer operating frequency. A1A amplifies and buffers Q1's output and drives the LVDT (waveform A, *Figure 6c*). Since the transducer's output will vary with drive level, feedback is used to stabilize the 2.5 kHz amplitude. A1C and A1D full wave rectify a sample of the drive waveform. A1C's filtered output is applied to A1D, a servo amplifier. A1D compares A1C's output to the LM329 reference and drives the Q1 oscillator to complete an amplitude stabilization loop. The LVDT's output is amplified by A2C and fed to A2A. A2A is a unity gain ampilifer whose sign alternates between "+" and "−". Synchronous switching for A2A comes from C1 (waveform B, *Figure 6c*), which is driven by the modulation sine wave output via a phase shift network. The phase trim network compensates phase shift in the LVDT and ensures that C1 switches at the zero crossings relative to A2A's output. When C1's output is low, the 2N4393 FET is off and A2A's positive input (waveform C, *Figure 6c*) receives signal. When the sine wave reverses polarity, C1's output goes high, turning on the FET, which grounds A2A's "+" input. Under these conditions A2A is always switching its amplification's sign from "+" to "−" in synchronism with the sine wave output from the LVDT. A2A's phase sensitive output, in this case positive, appears in trace D, *Figure 6c*. A2B provides a scaled and filtered DC output. To trim the circuit, set the LVDT to at least ½ physical displacement and adjust the phase trim for maximum output indication. Next, adjust the gain trim for the desired circuit output at full-scale LVDT displacement.

FORCE-BALANCED PENDULOUS ACCELEROMETER

The operating principles of the LVDT are applied in the force-balanced pendulous accelerometer. Transducers of this type feature wide dynamic range, high linearity and very high accuracy. *Figure 7a* shows one form of a conceptual force-balanced pendulous accelerometer. The device operates by using an LVDT-type pick-off to determine the position of the pendulum. The DC output of the LVDT is fed to a servo amplifier which drives the torque coil. The magnetic output of the torque coil completes a servo loop around the pendulum, forcing it to become immobile. Because the torque coil's field can attract only the pendulum, a second bias coil provides a steady force for the torque coil to work against. When an input acceleration occurs along the sensitive axis, the servo applies the necessary current to the torque coil to keep the pendulum from moving. The amount of current required is directly proportional to the value of the input acceleration. Because the pendulum never moves, transducer linearity and accuracy can be very high. In addition, wide dynamic range is possible. Force-balanced accelerometers are widely applied in aircraft inertial guidance systems, aerospace applications, seismic monitoring, shock and vibration studies, oil drilling platform stabilization and similar applications. In recent years these accelerometers have become available in complete signal conditioned packages, although there are a number of applications where it is desirable to independently signal condition the transducer. *Figure 7b* shows a detailed schematic of such signal conditioning. The pick-off circuitry is similar to the LVDT shown in *Figure 6b* and does not require further comment. The bias coil is driven by the LH0002 boosted LF347 (A1A) which is in a current sensing feedback configuration. For the accelerometer shown, the manufacturer specifies

60 mA of bias coil current. Torque pulses are applied by servo amplifier A3B, which is biased from the LVDT demodulator output. The output of the circuit is taken across the 100Ω resistor in series with the torque coil. Servo gain is set at A3B while damping for the loop is provided by the 1 μF unit in A3B's feedback loop. In addition, accelerometer damping is controlled by stabilizing the temperature of the mechanical assembly. This is accomplished by A3C, which is set up as a simple on-off temperature controller. The interior of the accelerometer is filled at manufacture with a liquid whose viscosity provides appropriate damping characteristics at a specified temperature, in this case 180°F. Accelerometers of this type routinely yield 100ppm accuracy from ranges of 20 mG to 100G.

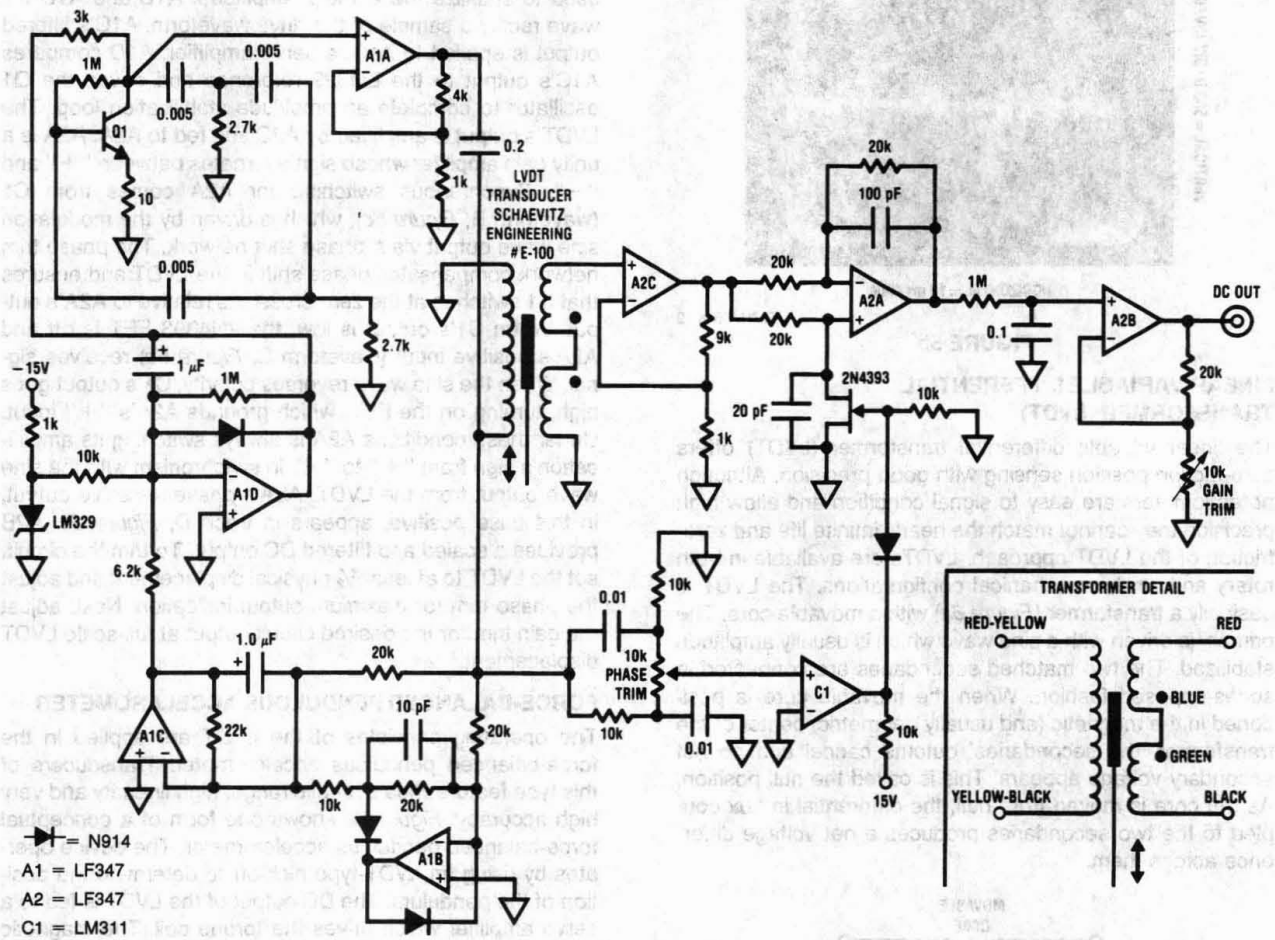


FIGURE 6b

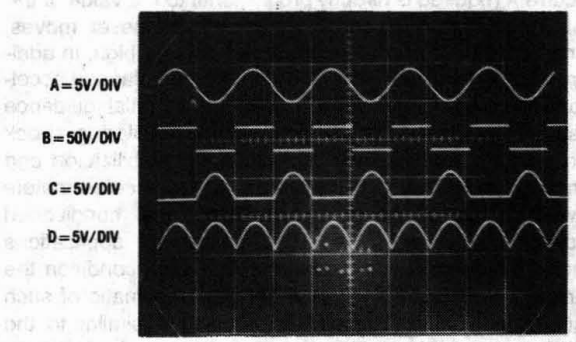


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FIGURE 6c

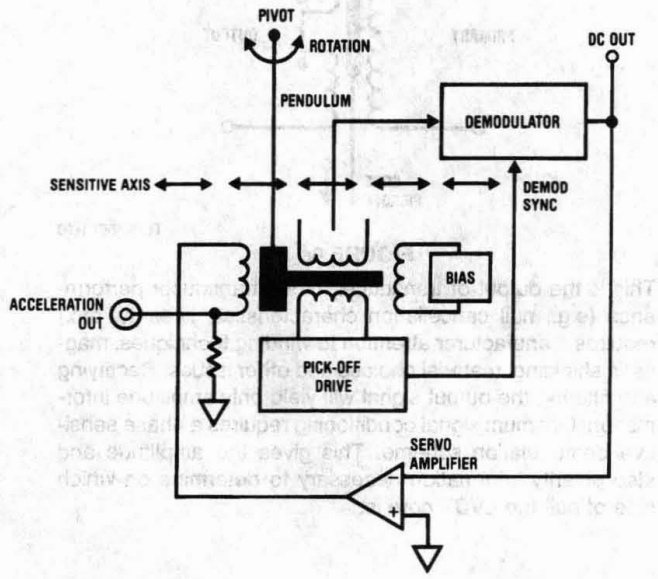

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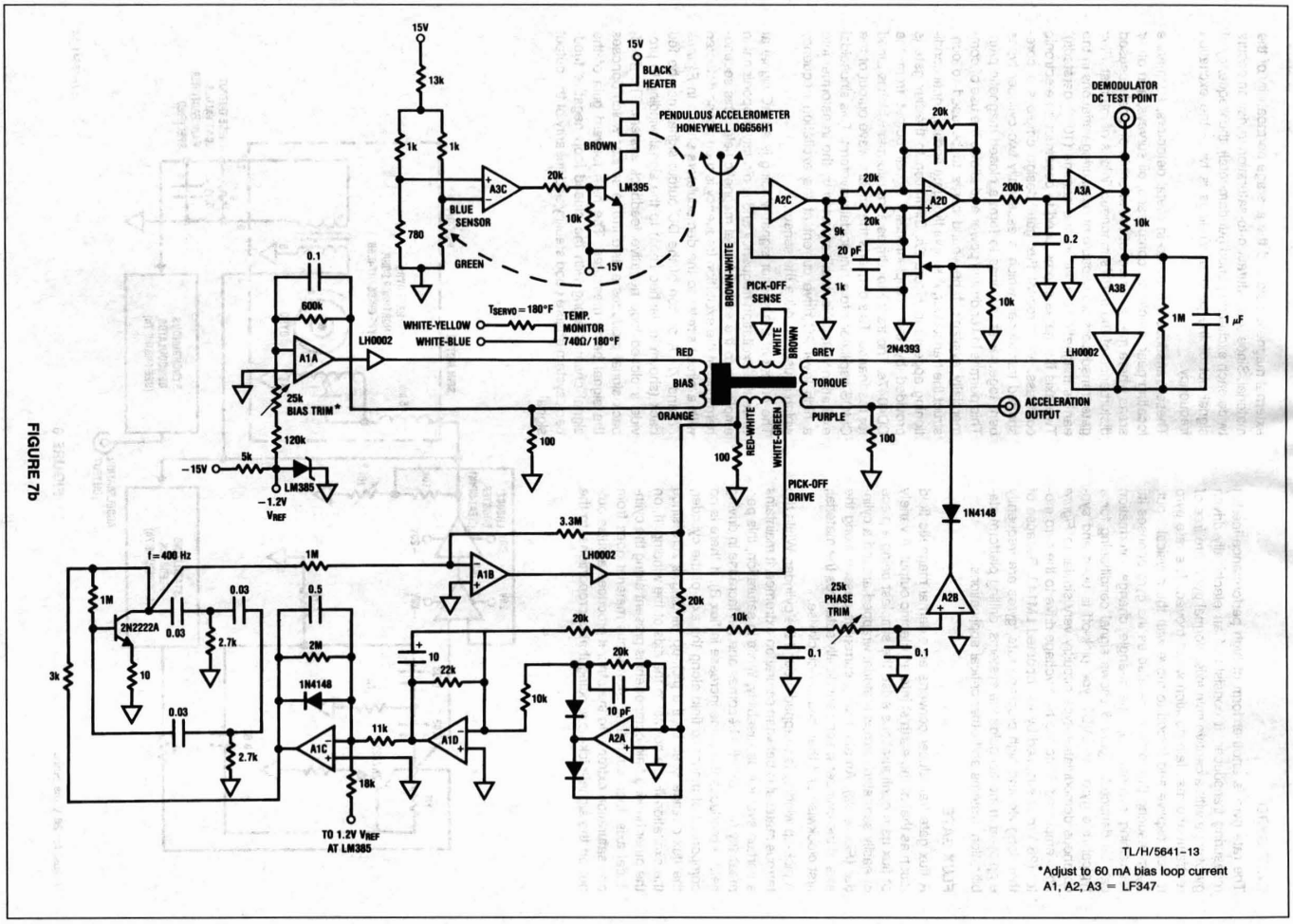
FIGURE 7a



TL/H/5641–13

*Adjust to 60 mA bias loop current
A1, A2, A3 = LF347

FIGURE 7b

RATE GYRO

The rate gyro is another form of high performance inertial measuring transducer. It consists of an electrically driven gyroscope with a captive spin axis. Normal gyros are free of restraint and maintain position when moved. The rate gyro is held captive and forced to move with the physical input. By measuring the force generated as the gyro opposes its restraining mechanism, rate-of-angle change information can be deduced. *Figure 8* shows signal conditioning for a typical rate gyro. An LVDT-type pick-off is used and synchronous demodulation-type circuitry very similar to *Figure 7b* is employed. Note the high voltage drive to the gyro motor (26 Vrms) supplied by the boosted LM143. Because of their long life and high precision rate, gyros are frequently employed in inertial guidance systems, drilling platform stabilization systems and other critical applications.

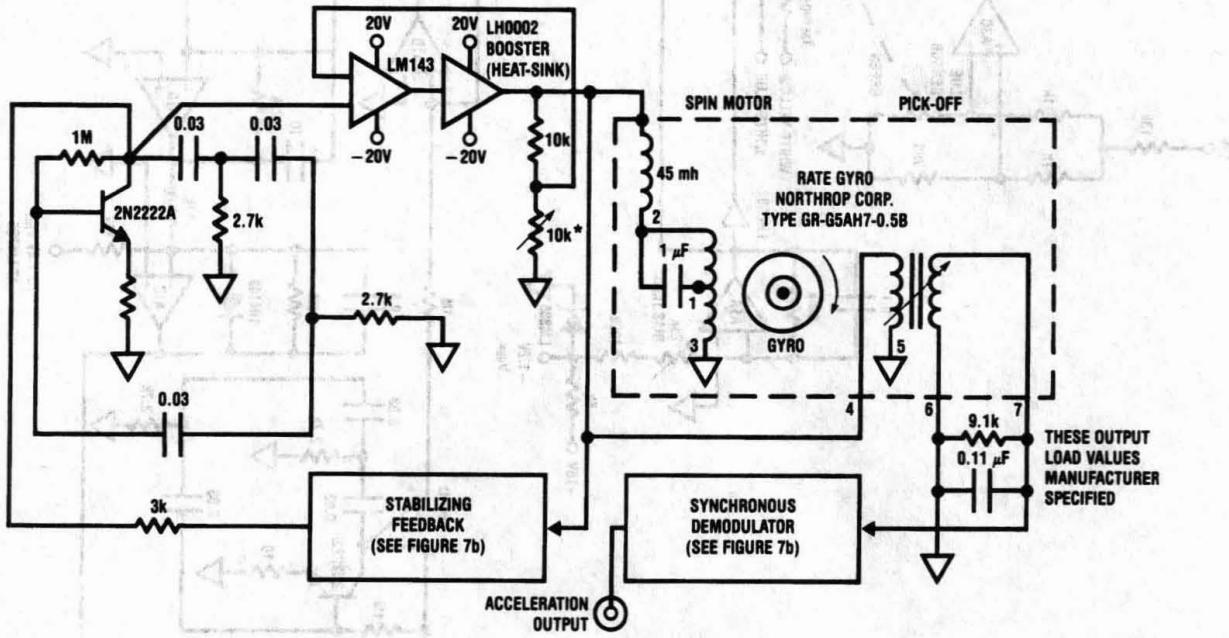
FLUX GATE

A flux gate transducer converts an external magnetic field (such as that of the earth's) into an electric output. A variety of flux gate configurations exist, the simplest being a piece of easily saturable ferrous material wrapped around a cylinder (*Figure 9a*). An alternating current is passed along the axis of the cylinder which periodically saturates the material, first clockwise and then counter-clockwise.

A pick-up winding is wrapped around the cylinder. While the ferrous material is between saturation extremes, it maintains a certain average permeability. While in saturation, this permeability (μ = dB/dH) becomes one (an increase in driving field H produces the same increase in flux B). If there is no component of magnetic field along the axis of the cylinder, the flux change seen by the pick-up winding is zero since the excitation flux is normal to the axis of the winding. If, on the other hand, a field component is present along the cylindrical axis, then each time the ferrous material goes from one saturation extreme to the other it produces a pulse output on the signal pick-up winding that is proportional to the external magnetic field and the average permeability of the material. Since this saturation-to-saturation transition occurs twice each excitation period (fundamental), the frequency of signal out of the pick-up windings is twice the excitation frequency.

These transducers find use in metal detectors, submarine locating gear, electronic compasses, oil surveys, and other areas where measurement of the strength or locally caused disturbance of the earth's magnetic field is of interest. Flux gate transducers are capable of measuring variations in the earth's magnetic field within one gamma (10^{-5} oersteds). Two axis flux gates can be used to construct an electronic compass. More recent flux gate design employs a core-shaped transducer, which is essentially two cylinder types bent together at the ends to form a closed magnetic path. This permits lower driving power and allows the use of commercially available tape-wound cores to be used to construct the transducer. A simple flux gate and its signal conditioning appears in *Figure 9b*. Excitation to the flux gate is provided by the complementary signal output from the CD4047s. The transistor drives a transformer which is tuned for resonance. This converts the square wave output of the CMOS oscillator into a sinusoidal waveform. This sinusoidal excitation voltage is then converted by the transformer into a high level AC drive current at the excitation frequency which is used to drive the sensor.

The output of the sensor signal winding is an AC signal at twice the excitation frequency and is directly proportional in amplitude to the external axial magnetic field. This second-harmonic of the excitation frequency is then phase detected with a circuit similar to the demodulators shown in *Figures 6b* and *7b*. A portion of the DC output signal may be fed back (shown in dashed lines) to the signal winding to provide a closed loop negative feedback system. This feedback signal produces a field in the sensor which opposes the signal being measured. The high forward gain of the signal channel along with the closed loop negative feedback system ensure good stability and linearity of the output signal.



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*Adjust for 26 Vrms output

FIGURE 8

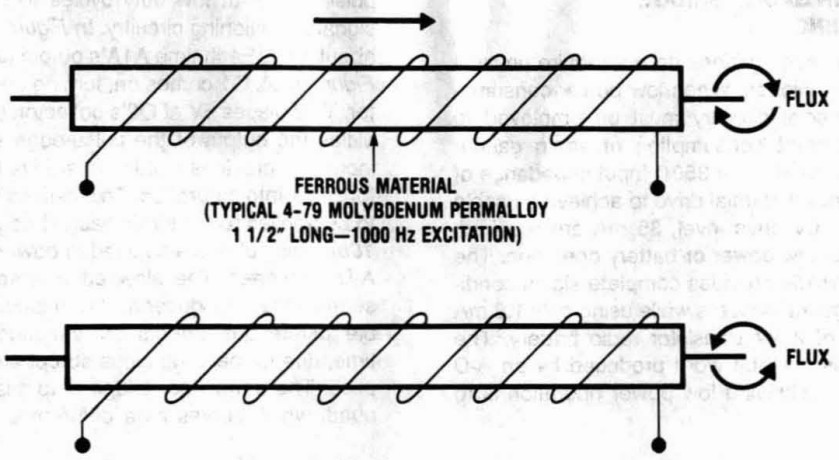

FIGURE 9a

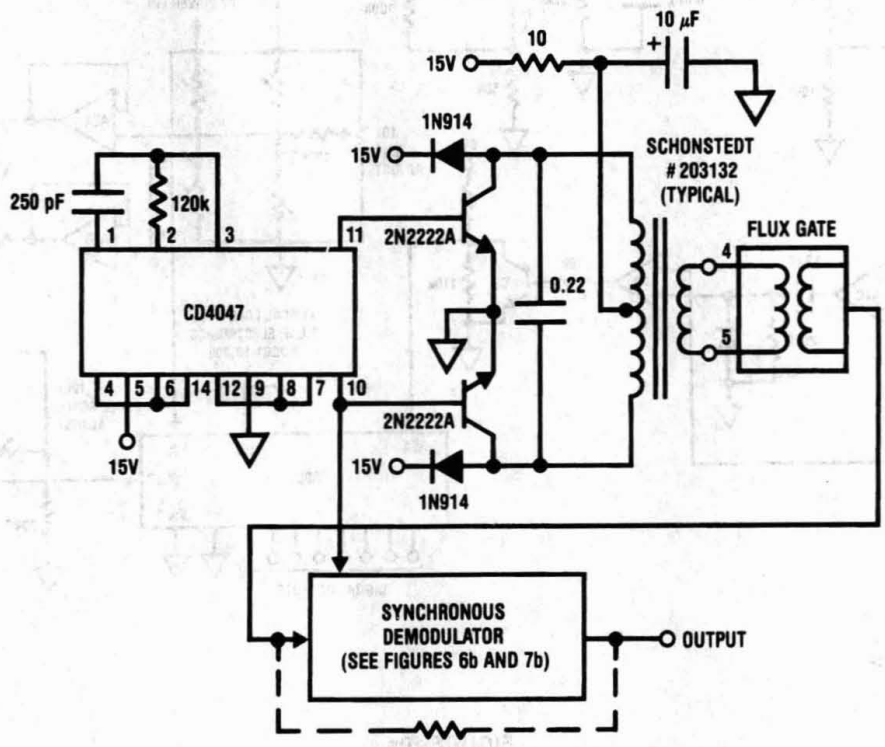

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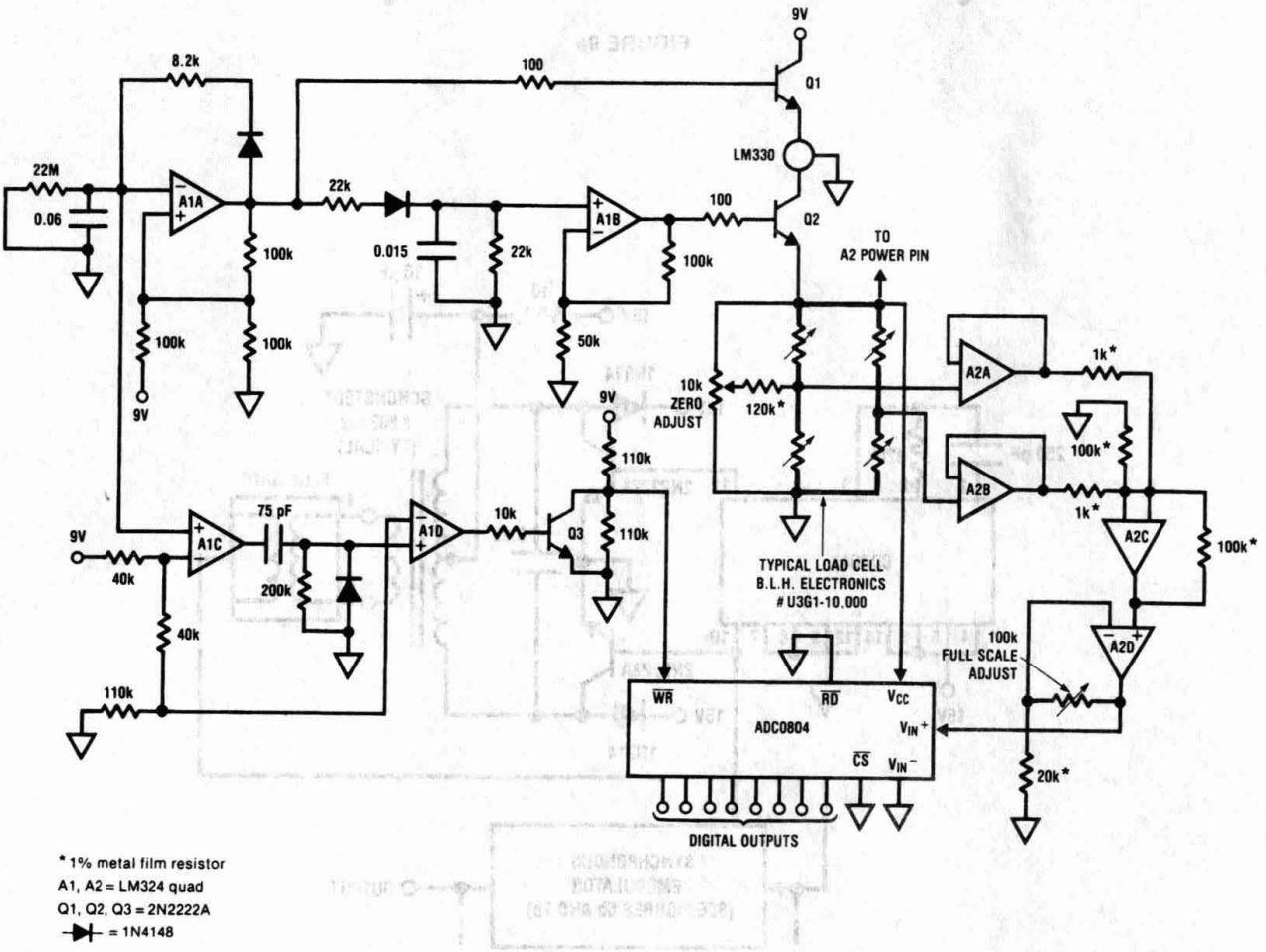
FIGURE 9b

LOW POWER STRAIN GAUGE BRIDGE SIGNAL CONDITIONING

In most cases, strain gauge bridges do not require unusual signal conditioning techniques. When low power consumption is necessary, special circuitry must be employed to eliminate the high current consumption of strain gauge-based transducers. Normally, the 350Ω input impedance of these devices requires substantial drive to achieve a usable output. For a typical 10V drive level, 35 mA are required; hardly compatible with low power or battery operation. The circuit shown in *Figure 10a* provides complete signal conditioning for strain gauge transducers while using only 1.8 mA average current out of a 9V transistor radio battery. The output of the circuit is an 8-bit word produced by an A-D converter. The key to achieving low power operation is to pulse power at low duty cycles to the transducer and its signal conditioning circuitry. In *Figure 10b*, A1A oscillates at about 1 Hz. Each time A1A's output goes high (waveform A, *Figure 10b*), Q1 comes on, turning on the LM330 5V regulator. This places 5V at Q2's collector. Concurrently, A1B amplifies the output of the pulse-edge shaping network at its input and provides voltage overdrive to emitter-follower Q2, forcing it into saturation. This causes an edge shaped pulse to be applied to the strain gauge bridge (waveform B, *Figure 10b*). This pulse is also used to power A2 and the ADC0804 A-D converter. The slow edge shaping limits the DV/DT seen by the transducer as it is pulsed. This eliminates possible deleterious effects on transducer performance over time, due to the continuous abrupt step functions being applied. The transducer bridge output is monitored by the A2 quad, which serves as a differential input (A2A and A2B),



* 1% metal film resistor
A1, A2 = LM324 quad
Q1, Q2, Q3 = 2N2222A
→|← = 1N4148

TL/H/5641-16

FIGURE 10a

single-ended output (A2C and A2D) amplifier. A2D's output (waveform C, *Figure 10b*) feeds the ADC0804 A-D converter. The A-D is triggered by a delayed pulse generated by the A1C and A1D pair (waveform D, *Figure 10b*). This pulse is positioned so that it occurs after A2D's output has settled to final value. To calibrate the circuit, apply zero physical load to the transducer shown and adjust the zero trim so the A-D converter is just below indicating 1 LSB output. Next, apply (or electrically simulate) 10,000 lbs. and adjust the gain trim for a full output code at the A-D converter.

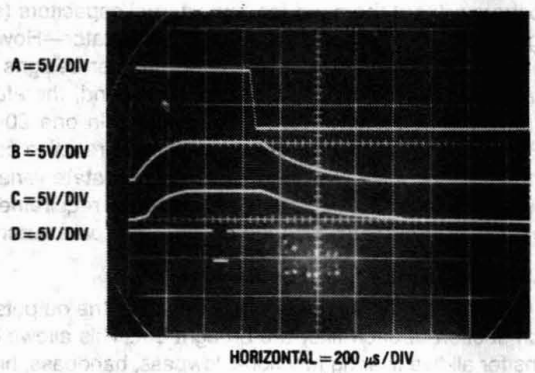


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FIGURE 10b

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Northrop Corporation, Precision Products Division

RCA Electro-Optics Division

Lancaster Radiology Associates

Introducing the MF10: A Versatile Monolithic Active Filter Building Block

National Semiconductor
Application Note 307
Tim Regan

A unique alternative for active filter designs is now available with the introduction of the MF10. This new CMOS device can be used to implement precise, high-order filtering functions with no reactive components required.

Filter design takes one of two approaches: passive or active. Passive designs combine resistors, capacitors and inductors to perform specific frequency filtering in applications where precision is less important than mass producibility. For very high frequency applications, a passive approach is quite often the only way to go. Active filters combine op amps and discrete transistors, primarily with resistors and capacitors, to provide impedance buffering and filter parameter tunability. In precision filters, it is most desirable to have an independent "handle" for each of three basic filter parameters: resonant frequency (f_0), Q or quality factor, and the passband gain (H_0). As a general rule, the degree of tunability increases with the number of amplifiers used. The three op amp, state variable active filter, *Figure 1*, is most popular for 2nd order designs.

A major shortcoming of this type of filter is that resonant frequency accuracy is only as good as the capacitors used. In high volume production, to minimize filter tuning procedures, costly, low-tolerance, low-drift capacitors are required. Furthermore, these filters use a fair number of components; 3 op amps, 7 resistors and 2 capacitors for each 2nd order section. Even the best single amplifier 2nd order filter realizations require 3 to 5 resistors and 2 capacitors.

To offer designers an attractive alternative to these types of active filters, a device would have to:

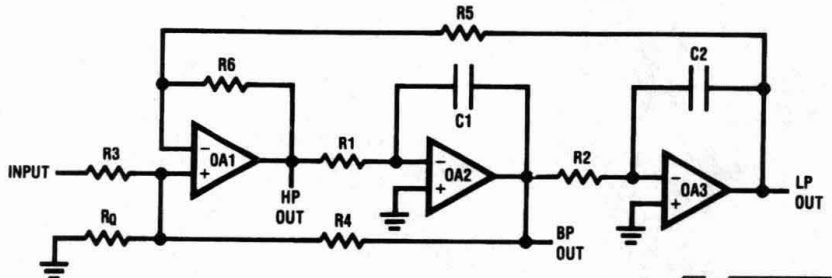
1) eliminate critical capacitors entirely
2) minimize overall parts count
3) provide easy tunability of filter parameters
4) allow for the design of all five filter responses and,
5) simplify design equations.

These are the design objectives behind the development of the MF10. Recent advances in sample-data techniques permit the construction of an op amp integrator on a monolithic substrate without the need for any external capacitors (see page 11 "The Switched Capacitor Integrator—How it Works"). The integrator is a key factor in filter designs for establishing the overall filter time constant and, therefore, its resonant frequency. The MF10 contains, in one 20-pin DIP package, all of the necessary active and reactive components to construct two complete 2nd order state variable type active filters, *Figure 2*. The only external requirements are for resistors to establish the desired filter parameters.

BASIC CIRCUIT DESCRIPTION

To keep the device as universal as possible, the outputs of each section of each filter are brought out. This allows designs for all five filtering functions: lowpass, bandpass, highpass, allpass and bandreject or notch filters. With two independent 2nd order sections in one package, cascading to achieve 4th order responses can easily be accomplished. Additionally, any of the classical filter response types such as Butterworth, Chebyshev, Bessel and Cauer can be implemented.

Between the output of the summing op amp and the input of the first integrator there is a unique 3-input summing stage where two of the inputs are subtracted from the third. One of the (−) inputs is brought out to serve as the signal input for some filter configurations. The other (−) input is connected through an internal switch to either the lowpass output or analog ground depending upon the desired filter implementation. The direction of this input connection is common to both halves of the MF10 and is controlled by the voltage level on the $S_{A/B}$ input terminal.



$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{R1\,R2\,C1\,C2}}$$

$$Q = \left(\frac{1+\frac{R4}{R3}+\frac{R4}{R0}}{1+\frac{R6}{R5}}\right)\sqrt{\frac{R6\,R1\,C1}{R5\,R2\,C2}}$$

TL/H/5035–1

FIGURE 1. The Universal State Variable 2nd Order Active Filter (note the complexity of design equations and the number of critical external components)

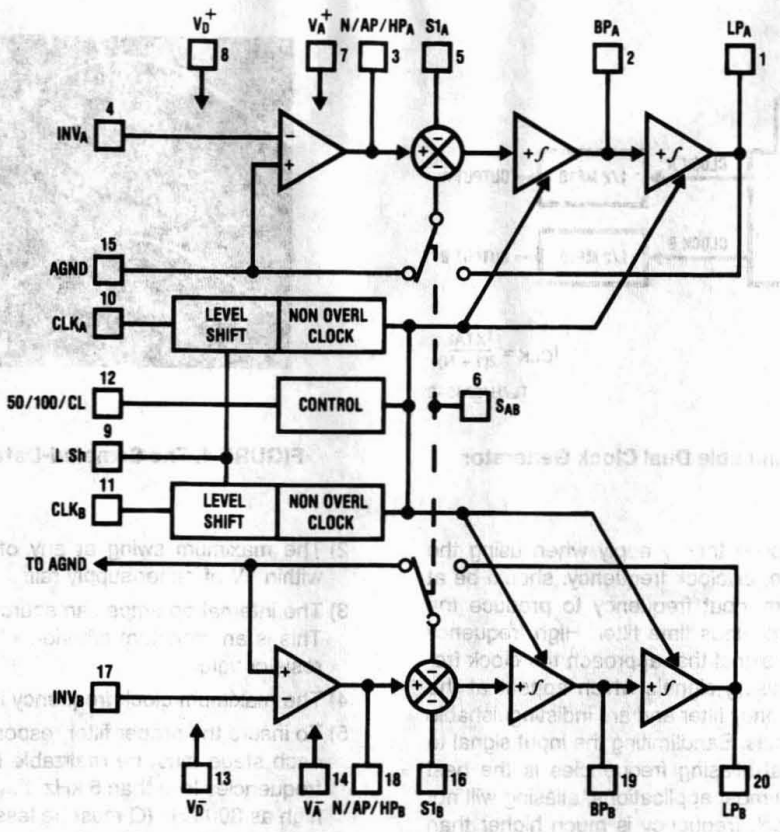


FIGURE 2. Block Diagram of the MF10

When tied to V_D^+ [the (+) supply], the switch connects the lowpass output, and when tied to V_D^- [the (−) supply], the connection to ground is made. In some applications one half of the MF10 may require that both of the (−) inputs to this summer be connected to ground, while the other side requires one to be connected to the lowpass output and the other to ground. For this, the $S_{A/B}$ control should be tied to the (−) supply and the connection to the lowpass output should be made externally to the $S1_A$ ($S1_B$) pin.

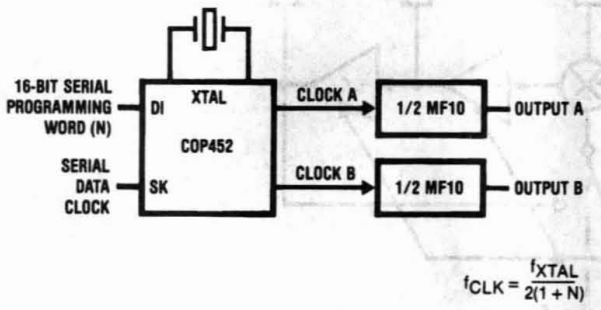
A clock with close to 50% duty cycle is required to control the resonant frequency of the filter. Either TTL or CMOS logic compatible clocks can be accommodated, whether the MF10 is powered from split supplies or a single supply, by simply grounding the level shift (L Sh) control pin.

The resonant frequency of each filter is directly controlled by its clock. A tri-level control pin sets the ratio of the clock frequency to the center frequency (the 50/100/CL pin) for both halves. When this pin is tied to V^+ the center frequency will be 1/50 of the clock frequency. When tied to mid-supply potential (i.e., ground, when biased from split supplies) provides 100 to 1 clock to center frequency operation. When this pin is tied to V^- a power saving supply current limiter shuts down operation and rolls back the supply current by 70%.

Filter center frequency accuracy and stability are only as good as the clock provided. Standard crystal oscillators, combined with digital counters, can provide very stable clocks for specific filter frequencies. A relatively new device from National's COPS family of microcontrollers and peripherals, the COP452 programmable frequency generator/counter, finds a unique use with the MF10, *Figure 3*. This low cost device can generate two independent 50% duty cycle clock frequencies. Each clock output is programmed via a 16-bit serial data word (N). This allows over 64,000 different clock frequencies for the MF10 from a single crystal.

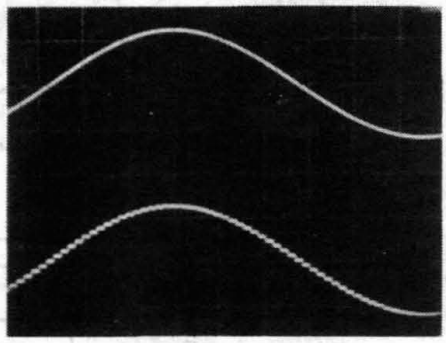
The MF10 is intended for use with center frequencies up to 20 kHz, and is guaranteed to operate with clocks up to 1 MHz. This means that for center frequencies greater than 10 kHz, the 50 to 1 clock control should be used. The effect of using 100 to 1 or 50 to 1 clock to center frequency ratio manifests itself in the number of "stair-steps" apparent in the output waveform. The MF10 closely approximates the time and frequency domain response of continuous filters (RC active filters, for example) but does so using sampling techniques. The clock to center frequency control determines the number of samples taken (1 per clock cycle) in one cycle of the center frequency. Therefore, as shown in the photo of *Figure 4*, 100 to 1 clocking provides a smoother looking output as it has twice as many samples per cycle. For most audio applications, the audible effects of these step edges and the clock frequency component in the output are negligible as they are beyond 20 kHz. To obtain a cleaner output waveform, a simple passive RC lowpass can be added to the output to serve as a smoothing filter without affecting the MF10 filtering action.

Several of the modes of operation (discussed in a later section) allow altering of the clock to center frequency ratio by an external resistor ratio. This can be used to obtain center frequencies of values other than 1/50 or 1/100 of the clock frequency. In multiple stage, staggered tuned filters, the center frequency of each stage can be set independently with resistors to allow the overall filter to be controlled by just one clock frequency.



TL/H/5035–3

FIGURE 3. A Programmable Dual Clock Generator



TL/H/5035–4

FIGURE 4. The Sampled-Data Output Waveform

All of the rules of sampling theory apply when using the MF10. The sampling rate, or clock frequency, should be at least twice the maximum input frequency to produce the best equivalent to a continuous time filter. High frequency components in the input signal that approach the clock frequency will generate aliasing signals which appear at the output of the lower frequency filter and are indistinguishable from valid passband signals. Bandlimiting the input signal to attenuate these potential aliasing frequencies is the best preventative measure. In most applications, aliasing will not be a problem as the clock frequency is much higher than the passband of interest. In the event that a much higher clock frequency is required, the modes of operation which utilize external resistor ratios to increase the clock to center frequency ratio can extend the clock frequency to greater than 100 times the center frequency. By using a higher clock frequency, the aliasing frequencies are correspondingly higher. The limiting factor, with regard to increasing the clock to center frequency ratio, has to do with increased DC offsets at the various outputs.

THE BASIC FILTER CONFIGURATIONS

There are six basic configurations (or modes of operation) for the 2nd order sections in the MF10 to realize a wide variety of filter responses. In all cases, no external capacitors are required. Design is a simple matter of establishing a few resistor ratios to set the desired passband gain and Q and generating a clock for the proper resonant frequency. Each 2nd order section can be treated in a modular fashion, with regard to individual center frequency, Q and gain, when cascading either the two sections within a package or several packages for very high order filters. This individuality of sections is important in implementing the various response characteristics such as Butterworth, Chebyshev, etc.

The following is a general summary of design hints common to all modes of operation.

1) The maximum supply voltage for the MF10 is ±7V or just + 14V for single supply operation. The minimum supply to properly bias the part is 8V.
2) The maximum swing at any of the outputs is typically within 1V of either supply rail.
3) The internal op amps can source 3 mA and sink 1.5 mA. This is an important criterion when selecting a minimum resistor value.
4) The maximum clock frequency is typically 1.5 MHz.
5) To insure the proper filter response, the $f_o \times Q$ product of each stage must be realizable by the MF10. For center frequencies less than 5 kHz, the $f_o \times Q$ product can be as high as 300 kHz (Q must be less than or equal to 150). A 3 kHz bandpass filter, for example, could have a Q as high as 100 with just one section. For center frequencies less than 20 kHz, the allowable $f_o \times Q$ product is limited to 200 kHz. A 10 kHz bandpass design using a single section should have a Q no larger than 20.
6) Center frequency matching from part to part for a given clock frequency is typically ±0.2%. Center frequency drift with temperature (excluding any clock frequency drift) is typically ±10 ppm/°C with 50:1 switching and ±100 ppm/°C for 100:1.
7) Q accuracy from part to part is typically ±2% with a temperature coefficient of ±500 ppm/°C.
8) The expressions for circuit dynamics given with each of the modes are important. They determine the voltage swing at each output as a function of the circuit Q. A high Q bandpass design can generate a significant peak in the response at the lowpass output at the center frequency.
9) Both sides of the MF10 are independent, except for supply voltages, analog ground, clock to center frequency ratio setting and internal switch setting for the three input summing stage.

In the following descriptions of the filter configurations, f_o is the filter center frequency, H_o is the passband gain and Q is the quality factor of the complex pole pair and is equal to f_o/BW where BW is the −3 dB bandwidth measured at the bandpass output.

MODE 1A: Non-Inverting Bandpass, Inverting Bandpass, Lowpass

This is a minimum external component configuration (only 2 resistors) useful for low Q lowpass and bandpass applications. The non-inverting bandpass output is necessary for minimum phase filter designs.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -1$$

$$H_{OBP_1} = -\frac{R3}{R2}$$

$$H_{OBP_2} = 1 \text{ (non-inverting)}$$

Circuit Dynamics

$H_{OBP_1} = -Q$ (this is the reason for the low Q recommendation)

$H_{OLP\,(peak)} = Q \times H_{OLP}$

MODE 1: Notch, Bandpass and Lowpass

With the addition of just one more external resistor, the output dynamics are improved over Mode 1A to allow bandpass designs with a much higher Q. The notch output features equal gain above and below the notch frequency.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$f_{notch} = f_o$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

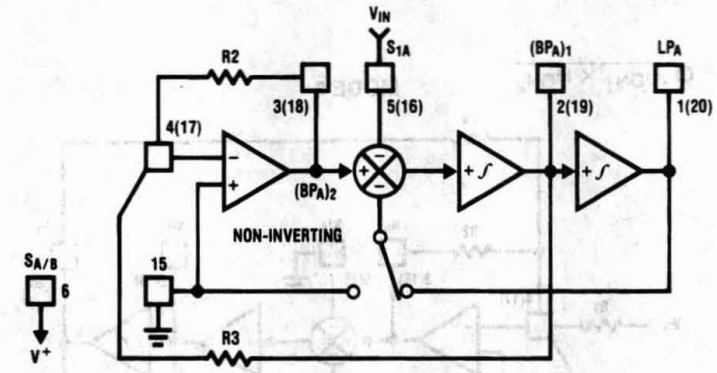
$$H_{ON} = -\frac{R2}{R1} \text{ as } f \rightarrow 0 \text{ and as } f \rightarrow \frac{f_{CLK}}{2}$$

Circuit Dynamics

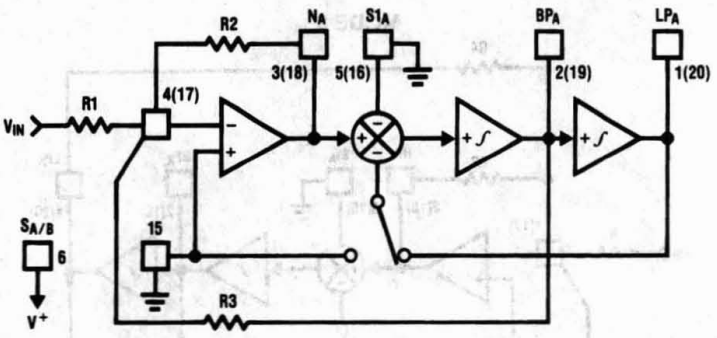
$H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$

$H_{OLP\,(peak)} = Q \times H_{OLP}$ (if the DC gain of the LP output is too high, a high Q value could cause clipping at the lowpass output resulting in gain non-linearity and distortion at the bandpass output).

MODE 1A



MODE 1



TL/H/5035–5

MODE 2: Notch (with $f_n \leq f_o$), Bandpass and Lowpass

This configuration allows tuning of the clock to center frequency ratio to values greater than 100 to 1 or 50 to 1. The notch output is useful for designing elliptic highpass filters because the frequency of the required complex zeros (f_{notch}) is less than the frequency of the complex poles (f_o).

Design Equations

$$f_o = \frac{f_{CLK}}{100}\sqrt{1+\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{1+\frac{R2}{R4}}$$

$$f_n = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{\sqrt{R_2/R_4+1}}{R_2/R_3}$$

$$H_{OLP} = \frac{-\frac{R2}{R1}}{1+\frac{R2}{R4}}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON_1}\ (\text{as } f \rightarrow 0) = \frac{-\frac{R2}{R1}}{1+\frac{R2}{R4}}$$

$$H_{ON_2}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

Circuit Dynamics

$$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON_2}} = Q\sqrt{H_{ON_1} \times H_{ON_2}}$$

MODE 3: Highpass, Bandpass and Lowpass

This configuration is the classical state variable filter (the circuit of *Figure 1*) implemented with only 4 external resistors. This is the most versatile mode of operation, since the clock to center frequency ratio can be externally tuned either above or below the 100 to 1 or 50 to 1 values. The circuit is suitable for multiple stage Chebyshev filters controlled by a single clock.

Design Equations

$$f_o = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

Circuit Dynamics

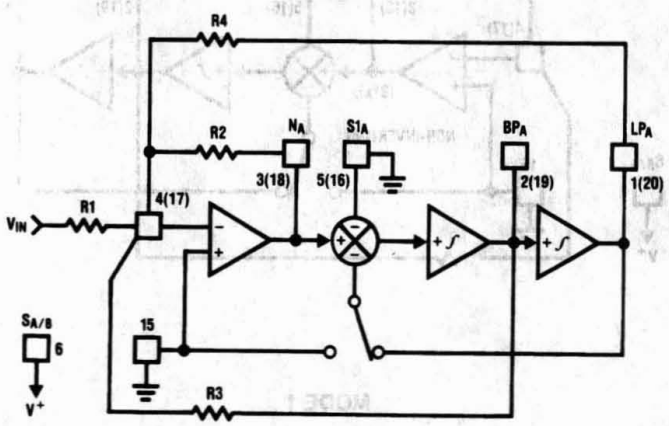
$$H_{OHP} = H_{OLP}\left(\frac{R2}{R4}\right)$$

$$H_{OLP\ (peak)} = Q \times H_{OLP}$$

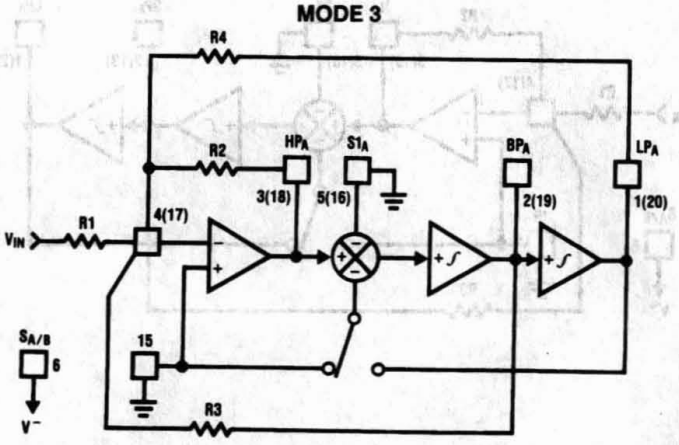
$$H_{OBP} = Q\sqrt{H_{OHP} \times H_{OLP}}$$

$$H_{OHP\ (peak)} = Q \times H_{OHP}$$

MODE 2



MODE 3



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MODE 3A: Highpass, Bandpass, Lowpass and Notch

A notch output is created from the circuit of Mode 3 by summing the highpass and lowpass outputs through an external op amp. The ratio of the summing resistors R_h and R_l adjusts the notch frequency independent of the center frequency. For elliptic filter designs, each stage combines a complex pole pair (at f_o) with a complex zero pair (at f_{notch}) and this configuration provides easy tuning of each of these frequencies for any response type. When cascading several stages of the MF10 the external op amp is needed only at the final output stage. The summing junction for the intermediate stages can be the inverting input of the MF10 internal op amp.

Design Equations

$$f_o = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$f_{notch} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON}\,(\text{at } f = f_o) = \left| Q\left(\frac{R_g}{R_l}H_{OLP} - \frac{R_g}{R_h}H_{OHP}\right)\right|$$

$$H_{ON_l}\,(\text{as } f \rightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{ON_h}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times H_{OHP}$$

MODE 4: Allpass, Bandpass and Lowpass

Utilizing the $S1_A$ ($S1_B$) terminal as a signal input, an allpass function can be obtained. An allpass can provide a linear phase change with frequency which results in a constant time delay. This configuration restricts the gain at the allpass output to be unity.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_z (frequency of complex zero pair) $= f_o$

$$Q = \frac{R3}{R2}$$

$$Q_z \text{ (Q of complex zero pair)} = \frac{R3}{R1}$$

$$H_{OAP} = -\frac{R2}{R1} = -1$$

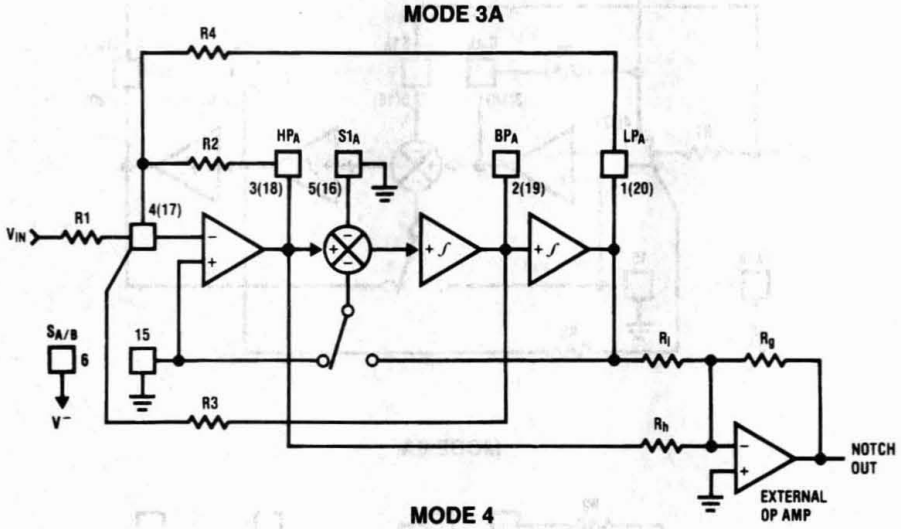
$$H_{OLP} = -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = -\left(1 + \frac{R2}{R1}\right)\frac{R3}{R2} = -2\frac{R3}{R2}$$

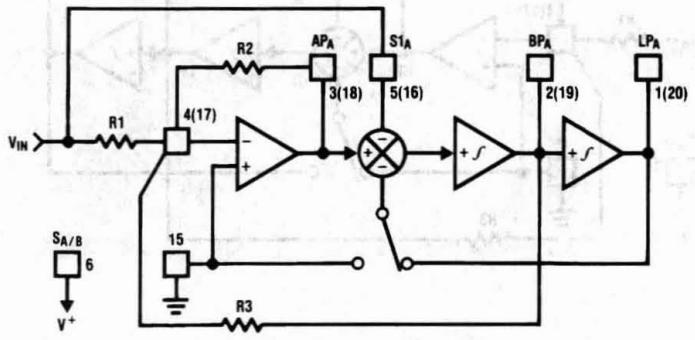
Circuit Dynamics

$$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)Q$$

MODE 3A



MODE 4



TL/H/5035–7

MODE 5: Complex Zeros (C.z), Bandpass and Lowpass

This mode features an improved allpass design over that of Mode 4, in that it maintains a more constant amplitude with frequency at the complex zeros (C.z) output. The frequencies of the pole pair and zero pair are resistor tunable.

Design Equations

$$f_o = \frac{f_{CLK}}{100}\sqrt{1+\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{1+\frac{R2}{R4}}$$

$$f_z = \frac{f_{CLK}}{100}\sqrt{1-\frac{R1}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{1-\frac{R1}{R4}}$$

$$Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$$

$$Q_z = \frac{R3}{R1}\sqrt{1-\frac{R1}{R4}}$$

$$H_{O(C.z)} \text{ as } f \longrightarrow 0 = \frac{R2(R4-R1)}{R1(R2+R4)}$$

$$H_{O(C.z)} \text{ as } f \longrightarrow \frac{f_{CLK}}{2} = \frac{R2}{R1}$$

$$H_{OBP} = \frac{R3}{R2}\left(1+\frac{R2}{R1}\right)$$

$$H_{OLP} = \frac{R4}{R1}\left(\frac{R2+R1}{R2+R4}\right)$$

MODE 6A: Single Pole, Highpass and Lowpass

By using only one of the internal integrators, this mode is useful for creating odd-ordered cascaded filter responses by providing a real pole that is clock tunable to track the resonant frequency of other 2nd order MF10 sections. The corner frequency is resistor tunable.

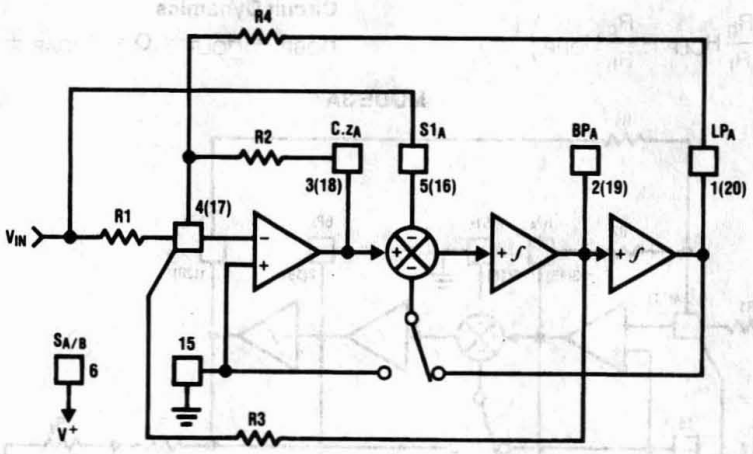
Design Equations

$$f_c \text{ (cut-off frequency)} = \frac{f_{CLK}}{100}\left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50}\left(\frac{R2}{R3}\right)$$

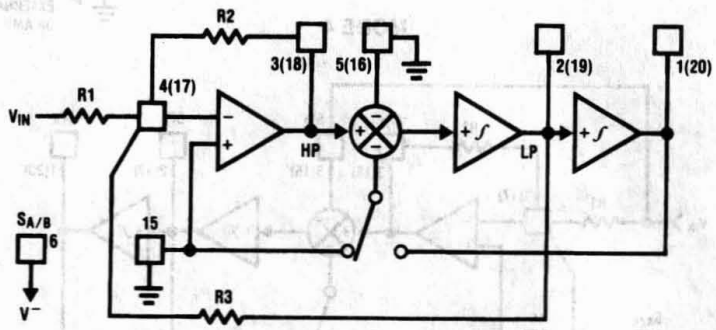
$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 5



MODE 6A



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MODE 6B: Single Pole Lowpass (Inverting and Non-Inverting)

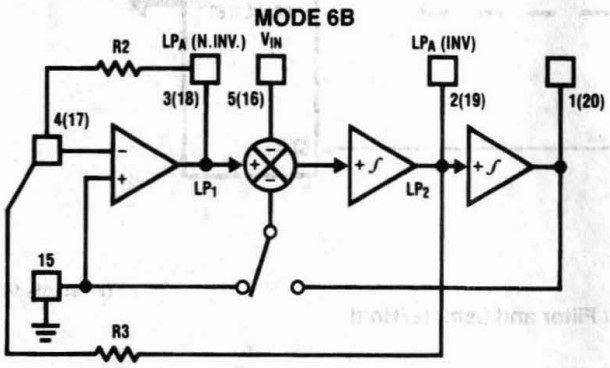
This mode utilizes only one of the integrators for a single pole lowpass, and the input op amp as an inverting amplifier, to provide non-inverting lowpass output. Again, this mode is useful for designing odd-ordered lowpass filters.

Design Equations

$$f_c \text{ (cut-off frequency)} = \frac{f_{CLK}}{100}\left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50}\left(\frac{R2}{R3}\right)$$

$$H_{OLP} \text{ (inverting output)} = -\frac{R3}{R2}$$

$$H_{OLP} \text{ (non-inverting output)} = +1$$



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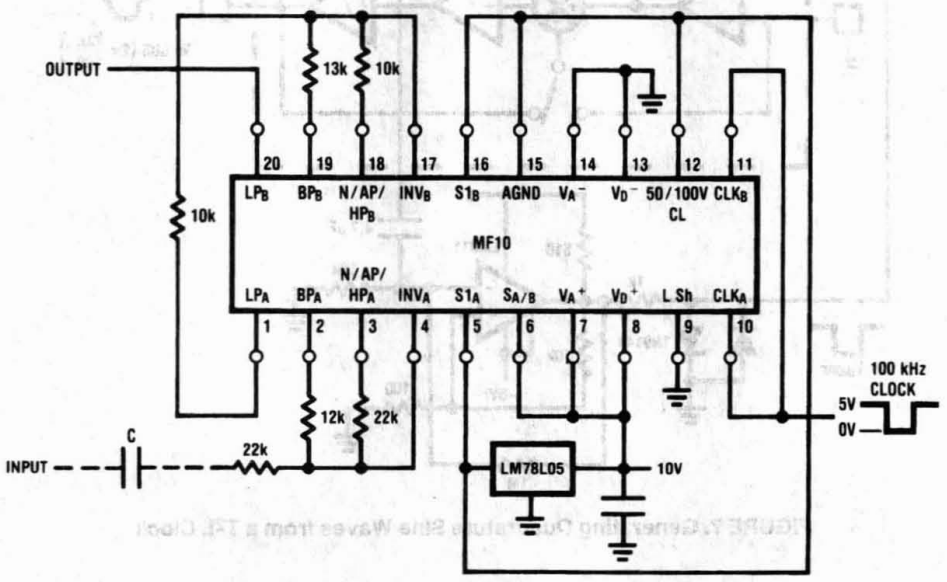
SOME SPECIFIC APPLICATION EXAMPLES

For single-supply operation, it is important for several terminals to be biased to half supply. A single-supply design for a 4th order 1 kHz Butterworth lowpass (24 dB/octave or 80 dB/decade rolloff) is shown using Mode 1 in *Figure 5*. Note that the analog ground terminal (pin 15), the summer inputs $S1_A$ and $S1_B$ (pins 5 and 16) and the clock switching control pin (pin 12) are all biased to $V_{CC}/2$. For symmetrical split supply operation these pins would be grounded. An input coupling capacitor is optional, as it is needed only if the input signal is not also biased to $V_{CC}/2$. For a two-stage Butterworth response, both stages have the same corner frequency, hence the common clock for both sides. The resistor values shown are the nearest 5% tolerance values used to set the overall gain of the filter to unity and to set the required Q of the first stage (side A) to 0.504 and the second stage (side B) Q to 1.306 for a flat passband response.

A unique advantage of the switched capacitor design of the MF10 is illustrated in *Figure 6*. Here the MF10 serves double duty in a data acquisition system as an input filter for simple bandlimiting or anti-aliasing and, as a sample and hold to allow larger amplitude, higher frequency input signals. By gating OFF the applied clock, the switched capacitor integrators will hold the last sampled voltage value. The droop rate of the output voltage during the hold time is approximately 0.1 mV per ms.

A useful non-filtering application of the MF10 is shown in *Figure 7*. In this circuit, the MF10, together with an LM311 comparator, are used as a resonator to generate stable amplitude sine and cosine outputs without using AGC circuitry. The MF10 operates as a Q of 10 bandpass filter which will ring at its resonant frequency in response to a step input change. This ringing signal is fed to the LM311 which creates a square wave input signal to the bandpass to regenerate the oscillation. The bandpass output is the filtered fundamental frequency of a 50% duty cycle square wave. A 90° phase shifted signal of the same amplitude is available at the lowpass output through the second integrator in the MF10. The frequency of oscillation is set by the center frequency of the filter as controlled by the clock and the 50:1/100: 1 control pin. The output amplitude is set by the peak to peak swing of the square wave input, which in this circuit is defined by the back to back diode clamps at the LM311 output.



TL/H/5035–10

FIGURE 5. Only 6 resistors required for this 4th order, 1 kHz Butterworth lowpass filter. This example also illustrates single-supply biasing.

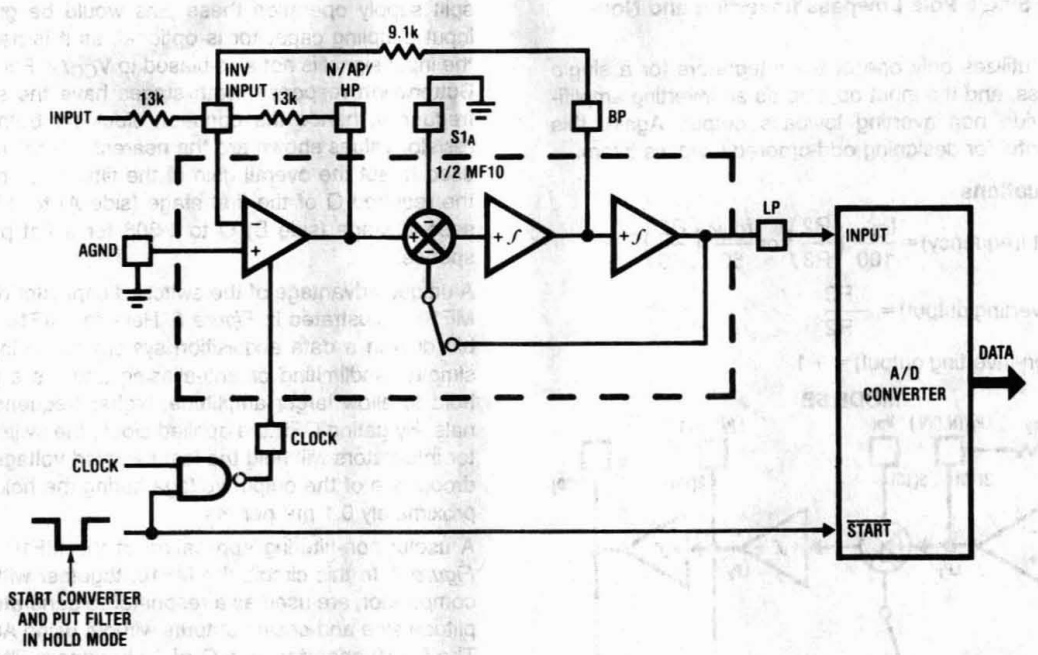


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FIGURE 6. An MF10 as an Input Filter and Sample/Hold

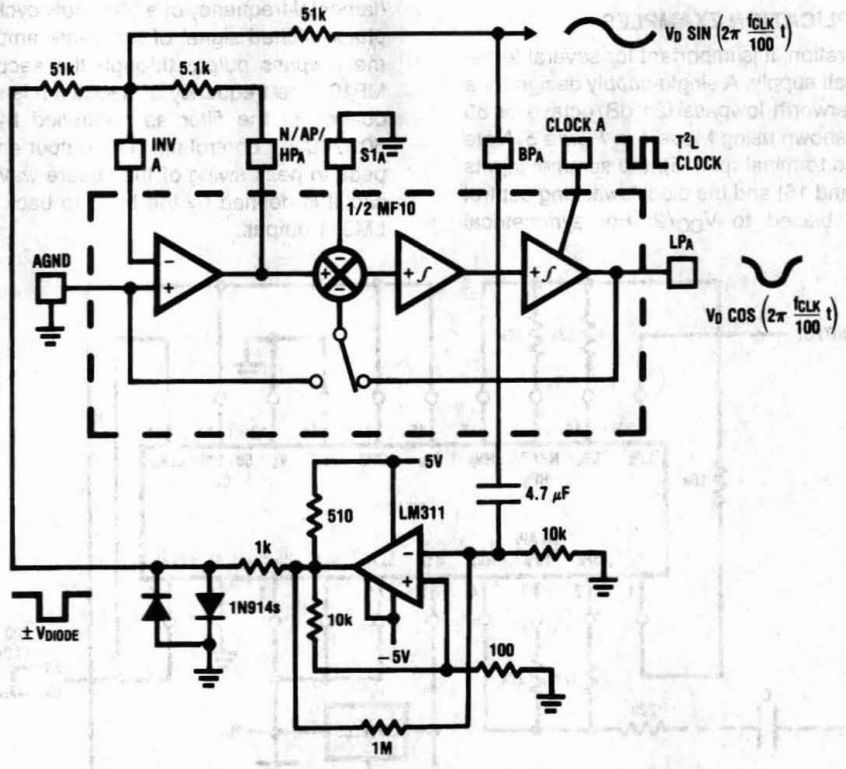

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FIGURE 7. Generating Quadrature Sine Waves from a T²L Clock

Finally, as a graphic illustration of the simplicity of filter implementation using the MF10, *Figure 8* is a complete 300 baud, full-duplex modem filter. The filter is an 8th order, 1 dB ripple Chebyshev bandpass which functions as both an 1170 Hz originate filter and a 2125 Hz answer filter. Control of answer or originate operation is set by the logic level at the 50/100/CL input so that only one clock frequency is required. The overall filter gain is 22 dB.

Construction of this filter on a printed circuit board would obviously be more compact than an RC active filter approach and much more cost effective for the level of precision required. An even more attractive implementation from a space savings point of view would be a hybrid circuit approach. A film resistor array connecting to two MF10 die could produce the entire filter in one package requiring only 7 external connections for input, output, supplies, etc.

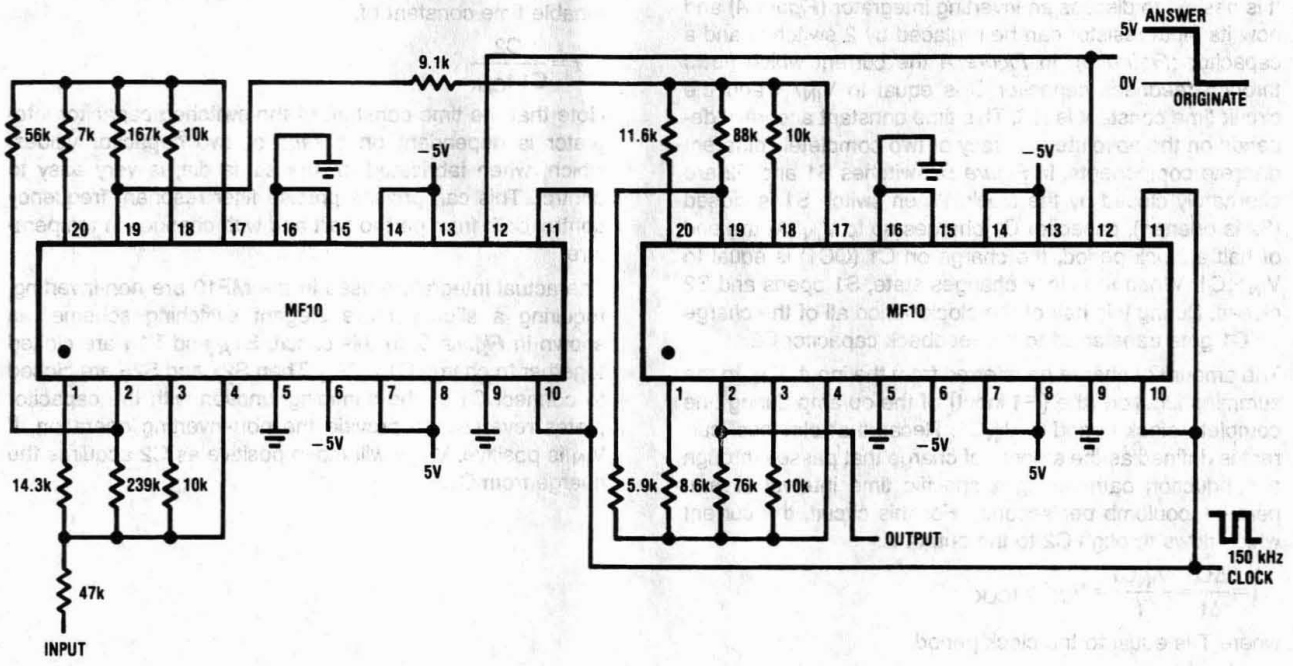

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FIGURE 8. A Complete Full-Duplex 300 Baud Modem Filter

THE SWITCHED CAPACITOR INTEGRATOR—HOW IT WORKS

The most important feature of the MF10 is that it requires no external capacitors, yet can implement filters over a wide range of frequencies. A clock is used to control the time constant of two non-inverting integrators. To feel comfortable with the operation of the MF10, it is important to understand how this control is accomplished.

It is easiest to discuss an inverting integrator (*Figure A*) and how its input resistor can be replaced by 2 switches and a capacitor (*Figure B*). In *Figure A* the current which flows through feedback capacitor C is equal to V_{IN}/R and the circuit time constant is RC. This time constant accuracy depends on the absolute accuracy of two completely different discrete components. In *Figure B*, switches S1 and S2 are alternately closed by the clock. When switch S1 is closed (S2 is opened), capacitor C1 charges up to V_{IN}. At the end of half a clock period, the charge on C1 (QC1) is equal to $V_{IN} \times C1$. When the clock changes state, S1 opens and S2 closes. During this half of the clock period all of the charge on C1 gets transferred to the feedback capacitor C2.

The amount of charge transferred from the input, V_{IN}, to the summing junction [the (−) input] of the op amp during one complete clock period is $V_{IN}C1$. Recall that electrical current is defined as the amount of charge that passes through a conduction path during a specific time interval (1 ampere = 1 coulomb per second). For this circuit, the current which flows through C2 to the output is:

$$I = \frac{\Delta Q}{\Delta t} = \frac{V_{IN}C1}{T} = V_{IN}C1\, f_{CLK}$$

where T is equal to the clock period.

The effective resistance from V_{IN} to the (−) input is therefore:

$$R = \frac{V_{IN}}{1} = \frac{1}{C1\, f_{CLK}}$$

This means that S1, S2 and C1, when clocked in *Figure B*, act the same as the resistor in *Figure A* to yield a clock tunable time constant of:

$$\tau = \frac{C2}{C1\, f_{CLK}}$$

Note that the time constant of the switched capacitor integrator is dependent on a *ratio* of two capacitor values, which, when fabricated on the same die, is very easy to control. This can provide precise filter resonant frequency control both from part to part and with changes in temperature.

The actual integrators used in the MF10 are non-inverting, requiring a slightly more elegant switching scheme, as shown in *Figure C*. In this circuit, $S1_A$ and $S1_B$ are closed together to charge C1 to V_{IN}. Then $S2_A$ and $S2_B$ are closed to connect C1 to the summing junction with the capacitor plates reversed, to provide the non-inverting operation. If V_{IN} is positive, V_{OUT} will move positive as C2 acquires the charge from C1.

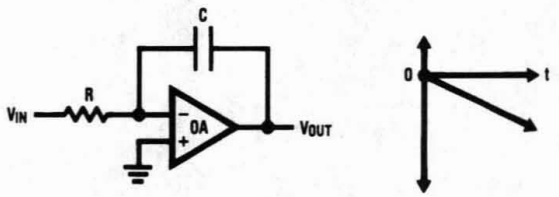

FIGURE A

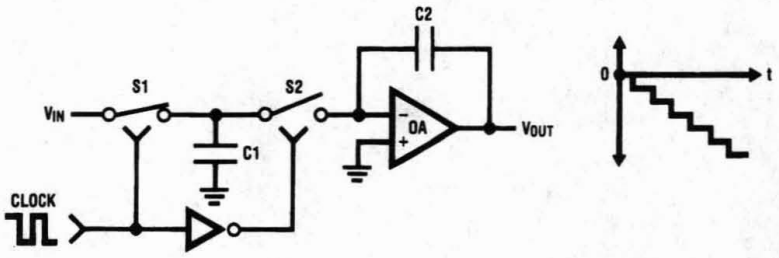

FIGURE B

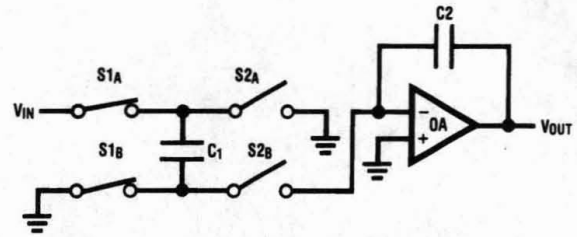

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FIGURE C. The Non-Inverting Integrator Used in the MF10

Theory and Applications of Logarithmic Amplifiers

National Semiconductor
Application Note 311

A number of instrumentation applications can benefit from the use of logarithmic or exponential signal processing techniques. The design and use of logarithmic/exponential circuits are often associated with involved temperature compensation requirements and difficult to stabilize feedback loops. For these considerations and others, designers tend to avoid these circuits. Hybrid and modular logarithmic/exponential devices are available commercially, but are quite expensive and earn very high profits for their manufacturers.

The theory and construction of these circuits are actually readily understood. *Figure 1* shows an amplifier which provides a logarithmic output for a linear input current or voltage. For input currents, the circuit will maintain 1% logarithmic conformity over almost 6 decades of operation. This circuit is based, as are most logarithmic circuits, on the inherent logarithmic relationship between collector current and V_{BE} in bipolar transistors. Q1A functions as the logging transistor in this circuit and is enclosed within A1A's feedback loop, which includes the 15.7 kΩ-1 kΩ divider. The circuit's input will force A1A's output to achieve whatever value is required to maintain its summing junction at zero potential. Because Q1A's response is dictated by the logarithmic relationship between collector current and V_{BE}, the output of A1A will be the logarithm of the circuit input. A1B and Q1B provide compensation for Q1A's V_{BE} temperature dependence. A1B servos Q1B's collector current to equal the 10 μA current established by the LM329 reference diode and the 700 kΩ resistor. Since Q1B's collector current cannot vary, its V_{BE} is also fixed. Under these conditions only Q1A's V_{BE} will be affected by the circuit's input. The circuit's output is a function of:

$$E_{OUT} = \frac{15.7k + 1k}{1k}(V_{BE}Q1B - V_{BE}Q1A)$$

For Q1A and Q1B operating at different collector currents, the V_{BE} difference is:

$$\Delta V_{BE} = \frac{KT}{q}\log_e \frac{I_{CQ1A}}{I_{CQ1B}}$$

where K = Boltzmon's constant

T = temperature °K

q = charge of an electron.

If both equations are combined, the circuit output for a voltage input is:

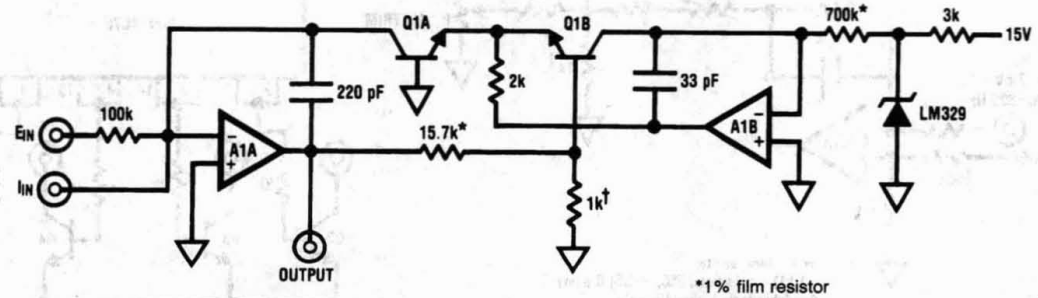
$$E_{OUT} = \frac{-KT}{q}\frac{15.7k + 1k}{1k}\log_e \frac{E_{IN} \bullet 700k}{6.9V \bullet 100k}$$

where 6.9V = V_Z of LM329

100k = input resistor

$E_{IN} \geq 0$.

This confirms that the circuit output voltage is logarithmically related to the circuit's input. Without some form of compensation, the scale factor will change with temperature. The simplest way to avoid this is to have the 1 kΩ value vary with temperature. For the device shown, compensation is within 1% over −25°C to +100°C. The circuit's gain is set by the 15.7 kΩ-1 kΩ divider to a factor of 1V/decade.



*1% film resistor

†1 kΩ (±1%) at 25°C, +3500 ppm/°C. Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

A1A, A1B = LF412 dual

Q1A, Q1B = LM394 dual

TL/H/5045–1

FIGURE 1

This circuit may be easily turned around to generate exponentials. In *Figure 2,* Q1A is driven from the input via the 15.7 kΩ divider. Q1B's collector current varies exponentially with its V_{BE}, and A1B provides a voltage output representation of this action.

These circuits are easy to construct and use if a few considerations are kept in mind. Because of the V_{BE} and scale factor temperature dependences, it is important that Q1A, Q1B and the 1 kΩ resistor be kept at the same temperature. Since Q1 is a dual monolithic device, both halves will track. The resistor should be mounted as closely as possible to Q1, and these components should be kept away from air currents or drafts. The KT/q factor for which the resistor compensates varies at about 0.3%/°C, so a few degrees difference between Q1 and the resistor will introduce significant error.

Once the theory and construction techniques are understood, the circuits can be applied. *Figure 3* shows a way to achieve very precise control of a rotary pump, used to feed a biochemical fermentation process. In this example, the exponentiator, composed of Q1 and A1A, is driven from

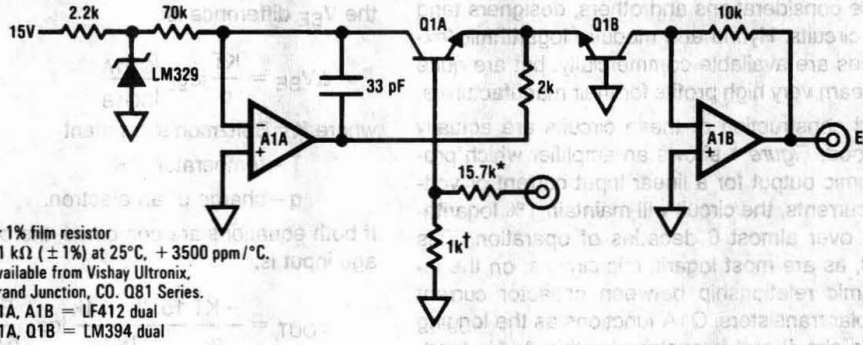


FIGURE 2

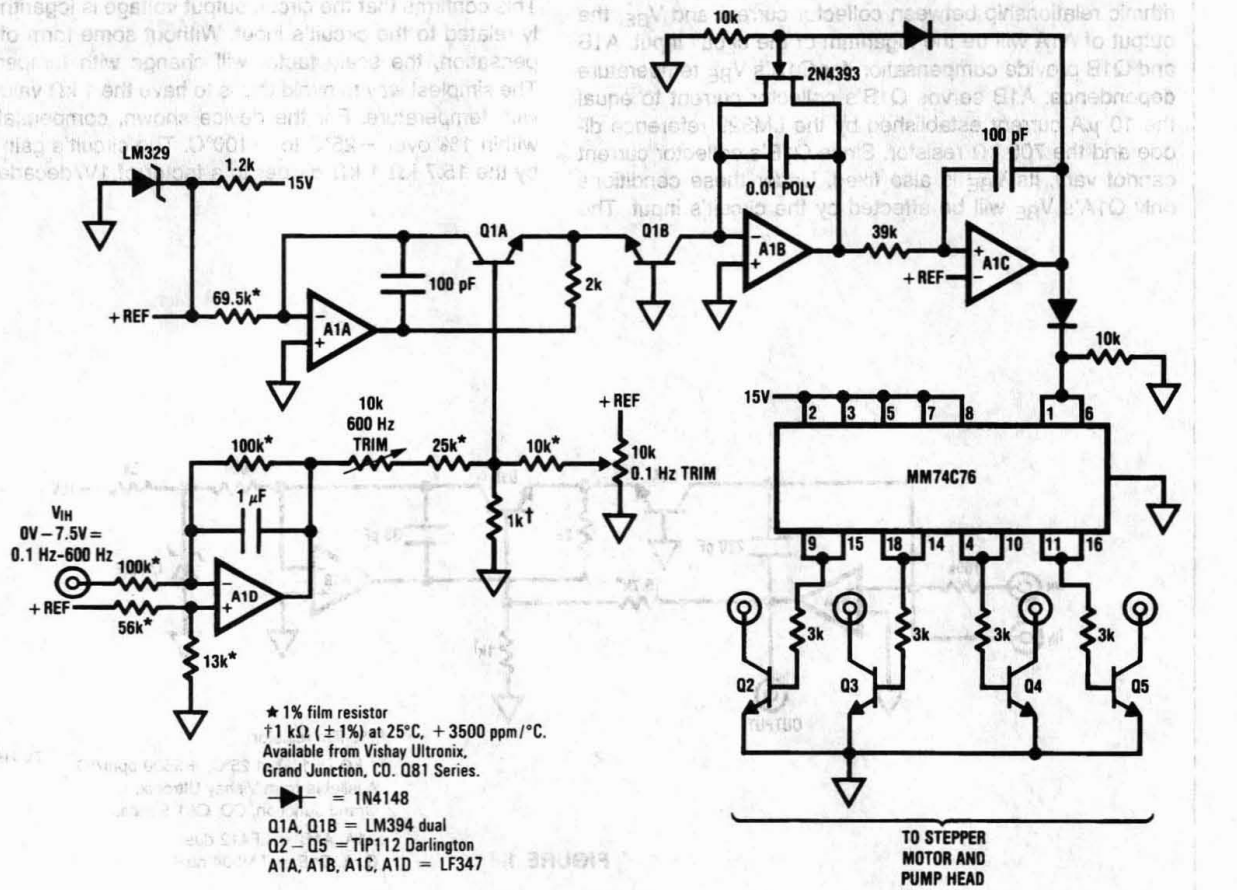


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FIGURE 3

input amplifier A1D. Q1B's collector current, instead of biasing a voltage output amplifier as in *Figure 2,* pulls current from the A1B integrator which ramps up (trace A, *Figure 4)* until it is reset by level triggered A1C (A1C output is trace B, *Figure 4).* The 100 pF capacitor provides AC positive feedback to A3C's "+" input (trace C, *Figure 4).* The magnitude of the current that Q1B's collector pulls from A1B's summing junction will set the frequency of operation of this oscillator. Note that the operation of the exponentiator is similar to the basic circuit in *Figure 3* because A1B's summing junction is always at virtual ground. A1C's output drives the MM74C76 flip-flop to bias the output transistors with 4-phase drive for a stepper motor which runs the pump head. In practice, the exponentiator allows very fine and predictable control for very slow pump rates (e.g., 0.1 rpm-10 rpm of the stepper motor), aiding tight feedback control of the fermentation process. When high pump rates are required, such as during process start-up or when a wide feedback control error exists, the exponentiator can be voltage directed to the top of its range. To calibrate the circuit, ground V_{IN} and adjust the 0.1 Hz trim until oscillation just ceases. Next, apply 7.5V at V_{IN} and adjust the 600 Hz trim for 600 Hz output frequency. *Figure 5* shows a circuit similar to *Figure 3,* except that a more accurate V-F converter is used. This circuit is intended for laboratory and audio studio applications requiring an oscillator whose frequency changes exponentially with an applied input sweep voltage. Applications include swept distortion measurements (where this circuit's output is used to drive a sine coded ROM-DAC combination or analog shaper) and music synthesizers. The V-F converter employed allows better than 0.15% total conformity over a range of 10 Hz-30 kHz. The voltage reference used to drive A1A's input resistor is derived from the LM331A's internal reference and is scaled by A1B, which also biases the zero trim setting. The DM74C74 provides a square wave output for applications requiring a waveform with substantial fundamental frequency content. The 0.15% conformity performance achieved by this circuit will meet almost any synthesizer or swept distortion measurement and the scale factor may be easily varied. To trim, apply OV to the input and adjust zero until oscillation (typically 2 Hz-3 Hz) just starts. Next, apply −8V and adjust the 5k unit for an output frequency of 30 kHz. For the values given, the K factor of the exponentiator will yield a precise doubling in frequency for each volt of input (e.g., 1V in per octave out).

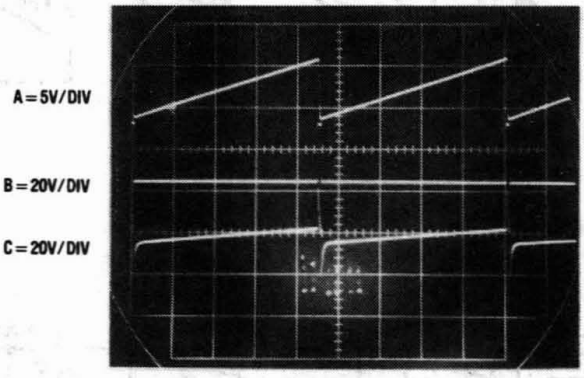

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FIGURE 4

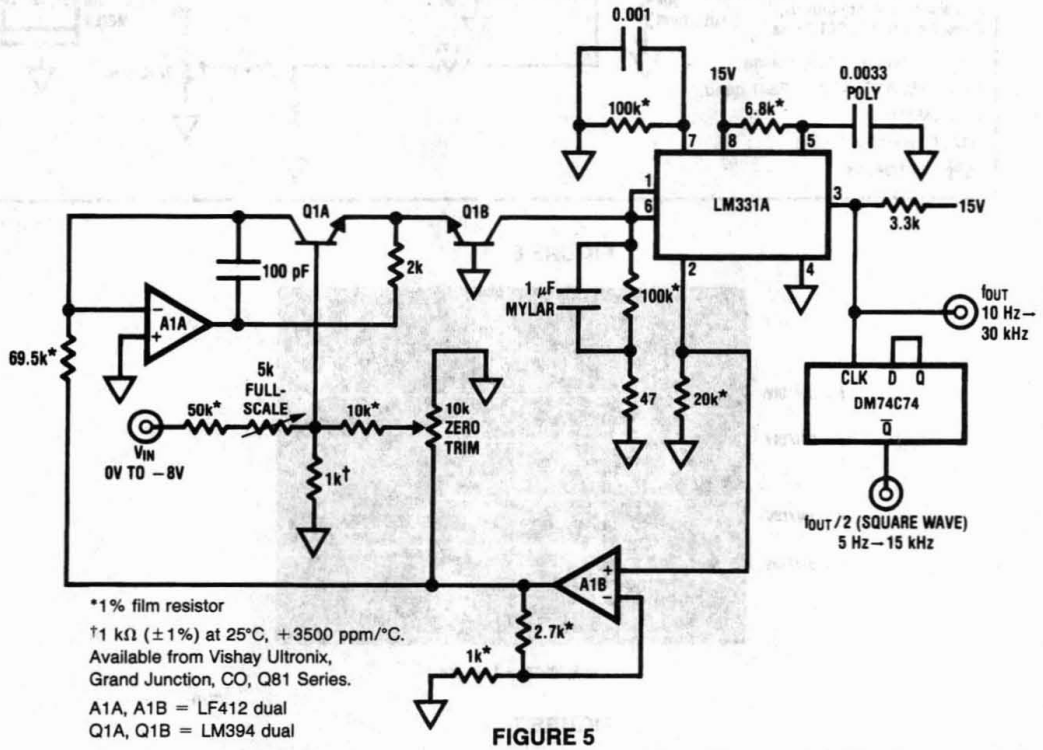

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FIGURE 5

Figure 6 shows a way to use the exponentiator circuit in a non-invasive, high reliability gas gauge which was designed for use in irrigation pump arrangements in remote locations. The application calls for a highly reliable gas gauge to be retrofitted to large fuel tanks which supply pump motors. It is desirable to run the gas tanks down as closely to empty as possible to eliminate condensation build-up without running out of fuel. This acoustically-based scheme operates by bouncing an ultrasonic pulse off the liquid level surface and using the elapsed time to determine the fuel remaining. This time is converted to a voltage, which is exponentiated to provide a readout with high resolution for nearly empty tanks. The 60 Hz derived clock pulse (trace A, *Figure 7)* drives the transistor pair to bias the ultrasonic transducer with a 100V pulse. Concurrently, the DM74C74 flip-flop is set high (trace C, *Figure 7)* and the DM74C221 one-shot (trace D, *Figure 7)* is used to disable the output of the receiver amplifier. The acoustic pulse bounces off the gasoline's surface and returns to the transducer. By this time, the disable pulse has gone low and the A1A, A1B, A1C and C1 receiver responds (trace B, *Figure 7)* to the transducer's output. C1's output resets the flip-flop low via the DM74C04 inverter. The width of the 60 Hz flip-flop output pulse represents the transit time and the fuel remaining. This width is

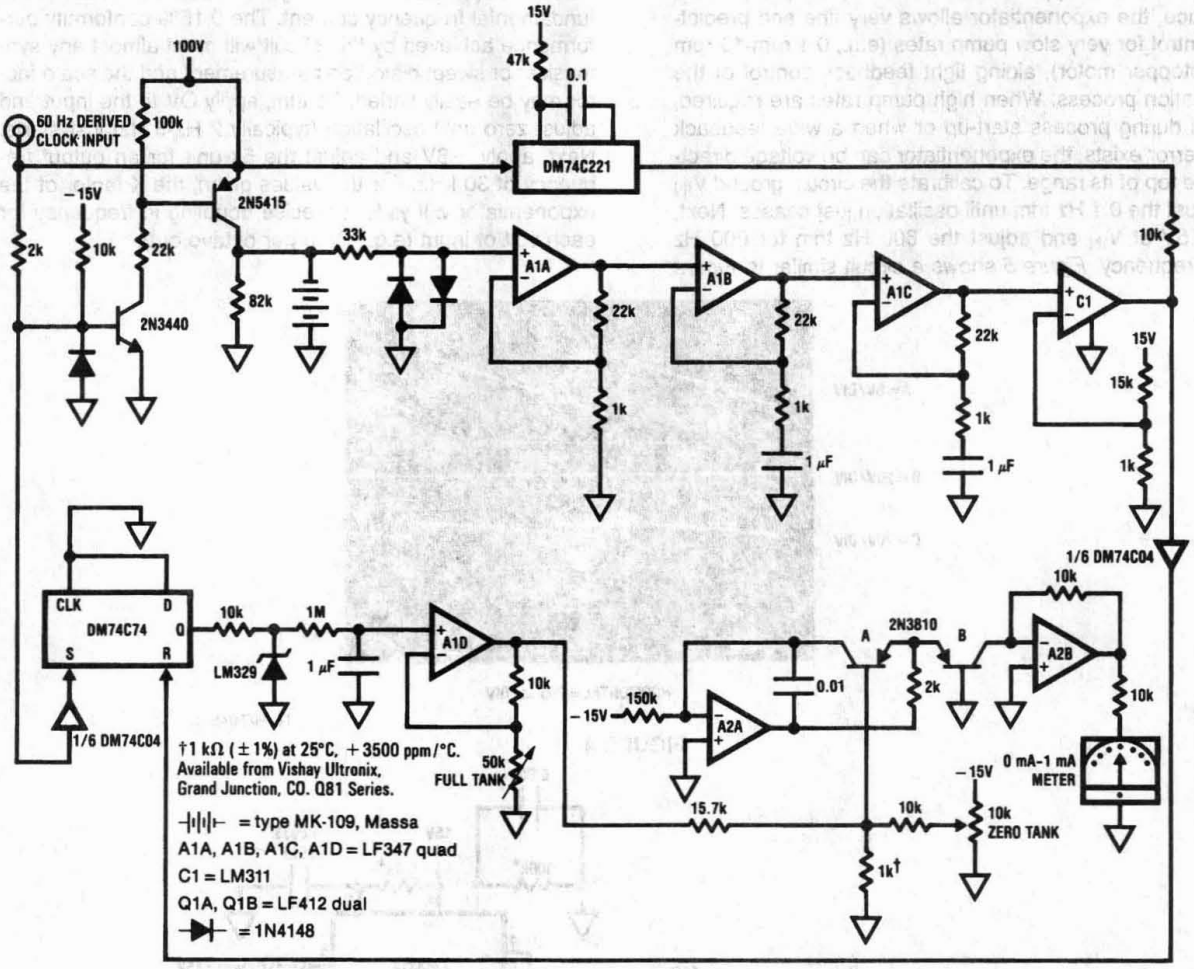

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FIGURE 6

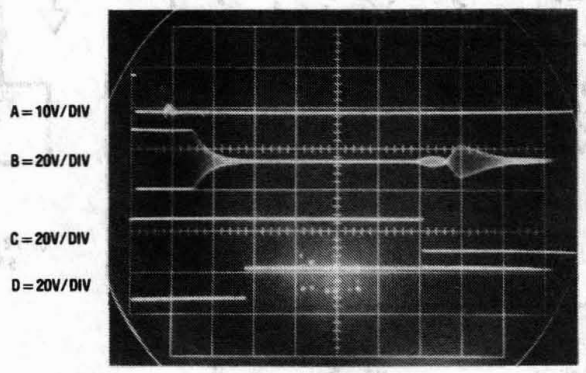

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FIGURE 7

voltage clamped and integrated at A1D, whose output drives the exponentiator. The 1V/decade scale factor of the exponentiator means that the last 20% of the meter scale corresponds to a tank with only 2% fuel remaining. The first 10% of the meter indicates 80% of the tank's capacity.

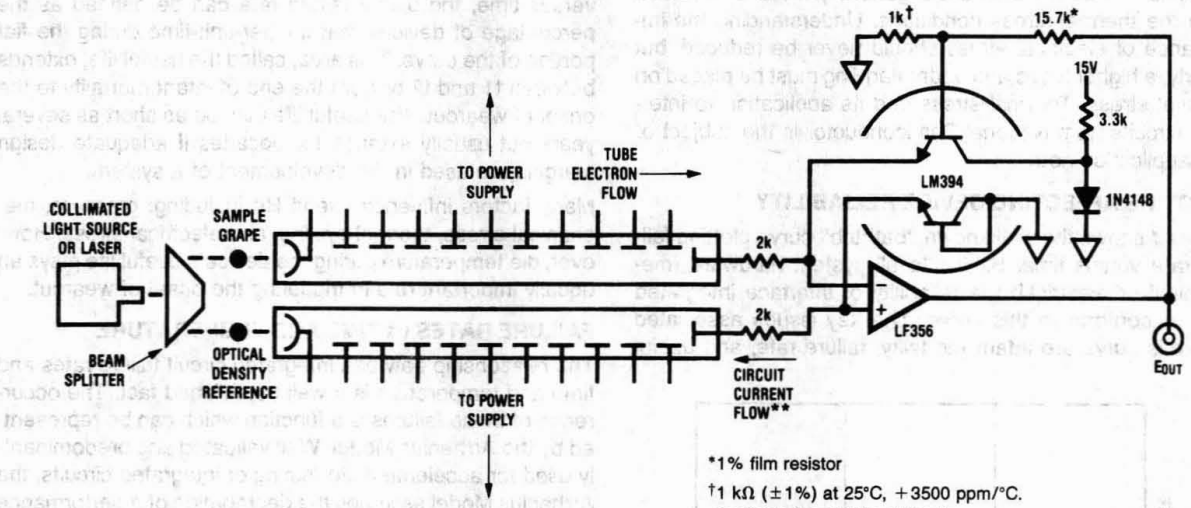
The last application determines density by using photometry. In this arrangement, a light source is optically split *(Figure 8)* and the resultant two beams drive light through a sample and an optical density reference. In this case, the optical sample is a grape, and the photometric set-up is used to correlate the optical density of the grape with its ripeness. Two photomultiplier tubes detect the light passed by the sample and the reference. The ratio of the photomultiplier outputs, which may vary over a wide range, is dependent upon the optical density difference of the sample and the reference. The tubes' output feed a log *ratio* amplifier. This configuration dispenses with the fixed current reference normally employed, and substitutes the output of the reference channel photomultiplier. In this fashion, the log amplifier's output represents the ratio between the densities of the sample and reference channels over a wide dynamic range. Variations in the light source intensity have no effect. Strictly speaking, the LF356 inputs are not at virtual ground, and an imperfect current-to-voltage conversion should result. In fact, the output impedance of the photomultipliers is so high that errors are minimal. The most significant log conformance error source in this simple log circuit is the fact that the transistor's collectors are at slightly different potentials. For the application shown, this uncertainty is not significant.

REFERENCES

Non-Linear Circuits Handbook; Analog Devices, Inc.

Logarithmic Converters, Application Note AN-30;

R. C. Dobkin; National Semiconductor Corporation.



*1% film resistor

†1 kΩ (±1%) at 25°C, +3500 ppm/°C. Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

**≈ 10 μA nominal but may vary from 10^{-4}A to 10^{-9}A

TL/H/5045–7

FIGURE 8

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor
Application Note 336
Charles Carinalli
Josip Huljev

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

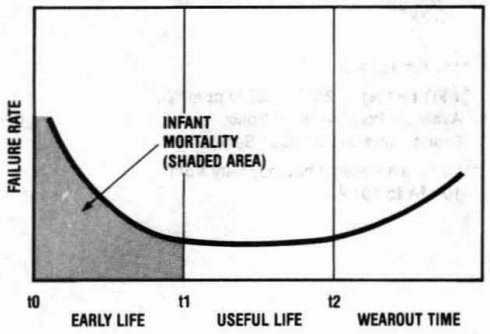


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

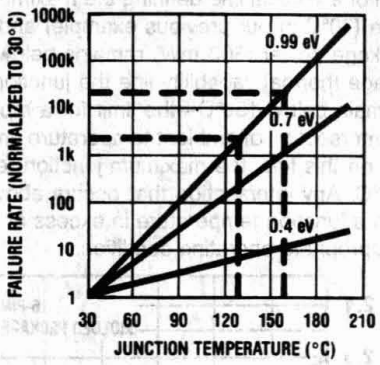

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D(\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

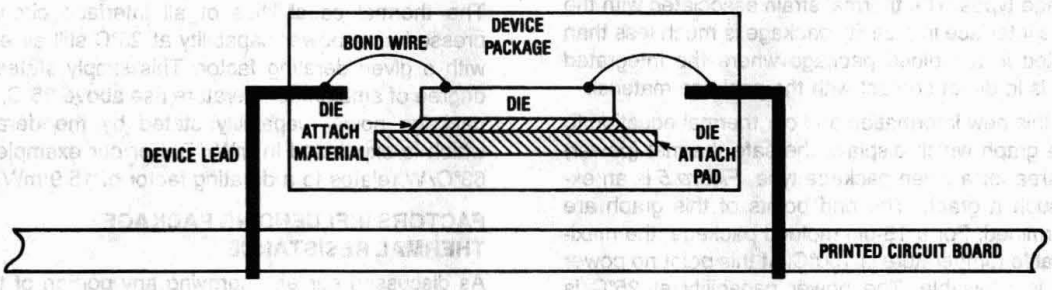

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

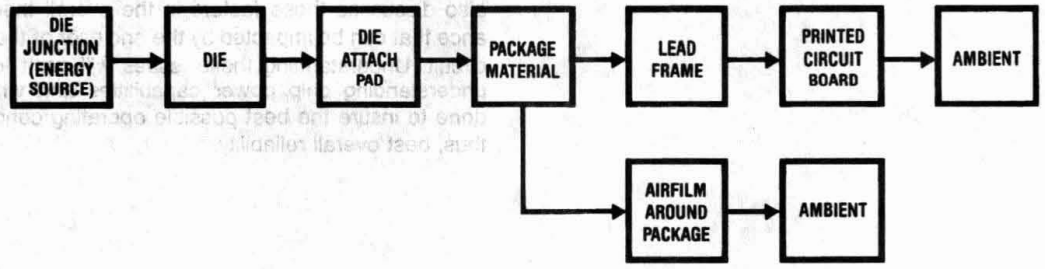

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

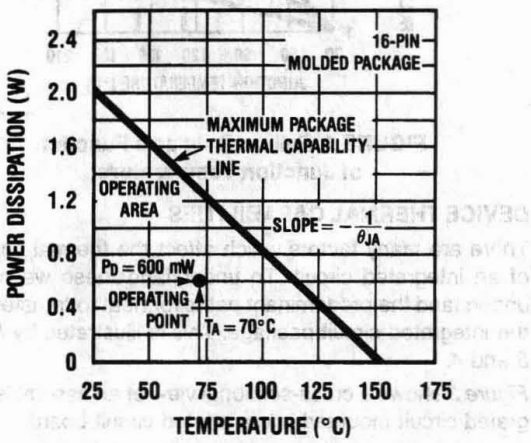

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

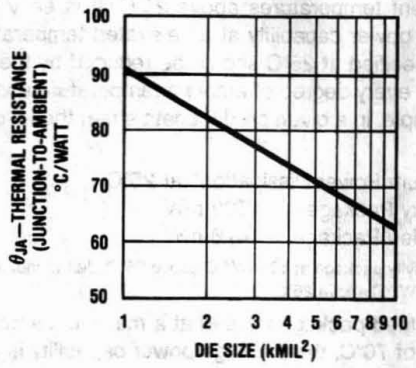

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 43 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

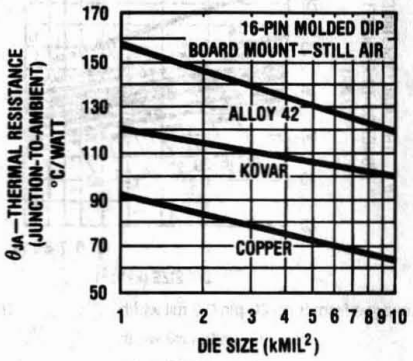

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

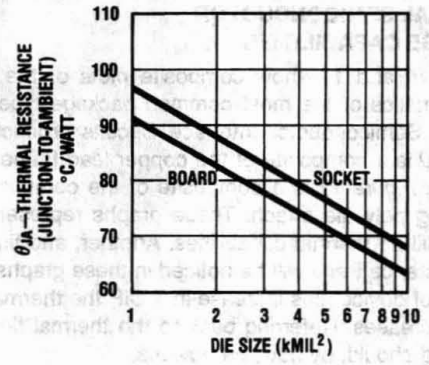

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

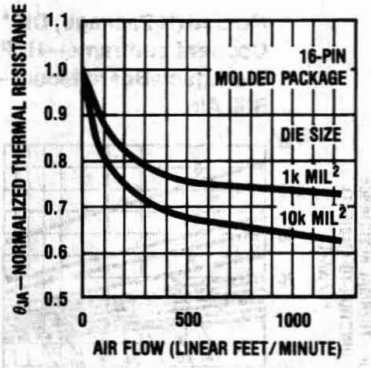

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

Maximum Power Dissipation* at 25°C

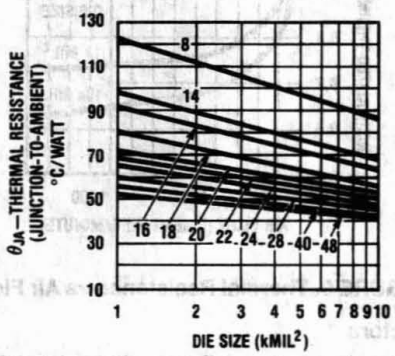
Cavity Package	1509 mW
Molded Package	1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70°C = 1476 \text{ mW} - (11.8 \text{ mW/°C}) \times (70°C - 25°C)$$
$$= 945 \text{ mW}$$

Molded (N Package) DIP*
Copper Leadframe—HTP
Die Attach Board Mount—
Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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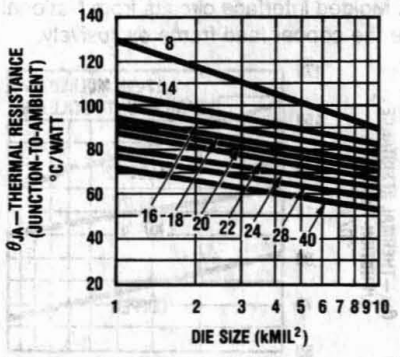
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP*
Poly Die Attach Board
Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

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FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

LH1605 Switching Regulator

National Semiconductor
Application Note 343

INTRODUCTION

The LH1605 is the first in a family of high-efficiency switching regulators designed to simplify power conversion while minimizing power losses. It can deliver 5 amps continuous output current and operate over a wide range of input and output voltages. In classic step-down voltage regulator applications it requires only 4 external parts: a resistor, 2 capacitors and an inductor. The device is housed in a standard 8-pin TO-3 power package containing a temperature compensated voltage reference, an error amplifier, a pulse-width modulator with programmable operating frequency and a high current output switch and steering diode. Typical performance of the LH1605 is summarized in Table I.

This discussion details LH1605 operating theory and analyzes device power considerations. It also explains DC/DC conversion using the LH1605 and presents design criteria and examples. A section suggesting other typical LH1605 applications is included, as in an appendix listing suppliers of capacitors, magnetic components and heat sinks suitable for use with the LH1605.

TABLE I. LH1605 Typical Performance Characteristics

	Parameter	Value
I_O	Continuous Output Current	5A
V_{IN}	Input Voltage	10V–35V
V_O	Output Voltage	3V–30V
V_S	Switch Saturation Voltage, I_{OUT} = 4A	1.4V
ΔV_R	Line Regulation of Reference Voltage	20 mV
η	Efficiency	70%
θ_{JC}	Thermal Resistance	5°C/W

THEORY OF OPERATION

Unlike linear regulators, which rely on a linear series element to control the flow of power to a load, switching regulators utilize a series switch which is either open or closed *(Figure 1)*. Average output voltage is proportional to the ratio of switch closed time to switch open time, expressed as the switch duty cycle.

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad (1)$$

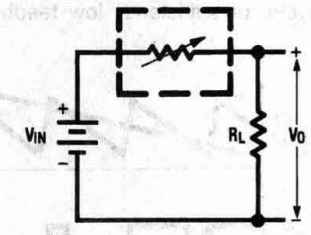

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FIGURE 1a. Linear Regulator

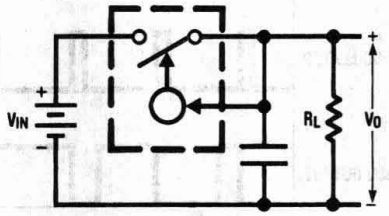

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FIGURE 1b. Switching Regulator

A switching regulator achieves a constant average output by varying the switch duty cycle according to output feedback.

In the LH1605 *(Figure 2)*, a pulse-width modulator operating at a frequency determined by an external capacitor, C_T, varies the duty cycle of a Darlington transistor switch according to the feedback voltage applied to pin 3.

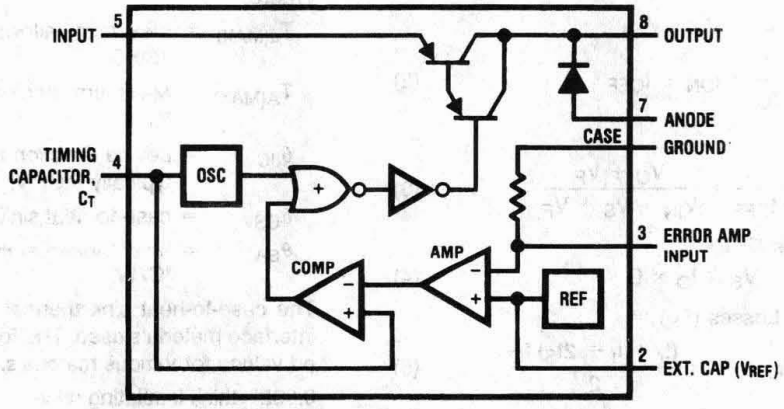

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FIGURE 2. Block Diagram of the LH1605

To achieve precise regulation, the difference between the feedback voltage and the internal reference is amplified, creating an error voltage which varies inversely with the feedback signal. This error voltage is compared to a periodic ramp voltage created across C_T by a constant current source within the oscillator. Comparator output is low until the ramp voltage exceeds the error voltage. *Figure 3* illustrates how fluctuations in error voltage alter the duty cycle of the comparator's output.

The comparator output is logically combined with a blanking pulse created by the oscillator while discharging C_T. This produces a constant frequency switch drive signal whose leading edge coincides with the falling edge of the blanking pulse. Note that, because the oscillator blanking pulse is shorter than the combined delay time of the drive signal buffer and the switch transistors, the LH1605 can run at 100% duty cycle for sufficiently low feedback voltage on pin 3.

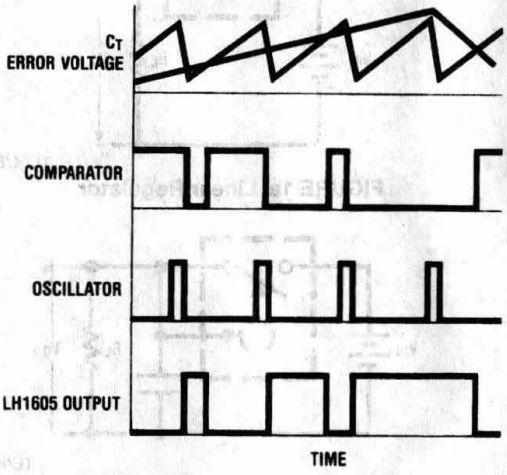

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FIGURE 3. LH1605 Timing Diagram

EFFICIENCY CALCULATIONS

Because high-efficiency is the principle advantage of switched-mode power conversion, switching regulator losses are an important design concern. Losses and efficiency of the LH1605 can be calculated with the following equations. (Note: pin 7 is grounded; I_O = average current output at pin 8.)

Switching Period (T) =

$$\frac{1}{f_O} = t_{ON} + t_{OFF} \tag{2}$$

Duty Cycle (D) =

$$\frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_O + V_F}{V_{IN} - V_S + V_F} \tag{3}$$

Transistor DC Losses (P_T) =

$$V_S \times I_O \times D \tag{4}$$

Transistor Switching Losses (P_S) =

$$(V_{IN} + V_F) \times I_O \times \frac{(t_r + t_f + 2t_S)\, f_O}{2} \tag{5}$$

Diode DC Losses (P_D) =

$$V_F \times I_O \times (1 - D) \tag{6}$$

Drive Circuit Losses (D_L) =

$$\frac{V_{IN}^2}{300} \times D \tag{7}$$

Power Output (P_O) =

$$\frac{(V_{IN} - V_S)\, t_{ON} - (V_F)\, t_{OFF}}{t_{ON} + t_{OFF}} \times I_O \tag{8}$$

Efficiency (η) =

$$\frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_T + P_S + P_D + D_L} \tag{9}$$

As with all switching regulators, the LH1605 requires some external filter to achieve a non-pulsating output. The overall circuit efficiency, therefore, must include power losses in the filter section (discussed later) as well as losses in the LH1605.

From equation 5, it follows that LH1605 efficiency is improved as the operating frequency is reduced. Efficiency can also be improved by adding an external Schottky diode with the LH1605's as shown in *Figure 4*. Schottky diodes exhibit almost no storage time and have a very low forward voltage drop. When using an external Schottky diode, the steering diode at pin 7 should be left open to insure that it contributes no storage delay losses.

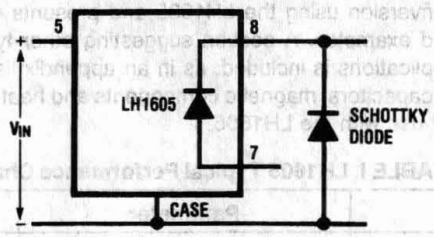

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FIGURE 4. LH1605 with External Schottky Diode

HEAT SINKING CONSIDERATIONS

Even at moderate output power, there is significant self-heating of the LH1605 due to internal power dissipation. To prevent thermal damage, the junction temperature, T_j, must remain below 150°C under all operating conditions. Some useful expressions for steady state thermal design are given below:

$$P_{DISS} = \frac{P_O - \eta P_O}{\eta} < \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JC} + \theta_{CS} + \theta_{SA}} \tag{10}$$

$$\theta_{CS} + \theta_{SA} < \frac{T_{J(MAX)} - T_{A(MAX)}}{P_{DISS}} - \theta_{JC} \tag{11}$$

Where:

$T_{J(MAX)}$ = maximum allowable junction temperature, 150°C.

$T_{A(MAX)}$ = Maximum ambient operating temperature in °C.

θ_{JC} = device junction-to-case thermal resistance, typically 5°C/W.

θ_{CS} = case-to-heat sink thermal resistance in °C/W.

θ_{SA} = heat sink-to-ambient thermal resistance in °C/W.

The case-to-heat sink thermal resistance depends on the interface materials used. The following list gives the expected values for various materials.

0.002″ thick insulating mica

without thermal grease	1.20°C/W
with thermal grease	0.35°C/W

0.003″ thick insulating mica
- without thermal grease 1.30°C/W
- with thermal grease 0.38°C/W

Bare joint
- without thermal grease 0.50°C/W
- with thermal grease 0.15°C/W

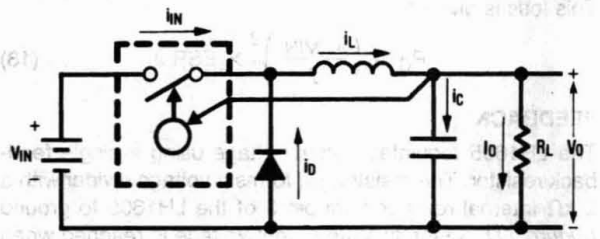
Most heat sink manufacturers provide the heat sink-to-ambient thermal resistance under convection as well as forced-air cooling. Appendix A gives a partial list of hardware and manufacturers.

DC/DC CONVERSION

The LH1605 operates only in Buck-type DC/DC converters. A Buck converter produces a positive DC output voltage which is less than its input voltage. It consists of a switching regulator, a steering diode, an inductor and a capacitor (*Figure 5*). During the switch ON time, inductor current, i_L, builds, flowing to both the capacitor and the load. During t_{OFF}, the magnetic energy stored in the inductor draws current through the diode. The capacitor serves to filter the output voltage by sourcing current while i_L is low and sinking current when i_L is high.

Figure 6 illustrates the current waveforms of the paths labeled in *Figure 5*.

As the load increases, more current must be supplied to maintain a given output voltage. The switching regulator senses the drop in V_O and increases switch duty cycle to raise the average i_L. Likewise, a reduction in loading causes a reduction in switch duty cycle.



TL/K/5496–6

FIGURE 5. Buck-Type Step-Down Voltage Converter

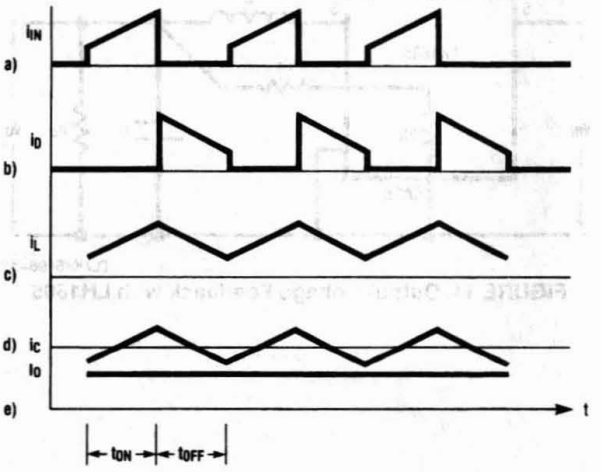


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FIGURE 6. Buck Converter Current Waveforms

INDUCTOR DESIGN

The primary function of the inductor in a switching converter is to reduce the ripple current flowing to the output node. Inductor current, *Figure 6c*, consists of a DC value equal to the average converter output current, I_O, and a ripple current whose peak-to-peak value is:

$$\Delta I_L = \frac{(V_{IN} - V_O)}{L} \times t_{ON} \quad (12)$$

If ΔI_L is greater than $2I_O$, i_L will become zero for a portion of each switching cycle (*Figure 7*), which may result in an unstable output voltage.

To maintain $i_L > 0$, L must be made large enough so that:

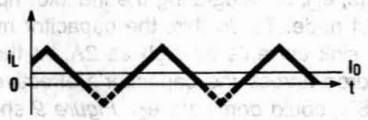
$$I_{O(MIN)} > \frac{[V_{IN(MAX)} - V_O]}{2L} \times t_{ON} \quad (13)$$

Equation 14 conveniently expresses the minimum required inductance as a function of $I_{O(MIN)}$ and the operating frequency, f_O.

$$L > [V_{IN(MAX)} - V_O] \left(\frac{V_O}{V_{IN(MAX)}}\right) \times \frac{1}{2f_O} \times \frac{1}{I_{O(MIN)}} \quad (14)$$

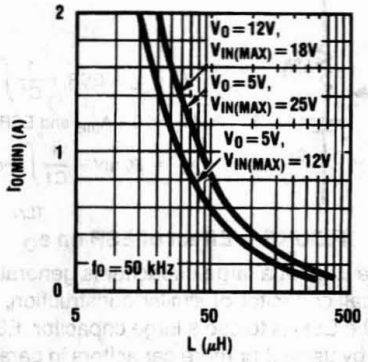
The graph in *Figure 8* plots L vs $I_{O(MIN)}$ for some common converter parameters.

The next consideration for inductor design is the choice of an appropriate magnetic core. The core must provide the desired inductance without saturating under maximum output conditions. Magnetic core saturation leads to excessive inductor current which jeopardizes output stability and may damage both the switching regulator and the load circuitry it supplies.



TL/K/5496–8

FIGURE 7. Inductor Current with $\Delta I_L > 2I_O$



TL/K/5496–9

FIGURE 8. Inductance vs Minimum Output Current

Switching converter inductor cores are normally made of ferrite or molypermalloy powder to minimize core loss at high switching frequencies. The core should provide a closed flux path to minimize radiated noise due to flux leakage. Toroidal and fully enclosed pot cores are popular for this reason.

To further reduce flux leakage, the core winding should be a single layer covering a maximum amount of the winding surface. The number of winding turns necessary for an inductance, L, is:

$$N = 1000 \times \sqrt{\frac{L}{L_{1000}}} \qquad (15)$$

Core manufacturers specify the nominal inductance, L_{1000} mH per 1000 turns, for a given core as well as the maximum magnetic energy, LI^2, that a core can sustain without saturation. LI^2 is calculated using L as determined by equation 14 and I equal to the maximum anticipated output current plus $I_{O(MIN)}$.

When using a core with optimum magnetic performance at the desired switching frequency, the I^2R loss in the winding will dominate inductor power losses. This loss,

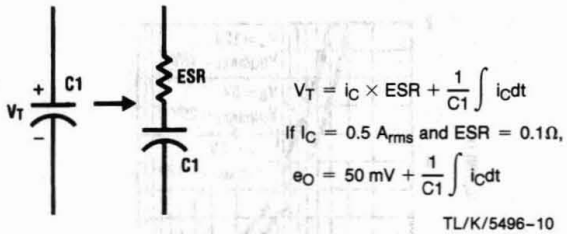
$$P_L = I_O^2 \times R_L \text{ (DC winding resistance)} \qquad (16)$$

can be reduced by using large diameter copper wire for the core winding.

Many magnetic core manufacturers offer further information on inductor design. Some companies now specialize in supplying pre-wound inductors to meet specific switching converter needs. A partial list of core manufacturers and inductor suppliers is included in Appendix A.

CHOOSING AN OUTPUT CAPACITOR

The output filter capacitor reduces the peak-to-peak output ripple voltage, e_O, by integrating the inductor ripple current at the output node. To do this, the capacitor may have to source and sink currents as high as 2A. At these current levels, the drop across the capacitor's effective series resistance, ESR, could dominate e_O. *Figure 9* shows an example where no amount of capacitance could achieve less than 50 mV output ripple.



TL/K/5496–10

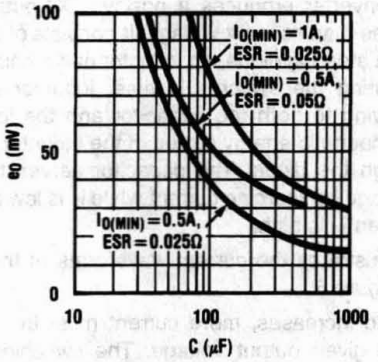
FIGURE 9. Effect of ESR on e_O

Because the ESR of a large capacitor is generally less than that of a small capacitor of similar construction, the easiest way to reduce ESR is to use a large capacitor. ESR can also be reduced by using 2 or more capacitors in parallel. Capacitor leads and the PC board traces connecting them contribute to the ESR and should be made as short as possible. To reduce output voltage spikes due to switching transients, a 0.1 μF ceramic capacitor should be used in parallel with an electrolytic capacitor. A partial list of manufacturers of low ESR capacitors is included in Appendix A.

Equation 17 is a convenient expression for determining the minimum required capacitance as a function of e_O, f_O, ESR, and the inductor ripple current.

$$C > \frac{I_{O(MIN)}}{4f_O} \times \frac{1}{e_O - (I_{O\,(MIN)} \times ESR)} \qquad (17)$$

Figure 10 plots C vs e_O for some common converter parameters.



TL/K/5496–11

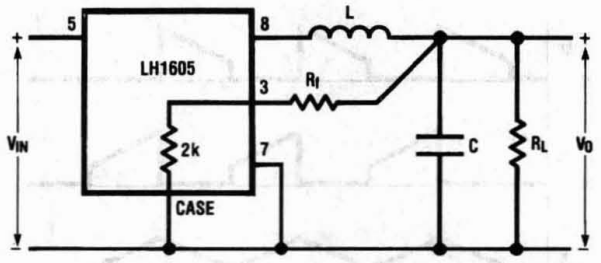
FIGURE 10. Capacitance vs Output Ripple Voltage

Power loss in a filter capacitor is almost entirely due to ESR. This loss is given by:

$$P_C = \left(\frac{I_{O(MIN)}}{2}\right)^2 \times ESR \qquad (18)$$

FEEDBACK

The LH1605 regulates output voltage using a single feedback resistor. The resistor, R_f, forms a voltage divider with a 2 kΩ internal resistor from pin 3 of the LH1605 to ground *(Figure 11)*. A steady state output voltage is reached when the voltage on pin 3 is approximately equal to the reference voltage on pin 2, about 2.5V.



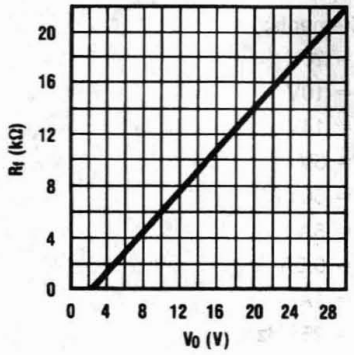
TL/K/5496–12

FIGURE 11. Output Voltage Feedback with LH1605

The output voltage can be programmed by selecting a feedback resistor as follows:

$$R_f = 2\,k\Omega \frac{V_{OUT} - 2.5V}{2.5V} \quad (19)$$

Figure 12 shows the linear relationship between R_f and V_O.



TL/K/5496–13

FIGURE 12. Feedback Resistance vs Output Voltage

CURRENT LIMITING

LH1605 current limiting is best done by pulling down the reference voltage at pin 2. This reduces the output pulse-width on a cycle-to-cycle basis. Clamping the reference to ground inhibits the output switch and can be done with any general purpose transistor.

A 10 μF capacitor from pin 2 to ground will allow the LH1605 to recover with a soft start from an over-current condition. *Figure 13* illustrates a typical current limit circuit for the LH1605 requiring only two transistors and three resistors.

Although this circuit is effective, it has several shortcomings. The −2.2 mV/°C TC of Q1 can cause a 34% drift in the current limit set point over the −25°C to +85°C temperature range, and the relatively large R_S can decrease overall converter efficiency by as much as 10%. Furthermore, a short circuit condition draws significant power from the input supply. Superior performance can be obtained from a foldback current limit with only a slightly higher parts count.

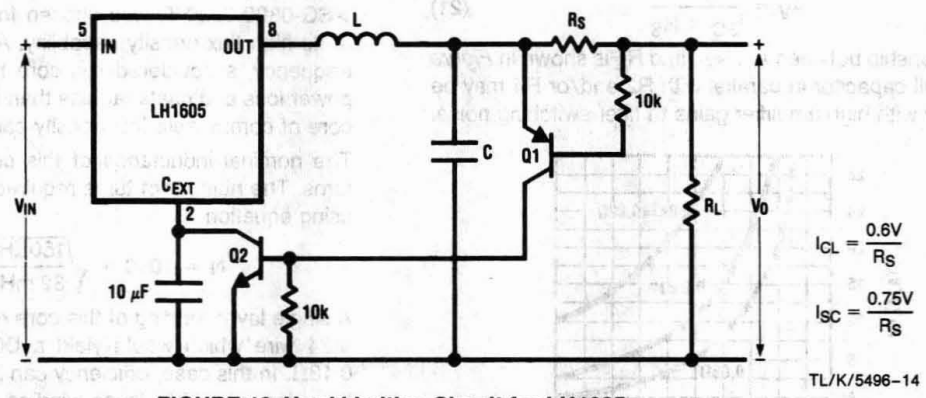
FOLDBACK CURRENT LIMITING

A foldback current limit reduces the current limit threshold as the converter's load increases from an initial overcurrent condition to a complete short circuit. Because short circuit current, I_{SC}, is much less than the initial current limit set point, I_{CL}, a prolonged short circuit draws very little power from the input supply.

In the circuit of *Figure 14*, initial current limit is reached when the output of Q2 reaches 0.6V, $V_{BE(ON)}$ of Q1.

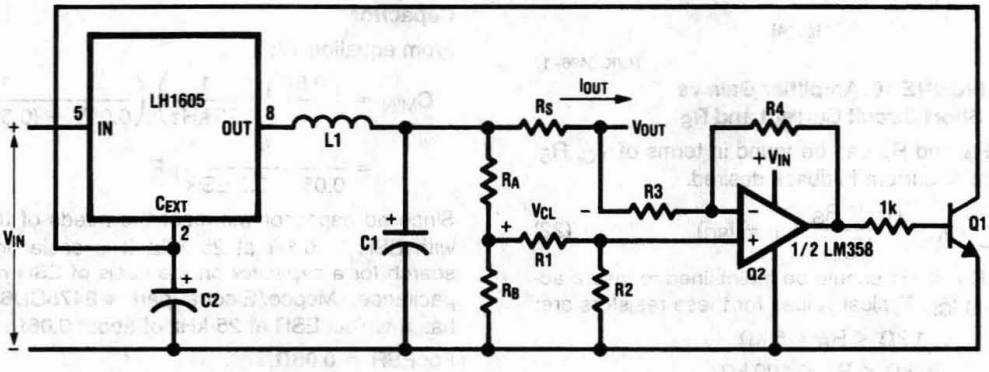
This corresponds to $V_{CL} = \frac{0.6V}{A_V}$ where

$$A_V = \frac{R2}{R1},\ R1 = R3,\ R2 = R4. \quad (20)$$



TL/K/5496–14

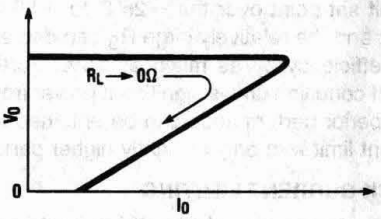
FIGURE 13. Hard Limiting Circuit for LH1605



TL/K/5496–15

FIGURE 14. Foldback Limiting for LH1605

V_{CL} is the sum of the voltage drop across R_S and the opposing drop across R_A. As current limit is reached, V_O is reduced, lowering the voltage across R_A. It then requires less current through R_S to create a V_{CL} sufficient to cause further current limiting. This action produces the I-V characteristics shown in *Figure 15*. As the overload is removed, the converter output recovers along the same curve.



TL/K/5496–16

FIGURE 15. V_O vs I_O with Foldback Limiting

Because the gain of Q2 can be quite large, generally 10 to 20, the sense resistor, R_S, can be made very small, 0.02Ω to 0.06Ω. This significantly improves overall converter efficiency. Another advantage of amplifier gain is increased temperature stability. A gain of 10 reduces I_{CL} drift to about −3.3 mA/°C with R_S = 0.06Ω

The first step in designing a foldback current limit for the LH1605 is to choose a readily available value for R_S. Then the amplifier gain can be determined as a function of R_S and the desired short circuit current.

$$A_V = \frac{0.6}{I_{SC} \times R_S} \qquad (21)$$

The relationship between A_V, I_{SC}, and R_S is shown in *Figure 16*. A small capacitor in parallel with R2 and/or R4 may be necessary with high amplifier gains to filter switching noise.

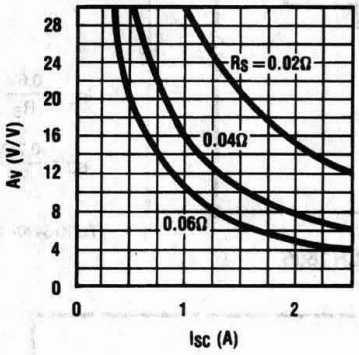


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FIGURE 16. Amplifier Gain vs Short Circuit Current and R_S

The resistors R_A and R_B can be found in terms of V_O, R_S, and the amount of current foldback desired.

$$R_A = \frac{R_B \times R_S}{V_O} (I_{CL} - I_{SC}) \qquad (22)$$

The condition $R_B \ll R1$ should be maintained to insure accuracy in setting I_{CL}. Typical values for these resistors are:

$$1\ k\Omega < R_B < 5\ k\Omega$$

$$20\ k\Omega < R1 < 100\ k\Omega$$

Power loss due to the current limit circuit under normal converter operation is:

$$P_{CL} = I_O^2 \times R_S \qquad (23)$$

Power drained from the input supply with the converter output short circuited cannot be easily expressed due to the nature of the LH1605's control loop while in current limit. The drain, however, can be minimized by using a foldback current limit with a low I_{SC}.

Design Example

Design requirements:

$V_{IN(MAX)}$ = 20V
$V_{IN(MIN)}$ = 10V
$V_{IN(NOM)}$ = 14V
V_O = 5V
e_O = 50 mV
I_{CL} = 5A
$I_{O(MIN)}$ = 0.5A
I_{SC} = 1A
f_O = 25 kHz

Inductor

From equation 14:

$$L_{MIN} = (20V - 5V)\left(\frac{5V}{(20V)}\right)\left(\frac{1}{2}\right)\left(\frac{1}{25\ kHz}\right)\left(\frac{1}{0.5A}\right)$$

$$= 150\ \mu H.$$

The maximum magnetic energy will be:

$$E_L = (150\ \mu H)\ (5A + 0.5A)^2 = 4.54\ mJ.$$

A toroidal powdered-iron core from Arnold Engineering, part #SG-0800-0320-T, was chosen for this example because of its high flux density capability. At only 25 kHz switching frequency, a powdered-iron core has very little hysteresis power loss and costs far less than a molypermalloy powder core of comparable flux density capability.

The nominal inductance of this core is 32 mH per 1000 turns. The number of turns required for this design is found using equation 15:

$$N = 1000 \times \sqrt{\frac{150\mu H}{32\ mH}} = 69\ turns$$

A single layer winding of this core requires about 5.1 feet of #24 wire which would yield a DC winding resistance of 0.13Ω. In this case, efficiency can be improved significantly by using a double layer winding of #20 wire with only 0.050Ω.

Capacitor

From equation 17:

$$C_{MIN} = \left(\frac{0.5A}{4}\right)\left(\frac{1}{25\ kHz}\right)\left(\frac{1}{0.05V - (0.5A \times ESR)\ V}\right)$$

$$= \frac{5}{0.05 - 0.5\ ESR}\ \mu F$$

Since no capacitor will meet the needs of this application with ESR > 0.1Ω at 25 kHz, it is easier in this case to search for a capacitor on the basis of ESR rather than capacitance. Mepco/Electra part #3475GD681M6P3JMBS has a typical ESR at 25 kHz of about 0.06Ω.

For ESR = 0.06Ω,

$$C_{MIN} = 250\ \mu F.$$

This part, rated at 680 μF, 6.3 WV_{DC}, is more than adequate for this application.

Feedback

From equation 19:

$$R_f = 2\,k\Omega\,\frac{5V - 2.5V}{2.5V} = 2\,k\Omega.$$

Current Limit

$R_S = 0.05\Omega$, 1.5W will be used in this application.

From equations 21 and 22:

$$A_V = \frac{0.6V}{1A \times 0.05\Omega} = 12,$$

$$R_A = R_B\left(\frac{0.05\Omega}{5V}\right)(5A - 1A) = 0.04\,R_B.$$

If $R_B = 2\,k\Omega$ and R1 = 100 kΩ, then,

$R_A = 80\Omega$,

R2 = R4 = 1.2 MΩ,

R3 = 100 kΩ.

Operating Frequency

From the LH1605 data sheet graph of C_T vs f_O, the desired timing capacitor is,

$$C_T = 0.001\,\mu F.$$

Input Capacitor

The choice of this capacitor depends upon the source impedance and ripple voltage requirements of the input supply. In most applications,

$$C_{IN} > 50\,\mu F$$

The complete circuit is shown in *Figure 17*.

Using LH1605 data sheet information and equations 2–9 of this note, LH1605 efficiency in this design with V_{IN} = 14V and I_O = 3A is,

$$\eta = \frac{15}{15 + 1.66 + 2.34 + 2.59 + 0.30} = 0.69$$

Equation 11 gives the maximum allowable thermal resistance of heat sink bolted directly to the LH1605 with thermal grease at 50°C ambient temperature:

$$\theta_{SA} = \frac{(150°C - 50°C)}{6.89W} - 5°C/W - 0.15°C/W$$

$$= 9.4°C/W$$

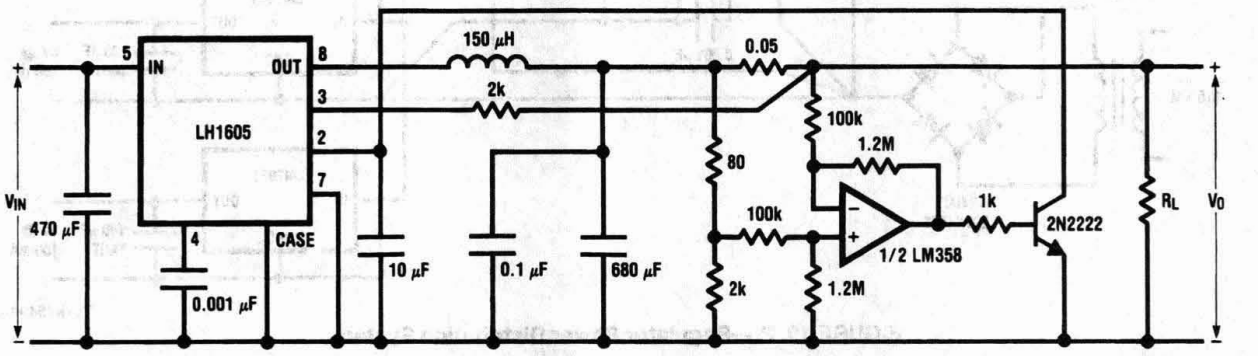
By including the power losses found in equations 16, 18 and 23, equation 9 yields the overall converter efficiency:

$$\eta = \frac{15}{21.89 + 0.45 + 0.004 + 0.45} = 0.66$$

So, in this design example, the converter dissipates only 7.8W, whereas a linear regulator under identical input/output conditions would dissipate 27W.

TYPICAL APPLICATIONS

Figure 18 shows a typical LH1605 Buck regulator application powered from the rectified output of a step-down transformer. Because LH1605 regulation is more efficient than equivalent linear regulation, the size and power rating of the transformer and bridge rectifier can be much smaller. Table II contains component values for several converters with this topology.



TL/K/5496–18

FIGURE 17. Complete Buck Converter Using LH1605

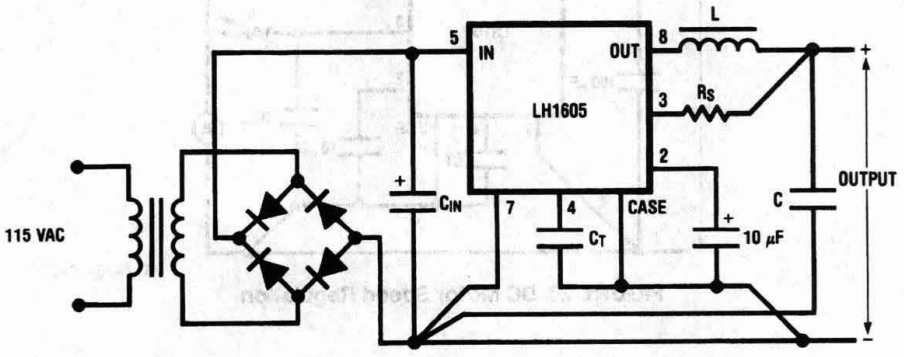


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FIGURE 18. Typical Power Supply System

TABLE II. Typical Component Values for Buck Regulators

f_O = kHz, e_O = 50 mV			$I_{O\ (MIN)}$				
			1.0A		0.5A		
ESR_C (Ω)	$V_{IN\ (MAX)}$ (V)	V_O (V)	L_{MIN} (μH)	C_{MIN} (μF)	L_{MIN} (μH)	C_{MIN} (μF)	R_f (Ω)
0.02	12	5	59	334	117	125	2k
0.03	15	5	67	500	134	143	2k
0.04	25	12	125	1000	250	167	7.6k
0.05	35	24	151	—	302	200	17.2k

Power Distribution Pre-Regulator

In applications requiring very low output ripple voltage, the LH1605 can be used as a pre-regulator to improve system performance and efficiency *(Figure 19)*. By pre-regulating the input to the linear regulators to 5.8V, line frequency ripple is virtually eliminated from the 5V output. The 25 kHz switching ripple is attenuated 70 dB by the LM2931's giving less than 1 mV total output noise voltage.

DC Motor Speed Controller

Figure 20 shows how an LH1605 can be connected as a fractional-horsepower, DC motor speed controller. The constant average output voltage of the LH1605 is set with a single resistor, R_f, as it is in Buck converter applications. Current limiting may be required to protect the LH1605 during start-up of motors with low armature resistance.

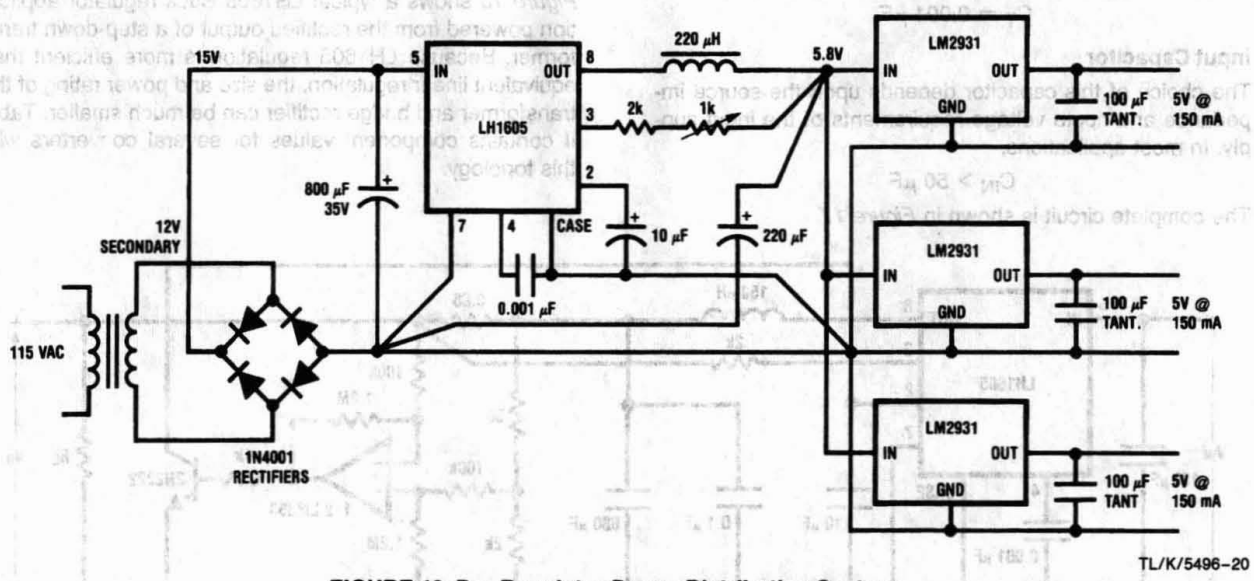

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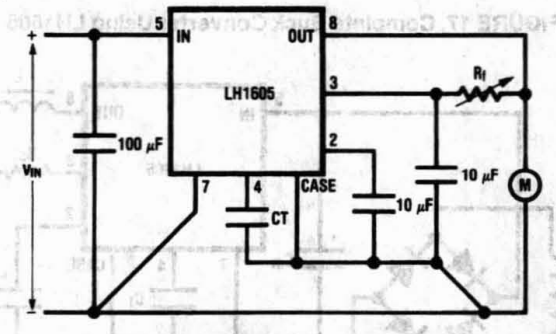
FIGURE 19. Pre-Regulator Power Distribution System



TL/K/5496–21

FIGURE 20. DC Motor Speed Regulation

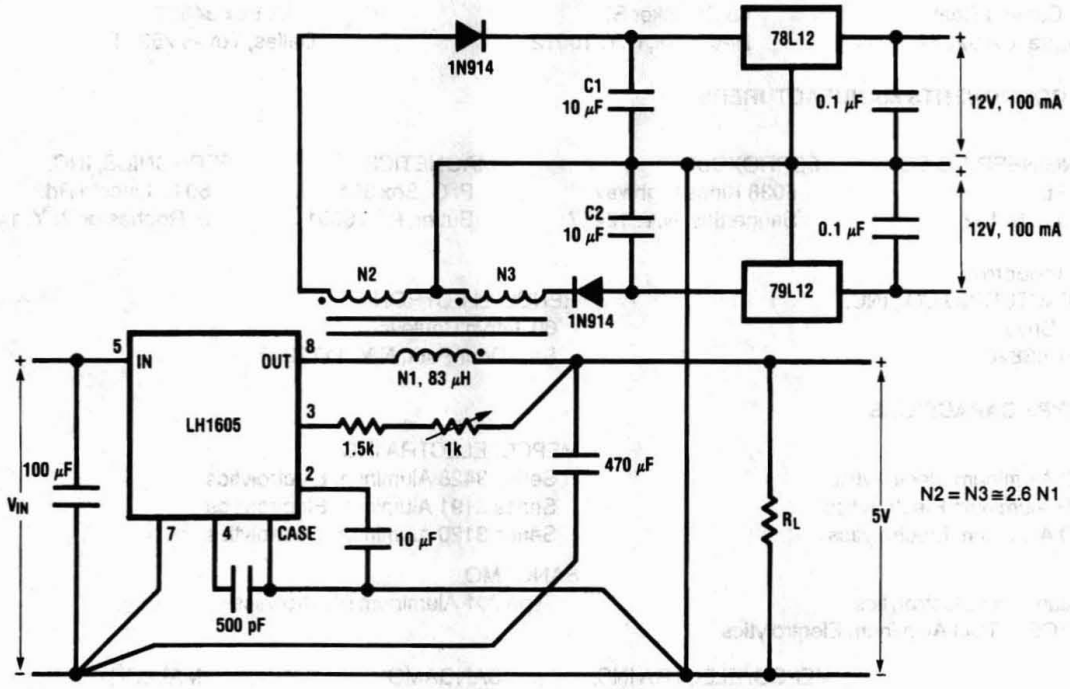
Multiple Outputs

It is possible, as *Figure 21* suggests, to obtain any number of outputs from a single LH1605 provided there is one primary output in a Buck configuration drawing sufficient output current. During t_{OFF}, the voltage across the primary inductance is $(V_O + V_f)$. The voltage across any secondary windings wound on the same core is N_S/N_p $(V_O + V_f)$. Because V_O is regulated and V_f is nearly constant, the voltages on the secondaries are also constant.

During t_{ON}, the diodes in the secondaries are reverse biased so all secondary power comes from the filter capacitors, C1 and C2. During t_{OFF}, the diodes conduct, and the capacitors are recharged. To ensure stable output voltages, the Buck converter's output power must be greater than that of the secondaries. In the circuit of *Figure 21*, $I_O \geq 0.8A$ in the 5V primary is necessary in order to have 100 mA capability in the ±12V secondaries.

REFERENCES

1. National Semiconductor, 1982 Hybrid Products Databook.
2. National Semiconductor, "LH1605 5 Amp, High Efficiency Switching Regulator" datasheet.
3. Abraham I. Pressman, "Switching and Linear Power Supply, Power Converter Design", Hyden Book Company, 1977.



TL/K/5496–22

FIGURE 21. Multiple Output Voltages from a Single LH1605

APPENDIX A

Following is a partial list of sockets, heat dissipators, magnetic components and low ESR-type capacitors for use with the LH1605. National Semiconductor Corporation assumes no responsibility for their quality or availability.

8-LEAD TO-3 HARDWARE

Sockets

Robinson Nugent 0002011
Azimuth 6028 (test socket)

Heat Sinks

Thermalloy 2266B (35°C/W)
IERC LAIC 3B4CB
IERC HP1-TO3-33CB (7°C/W)
AAVID 5791B

Mica Washers

Keystone 4658

AAVID ENGINEERING
30 Cook Court
Laconia, New Hampshire 03246

IERC
135 W. Magnolia Blvd.
Burbank, CA 91502

ROBINSON NUGENT INC.
800 E. 8th St.
New Albany, IN 47150

AZIMUTH ELECTRONICS
2377 S. El Camino Real
San Clemente, CA 92672

KEYSTONE ELECTRONICS CORP.
49 Bleecker St.
New York, N.Y. 10012

THERMALLOY
P. O. Box 34829
Dallas, Texas 75234

MAGNETIC COMPONENTS MANUFACTURERS

Cores

ARNOLD ENGINEERING CO.
300 West St.
Marengo, ILL. 60152

FERROXCUBE
5038 Kings Highway
Saugerties, N.Y. 12477

MAGNETICS
P. O. Box 391
Butler, PA 16001

FERRONICS, INC.
60 N. Lincoln Rd.
E. Rochester, N.Y. 14445

Pre-Wound Inductors

GFS MANUFACTURING CO., INC.
6 Progress Drive
Dover, N.H. 03820

RENCO ELECTRONICS
60 Jefryn Boulevard
East Deer Park, N.Y. 11729

LOW ESR-TYPE CAPACITORS

SPRAGUE
Type 672D Aluminum Electrolytics
Type 32DR Aluminum Electrolytics
Type 622D Aluminum Electrolytics

MEPCO/ELECTRA INC.
Series 3428 Aluminum Electrolytics
Series 3191 Aluminum Electrolytics
Series 3120 Aluminum Electrolytics

MALLORY
Type TT Aluminum Electrolytics
Types CG/CGS/TCG Aluminum Electrolytics

SANGAMO
Type 301 Aluminum Electrolytics

SPRAGUE
481 Marshall St.
North Adams, MA 01247

MEPCO/ELECTRA INC.
265 Industrial Dr.
Roxboro, NC 27573

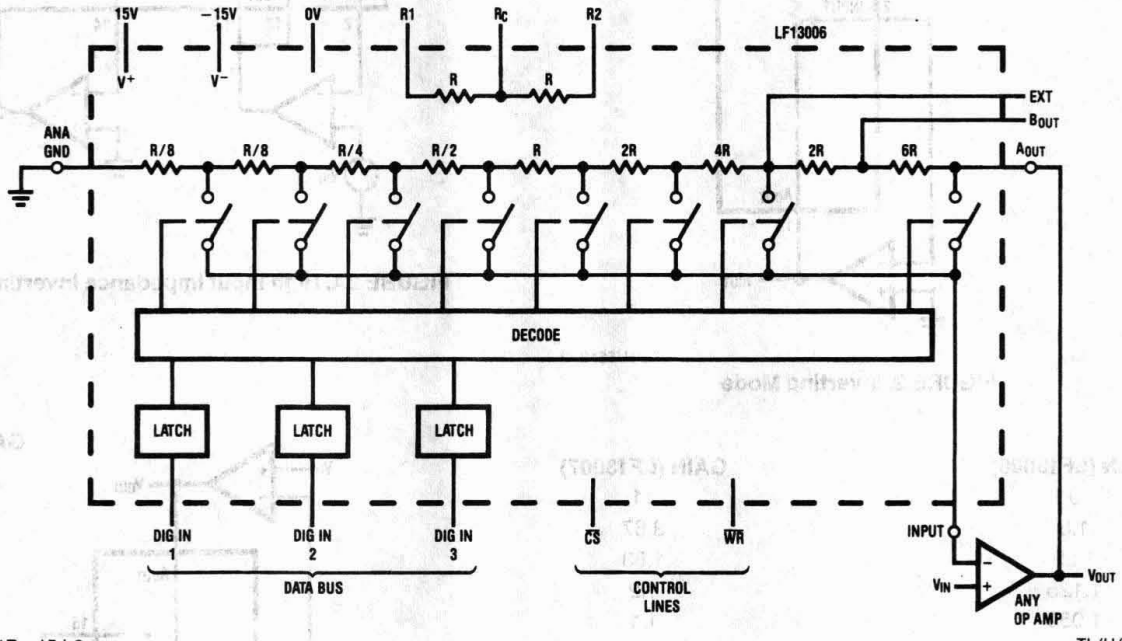
SANGAMO
P. O. Box 128
Pickens, SC 29671

MALLORY
P. O. Box 1284
Indianapolis, IN 46206

LF13006/LF13007 Precision Digital Gain Set Applications

National Semiconductor
Application Note 344

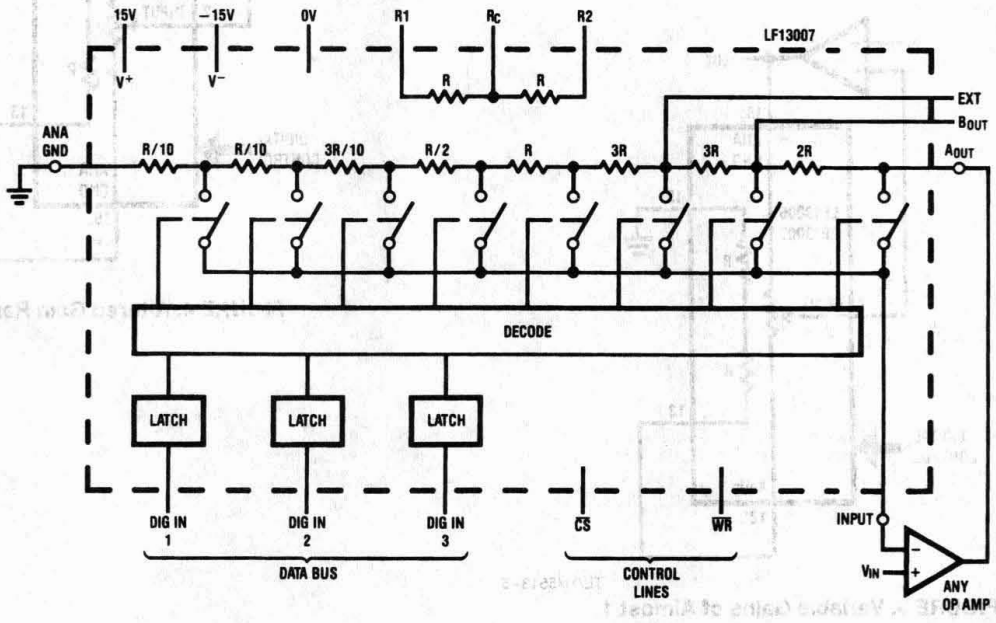
Some basic circuit configurations for using the LF13006 and LF13007 are shown in *Figures 1 through 4*. In each case only the Digital Gain Set and an op-amp are required, although in some instances the amplifier may need external compensation in order to maintain stability over wide ranges of closed loop gain. As shown, inverting and noninverting configurations are possible with several variations. Nearly unlimited values of gain can be realized using different combinations of outputs and/or the additional resistors at R1, Rc, and R2 to modify an amplifier's input or feedback.



Note: 1R = 15 kΩ

TL/H/5513–1

FIGURE 1A. LF13006, GAIN = 1 to 128 in Binary Sequence



Note: 1R = 15 kΩ

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FIGURE 1B. LF13007, GAIN = 1 to 100 in "1, 2, 5" Sequence

Of significant interest are circuits such as in *Figure 3*, which allow gain switching at values near one. These configurations can be useful where in-circuit trimming may be needed for small, narrow range adjustments. Also, by cascading two circuits, high resolution as well as wide gain range can be realized. For example, by using *Figure 4* in conjunction with *1A*, the programmed gains of 1.2 and 1.7 can be used to "fill in" between the binary steps supplied by *1A*. In audio applications, this particular arrangement would provide steps of 3 dB or less over a 46 dB range and slightly larger steps to 57 dB.

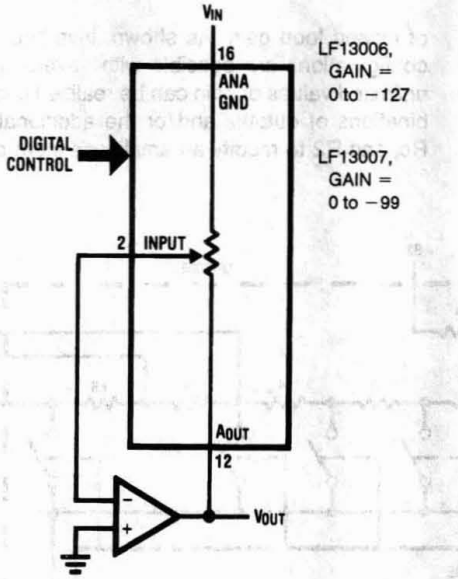

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FIGURE 2. Inverting Mode

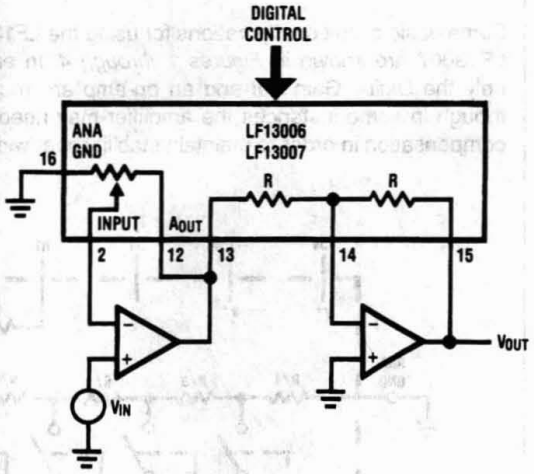

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FIGURE 2A. High Input Impedance Inverting Mode

GAIN (LF13006)	GAIN (LF13007)
9	11
1.8	3.67
1.29	1.83
1.125	1.2
1.059	1.1
1.029	1.048
1.014	1.02
1.007	1.01

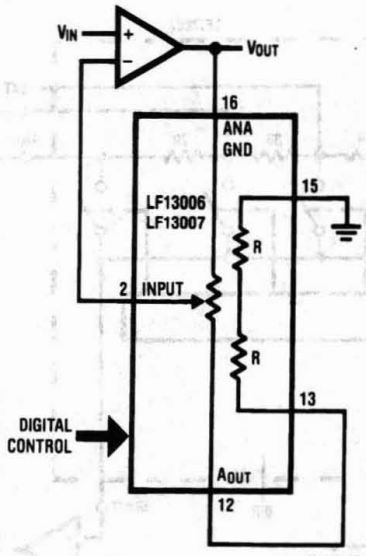

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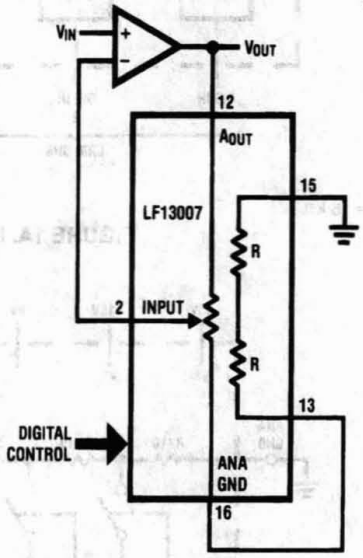
FIGURE 3. Variable Gains of Almost 1



GAIN (13007)
1.0
1.2
1.7
3.0
4.0
4.8
5.45
5.7

TL/H/5513–6

FIGURE 4. Altered Gain Range

Applications for these devices also include a wide variety of circuits besides those which simply switch op-amp gain. A simple digital "handle" on one or more other circuit parameters can do a great deal to enhance the capabilities of many analog designs. In circuits such as filters, precision references, current sources, and countless others, the addition of programming capability can be invaluable.

One good example of such versatility is shown in a digitally adjustable low pass filter in *Figure 5*. Applications for this function include variable bandwidth front-ends for data acquisition and "smart" filters for DC signals which combine fast settling with high noise rejection. This can be done by increasing bandwidth in the presence of a large input-to-output differential at the filter, and then cutting back as the output gets close to its final level. The corner frequency is easily set via the 3-bit code input to an LF13006 or 7. When using the LF13006, time constants from RxC1 to 128RxC1 can be programmed in binarily weighted steps. The same function performed with a conventional CMOS DAC would need more bits to cover the same range and would still not be able to maintain the precision of setting at its limits of operation.

Time Constant $t = NRC_1$

N = Set gain in basic configuration (N = GAIN of Fig 1)

Circuit operation of the variable low pass is very straightforward. The LF13006 Network along with an LF412 dual op-amp form a resistance "multiplier" in which a settable fraction of the input voltage is used to determine the charge or discharge current though R into C1. One half of the dual amplifier (A1) is used to buffer the LF13006's "output" (Input, pin 2) and provide charging current for C1, while the second op-amp (A2) allows the resistor ladder to float on C1. In addition, the ratio of the selected time-constants will be very precise since these will be proportional to the LF13006's gain accuracy.

To a similar end, a classical capacitance multiplier can be made programmable with the circuit of *Figure 6*. The Digital Gain Set controls what is in effect a high input-impedance inverting amplifier which is used to drive the lower side of C1. The value of the "virtual" capacitor seen at the circuit's input will be C1 multiplied by the programmed gain. A drawback of this scheme is that the signal swing at A1's output can be large and may cause amplifier saturation. Thus for high capacitance multiplication factors, the input swing must be kept small in order to prevent clipping.

$C_{effective} = C_1N$

N = GAIN of Fig 1

Note: Output swing at input op amp is multiplied by set gain. Signal range may be limited.

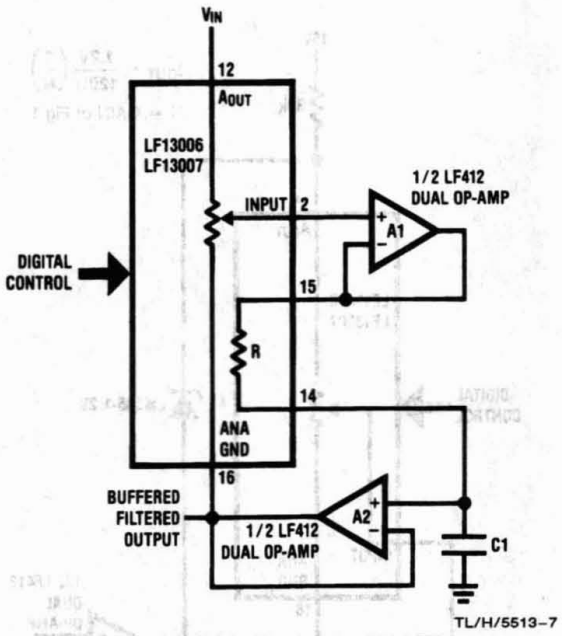


FIGURE 5. Variable Time Constant Filter

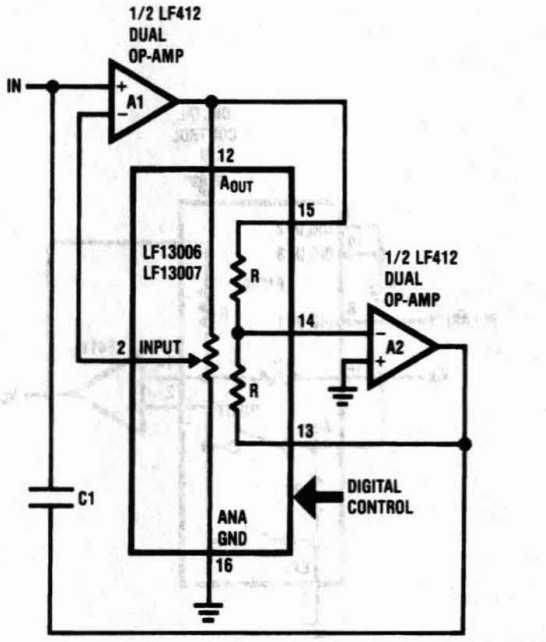


FIGURE 6. Variable Capacitance Multiplier

In *Figure 7*, an LF13006 is used to switch a single amplifier's gain but not quite in the conventional sense in this case. The LF411 op-amp can be flipped from a follower to an inverter using no additional parts and only the "Dig. In 1" input (pin 8) of the gain network. This "two part" approach can be used in precision rectifier and synchronous modulator/demodulator circuits as well as for polarity inverters in front of A to D converters.

The two extra matched resistors that are provided at R1, R2, and Rc (pins 13, 14, 15) are used to set the inverter gain while two of the internal switches are configured to switch the op-amp's noninverting input. The 8R resistor (approximately 120K) which exists from the circuit input to ground is not actually needed but is an unavoidable result of this particular switch connection.

In another example, a precision current source can be given direct digital control by using the simple scheme shown in *Figure 8*. Here, the current source's reference is "floated" on the load terminal (I_{OUT}) by using one half of a Bi-Fet dual op-amp (LF412, A1) as a buffer for the output. This provides a current return path for the gain set's resistor ladder and the circuit's reference (LM385-1.2) which doesn't interfere with the main output. The other half of the Bi-Fet dual (A2) is used to supply the output current via the sense resistor, R1. The current source's output is varied by changing the fraction of the reference voltage which will be forced to appear across R1. With this scheme, the output current is governed by the equation; $I_{OUT} = V_{REF}/(R1 \times \text{Set Gain})$.

Applications for the above circuit include bias sources for programmable amplifiers, linear ramp generators, and variable current limiters. For greater output currents, R1 can be reduced and an external pass transistor can be added to A2's output.

A common need in data acquisition systems is for a differential input amplifier, or instrumentation amplifier, with easily adjustable precision gains. Normally this can't be done without using several precision resistors and switches or employing expensive modular products that have this capability already built in. In *Figure 9*, a differential gain can be varied by using one Digital Gain Set in one version of a three op-amp instrumentation amp circuit. The amplifier's front end uses an LF412A precision dual op-amp as a follower (A1) and also as a variable gain inverter (A2), both which drive the inputs of a fixed gain difference amp (LF411). The instrumentation amp's common-mode performance will directly depend on the four external resistors. For designs where common-mode rejection is critical, close matching of resistor pairs R1, R2 and R3, R4 are required, i.e. 60 dB DC CMRR requires 0.1% matching. However, reasonable rejection can still be achieved (54 dB typ) if only two external resistors are used and the gain set's uncommitted resistors serve as R1 and R2.

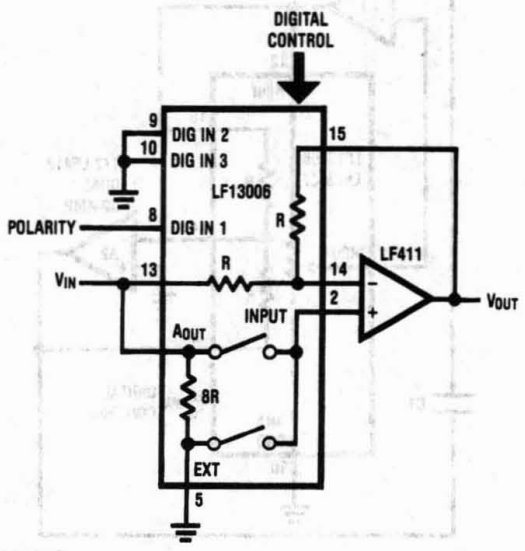


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FIGURE 7. Switchable Gain of ±1

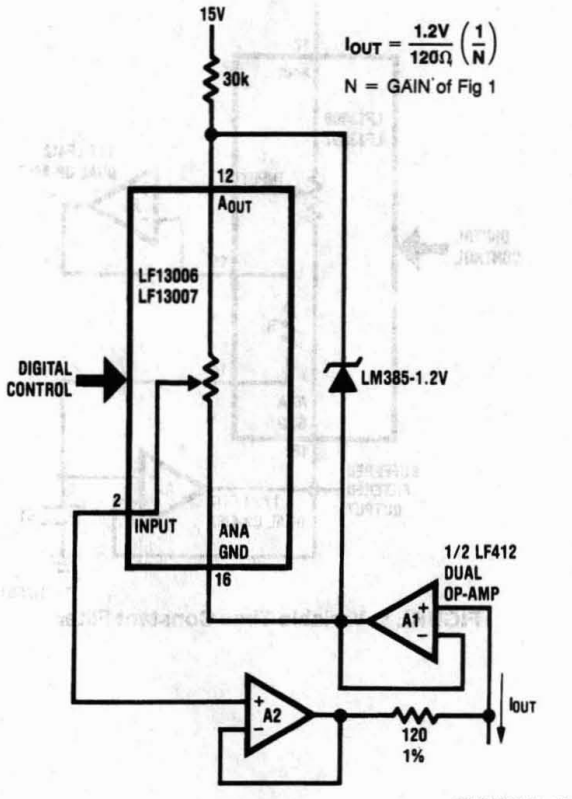

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FIGURE 8. Programmable Current Source

In *Figure 10*, the programmable function generator shown will shift its operating frequency one octave for each LSB change in the program code. Triangle square-wave and sinewave outputs are available over an eight octave range. If an LF13007 were to be used rather than the 13006, the 1, 2, 5 sequence would provide ideal scaling for horizontal sweep or other scanning circuits.

This particular function generator employs ¾ of a quad op-amp as an integrator, comparator, and buffer. The integrator (A1) is driven from a controllable source which is simply the Digital Gain Set used as a passive voltage divider, and buffered by A2. The triangle output from A1 is used to drive a sine shaping circuit consisting of the last quarter of the LF347 (A4) and two dual transistors. Sine distortion can be reduced to 0.5% by trimming the symmetry and waveshape adjustments provided. The circuits' frequency range as shown is from 10 to 1280 Hz.

Note 1: R_1, R_2, R_3, R_4 = 15k

Note 2: For 46 dB min CMRR, R_1, R_2 can be replaced by internal resistors in the LF13006/7

Note 3: For 60 dB CMRR R_1, R_2 and R_3, R_4 must match to 0.1%

Note 4: $V_{OUT} = N(V_A - V_B)$

N = GAIN of Fig 1

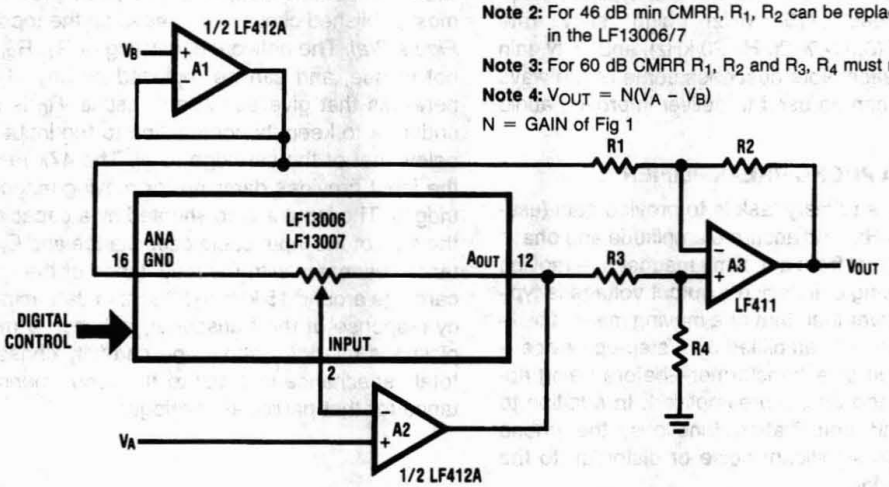

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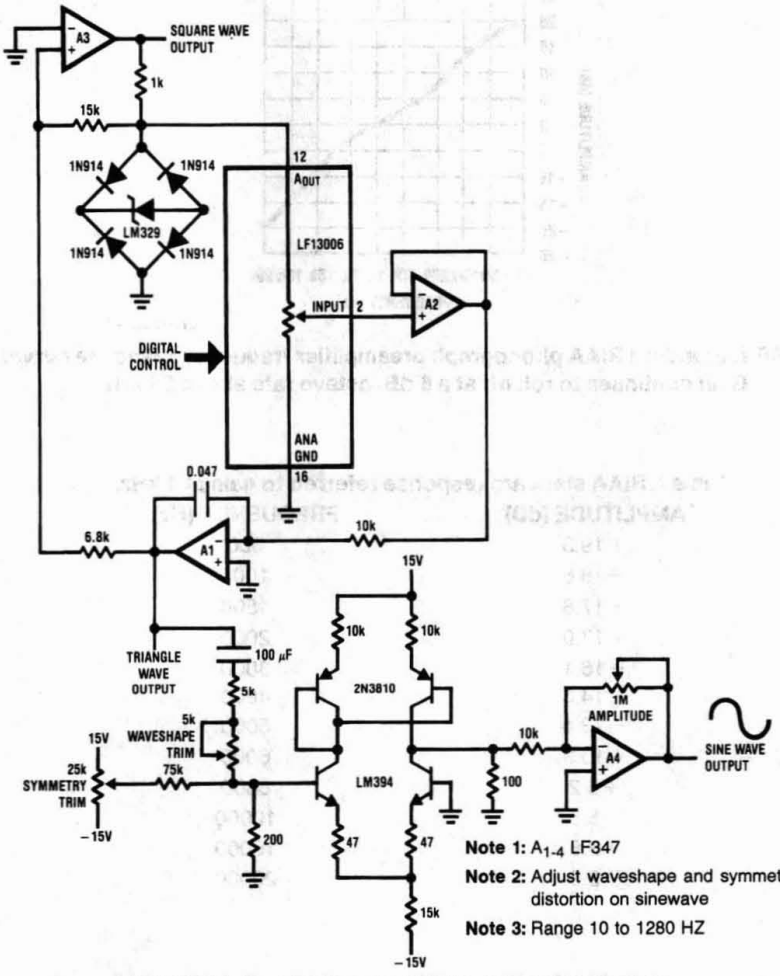
FIGURE 9. Programmable Instrumentation Amp



Note 1: A_{1-4} LF347

Note 2: Adjust waveshape and symmetry trims for lowest output distortion on sinewave

Note 3: Range 10 to 1280 HZ

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FIGURE 10. One Octave per Bit Function Generator

High-Performance Audio Applications of The LM833

National Semiconductor
Application Note 346
Kerry Lacanette

Designers of quality audio equipment have long recognized the value of a low noise gain block with "audiophile performance". The LM833 is such a device: a dual operational amplifier with excellent audio specifications. The LM833 features low input noise voltage (4.5 nV/$\sqrt{Hz}$ typical), large gain-bandwidth product (15 MHz), high slew rate (7V/μSec), low THD (0.002% 20 Hz-20 kHz), and unity gain stability. This Application Note describes some of the ways in which the LM833 can be used to deliver improved audio performance.

I. TWO STAGE RIAA PHONO PREAMPLIFIER

A phono preamplifier's primary task is to provide gain (usually 30 to 40 dB at 1 kHz) and accurate amplitude and phase equalization to the signal from a moving magnet or a moving coil cartridge. (A moving coil device's output voltage is typically around 20 dB lower than that of a moving magnet pickup, so this signal is usually amplified by a step-up device—either an active circuit or a transformer—before being applied to the input of the phono preamplifier). In addition to the amplification and equalization functions, the phono preamp must not add significant noise or distortion to the signal from the cartridge.

Figure 1 shows the standard RIAA phono preamplifier amplitude response. Numerical values relative to the 1 kHz gain are given in Table I. Note that the gain rolls off at a 6 dB/octave rate above 2122 Hz. Most phono preamplifier circuits in commercially available audio products, as well as most published circuits, are based on the topology shown in *Figure 2(a)*. The network consisting of R_1, R_2, C_1, and C_2 is not unique, and can be replaced by any of several other networks that give equivalent results. R_0 is generally well under 1k to keep its contribution to the input noise voltage below that of the cartridge itself. The 47k resistor shunting the input provides damping for moving-magnet phono cartridges. The input is also shunted by a capacitance equal to the sum of the input cable capacitance and C_p. This capacitance resonates with the inductance of the moving magnet cartridge around 15 kHz to 20 kHz to determine the frequency response of the transducer, so when a moving magnet pickup is used, C_p should be carefully chosen so that the total capacitance is equal to the recommended load capitance for that particular cartridge.

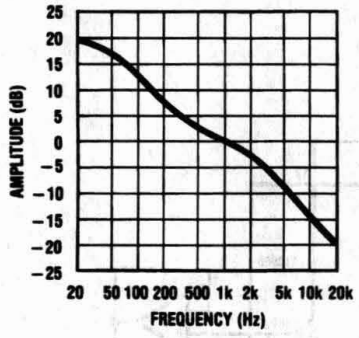

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FIGURE 1. Standard RIAA phonograph preamplifier frequency response curve. Gain continues to roll off at a 6 dB/octave rate above 20 kHz.

Table I. RIAA standard response referred to gain at 1 kHz.

FREQUENCY (Hz)	AMPLITUDE (dB)	FREQUENCY (Hz)	AMPLITUDE (dB)
20	+19.3	800	+0.7
30	+18.6	1000	0.0
40	+17.8	1500	−1.4
50	+17.0	2000	−2.6
60	+16.1	3000	−4.8
80	+14.5	4000	−6.6
100	+13.1	5000	−8.2
150	+10.3	6000	−9.6
200	+8.2	8000	−11.9
300	+5.5	10000	−13.7
400	+3.8	15000	−17.2
500	+2.6	20000	−19.6

The circuit of *Figure 2(a)* has a disadvantage: it cannot accurately follow the curve in *Figure 1*, no matter what values are chosen for the feedback resistors and capacitors. This is because the non-inverting amplifier cannot have a gain of less than unity, which means that the high frequency gain cannot roll off continuously above the 2122 Hz breakpoint as it is supposed to. Instead, a new breakpoint is introduced at the unity gain frequency.

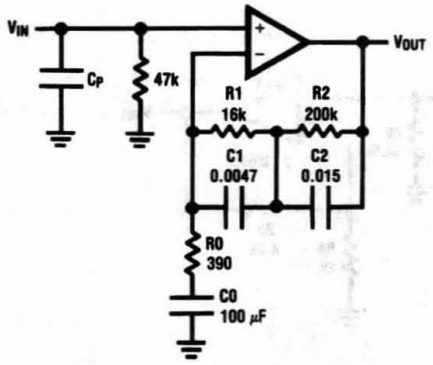
In addition to the amplitude response errors (which can be made small through careful design), the lack of a continued rolloff can cause distortion in later stages of the audio system by allowing high frequency signals from the pickup cartridge to pass through the phono equalizer without sufficient attenuation. This is generally not a problem with moving magnet cartridges, since they are usually severely band-limited above 20 kHz due to the electrical resonance of cartridge inductance and preamp input capacitance. Moving coil cartridges, however, have very low inductance, and can produce significant output at frequencies as high as 150 kHz. If a subsequent preamplifier stage or power amplifier suffers from distortion caused by slew-rate limitations, these ultrasonic signals can cause distortion of the audio signal even though the signals actually causing the distortion are inaudible.

Preamplifers using the topology of *Figure 2(a)* can suffer from distortion due to input stage nonlinearities that are not corrected by the feedback loop. The fact that practical amplifiers have non-infinite common mode rejection ratios means that the amplifier will have a term in its gain function that is dependent on the input voltage level. Since most good operational amplifiers have very high common mode rejection ratios, this form of distortion is usually quite difficult to find in opamp-based designs, but it is very common in discrete amplifiers using two or three transistors since these circuits generally have poor common mode performance. Another source of input stage distortion is input impedance nonlinearity. Since the input impedance of an amplifier can vary depending on the input voltage, and the signal at the amplifier input will be more strongly affected by input impedance if the source impedance is high, distortion will generally increase as the source impedance increases. Again, this problem will typically be significant only when the amplifier is a simple discrete design, and is not generally troublesome with good op amp designs.

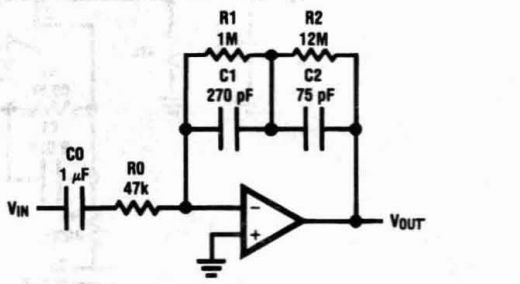
The disadvantages of the circuit configuration of *Figure 2(a)* have led some designers to consider the use of RIAA preamplifiers based on the inverting topology shown in *Figure 2(b)*. This circuit can accurately follow the standard RIAA response curve since the absolute value of its gain can be less than unity. The reduced level of ultrasonic information at its output will sometimes result in lower perceived distortion (depending on the design of the other components in the audio system). Since there is no voltage swing at the preamplifier input, distortion will be lower in cases where the gain block has poor common-mode performance. (The common-mode distortion of the LM833 is low enough that it exhibits essentially the same THD figures whether it is used in the inverting or the non-inverting mode.)

The primary handicap of the inverting configuration is its noise performance. The 47k resistor in series with the source adds at least 4 μV of noise (20 Hz to 20 kHz) to the preamplifier's input. In addition to 4 μV of thermal noise from the 47k resistor, the high impedance in series with the preamp input will generally result in a noise increase due to the preamplifier's input noise current, especially when the series impedance is made even larger by a moving magnet cartridge at resonance. In contrast, the 47k damping resistor in *Figure 2(a)* is in parallel with the source, and is a significant noise contributor only when the source impedance is high. This will occur near resonance, when the source is a moving magnet cartridge. Since the step-up devices used with moving coil cartridges present a low, primarily resistive source impedance to the preamplifier input, the effects of cartridge resonance and input noise current are virtually eliminated for moving coil sources. Therefore, the circuit of *Figure 2(a)* has a noise advantage of about 16 dB with a moving coil source, and from about 13 dB to about 18 dB (depending on the source impedance and on the input noise current of the amplifier) with a moving magnet source. Using the component values shown, the circuit in *Figure 2(a)* follows the RIAA characteristic with an accuracy of better than 0.5 dB (20–20 kHz) and has an input-referred noise voltage equal to 0.33 μV over the Audio frequency range.

Even better performance can be obtained by using the two-amplifier approach of *Figure 3*. The first operational amplifier takes care of the 50 Hz and 500 Hz breakpoints, while the 2122 Hz rolloff is accomplished by the passive network R_3, R_6, and C_3. The second amplifier supplies additional gain—10 dB in this example. Using two amplifiers results in accurate conformance to the RIAA curve without reverting to the noisy inverting topology, as well as lower distortion due to the fact that each amplifier is operating at a lower gain than would be the case in a single-amplifier design. Also, the amplifiers are not required to drive capacitive feedback networks with the full preamplifier output voltages, fur-



(a)



(b)

FIGURE 2. Two typical operational amplifier-based phonograph preamplifier circuits. (a) Non-inverting. (b) Inverting.

ther reducing distortion compared to the single-amplifier designs.

The design equations for the preamplifier are:

1) $R_1 = 8.058\ R_0A_1$, where A_1 is the 1 kHz voltage gain of the first amplifier.

2) $C_1 = \dfrac{3.18 \times 10^{-3}}{R_1}$

3) $R_2 = \dfrac{R_1}{9} - R_0$

4) $C_3 = 7.5 \times 10^{-5} \dfrac{(R_3 + R_6)}{R_3R_6} = \dfrac{7.5 \times 10^{-5}}{R_P}$

5) $C_4 = \dfrac{1}{2\pi f_L (R_3 + R_6)}$

where f_L is the low-frequency −3 dB corner of the second stage. For standard RIAA preamplifiers, f_L should be kept well below the audible frequency range. If the preamplifier is to follow the IEC recommendation (IEC Publication 98, Amendment #4), f_L should equal 20.2 Hz.

6) $A_{V2} = 1 + \dfrac{R_5}{R_4}$

where A_{V2} is the voltage gain of the second amplifier.

7) $C_0 \approx \dfrac{1}{2\pi f_0 R_0}$

where f_0 is the low-frequency −3 dB corner of the first amplifier. This should be kept well below the audible frequency range.

A design procedure is shown below with an illustrative example using 1% tolerance E96 components for close conformance to the ideal RIAA curve. Since 1% tolerance capacitors are often difficult to find except in 5% or 10% standard values, the design procedure calls for re-calculation of a few component values so that standard capacitor values can be used.

RIAA PHONO PREAMPLIFIER DESIGN PROCEDURE

1) Choose R_0. R_0 should be small for minimum noise contribution, but not so small that the feedback network excessively loads the amplifier.

Example: Choose $R_0 = 500$.

2) Choose 1 kHz gain, A_{V1} of first amplifier. This will typically be around 20 dB to 30 dB.

Example: Choose $A_{V1} = 26$ dB $= 20$.

3) Calculate $R_1 = 8.058R_0A_{V1}$

Example: $R_1 = 8.058 \times 500 \times 20 = 80.58$k.

4) Calculate $C_1 = \dfrac{3.18 \times 10^{-3}}{R_1}$

Example: $C_1 = \dfrac{3.18 \times 10^{-3}}{8.058 \times 10^4} = 0.03946\ \mu F$

5) If C_1 is not a convenient value, choose the nearest convenient value and calculate a new R_1 from

$$R_1 = \frac{3.18 \times 10^{-3}}{C_1}$$

Example: New $C_1 = 0.039\ \mu F$.

$$\text{New } R_1 = \frac{3.18 \times 10^{-3}}{3.9 \times 10^{-8}} = 81.54k$$

Use $R_1 = 80.6$k.

6) Calculate a new value for R_0 from $R_0 = \dfrac{R_1}{8.058A_{V1}}$

Example: New $R_0 = \dfrac{8.06 \times 10^4}{8.058 \times 20} = 498.8$.

Use $R_0 = 499$.

7) Calculate $R_2 = \dfrac{R_1}{9} - R_0$

Example: $R_2 = \dfrac{8.06 \times 10^4}{9} - 499 = 8456.56$

Use 8.45k.

8) Choose a convenient value for C_3 in the range from 0.01 μF to 0.05 μF.

Example: $C_3 = 0.033\ \mu F$.

9) Calculate $R_P = \dfrac{7.5 \times 10^{-5}}{C_3}$

Example: $R_P = \dfrac{7.5 \times 10^{-5}}{3.3 \times 10^{-8}} = 2.273$k.

10) Choose a standard value for R_3 that is slightly larger than R_P.

Example: $R_3 = 2.37$k.

11) Calculate R_6 from $1/R_6 = 1/R_P - 1/R_3$

Example: $R_6 = 55.36$k

Use 54.9k.

12) Calculate C_4 for low-frequency rolloff below 1 Hz from design equation (5).

Example: $C_4 = 2\ \mu F$. Use a good quality mylar, polystyrene, or polypropylene.

13) Choose gain of second amplifier.

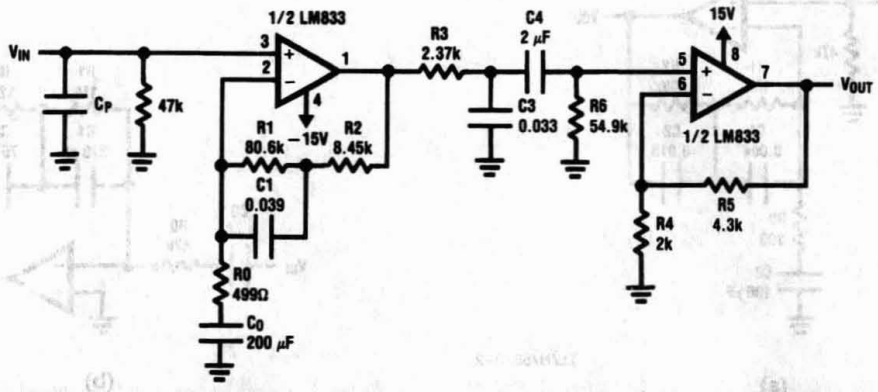


FIGURE 3. Two-amplifier RIAA phono preamplifier with very accurate RIAA response.

Example: The 1 kHz gain up to the input of the second amplifier is about 26 dB for this example. For an overall 1 kHz gain equal to about 36 dB we choose:
A_{V2} = 10 dB = 3.16.

14) Choose value for R_4.

Example: R_4 = 2k.

15) Calculate $R_5 = (A_{V2} - 1) R_4$

Example: R_5 = 4.32k.

Use R_5 = 4.3k

16) Calculate C_0 for low-frequency rolloff below 1 Hz from design equation (7).

Example: C_0 = 200 μF.

The circuit of *Figure 3* has excellent performance: Conformance to the RIAA curve is within 0.1 dB from 20 Hz to 20 kHz, as illustrated in *Figure 4* below for a prototype version of the circuit. THD and noise data are reproduced in *Figure 5* and Table II, respectively. If a "perfect" cartridge with 1mV/cm/s sensitivity (higher than average) is used as the input to this preamplifier, the highest recorded groove velocities available on discs (limited by the cutting equipment) will fall below the 1V curve except in the 1 kHz to 10 kHz region, where isolated occurances of 2V to 3V levels can be generated by one or two of the "superdiscs". (See reference 4). The distortion levels at those frequencies and signal levels are essentially the same as those shown on the 1V curve, so they are not reproduced separately here. It should be noted that most real cartridges are very limited in their ability to track such large velocities, and will not generate preamplifier output levels above 1Vrms even under high groove velocity conditions.

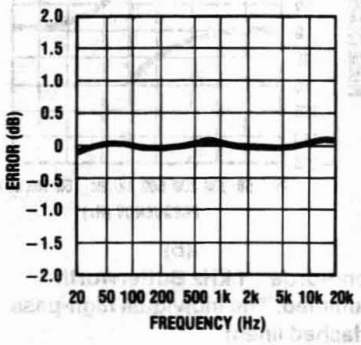


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FIGURE 4. Deviation from ideal RIAA response for circuit of *Figure 3* using 1% resistors. The maximum observed error for the prototype was 0.1 dB.

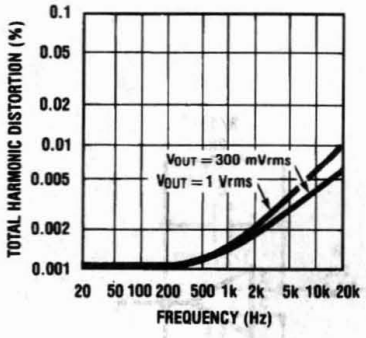

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FIGURE 5. THD of circuit in *Figure 3* as a function of frequency. The lower curve is for an output level of 300mVrms and the upper curve is for an output level of 1Vrms.

Table II. Equivalent input noise and signal-to-noise ratio for RIAA preamplifier circuit of *Figure 3*. Noise levels are referred to gain at 1 kHz.

NOISE WEIGHTING	CCIR/ARM	"A"	FLAT
Noise voltage	0.26 μV	0.23 μV	0.37 μV
S/N referred to 5 mV input at 1 kHz	86 dB	87 dB	82 dB

II. ACTIVE CROSSOVER NETWORK FOR LOUDSPEAKERS

A typical multi-driver loudspeaker system will contain two or more transducers that are intended to handle different parts of the audio frequency spectrum. Passive filters are usually used to split the output of a power amplifier into signals that are within the usable frequency range of the individual drivers. Since passive crossover networks must drive loudspeaker elements whose impedances are quite low, the capacitors and inductors in the crossovers must be large in value, meaning that they will very likely be expensive and physically large. If the capacitors are electrolytic types or if the inductors do not have air cores, they can also be significant sources of distortion. Futhermore, many desirable filter characteristics are either impossible to realize with passive circuitry, or require so much attenuation to achieve passively that system efficiency is severely reduced.

An alternative approach is to use low-level filters to divide the frequency spectrum, and to follow each of these with a separate power amplifier for each driver or group of drivers. A two-way (or "bi-amped") system of this type is shown in *Figure 6*. This basic concept can be expanded to any number of frequency bands. For accurate sound reproduction, the sum of the filter outputs should be equal to the crossover input (if the transducers are "ideal"). While this seems to be an obvious requirement, it is very difficult to find a commercial active dividing network that meets it. Consider an active crossover consisting of a pair of 2nd-order Butterworth filters, (one is a low-pass; the other is a high-pass). The transfer functions of the filters are of the form:

$$\frac{V_L(s)}{V_{in}(s)} = \frac{1}{s^2 + \sqrt{2}s + 1}$$

$$\frac{V_H(s)}{V_{in}(s)} = \frac{s^2}{s^2 + \sqrt{2}s + 1}$$

and their sum is:

$$\frac{V_L(s)}{V_{in}(s)} + \frac{V_H(s)}{V_{in}(s)} = \frac{1 + s^2}{s^2 + \sqrt{2}s + 1}$$

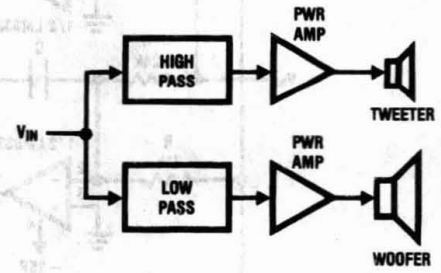

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FIGURE 6. Block diagram of a two-way loudspeaker system using a low level crossover network ahead of the power amplifiers.

The output will therefore never exactly equal the input signal (except in the trivial case of a DC input). *Figure 7* shows the response of this crossover to a square wave input, and the amplitude and phase response of the crossover to sinusoidal steady state inputs can be seen in *Figure 8*. Higher-order filters will yield similarly dissatisfying results when this approach is used.

A significant improvement can be made by the use of a constant voltage crossover like the one shown in *Figure 9*. The term "constant voltage" means that the outputs of the high-pass and low-pass sections add up to produce an exact replica of the input signal. The rolloff rate is 12 dB/octave. The input impedance is equal to R/2, or 12 kΩ in the circuit of *Figure 9*. The LM833 is especially well-suited for active filter applications because of its high gain-bandwidth product. The transfer functions of this crossover network are of the form

$$\frac{V_L(s)}{V_{in}(s)} = \frac{a_1 s + 1}{a_3 s^3 + a_2 s^2 + a_1 s + 1}$$

and

$$\frac{V_H(s)}{V_{in}(s)} = \frac{a_3 s^3 + a_2 s^2}{a_3 s^3 + a_2 s^2 + a_1 s + 1}$$

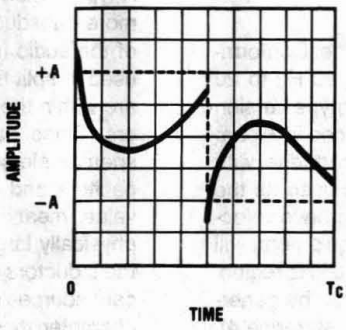

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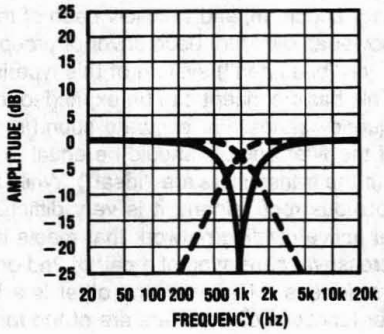
FIGURE 7. Response of second-order Butterworth crossover network (high-pass and low-pass outputs summed) to a square wave input (dashed line) at the crossover frequency. Period is $T_C = 1/f_C$.



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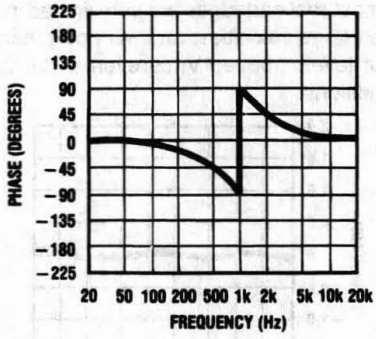
(a)



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(b)

FIGURE 8. Magnitude (a) and phase (b) response of a second-order, 1 kHz Butterworth crossover network with the high-pass and low-pass outputs summed. The individual high-pass and low-pass outputs are superimposed (dashed lines).

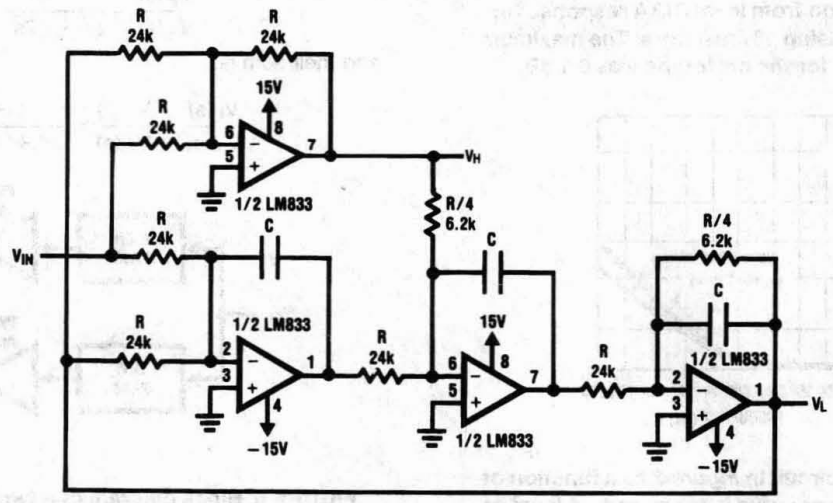

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FIGURE 9. Constant-voltage crossover network with 12 dB/octave slopes.

The crossover frequency is equal to $\frac{1}{2\pi RC}$.

The low-pass and high-pass constant voltage crossover outputs are plotted in *Figure 10.* The square-wave response (not shown) of the summed outputs is simply an inverted square-wave, and the phase shift (also not shown) is essentially 0° to beyond 20 kHz.

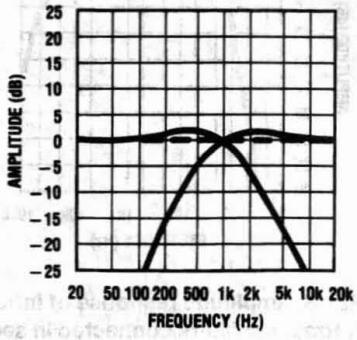

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FIGURE 10. Low-pass and high-pass responses of constant-voltage crossover network in *Figure 9* with crossover frequency of 1 kHz. For the circuit of *Figure 9*, $a_1 = 4$, $a_2 = 4$, and $a_3 = 1$. Note that the summed response (dashed lines) is perfectly flat.

It is important to remember that even a constant voltage crossover transfer function does not guarantee an ideal overall system response, because the transfer functions of the transducers will also affect the overall response. This can be minimized to some extent by using drivers that are "flat" at least two octaves beyond the crossover frequency.

III. INFRASONIC AND ULTRASONIC FILTERS

In order to ensure "perfectly flat" amplitude response from 20 Hz to 20 kHz, many audio circuits are designed to have bandwidths extending far beyond the audio frequency range. There are many high-fidelity systems, however, that can be audibly improved by reducing the gain at frequencies above and below the limits of audibility.

The phonograph arm/cartridge/disc combination is the most significant source of unwanted low-frequency information. Disc warps on 33⅓ rpm records can cause large-amplitude signals at harmonics of 0.556 Hz. Other large low-frequency signals can be created at the resonance frequency determined by the compliance of the pickup cartridge and the effective mass of the cartridge/arm combination. The magnitude of undesireable low-frequency signals can be especially large if the cartridge/arm resonance occurs

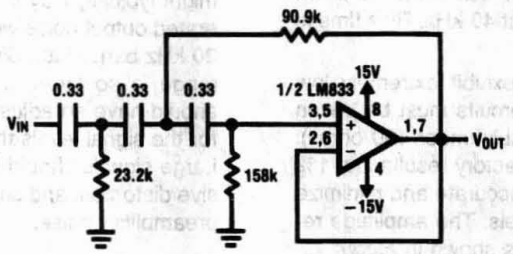

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FIGURE 11. Filter for rejection of undersireable infrasonic signals. Filter characteristic is third-order Butterworth with −3 dB frequency at 15 Hz. Resistor and capacitor values shown are for 1% tolerance components. 5% tolerance units can be substituted in less critical applications.

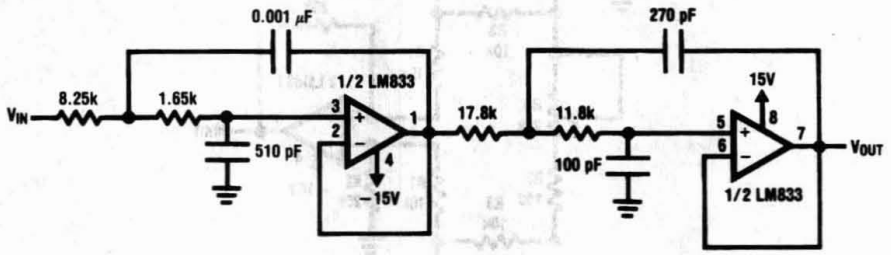

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FIGURE 12. Ultrasonic rejection filter with fourth-order Bessel low-pass characteristic. The filter gain is down 3 dB at about 40 kHz. As with the infrasonic filter, 1% tolerance components should be used for accurate response.

at a warp frequency. Infrasonic signals can sometimes overload amplifiers, and even in the absence of amplifier overload can cause large woofer excursions, resulting in audible distortion and even woofer damage.

Ultrasonic signals tend to cause problems in power amplifiers when the amplifiers exhibit distortion mechanisms due to slew rate limitations and other high frequency nonlinearities. The most troublesome high-frequency signals come principally from moving-coil cartridges and sometimes from tape recorders if their bias oscillator outputs manage to get into the audio signal path. Like the infrasonic signals, ultrasonic signals can place distortion products in the audio band even though the offending signals themselves are not audible.

The circuits in *Figures 11* and *12* attenuate out-of-band signals while having minimal effect on the audio program. The infrasonic filter in *Figure 11* is a third-order Butterworth high-pass with its −3 dB frequency at 15 Hz. The attenuation at 5 Hz is over 28 dB, while 20 Hz information is reduced by only 0.7 dB and 30 Hz information by under 0.1 dB.

The ultrasonic filter in *Figure 12* is a fourth-order Bessel alignment, giving excellent phase characteristics. A Bessel filter approximates a delay line within its passband, so complex in-band signals are passed through the filter with negligible alteration of the phase relationships among the various in-band signal frequencies. The circuit shown is down 0.65 dB at 20 kHz and −3 dB at about 40 kHz. Rise time is limited to about 8.5 μSec.

The high-pass and low-pass filters exhibit extremely low THD, typically under 0.002%. Both circuits must be driven from low impedance sources (preferably under 100 ohms). 5% components will often yield satisfactory results, but 1% values will keep the filter responses accurate and minimize mismatching between the two channels. The amplitude response of the two filters in cascade is shown in *Figure 13*. When the two filters are cascaded, the low-pass should precede the high-pass.

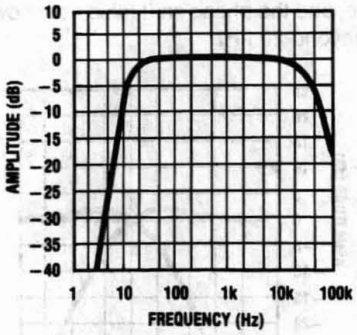

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FIGURE 13. Amplitude response of infrasonic and ultrasonic filters connected in series.

IV. TRANSFORMERLESS MICROPHONE PREAMPLIFIERS

Microphones used in professional applications encounter an extremely wide dynamic range of input sound pressure levels, ranging from about 30 dB SPL (ambient noise in a quiet room) to over 130 dB SPL. The output voltage of a low impedance (200 ohm) microphone over this range of SPLs might typically vary from 20 μV to 2V rms, while its self-generated output noise would be on the order of 0.25 μV over a 20 kHz bandwidth. Since the microphone's output dynamic range is so large, a preamplifier for microphone signals should have an adjustable gain so that it can be optimized for the signal levels that will be present in a given situation. Large signals should be handled without clipping or excessive distortion, and small signals should not be degraded by preamplifier noise.

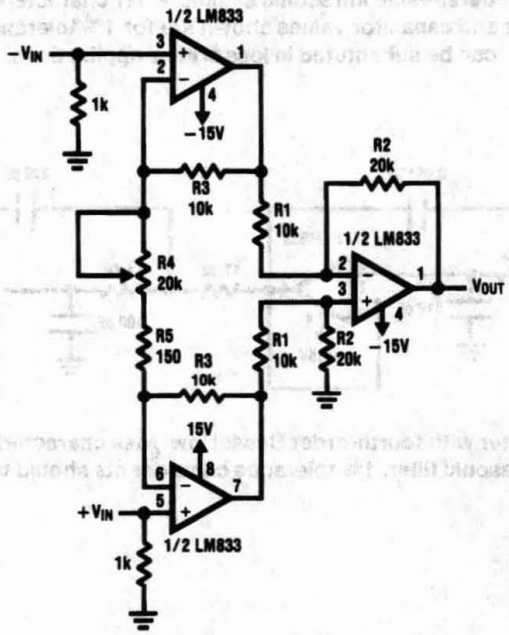

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FIGURE 14. Simple transformerless microphone preamplifier using LM833. R_1, R_2, and R_3 are 0.1% tolerance units (or R_2 can be trimmed).

For a conservative low noise design, the preamplifier should contribute no more noise to the output signal than does the resistive portion of the source impedance. In practical applications, it is often reasonable to allow a higher level of input noise in the preamplifier since ambient room noise will usually cause a noise voltage at the microphone output terminals that is on the order of 30 dB greater than the microphone's intrinsic (due to source resistance) noise floor.

When long cables are used with a microphone, its output signal is susceptable to contamination by external magnetic fields—especially power line hum. To minimize this problem, the outputs of most professional microphones are balanced, driving a pair of twisted wires with signals of opposite polarity. Ideally, magnetic fields will induce equal voltages on each of the two wires, which can then be cancelled if the signals are applied to a transformer or differential amplifier at the preamplifier input.

The circuits in *Figures 14* and *15* are transformerless differential input microphone preamplifiers. Avoiding transformers has several advantages, including lower cost, smaller physical size, and reduced distortion. The circuit of *Figure 14* is the simpler of the two, with two LM833s amplifying the input signal before the common-mode noise is cancelled in the differential amplifier. The equivalent input noise is about 760 nV over a 20 Hz to 20 kHz frequency band (−122 dB referred to 1V), which is over 26 dB lower than a typical microphone's output from the 30 dB SPL ambient noise level in a quiet room. THD is under .01% at maximum gain, and .002% at minimum gain. For more critical applications with lower sensitivity microphones, the circuit of *Figure 15* uses LM394s as input devices for the LM833 gain stages. The equivalent input noise of this circuit is about 2.4 nv/$\sqrt{\text{Hz}}$, at maximum gain, resulting in a 20 Hz to 20 kHz input noise level of 340 nV, or −129 dB referred to 1V.

In both circuits, potentiometer R_4 is used to adjust the circuit gain from about 4 to 270. The maximum gain will be limited by the minimum resistance of the potentiometer. If R_1, R_2, and R_3 are all 0.1% tolerance units, the rejection of hum and other common-mode noise will typically be about 60 dB, and about 44 dB worst case. If better common-mode rejection is needed, one of the R_2s can be replaced by an 18k resistor and a 5k potentiometer to allow trimming of CMRR. To prevent radio-frequency interference from getting into the preamplifier inputs, it may be helpful to place 470 pF capacitors between the inputs and ground.

References:

1) S. P. Lipshitz, J. Audio Eng. Soc., "On RIAA Equalization Networks", June 1979.

2) P. J. Baxandall, J. Audio Eng. Soc., Letter, pp47–52, Jan 1981.

3) Ashley and Kaminsky, J. Audio Eng. Soc., "Active and Passive Filters as Loudspeaker Crossover Networks", June 1971.

4) T. Holman, Audio, "Dynamic Range Requirements of Phonographic Preamplifiers", July 1977.

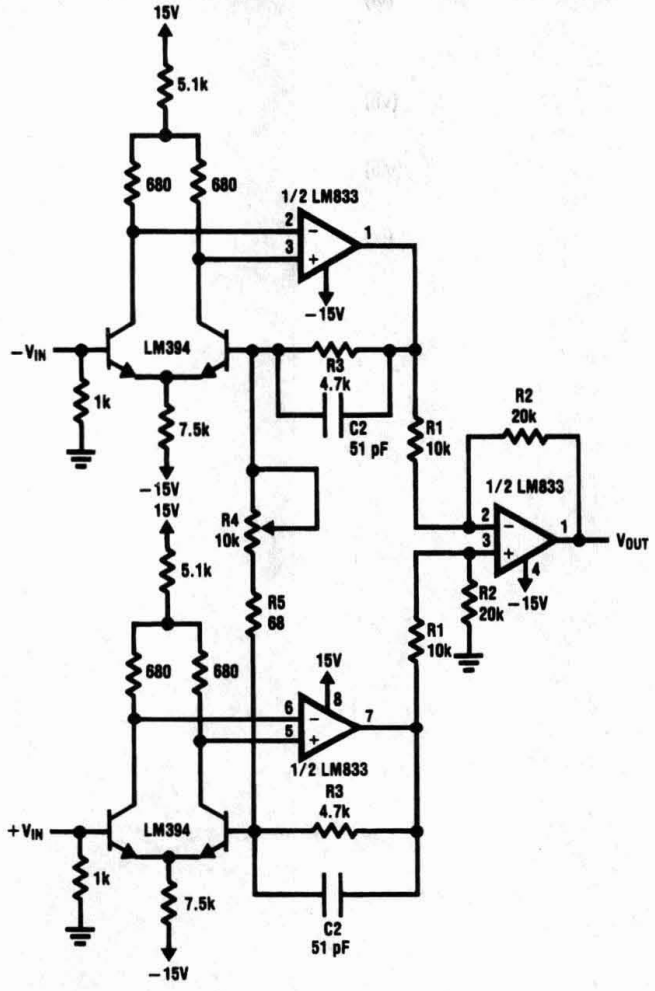

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FIGURE 15. Transformerless microphone preamplifier similar to that of *Figure 14*, but using LM394s as low-noise input stages.

APPENDIX I: DERIVATION OF RIAA PHONO PREAMPLIFIER DESIGN EQUATIONS (1), (2), AND (3).

The first three design equations on the third page are derived here. The derivations of the others should be apparent by observation. The purpose of the preamplifier's first stage is to produce the transfer function:

$$A_V(s) = A_V(dc)\frac{(3.18\times10^{-4}+1)}{(3.18\times10^{-3}+1)} \quad \text{(i)}$$

where $A_V(dc)$ is the dc gain of the first stage.

The actual first stage transfer function is (ignoring C_0):

$$A_V(s) = \frac{sC_1(R_0R_1+R_1R_2)+R_0+R_1+R_2}{sC_1R_0R_1+R_0}$$

$$= \left[\frac{R_0+R_1+R_2}{R_0}\right]\left[\frac{sC_1\dfrac{(R_0R_1+R_1R_2)}{R_0+R_1+R_2}+1}{sC_1R_1+1}\right] \quad \text{(ii)}$$

Equating terms, we have:

$$\frac{C_1(R_0R_1+R_1R_2)}{R_0+R_1+R_2} = 3.18\times10^{-4} \quad \text{(iii)}$$

$$C_1R_1 = 3.18\times10^{-3} \quad \text{(iv)}$$

$$A_V(dc) = \frac{R_0+R_1+R_2}{R_0} \quad \text{(v)}$$

Note that (iv) is quivalent to (2) on page three.

From (iii) and (iv) we have:

$$\frac{C_1R_1(R_0+R_2)}{R_0+R_1+R_2} = \frac{C_1R_1}{10} \quad \text{(vi)}$$

Therefore:

$$\frac{R_0+R_1+R_2}{R_0+R_2} = 10 \quad \text{(vii)}$$

$$\frac{R_1}{R_0+R_2} = 9 \quad \text{(viii)}$$

$$\text{and } R_2 = \frac{R_1}{9} - R_0 \quad \text{(ix)}$$

(ix) is equivalent to design equation (3) on page three.

Combining (v) and (ix),

$$A_V(dc) = \frac{R_0+R_1+R_2}{R_0} = \frac{R_1(1+1/9)}{R_0} \quad \text{(x)}$$

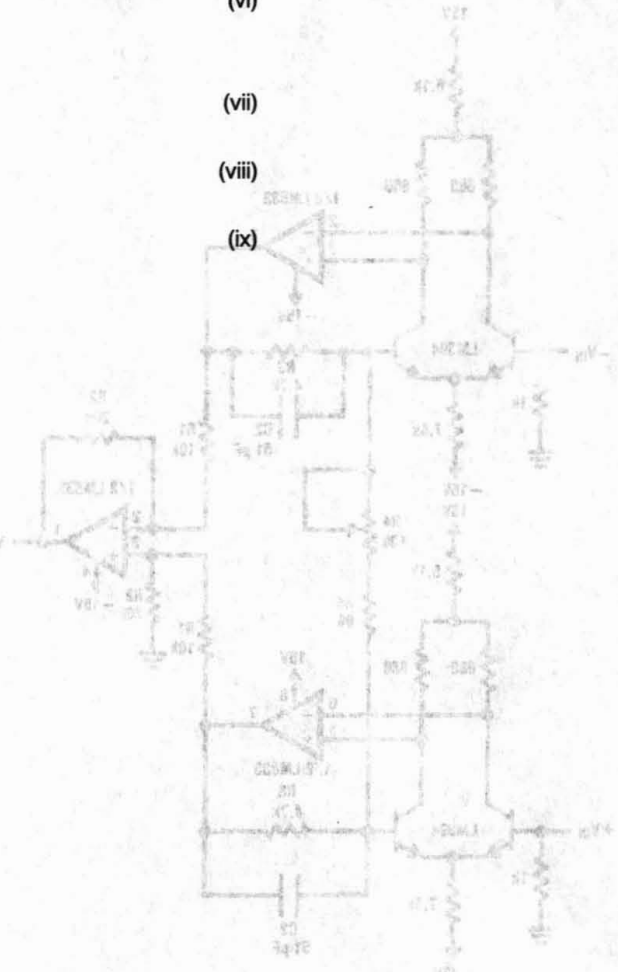
Finally, solving for R_1 and using $A_V(dc) = 8.9535A_V$ (1 kHz) yields:

$$R_1 = \frac{R_0A_V(dc)}{10/9} = 0.9R_0A_V(dc) = 8.058A_V\ (1\ kHz)\ R_0, \quad \text{(xi)}$$

which is equivalent to (1) on page three.

APPENDIX II: STANDARD E96 (1%) RESISTOR VALUES

Standard Resistor Values (E-96 Series)							
10.0	13.3	17.8	23.7	31.6	42.2	56.2	75.0
10.2	13.7	18.2	24.3	32.4	43.2	57.6	76.8
10.5	14.0	18.7	24.9	33.2	44.2	59.0	78.7
10.7	14.3	19.1	25.5	34.0	45.3	60.4	80.6
11.0	14.7	19.6	26.1	34.8	46.4	61.9	82.5
11.3	15.0	20.0	26.7	35.7	47.5	63.4	84.5
11.5	15.4	20.5	27.4	36.5	48.7	64.9	86.6
11.8	15.8	21.0	28.0	37.4	49.9	66.5	88.7
12.1	16.2	21.5	28.7	38.3	51.1	68.1	90.9
12.4	16.5	22.1	29.4	39.2	52.3	69.8	93.1
12.7	16.9	22.6	30.1	40.2	53.6	71.5	95.3
13.0	17.4	23.2	30.9	41.2	54.9	73.2	97.6



Audio Noise Reduction and Masking

National Semiconductor
Application Note 384
Martin Giles

INTRODUCTION

Audio noise reduction systems can be divided into two basic approaches. The first is the complementary type which involves compressing the audio signal in some well-defined manner before it is recorded (primarily on tape). On playback, the subsequent complementary expansion of the audio signal which restores the original dynamic range, at the same time has the effect of pushing the reproduced tape noise (added during recording) farther below the peak signal level—and hopefully below the threshold of hearing.

The second approach is the single-ended or non-complementary type which utilizes techniques to reduce the noise level already present in the source material—in essence a playback only noise reduction system. This approach is used by the LM1894 integrated circuit, designed specifically for the reduction of audible noise in virtually any audio source.

While either type of system is capable of producing a significant reduction in audible noise levels, compandors are inherently capable of the largest reduction and, as a result, have found the most favor in studio based equipment. This would appear to give compandors a distinct edge when it comes to translating noise reduction systems from the studio or lab to the consumer marketplace. Compandors are not, unfortunately, a complete solution to the audio noise problem. If we summarize the major desirable attributes of a noise reduction system we will come up with at least eight distinct things that the system must do—and no system as yet does all of them perfectly.

1) The reproduced signal (now free of noise) is audibly identical to the original signal in terms of frequency response, transient response and program dynamics. The stereo image is stable and does not wander.
2) Overload characteristics of the system are well above the normal peak signal level.
3) The system electronics do not produce additional noise (including perturbations produced by the control signal path).
4) Proper response of the system does not depend on phase/frequency or gain accuracy of the transmission medium.
5) System operation does not cause audible modulation of the noise level.
6) The system enables the full dynamic range of the source to be utilized without distortion.
7) The recorded signal sounds natural on playback—even when decoding is not used. This means that the system is compatible with existing equipment.
8) Finally, the system is universal and can be used with any medium; disc, FM broadcast, television broadcast, audio and video tapes.

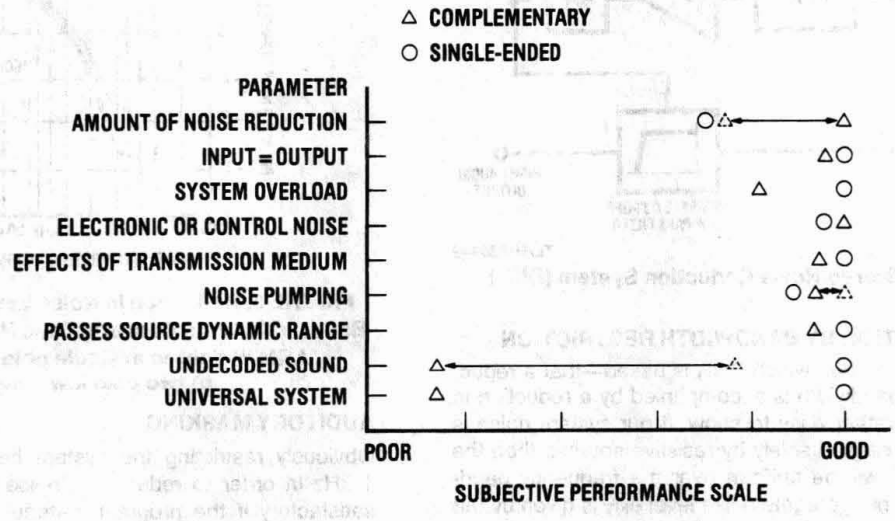


FIGURE 1. Comparison of Noise Reduction Systems

Although no system presently meets all these requirements—and the performance level they do reach is often judged subjectively—they provide a useful set of performance standards by which to judge the n.r. systems that are available. In particular, in the consumer field items 7) and 8) are significant. The most popular n.r. system, Dolby B Type, got that way in part because pre-recorded and encoded tapes could be played back on tape-decks that did not have Dolby B decoders (Dolby B uses a relatively small amount of compression and that only for low level higher frequency signals). Similarly, DNR™, which uses the LM1894, is gaining in popularity because it does not require any encoding and, in addition, can work with any audio source, including Dolby B encoded tapes.

DNR is a non-complementary noise reduction system which can give up to 14 dB noise reduction in stereo program material. The operation of the LM1894 is dependent on two principles; that the audible noise is proportional to the system bandwidth—decreasing the bandwidth decreases the noise—and that the desired signal is capable of "masking" the noise when the signal to noise ratio is sufficiently high. DNR automatically and continuously changes the system bandwidth in response to the amplitude and frequency content of the program. Restricting the bandwidth to less than 1 kHz reduces the audible noise by up to 14 dB (weighted) and a special spectral weighting filter in the control path ensures that the bandwidth is always increased sufficiently to pass any music that may be present. Because of this ability to analyze the auditory masking qualities of the program material, DNR does not require the source to be encoded in any special way for noise reduction to be obtained.

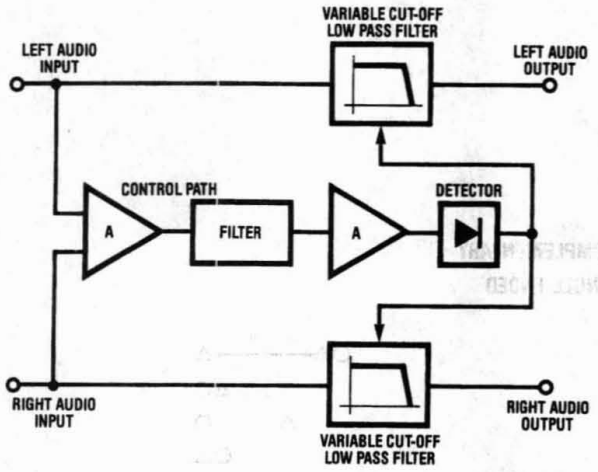


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FIGURE 2. Stereo Noise Reduction System (DNR)

NOISE REDUCTION BY BANDWIDTH RESTRICTION

The first principle upon which DNR is based—that a reduction in system bandwidth is accompanied by a reduction in noise level—is rather easy to show. If our system noise is assumed to be caused solely by resistive sources then the noise amplitude will be uniform over the frequency bandwidth. The total or aggregate noise level $\overline{e_{NT}}$ is given by the familiar formula

$$\overline{e_{NT}} = \sqrt{4\,KTBR} \qquad (1)$$

where K = Boltzmanns cons't
T = absolute temp.
B = bandwidth
R = source resistance

At any single frequency, the noise amplitude measured in a bandwidth of 1 Hz is $\overline{e_n}$, and therefore

$$\overline{e_{NT}} = \overline{e_n}\sqrt{B} \qquad (2)$$

This shows that the total noise, and hence the S/N ratio, is directly proportional to the square root of the system bandwidth. For example, if the system bandwidth is changed from 30 kHz to 1 kHz, the aggregate S/N ratio changes by

$$20\log_{10}\sqrt{1\times10^3} - 20\log_{10}\sqrt{30\times10^3} = -14.8\ \text{dB}$$

This result, although mathematically correct, is not exactly what will occur in practice for several reasons. Most audio systems will have a generally smooth noise spectrum similar to white noise, but the amplitude is not necessarily uniform with frequency. In audio cassette systems where the dominant noise source is the tape itself, the frequency response often falls off rapidly beyond 12 kHz anyway. For video tapes with very slow longitudinal audio tracks, the frequency response is well below 10 kHz, depending on the recording mode. Disc noise generally increases towards the low frequency end of the audio spectrum whereas FM broadcast noise decreases below 2 kHz. On the other hand, the frequency range of the noise spectrum is not always indicative of its obtrusiveness. The human ear is most sensitive to noise in the frequency range from 800 Hz to just above 8 kHz. Because of this, a weighting filter inserted into the measurement system which gives emphasis to this frequency range, produces better correlation between the S/N "number" and the subjective impression of noise audibility. Generally speaking, a typical tape noise spectrum and a weighting filter such as CCIR/ARM will yield noise reduction numbers between 10–14 dB when a single pole low pass filter is used to restrict the audio bandwidth to less than 1 kHz. Up to 18 dB noise reduction is possible with a two pole low pass filter. Consistent with the many reported experiments on ear sensitivity (Fletcher-Munson, Robinson-Dadson etc.) we see that decreasing the bandwidth below 800 Hz is not particularly beneficial, and that once the bandwidth is above 8 kHz, there is little perceived increase in the audible noise level.

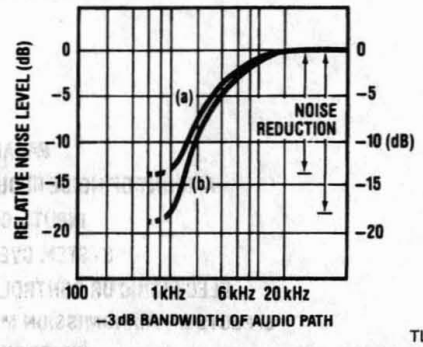

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FIGURE 3. Reduction in Noise Level with Decreasing Bandwidth Audio Cassette Tape Noise Source—CCIR/ARM Weighted a) single pole low pass filter; b) two pole low pass filter

AUDITORY MASKING

Obviously restricting the system bandwidth to less than 1 kHz in order to reduce the noise level will not be very satisfactory if the program material is similarly restricted, and this is where the second operating principle of DNR comes into play—whenever a sound is being heard it reduces the ability of the listener to hear another sound. This is known as auditory masking and is not a newly discovered phenomenon. It has been investigated for many years, primarily in connection with noise masking the ability of the listener to hear tones. The measurements have been made

under steady state conditions and are summarized in the curves of *Figure 4.* Before discussing the shape of the curves and the conclusions that can be drawn it is worth looking at the scales employed. One difficulty that occurs in evaluating electronic equipment for audio is to be able to relate a quantity measured in electrical terms to the subjective stimulus (hearing) that it produces. For audio we are most interested in the conversion of electrical power into acoustic power. Since neither sound power nor sound intensity can be measured directly, we must use a related quantity known as sound pressure level (SPL) as our reference scale in *Figure 4.* The reference sound pressure, which approximates the threshold of hearing at 1 kHz is 0.0002 μBars (10^6 μBars = 1 Bar = 1 atmosphere). For this sound pressure scale, the level at which noise spectra will appear depends on the degree of amplification we are giving the desired signal to produce the maximum anticipated sound pressure. Typically a maximum preferred listening level is +90 dB (SPL) and the assumption is made that the total audio system, including speakers, is producing this SPL at the listener's ear when the recorded level (on tape, for example) corresponds to OVU. By comparing the amplitude of noise spectra with this OVU level signal we obtain the tape noise curves of *Figure 4* and can compare them with the audible noise threshold. Increasing the volume level by 10 dB (say), to compensate for a lower recording level will raise all the *noise spectra curves* by 10 dB. The audible noise threshold curve *does not change* with changes in SPL produced by twiddling the volume control (except after prolonged listening at high levels) since it depends on the characteristics of the ear and partly upon the masking effects of room noise.

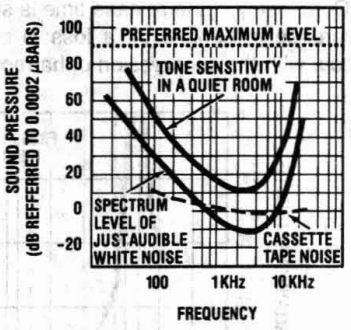

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FIGURE 4. Relating the Spectral Sensitivity of the Ear to Tones and Audible Noise with the Noise Output Level from an Electric Source

The upper solid curve in *Figure 3* shows the sensitivity of the ear to pure tones in a typical room environment. Notice that tones at very low frequencies and at very high frequencies must be much louder than tones at mid-frequencies in order to be heard. The lower solid curve shows the spectrum level of just audible white noise. This curve is some 20 dB–30 dB below the tone spectrum because, unlike a single tone, noise has spectral components at all frequencies. Noise spectra at frequencies either side of a specific frequency contribute to the auditory sensation and thus can be heard at a lower threshold level. The two curves also imply that noise at or above the lower curve is able to completely mask single tones on the upper curve. Also sources with noise spectra above the lower curve are going to be audible. Clearly for cassette tapes we need to push the noise level down by another 10 dB if it is to be inaudible at preferred listening levels. If the tape is under-recorded and the volume level increased to compensate, yet more noise reduction is needed.

Reversing these conclusions to determine the ability of tones to mask the noise is not as easy. The hearing mechanism in the ear involves the basilar membrane which is approximately 30 mm long by 0.5 mm wide. The nerve endings giving the sensation of hearing are spaced along this membrane so that the ability to hear at one frequency is not masked at another frequency when the frequencies are well separated. White noise can excite the entire basilar membrane since it has spectral components at all frequencies. For any single frequency therefore, there will be a band of noise spectra capable of simultaneously exciting the nerve endings that are responding to the single frequency—and masking occurs. Conversely, a single tone at the upper curve level is quite incapable of masking noise spectra at the lower curve level snce it can only excite nerve endings at one particular point on the membrane. Noise spectra at frequencies on either side of the tone will still excite different parts of the membrane—and will be heard. Extremely high SPL's are required if single tones are to raise the audible noise threshold level and provide masking. As might be expected, the most effective tone frequencies are near the natural resonance of the ear—between 700 Hz and 1 kHz—and even then SPL's higher than 75 dB are needed for masking noise at 16 dBSPL. Fortunately for n.r. systems in general, including compandors, this applies only to pure tones. As soon as the tone acquires distortion, frequency modulation or transient qualities, or a mixture of tones is present, the masking abilities change dramatically. Typically music and speech, with high energy concentration around 1 kHz, can be regarded as excellent noise masking sources—up to 30 dB more effective than single tones. Therefore, recorded signals at an average level of 40–45 dB SPL will allow a full audio bandwidth to be used without the noise becoming audible. Signal levels lower than this can provide adequate masking, particularly if the source has employed dynamic range compression (FM broadcast for example), but speech and solo musical instruments are likely to betray noise modulation. These conclusions can apply equally to complementary noise reduction systems with the noise modulation effects depending on the degree of compression/expansion and the threshold level at which compression begins in the record chain.

CONTROL PATH FILTERING AND TRANSIENT CHARACTERISTICS

If the signal source always maintained a relatively high SPL, then there wouldn't be any need for an n.r. system. However, when the program material SPL momentarily drops, the noise is unmasked and becomes audible. Much of the design effort involved in n.r. systems is in making the system track the program dynamics so that unmasking does not occur—at least not audibly. Similarly when the program material increases abruptly following a quiet passage, the n.r. system must respond quickly enough that the audio material is not distorted. For DNR, this means that the −3 dB corner frequency of the low pass filters inserted in each audio channel must increase quickly enough to pass all the music yet decrease back to around 1 kHz in the absence of music to reduce the noise. Matching low pass filters are used with a flat response below the cut-off frequency, and a smoothly decreasing response (−6 dB/octave) above the cut-off frequency, which can be varied from 800 Hz to over 30 kHz by the control signal.

A first approach to generating this control signal might be to use a filter and a gain block, driving a peak detector circuit. Since the amplitude spectra of musical instruments falls off with increasing frequency, and the characteristics of the ear

are such that masking is most effective with sounds around 1 kHz, a reasonable filter for the control path might be low pass. This turns out *not* to be the case. To take a worse case situation (from the viewpoint of masking), when a French Horn is the dominant source, most of the energy is at frequencies below 1 kHz. If we were detecting this energy through a low pass filter, the control path would respond to the high amplitude and cause the audio filters to open to full bandwidth. Noise in the 2 kHz and above region would be promptly unmasked and audible. To avoid this, DNR uses a *highpass* filter in the control path. Below 1.6 kHz, the response falls at an 18 dB/octave rate. Above 1.6 kHz the filter response increases at a 12 dB/octave rate until a −3 dB corner frequency around 6 kHz is reached. After this the response is allowed to drop again and may include notches at 15.734 kHz (for television sound), or at 19 kHz to suppress the subcarrier pilot signal in FM stereo broadcasts. Returning to the case of the French Horn, the absence of high amplitude higher frequency harmonics means that the control signal will generate only a small increase in the audio bandwidth (depending on the sound level) and the noise will remain filtered out.

Contrasted with this, multiple instruments, or solo instruments such as the violin or trumpet, can have significant energy levels above 1 kHz which not only provide masking at higher frequencies but also require wider audio bandwidths for fidelity transmission in the audio path. Put another way, when the presence of high frequencies is detected in the control path we know that the audio bandwidth must be increased and that simultaneously large levels of signal energy are present in the critical masking frequency range. Since the harmonic amplitude can decrease rapidly with increase in frequency, the control sensitivity is raised at a 12 dB/octave rate up to 6 kHz to ensure that an adequate audio bandwidth is always maintained.

The attack and release times of the control path signal are also based on typical program dynamics and the characteristics of the human ear. If the detector cannot respond to the leading edge transient in the music, then distortion in the audio path will result from the initial loss of high frequency components. As might be expected, the rise time of any musical selection will depend on the instruments that are being played. An English Horn is capable of reaching 60% of its peak amplitude in 5 ms. For other instruments, rise-times can vary from 50 ms to 200 ms whereas a hand-clap can be as fast as 0.5 ms. With this data in mind, DNR has been designed with an attack time of 0.5 ms. A distinction should be made in the effects of longer attack times for DNR compared to a companding noise reducer. If the compander does not respond immediately to an input transient, then instantaneous overload of the audio path can occur, with an overshoot amplitude as much as the maximum compression capability. If the system does not have adequate headroom, this overshoot can cause audible effects that last for longer than the period of the overshoot. The DNR filters simply cannot produce such an overshoot by failure to respond to the input rise-time. Since the ear has difficulty registering sounds of less than 5 ms duration, and can tolerate severe distortion if it lasts less than 10 ms, DNR has considerable flexibility in the choice of detector attack time.

Attack time is only half the story. Once the detector has responded to a musical transient, it needs to decay back to the quiescent output level at the cessation of the transient. A slow decay time would mean that for a period following the end of the transient, the system audio bandwidth would still be relatively wide. The noise in this bandwidth would be unmasked and a noise "burst" heard at the end of each musical transient. Conversely, if the release time is short to ensure a rapid decrease in bandwidth, a loss in musical "ambience" will occur with the suppression of harmonics at

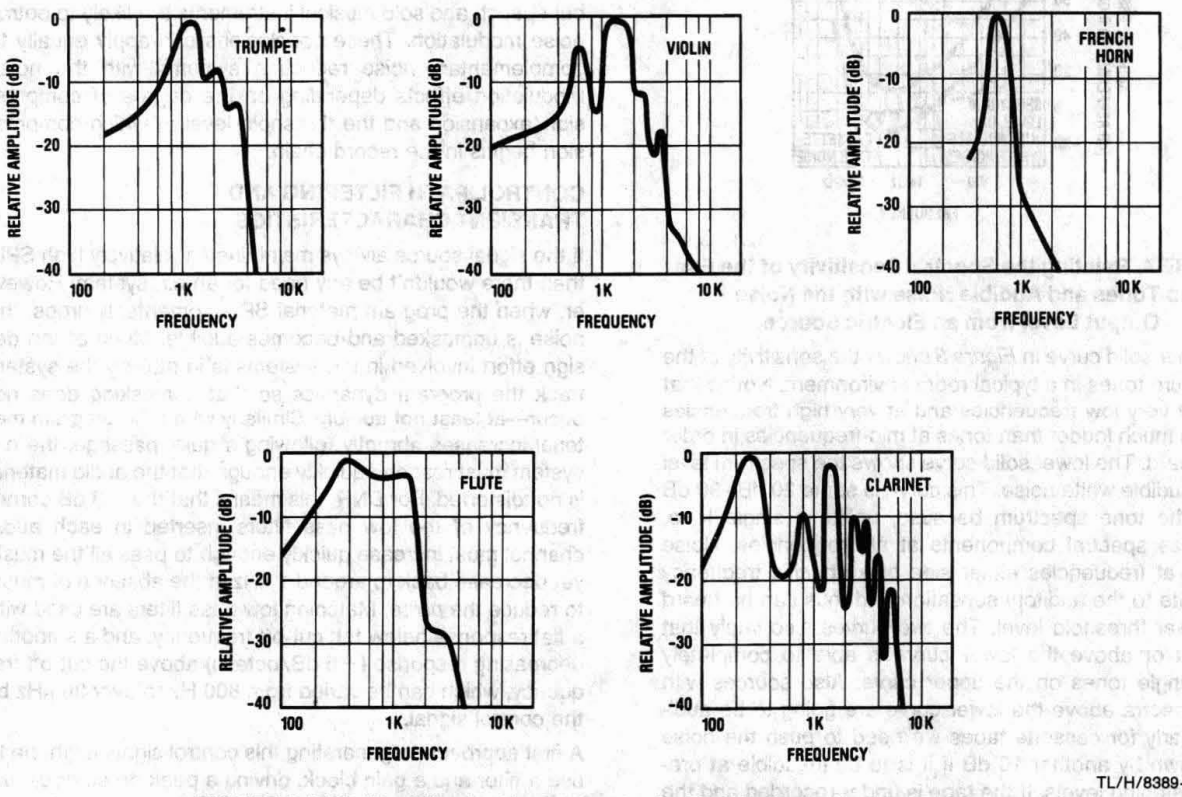

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FIGURE 5. With Most Musical Instruments, As Well As Speech, Energy Is Concentrated around 1 kHz with a Rapid Fall-Off in Level above 6 kHz

the end of a large signal transient. To avoid this, DNR uses a natural decay to within 10% of the final value in 60 ms. The inability of the ear to recover for 100 ms to 150 ms following a loud sound prevents the noise that is present (until the bandwidth is closed down) from being heard. Again a contrast with compander action is appropriate. As the DNR detector control voltage decays, the bandwidth starts to diminish, Initially only high frequencies are affected and since the harmonic amplitude of the signal is also decaying rapidly, the audio is unaffected by this decrease in bandwidth. For a compander however, as the control voltage decays, the system gain is altered—which also affects the signal mid-band and low frequency components. Thus, as with attack times, DNR is substantially less affected by the choice of release times, permitting a high tolerance in component values.

CIRCUIT OPERATION

The entire DNR system is contained within a single I/C and consists of two main functional signal paths. The audio path includes two low distortion low pass filters for a stereo audio source and the control path has a summing amplifier, variable gain filter amplifier and a peak detector. These functions are combined as shown in *Figure 7* which also shows the typical external components required for a complete n.r. system. By low distortion, we mean a filter that maintains the same cut-off slope and does not peak at the corner frequency as this frequency is changed. A 6 dB/octave filter slope was chosen since this provides a reasonable amount of noise reduction when the −3 dB frequency is less than 2 kHz and does not audibly affect the program material when the control path threshold is correctly set. It is possible to cascade the two audio filters—with a corresponding reduction in the size of the feedback capacitors to maintain the same operating frequency range—for a 12 dB/octave slope and up to 18 dB noise reduction. However, this steeper roll-off characteristic is better suited for program material that is relatively deficient in high frequency content, early recordings or video tapes for example.

Each audio filter consists of a variable transconductance stage driving an amplifier with capacitative feedback. For a fixed capacitor value, as the transconductance is changed by the control signal, the open loop unity gain frequency is changed correspondingly, giving a variable corner frequency low-pass filter. Of particular importance in the design is the need to avoid voltage offsets at the filter output caused by control action, and the ability of the input stage to accommodate large signal swings without introducing distortion. Output offset voltages are not necessarily proportional to the change in control voltage but will, in any case, be accompanied by a significant change in the program level. Extensive listening tests have shown that offset voltages 26 dB or more below the nominal signal input level will not be heard. Overload capability is dependent on the input stage current level and the available supply voltage, but

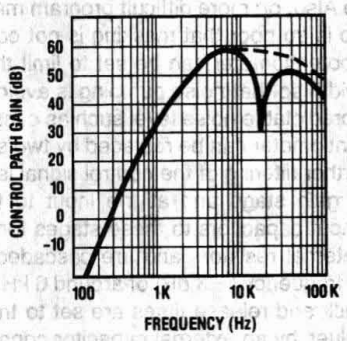

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FIGURE 6. Control Path Characteristic (Including Optional 19 kHz Notch)

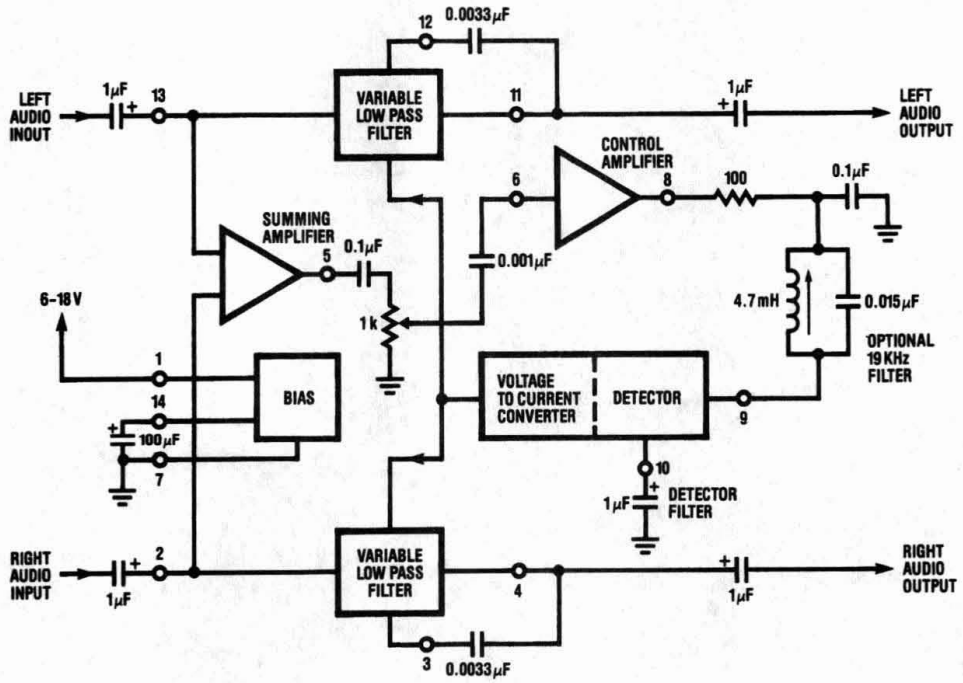

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FIGURE 7. The DNR System with Recommended Circuit Values

even with an 8 VDC supply the LM1894 can handle signals more than 20 dB over the nominal input level without increased distortion.

A summing amplifier is used at the input to the control path so that both left and right audio channels contribute to the control signal. Both audio filters are controlled with the same signal yielding matched audio bandwidths and maintaining a stable stereo image. From the summing amplifier the signal passes through a high-pass filter formed by the coupling capacitor and a 1 kΩ potentiometer. These components produce an amplitude roll-off below 1.6 kHz to avoid control path overload and help prevent high level, low frequency signals (drum beats for example) from activating the detector unnecessarily. The potentiometer provides a means to adjust the overall gain of the control path such that the input source noise level is able to just cross the detector threshold and begin opening the audio bandwidth. The correct adjustment point is one that permits alternate use and bypass of the DNR system with no audible change in the program material—other than reduction of background noise Also, on more difficult program material where the S/N ratio is so poor that masking is not completely effective, the potentiometer can be set to limit the maximum audio bandwidth so that noise pumping is avoided. For systems with a predictable noise level such as cassette recorders, the potentiometer can be replaced by two suitable fixed resistors. Further filtering of the control signal is done at the input to the gain stage and at the input to the detector stage. The input capacitors to these stages form high pass filters with internal resistors and are cascaded for a combined corner frequency (−3 dB) of around 6 kHz. Finally the detector attack and release times are set to the previously described values by an external capacitor connected to the peak detector output.

This paper has described the DNR non-complementary noise reduction system in terms of the functional blocks and the psychocoustic background necessary to understand the operating principles. For a more complete circuit description and practical details on the use of the LM1894, see the data sheet and AN386. Note that DNR is a trademark of National Semiconductor Corporation and that use of the DNR logo is by license agreement only.

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2) 'Absolute Amplitudes and Spectra of Certain Musical Instruments and Orchestras', Sixian et al, JASA, Vol. 2, #1.
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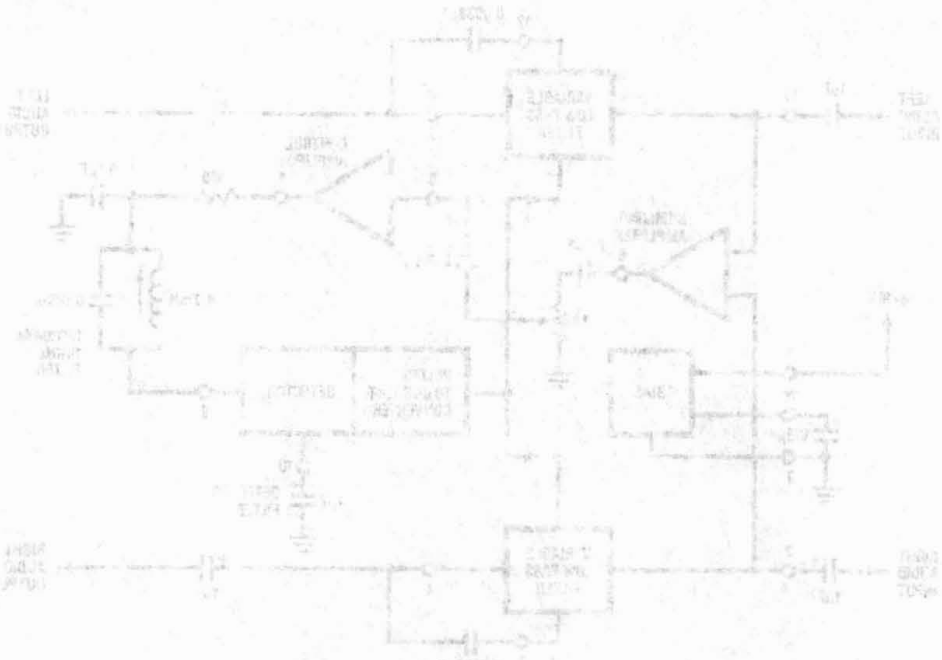


A Non-Complementary Audio Noise Reduction System

National Semiconductor
Application Note 386
Martin Giles

INTRODUCTION

The popularity of companding or complementary noise reduction systems is self-evident. Nearly all medium to high quality cassette tape decks include either Dolby® B or Dolby C type noise reduction. A scant few have different systems such as dbx or Hi-Com. The universal appeal of compandors to n.r. system designers is the amount of noise reduction they can offer, yet one of the major reasons the Dolby B system gained dominance in the consumer marketplace is because it offered only a limited degree of noise reduction — just 10 dB. This was sufficient to push cassette tape noise down to the level where it became acceptable in good-quality applications, yet wasn't enough that undecoded playback on machines not equipped with a Dolby B system was unsatisfactory — quite the contrary, in fact. The h.f. boost on Dolby B encoded tapes when reproduced on systems with modest speakers was frequently preferred. Since companding systems are so popular, it is not unreasonable to ask, "why do we need another noise reduction system?"

For many of the available audio sources today, compandors are not a solution for audio noise. When the source material is not encoded in any way and has perceptible noise, complementary noise reduction is not possible. This includes radio and television broadcasts, the majority of video tapes and of course, older audio tape recordings and discs. The DNR™ single-ended n.r. system has been developed specifically to reduce noise in such sources. A single-ended system, able to provide noise reduction where non previously existed, and which avoids compatability restraints or the imposition of yet another recording standard for consumer equipment, is therefore attractive.

The DNR system can be implemented by either of two integrated circuits, the LM1894 or the LM832, both of which can offer between 10 and 14 dB noise reduction in stereo program material. Although differing in some details (the LM832 is designed for low-signal, low-supply voltage applications) the operation of the integrated circuits is essentially the same. Two basic principles are involved; that the noise output is proportional to the system bandwidth, and that the desired program material is capable of "masking" the noise when the signal-to-noise ratio is sufficiently high. DNR automatically and continuously changes the system bandwidth in response to the amplitude and frequency content of the program. Restricting the signal bandwidth to less than 1 kHz reduces the audible noise and a special spectral weighting filter in the control path ensures that the audio bandwidth in the signal path is always increased sufficiently to pass any music that may be present. Because of this ability to dynamically analyze the auditory masking qualities of the program material, DNR does not require the source to be encoded in any special way for noise reduction to be obtained. This paper deals with the design and operating characteristics of the LM1894. For a more complete description of the principles behind the DNR system, refer to AN384.

THE DNR SYSTEM FORMAT

A block diagram showing the basic format of the LM1894 is shown in *Figure 1*. This is a stereo system with the left and right channel audio signals each being processed by a controlled cut-off frequency ($f_{-3\ dB}$) low-pass filter. The filter cut-off frequency can be continuously and automatically adjusted between 800 Hz and 35 kHz by a signal developed in the control path. Both audio inputs contribute to the control path signal and are used to activate a peak detector which, in turn, changes the audio filters' cut-off frequency. The audio path filters are controlled by the same signal for equally matched bandwidths in order to maintain a stable stereo image.

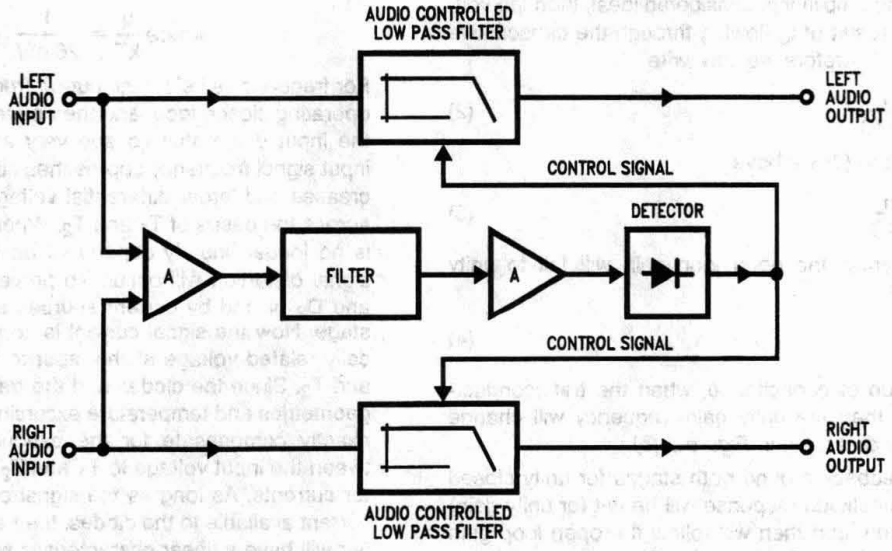
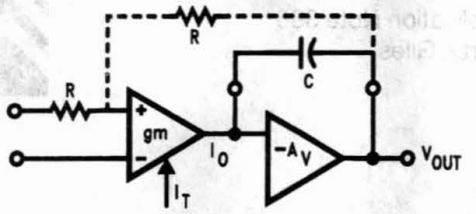


FIGURE 1. Stereo Noise Reduction System (DNR)



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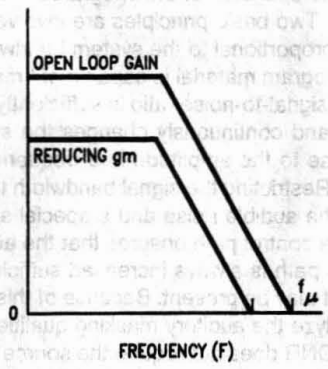
(a) Variable Lowpass Filter



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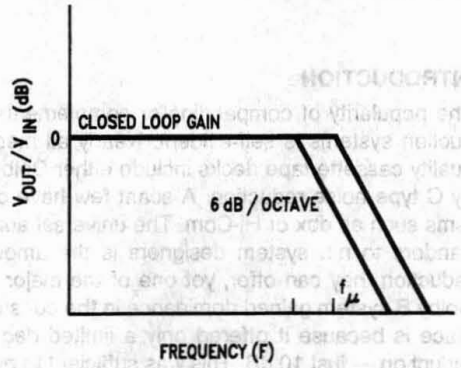
(b) Open Loop Response



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(c) Closed Loop Response

FIGURE 2

VARIABLE CUT-OFF LOW DISTORTION FILTERS

By low distortion we mean a filter that has a flat response below the cut-off frequency, a smooth, constant attenuation slope above the cut-off frequency and does not peak at the cut-off frequency as this frequency is changed.

The circuit topology is shown in *Figure 2 (a)* and is, in fact, very similar to the pole-splitting frequency compensation technique used on many integrated circuit operational amplifiers (see pp. 24–26 of "Intuitive I/C Op Amps" by T. M. Fredericksen). A variable transconductance (g_m) stage drives an amplifier configured as an integrator. The transconductance stage output current I_O is given by

$$I_o = g_m V_{in} \quad (1)$$

and if the second amplifier is considered ideal, then the voltage V_{out} is the result of I_o flowing through the capacitative reactance of C. Therefore we can write

$$V_{out} = \frac{I_o}{2\pi fC} \quad (2)$$

Combining (1) and (2) we have

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{2\pi fC} \quad (3)$$

At some frequency, the open loop gain will fall to unity ($f = f_u$) given by

$$f_u = \frac{g_m}{2\pi C} \quad (4)$$

For a fixed value of capacitance, when the transconductance changes, then the unity gain frequency will change correspondingly as shown in *Figure 2 (b)*.

If we put dc feedback around both stages for unity closed loop gain, the amplitude response will be flat (or unity gain) until f_u is reached, and then will follow the open loop gain curve which is falling at 6 dB/octave. Since we control g_m, we can make f_u any frequency we desire and therefore have a controlled cut-off frequency low pass filter.

A more detailed schematic is given in *Figure 3* and shows the resistors R_f and R_i which provide dc feedback around the circuit for unity closed-loop gain (i.e. at frequencies below f_u). The transconductance stage consists of a differential pair T_1 and T_2 with current mirrors replacing the more conventional load resistors. The output current I_o to the integrator stage is the difference between T_1 and T_2 collector currents.

For a differential pair, as long as the input differential voltage is small — a few millivolts — the g_m is dependent on the tail current I_T and can be written

$$g_m = \frac{q}{kT} \times \frac{I_T}{2} \quad (5)$$

$$\text{where } \frac{q}{kT} = \frac{1}{26\text{ mV}} \text{ @25°C}$$

For frequencies below the cut-off frequency, the amplifier is operating closed loop, and the dc feedback via Rf will keep the input differential voltage very small. However, as the input signal frequency approaches cut-off, the loop gain decreases and larger differential voltages will start to appear across the bases of T_1 and T_2. When this happens, the g_m is no longer linearly dependent on the tail current I_T and signal distortion will occur. To prevent this, two diodes D_1 and D_2 biased by current sources are added to the input stage. Now the signal current is converted to a logarithmically related voltage at the input to the differential pair T_1 and T_2. Since the diodes and the transistors have identical geometries and temperature excursions, this conversion will exactly compensate for the exponential relationship between the input voltage to T_1 and T_2 and the output collector currents. As long as the signal current is less than the current available to the diodes, the transconductance amplifier will have a linear characteristic with very low distortion.

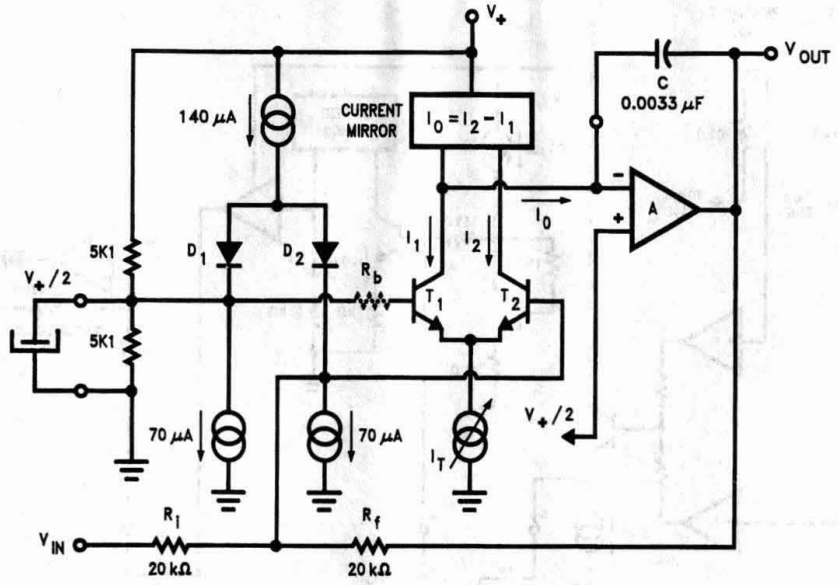

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FIGURE 3. Variable Lowpass Filter with Distortion Correcting Diodes and Control Voltage Offset Compensation

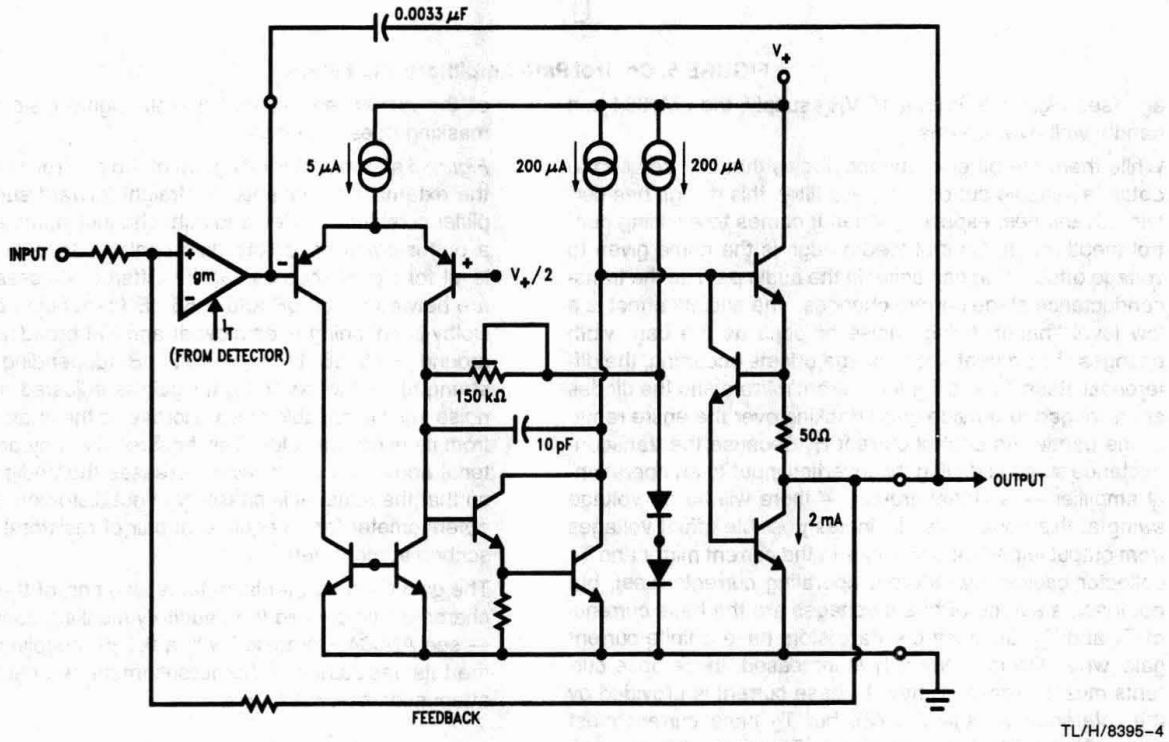

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FIGURE 4. The OP AMP Output Stage of the LM1894

For the entire circuit, if $R_i = R_f = R$ and the diode dynamic resistance is r_e, we can write the transfer characteristic as

$$\frac{V_{out}}{V_{in}} = \frac{-1}{\left(1 + \frac{4\pi f C K\, 26 \times 10^{-3}}{I_T}\right)} \qquad (6)$$

$$\text{where } K = \left(2 + \frac{R}{2r_e}\right)$$

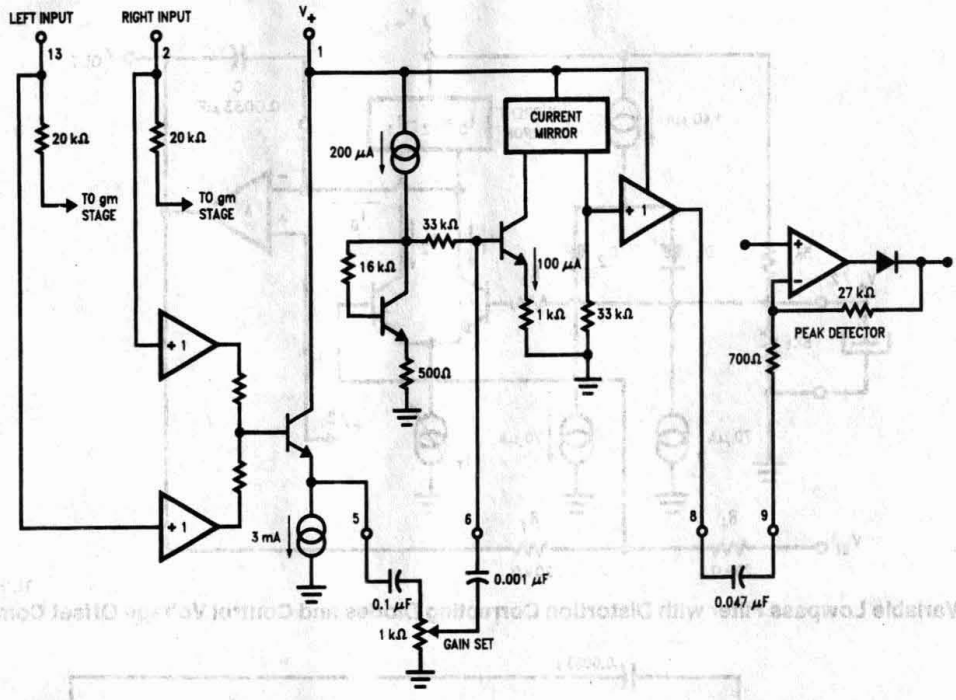
Therefore the pole frequency for C = 0.0033 µF is

$f_u = I_T/4\,\pi\, 26 \times 10^{-3} CK = I_T \times 33.2 \times 10^6$

for f_u = 1 kHz, I_T = 33.2 µA

for f_u = 35 kHz, I_T = 1.1 mA

In operation, the transconductance stage current I_T for the LM1894 will vary between the levels given above in response to the control path detected voltage. Notice that with the circuit values given in *Figure 3* the maximum output voltage swing at the cut-off frequency is about IV_{rms} (use equation 2 and put $I_O = I_T$ = 33 µA) and this is specified in the LM1894 data sheet as the input voltage for 3% THD. This is, of course, the condition for minimum bandwidth when noise only is normally present at the input. When signals are simultaneously present causing the audio bandwidth to increase out to 35 kHz, the transconductance stage current is over 1 mA, allowing signal swings at 1 kHz (theoretically) of over 34 Vrms. Practically, at maximum bandwidth the output swing is determined by the output stage saturation voltages which are dependent on the supply volt-



TL/H/8395–5

FIGURE 5. Control Path Amplifiers and Filters

age (see *Figure 4*). With a 15 V_{DC} supply, the LM1894 can handle well over 4 Vrms.

While there are other circuit topologies that can be used to obtain a variable cut-off low pass filter, this design has certain advantages, especially when it comes to avoiding control feedthrough. Control feedthrough is the name given to voltage offsets that can occur in the audio path as the transconductance stage current changes. The audible effect is a low level "bacon frying" noise or pops as the bandwidth changes. To prevent such voltage offsets occurring, the differential stage T_1 and T_2, the current mirrors and the diodes are arranged to provide good tracking over the entire range of the bandwidth control current I_T. Because the transconductance stage is driving the inverting input to an operational amplifier — a virtual ground — there will be no voltage swing at this node. This eliminates possible offset voltages from output impedance changes in the current mirror and T_1 collector caused by different operating currents. Last, but not least, a source of offset voltages are the base currents of T_1 and T_2. Because the transistors have a finite current gain, when the tail current I_T is increased, these base currents must increase slightly. T_1 base current is provided by the reference voltage ($V_+/2$), but T_2 base current must come via the feedback resistor R_f. This current is not normally available from D_2 because the feedback loop is holding T_1 and T_2 base voltages equal. By adding the resistor R_b in series with T_1 base, a compensating offset voltage is produced across the input diodes. This reduces the current in D_1 slightly and increases the current in D_2 correspondingly, allowing it to supply the increased base current requirement of T_2.

THE CONTROL PATH

The purpose of the control path is to ensure that the audio bandwidth is always sufficiently wide to pass the desired signal, yet in the absence of this signal will decrease rapidly enough that the noise also present does not become audible. In order to do this, the control path must recognize the masking qualities of the signal source and the detector stage must be able to take advantage of the characteristics of the human ear so that audible signal distortion or unmasking does not occur.

Figure 5 shows a block diagram of the control path including the external components. A straight-forward summing amplifier combines the left and right channel inputs and acts as a buffer amplifier for the gain control. Because the noise level for signal sources can be different — cassette tapes are between −50 dB and −65 dB (depending on whether Dolby B encoding is employed) and FM broadcast noise is around −45 dB to over −75 dB (depending on signal strength) — the control path gain is adjusted such that a noise input is capable of just increasing the audio bandwidth from its minimum value. This ensures that any program material above the noise level increases the audio bandwidth so that the material is passed without distortion. Setting the potentiometer (or an equivalent pair of resistors) will be described in more detail later.

The gain control potentiometer is also part of the DNR filter characteristic derived from auditory masking considerations — see AN384. Combined with a 0.1 μF coupling capacitor, the total resistance of the potentiometer will cause a signal attenuation below 1.6 kHz.

$$\text{i.e. } f_1 = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}} = 1.6 \text{ kHz}$$

This helps to prevent signals with a high amplitude but no high frequency content above 1 kHz — such as a bass drum — from activating the control path detector and unnecessarily opening the audio bandwidth. For signals that do have a significant high frequency content (predominantly harmonics), the control path sensitivity is increased at a 12 dB/octave rate. This rapid gain in sensitivity is important since the harmonic content of program material typically falls off quickly with increasing frequency. The 12 dB/octave slope is provided by cascading two RC high pass filters composed of the coupling capacitors to the control path gain stage and detector stage and the internal input resistors to these stages. Individual corner frequencies of 5.3 kHz and 4.8 kHz respectively are used, with a combined corner frequency around 6 kHz. Above 6 kHz the gain can be allowed to

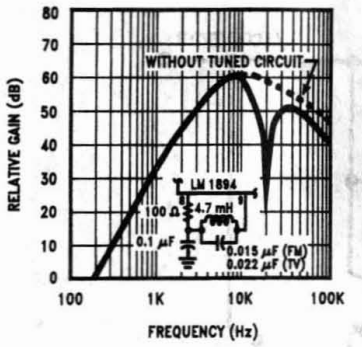


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FIGURE 6. Control Path Frequency Response

decrease again since the signal energy content between 1 kHz and 6 kHz (the critical masking frequency range) will have already caused the audio bandwidth to extend beyond 30 kHz, allowing passage of any high frequency components in the audio path.

Under some circumstances, not normal to music or speech, the source can contain relatively high level, high frequency components which are not necessarily accompanied by large levels of low frequency signal energy providing noise masking. These are spurious components such as the line scan frequency in a television receiver (15.734 kHz) or subcarrier signals such as the 19 kHz pilot tone in FM stereo broadcasting. Although both these components should be low enough to be inaudible in the audio path, their presence in the control path could cause a change in the minimum bandwidth and hence the amount of available noise reduction. Since these unwanted components are at frequencies higher than the desired control path frequency range, they are easily accommodated by including a notch filter in the control path at the specified frequency. A resonant L-C circuit with a Q of 30 will attenuate 19 kHz by over 28 dB. If a 10% tolerance 0.015μF capacitor is used, the coil can be a fixed 4.7 mH inductance. For 15.734 kHz a 0.022 μF capacitor is needed. When those frequency components are not present (i.e. in cassette tapes) the L-C circuit is eliminated and the gain amplifier and detector stage are coupled together with a single 0.047 μF capacitor.

Apart from providing the proper frequency response the control path gain must be enough to ensure that the detector threshold can be reached by very low noise input levels. The summing amplifier has unity gain to the sum of the left and right channel inputs and the necessary signal gain of 60 dB is split between the following gain amplifier and the detector stage. For the gain amplifier

$$A_V = 33 \times 10^3/(r_e + 10^3) = 26.2 = 28.4 \text{ dB}$$

For the detector stage, the gain to negative signal swings is

$$A_V = 27 \times 10^3/700 = 38.6 = 31.7 \text{ dB}$$

With over 60 dB gain and typical source input noise levels, the gain potentiometer will normally be set with the wiper arm close to the ground terminal.

THE DETECTOR STAGE

The last part of the LM1894 to be described is the detector stage which includes a negative peak detector and a voltage to current converter. As noted earlier, the input resistance of the detector, together with the input coupling capacitor, forms part of the control path filter. Similarly the output resistance from the detector and the gain setting feedback resistor help to determine the detector time constants. With a pulse or transient input signal, the rise time is 200 μs to 90% of the final detected voltage level. Actual rise-times will normally be longer with the detector tracking the envelope of the combined left and right channel signals after they have passed through the control path filter.

An interesting difference to compandor performance can be demonstrated with a 10 kHz tone burst. Since the LM1894 detector responds only to negative signal peaks, it will take about four input cycles to reach 90% of the final voltage on the detector capacitor (this is the 500 μs time constant called out in the data sheet). After the first two cycles the audio bandwidth will have already increased past 10 kHz and a comparison of the input and output tone bursts will show only a *slight* loss in amplitude in these initial cycles. A compandor, however, usually cannot afford a fast detector time constant since the rapid changes in system gain that occur when a transient signal is processed can easily cause modulation products to be developed which may not be treated complementarily on playback, Therefore there is a time lag before the system can change gain, which may be to the maximum signal compression (as much as 30 dB depending on the compandor type). Failure to compress immediately at the start of the tone burst means that an *overshoot* is present in the signal which can be up to 30 dB higher than the final amplitude. To prevent this overshoot from causing subsequent amplifier overload (which can last for several times the period of the overshoot), clippers are required in the signal path, limiting the dynamic range of the system. Obviously, the LM1894 does not need clippers since no signal overshoots in the audio path are possible.

When the input signal transient decays, the diode in the detector stage is back biassed and the capacitor discharges primarily through the feedback resistor and takes about 60 ms to reach 90% of the final value.

$$T = RC \times 2.3 = 27 \times 10^3 \times 1 \times 10^{-6} \times 2.3 = 62.1 \text{ ms}$$

The decay time constant is required to protect the reverberatory or "ambience" qualities of the music. For material with a limited high frequency content or a particularly poor S/N ratio, some benefit can be obtained with a faster decay time—a resistor shunted across the detector capacitor will do this. Resistors less than 27 kΩ should not be used since very fast decay times will permit the detector to start tracking the signal frequency. For signal amplitudes that are not producing the full audio bandwidth, this will cause a rapid and audible modulation of the audio bandwidth.

BYPASSING THE SYSTEM

Sometimes it is necessary or desirable to bypass the n.r. system. This will allow a direct and instantaneous comparison of the effect that the system is having on the program material and will assist in arriving at the correct setting for the control path gain potentiometer. This facility is not practical with compandors unless unencoded passages occur in the program material. Also, should the action of the compandor become more objectionable than the noise in the original material, there is no way of switching the n.r. system off.

One way of bypassing is to simply use a double pole switch to route the signals around the LM1894. This physically ensures complete bypassing but does present a couple of problems. First, there may be a level change caused by the different impedances presented to the following audio stages when switching occurs. Second, the signal now has to be routed to the front panel where the switch is located, perhaps calling for shielded cable.

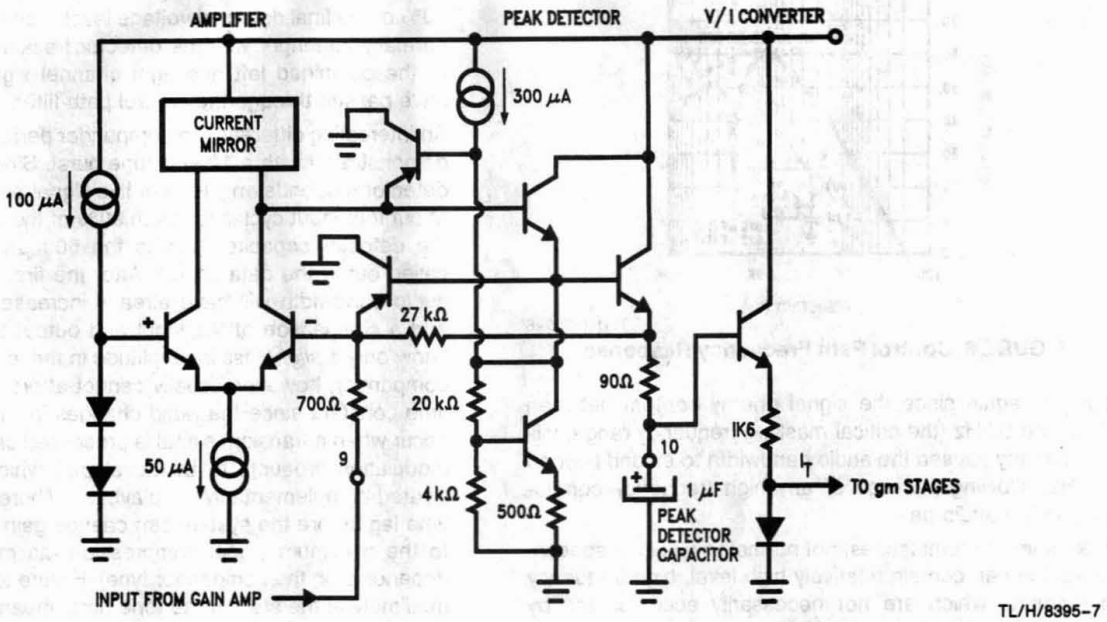
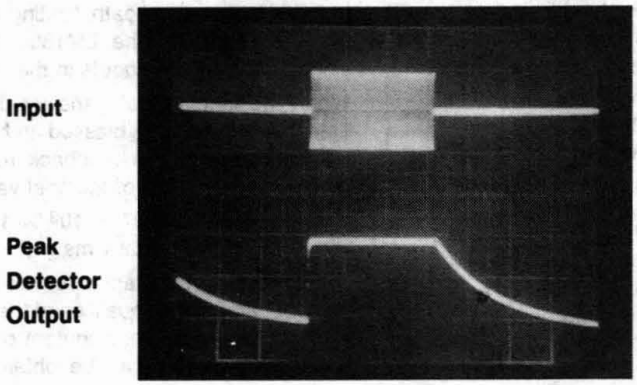
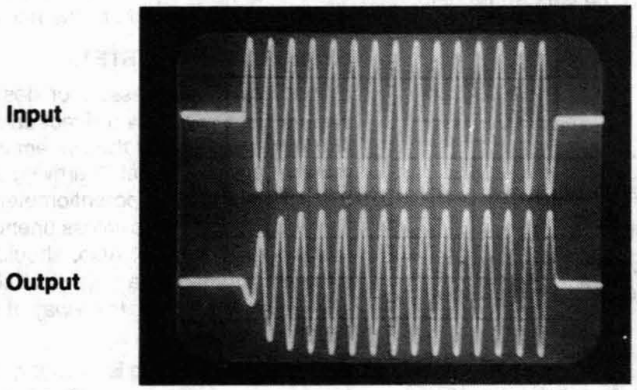


FIGURE 7. Peak Detector and Voltage to Current Converter



TIME: 20 ms/DIV

Peak Detector Response, 500 mV/Div



TIME: 0.5 ms/DIV

Audio Output Response, 10 kHz Tone Burst

FIGURE 8

A different technique, which avoids these problems, is to switch the LM1894 permanently into the full audio bandwidth mode. Since this provides a high S/N ratio path and low distortion the impact on the signal is minimal. Two methods can be used to switch the LM1894 audio bandwidth fully open, both with a single pole switch that is not in the audio path. Simply grounding the input of the peak detector amplifier will generate the maximum bandwidth control current and simultaneously prevent any control signals reaching the detector. Usually this is more than adequate since the maximum audio bandwidth is 34 kHz, but in some cases the 1 dB loss at 17 kHz produced by the single pole audio filters may not be desired. *Figure 9* shows a way to increase the audio bandwidth to 50 kHz (−1 dB at 25 kHz) by pulling up the detector capacitor to the reference voltage level ($V_+/2$) through a 1 kΩ resistor. This method is useful only for higher supply voltage applications. To increase the bandwidth significantly the detector capacitor must be pulled up to around 5V ($V_+ > 10V$). Although a separate voltage source other than the reference pin could be used when V_+ is less than 10V, this can cause an internal circuit latch-up if the voltage on the detector increases faster than the reference voltage at initial turn-on.

GENERAL SYSTEM MEASUREMENTS AND PRECAUTIONS

For most applications the external components shown in *Figure 9* will be required. In fact, the only recommended deviation from these values is the substitution of an equivalent pair of fixed resistors for the gain setting potentiometer. Location of the LM1894 in the audio path is important and should be prior to any tone or volume controls. In tape systems, right after the playback head pre-amplifier is the best place, or at the stereo decoder output (after de-emphasis and the multiplex filter) in an FM broadcast receiver. The LM1894 is designed for a nominal input level of 300 mVrms and sources with a much lower pre-amplifier output level will either require an additional gain block or substitution of the LM832 which is designed for 30 mVrms input levels.

The same circuit as *Figure 9* can be used for measurements on the I/C performance but, as with any other n.r. system, care in intepretation of the results may be necessary. For example, while the decay time constant for a tone burst signal is pretty constant, the attack time will depend on the tone frequency.

Sometimes separation of the audio path input and the control path is required, particularly when the frequency response or the THD with low input signal levels is being measured. If the audio and control paths are not separated then a typical audio system measurement of the frequency response will not appear as expected. This is because the control path frequency response is non-linear, exhibiting low sensitivity at low frequencies. When a low level input signal is swept through the audio frequency range, at low frequencies the audio −3 dB bandwidth will be held at 1 kHz, and the audio path signal will fall in amplitude as the signal goes above 1 kHz. As the signal frequency gets yet higher, the increasing sensitivity of the control path will allow the detector to be activated and the audio path −3 dB frequency starts to overtake the signal frequency. This causes the output signal amplitude to increase again giving the appearance that there is a dip in the audio frequency response around 1–2 kHz. It is worth remembering at this point that the audio path frequency response is always flat below some corner frequency and rolls off at 6 dB/octave above this frequency. In normal operation this corner frequency is the result of the aggregate control path signals in the 1 kHz to 6 kHz region and not the result of a single input frequency. To properly measure the frequency response of the audio path at a particular signal input frequency and amplitude, the control path input is separated by disconnecting C_5 from Pin 5 and injecting the signal through C_5 only. Then, a separate swept frequency response measurement can be made in the audio path. Similarly measurements of THD should include separation of the audio and control path inputs.

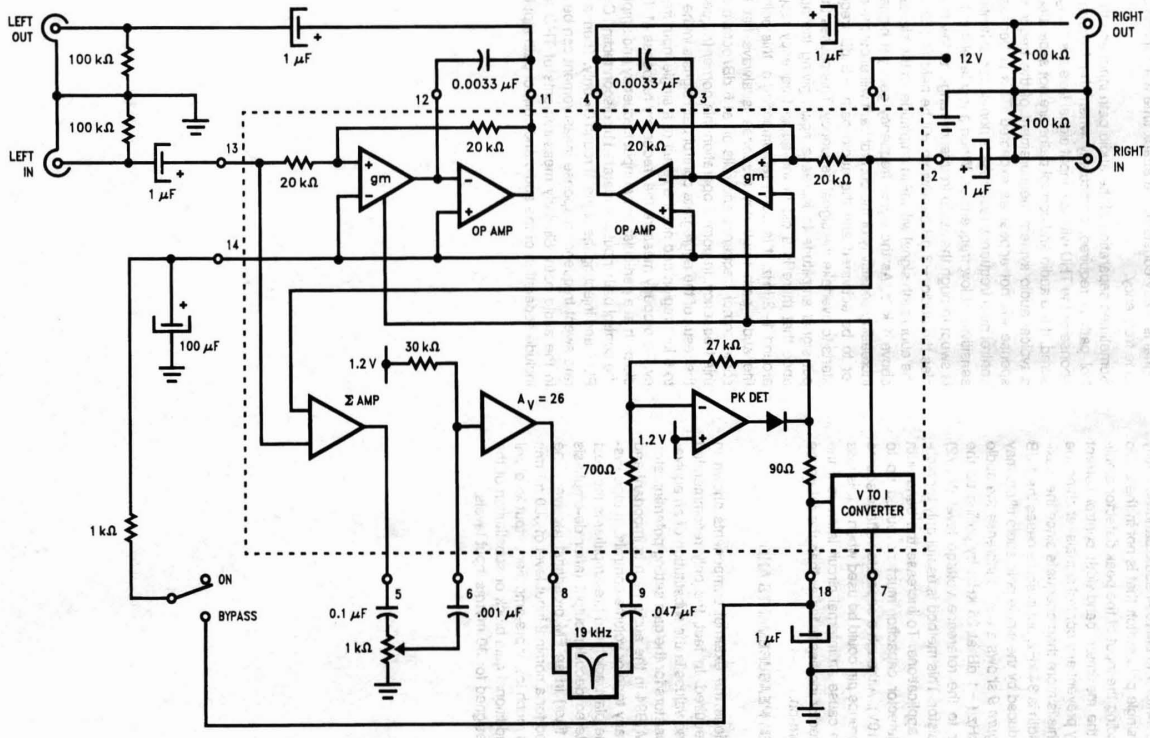


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FIGURE 9. Complete Stereo Noise Reduction System

PITFALLS - OR WHAT TO LISTEN FOR

Many people are understandably wary of non-complementary n.r. systems since there is no perfect means for distinguishing between the desired signal and noise. A thorough understanding of the psycho-acoustic basis for noise masking will go a long way to allaying these fears, but a much simpler method is to listen to a variety of source material with a DNR system being switched in and out. Even so, improper implementation of the LM1894—wrong location in the audio path changing either the level or frequency response of the source—or incorrect external component values, or the wrong sensitivity setting, can all strongly affect the audio in an undesired way. Sometimes, unhappily, the source is really beyond repair and some compromise must be made. Phonograph discs with bad scratches may require special treatment (a click and pop remover) and some older tape recordings may show some or all of the following problems.

1) Pumping:

   Incorrect selection of the control path bandwidth external components can result in an audible increase in noise as the input level changes. This is most likely to be heard on solo instruments or on speech. Sometimes the S/N rate is too poor and masking will not be completely effective - i.e., when the bandwidth is wide enough to pass the program material, the increase in noise is audible. Cutting down on the pumping will also affect the program material to some extent and judgement as to which is preferable is required. Sometimes a shorter decay time constant in the detector circuit will help, especially for a source which always shows these characteristics, but for better program material a return to the recommended detector characteristics is imperative.

2) High Frequency Loss:

   This can be caused by an improper control path gain setting—perhaps deliberate because of the source S/N ratio as described above—or incorrect values for the audio path filter capacitors. Capacitors larger than the recommended values will scale the operating bandwidth lower, causing lower −3 dB corner frequencies for a given control path signal. Return to the correct capacitor values and the appropriate control path gain setting will *always* ensure that the h.f. content of the signal source is preserved.

3) Apparent High Frequency Loss:

   The ability to instantaneously A/B the source with and without noise reduction can sometimes exhibit an apparent loss of h.f. signal content as the DNR system operates. This is most likely to happen with sources having an S/N ratio of less than 45 dB and is a subjective effect in that the program material probably does not have any significant h.f. components. It has been reported several times elsewhere that adding high frequency noise (hiss) to a music signal with a limited frequency range will seem to add to the h.f. content of the music. Trying sources with a higher S/N ratio that do not demonstrate this effect can re-assure the listener that the DNR system is operating properly. Alternatively a control path sensitivity can be used that leaves the audio bandwidth slightly wider, preserving the "h.f. content" at the expense of less noise reduction in the absence of music.

4) Sensitivity Setting:

   Since this is the only adjustment in the system, it is the one most likely to cause problems. Improper settings can cause any of the previously described problems. Factory pre-sets can (and are) used, but only when the source is well defined with known noise level. For the user who intends to noise reduce a variety of sources, the control path gain potentiometer is required and should be adjusted for each application. A bypass switch is helpful in this respect since it allows rapid A/B comparison. Another useful aid is a bandwidth indicator, shown in *Figure 10*. This is simply an LED display driver, the LM3915, operating from the voltage on the detector filter capacitor at Pin 10 of the LM1894. The LM3915 will light successive LEDs for each 3 dB increase in voltage. The resistor values are chosen such that the capacitor voltage when the LM1894 is at minimum audio bandwidth, is just able to light the first LED, and a full audio bandwidth control signal will light the upper LED. Experience will show that adjusting the sensitivity so that the noise in the source (no signal is present) is just able to light the second LED, will produce good results. This display also provides constant reassurance that the system audio bandwidth really is adequate to process the music. A simpler detector, using a dual comparator and a couple of LEDs can be constructed instead, with threshold levels selected to show the correct sensitivity setting, minimum bandwidth, maximum bandwidth or some intermediate bandwidth as desired.

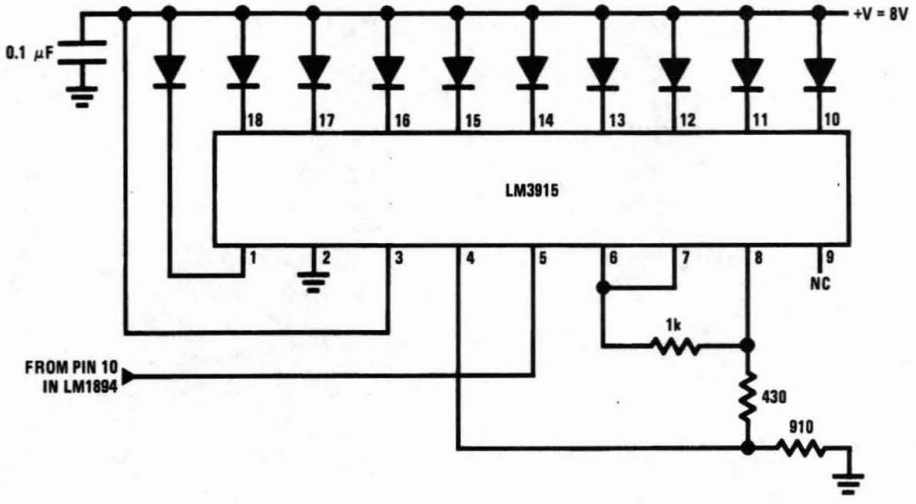

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FIGURE 10. Bar Graph Display of Peak Detector Voltage

DNR Component Diagram

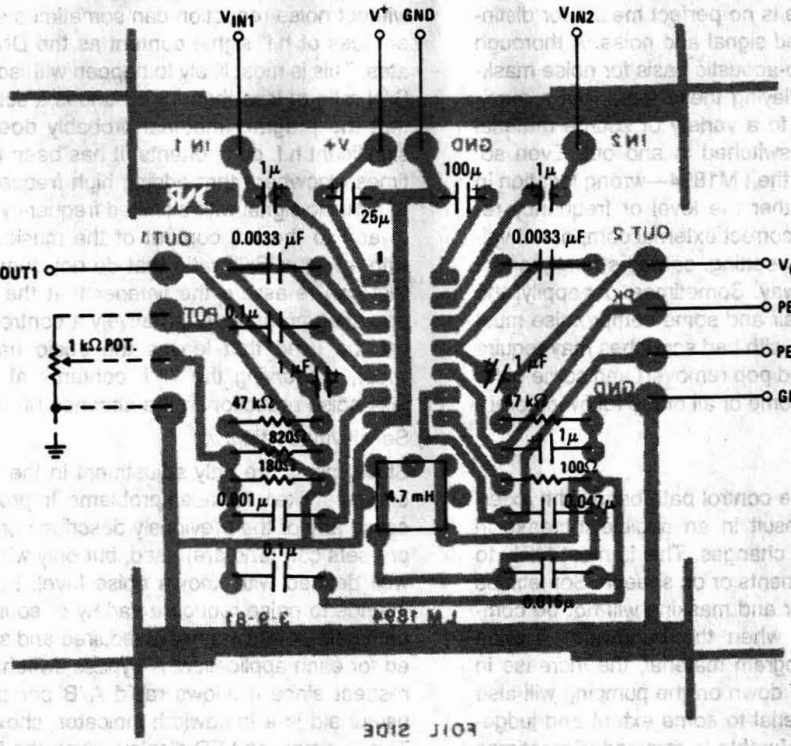

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FIGURE 11. Printed Circuit Layout

DNR™ Applications of the LM1894

National Semiconductor
Application Note 390
Martin Giles
Kerry Lacanette

INTRODUCTION

The operating principles of a single-ended or non-complementary audio noise reduction system, DNR, have been covered extensively in a previous application note AN384, Audio Noise Reduction and Masking. Although the system was originally implemented with transconductance amplifiers (LM13600) and audio op-amps (LM387), dedicated I/Cs have since been developed to perform the DNR function. The LM1894 is designed to accommodate and noise reduce the line level signals encountered in video recorders, audio tape recorders, radio and television broadcast receivers, and automobile radio/cassette receivers. A companion device, the LM832, is designed to handle the lower signal levels available in low voltage portable audio equipment. This note deals chiefly with the practical aspects of using the LM1894, but the information given can also be applied to the LM832.

THE BASIC DNR APPLICATION CIRCUIT

At the time of writing, the LM1894 has already found use in a large variety of applications. These include:

AUTOMOTIVE RADIOS
TELEVISION RECEIVERS
HOME MUSIC CENTERS
PORTABLE STEREOS (BOOM BOXES)
SATELLITE RECEIVERS
AUDIO CASSETTE PLAYERS
AVIONIC ENTERTAINMENT SYSTEMS
HI-FI AUDIO ACCESSORIES
BACKGROUND MUSIC SYSTEMS
ETC.

In the majority of these applications the circuit used is identical to that shown in *Figure 1,* and this is the basic stereo Dynamic Noise Reduction System. Although a split power supply can be used, a single positive supply voltage is shown, with ac coupled inputs and outputs common in many consumer applications. This supply voltage can be between 4.5 V_{DC} and 18 V_{DC} but operation at the higher end of the range (above 8 V_{DC}) is preferred, since this will ensure adequate signal handling capability. The LM1894 is optimized for a nominal input signal level of 300 mVrms but with an 8 V_{DC} supply it can handle over 2.5 Vrms at full audio bandwidth. Smaller nominal signal levels can be processed but below 100 mVrms there may not be sufficient gain in the control path to activate the detector with the source noise. In this instance, and where battery powered operation is desired, the LM832 is a better choice. The LM832 has identical operating principles and a similar (but not identical) pinout. It is optimized for input levels around 30 mVrms and a supply voltage range from 1.5 V_{DC} to 9.0 V_{DC}.

The capacitors connected at Pins 12 and 3 determine the range of −3 dB cut off frequencies for the audio path filters. Increasing the capacitor value scales the range downward – the minimum frequency becomes lower and the maximum or full bandwidth frequency will decrease proportionally. Similarly, smaller capacitors will raise the range.

$$f_{-3\,dB} = I_T/9.1C \; (I_T = 33\ \mu A\ MIN) \qquad (1)$$
$$(\quad = 1.05\ mA\ MAX)$$

For normal audio applications the recommended value of 0.0033 μF should be adhered to, producing a frequency range from 1 kHz to 35 kHz.

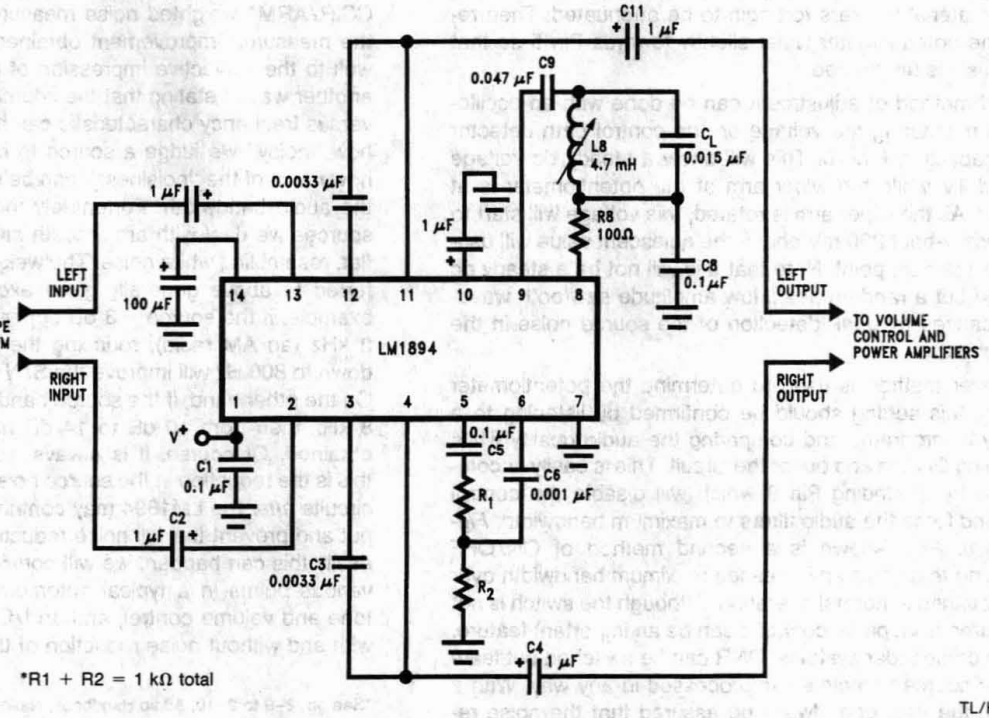

FIGURE 1. Complete DNR Application Circuit

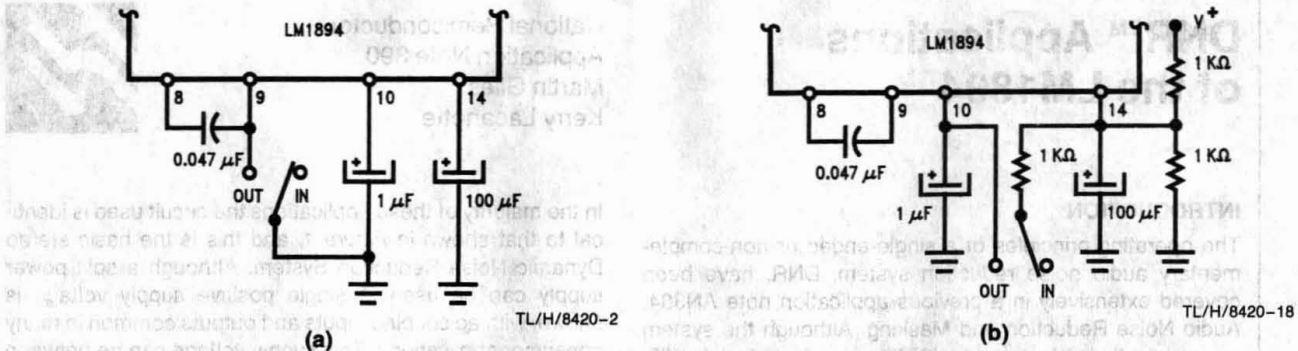

FIGURE 2. Two Methods of DNR IN/OUT Switching

The two resistors connected at Pin 5 set the overall control path gain, and hence the system sensitivity. A lower tap point will decrease the sensitivity for high signal level sources, and a higher tap point will accommodate lower level sources. For purposes of initial calibration it is best to replace the resistors with a 1 kΩ potentiometer (the wiper arm connecting through C_6 to Pin 6), and follow the procedures outlined below. Once the correct adjustment point has been found, the position of the wiper arm is measured and an equivalent pair of resistors are used to replace the potentiometer. This, of course, can be done only if the source has a relatively fixed noise floor—the output from an audio cassette tape for example. For an add-on audio accessory the potentiometer should be retained as a front panel control to allow adjustment for individual sources. Use of DNR with multiple sources is described later.

SYSTEM CALIBRATION

System calibration can be performed in a number of ways. With the source connected play a blank but biased section of the cassette tape. Set the potentiometer so that the wiper arm is at ground and then steadily rotate it until a slight increase in the output noise level is heard. Alternatively, with source program material present, set the potentiometer with the wiper arm connected to the Pin 5 end of the slider and again rotate until the high frequency content of the program material appears to begin to be attenuated. Then return the potentiometer wiper slightly towards Pin 5 so that the music is unaffected.

A third method of adjustment can be done with an oscilloscope monitoring the voltage on the control path detector filter capacitor, Pin 10. This will show a steady dc voltage around 1V while the wiper arm of the potentiometer is at ground. As the wiper arm is rotated, this voltage will start to increase. About 200 mV above the quiescent value will usually be the right point. Note that this will not be a steady dc voltage but a random peak, low amplitude sawtooth waveform caused by peak detection of the source noise in the control path.

Whatever method is used to determine the potentiometer setting, this setting should be confirmed by listening to a variety of programs and comparing the audio quality while switching DNR in and out of the circuit. This is easily accomplished by grounding Pin 9 which will disable the control path and force the audio filters to maximum bandwidth, *Figure 2(a)*. Also shown is a second method of ON/OFF switching that gives an increased maximum bandwidth over that obtained in normal operation. Although the switch is not a required front panel control it can be an important feature. Unlike compander systems, DNR can be switched out leaving the source completely unprocessed in any way. With a switch, the user can always be assured that the noise reduction is not affecting the program material.

Apart from the basic circuit shown in *Figure 1,* all applications of the DNR system have another feature in common—the location of the LM1894 in the signal chain. As *Figure 3* shows, the LM1894 is *always* placed right after the signal source pre-amplifier and *before* any circuit that includes user adjustable controls for volume or frequency response. The reasons for this are obvious. If the gain of the signal amplifier preceding DNR is changed arbitrarily, the noise input level to the LM1894 will not be at the correct point to begin activation of the audio path filters. Either reduced noise reduction will be obtained, or the high frequency content of the program material will be affected. A change in system gain prior to the LM1894 requires a corresponding change in the control path threshold sensitivity. Similarly modifying the frequency response, by heavy boost or cut of the mid to high frequencies, will have the same effect of changing the required threshold setting—apart from modifying the masking qualities of the program material.

HOW MUCH NOISE REDUCTION?

The actual sensitivity setting that is finally used, and the amount of noise reduction that is obtained, will depend on a number of factors. As the data sheet for the LM1894 and other application notes have explained in some detail, the noise reduction effect is obtained by audio bandwidth restriction with a pair of matched low-pass filters. A CCIR/ARM* weighted noise measurement is used so that the measured improvement obtained with DNR correlates well to the subjective impression of reduced noise. This is another way of stating that the source noise spectrum level versus frequency characteristic can have a large impact on how "noisy" we judge a source to be—and concomitantly how much of the "noisiness" can be reduced by decreasing the audio bandwidth. Fortunately most of the audio noise sources we deal with are smooth although not necessarily flat, resembling white noise. The weighting characteristic referred to above generally gives excellent correlation. For example, if the source −3 dB upper frequency limit is only 2 kHz (an AM radio), reducing the audio path bandwidth down to 800 Hz will improve the S/N ratio by only 5 to 7 dB. On the other hand, if the source bandwidth exceeds at least 8 kHz then from 10 dB to 14 dB noise reduction can be obtained. Of course, it is always worth remembering that this is the reduction in the source noise—any noise added in circuits *after* the LM1894 may contribute to the audible output and prevent the full noise reduction effect. To see how easily this can happen, we will consider the noise levels at various points in a typical automotive radio using an I/C tone and volume control, and an I/C power amplifier, both with and without noise reduction of the cassette player.

*See pp. 2-9 to 2-10, Audio Handbook, National Semiconductor 1980.

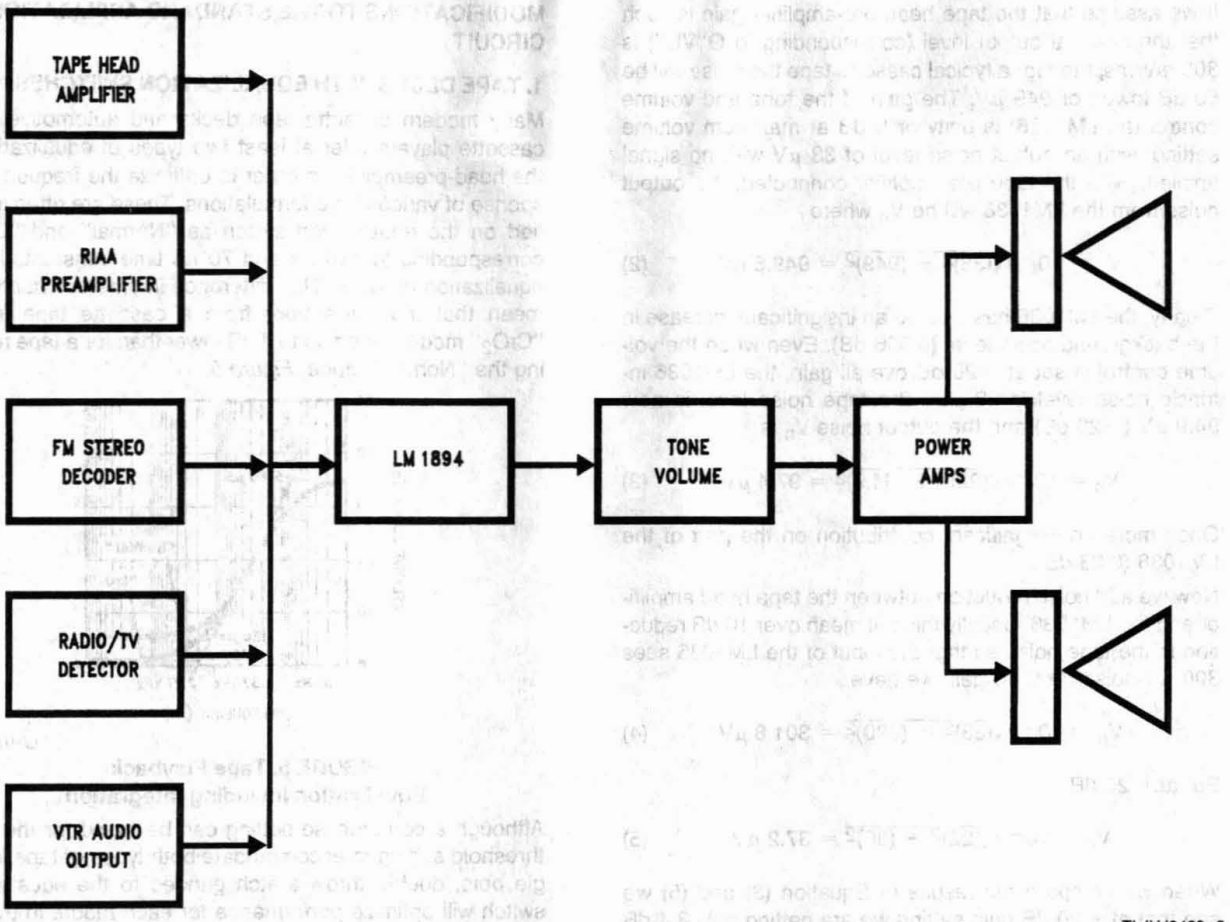

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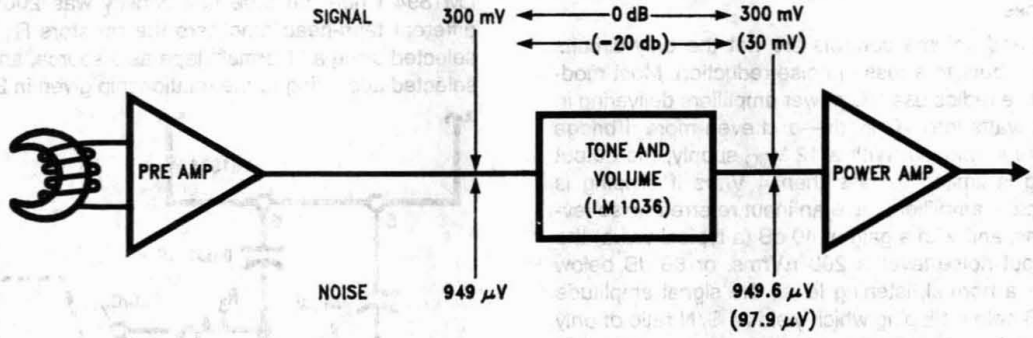
FIGURE 3. Location of DNR in Audio Systems



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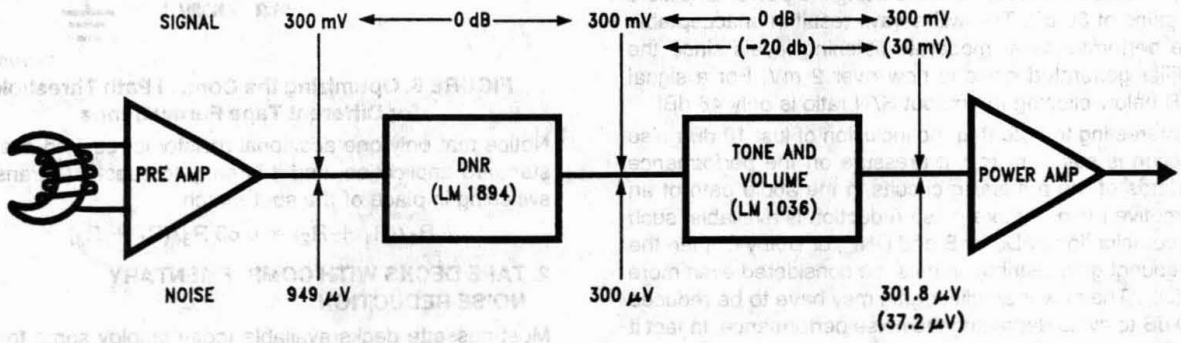
(a) Without Noise Reduction



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(b) With Noise Reduction

FIGURE 4. Signal and Noise Levels in the Audio Path

If we assume that the tape head pre-amplifier gain is such that the nominal output level (corresponding to O"VU") is 300 mVrms, then for a typical cassette tape the noise will be 50 dB lower, or 949 μV. The gain of the tone and volume control (an LM1036) is unity or 0 dB at maximum volume setting, with an output noise level of 33 μV with no signal applied. With the tape pre-amplifier connected, the output noise from the LM1036 will be V_n where

$$V_n = 10^{-6}\sqrt{(33)^2 + (949)^2} = 949.6\ \mu V \qquad (2)$$

Clearly, the LM1036 has caused an insignificant increase in the background noise level (0.006 dB). Even when the volume control is set at −20 dB overall gain, the LM1036 intrinsic noise level is 22 μV. The tape noise level is now 94.9 μV (−20 dB) and the output noise V_n is

$$V_n = 10^{-6}\sqrt{(22)^2 + (94.9)^2} = 97.4\ \mu V \qquad (3)$$

Once more an insignificant contribution on the part of the LM1036 (0.23 dB).

Now we add noise reduction between the tape head amplifier and the LM1036. Usually this will mean over 10 dB reduction in the tape noise so that the input of the LM1036 sees 300 μV noise. At 0 dB gain we have

$$V_n = 10^{-6}\sqrt{(33)^2 + (300)^2} = 301.8\ \mu V \qquad (4)$$

But at −20 dB

$$V_n = 10^{-6}\sqrt{(22)^2 + (30)^2} = 37.2\ \mu V \qquad (5)$$

When we compare the results of Equation (3) and (5) we see that at −20 dB gain setting we are getting only 8.4 dB noise reduction compared to 10 dB at maximum gain! Since the volume control is not normally set to maximum, this is a significant loss.

Active tone and volume controls are not the only circuits that can contribute to a loss in noise reduction. Most modern automotive radios use I/C power amplifiers delivering in excess of 6 watts into 4Ω loads—and even more if bridge amplifiers are employed. With a 12 V_{DC} supply, the output signal swing is limited to less than 4 Vrms if clipping is avoided. Typical amplifiers have an input referred noise level of 2 μVrms, and with a gain of 40 dB (a typical value) the intrinsic output noise level is 200 μVrms, or 86 dB below clipping. For a normal listening level, the signal amplitude will be 20 dB below clipping which yields a S/N ratio of only 66 dB—which is just better than the noise reduced input to the amplifier.

Many manufacturers recommend using I/C power amplifiers with gains of 60 dB. This will always result in unacceptable noise performance at moderate listening levels since the amplifier generated noise is now over 2 mV. For a signal 20 dB below clipping the output S/N ratio is only 46 dB!

It is interesting to note that the inclusion of just 10 dB noise reduction is sufficient to put pressure on the performance standards of the remaining circuits in the audio path of an automotive radio. If more noise reduction is available, such as a combination of Dolby B and DNR, or Dolby C, then the subsequent gain distribution must be considered even more carefully. The power amplifier gain may have to be reduced to 20 dB to avoid degrading the noise performance. In fact it may be impractical to realize the full noise performance capability of systems providing high levels of noise reduction in many automotive stereo radios.

MODIFICATIONS TO THE STANDARD APPLICATIONS CIRCUIT

1. TAPE DECKS WITH EQUALIZATION SWITCHES:

Many modern cassette tape decks and automotive radio cassette players offer at least two types of equalization in the head-preamplifier in order to optimize the frequency response of various tape formulations. These are often identified on the equalization switch as "Normal" and "CrO_2" corresponding to 120 μs and 70 μs time constants in the equalization network. This difference in time constants can mean that the noise floor from a cassette tape in the "CrO_2" mode can be up to 4 dB lower than for a tape requiring the "Normal" mode, *Figure 5*.

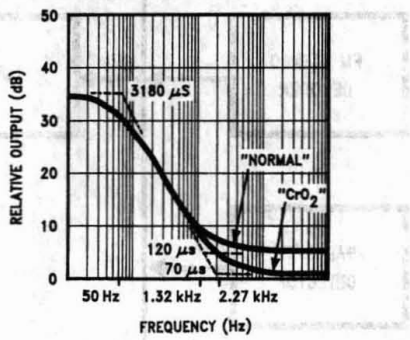

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FIGURE 5. Tape Playback Equalization Including Integration

Although a compromise setting can be found for the DNR threshold setting to accommodate both types of tape, a single pole, double throw switch ganged to the equalization switch will optimize performance for each mode. In the example given in *Figure 6,* the resistor values shown are from an application that yielded a 400 mVrms input to the LM1894 when the tape flux density was 200 nW/m. For different tape-head amplifiers the resistors R_1 and R_2 are selected using a "Normal" tape as a source, and then R_3 is selected according to the relationship given in Equation (5).

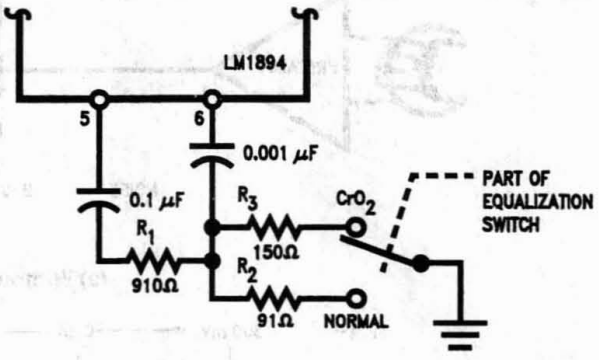

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FIGURE 6. Optimizing the Control Path Threshold for Different Tape Formulations

Notice that only one additional resistor is required over the standard application, and it is easy to substitute transistor switching in place of the spdt switch.

$$R_1/(R_1 + R_2) = 0.63\ R_3/(R_1 + R_3) \qquad (5)$$

2. TAPE DECKS WITH COMPLEMENTARY NOISE REDUCTION:

Most cassette decks available today employ some form of complementary (companding) noise reduction system, usually Dolby B Type. DNR can be used in conjunction with these noise reduction systems as a means to provide yet more noise reduction on decoded tapes and still provide

noise reduction for unencoded tapes. The LM1894 is located after the companding system and provision must be made for the drop in noise level when the compandor is being used. The DNR threshold sensitivity is increased by the appropriate amount so that the lower noise levels are still able to activate the audio filters. For example, the circuit in *Figure 7* shows a switching arrangement to compensate for the 9 dB lower noise floor from a Dolby B decoded tape. Notice the change in resistor values R_1 through R_3 to raise the sensitivity (yet keeping the sum of R_1 and R_2 to 1k) and the 9 dB pad formed by the 3 kΩ resistor and the 1.5 kΩ resistor in parallel with the control path input Pin 6, for use when the compandor is switched off. Since the output level from the compandor is usually around 580 mV for a flux density of 200 nW/m, the ratio of R_1 to R_2 and R_3 is changed by only 5.6 dB compared to that shown in the previous Figure where the input level was 400 mVrms.

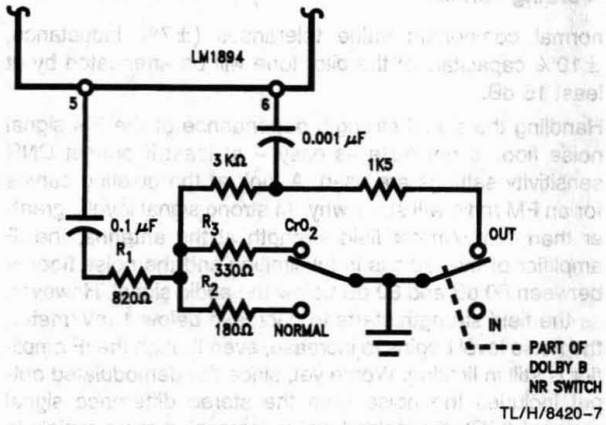

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FIGURE 7. Switching with Other NR Systems

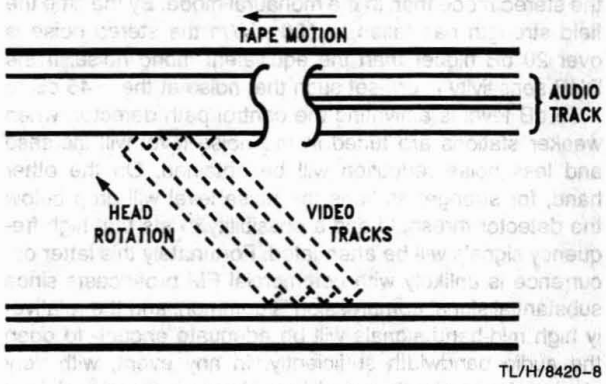

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FIGURE 8. Video Magnetic Tape Format

3. VIDEO TAPE RECORDERS:

The audio track of a video cassette tape is similar to an audio cassette and appears along one edge of the tape. Although provision is made for two tracks, each 0.35 mm wide, a large number of recordings are monaural with a track width of 1 mm (0.04 inches).

Unlike the video heads, which are mounted on a rotating drum and angled to the direction of tape travel in order to give a much higher recording speed, the audio is recorded longitudinally with a separate head at 33.35 mm/sec for standard play, 16.88 mm/sec for long play, and 11.12 mm/sec for the very long play mode (VHS format tape machines). The noise spectrum is similar to an audio cassette but with a couple of differences. The typical frequency response from the head pre-amplifier does not extend beyond 10 kHz in the SP mode and is less in the LP and VLP modes. Even so, this bandwidth is enough to ensure the presence of the familiar tape "hiss" when played through modest or better Hi-Fi systems. Although the mono track width (twice as wide as an audio cassette stereo track) should help the S/N ratio, the slower tape speed does not, as shown in the curves of *Figure 9.* For the SP mode the S/N ratio is approximately 5 to 10 dB lower than the audio cassette and worsens by 3 to 5 dB in the extended play modes. Some "spurs" or "spikes" may be observed at harmonics of the video field frequency (60 Hz) and at the video line scan frequency of 15.734 kHz. The low frequency spikes will not affect DNR operation since the control path sensitivity decreases sharply below 1 kHz, but the presence of the 15.734 kHz component could cause improper sensitivity settings to be obtained. If this is the case, the pilot frequency notch filter for FM, described later, can be retuned by changing the capacitor from 0.015 μF to 0.022 μF.

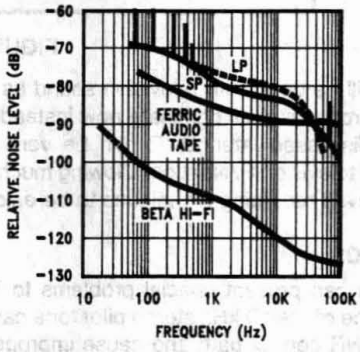

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FIGURE 9. Video Tape Noise Spectrum Levels

Figure 9 also shows the noise spectrum with the new Beta Hi-Fi format. This is clearly superior to both the standard format and audio cassette tapes and is realized by using the two video record/play heads simultaneously for audio, thus taking advantage of the substantially higher relative tape speed. The audio is added in the form of four FM carriers, *Figure 10.* Four carriers are necessary for two audio channels since the azimuth loss between the normal video heads (reducing crosstalk between the heads at video frequencies) is not enough at the lower audio carrier frequencies. Each head therefore uses different carriers for the left and right channel signals.

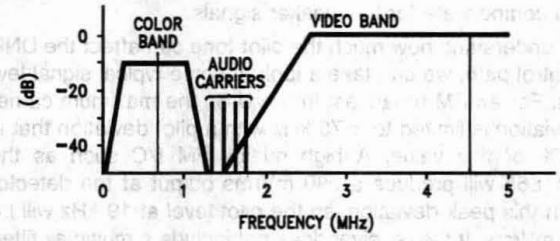

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FIGURE 10. Beta Hi-Fi Carrier Frequencies

A quite different technique is used for VHS Hi-Fi, which is similar to that for 8 mm video. Separate audio heads are mounted on the same rotating drum that is carrying the video heads, but with a much larger azimuth angle compared to the video heads. The sound signal is written deep into the tape coating and then written over by the video signal which causes partial erasure of the audio—about a 10 dB to 15 dB loss. The difference in azimuth angle prevents crosstalk and the much greater writing speed still yields an S/N of over 80 dB.

Both Hi-Fi formats provide excellent sound quality with hardly any need for noise reduction but DNR can still play a role. Conventionally recorded tapes are and will be popular for quite a while, and even with Hi-Fi recording capability much

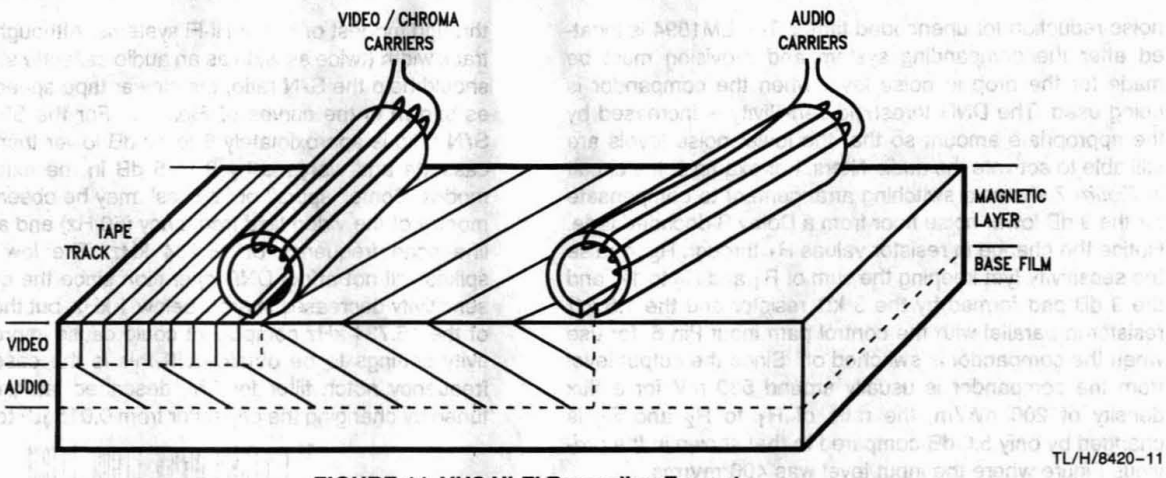

FIGURE 11. VHS Hi-Fi Recording Format

recording will be done with television sound as a source—and the source noise will dominate now instead of the tape noise. As discussed later, DNR can be very effective in dealing with television S/N ratios, allowing much of the benefit of improved recording techniques to be enjoyed.

4. FM RADIOS:

FM sources can present special problems to DNR users. The presence of the 19 kHz stereo pilot tone can be detected in the DNR control path and cause improper threshold settings (the problem is not so much that the 19 kHz tone gives the wrong setting, but that if the threshold is adjusted with the tone present, then the threshold is wrong when the tone is absent—as in a monaural broadcast). Secondly, for FM broadcasts the noise level at the receiver detector output is dependent on the r.f. field strength when this field strength is under 100 μV/meter at the antenna terminal. With a fixed DNR threshold, as the noise level increases with decreasing field strength, the minimum audio bandwidth becomes wider and a loss in noise reduction is perceived. This latter problem occurs primarily with automobile radios where the signal strength can vary dramatically as the radio moves about. For the home receiver, re-adjustment of the DNR threshold setting for an individual station will compensate for the weaker signals.

To understand how much the pilot tone can affect the DNR control path, we can take a look at some typical signal levels. For an FM broadcast in the U.S., the maximum carrier deviation is limited to $\pm$75 kHz with a pilot deviation that is 10% of this value. A high quality FM I/C such as the LM1865 will produce a 390 mVrms output at the detector with this peak deviation, so the pilot level at 19 kHz will be 39 mVrms. If the receiver does not include a multiplex filter, after de-emphasis 4 mV will appear at the inputs to the LM1894. Typically for FM signal noise floors, the resistive divider at Pin 5 will attenuate the pilot by 20 dB leaving 0.4 mVrms at Pin 6. This input level to the LM1894 control path is sufficient to cause the audio bandwidth to increase by over 1 kHz compared to the monaural minimum bandwidth. Of course, if the receiver does have a multiplex filter, which is common in high quality equipment or receivers that include Dolby B Type noise reduction, this problem will not happen, but otherwise we require an extra 15 dB to 20 dB attenuation at 19 kHz. This is obtained with a notch filter tuned to the pilot frequency connected between Pins 8 and 9 of the LM1894. Although a tuned inductor is shown, a fixed coil of similar inductance and Q can be used since with normal component value tolerances ($\pm$7% inductance, $\pm$10% capacitance) the pilot tone will be attenuated by at least 15 dB.

Handling the signal strength dependence of the FM signal noise floor is not quite as easy – at least if pre-set DNR sensitivity settings are used. A look at the quieting curves for an FM radio will show why. At strong signal levels, greater than 1 mV/meter field strength at the antenna, the IF amplifier of the radio is in full limiting and the noise floor is between 60 dB and 80 dB below the audio signal. However, as the field strength starts to decrease below 1 mV/meter, the noise level begins to increase, even though the IF amplifier is still in limiting. Worse yet, since the demodulated output includes the noise from the stereo difference signal channel (L-R), the noise level is increasing more rapidly in the stereo mode than in the monaural mode. By the time the field strength has fallen to 100 μV/m the stereo noise is over 20 dB higher than the equivalent mono noise. If the DNR sensitivity is pre-set such that noise at the $-$45 dB to $-$55 dB level is activating the control path detector, when weaker stations are tuned in the noise level will increase and less noise reduction will be obtained. On the other hand, for stronger stations the noise level will drop below the detector threshold and a possibility exists that high frequency signals will be attenuated. Fortunately this latter occurrence is unlikely with commercial FM broadcasts since substantial signal compression is common, and the relatively high mid-band signals will be adequate enough to open the audio bandwidth sufficiently. In any event, with very strong r.f. signals, the need for noise reduction is minimal and DNR can be switched out.

	FM	TV
L	4.7 mH	4.7 mH
C	0.015 μF	0.022 μF

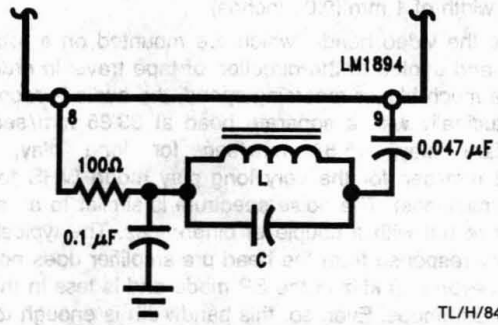

FIGURE 12. Control Path Notch Filter

Recognizing that a fixed threshold setting is necessarily a compromise for FM, the designer can still elect to use a preset adjustment for convenience. The set-up procedure is a little more complicated than for an audio tape source and involves the use of an FM signal generator. The carrier frequency from the generator (between 88 MHz and 108 MHz) is unmodulated except for the stereo pilot tone, and the receiver is tuned to this carrier frequency. Then the carrier level is increased until the stereo demodulator output S/N ratio is that desired for the DNR threshold setting. For example, if the recovered audio output is 390 mVrms for 75 kHz deviation of the carrier frequency, the stereo noise level is 2.2 mVrms for a 45 dB S/N ratio. The generator level is increased until this noise voltage is measured at the demodulator output and the resistive divider at Pin 5 of the LM1894 adjusted correspondingly. A multiplex filter should be inserted between the decoder output and the S/N meter to prevent the pilot tone from giving an erroneous reading. At no time should the pilot tone be switched off since this will allow the decoder to switch into the nomaural mode, decreasing the noise level −65 dB instead. A S/N ratio of 45 dB is chosen since many modern receivers incorporate blending stereo demodulators. As the dashed curve of *Figure 13* shows, when the stereo S/N ratio falls to 45 dB, the decoder starts to blend into monaural operation, thus keeping a constant S/N ratio. The loss in stereo separation that inevitably accompanies this blending is far less objectionable than abrupt switching from stereo to mono operation at weak signal levels.

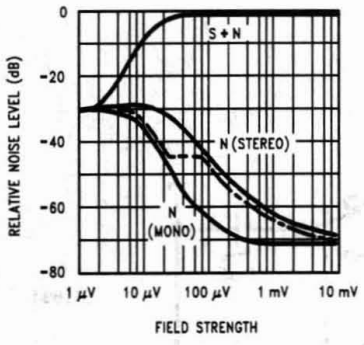

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FIGURE 13. FM Radio Quieting Curves

5. TELEVISION RECEIVERS:

At first it might be thought that television broadcast signals, with an FM sound carrier located 4.5 MHz above the picture carrier frequency, will present the same difficulties as FM radio broadcasts to a DNR system with a pre-set threshold. This conclusion is modified by two considerations. First the TV receiver is unlikely to be mobile and the received signal strength will be relatively constant from an individual broadcast station. Secondly another subjective factor, the picture quality, will largely determine whether the signal strength is adequate enough for the viewer to stay tuned to that station. A representative television receiver will have a VHF Noise Figure between 6 dB and 7 dB such that, with a 75Ω antenna impedance, the picture will be judged noise-free at an input signal level of just above 0.5 mVrms – i.e. a picture signal to noise ratio of 43 dB. Noise will become perceptible to most viewers at a S/N ratio of 38 dB and become objectionable at 28 dB to 30 dB. Therefore 13 dB below 1 mVrms the picture noise is objectionable, and at −25 dB to −30 dB it will probably be totally unacceptable to the majority of viewers. For off-air broadcasts, the audio carrier amplitude is 7 dB to 10 dB below the picture carrier amplitude and for cable services the typical sound/picture carrier ratio is −15 dB. However, due to the FM improvement factor (45.4 dB for equal amplitude carriers compared to the AM picture carrier) audio S/N ratios do not degrade as rapidly as the picture S/N—even with the lower audio carrier amplitudes. *Figure 14* shows the increase in audio noise level as both carrier amplitudes are reduced from the picture carrier level that produces a noise-free picture. When the picture noise is already objectionable the audio noise level has remained virtually unchanged, even for an audio carrier 30 dB below the picture carrier. By the time an unacceptable picture noise level has been reached, the audio noise has increased by less than 3 dB for sound carriers at −10 dB and −20 dB relative to the picture carrier. Therefore it is unlikely that a perceptible increase in noise compared to a strong channel will occur before the viewer switches to another channel.

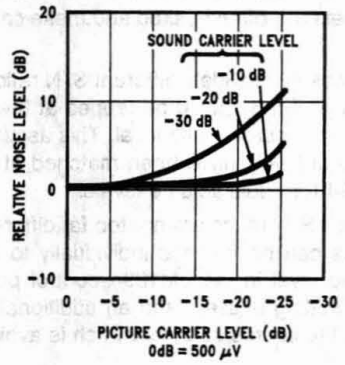

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FIGURE 14. Increase in Audio Noise with Decreasing Carrier Levels

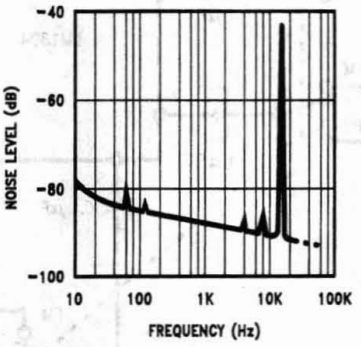

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FIGURE 15. TV Noise Spectrum Level

Figure 15 shows the noise spectrum level of a strong audio carrier (1 mVrms) referred to 7.5 kHz carrier deviation. The standard peak deviation in the U.S. is 25 kHz so that the spectrum level will be 10 dB lower when referred to the peak audio level, meaning that the noise is not much better than the cassette tape noise levels shown previously. Only the relatively small power capability and limited bandwidth of audio amplifiers and speakers in conventional receivers has made this noise level acceptable. Unfortunately for the listener who hooks up the audio to his Hi-Fi system, or buys a new receiver with wider audio bandwidth and high output power (in anticipation of the proposed BTSC stereo audio broadcasts for television), TV sound will exhibit this noise.

Because the noise floor will be relatively constant, a pre-set threshold can be used for the LM1894 control path (although broadcast of older movies with unprocessed and noisy optical soundtracks might increase the received noise), and the only modification to the standard application circuit is to shift the control path notch filter down to 15.734 kHz. This is done with sufficient accuracy simply by changing the 0.015 μF tuning capacitor to 0.022 μF.

Note: The introduction of a stereo audio broadcast (the BTSC-MCS proposal) does not substantially modify the above conclusions, even though dbx noise processing is used. The dbx-TV noise reduction is applied only to the new stereo difference signal channel (L-R) to decrease the *additional* noise intrinsic in the use of an AM subcarrier along with the normal (L+R) monaural channel. This means that the new stereo signal should have roughly the same characteristics as the present monaural signal.

6. MULTIPLE SOURCES:

Multiple sources are best accommodated by keeping the potentiometer in the LM1894 control path and allowing the user to optimize each source. Nevertheless, for convenience, pre-sets are often desired and these can be done in two ways.

1) If the sources have widely different S/N ratios, the resistive divider at Pin 5 should be tapped at the appropriate point for each source noise level. This assumes that the source signal levels have been matched at the input to the LM1894 for equal volume levels.
2) If the source S/N ratios are not too far different, then the input levels can be trimmed individually to produce the same noise level in the LM1894 control path. A single sensitivity setting is used, and an additional switch pole ganged to the source selector switch is avoided.

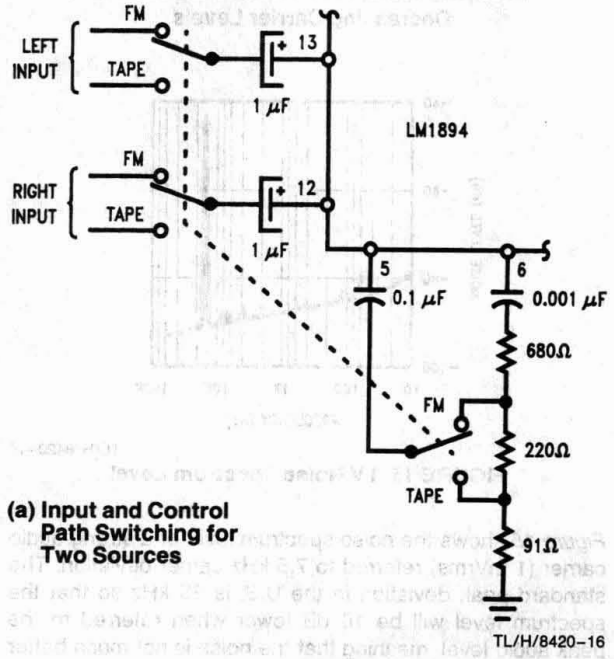
Examples of both arrangements are shown in *Figure 16(a)* and *(b)*. To set up the multiple source system of *16(b)*, the DNR control path sensitivity is adjusted for the source with the *lowest* noise floor. Measure the peak detector voltage (Pin 10) produced by this noise source and then switch to the next source. Adjust (attenuate) the input level of the new source to match the previous Pin 10 detector voltage and repeat this procedure for each subsequent source.

7. CASCADING THE LM1894 AUDIO FILTERS

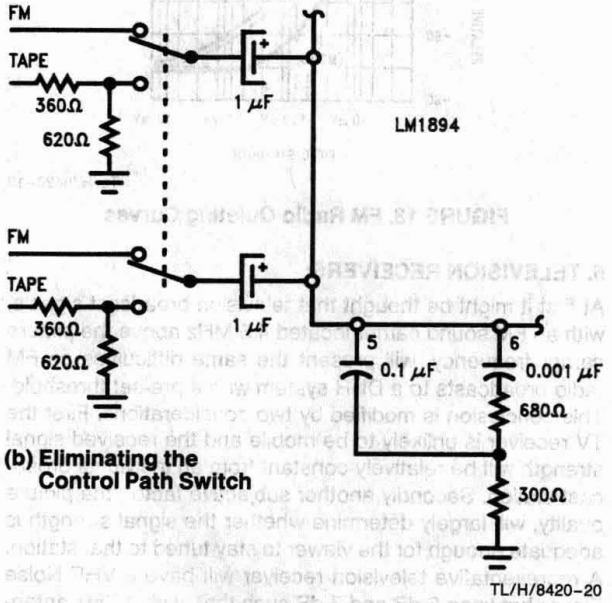
The LM1894 has two matched audio lowpass filters which can be cascaded, providing a single channel filter per I/C with a 12 dB/octave roll-off. This produces slightly more noise reduction (up to 18 dB) but because the steeper filter slope may in some cases produce audible effects on high frequency material, cascaded filters are best used for sources with a relatively restricted h.f. content. When the filters are cascaded the combined corner frequency decreases by 64% according to Equation (6), for n = 2

$$fc = fo\sqrt{10^{0.3/n} - 1} \quad (6)$$

Therefore, to retain the original frequency range, the capacitor values must be reduced by the same factor to 0.0022 μF. One of the audio outputs is connected over to the other audio filter input and the summing amplifier in the control path is by-passed by moving the 0.1 μF coupling capacitor from Pin 5 over to the single audio input. If the audio source is unable to drive the 1 kΩ impedance of the control path input network, this can be scaled up by using a 0.01 μF capacitor and a 10 kΩ potentiometer.



(a) Input and Control Path Switching for Two Sources



(b) Eliminating the Control Path Switch

FIGURE 16. Multiple Programme Source Switching

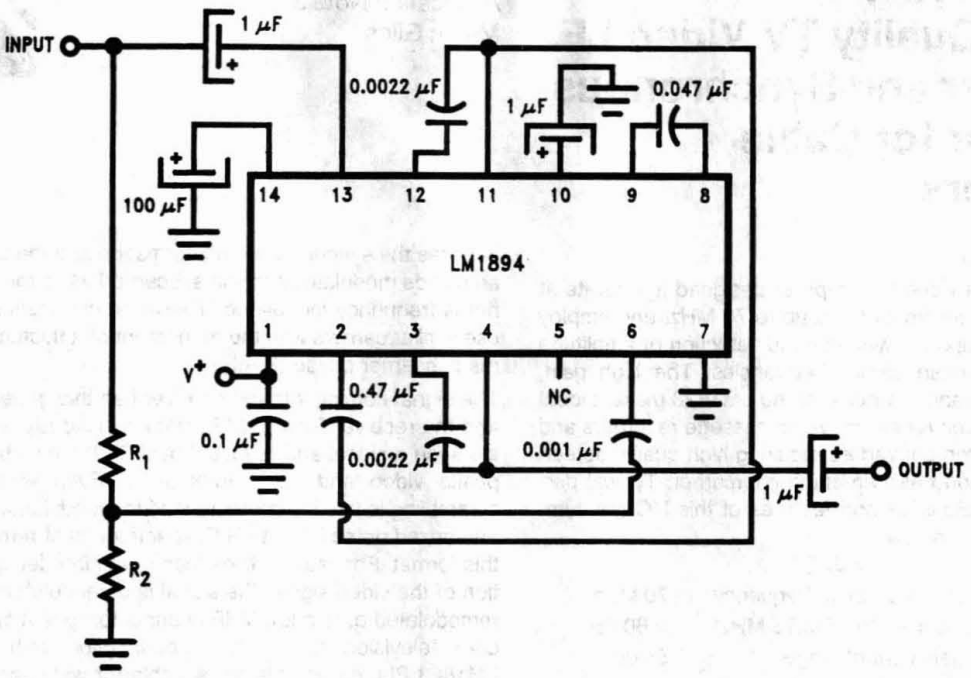


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FIGURE 17. Cascading the Audio Filters of the LM1894

The LM1823: A High Quality TV Video I.F. Amplifier and Synchronous Detector for Cable Receivers

National Semiconductor
Application Note 391
Martin Giles

INTRODUCTION

The LM1823 is a video I.F. amplifier designed to operate at intermediate carrier frequencies up to 70 MHz, and employ phase locked loops for synchronous detection of amplitude modulation on these carrier frequencies. The high gain, wide AGC range and low noise of the LM1823 make it ideal for use in television receivers, video cassette recorders and in cable TV set-top converters requiring high quality detected base-band video and an audio intercarrier. Typical performance characteristics and features of this I/C are summarized in Table I below.

TABLE I

Maximum system operating frequency	70 MHz
Typical I.F. amplifier Gain (45.75 MHz)	>60 dB
I.F. amplifier gain control range	55 dB
True synchronous detector with a PLL	
Detector conversion gain	34 dB
Detector output bandwidth	9 MHz
Detector differential gain	2%
Detector differential phase	1 degree
Noise averaged AGC system	
Internal AGC gated comparator	
Reverse tuner AGC output	
DC controlled video detection phase	
AFC detector	

THE R.F. SIGNAL FORMAT

Despite the wide variety of signal sources available to the home television receiver—broadcast, cable, satellite, video games etc.—on channel carrier frequencies from 55.25 MHz to 885.25 MHz, the spectral content of each R.F. channel has been established for many years. In the United States the channel bandwidth is fixed at 6 MHz with the picture carrier located 1.25 MHz from the lower end of the band, and an aural carrier placed 4.5 MHz above the picture (pix) carrier. Introduction of color television in the early fifties added another carrier, the chroma sub-carrier, positioned 3.58 MHz above the pix carrier frequency. The pix carrier is amplitude modulated* by the baseband video signal (which includes the synchronization information and the phase and amplitude modulated chroma subcarrier) while the aural carrier is frequency modulated. Television channels in Europe use similar carriers with the refinement of a fluctuating chroma subcarrier phase (P.A.L.).

The signal coming into the receiver has this general format and the receiver R.F. and I.F. circuits are designed to handle such a signal and reduce it back to the baseband composite video and audio intercarrier. Even where signal scrambling is used to protect the video modulation from unauthorized detection, the R.F. spectrum must remain within this format. For satellite broadcasts with frequency modulation of the video signal, the signal is demodulated and then remodulated onto a low VHF channel for reception by standard television receivers. In connection with this, the LM1823 PLL detector is not suitable for wide-band FM detection—even though the I.F. carrier (70 MHz) is well within the LM1823 I.F. amplifier frequency capability.

Notice again that the pix carrier is located at one end of the occupied bandwidth and only the upper sidebands are being fully transmitted. The lower sidebands are truncated with only frequencies close to the pix carrier frequency modulating the carrier. This method of conserving the frequency spectrum is referred to as vestigial sideband transmission.

* A more appropriate term is "negative downward modulation" since any modulating signal causes a decrease in the peak carrier amplitude (compared to conventional a.m., where the modulating signal alternately increases and decreases the peak carrier level with the mean carrier level remaining constant). For television carriers, syncs correspond to peak carrier and increasing brightness causes decreasing carrier amplitudes.

THE CABLE CONNECTION

Originally introduced many years ago as a means for providing broadcast TV to isolated areas or where the terrain made direct reception difficult, cable TV had modest growth in the U.S. and was a stagnating industry until the mid-seventies. Lower cost satellite earth stations were the turning point, allowing cable operators access to many varied program sources from any part of the country.

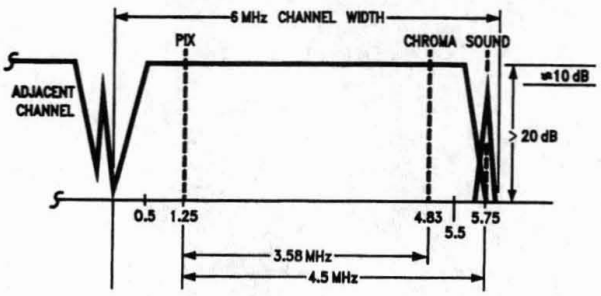

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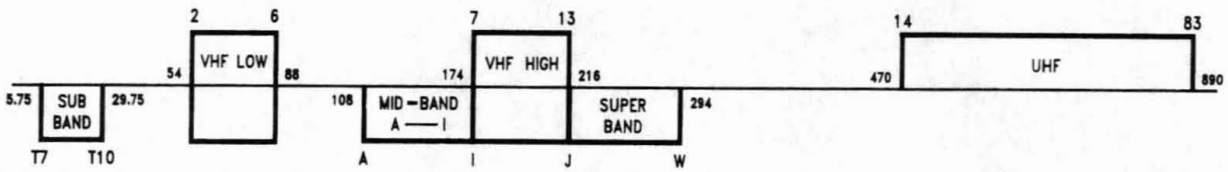
FIGURE 1. U.S. Broadcast Channel Spectrum

Broadcast Channel Frequency Allocations



Cable Channel Frequency Allocations

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FIGURE 2. Broadcast and Cable Bands in the U.S.

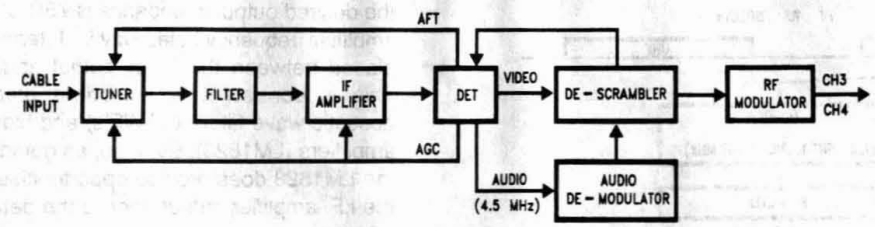

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FIGURE 3. Cable Set-Top Converter Block Diagram

Standard television receivers in the U.S. tune to VHF channels 2 through 13 and UHF channels 14 through 83, and initially cable operators used the 12 VHF channels for their program material. With increased sources soon all channels were occupied on some systems creating significant demands on television tuner and I.F. amplifier strips. More space yet was needed and rather than using UHF channel allocations starting at 470 MHz because of cable signal attenuation (typically 0.8 dB/100 ft. at 300 MHz), operators turned to the unused spectrum space between VHF channel 13 and UHF channel 14. Naturally, since standard TV receivers could not tune to these channels, the set-top converter came into being. Each of the new channels could be converted to a low VHF channel to be received on the standard TV. Television manufacturers responded, and with the common introduction of varactor tuners were soon able to offer "cable ready" televisions capable of tuning to all the new cable frequencies. This meant that customer conveniences such as remote control of channel selection also became available. Unfortunately it aggravated a problem already confronting the cable operator. Since standard television receivers couldn't tune to the cable channels, operators had been able to offer premium services on some of these frequencies, paid for by subscribers who rented the appropriate set-top converter box. This didn't prove very secure since one operator's "free" channel was another operator's "pay" channel, and the introduction of cable-ready televisions ensured the eventual demise of such systems.

Scrambling the signal, a technique already being used by over-the-air subscription television, has become common in the cable service. The degree of scrambling* is limited since the scrambled signal spectrum must remain within the channel allocation and anything done to the signal must be subsequently undone without noticable degradation of the signal.

Generally for television, scrambling means a pulse or sine wave suppression of the signal horizontal blanking pulse interval so that the sync-tips occur between the black and white levels instead of always below black level. The standard television sync separator does not function well with this signal and the I.F./tuner AGC circuits will not work properly, effectively scrambling the displayed picture. Other techniques include random inversion of the video information to provide an even greater degree of security.

The means used to encode such a scrambled signal gives rise to the terms "in band scrambling" and "out of band scrambling". With cable ready television receivers capable of tuning to the scrambled channel, the decoder can be a simple broad-band gain switch (to change the signal R.F. amplitude during horizontal blanking) with a separate receiver tuned to the decoding data carrier frequency, which is located outside the signal channel. This permits use of the television receiver in a normal way but does require simultaneous switching of the decoder receiver with channel changes.

Also, spectrum space must be reserved for each scrambled channel's data carrier.

A more popular method of scrambling is "in band scrambling" where the data carrier to decode the signal is included inside the transmitted signal channel, usually within the aural carrier. Any number of channels can be scrambled and now different levels of service can easily be added or deleted without the need to rewire the decoder box. This is achieved by including time multiplexed binary "tags" along with the sync information so that special programs can be identified. Individual subscriber boxes can be similarly addressed and turned on or off by the cable operator. In these types of systems, the LM1823 and LM2889 have obvious applications. The LM1823 is able to provide an excellent baseband signal inside the decoder box, which signal is then remodulated on a low VHF channel carrier by the LM2889 for retransmission to the standard television receiver. Clearly, the highest possible performance is desireable to prevent any noticeable difference between a converted channel, whether scrambled or not, and a regular off-air broadcast channel. (For a complete description of the LM2889 modulator I/C see AN402).

THE RECEIVER FRONT-END

The typical receiver front-end consists of a tuner, I.F. amplifier, I.F. filters and a video/sound intercarrier detector stage. These circuits are designed to provide a number of functions:

1) Select (tune) a specific R.F. channel in a band of frequencies.
2) Provide rejection to adjacent and other channels in the band.
3) Amplify low level R.F./I.F. signals prior to detection of the modulation.
4) Avoid overload on high level R.F. signals.
5) Trap or attenuate specific frequencies within the channel bandwidth to ensure a proper detected frequency response is obtained.
6) Linearly demodulate all desired modulating frequencies on the carrier.
7) Produce a noise-free video signal at the detector.
8) Provide automatic gain control (AGC) to compensate for changing signal strength at the receiver input.
9) Provide automatic frequency control (AFC) to the tuner local oscillator (L.O.) to maintain the carrier intermediate frequency (I.F.).

N.B. Items 8) and 9) have previously been provided in part by circuits external to the conventional I.F. amplifier. However, these functions are completely included with the LM1823 leading to overall performance improvements and reduction in external parts count and cost.

*Other security techniques such as jamming or trapping are used but since jamming is easy to defeat and trapping requires removal or replacement of filters in the cable drop to individual subscribers, scrambling the signal is receiving a lot more attention.

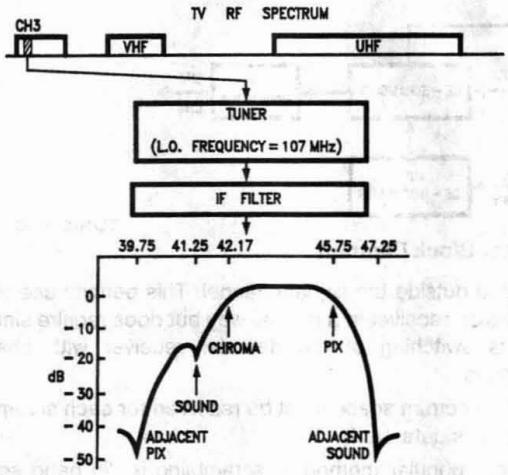

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FIGURE 4. R.F. Tuning and I.F. Conversion (Note High Side L.O. Reverses the Relative Position of the Picture Chroma & Sound Carriers. c.f. *Figure 1*).

Although we are not directly concerned with the tuner design in this application note, it is useful to understand the design goals and constraints on the tuner for at least two reasons. First, since the tuner and I.F. amplifier interact very closely to obtain and maintain a noise-free picture, we need to know something about the tuner in order to provide the correct gain distribution and AGC action. Second, when the two functions are finally placed together, we need to know where to look to solve visible problems that may have become apparent. In some instances, either the tuner or the I.F. amplifier may be at fault, and a good understanding of the system interaction is needed to ensure that the appropriate action is taken.

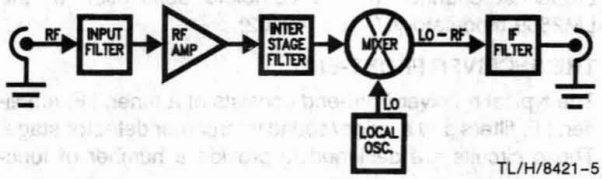

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FIGURE 5. Typical Single Conversion Tuner

Both single conversion and double conversion techniques are used in cable converter tuners. The single conversion type is similar to the conventional TV receiver tuner and consists essentially of an R.F. stage, mixer stage, and local oscillator. Usually some input filtering is done to help match the cable to the input device and provide some rejection to unwanted signals outside the operating channel. Further rejection to unwanted signals, such as the I.F. frequency radiated back from the I.F. amplifier, is accomplished with interstage filtering between the R.F. amplifier and the mixer, and finally an output filter matches the mixer output to the cable feeding the I.F. amplifier. For convenience, we are assuming the desired output impedance is 75Ω and that the major I.F. amplifier frequency selectivity is determined by a block filter placed between the tuner output and I.F. amplifier input. This is consistent with modern practice using surface acoustic wave filters (SAWF's) and high gain stabilized I/C amplifiers (LM1823). Even so, as noted in more detail later, the LM1823 does provide opportunities for more filtering at the I.F. amplifier output prior to the detector stage.

Dual conversion tuners have been popular for a number of years and use first L.O. frequencies that are above the input R.F. bandwidth, avoiding problems with L.O. leakage back onto the feed cable. The second L.O. and mixer convert the high first I.F. to a Ch 3 or Ch 4 carrier for reception by the TV receiver. The addition of PLL's to control the first L.O. and descrambling networks on the R.F. output have added sufficient complexity to such converters that they are now called "set-top terminals". Also, since the scrambling techniques have become more sophisticated the signal is now frequently converted down to baseband before decoding and remodulation on Ch 3 or Ch 4 carriers. The high first I.F. has the advantage that image signal rejection is achieved without the switchable filters necessary at the input to the single conversion tuner. However, the absence of these filters does mean that care must be exercised to avoid generation of intermodulation products that "talk back" onto the cable (up conversion of the R.F. signal has been proposed as a way to minimize intermodulation components). Another disadvantage of the dual conversion tuner shown in *Figure 6* is that it typically has a very high Noise Figure, often between 14 dB to 16 dB. This is because the signal is applied directly to the first mixer which is a passive, double balanced diode mixer. As discussed in more detail later when we look at SAWF's between the tuner and the I.F. amplifier, a pre-amp in front of the mixer can improve the N.F. to 6 dB to 8 dB, especially in a baseband converter where an AGC voltage is available to help the tuner handle the input signal strength range.

Returning to the single conversion tuner, the major parameters to be considered are as follows:

1) Power gain
2) Noise Figure
3) Good Cross-Modulation rejection
4) VSWR
5) AGC Range
6) Impedance changes with AGC
7) Overload capability
8) Channel 6 beat rejection
9) Curve tilt (tracking)
10) L.O. drift and radiation

For an I.F. amplifier design, items 1), 2), 7), and 8) are the most significant, but if the tuner designer has overlooked the others we may see some problems when the tuner and I.F. amplifier are hooked together.

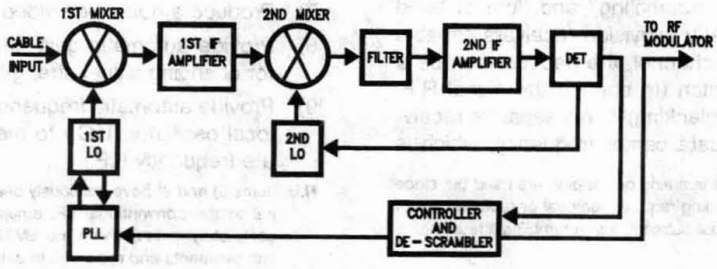

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FIGURE 6. Dual Conversion Tuner

Crossmodulation describes the condition wherein the modulation information on an adjacent channel (usually) is transferred on to the desired carrier. A typical specification is the undesired carrier level with 30% modulation needed to cause 1% modulation of the desired carrier level.

Crossmodulation is particularly likely to occur in cable systems and is usually observed as sync bars drifting through the picture. In particularly severe cases the interfering picture can actually be seen. High signal levels at the input of the mixer are a frequent cause of crossmodulation, particularly when high gain R.F. stages are used to obtain a low tuner noise figure (N.F.). But when AGC is applied the crossmodulation source often shifts to the R.F. device.

When overload occurs, (measured as the total harmonic distortion of a specified modulation frequency), the peaks of the R.F. carrier waveform become compressed and this will show up at the video detector as a smaller sync pulse amplitude (sync tip to black level). Since the AGC system operates on the sync tip level the effective result is that the black level appears to go blacker than black—i.e. some near black information will be lost and the picture will appear to have too much contrast. Alternatively if the subsequent receiver circuits have black level restoration the screen brightness increases and picture tube blooming on peak whites may occur. As overload increases there is a strong chance that vertical sync will be lost. Generally the tuner mixer device is the first stage to overload, followed by the R.F. stage. While overload is caused by very strong signal strengths and therefore may appear to be of limited concern it can also occur at weak to intermediate signal strengths because of incorrect AGC threshold settings and this will be discussed in detail later.

Channel 6 beat is a phenomenon related to mixer overload and occurs because of the choice in the U.S. of 45.75 MHz as the intermediate frequency. On channel 6, mixing of the sound and pix carriers produces a signal at 171 MHz which is then mixed with the channel 6 L.O. frequency to give 42 MHz. The I.F. sound and pix carriers can also mix with the channel 6 L.O. to produce 42 MHz. Since 42 MHz is only 170.455 kHz from the I.F. chroma subcarrier of 42.17 MHz, after detection wavey lines will appear in colored areas of the picture. Turning down the receiver color level (saturation) control will eliminate the 170 kHz pattern and identify the problem as Channel 6 beat.

Curve tilt or tracking refers to the ability of the tuner filters to track the L.O. frequency as the channel selection is changed. Problems in this area are easily identified at the video detector output (sometimes referred to as the 2nd detector) since the effect is to cause changes in the relative amplitudes of the pix, sound and chroma carriers compared to that expected from the I.F. filter response. When the detector VCO and AFT circuits of the LM1823 are aligned to 45.75 MHz, the chroma burst located on the back porch (or breezeway) portion of the horizontal blanking period in the video signal will normally be −6 dB compared to the sync pulse amplitude. If mistracking is causing a loss of high frequencies on certain channels, the burst amplitude will be lower on these channels and the picture (in severe cases) will have watery and noisy colored areas with smeared off picture detail. When the loss occurs down at the pix carrier frequency, the burst amplitude is increased and the picture will become harsh with excessive overshoots.

Similar problems can occur on any specific channel simply due to mis-tuning or L.O. drift. In particular, as the L.O. frequency drifts high and the chroma subcarrier amplitude increases, the sound carrier also increases and chroma/sound beats will appear in the picture. In the U.S. the chroma/sound carrier beat is at 920 kHz (4.5 MHz—3.58 MHz) and appears as a herringbone pattern while the audio modulates the sound carrier. This 920 kHz beat can also be caused by detector non-linearities, and after the video detector by the detected 4.5 MHz sound intercarrier mixing with the chroma subcarrier in subsequent receiver stages. If turning down the color level control removes the 920 kHz beat then a better 4.5 MHz trap is needed at the video detector output.

These preceding comments are not meant to imply that the tuner is the root cause of all the nasty phenomenae that can be observed in the picture display. Overload, Channel 6 beat and video noise are very dependent of the tuner/I.F./AGC interaction. To understand why this is the case, we need to look at the demands that the input signal field strength puts on the system.

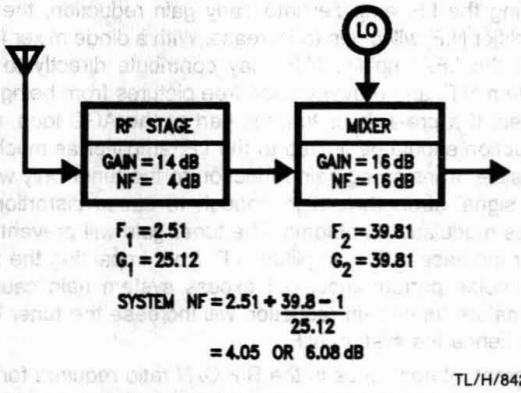

FIGURE 7. Typical Tuner Gain and Noise Figure

INPUT SIGNAL LEVELS

The smallest input signal is, of course, no signal or simply the noise level generated at the cable drop. To this noise level will be added the input noise of the tuner itself, giving rise to an equivalent noise input defined by the tuner noise figure (N.F.) While a specific design will have to take into account the actual operating parameters of the tuners available, we will assume a typical tuner configuration with an R.F. stage providing 14 dB gain and having a 4 dB N.F., followed by a mixer stage with 16 dB conversion gain and a 16 dB N.F. The N.F. of this combination is 6 dB, a fairly typical number, which will have the effect of increasing the actual input noise by a factor of 2. If our noise source is the cable impedance with a real part of 75Ω, at an ambient temperature of 290k, then the equivalent input noise is 2.2 uVrms (the noise contribution of any matching network or cable termination is ignored as this is included in the tuner N.F.).

Cable signal levels run from −6 dBmV to +15 dBmV with a typical system goal of maintaining a C/N ratio of at least

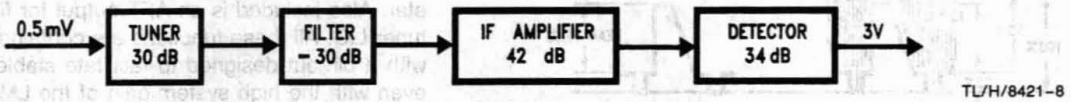

FIGURE 8. System Gain Distribution

43 dB at the cable drop to the subscriber. If a 0.5 mVrms signal is to produce the rated detector output of 3V (o–p)* for the LM1823 then we need a total system gain of at least 75 dB. Usually the SAWF connected between the tuner output and the I.F. input will have an insertion loss of 20 dB to 30 dB so that with the 30 dB tuner gain, the I.F. amplifier/detector is required to provide the remaining 76 dB. If the tuner is simply a diode mixer with a 6–8 dB insertion loss, the gain requirement increases to 114 dB.

*(o–p) means the detected zero carrier voltage level to the detected sync tip voltage level. The actual peak white signal to sync tip excursion at the detector will be 87.5% of this—2.63V (p–p). In the absence of a carrier, thermal noise will be present with amplitude peaks on both sides of the detected zero carrier voltage.

Fortunately the LM1823 has a high conversion gain detector (34 dB) and the I.F. amplifier gain can be set to well over 75 dB at 45.75 MHz (but we will see that some gain prior to the I.F. amplifier filter will be necessary if a good system N.F. is desired). Substantially more gain than necessary should be avoided however, even though there is plenty of AGC range in the I.F. amplifier (from 48 dB to 60 dB depending on external components). While at least 22 dB AGC capability is needed to accommodate the expected input signal strength range, if excessive system gain is used, forcing the I.F. amplifier into early gain reduction, the I.F. amplifier N.F. will begin to increase. With a diode mixer front end, the I.F. amplifier N.F. may contribute directly to the system N.F. and prevent noise-free pictures from being obtained. If a pre-amp or tuner is part of the AGC loop, gain reduction should be limited to the I.F. amplifier as much as possible, transferring gain reduction to the tuner only when the signal strength is high enough to cause distortion or cross modulation problems. The tuner gain will prevent the prior increase in I.F. amplifier N.F. from impacting the system noise performance, but excess system gain causing premature tuner gain reduction will increase the tuner N.F. and hence the system N.F.

Of great interest to us is the R.F.C/N ratio required for the detected output to be considered noise free. Actual television video S/N ratios are a little complicated by the fact that the displayed video signal does not occupy the full R.F. carrier envelope. 25% of the carrier is reserved for the synchronizing pulses and 12 ½% is retained even under conditions of peak white modulation, for the benefit of intercarrier sound detectors. A common definition of the video S/N ratio is the ratio measured in decibels of the peak video signal amplitude to the r.m.s. noise voltage amplitude. In this context peak video refers to the voltage excursion between black and white levels (from 75% peak carrier to 12½% peak carrier). With this definition in mind, it is generally accepted that the subjective effect of imperceptible noise occurs at an S/N ratio of 43 dB. Noise will become perceptible (for most viewers) at an S/N ratio around 38 dB; is clearly visible but not necessarily disturbing at 34 dB and becomes objectionable at 28 dB to 30 dB. Alternatively if we measure the signal amplitude as an r.m.s. sine wave with the same peak to peak amplitude as the R.F. carrier during the sync pulse period, our signal is free of noise for a 47 dB C/N ratio.

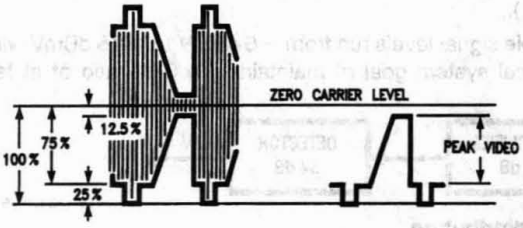

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FIGURE 9. Television R.F. Modulation Envelope

If the input signal were completely noise-free (i.e. no excess noise from head-end amplifiers etc.) then the detected C/N ratio is determined by the equivalent input noise level of the tuner—2.2 uVrms for a 6 dB N.F. With a minimum signal level of 0.5 mVrms the detected C/N ratio will be 47 dB for the converter alone. When the actual signal has noise, for a cable C/N ratio of 43 dB the noise detected at the converter output is now

$$e_n = 10^{-6}\sqrt{(2.2)^2 + (3.5)^2} = 4.13\ \mu V$$

This gives a detected C/N ratio of 41.6 dB, a loss of 1.3 dB compared to the original signal. For most viewers this is the just perceptible level for video noise. On the other hand, if a 14 dB N.F. converter is used, the detected C/N is 32.7 dB which is considered objectionable. A 0 dBmV signal would produce 38.7 dB C/N ratio which would be acceptable. Obviously a low N.F. is important, and any increases in N.F. should be carefully controlled to get the best picture quality possible. *Figure 10* shows the change in N.F. for the LM1823 I.F. amplifier. For over 30 dB gain reduction, the N.F. is unchanged and increases by only 4 dB for the next 20 dB of gain reduction.

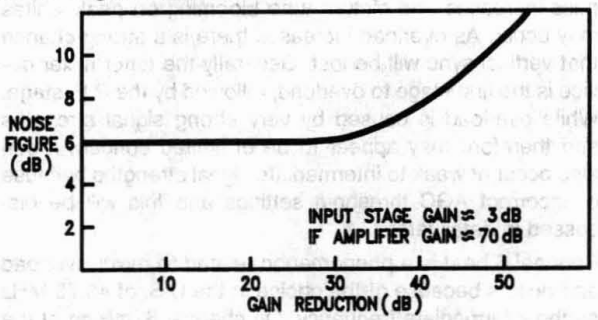

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FIGURE 10. Increase in I.F. Amplifier N.F. with Gain Reduction

LM1823-GENERAL CIRCUIT DESCRIPTION

The basic arrangement of the LM1823 is shown in *Figure 11*. A five stage I.F. amplifier provides gain with a low impedance input stage to ensure adequate suppression of triple transit echo in SAW filters, and AGC on the three interstages. The output stage buffers the I.F. signal which is split off into two paths. A linear path takes the modulated signal to a true synchronous detector while a high gain limiter amplifier passes the I.F. carrier waveform to a second phase detector which is part of the PLL for the VCO. The PLL has an externally adjustable filter and locks the oscillator in quadrature with the incoming I.F. carrier. An in-phase component of the oscillator also drives the linear path detector to recover the signal amplitude modulation. An external DC control allows fine adjustment of the detection phase in order to optimize the detector linearity. The output from the detector is coupled back into the AGC comparator input, and is internally gated during the sync pulse period for good nose immunity and a fast response. Two AGC voltages are available; an early AGC for the I.F. amplifiers and a late, or delayed AGC for the tuner. The take-over point between the I.F. AGC and the tuner AGC is set by an external potentiometer. Also included is an AFT output for fine control of the tuner L.O. All these functions are contained in a 28-pin DIP with a pin-out designed to facilitate stable p.c.b. layouts—even with the high system gain of the LM1823 at frequencies up to 70 MHz.

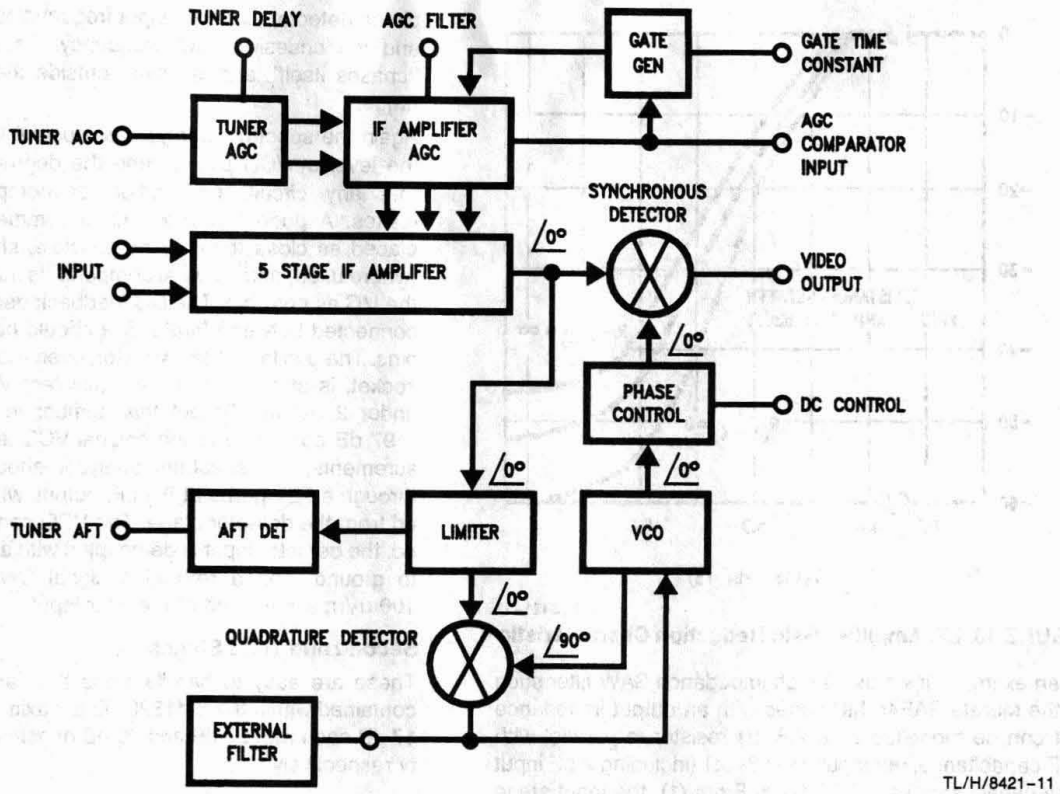

FIGURE 11. Block Diagram of the LM1823

I.F. Amplifier Stages:

The LM1823 I.F. amplifier is composed of five separate stages designed to provide high gain primarily in the frequency range of 35 MHz to 60 MHz, and gain control over a 60 dB range without overload of any stage and without introducing excess noise into the signal.

To achieve this, AGC is applied to the second through fourth stages by a control voltage that is either internally generated from the video detector output or from an externally applied bias voltage at Pin 13. AGC action starts when the voltage at Pin 13 reaches approximately 4 VDC and over 50 dB of gain reduction is obtained by the time Pin 13 voltage reaches 6.5 VDC. For a typical application, the I.F. noise figure is around 6 dB for the first 30 dB of gain reduction, and then begins to increase to above 10 dB by the time the amplifier is gain reduced over 50 dB (see *Figure 10*).

As mentioned earlier, the total system gain desired from the I.F. amplifier input to the video detector output needs to be selected for a specific set of tuner parameters and I.F. filter losses. Excess gain simply means premature AGC action with possible loss of optimum video S/N ratios. To see how and where the LM1823 gain can be adjusted, we will look at each gain stage in turn.

Input Stage:

The input stage is a common-base differential amplifier designed to give good rejection of unwanted I.F. output and detector VCO signals that may be radiated back to the input. The low input impedance of 60Ω ensures that SAW filters are terminated sufficiently to keep the TTE better than 40 dB below the signal level, even with low impedance SAWF's. Because it is a common base stage, the input stage gain is determined by the source impedance presented to the input. An approximate expression for the gain is given by Equation (1)

$$Av = 531/(Zs + 60) \quad (1)$$

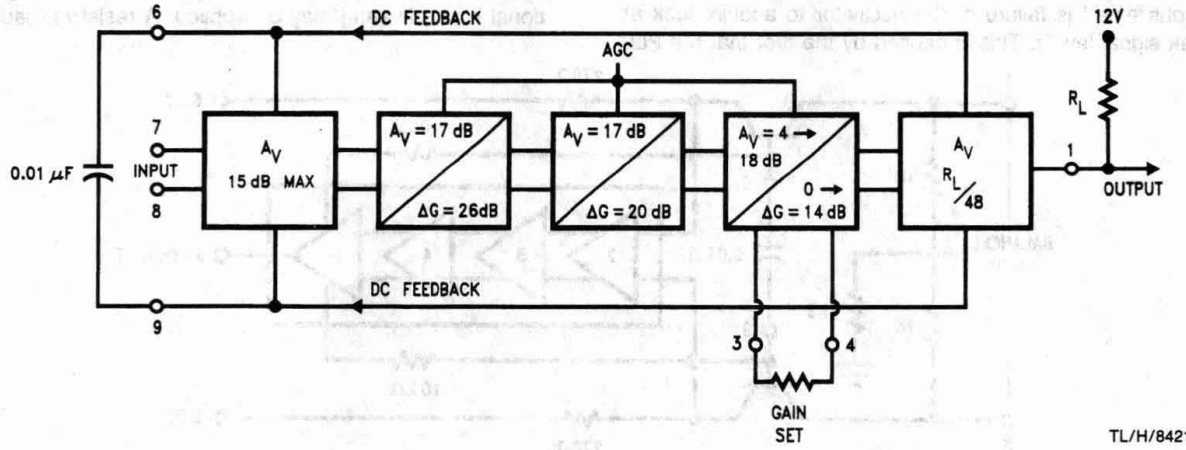

FIGURE 12. Gain Distribution in the I.F. Amplifier

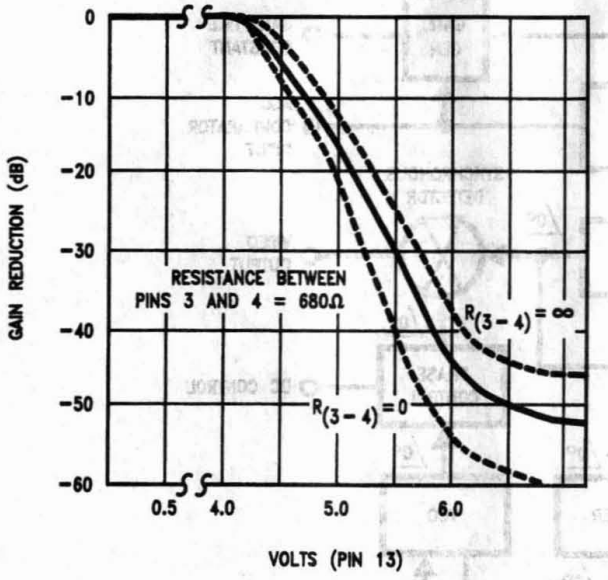

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FIGURE 13. I.F. Amplifier Gain Reduction Characteristic

As an example, if we use a high impedance SAW filter such as the Murata SAF45 MC series with an output impedance that can be modelled as a 2.8 kΩ resistor in parallel with 8 pF capacitance, our input Zs is 345Ω (including 2 pF input stray capacitance) at 45.75 MHz. From (1), the input stage gain is 2.4 dB. If a filter is used that matches to the input stage with 60Ω, then the gain can be as much as 13 dB.

A balanced input is extremely important since the input leads Pins 6–9 are the most sensitive parts in the system to unwanted I.F. coupling. For example, if the I.F. output couples into these pins it can cause changes in the frequency response and can easily promote oscillation. A spectrum analyzer is invaluable for helping determine the system susceptibility to this phenomenon. With the input terminated by the I.F. filter (or an equivalent resistor), the I.F. amplifier output noise spectrum will show if oscillation is likely to occur.

Another signal that can appear at the input is the detector local oscillator waveform. Unlike quasi-synchronous detectors, the LM1823 has a constant (and relatively high) oscillator signal for good linear detection, even with low input signal levels. It is the balance between the input pins to the VCO radiation pick-up that will determine whether the p.c.b. layout is good enough. VCO pick-up can cause AFC skewing and assymetrical oscillator pull-in, but probably the most serious effect is failure of the oscillator to acquire lock at weak signal levels. This is caused by the fact that the PLL phase detector sees two input frequencies—the desired I.F. and the undesired L.O. frequency. As a result the L.O. "chases itself" and is driven outside the loop acquisition range.

Again the spectrum analyzer is a useful tool for measuring the level of VCO pick-up and the degree of improvement that any circuit modification or component relocation makes. A good layout will have symmetrical input leads placed as close together as possible, shielded input coils (where used) and external components mounted as close to the I/C as possible. The DC feedback decoupling capacitor connected between Pins 6 & 9 should be right against the pins. The pcb layout shown later, even though it uses an I/C socket, is able to keep the equivalent VCO input level to under 2 uVrms. To put this number in perspective, it is −97 dB compared to the original VCO level. For the measurements, the spectrum analyzer should be connected through a FET probe at the I.F. output, which is disconnected from the detector stage. The VCO control pin is grounded, the detector input is de-coupled with a 0.01 uF capacitor to ground, and a reference signal CW of the order of 100 uVrms is applied at the filter input.

Second and Third Stages

These are easy to handle since they are completely self contained within the LM1823. The maximum gain is fixed at 17 dB each with 26 dB and 20 dB of gain reduction capability respectively.

Fourth Stage

Unlike the preceding stages, the emitters of the fourth differential amplifier are available at Pins 3 & 4. An internal resistance of 1360Ω between these pins sets the minimum stage gain at 4 dB, and under these conditions (Pins 3 & 4 open) the stage does not provide significant gain reduction with AGC action. However, when an external resistor is connected between the emitters, the gain increases. For Pins 3 & 4 shorted together the gain is as much as 18 dB and the stage can provide up to 14 dB gain reduction with AGC action. Because of the way in which the total I.F. amplifier gain reduction is shared between the stages, the effective gain increase obtained by a resistor between Pins 3 & 4 occurs only for signals below the AGC threshold. After 20 dB of system gain reduction the fourth stage is fixed at 4 dB.

Fifth Stage and I.F. Amplifier Output

The fifth and final I.F. amplifier stage has a single-ended output. There is no internal connection to the detector stage, permitting convenient isolation of the IF amplifier and detector functions. Pin 1 is also a point at which any additional signal filtering may be applied. A resistive load con-

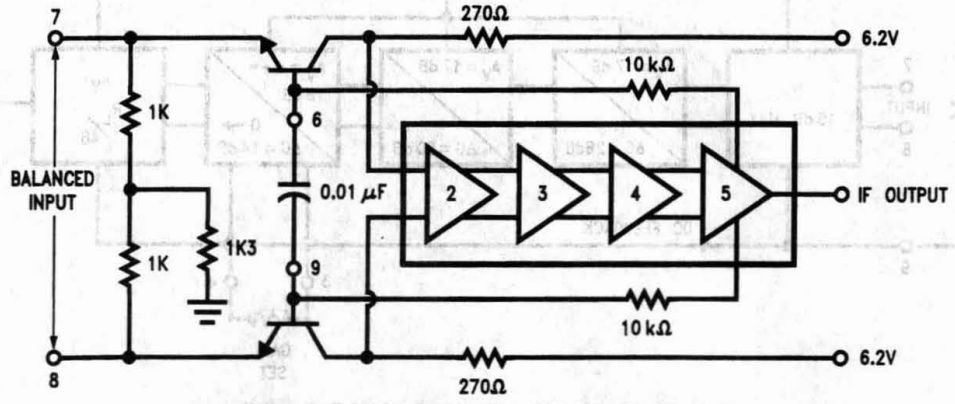

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FIGURE 14. Low Impedance Common Base Input Stage

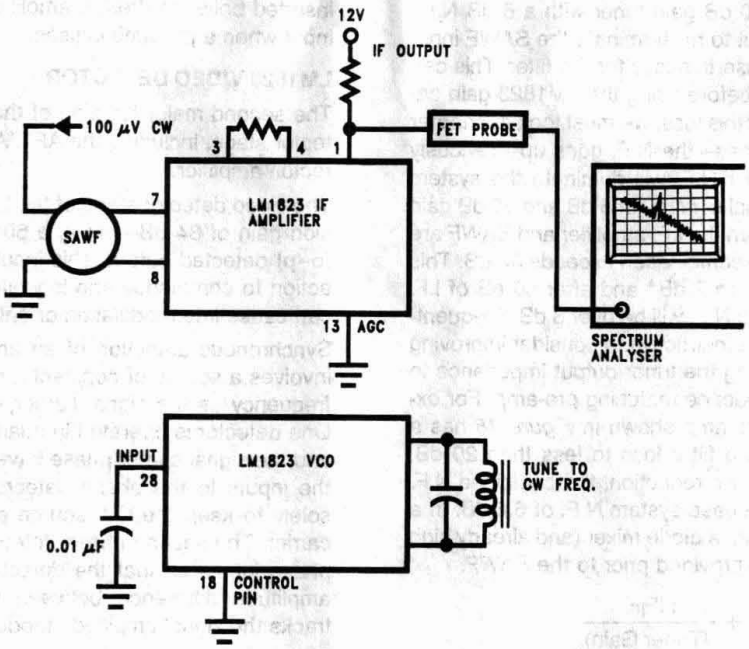

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FIGURE 15. Checking the pcb for Excess VCO Pick-up

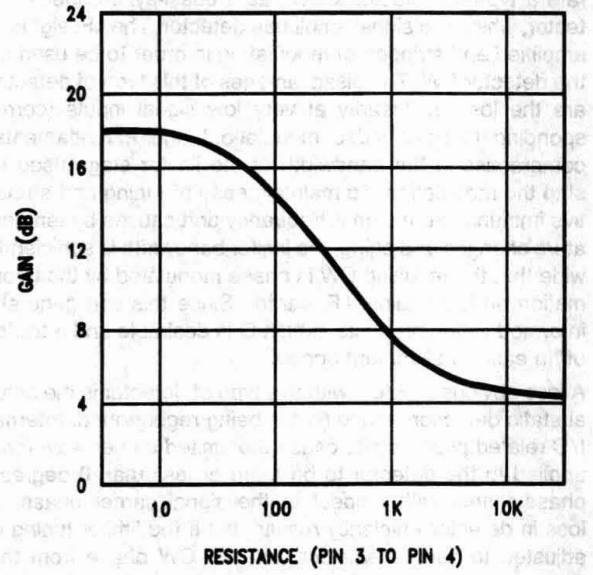

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FIGURE 16. Fourth I.F. Amplifier Stage Gain with External Resistor

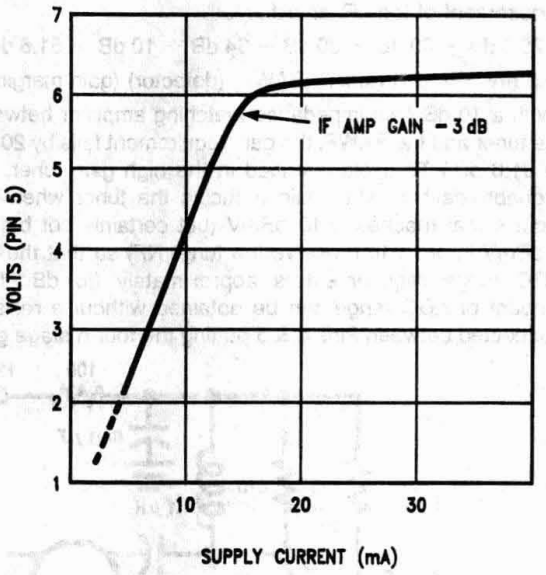

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FIGURE 17. I.F. Amplifier Voltage Regulator Current Requirement

nected to the 12V power supply can be used, but the maximum value is limited in practice to less than 500Ω at intermediate frequencies because of stray p.c.b. capacitance and the loading of the detector stage input impedance of 3 kΩ. The stage gain for a total load impedance of Z is given by Equation (2)

$$AV = 1Z1/48 \quad (2)$$

The last part of the I.F. amplifier concerns the power supply input at Pin 5. This is a shunt regulated input with a nominal value of 6.3V and the I.F. amplifier current is delivered through a dropping resistor from the 12V rail supplying the remainder of the I/C. The 0.01 μF ceramic r.f. decoupling capacitor at Pin 5 should be grounded through very short leads—preferably on the copper side of the p.c.b. A nominal current level into Pin 5 is 32 mA, set by a 180Ω resistor. This current should not exceed 60 mA and the minimum current is about 20 mA, below which the I.F. amplifier will start to lose gain as Pin 5 voltage drops below the regulated level.

SELECTING THE I.F. GAIN

Clearly the LM1823, with all the gain provided by five I.F. amplifier stages and with 34 dB detector conversion gain, has a more than adequate gain margin to provide signal sensitivity and compensate for interstage filter losses. To show how this gain may be distributed we can look at a first cut design example.

If we continue with the 30 dB gain tuner with a 6 dB N.F., using the tuner 75Ω output to misterminate the SAWF input will produce a very high insertion loss for the filter. This can easily be over 30 dB but before using the LM1823 gain capability to compensate for this loss, we must look at another aspect of filter insertion loss—the N.F. goes up Previously we assumed that the tuner N.F. will dominate the system N.F.—and with a tuner amplifier N.F. of 6 dB and 30 dB gain this is indeed true. But when the I.F. amplifier and SAWF are combined the N.F. for the combination exceeds 30 dB. This degrades the system N.F. to 7 dB* and after 50 dB of I.F. amplifier gain reduction the N.F. will be over 8 dB. Frequently this will be alright but it is instructive to consider improving the SAWF N.F. by matching the tuner output impedance to the filter or using an impedance matching pre-amp. For example, the 10 dB gain pre-amp shown in *Figure 18* has a 4 dB N.F. and reduces the filter loss to less than 20 dB. After 50 dB I.F. amplifier gain reduction, the combined N.F. is only 27 dB—for a worst case system N.F. of 6.6 dB. In a dual conversion system with a diode mixer (and already high N.F.), some gain *must* be provided prior to the SAWF.

$$*NF_{system} = NF_{tuner} + \frac{NF_{IF}}{(\text{Tuner Gain})}$$

Leaving a 10 dB gain margin over that required to raise a −6 dBmV signal to the rated detector output, the total gain requirement of the I.F. amplifier is

$$75.6\ dB - 30\ dB + 30\ dB - 34\ dB + 10\ dB = 51.6\ dB$$

(0.5 mV → 3V) (tuner) (SAWF) (detector) (gain margin)

(With a 10 dB gain impedance matching amplifier between the tuner and the SAWF, the gain requirement falls by 20 dB to 31.6 dB.) To avoid overload in the high gain tuner, we probably have to start gain reducing the tuner when the input signal reaches +10 dBmV (but certainly not before 0 dBmV in order to preserve the tuner NF) so that the I.F. AGC range requirement is approximately 26 dB. This amount of AGC range can be obtained without a resistor connected between Pins 4 & 5 putting the fourth stage gain

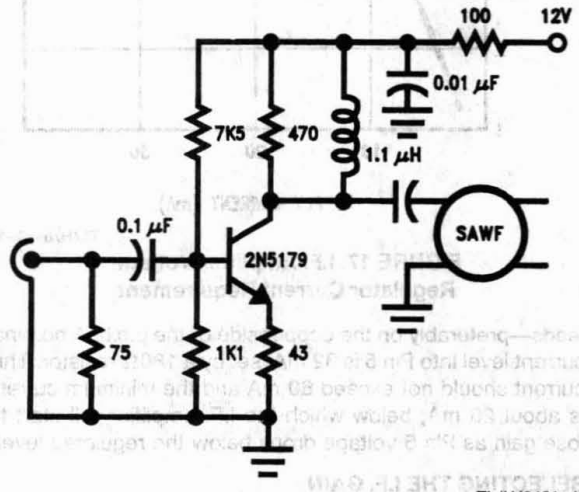

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FIGURE 18. Impedance Matching Pre-amplifier

at 4 dB. The SAWF impedance sets the input stage gain at 3 dB for a total of 41 dB to the input of the final stage. A 180Ω resistor at Pin 1 gives the desired last stage gain of 11 dB, or this resistor is reduced to 50Ω and a 10 dB pad is inserted between the I.F. amplifier output and the detector input when a pre-amp is used.

LM1823 VIDEO DETECTOR

The second major function of the LM1823 is the video detector stage, including the AFT/AFC detector and AGC detector/amplifier.

The video detector stage of the LM1823 has a fixed conversion gain of 34 dB—giving a 60 Vrms input level for a 3V (o–p) detected output. This input level is required for AGC action to commence and is well below the input level that can cause intermodulation or catastrophic overload.

Synchronous detection of an amplitude modulated carrier involves a source of constant amplitude CW with the same frequency as the signal carrier, and two phase detectors. One detector is operated in quadrature—i.e. the CW phase and the signal carrier phase have a 90 degree difference at the inputs to the phase detector. This detector operates solely to keep the CW source phase-locked to the signal carrier. The second phase detector has synchronous or in-phase inputs so that the detector output responds to the amplitude difference between the inputs and therefore tracks the signal amplitude modulation.

The benefits of synchronous detection over envelope detection are well known, and most modern receivers incorporate a type of detector known as a quasi-synchronous detector, which is a signal amplitude detector. The I.F. signal is amplified and stripped of modulation in order to be used as the detector CW. The disadvantages of this type of detector are the loss of linearity at very low signal inputs (corresponding to peak video modulation) and a fundamental compromise in the bandwidth of the limiter stage used to strip the modulation. To maintain ease of tuning and a relative immunity from center frequency drift caused by temperature changes and aging, the limiter bandwidth is sufficiently wide that the resulting CW is phase modulated by the information on the original I.F. carrier. Since this can generate intermodulation products, a high Q is desirable and a trade-off in ease of alignment occurs.

A less obvious problem with this type of detector is the actual static detection phase that is being regenerated. Internal I/C related phase shifts cause the limited carrier waveform applied to the detector to be more or less than 0 degrees phase-shifted with respect to the signal carrier phase. A loss in detector efficiency results, but if the limiter tuning is adjusted to compensate for this, the CW phase from the limiter will depend on the drive to the limiter. The detection phase then changes with amplitude modulation of the original I.F. carrier. The effect of this is observed primarily as differential phase in the chroma subcarrier signal and increased levels of sound buzz. Although, as discussed later, the desired phase difference between the detector CW and signal carrier is not necessarily 0 degrees, the limiter tuning cannot be used to correct the amplitude modulation detector phase—the limiter must be center tuned to avoid carrier phase shifts with modulation level.

The LM1823 overcomes these problems by providing a true synchronous detector system, which, as the block diagram shows, comprises of an internal VCO and in-phase and quadrature phase detectors. The incoming signal from the

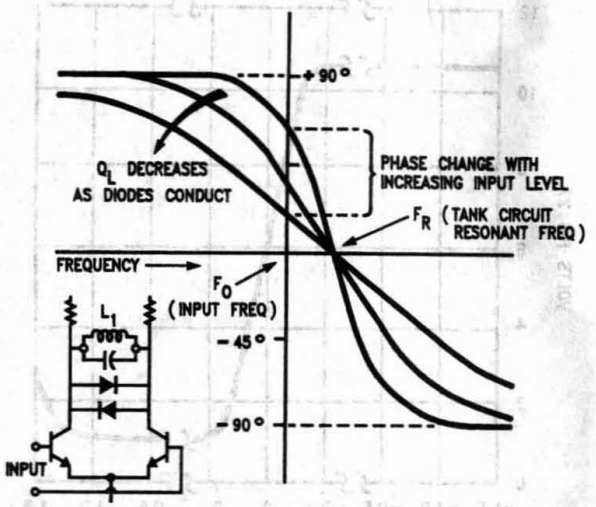

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FIGURE 19. Limited I.F. Carrier Phase Shifts with Input Amplitude when the Limiter Tank is Mistuned

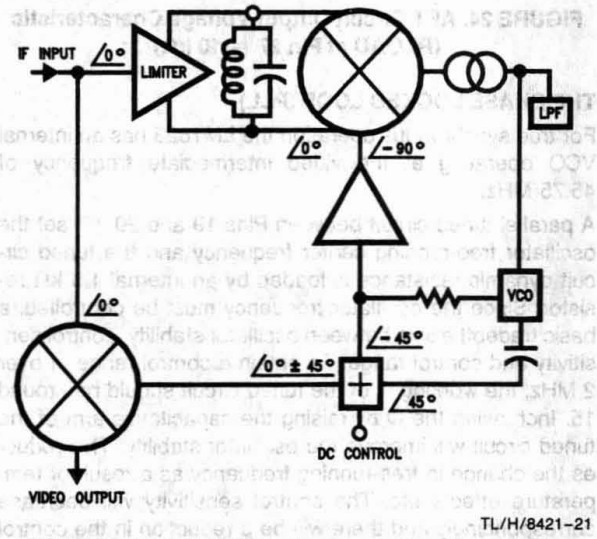

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FIGURE 20. LM1823 Synchronous Detector and DC Controlled Detection Phase

I.F. amplifier is split into two paths. One path is through a high gain limiter stage which strips the amplitude modulation from the CW and applies it to one input of the quadrature phase detector. The other detector input is from the VCO and, once synchronized to the intermediate frequency, if the VCO phase deviates from a 90 degree relationship with the limiter CW phase, a control current is generated by the phase detector and is filtered at Pin 18 to correct the VCO. Even though the limiter stage tuned circuit faces the same compromises of desired narrow bandwidth versus ease and stability of tuning, the filter at Pin 18 can be made to have a very narrow bandwidth. Therefore the VCO can provide a reference signal to the phase detectors with a high degree of spectral purity. The second path for the I.F. signal is directly to the in-phase detector. The VCO output passes through a DC voltage controlled phase shifter before being applied to this detector. The DC phase shifter allows precise adjustment of the synchronized VCO phase for maximum amplitude modulation detection efficiency, and compensates for any internal I/C phase shift variations. At the same time, proper center-tuning of the limiter coil is possible.

The benefits of center-tuning the limiter are clearly shown by comparing the differential chroma phase of the LM1823

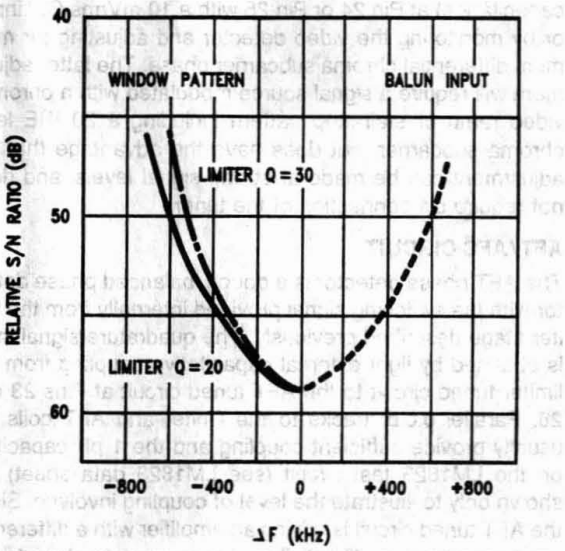

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FIGURE 21. Relative S/N Ratio with Limiter Tuning (No SAWF)

with a conventional quasi-synchronous detector. The LM1823 can consistently produce DP'S of under 1 degree compared with up to 10 degrees for a quasi-synchronous detector. There is also a substantial improvement in the sound carrier S/N ratio. When the limiter is detuned to compensate for internal I/C phase shifts or for detection phase-lags to produce video overshoots (for a subjectively crisper picture), the S/N ratio degrades by 5 dB to 7 dB, depending on the video modulating signal.

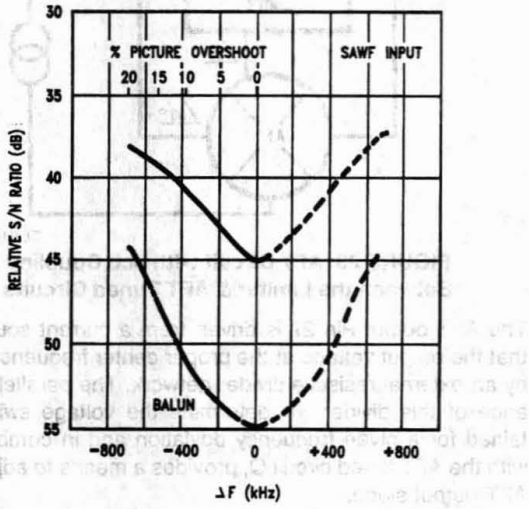

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FIGURE 22. Effect of Limiter Retuning with SAWF

THE LIMITER

The limiter tuned circuit at Pins 24 and 25 is driven by a differential stage with a 6.6 kΩ internal load impedance. A small signal gain of 50 (with a tuned circuit dynamic resistance of 8 KΩ) ensures that full quadrature detector efficiency is obtained with input levels above 10 mVrms, and internal Schottky diodes limit the maximum amplitude at Pins 24 and 25 to about 500 mV (p–p). Tuning is achieved either for a peak amplitude signal measured with an F.E.T. probe (low

capacitance) at Pin 24 or Pin 25 with a 10 mVrms CW input, or by monitoring the video detector and adjusting for minimum differential chroma subcarrier phase. The latter adjustment will require a signal source modulated with a chroma/video ramp or stair-step pattern including a 20 IRE level chroma subcarrier, but does have the advantage that the adjustment can be made at strong signal levels, and does not require dis-connection of the tuner.

AFT/AFC CIRCUIT

The AFT phase detector is a doubly-balanced phase detector with the switching signal provided internally from the limiter stage described previously. The quadrature signal input is obtained by light external capacitative coupling from the limiter tuned circuit to the AFT tuned circuit at Pins 23 and 26. Parallel p.c.b. tracks to the limiter and AFT coils will usually provide sufficient coupling and the 1 pF capacitors on the LM1823 test circuit (see LM1823 data sheet) are shown only to illustrate the level of coupling involved. Since the AFT tuned circuit is driving an amplifier with a differential input resistance of 20 kΩ, it is able to operate close to the unloaded Q of the inductor.

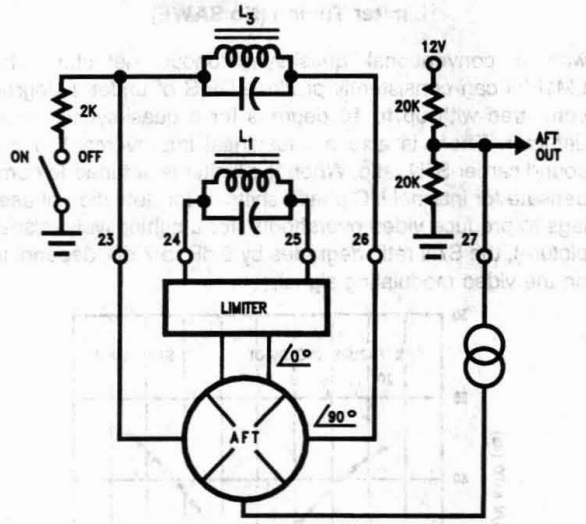

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FIGURE 23. AFT Circuit with pcb Coupling Between the Limiter & AFT Tuned Circuits

The AFT output Pin 27 is driven from a current source so that the output voltage at the proper center frequency is set by an external resistive divider network. The parallel resistance of this divider will determine the voltage swing obtained for a given frequency deviation and in combination with the AFT tuned circuit Q, provides a means to adjust the AFT output slope.

Once outside the desired tuning range the AFT output voltage should stay either close to ground (I.F. frequency high) or close to the positive supply voltage (I.F. frequency low). If the voltage moves back towards the center voltage as the signal moves further away from the desired tuning range, then more coupling from the limiter tank may be needed. Grounding Pin 26 through a 2 kΩ resistor will defeat the AFT circuit for receiver fine-tuning purposes. The 2 kΩ provides isolation of the AFT switch & associated cable from the tuned circuit which has a relatively low dynamic resistance of 1.8 kΩ. Resistor values larger than 2 kΩ may prevent the circuit from being defeated, but either Pin 23 or Pin 26 can be grounded directly without damaging the I/C.

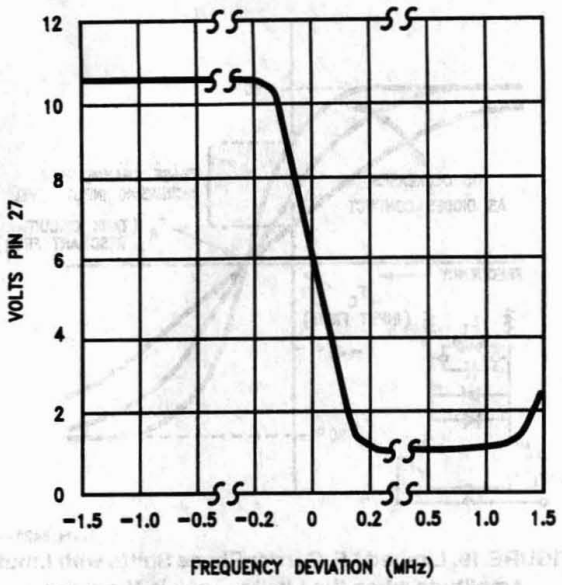

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FIGURE 24. AFT Circuit Output Voltage Characteristic (RLOAD at Pin 27 = 10 kΩ)

THE PHASE LOCKED LOOP (PLL)

For true synchronous operation the LM1823 has an internal VCO operating at the video intermediate frequency of 45.75 MHz.

A parallel tuned circuit between Pins 19 and 20 will set the oscillator free-running center frequency and the tuned circuit dynamic resistance is loaded by an internal 1.5 kΩ resistor. Since the oscillator frequency must be controlled, a basic tradeoff exists between oscillator stability, control sensitivity and control range. To obtain a control range of over 2 MHz, the working Q of the tuned circuit should be around 15. Increasing the Q by raising the capacitative arm of the tuned circuit will improve the oscillator stability. This reduces the change in free-running frequency as a result of temperature effects etc. The control sensitivity will decrease correspondingly and there will be a reduction in the control range. The control range in the application circuit has been chosen to cover the expected deviations in the I.F. carrier that are allowed by AFT circuits. With a coil unloaded Qu of

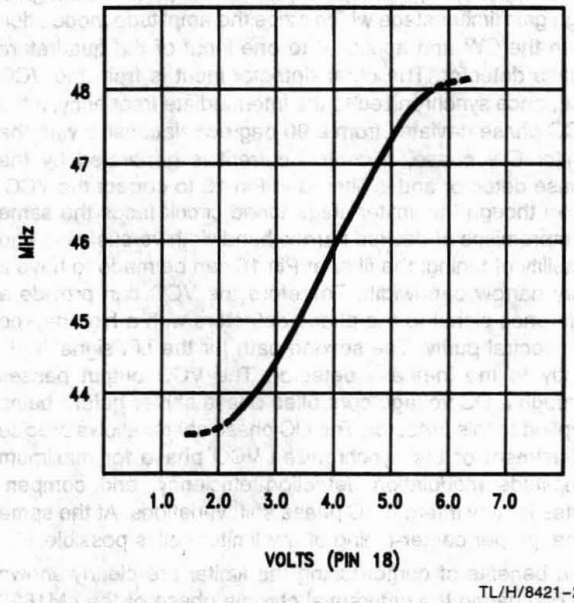

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FIGURE 25. VCO Control Sensitivity Characteristic

55, and a working Q of 15, the inductance should be 0.24 uH, which tunes with 51 pF at 45.75 MHz.

The V.C.O. frequency is adjusted by injecting a 60 mVrms CW at Pin 28. If the VCO tuning (L_3) is a long way from being correct, the detector output Pin 16 will show an AC signal of about 4V (p–p) centered around 7.5 VDC. As the oscillator is tuned toward the correct frequency the AC beat note will decrease and abruptly disappear as the oscillator locks to the carrier frequency. Final adjustment of the VCO is done by tuning L_3 until the voltage at the phase detector filter Pin 18 is 4 VDC.

Oscillator control is accomplished by internally phase shifting the currents in a direct cross-coupled differential stage in response to the control voltage developed at Pin 18. Direct cross-coupling of the bases and collectors of this differential stage means that the transistors are operating in a soft-saturated mode, enabling a constant output amplitude to be obtained of about 500 mV (p–p). This output amplitude does not change with coil tuning or over the frequency control range of the oscillator. With the specified tuning components at Pins 19 and 20, the VCO sensitivity is 1.5 MHz/volt. Other general characteristics of the VCO are a negative temperature coefficient of 150 ppm/degree C, and a tendency for the oscillator control sensitivity to decrease with decreasing frequency of operation (below 10 MHz).

The VCO tuning components are mounted across the I/C package from the I.F. amplifier input. This minimizes inductive coupling and yields approximately 105 dB isolation for the I/C alone. Leads and components connected to the I.F. amplifier input will reduce the VCO isolation (as will higher operating frequencies).

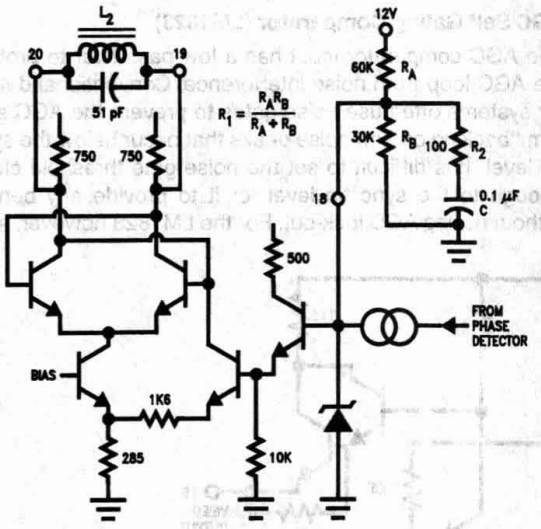

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FIGURE 26. LM1823 VCO Circuit

The quadrature phase detector output is a push-pull current source so that the control voltage at Pin 18 is determined by the parallel resistance of the external divider network, which also sets the quiescent control voltage in the absence of an I.F. signal. This divider voltage should be centered at 4 VDC since the lower voltage swing for controlling the oscillator frequency is 2 VDC, and an internal clamp prevents Pin 18 increasing above 5.6 VDC. By using a 20 kΩ parallel resistance at Pin 18, the phase detector current of 7.5 uA/degree gives a phase detector sensitivity (μ) of 0.15 volts/degree. This parallel resistance is equivalent to R1 in the conventional filter for a 2nd order PLL. The oscillator and phase detector sensitivities given above yield a DC loop gain of 12.9 MHz/radian. For the data sheet value of 100Ω for R2, and a filter capacitor of 0.1 uF, the loop damping factor (K) is 1.01 and the natural resonant frequency (w) is 32 kHz. From this we can calculate that the loop −3 dB bandwidth is 73 kHz which is substantially less than would be practicable with a quasi-synchronous detection system, and this brings the desired benefits of low luma/sound/chroma crosstalk and freedom from quadrature distortion produced by the I.F. filter slope characteristic in the vicinity of the picture carrier frequency. Nevertheless, some signal conditions may cause wider PLL bandwidths to be used. A probable problem is incidental carrier phase modulation (ICPM).

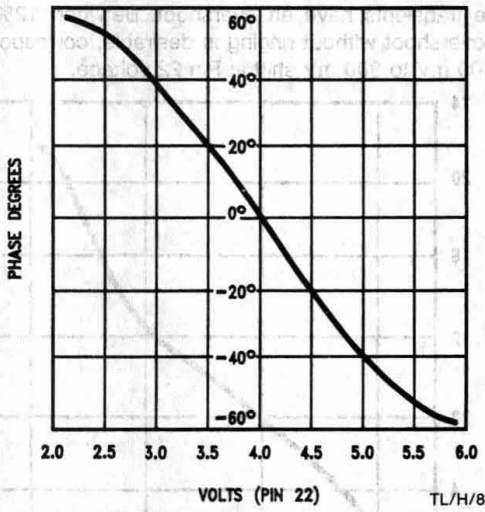

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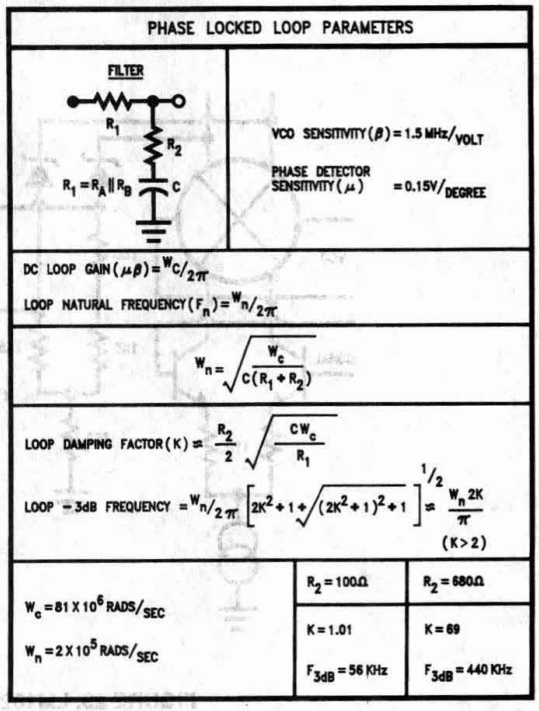
FIGURE 27. DC Controlled Phase Shifter Characteristic

This describes the shift in carrier phase as the modulation depth changes, and is particularly likely to happen where prior processing of the original carrier waveform has occurred—in distribution or conversion amplifiers employed in MATV and cable systems for example. It is also present to an extent in broadcast transmitters and if the PLL loop bandwidth is too narrow for the VCO to track this phase shift, then the ICPM is transferred to the signal modulation. This can be observed as a tint shift in color bars or a smear


PHASE LOCKED LOOP PARAMETERS
FILTER
R1
R2
C
R1 = RA ‖ RB
VCO SENSITIVITY (β) = 1.5 MHz/VOLT
PHASE DETECTOR SENSITIVITY (μ) = 0.15V/DEGREE
DC LOOP GAIN (μβ) = Wc/2π
LOOP NATURAL FREQUENCY (Fn) = Wn/2π
Wn = √(Wc / C(R1 + R2))
LOOP DAMPING FACTOR (K) ≈ R2/2 √(CWc/R1)
LOOP −3dB FREQUENCY = Wn/2π [2K² + 1 + √((2K² + 1)² + 1)]^1/2 ≈ Wn 2K/π (K > 2)
Wc = 81 X 10⁶ RADS/SEC
Wn = 2 X 10⁵ RADS/SEC
R2 = 100Ω
K = 1.01
F3dB = 56 KHz
R2 = 680Ω
K = 69
F3dB = 440 KHz

TL/H/8421–29

in the leading edge of a color bar as the VCO belatedly attempts to track the phase change. For these types of signals it is desirable to increase the loop bandwidth to about 500 kHz—changing R2 to 680Ω is an easy fix. The loop damping factor is kept greater than 1 to avoid ringing on the phase transients. Larger loop bandwidths will increase the possibility of luma/sound/chroma crosstalk.

Once the VCO is locked in phase to the I.F. signal, the DC phase shifter Pin 22 is normally around 4 VDC for peak detector efficiency. Usually some extra phase lag will be introduced since a subjectively crisper picture is obtained if picture transients have an overshoot. Between 12% and 20% overshoot without ringing is desirable, corresponding to a 400 mV to 800 mV shift in Pin 22 voltage.

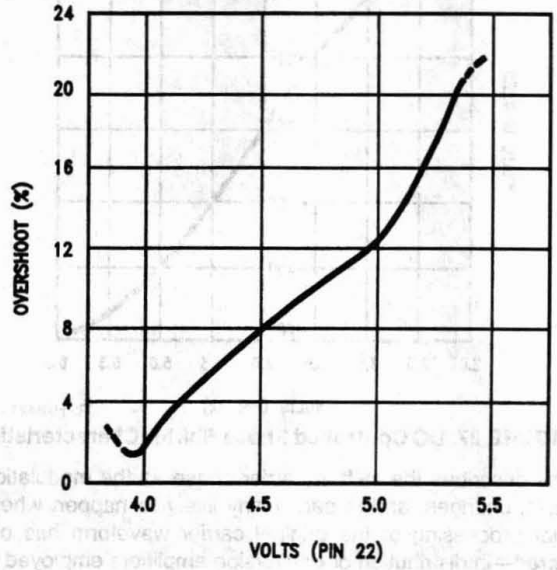


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FIGURE 28. Signal Overshoot Produced by Carrier Detection Phase Shift

VIDEO DETECTOR POST AMPLIFIER

The response of the video amplifier is rolled off above 9 MHz to minimize the amount of the VCO waveform and its harmonics appearing in the output at Pin 16. Typical oscillator products are 40 dB below the desired signal level.

Zener diodes are used in the video amplifiers for level shifting so that the use of PNP transistors is avoided and the detector linearity is preserved. Excellent differential gain characteristics are obtained—typically less than 3%. Pin 16 is a Darlington NPN emitter follower output. With no detector CW input signal, Pin 16 is at 7.6 VDC, representing zero carrier level which is slightly higher than peak white (by 12½%). As the CW input increases, Pin 16 voltage decreases towards black level with the sync pulses producing the most negative detector level.

The level reached by the sync tips is determined by the AGC loop threshold and if the internal AGC comparator is used (Pin 16 is directly connected to Pin 17), the sync tips will be clamped at 4 VDC. This produces a nominal detector output of 3.2V (p–p) but this is subject to variations in the Pin 16 detected zero carrier level. The resistive network shown connected between Pin 16 and Pin 17 in *Figure 30* can be used to change the zero carrier level at Pin 17 for an adjustable recovered video level. For best performance the recovered video level should never be less than 1V (p–p) or greater than 4V (p–p). In suppressed sync systems, the recovered video at Pin 16 is routed to the descrambler for restoration of the sync amplitude before it is applied to Pin 17. Obviously the signal DC content must be preserved through the descrambler if proper AGC action is to be maintained.

AGC Self Gating Comparator (LM1823)

The AGC comparator input has a low pass filter to protect the AGC loop from noise interference. Conventional detector systems often use noise gates to prevent the AGC system "backing off" on noise peaks that occur below the sync tip level. It is difficult to set the noise gate threshold close enough to the sync tip level for it to provide any benefit without risking AGC lock-out. For the LM1823 however, syn-

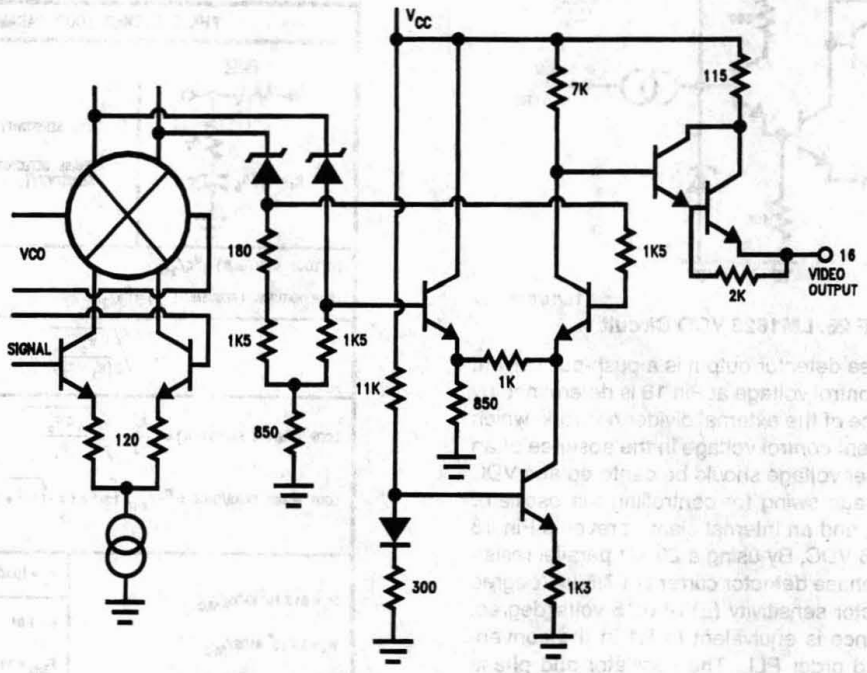

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FIGURE 29. LM1823 Detector and Video Amplifier

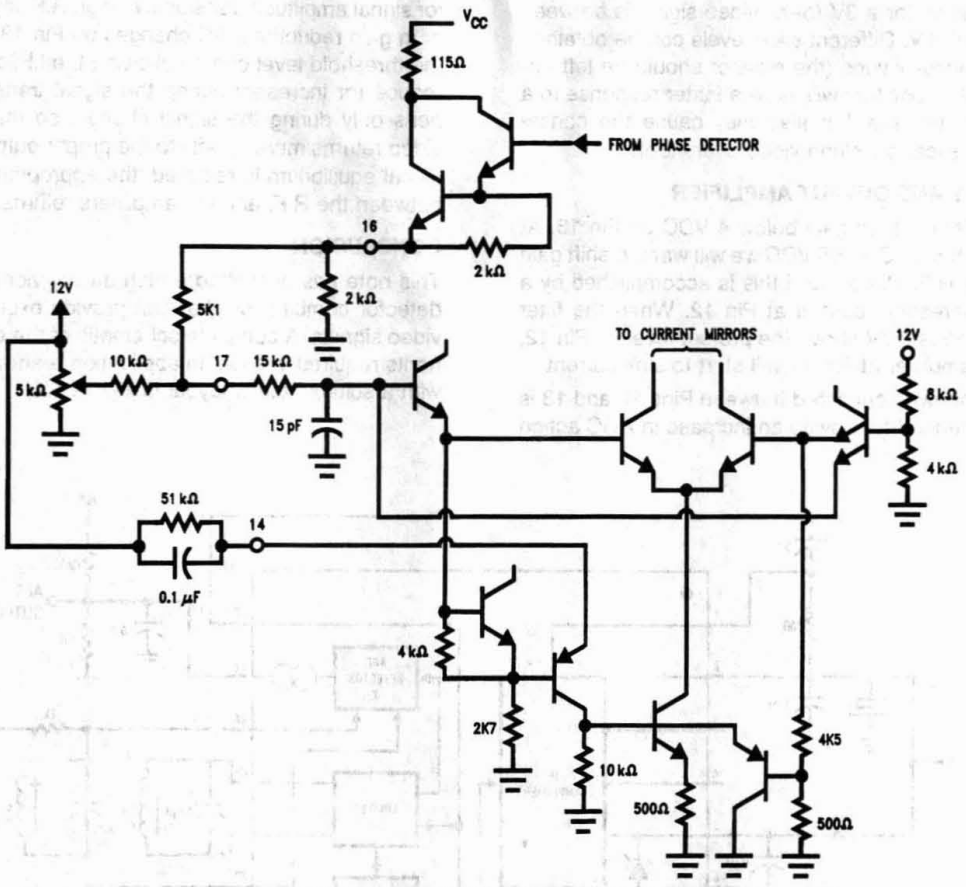


FIGURE 30. LM1823 Self Gating AGC Comparator

chronous detection allows the noise gate to be eliminated. Since the noise is random phase, the synchronous detector will not rectify the noise voltage and the low pass filter can average out the noise input to the comparator.

Further protection of the AGC comparator is provided by gating the comparator on only during the sync pulse period. The gate pulse is obtained from the input video waveform sync pulses at Pin 16. Essentially an emitter coupled sync stripper circuit, the slice level is set by an external time constant at Pin 14. During the sync pulse period the capacitor at Pin 14 is being charged toward ground potential and the comparator is gated on. Between sync pulses the capacitor discharges towards the positive supply voltage through the resistor and the comparator is off. The sync slice level is determined by the Pin 14 RC time constant and is given in Equation (3) as the number of millivolts the slice level is above the sync tip voltage.

$$V\,SLICE = 1/2\,RC\,(mV) \qquad (3)$$

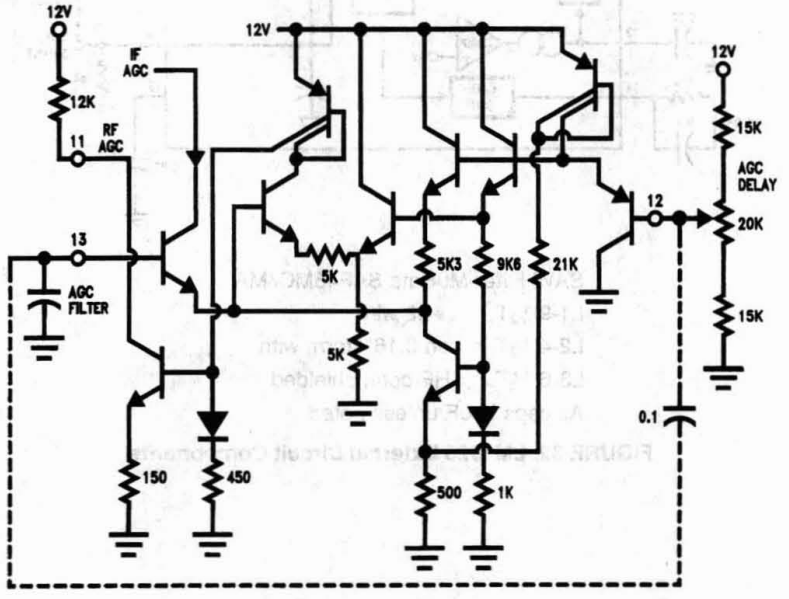


FIGURE 31. RF AGC Amplifier

A typical slice level for a 3V (o–p) video signal is between 100 mV and 250 mV. Different slice levels can be obtained with other capacitor values (the resistor should be left unchanged). Small capacitors will allow a faster response to a fluctuating sync tip level but also may cause the consequently deeper slice to include video overshoots.

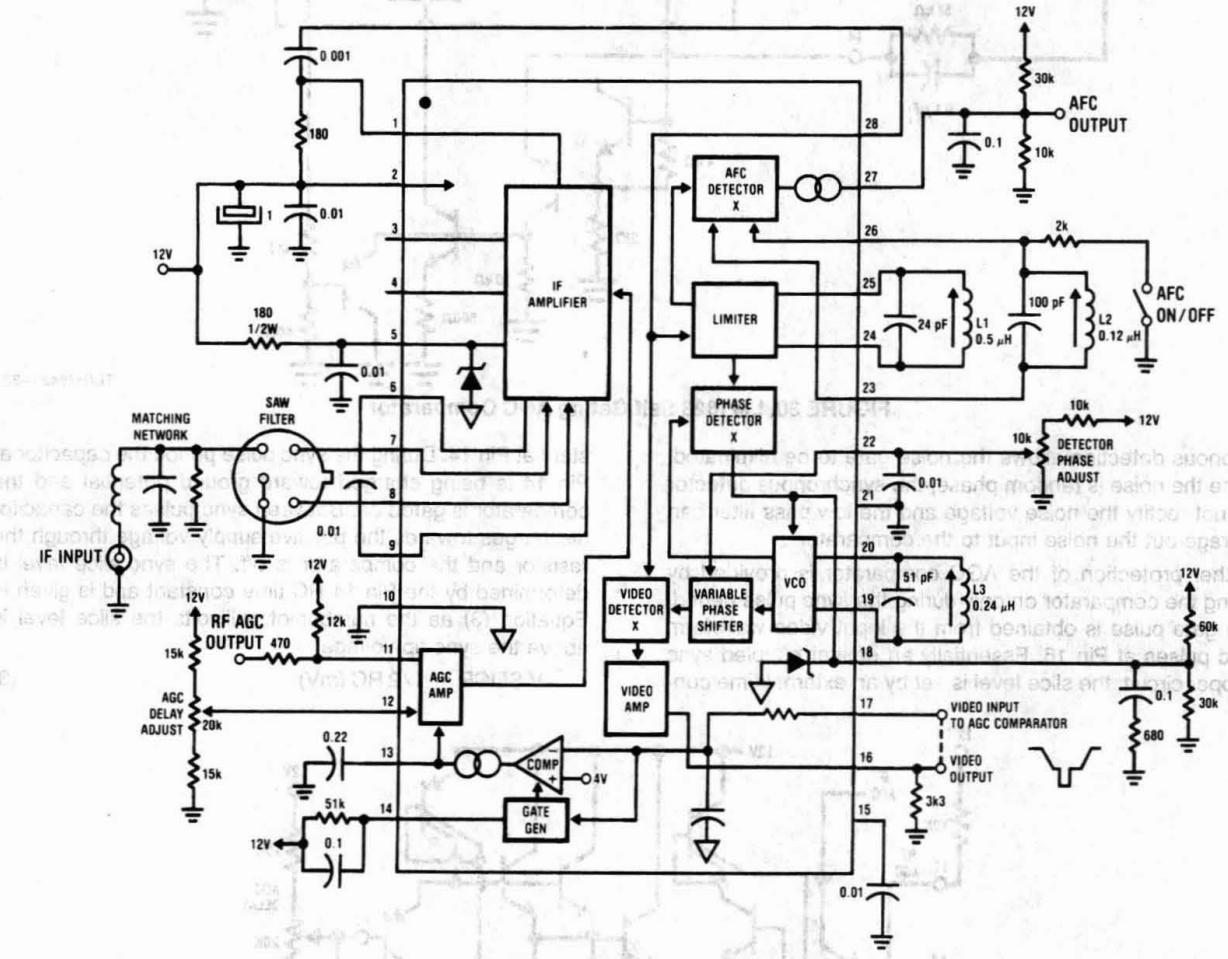
RE AGC DELAY AND OUTPUT AMPLIFIER

The I.F. amplifier is at full gain below 4 VDC on Pin 13. At anywhere from 5.5 VDC to 6.5 VDC we will want to shift gain control into the R.F. stages, and this is accomplished by a delayed AGC threshold control at Pin 12. When the filter voltage on Pin 13 is 0.7V above the pre-set level on Pin 12, the R.F. AGC amplifier at Pin 11 will start to sink current.

The capacitor shown connected between Pins 12 and 13 is optional and intended to provide an increase in AGC action for signal amplitude transients at high R.F. signal levels (tuner in gain reduction). AC changes on Pin 13 are coupled to the threshold level control allowing the I.F. amplifier to gain reduce (or increase) during the signal transient. This happens only during the signal change, so that the detected video returns more rapidly to the proper output levels. Once signal equilibrium is restored, the appropriate gain balance between the R.F. and I.F. amplifiers returns.

CONCLUSION

This note has described a high quality video I.F. amplifier/detector combination that can provide excellent baseband video signals. A complete schematic of the external components required in such an application is shown in *Figure 32*, with a suitable p.c.b. layout in *Figure 33*.



TL/H/8421–34

SAW Filter-MuRata SAF45MC/MA
L1-9 ½T } #22 wire
L2-4 ½T } on 3.16" form with
L3-6 ½T } HF core, shielded
All caps in uF unless noted

FIGURE 32. LM1823 External Circuit Components

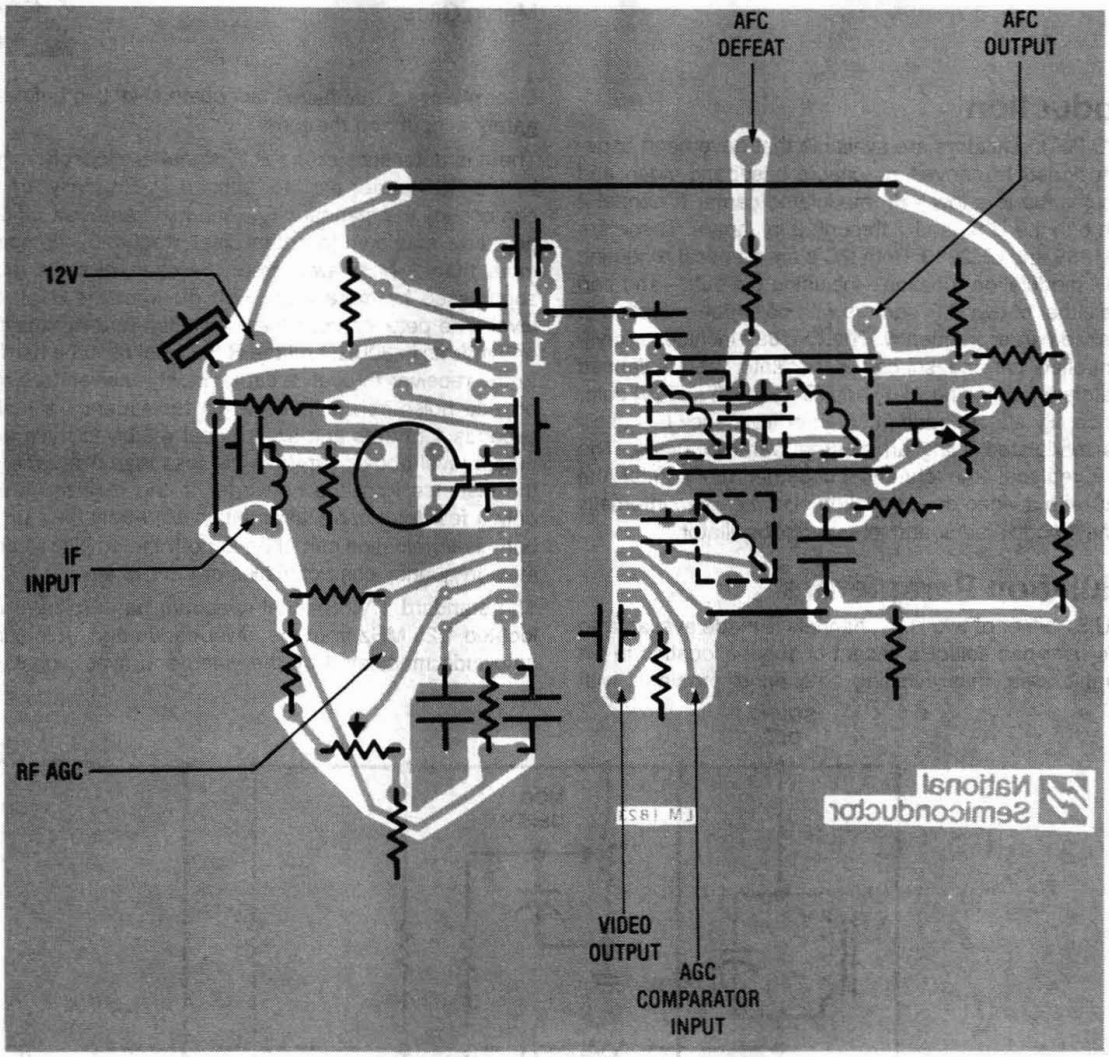


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FIGURE 33. LM1823 Printed Circuit Board Layout (Component Side)

LM2889 R.F. Modulator

National Semiconductor
Application Note 402
Martin Giles

Introduction

Two I/C RF modulators are available that have been especially designed to convert a suitable baseband video and audio signal up to a low VHF modulated carrier (Channel 2 through 6 in the U.S., and 1 through 3 in Japan). These are the LM1889 and LM2889. Both I/C's are identical regarding the R.F. modulation function—including pin-outs—and can provide either of two R.F. carriers with dc switch selection of the desired carrier frequency. The LM1889 includes a crystal controlled chroma subcarrier oscillator and balanced modulators for encoding (R-Y) and (B-Y) or (U) and (V) color difference signals. A sound intercarrier frequency L-C oscillator is modulated using an external varactor diode. The LM2889 replaces the chroma subcarrier function of the LM1889 with a video dc restoration clamp and an internally frequency modulated sound intercarrier oscillator.

Modulation Parameters

In the U.S., either of two R.F. channels is made available so that the user can select a vacant channel allocation in his geographic area, thus avoiding co-channel problems with older receivers that have inadequate shielding between the antenna input and the tuner.

The characteristics of the R.F. signal are loosely regulated by the FCC under part 15, subpart H. Basically the signal can occupy the standard T.V. channel bandwidth of 6 MHz, and any spurious (or otherwise) frequency components more than 3 MHz away from the channel limits must be suppressed by more than −30 dB from the peak carrier level. The peak carrier power is limited to 3 mVrms in 75Ω or 6 mVrms in 300Ω, and the R.F. signal must be hard-wired to the receiver through a cable. Most receivers are able to provide noise-free pictures when the antenna signal level exceeds 1 mVrms and so our goal will be to have an R.F. output level above 1 mVrms but less than 3 mVrms. Since the distance from the converter to the receiver is usually only a few feet, cable attenuation will rarely be a problem, but mis-termination can change both the amplitude and relative frequency characteristics of the signal.

The standard T.V. channel spectrum has a picture carrier located 1.25 MHz from the lower band edge. This carrier is amplitude modulated by the video and sync signal. In the

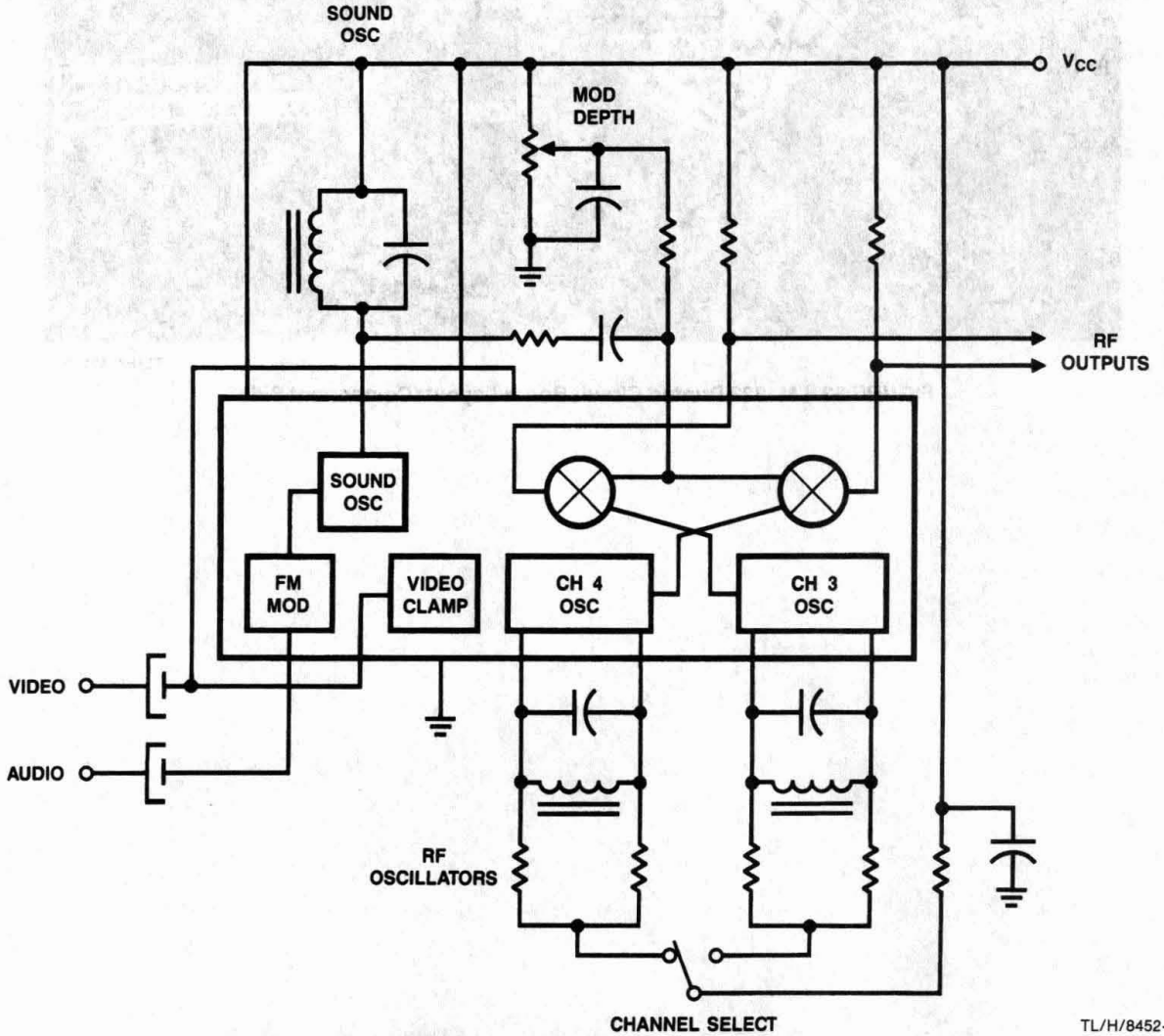

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FIGURE 1. The LM2889 Block Diagram With External Components

Modulation Parameters (Continued)

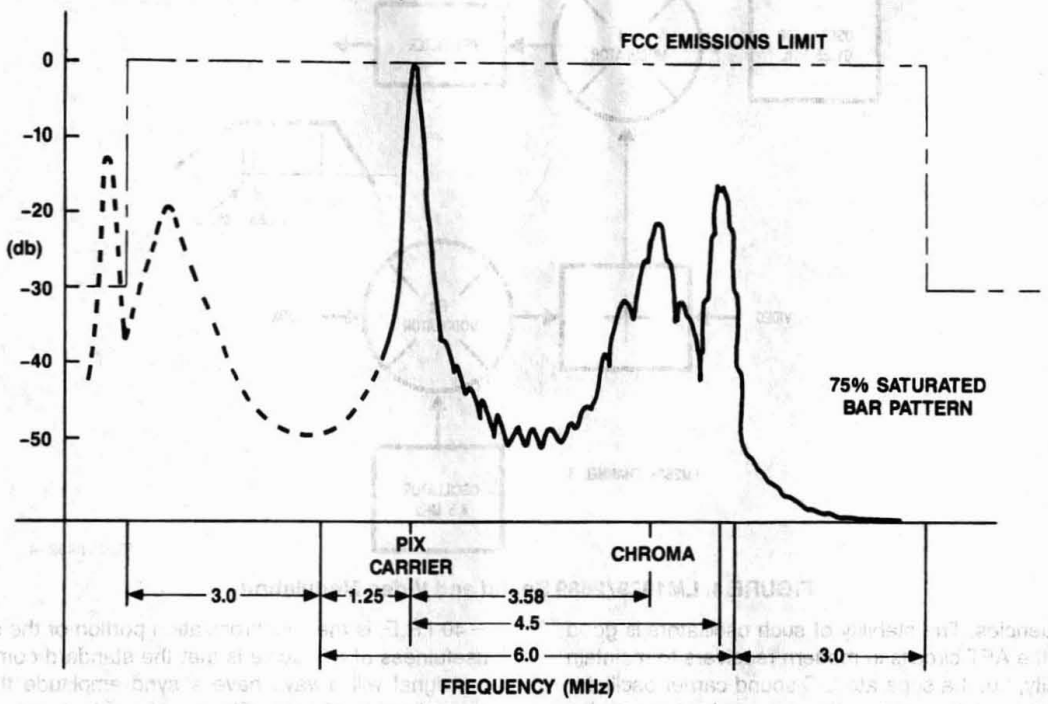

FIGURE 2. Television Channel R.F. Spectrum

case of a color signal, a second subcarrier is added 3.58 MHz above the picture carrier. The sound or aural carrier is 4.5 MHz above the picture carrier and is frequency modulated with the audio signal to a peak deviation of 25 kHz. This audio signal has pre-emphasis above 2.1 kHz (a 75 μs time constant). Similar modulation methods and standards are used in Japan and Europe.

With the picture carrier located near one end of the channel bandwidth, most of the available spectrum is used by the upper sideband modulation components. Only modulating frequencies within 0.75 MHz of the carrier frequency are transmitted double sideband and the lower sideband is truncated by at least −20 dB compared to the peak carrier level by the time the lower channel edge is reached. This is referred to as Vestigial Sideband (VSB) modulation and since most R.F. modulators are double sideband, a VSB filter is used at the transmitter output. A filter is needed for each channel and consists of bandpass and harmonic filter sections. A broadcast transmitter uses a separate modulator for the sound carrier and this is added to the picture carrier via a diplexer before reaching the transmitting antenna. Close control is maintained on the picture and sound carrier frequencies to keep a 4.5 MHz spacing between them. This tight frequency control is used to advantage by the majority of television receivers which employ intercarrier sound circuits. The I.F. amplifier processes both the pix and sound I.F. carriers and detects the 4.5 MHz difference frequency at the video detector stage. This frequency modulated sound intercarrier is then stripped of amplitude modulation by a high gain limiter circuit and a quadrature demodulator recovers the audio.

The LM1889 and LM2889 use a slightly different modulation scheme to that described above for several reasons. For circuit economy L-C oscillators are used to generate the pix

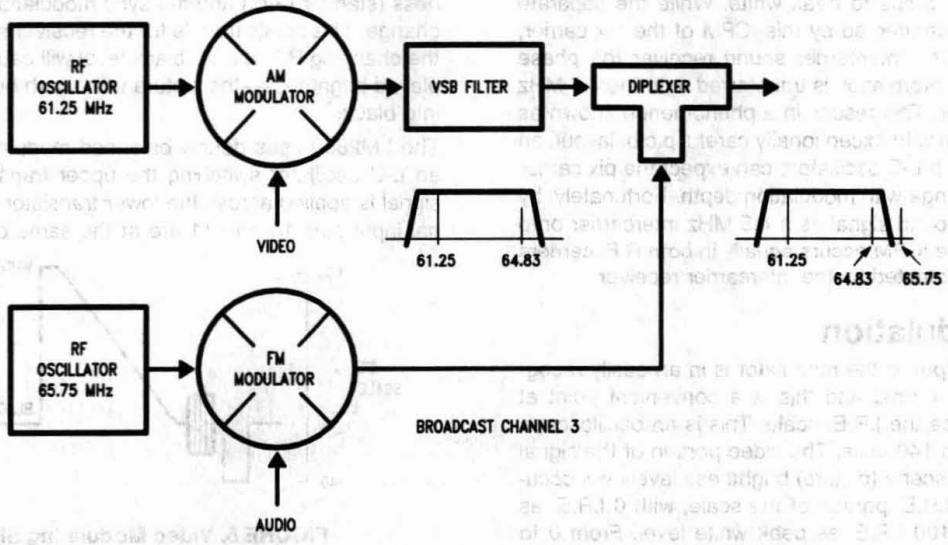

FIGURE 3. Broadcast Transmitter Block Diagram

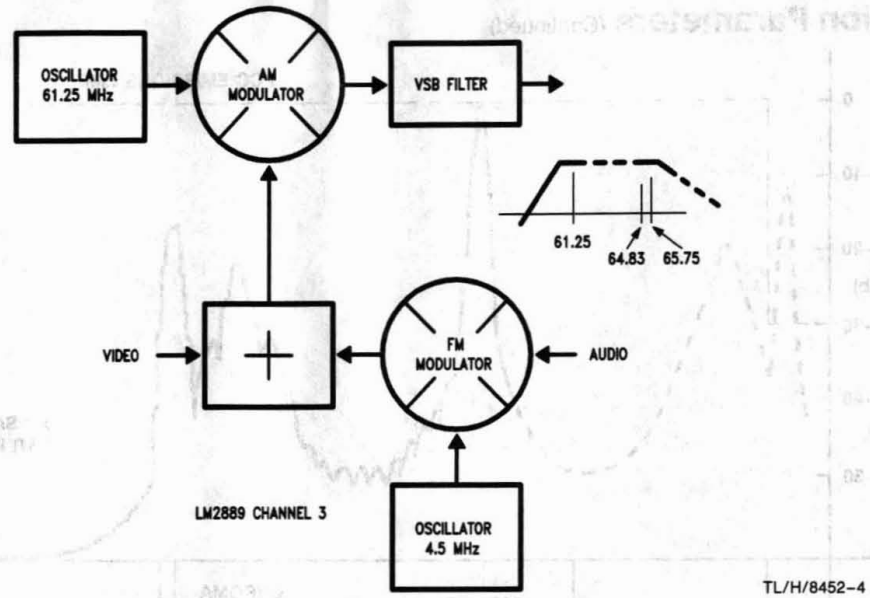

FIGURE 4. LM1889/2889 Sound and Video Modulation

carrier frequencies. The stability of such oscillators is good enough for the AFT circuits in modern receivers to maintain picture quality, but if a separate L-C sound carrier oscillator were used, the relative drift of the two carrier frequencies would be much too great for intercarrier sound receivers. For example, a typical television sound circuit tuned to 4.5 MHz will generate as much as 3% distortion if the difference between the R.F. carriers changes by 15 kHz. Apart from the difficulty of setting the initial frequency with sufficient accuracy, it is unlikely that two L-C oscillators could be kept within 15 kHz of each other at 60 MHz to 100 MHz operating frequencies. However, when the audio signal is modulated onto a 4.5 MHz intercarrier oscillator frequency and this carrier is used to modulate the picture carrier, we have only the 4.5 MHz oscillator drift to worry about.

A less obvious problem, but nevertheless significant if good audio quality is to be obtained, is incidental carrier phase modulation (ICPM). Even broadcast transmitters cannot maintain an invariant carrier phase as the modulation depth changes. Without feedback loops to control ICPM, a broadcast transmitter can produce from 3 degrees to as much as 30 degrees phase change as the carrier modulation decreases from sync tips to peak white. While the separate sound carrier is unaffected by this ICPM of the pix carrier, on reception in the intercarrier sound receiver the phase shift with picture information is transferred onto the 4.5 MHz sound intercarrier. This results in a phenomenon known as sound buzz. Even with exceptionally careful p.c.b. layout, an I/C modulator with L-C oscillators can expect the pix carrier frequency to change with modulation depth. Fortunately, by modulating the sound signal as a 4.5 MHz intercarrier onto the pix carrier, the ICPM occurs equally in both R.F. carriers and will not be detected by the intercarrier receiver.

Video Modulation

The baseband input to the modulator is in an easily recognized composite format and this is a convenient point at which to introduce the I.R.E. scale. This is an oscilloscope scale divided into 140 units. The video portion of the signal representing the scene (picture) brightness levels will occupy the 0 to 100 I.R.E. portion of the scale, with 0 I.R.E. as black level and 100 I.R.E. as peak white level. From 0 to −40 I.R.E. is the synchronization portion of the signal. The usefulness of this scale is that the standard composite video signal will always have a sync amplitude that can be normalized to 40 I.R.E. Similarly the color burst amplitude is always 40 I.R.E. For a 1V (p-p) video signal, an I.R.E. unit is equivalent to 7.5 mV.

Although the video is amplitude modulated on the carrier waveform, the carrier amplitude only decreases from the unmodulated level. This contrasts with standard AM where the carrier level alternately increases and decreases about the unmodulated level. For a television signal, the peak unmodulated level corresponds to sync tip level and increasing brightness levels cause decreasing carrier levels. To prevent complete suppression of the carrier (and consequent loss of the sound intercarrier in the receiver) the peak white signal is limited to a maximum modulation depth of 87.5% of the peak carrier. Returning to our I.R.E. scale we can see that from peak carrier to zero carrier is equivalent to 160 I.R.E. (140/0.875 = 160). One obvious consequence of this modulation scheme is that the video signal MUST BE dc coupled to the modulator. AC coupling will cause the peak carrier level to change with modulation scene brightness (standard AM) and the sync modulation amplitude will change. This spells trouble for the receiver sync circuits and the changing R.F. carrier black level will cause errors in displayed brightness—the picture will "wash out" or disappear into black.

The LM2889 uses doubly balanced modulator circuits with an L-C oscillator switching the upper transistor pairs. The signal is applied across the lower transistor pairs. If the signal input pins 10 and 11 are at the same dc potential, the

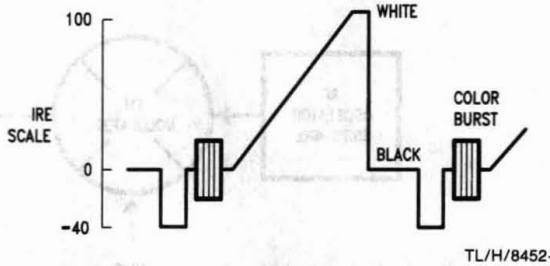

FIGURE 5. Video Modulating Signal (in terms of the I.R.E. Scale)

Video Modulation (Continued)

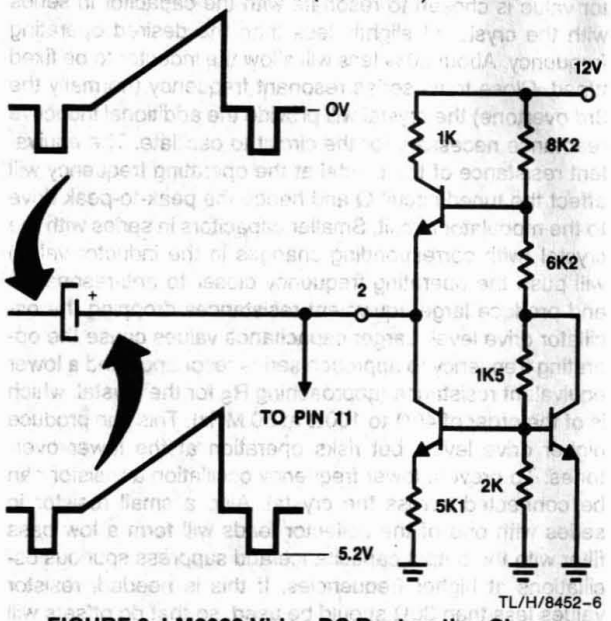

FIGURE 6. LM2889 Video DC Restoration Clamp

carrier is completely suppressed. As the offset voltage between pins 10 & 11 is increased, the carrier output level increases. With a 75Ω output load resistor, the conversion gain of the R.F. modulator is 20 mVrms/volt. A dc restoration circuit at pin 2 of the LM2889 allows the composite video to be ac coupled from the preceding stages, giving the designer flexibility in the video processing circuits (unless an LM1886 is being used as a video source, it is unlikely that the composite video dc level will be correct, even with dc coupled video sources). On a 12V supply, pin 2 clamps the sync tip of the video waveform to 5.1 VDC. Therefore, if we have a 2V (p-p) signal, one I.R.E. is equivalent to 14.3 mV and 160 I.R.E. is 2.29V. This is the required offset across the modulator input pins and since pin 11 will be clamped to 5.1 VDC by the dc restorer circuit, pin 10 should be biassed at 5.1V + 2.29V = 7.4 VDC. A look at the R.F. carrier output will confirm that now the syncs occupy from 100% to 75% of the peak carrier, and that white modulates the carrier down to 12½% of the peak. To maintain the proper modulation depth the clamp at pin 2 will track with supply voltage changes, allowing the bias at pin 10 to be set with a resistive divider connected between the supply and ground.

If the video signal polarity is reversed with positive syncs, either a dc coupled signal or an external dc restorer should be used that places the signal sync tip voltage towards the upper end of the common-mode input range at pin 11, which is 9 VDC with a 12V supply. Pin 10 is then offset below pin 11 voltage by the required amount for proper modulation. An input level of 2V (p-p) is optimal. Signal amplitudes of less than 1V (p-p) are also useable but internal offset voltages and the potential for carrier feedthrough or leakage to the output stage may make it difficult to maintain good R.F. linearity at peak modulation depths. Signal swings larger than 3V (p-p) should be avoided since this will produce relatively large AC/DC current ratios in the modulator and the resulting modulator non-linearities can cause a 920 kHz beat between the chroma and sound carriers.

Although only one video input is required, the LM2889 has two balanced R.F. modulators and two R.F. carrier frequency oscillators. Selection of the carrier frequency is by dc switching the supply voltage to the relevant oscillator tuned circuit. This automatically shuts off the other oscillator and modulator circuits. For test purposes when an output R.F. VSB filter isn't used, or when only one carrier frequency is needed, the output pins 8 and 9 can be wired together with a common load resistor. Providing two channel operation with two independent oscillator/modulator circuits is much superior to using a single modulator and attempting to change carrier frequency by switching the tuning components of a single L-C oscillator. The latter method involves

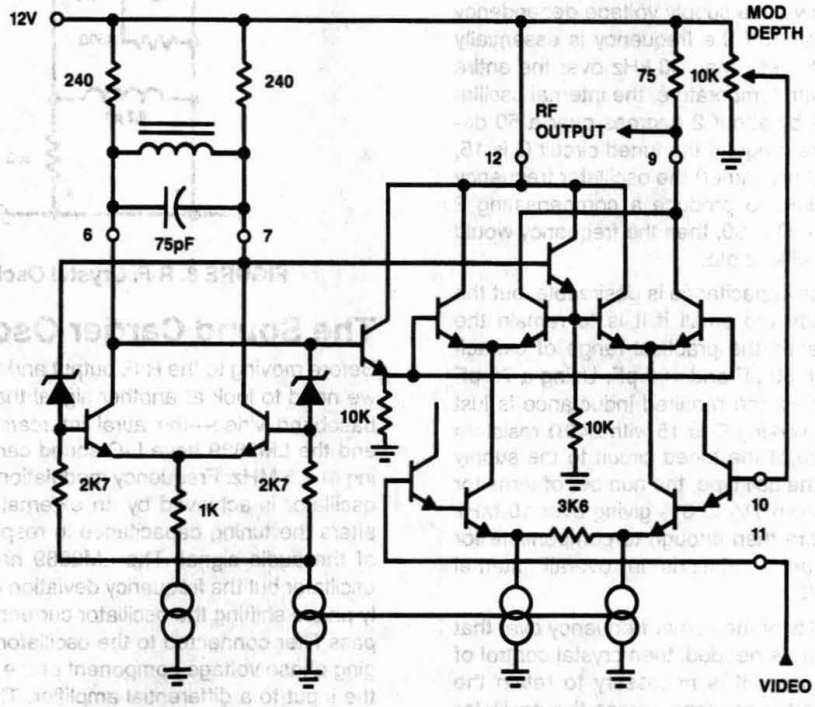

FIGURE 7. LM2889 R.F. Modulator and Oscillator (one channel)

Video Modulation (Continued)

use of isolating diodes (if unbalanced operation with attendant feed through problems is to be avoided) and expensive trimmer capacitors for tuning the second carrier frequency. A further disadvantage is the need to switch the VSB filter at the R.F. output.

The LM2889 oscillator configuration is the familiar cross coupled differential amplifier type, with level shifting zener diodes used to prevent the transistors from saturating with large oscillator output swings. The oscillator frequency is set by the tuned circuit components ($f = 1/2\pi\sqrt{LC}$), and the load resistors connected to the supply will set the oscillation amplitude and drive level to the modulators as well as determining the circuit working Q.

As might be expected, there are conflicting requirements on the practical range of working Q's. A high Q is desireable from the viewpoint of stability, but higher working Q's (set mainly by larger load resistors) increase the drive level to the modulator. Above 350 mV (p-p) the modulator will have attained full conversion gain and the R.F. output level will be determined by the amplitude of the video input signal. Unfortunately increased drive levels will also increase the carrier frequency second harmonic output from the modulator. Although a fully balanced design is used, parasitic capacitances on the emitters of the switching transistor pairs will rectify the oscillator waveform and this produces high levels of second harmonic. Load resistors much larger than 240Ω can produce a level of second harmonic matching the fundamental. Since relatively small load resistors are required (much smaller than the tuned circuit dynamic resistance) the working Q will be dominated by these resistors.

The acceptable degree of frequency stability will depend on the intended application, but L-C oscillators have proven to be adequate for most purposes. We can gain an idea of the frequency stability that is possible by considering the frequency drift produced by changes in the oscillator internal phase. A change in internal phase shift can be caused either by temperature or supply voltage changes but, as the LM2889 data sheet shows, the supply voltage dependency is low. Between 12V and 15V the frequency is essentially constant and changes by less than 30 kHz over the entire supply voltage range. With temperature, the internal oscillator phase shift changes by about 2 degrees over a 50 degree Celcius temperature range. If the tuned circuit Q is 15, then at 61.25 MHz (Ch 3 pix carrier) the oscillator frequency must change by −92 kHz to produce a compensating 2 degree phase shift. If the Q is 30, then the frequency would change by less than −45 kHz etc.

For high circuit Q, a large capacitance is desireable, but the inductor cannot be made too small if it is to remain the tuning element. This keeps the practical range of capacitance values to between 50 pF and 100 pF. Using a 75 pF capacitance, at 67.25 MHz the required inductance is just under 0.08 μH and the working Q is 15 with 240Ω resistors connected on either side of the tuned circuit to the supply voltage. Depending on the coil type, the number of turns for this inductance will be from 1½ to 3½ giving over 10 MHz tuning range. This is more than enough to compensate for component tolerance and variations in overall internal phase lag from I/C to I/C.

If better frequency stability of the carrier frequency over that provided by an L/C circuit is needed, then crystal control of the oscillators can be used. It is necessary to retain the inductor, since a dc short is required across the oscillator pins to avoid a collector current imbalance off-setting the oscillator differential pair and preventing start-up. The inductor value is chosen to resonate with the capacitor in series with the crystal at slightly less than the desired operating frequency. About 20% less will allow the inductor to be fixed tuned. Close to its series resonant frequency (normally the 3rd overtone) the crystal will provide the additional inductive reactance necessary for the circuit to oscillate. The equivalent resistance of the crystal at the operating frequency will affect the tuned circuit Q and hence the peak-to-peak drive to the modulator circuit. Smaller capacitors in series with the crystal (with corresponding changes in the inductor value) will push the operating frequency closer to anti-resonance and produce large equivalent resistances dropping the oscillator drive level. Larger capacitance values cause the operating frequency to approach series resonance and a lower equivalent resistance (approaching R_S for the crystal, which is of the order of 40Ω to 100Ω at 60 MHz). This can produce higher drive levels but risks operation at the lower overtones. To prevent lower frequency oscillation a resistor can be connected across the crystal. Also a small resistor in series with one of the collector leads will form a low pass filter with the output capacitance and suppress spurious oscillations at higher frequencies. If this is needed, resistor values less than 30Ω should be used, so that dc offsets will not prevent the oscillator from starting. For the circuit of *Figure 8*, capacitor values between 20 pF and 56 pF, with the appropriate inductor value, work well with only slightly reduced oscillator drive compared to the conventional L/C circuit.

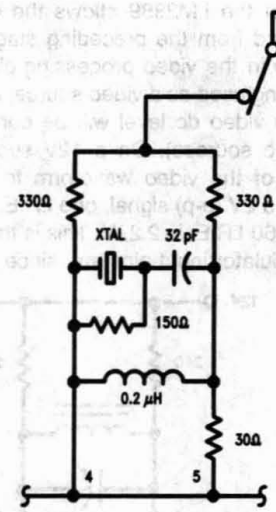

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FIGURE 8. R.F. Crystal Oscillator Circuit

The Sound Carrier Oscillator

Before moving to the R.F. output and the VSB requirements, we need to look at another signal that will be added to the baseband video—the aural intercarrier. Both the LM1889 and the LM2889 have L-C sound carrier oscillators operating at 4.5 MHz. Frequency modulation of the LM1889 sound oscillator is achieved by an external varactor diode which alters the tuning capacitance in response to the amplitude of the audio signal. The LM2889 has a similar tuned L-C oscillator but the frequency deviation is obtained by internally phase shifting the oscillator current. This is done by a low pass filter connected to the oscillator which provides a lagging phase voltage component of the oscillator waveform at the input to a differential amplifier. The current output from

Sound Modulation

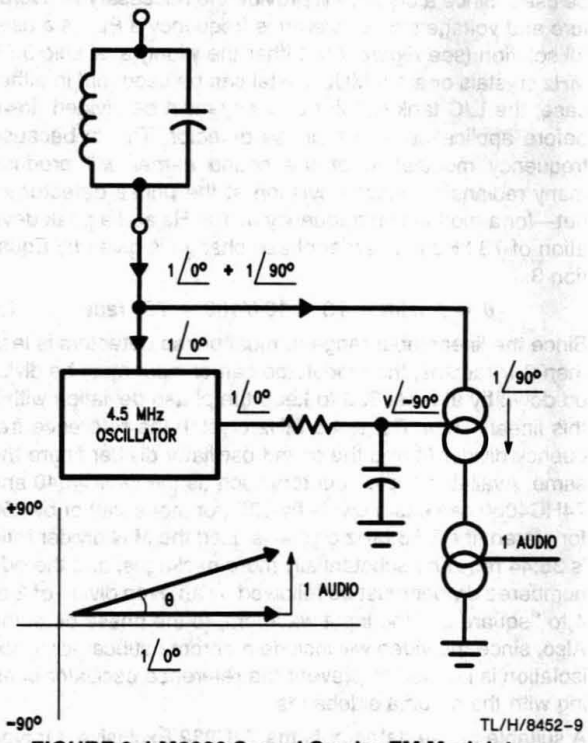

FIGURE 9. LM2889 Sound Carrier FM Modulator

this amplifier is controlled by the audio signal amplitude so that more or less of the current (now in quadrature to the original oscillator current) is added back to the tuned circuit producing the desired shift in the output frequency. Phase offsets of up to +12 degrees with increasing audio input levels will yield very low audio distortion (less than 0.2%). Also the use of a lagging oscillator waveform component reduces harmonic levels within the oscillator and a reduced possibility for undesired signals contaminating the R.F. waveform.

The tuned circuit operating Q is important in two respects. Similar to the R.F. oscillator tuned circuits, the 4.5 MHz tuned circuit should have a high loaded Q for stability, but the circuit bandwidth must also be wide enough to accommodate the FM sidebands produced by the audio modulation. For a maximum frequency deviation (Δf) and maximum modulating frequency f, the minimum bandwidth is given by Equation (1).

$$B\text{-}W \geq \Delta f\,(2.5 + 4f/\Delta f) \qquad (1)$$

The other requirement is that the maximum phase deviation of the oscillator current is able to produce the maximum frequency deviation (Δf) of the carrier. This is given by Equation (2).

$$\Delta f = 4.5 \times 10^6 \times 0.12 / Q \qquad (2)$$

Table I summarizes the results of calculating the maximum circuit Q that satisfies Equations (1) and (2) for the various monaural sound modulating standards used in the U.S. and Europe.

TABLE I

System		Δf	Modulation Bandwidth	Q_{max}	
				Modulation	Deviation
USA	Mono	25 kHz	125 kHz	≤36	≤21
	Stereo	73 kHz	400 kHz	≤12	≤7.4
UK		50 kHz	200 kHz	≤30	≤15
Continental Europe		30 kHz	150 kHz	≤36	≤22

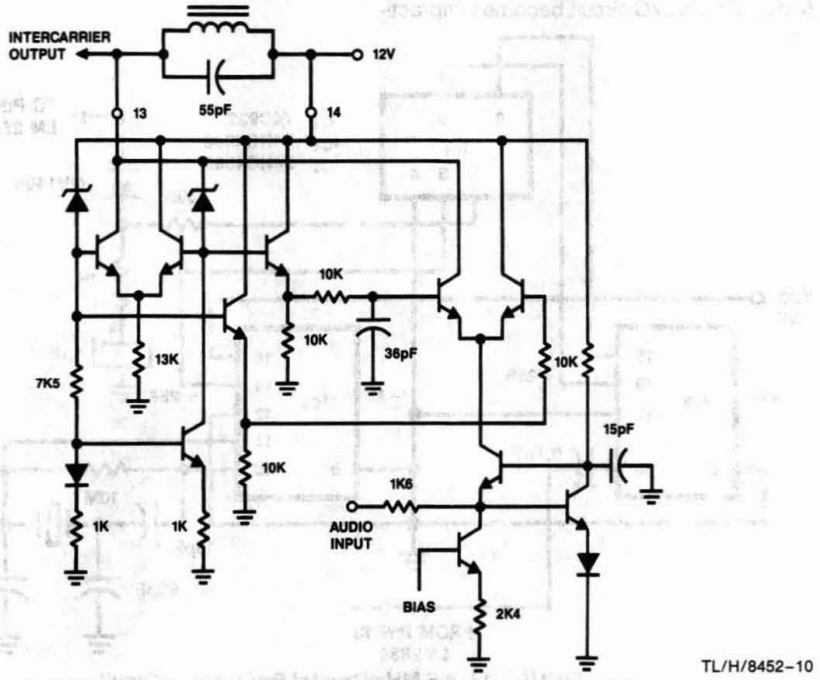

FIGURE 10. LM2889 4.5 MHz Sound Oscillator and Modulator

Sound Modulation (Continued)

Clearly the deviation phase offset dominates the circuit Q requirement.

If we choose a Q of around 10 then the oscillator drift with temperature (assuming a 2 degree phase change in oscillator current with a 50 degree rise in temperature) is of the order of −9 kHz. A typical receiver will generate less than 3% distortion at peak deviations with this much frequency drift but if better performance is required, then the circuit Q can be raised. High modulation linearity will still be retained with a Q of 20 and the oscillator maximum frequency drift will be halved. Alternatively temperature compensated tuning capacitors can be used (between N20 and N75). When higher circuit Q's than 20 are employed, increased audio input levels will produce the desired peak frequency deviations but with the possibility of increased modulation distortion. The actual operating parameters that are selected can be balanced between distortion as a result of modulation, and distortion in the receiver circuits as a result of oscillator frequency drift.

To ensure that we have a sufficient 4.5 MHz oscillator level to provide enough drive to the internal phase shift circuit, the load impedance at pin 13 should be greater than 3.5 kΩ. A second requirement is that we have enough oscillator level to generate the desired aural carrier amplitude when modulated on the picture carrier. This means that load impedances greater than 6 kΩ are desireable. At 4.5 MHz, a typical oscillator coil of 23 μH will have an unloaded Q of 55 and tune with 55 pF. For a working Q of 10, the external damping resistor is 7.5 kΩ.

Stereo Sound

The introduction in the U.S. of a multiplex stereo sound system (the BTSC system combining the Zenith MCS proposal with dbx noise reduction in the stereo difference channel) with peak carrier deviations in excess of 73 kHz puts even larger constraints on the tank circuit Q. Following the same rules as before, the maximum allowable Q for low distortion is now less than 7.4—with a loaded Q of 5 being likely. With this loaded Q, maintaining a carrier center frequency accuracy better than 5 kHz with an L/C circuit becomes impractical and other methods to set the oscillator frequency must be used. Since a crystal will provide the necessary temperature and voltage stable reference frequency a PLL is a useful solution (see *Figure 11*). Either the widely available 3.58 MHz crystals or a 4.5 MHz crystal can be used, but in either case, the L/C tank circuit frequency must be divided down before application to the phase detector. This is because frequency modulation of the sound carrier will produce many radians of phase deviation at the phase detector input—for a modulation frequency of 100 Hz and a peak deviation of 73 kHz the carrier phase change is given by Equation 3.

$$\theta = \Delta f/fm = 73 \times 10^3/100 = 730 \text{ rads} \qquad (3)$$

Since the linear input range of most phase detectors is less than 2 π radians, the modulated carrier input must be divided down by at least 233 to keep the phase deviation within this linear range. For a 4.5 MHz crystal, the reference frequency divider M and the sound oscillator divider N are the same. Available ripple counters such as the 74HC4040 and 74HC4060 can easily divide by 128 (for monaural) or by 256 for stereo. If a 3.58 MHz crystal is used the M:N divider ratio is 35:44 requiring substantially more packages, and the odd numbered divider must be followed by an even divide of 2 or 4 to "square up" the input waveform to the phase detector. Also, since the video will include a chroma subcarrier, good isolation is needed to prevent the reference oscillator beating with the chroma sidebands.

A suitable phase detector is the 74C932 Exclusive- Or type with a sensitivity of 1.6 volts/radian. The filter at the detector output prevents the input modulation from reaching the varactor diode and distorting the audio. Even so, the loop filter must have some ac bandwidth for a reasonable acquisition time and other dynamic characteristics. The components shown in *Figure 11* have been chosen such that with a varactor sensitivity of 100 kHz/volt the loop has a hold-in range of over ±150 kHz, with a lock-up time of less than 0.5 seconds. The T.H.D. is less than 1% for a 400 Hz modulating frequency producing 25 kHz deviation of the carrier. The accuracy of the sound carrier frequency is, of course, that of the crystal used for the reference oscillator.

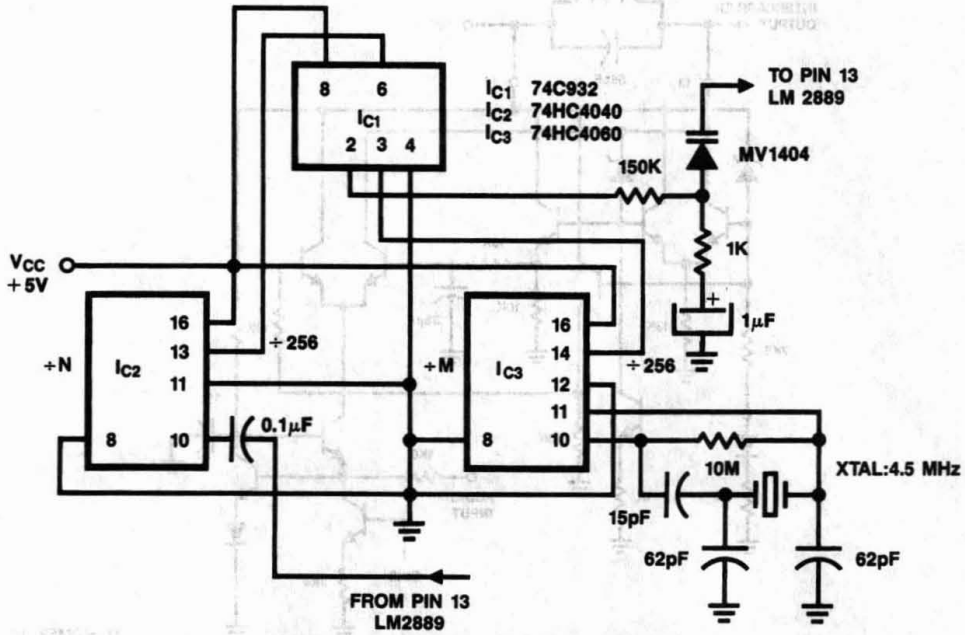

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FIGURE 11. 4.5 MHz Crystal Reference Circuit

Audio Processing For Sound Carrier Modulation

With the proper tuned circuit Q (see Table I), a linear increase in the amplitude of the audio signal will produce a correspondingly linear increase in the frequency deviation. Television receiver sound circuits in the U.S. have a 75 μs de-emphasis and in Europe frequencies above 3.2 kHz (50 μs) are de-emphasized at a 6 dB/octave rate. This is done to help improve the S/N ratio of FM reception and the transmitter incorporates the complementary pre-emphasis characteristic—above 2.1 kHz the audio frequencies are boosted at a 6 dB/octave rate. The consequence of this modulation scheme is that if a 0 dB peak signal amplitude at 15 kHz is capable of producing a 25 kHz deviation than a similar amplitude signal at 400 Hz will produce a peak deviation of only 3 kHz—a loss of some 18 dB in S/N ratio for the midband frequencies. Broadcasters usually employ compressors to enable high modulation levels to be obtained at mid-band frequencies without overmodulating high frequencies. If the audio input to the LM2889 is being sourced from an original broadcast (a scrambled signal decoder output for example) than this audio—without de-emphasis—can be directly applied to pin 1 of the LM2889, and the overall input level is adjusted so that the modulation limits are not exceeded except for brief intervals (less than 10 instances per minute). When the audio has not already been processed a different set of conditions will apply and an audio pre-emphasis network is required at pin 1.

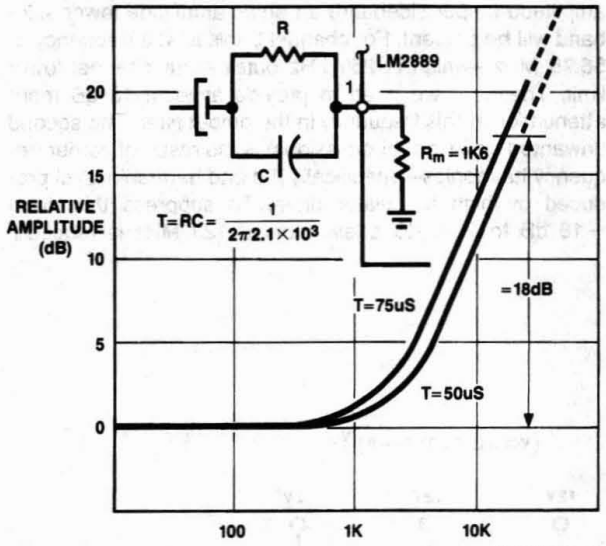

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FIGURE 12. Audio Pre-emphasis

Since the audio source is likely to be at a relatively low impedance (a pre-amplifier output), the pre-emphasis network will also be used to attenuate the level of the average audio input to the LM2889 as well as providing a relative boost to the higher frequencies. The input sensitivity of the audio modulator is 150 Hz/mV which means that 118 mVrms will give a peak deviation of 25 kHz.

Next we have to decide what signal frequency and amplitude to use in calibrating the audio input. Unfortunately the 75 μs time constant for FM broadcasting was chosen at a time when equipment limitations meant there was relatively low spectral energy at higher frequencies. Today, modern audio material is not well suited to boosting above 2.1 kHz since energy peaks at only −6 dB can be obtained at 10 kHz. A further complication is the ability of the audio level meter to predict high energy peaks. If a conventional VU meter is used, peak levels of +10 dB are possible while the meter is indicating OVU. Obviously without processing the audio to keep it within predetermined limits, the input level calibration will be somewhat empirical in nature.

If we assume the decrease in spectral energy above 10 kHz is such that overmodulation peaks above this frequency are unlikely to occur, then we can allow a signal at 10 kHz to produce full modulation deviation. Since the amplitude of most audio signals at 10 kHz is at least 6 dB below the midband frequency level, we can calibrate the audio input with a −6 dB amplitude, 10 kHz tone to produce 100% deviation. As we shall see later, a frequency close to 10 kHz will make the measurement of actual peak deviations very easy indeed. With the standard pre-emphasis network, at signal frequencies less than 2 kHz, the modulating signal amplitude at pin 1 will be −8 dB below the anticipated peak 10 kHz level producing 100% modulation. This corresponds to a modulator input level of 118/2.2 = 45.4 mVrms. The

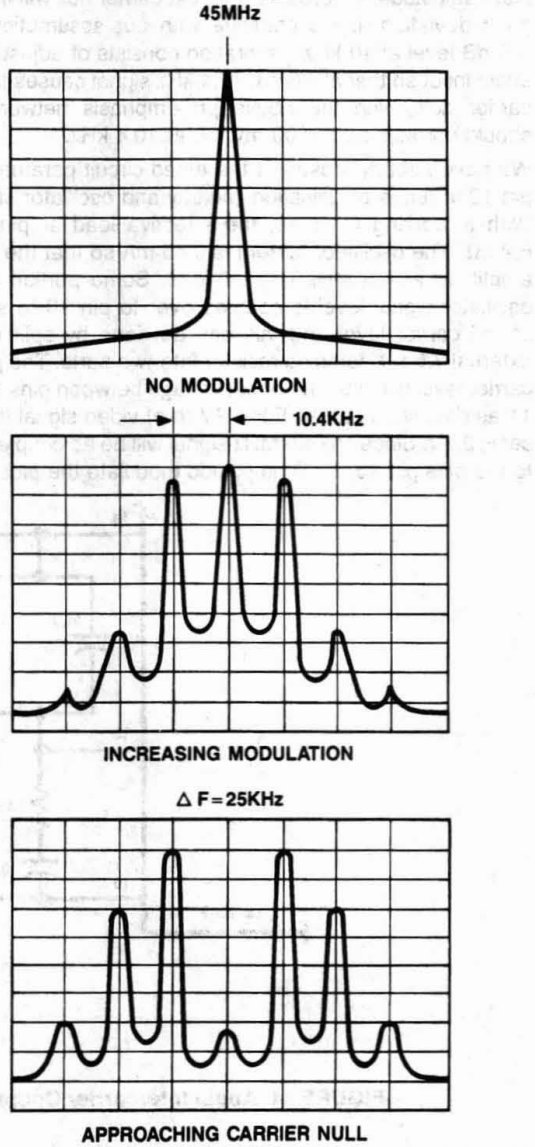

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FIGURE 13. FM Spectrum with Increasing Audio Amplitude (f mod = 10.4 kHz) 4.5 MHz Sound Carrier Level

Audio Processing For Sound Carrier Modulation (Continued)

input resistance at pin 1 is 1.5 kΩ so R1 = 30 kΩ, if we assume an input source level of 1 Vrms at 400 Hz. For a 2.1 kHz breakpoint, C = 0.0027 μF.

Anyone who has observed the output from an FM circuit with a spectrum analyzer will know that for a fixed modulating frequency the output spectrum will consist of the carrier frequency component and sidebands spaced by the modulating frequency from the carrier. As the modulation amplitude is increased (the modulation index m becomes larger), the carrier decreases to a null and then increases again. The modulation indices for which carrier nulls occur can be calculated and for our purposes it is important to know that the first carrier null occurs at m = 2.4048. For a system maximum deviation of 25 kHz the modulating frequency f is given by:

$$f = 25 \times 10^3/2.4048 = 10.4 \text{ kHz} \quad (4)$$

Therefore, if we use an input frequency of 10.4 kHz, as the input amplitude is increased the first carrier null will indicate peak deviation. If we continue with our assumption of a −6 dB level at 10 kHz, calibration consists of adjusting the audio input so that a −6 dB, 10.4 kHz signal causes the first carrier null. With the above pre-emphasis network, this should correspond to 500 mVrms at 10.4 kHz.

We have already looked at the tuned circuit parameters at pin 13 in terms of deviation linearity and oscillator stability. With a working Q of 10, the effective load at pin 13 is 6.2 kΩ. The oscillator current is 0.45 mA so that the output amplitude at 4.5 MHz is 3.6V (p-p). Some portion of this oscillator signal level is coupled over to pin 10 to set the sound carrier level and this can be done by splitting the external 7.5 kΩ damping resistor into two parts. The picture carrier level is set by the offset voltage between pins 10 and 11 as described earlier. For a 2V (p-p) video signal this offset is 2.3V. Since the 4.5 MHz signal will be ac coupled over to the bias pin 10, it will amplitude modulate the picture RF carrier. This is conventional AM and a 4.6V (p-p) signal will yield sound carrier sidebands at −6 dB relative to the picture carrier. If we require a sound carrier amplitude at −17 dB, the signal coupled to pin 10 must be 11 dB below 4.6V (p-p), or 1.3V (p-p). This is obtained by using a 4.7 kΩ resistor coupled through a 0.1 μF capacitor to pin 10, and a second 2.7 kΩ resistor connected to the wiper arm of the potentiometer used to set the video modulation depth. The effect of the potentiometer setting on the aural carrier level is eliminated by a 0.1 μF capacitor connected from the wiper arm to ground. However, since the impedance presented by the potentiometer will, for all practical purposes, be relatively constant, the capacitor could be removed and the parallel resistance of the upper and lower arms of the potentiometer network used to provide the second resistor of 2.7 kΩ. If the video input level is well controlled, it may be possible to replace the potentiometer with a fixed divider.

The final part of the design concerns the output stage, and involves meeting the constraints applied by any regulatory agency. In the U.S., apart from the need to restrict the peak carrier output level to less than 3 mVrms in 75Ω, we have two signals present in the output whose level will exceed the spurious emission limit of −30 dB with respect to the peak carrier level. One of these signals is the result of amplitude modulating the 4.5 MHz intercarrier audio on the picture carrier. Apart from the desired −17 dB sound carrier amplitude (upper sideband) an equal amplitude lower sideband will be present. For channel 3 this is at a frequency of 56.75 MHz—which is 250 kHz outside our channel lower limit. Therefore we need to provide at least 13 dB more attenuation at this frequency in the output filter. The second unwanted emission (or emissions) is the result of carrier frequency harmonics—specifically the 2nd harmonic level produced by high modulator drive. To suppress this, from −18 dB to −30 dB attenuation at 123 MHz is required.

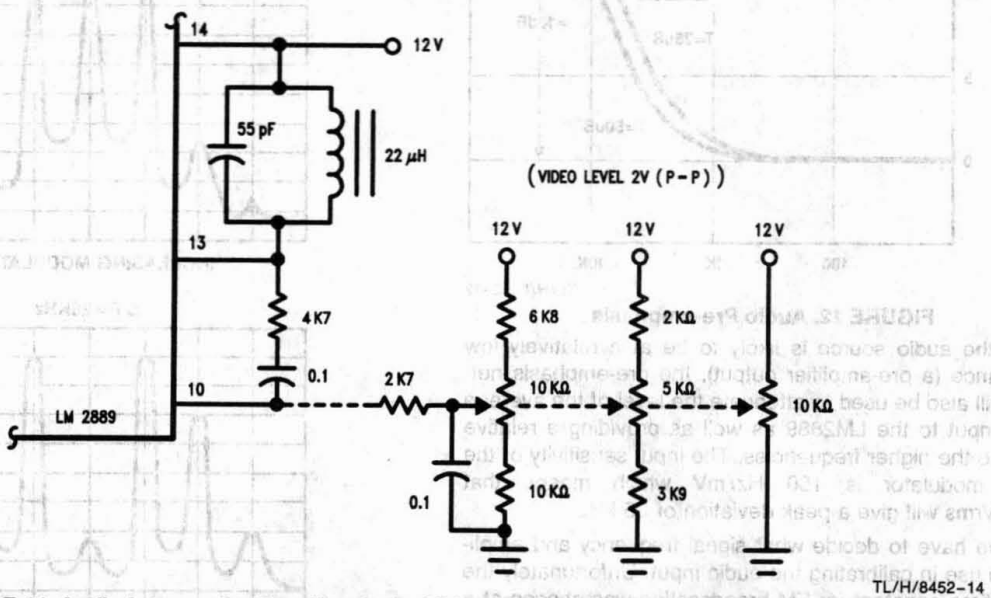

FIGURE 14. Audio Intercarrier Coupling to the Video Modulator R.F. Output and V.S.B. Filter

Audio Processing For Sound Carrier Modulation (Continued)

With a properly constituted baseband signal modulating the carrier, these are the only intrinsic unwanted emissions we are concerned with. Normal video modulation components appearing in the lower sideband will not have sufficient amplitude and do not extend beyond the lower channel limit. Even so, the filter requirements are not trivial.

If L-C filters are used, this can be done with three coils per channel but some alignment procedure will be required. Fortunately SAW filters are available from several sources which, although more expensive than the equivalent L-C filter, avoid the cost of production alignment. Usually the SAW filter will have a substantially greater insertion loss, but the LM2889 has enough output level to compensate for this. Both single channel and dual channel filters are available and in the latter case the LM2889 dual oscillator/modulator configuration enables easy dc switching between channels. A coil may be required, connected across the SAWF input, to tune out the SAWF input capacitance.

The load resistors connected to pins 8 and 9 will set the LM2889 conversion gain, which for 75Ω is typically 20 mVrms R.F. carrier per volt offset at the input pins 10 and 11. The actual load will include the input resistance of the filter. Since the output of the filter will normally be terminated in 75Ω to match the cable (and provide triple transit echo suppression for a SAWF), the best way to choose the load resistor is to monitor the output to the cable and apply a dc offset between pin 10 and 11 that is equivalent to the expected video input. The resistor is then chosen to give the desired peak carrier level of 2.5 mVrms. The carrier should be unmodulated since downward modulation will reduce the mean carrier level by as much as 2–3 dB.

If the offset voltage between pin 10 and 11 is reduced, a check can be made on the residual carrier level at the output. This residual level is the result of oscillator feedthrough in the modulators and external coupling from the oscillator tuned circuits. The residual carrier level is normally better than −26 dB below the peak carrier level, ensuring good modulation linearity. High levels of residual carrier can be caused by coupling through ground or power supply leads. A good technique to minimize the effect of unwanted pick-up is to decouple the supply voltage to pin 8 and 9 load resistors over to the output connector shield ground. This removes at the output any carrier signal on the supply line to the load resistors.

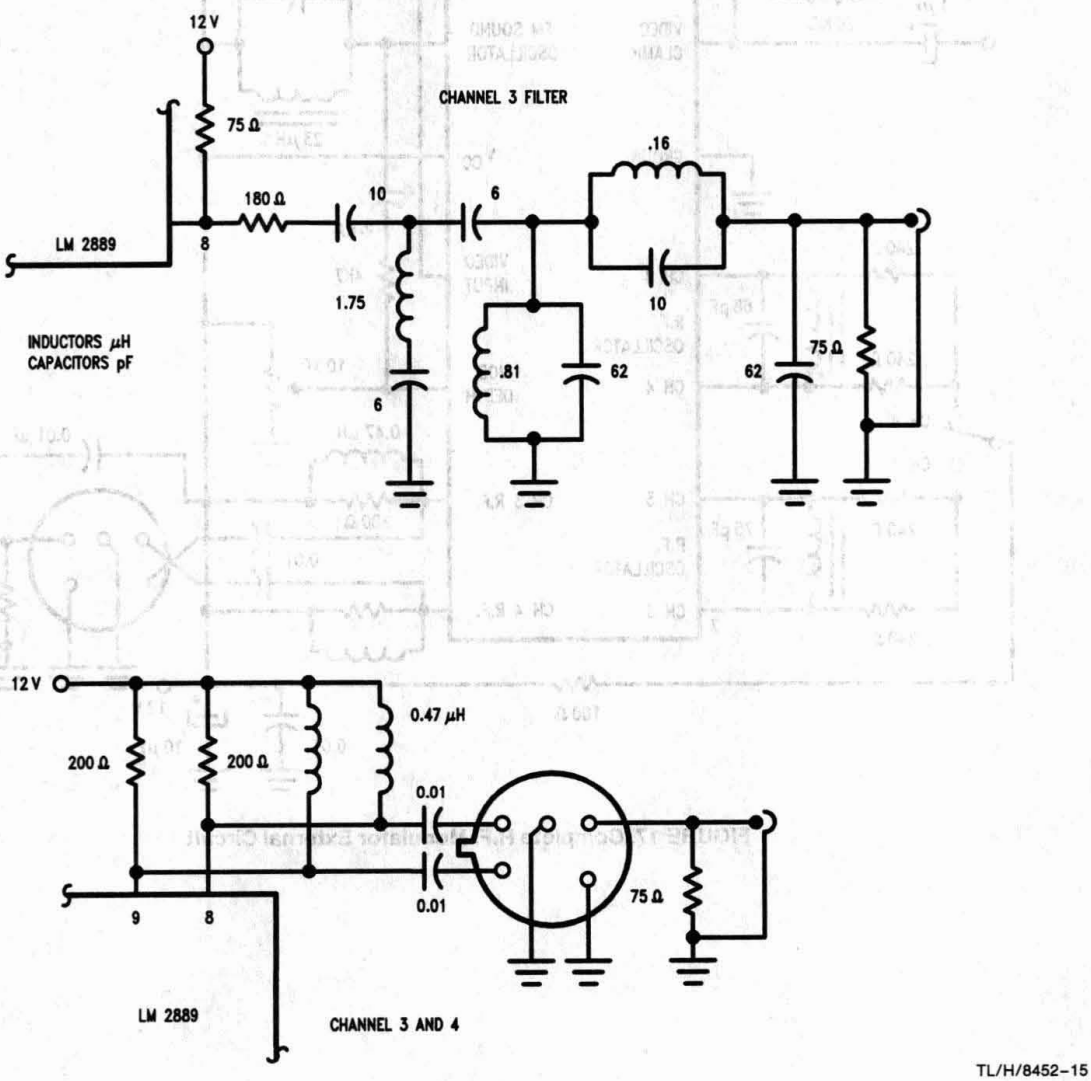

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FIGURE 15. Vestigial Sideband Filters

Audio Processing For Sound Carrier Modulation (Continued)

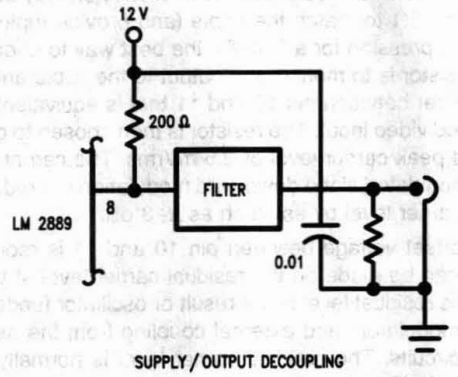

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FIGURE 16. R.F. Decoupling at the Output

Sources: SAWFs

Crystal Technology, Inc.
1035 E. Meadow Circle
Palo Alto, CA 94303

Kyocera International, Inc.
8611 Balboa Ave.
San Diego, CA 92123

MuRata Corp. of America
1148 Franklin Rd. S.E.
Marietta, GA 30067

CRYSTALS

Saronix
4010 Transport at San Antonio Rd.
Palo Alto, CA 94303

COILS

Toko America, Inc.
5520 W. Touhy Ave.
Skokie, Ill. 60077

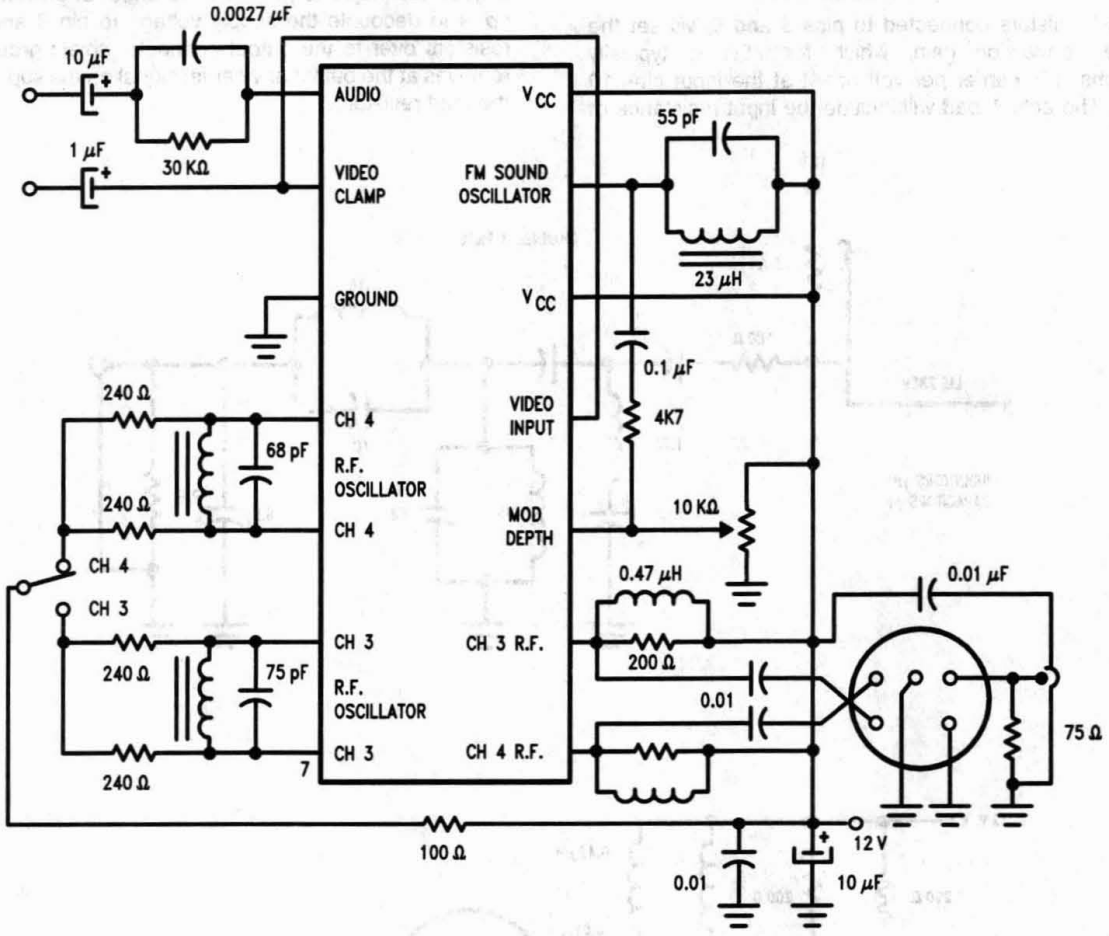

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FIGURE 17. Complete R.F. Modulator External Circuit

Designing with the LMC835 Digital-Controlled Graphic Equalizer

National Semiconductor
Application Note 435

INTRODUCTION

Because of the increasing use of digital techniques in consumer audio equipment, National has developed a digitally controlled graphic equalizer—the LMC835. This chip replaces the potentiometers used in a conventional graphic equalizer with digitally controlled step-variable resistors, thereby allowing computer manipulation of an analog signal path. The LMC835 is configured such that a high degree of flexibility remains in the overall equalizer design, without compromising the quality of the analog signal path.

Graphic equalizers are used to control the frequency response of an audio system. An equalizer contains a number of fixed-frequency bandpass/notch filters with a gain control for each filter. Resonances and nulls in the frequency response of an audio system are easily compensated with proper adjustment of the equalizer.

A single LMC835 contains enough step-variable resistors for a stereo, 7 band equalizer with 1 dB steps covering a ±12 dB range. Up to 14 monaural bands can be accommodated by paralleling the two halves of the chip. Because the internal step-variable resistors are implemented with inherently well-matched SiChrome resistors, accurate 1 dB control steps are possible. The LMC835 is available in a plastic 28-pin dual-in-line package.

The digital sections of a finished equalizing instrument will include a microprocessor, pushbutton controls, a large, multisegment display and any necessary circuitry to drive the display. The analog sections will contain the LMC835 and a number of associated operational amplifiers. Care has been taken in the design of the LMC835 to isolate sensitive analog circuitry from contamination by the digital sections. The analog sections of the equalizer will be considered first.

BASIC EQUALIZER TOPOLOGY

Many diverse equalizer circuit topologies have been commercially produced. A topology that works well within the constraints of step-variable resistors and uses a minimum of signal-path gain stages has been chosen for the LMC835.

The basic equalizer circuit shown in *Figure 1* uses two operational amplifiers in the signal path. This circuit represents ½ of an LMC835. R_B, R_C, R_{V1} through R_{V7}, and the selector switches are included on-chip. The first amplifier provides the boost (bandpass) function, while the second amplifier buffers the cut (notch) function. For any one frequency band both boost and cut functions are possible, but they are never selected simultaneously. Redundant external analog circuitry is therefore eliminated by exclusively switching each tuned circuit to either boost or cut.

The amount of boost or cut is controlled by on-chip variable resistors R_{V1} through R_{V7}. These are designed to ratio with R_B and R_C for perfect 1 dB steps. An optional 6 dB control range with 0.5 dB steps is discussed later in this application note.

Step-variable resistors were chosen for the LMC835 since they lend themselves well to digital control. Each variable

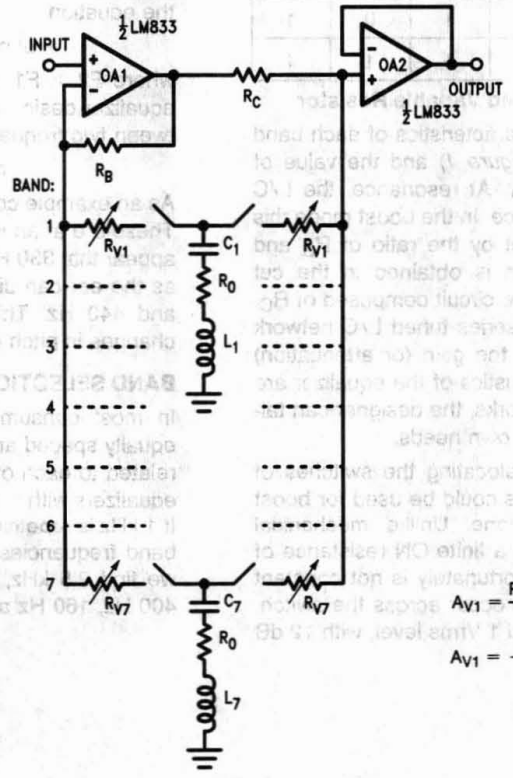
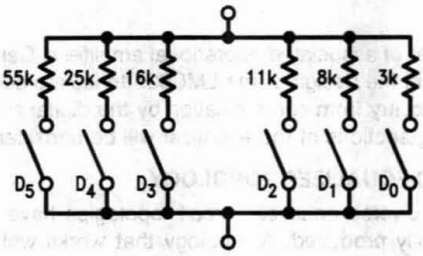


FIGURE 1. Basic Equalizer Topology

resistor shown in *Figure 1* is actually 6 fixed-value SiChrome resistors connected in parallel through CMOS FET switches. This is detailed in *Figure 2*. By selecting appropriate combinations of these 6 fixed resistors, better than 0.1 dB accuracy for each of 12 steps is obtained. The coding sequence is discussed in the programming section later.



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LEVEL	D_5	D_4	D_3	D_2	D_1	D_0
FLAT	0	0	0	0	0	0
1 dB	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	0	1	0	0	0
4	0	0	0	1	0	0
5	0	0	0	0	1	0
6	0	1	0	0	1	0
7	1	0	1	0	1	0
8	0	1	0	1	1	0
9	0	0	0	0	0	1
10	1	0	1	0	0	1
11	1	0	1	1	0	1
12	1	0	1	1	1	1

FIGURE 2. Digitally Controlled Variable Resistor

The frequency and bandwidth characteristics of each band are set by the L/C networks (*Figure 1*) and the value of each associated variable resistor. At resonance, the L/C network reduces to zero impedance. In the boost mode this leaves amplifier I with a gain set by the ratio of R_B and $R_O + R_V$. Conversely, attenuation is obtained in the cut mode with amplifier II buffering the circuit composed of R_C, R_O and R_V. Off resonance, the series tuned L/C network presents a high impedance and the gain (or attenuation) reduces to 1. Since the characteristics of the equalizer are determined by external L/C networks, the designer can tailor the equalizer circuit to suit his own needs.

Although it may seem that by relocating the switches of *Figure 1* a single bank of resistors could be used for boost and cut, this has not been done. Unlike mechanical switches, CMOS switches exhibit a finite ON resistance of several hundred ohms which unfortunately is not constant when large signal voltage swings occur across the switch. For a signal source with a nominal 1 Vrms level, with 12 dB of boost selected the signal swing would produce unacceptable distortion. By locating the switches between the resistor banks and the resonant circuit the actual peak signal swing across the switch is reduced to well within a linear operating region of the switches. The complete circuit with a 1 kHz, 1 Vrms signal input exhibits less than 0.003% distortion even with 12 dB boost.

BAND FREQUENCY SELECTION

Two basic equalizer types are in common use: one type has fixed band frequencies, the second type has variable band frequencies that can be tuned to allow control at specific points. The first type (graphic equalizer) is by far the most common, and the second type (parametric equalizer) finds limited popularity owing its cost and difficulty of use. The LMC835 circuit topology described here is intended for fixed band frequency applications.

The selection of band frequencies is entirely independent of the LMC835 as the chip has no frequency-sensitive or frequency-determining characteristics. There are two basic methods for selecting frequencies: 1) spread the bands out evenly over some desired frequency range, or 2) space the bands closely over the range where more control is desired, and space them more widely elsewhere. An example of this second technique is ***modified*** spacing where bands are tightly spaced at the low frequencies to allow control where it is most useful. The few remaining bands are spaced more widely at the higher frequencies (>500 Hz). Once the band frequencies have been selected, circuit Q, and the values for the series tuned circuits may be calculated. The following formulae find general use in equalizer design.

Band spacing is often measured in units of octaves. An octave covers a frequency ratio of 2:1, e.g. the frequencies between 1000 and 2000 Hz constitute an octave as do the frequencies between 200 Hz and 400 Hz. The number of octaves contained between any two frequencies is given by the equation

$$\#\ \text{of octaves} = \text{LOG}(F_2/F_1)/\text{LOG}(2) \qquad (1)$$

where F2 > F1. Another formula used in conjunction with equalizer design is that which finds the musical center between two frequencies:

$$\text{center frequency} = \sqrt{F_2 F_1} \qquad (2)$$

As an example consider 2 frequencies, 220 Hz and 440 Hz. These are at an interval of 1 octave. At first glance it might appear that 330 Hz is halfway between these two, but as far as the ear can discern, 311 Hz is equidistant from 220 Hz and 440 Hz. This is because the ear hears logarithmic changes in pitch equally.

BAND SELECTION

In most consumer equalizers the band frequencies are equally spaced and centered around 1 kHz. The bands are related to each other by some factor. For example, 7-band equalizers with a 1 kHz center frequency use a factor of 2.5. If 1 kHz is repetitively multiplied and divided by 2.5 the other band frequencies will be found: multiplying (and rounding) we find 2.5 kHz, 6.3 kHz and 16 kHz, and dividing yields 400 Hz, 160 Hz and 63 Hz.

If the desired control range is defined, the center frequency can be found with the formula

$$\text{center band} = \sqrt{F_{MAX}F_{MIN}} \quad (3)$$

and the factor

$$\text{factor} = (F_{MAX}/F_{MIN})^{(1/d)} \quad (4)$$

F_{MIN} represents the lower −3 dB point of the "bottom" band when it is in full boost and all other bands are flat. F_{MAX} is the analogous higher −3 dB point of the "top" band. "d" is the number of bands. These formulae can be combined as

$$F_n = \left(F_{MAX}^{\frac{2n-1}{2d}}\right)\left(F_{MIN}^{\frac{2(d-n)+1}{2d}}\right) \quad (5)$$

where "n" is the band number (from 1 to d).

A common misconception about equalizers is that the band frequencies relate to the frequency response of the instrument. This is not true at all—the flat frequency response of the equalizer is completely independent of the band frequencies. Even so, many equalizer designs have bands extending beyond the normal range of hearing while compromising control at low frequencies.

There is no magic in spacing band frequencies. While equal spacing can offer control over a wide frequency range, it is possible to enhance control over a limited range by closely spacing the bands in one area while spreading out the remaining bands elsewhere. This technique (modified spacing) is especially useful at frequencies below 500 Hz where speakers and listening environments have pronounced resonances and antiresonances.

SELECTION OF MAXIMUM Q

The maximum desired Q of each band occurs at full boost or full cut and is set by the values of $R_O + R_V$, L_O and C_O. Mathematically Q_{MAX} is a function of the adjacent band frequencies:

$$Q_{MAX} = \frac{\sqrt{F_2}}{\sqrt{F_3} - \sqrt{F_1}} \quad (6)$$

where Q_{MAX} is the maximum Q of F_2 during full cut or boost, and F_3 and F_1 are the adjacent band frequencies. The highest and lowest bands on an equalizer have only one adjacent band. In this case:

$$Q_{MAX} = \text{ABS}\left(\frac{\sqrt{F_1F_2}}{F_2 - F_1}\right) \quad (7)$$

where F_1 is the adjacent band. In terms of a factor:

$$Q_{MAX} = \frac{\sqrt{\text{factor}}}{\text{factor} - 1} \quad (8)$$

In terms of F_{MIN} and F_{MAX}:

$$Q_{MAX} = \frac{2d\sqrt{F_{MAX}/F_{MIN}}}{d\sqrt{F_{MAX}/F_{MIN}} - 1} \quad (9)$$

The formulae for Q_{MAX} cause the −3 dB points of any two bands to occur at approximately the same frequency. If this is not desired, the maximum Q may be set to any value by appropriately designing the resonant networks. Higher values of Q give greater definition between bands while lower values of Q gives less ripple response between adjacent bands.

Once the maximum Q has been determined, L and C (from *Figure 1*) may be calculated:

$$L_n = 2270\, Q_{MAX}/\omega_n \quad (10)$$

$$C_n = 1/(\omega_n^2 L_n) \quad (11)$$

Note that 2270Ω is the minimum resistance including the 680Ω resistor (R_O), switch resistance and SiChrome resistance (R_V) as shown in *Figure 1*.

Using the typical 7-band consumer center frequencies (factor = 2.5) and a Q_{MAX} = 1.05 (from equation 8), the following values are calculated:

Band	Frequency (Hz)	L_O (mH)	C_O (nF)
1	63	6040	1060
2	160	2380	416
3	400	952	166
4	1000	381	66.5
5	2500	152	26.6
6	6300	60.4	10.6
7	16000	23.8	4.16

The inductances required at low frequencies would seem prohibitive, but there is an easy solution. The LMC835 is designed for use with series resonant networks. Since the inductances required are quite large and discrete realizations would be expensive, a simulated inductor, also called a gyrator, may be used.

GYRATOR DESIGN

The properties of an inductor may be simulated by a simple op amp circuit (often called gyrator) as shown in *Figure 3*. The impedance seen at the input terminal is $j\omega R_L R_O C_L$ and the inductance is given by the product $R_L R_O C_L$. As shown, R_O represents a loss resistance in series with the inductor. The internal SiChrome resistors are designed to accommodate an R_O of 680Ω.

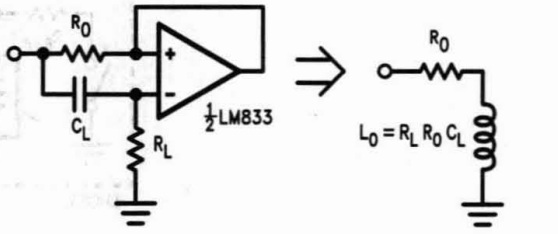

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FIGURE 3. Simulated Inductor

At high frequencies the impedance of the gyrator should approach infinity, but several effects limit the maximum impedance. The result is an increase in high frequency gain as contributed by the boost section, and a decrease in high frequency gain as contributed by the cut section.

Gyrator impedance is ultimately limited by the loading effects of R_L, especially for smaller inductances since R_L necessarily becomes small. To reduce loading effects keep $R_L > 47\ k\Omega$. In extreme cases C_L and R_L can be buffered by a second op amp as shown in *Figure 4*.

The voltage divider action caused by stray capacitance at the junction of C_L and R_L also reduces gyrator impedance. This effect is minimized by keeping $C_L > 470$ pF. Bootstrapping (*Figure 5*) is a viable alternative for reducing the effects of stray capacitance.

An important gyrator performance factor is the gain and phase of the op amp at high frequencies. An op-amp unity-gain bandwidth of at least 10 MHz is recommended since poor frequency response will reduce the gyrator impedance at high frequencies. Phase shift through the op amp causes the gyrator to become capacitive. The LM833 is an excellent choice for a gyrator as its bandwidth is well over 10 MHz, and it is unity gain stable.

Signal path stability and high frequency gain accuracy are affected by the feedback loop around the first amplifier of *Figure 6*. Most op amps cannot tolerate stray capacitance on their inverting input since it reduces the phase margin. This leads to increased gain at high frequency, if not instability. A 100 pF feedback capacitor compensates most op amps with little effect on the audio performance of the equalizer.

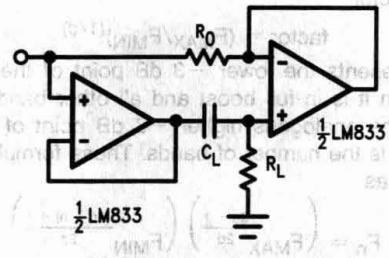

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FIGURE 4. Buffered Gyrator

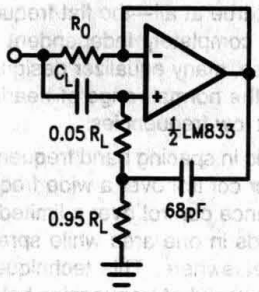

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FIGURE 5. Bootstrapped Gyrator

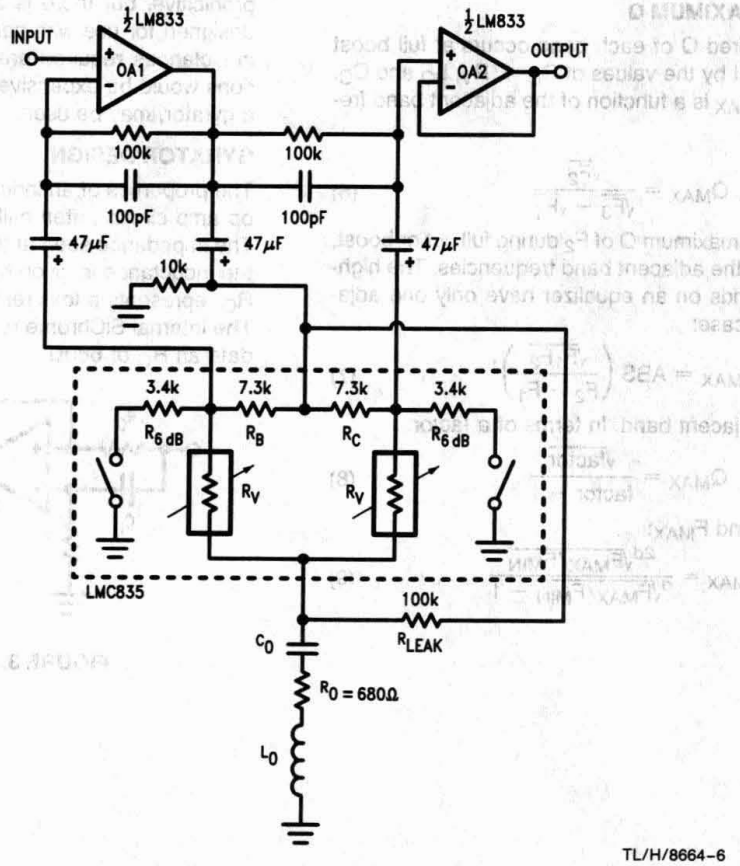

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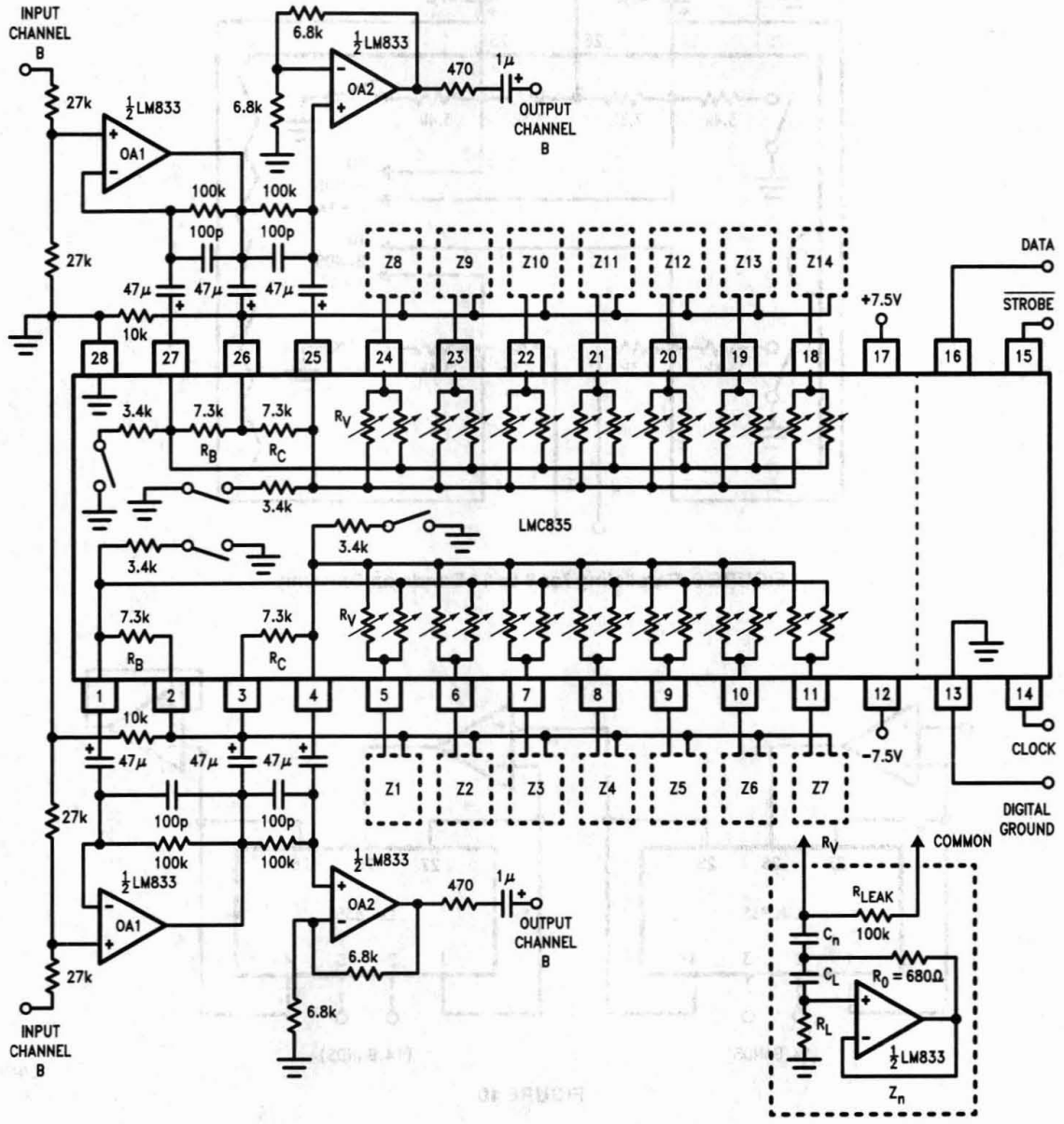
FIGURE 6. AC Coupled Signal Path

SWITCH LEAKAGE

When the CMOS switches are OFF, a small leakage current of typically 1 nA can flow either into or out of any of the gyrator connections. This current charges C_O until a state of equilibrium is reached. If one of the switches is now closed, the charge stored on C_O will be injected into the signal path possibly causing an audible "pop" in the output. A 100 kΩ resistor is all that is necessary (as shown in *Figure 6*) to bleed this charge away and prevent pops. This results in a gain error or less than 0.2 dB at maximum boost or cut.

Provision is made to convert the equalizer to a +/−6 dB control range. The 3.4 kΩ resistors shown in *Figure 6*, when selected, drop the control range to +/−6 dB with approximately 0.5 dB steps. When the 3.4 kΩ resistors are selected, the resultant changes in the signal path DC gain can produce pops. Op amp input offset voltage and bias current are the root cause; the solution is to AC couple the signal path to the LMC835. In addition to the three 47 μF coupling capacitors of *Figure 6*, two 100 kΩ resistors are also necessary to provide a DC path around the op amps. Since the majority of applications require a "popless" configuration, the internal 7.3 kΩ resistors have been adjusted to accommodate the effects of the external 100 kΩ resistors. If DC coupling is not used, the 100 kΩ signal path resistors should be included to insure gain accuracy.

A complete seven-band graphic equalizer circuit is shown in *Figure 7*. 470Ω resistors are used in series with the output amplifiers to isolate capacitive loads that could cause instability. To increase signal handling capability the input is attenuated 6 dB by two 27 kΩ resistors and then equally amplified in the output buffer. With this configuration the maximum signal level at the input (with flat equalization) is about 9 Vrms yet the LMC835 sees only one-half of this—less than its +/−7.5V supply limitation. Clipping is still possible if, for instance, a 9 Vrms input is boosted 12 dB. There is sufficient headroom to handle full boost on a 2 Vrms input signal. Gyrator component values are shown in *Figure 8*.



TL/H/8664–7

FIGURE 7. Complete 7-Band Graphic Equalizer

Z_n	f_O(Hz)	C_O(F)	C_L(F)	R_L(Ω)	R_O(Ω)
Z1, 8	63	1μ	100n	100k	680
Z2, 9	160	470n	33n	100k	680
Z3, 10	400	150n	15n	100k	680
Z4, 11	1k	68n	6.8n	82k	680
Z5, 12	2.5k	22n	3.3n	82k	680
Z6, 13	6.3k	10n	1.5n	62k	680
Z7, 14	16k	4.7n	680p	47k	680

FIGURE 8. Gyrator Component Values

PARALLELING FOR MORE BANDS

The two halves of an LMC835 can be paralleled to provide up to 14 monaural bands. Paralleling (*Figure 9*) is accomplished by connecting pin 1 to pin 27 and pin 4 to pin 25. Pins 2 and 3 are left open, and any unused gyrator pins are simply tied off to ground. The ±6 dB range is selected by activating only one set of ±6 dB resistors, and either set will do.

In applications requiring 15 to 28 bands a second LMC 835 can be cascaded as shown in *Figure 10*. Note that the output buffer of the first LMC835 is made redundant by the input amplifier of the second LMC835. Therefore only 3 signal path op amps are required instead of 4.

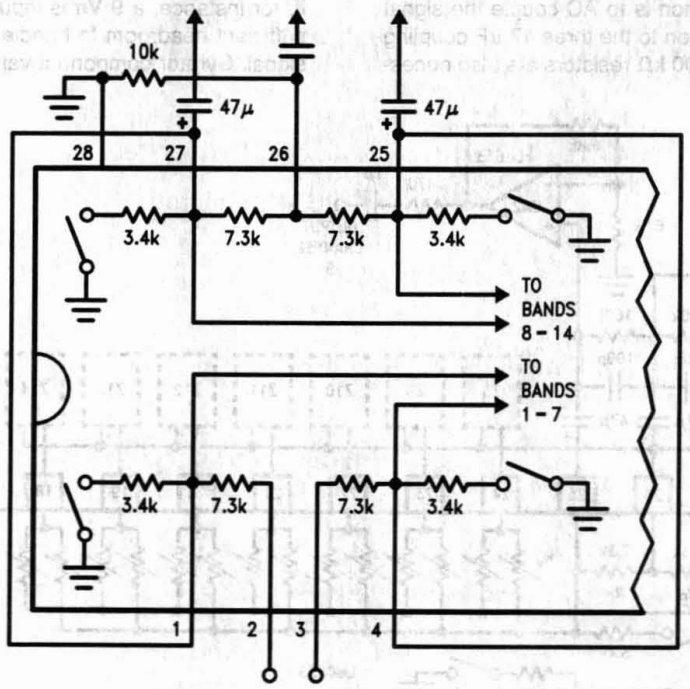


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FIGURE 9. Paralleling for 8 to 14 Bands on One Chip

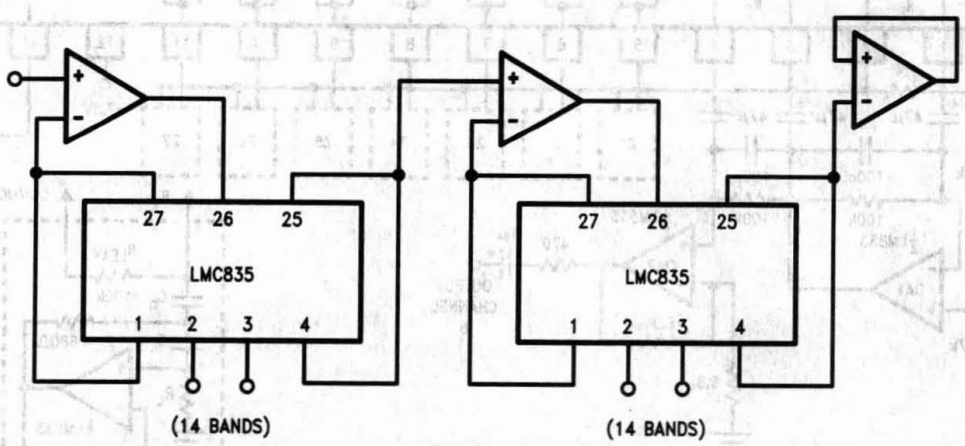

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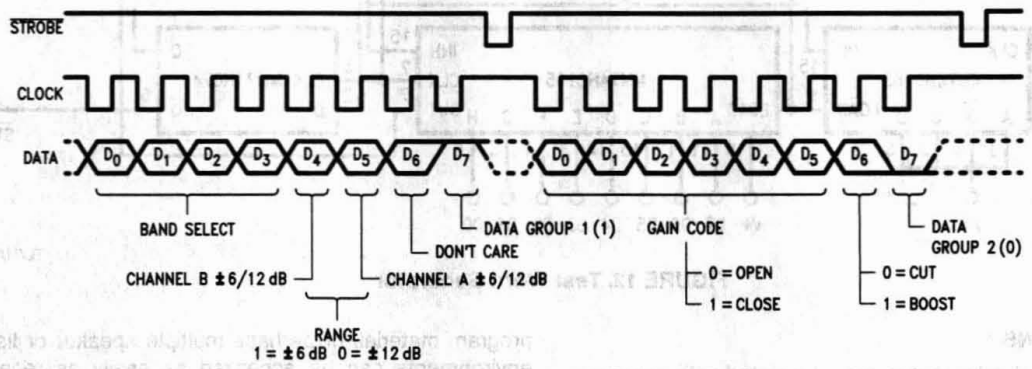
FIGURE 10

PROGRAMMING

A three wire interface consisting of a DATA, CLOCK and STROBE line (*Figure 7*) is provided for programming the LMC835. DATA bits are shifted in to an internal serial register on positive CLOCK edges. This data is then latched (and executed) by a low-going pulse on the STROBE pin. A separate digital ground pin is provided to prevent contamination of the sensitive analog signal path.

Programming is accomplished with two 8-bit words. The first word selects a band for adjustment and selects either of ±6 or ±12 dB control range. The second 8-bit word selects boost or cut and the desired level for the band previously addressed. A timing diagram is shown in *Figure 11*. Note that bit D0 is shifted in first, D7 last. *Figure 12* shows the coding used for band and gain selection. With the maximum clock rate of 500 kHz, the entire equalizer can be programmed in less than 500 μs.

Parallel entry of data is possible using a simple word generator circuit as shown in *Figure 13*. A clock signal is applied continuously, and D0 through D7 are loaded and shifted into the LMC835 commencing with the positive edge of a start pulse. CLOCK, DATA and STROBE signals are all automatically generated and sequenced. D0 through D7 could be supplied by a parallel data bus or even toggle switches.



TL/H/8664–9

FIGURE 11. Timing Diagram

DATA I (BAND SELECTION)

D7	D6	D5	D4	D3	D2	D1	D0	(CH A: BAND 1~7, CH B: BAND 8~14)
H	X	L	L	L	L	L	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, NO BAND SELECTION
H	X	L	L	L	L	L	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 1
H	X	L	L	L	L	H	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 2
H	X	L	L	L	L	H	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 3
H	X	L	L	L	H	L	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 4
H	X	L	L	L	H	L	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 5
H	X	L	L	L	H	H	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 6
H	X	L	L	L	H	H	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 7
H	X	L	L	H	L	L	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 8
H	X	L	L	H	L	L	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 9
H	X	L	L	H	L	H	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 10
H	X	L	L	H	L	H	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 11
H	X	L	L	H	H	L	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 12
H	X	L	L	H	H	L	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 13
H	X	L	L	H	H	H	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 14
H	X	L	L	H	H	H	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, NO BAND SELECTION
H	X	L	H	VALID BINARY INPUT				CH A ±12 dB RANGE, CH B ± 6 dB RANGE, BAND 1~14
H	X	H	L	VALID BINARY INPUT				CH A ± 6 dB RANGE, CH B ±12 dB RANGE, BAND 1~14
H	X	H	H	VALID BINARY INPUT				CH A ± 6 dB RANGE, CH B ± 6 dB RANGE, BAND 1~14

BAND CODE
CH B ±6 dB/12 dB RANGE
CH A ±6 dB/12 dB RANGE
DON'T CARE
DATA I

TL/H/8664–10

DATA II (BAND SELECTION)

	D7	D6	D5	D4	D3	D2	D1	D0
FLAT	L	X	L	L	L	L	L	L
1 dB BOOST	L	H	H	L	L	L	L	L
2 dB BOOST	L	H	L	H	L	L	L	L
3 dB BOOST	L	H	L	L	H	L	L	L
4 dB BOOST	L	H	L	L	L	H	L	L
5 dB BOOST	L	H	L	L	L	L	H	L
6 dB BOOST	L	H	L	H	L	L	H	L
7 dB BOOST	L	H	H	L	H	L	H	L
8 dB BOOST	L	H	L	H	L	H	H	L
9 dB BOOST	L	H	L	L	L	L	L	H
10 dB BOOST	L	H	H	L	H	L	L	H
11 dB BOOST	L	H	H	L	H	H	L	H
12 dB BOOST	L	H	H	L	H	H	H	H
1 dB~12 dB CUT	L	L	VALID ABOVE INPUT					

GAIN CODE
BOOST/CUT
DATA II

This is the gain if the ±12 dB range is selected by DATA I. If the ±6 dB range is selected, then the values shown must be approximately halved.

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FIGURE 12. Coding Information

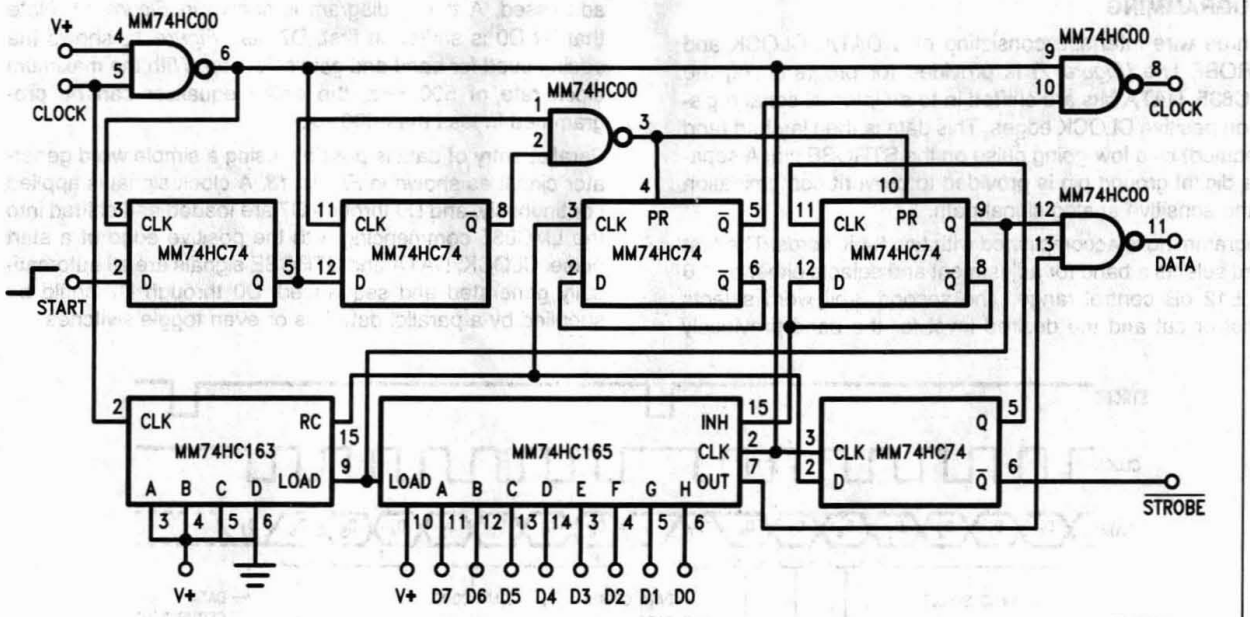

FIGURE 12. Test Word Generator

APPLICATIONS

Several distinct advantages are associated with computer controlled equalizers. Remote control is possible unlike conventional mechanically controlled equalizers. Since the LMC835 is programmed by a simple 3-wire interface, hard-wired control from a remote location is also possible. This is useful on stage or in the studio where the equalizer must be located near the source and the amplifiers and/or speakers, but the control point is behind the audience or in a control room. The 3-wire digital interface is easier to connect than attempting to route low-level analog signal lines over long distances between signal source and control point.

Microprocessor storage of various equalization settings is possible. Specific settings for different instruments, diverse program material, or perhaps multiple speaker or listening environments can be accessed as easily as recalling a pocket calculator memory. If a real time analyzer (RTA) is included in the equalizer, automatic equalization is possible. In this application pink noise is played through the amplifier/speaker system, and a calibrated microphone feeds the resultant spectrum back to the RTA. One band at a time, the controlling microprocessor adjusts the LMC835 equalizer for flat response. Two or three iterations are required since the adjustments are interactive.

By using analog circuit techniques, the LMC835 is able to achieve 0.0015% distortion, 114 dB signal to noise ratio and 20 dB headroom relative to a 1 Vrms input signal. This performance is suitable for use with conventional analog audio sources as well as digital audio formats.

A 150W IC Op Amp Simplifies Design of Power Circuits

National Semiconductor
Application Note 446

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Abstract: *A power op amp capable of driving ±35V at ±10A has been fabricated on a single silicon chip. Peak power ratings to 800W allow it to handle reactive loads. The IC incorporates internal management circuitry to insure smooth turn on and automatic protection from a variety of fault conditions; this includes instantaneous peak-temperature limiting within the power transistors. The op amp is described briefly, but emphasis is placed on the practical problems encountered in designing with power amplifiers. Numerous application examples are also given.*

introduction

Advances in IC technology have produced a power amplifier that is an order of magnitude more powerful than its predecessors. Unlike other IC's, its peak dissipation rating is many times higher than continuous, as is required for handling reactive loads. Protection circuitry is also more effective. The performance of the new IC, the LM12, puts it in the same class as discrete and hybrid amplifiers. However, it offers far more effective control of turn on, fault and overload conditions in addition to the economies of monolithic construction.

In the late 1960's, the availability of low cost IC op amps prompted their use in rather mundane applications, replacing a few discrete components. This power op amp now promises to extend this to high-power designs. Replacing single power transistors with an op amp may become cost-effective because of improved performance, simplification of attendant circuitry, vastly improved fault protection, greater reliability and the reduction in design time.

Some applications are given here to illustrate op amp design principles as they relate to power circuitry. Unusual design problems that have cropped up in using the LM12 in a wide variety of situations with all sorts of fault conditions are identified along with solutions.

the op amp

The performance of the LM12 is summarized in *Table I*. The input common-mode range extends to within a volt of the positive supply and to three volts above the negative supply. No input-polarity reversal is experienced should the input-voltage range be exceeded, and no damage results should the inputs be driven beyond the supplies.

The IC is compensated for unity-gain feedback, with a small-signal bandwidth of 700 kHz. Slew rate is 9V/μs, even as a follower. This translates to a 60 kHz power bandwidth under load with a ±35V output swing. The op amp is stable with or without capacitive loading; the maximum load capacitance depends upon loop gain. There are no spurious output stage oscillations, and a series-RC snubber is not required on the output.

The IC delivers ±10A output current at any output voltage yet is completely protected against output overloads, including shorts to the supplies. Dynamic safe-area protection is provided by peak-temperature limiting within the power transistor array. The turn-on characteristics are controlled by keeping the output open-circuited until the total supply voltage reaches 15V. The output is also opened should the case temperature exceed 150°C or as the supply voltage approaches the BV_{CEO} of the output transistors. The IC withstands overvoltages to 100V.

The LM12 is supplied in a steel TO-3 package with four through leads, plus case. A gold-eutectic die attach to a molybdenum interface is used to avoid thermal fatigue problems with power cycling. Two voltage grades are available; both are specified for either the military or industrial temperature range.

Table I. Some typical characteristics of the LM12 for V_S = ±40V and T_C = 25°C.

parameter	conditions	value
input offset voltage	V_{CM} = 0	2 mV
input bias current	V_{CM} = 0	150 nA
voltage gain	R_L = 4Ω	50V/mV
output voltage swing	I_{OUT} = ±1.5A	±38V
	±10A	±35V
peak output current	V_{OUT} = 0	±13A
continuous dc dissipation	T_C = 25°C	90W
	100°C	55W
pulse dissipation	t_{ON} = 10 ms	120W
	1 ms	240W
	0.2 ms	600W
power output	R_L = 4Ω	150W
total harmonic distortion	R_L = 4Ω	0.01%
bandwidth	A_V = 1	700 kHz
slew rate	R_L = 4Ω	9V/μs
supply current	I_{OUT} = 0	60 mA

general advice

Power op amps are subject to many of the same problems experienced with general-purpose op amps. Excessive input or feedback resistance can cause a dc offset voltage on the output because of bias-current drops, or it can combine with stray capacitances to cause oscillations. Improper supply bypassing and capacitive loading, alone or in combination, can also result in oscillations. Many hours spent tracking down incomprehensible design problems could have been saved by monitoring the op amp output with a wide-band oscilloscope.

With low impedance loads and current transients above 10A, the inductance and resistance of wire interconnects can become important in a number of ways. Further, an IC op amp rated to dissipate 90W continuously will not do so unless it is properly mounted to an adequate heat sink.

The management and protection circuitry of the LM12 can also affect operation. Should the total supply voltage exceed ratings or drop below 15V, the op amp shuts off completely. Case temperatures above 150°C also cause complete shut down until the temperature drops to 145°C. This may take several seconds, depending on the thermal system. Activation of dynamic safe-area protection causes both the main feedback loop to lose control and a reduction in output drive current, with possible oscillations. In ac applications, the dynamic protection will cause waveform distortion.

supply bypassing

All op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals to avoid spurious oscillation problems. Power op amps require larger bypass capacitors. The LM12 is stable with good-quality electrolytic bypass capacitors greater than 20 μF. Other considerations may require larger capacitors.

The current in the supply leads is a rectified component of the load current. If adequate bypassing is not provided, this distorted signal can be fed back into internal circuitry. Low distortion at high frequencies requires that the supplies be bypassed with 470 μF or more, at the package terminals.

lead inductance

With ordinary op amps, lead-inductance problems are usually restricted to supply bypassing. Power op amps are also sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load. Sensing to a remote load must be accompanied by a high-frequency feedback path directly from the output terminal. Lead inductance can also cause voltage surges on the supplies. With long leads to the power source, energy stored in the lead inductance when the output is shorted can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With 20 μF local bypass, these voltage surges are important only if the lead length exceeds a couple feet (>1 μH lead inductance). Twisting together the supply and ground leads minimizes the effect.

ground loops

With fast, high-current circuitry, all sorts of problems can arise from improper grounding. In general, difficulties can be avoided by returning all grounds separately to a common point. Sometimes this is impractical. When compromising, special attention should be paid to the ground returns for the supply bypasses, load and input signal. Ground planes also help to provide proper grounding.

Many problems unrelated to system performance can be traced to the grounding of line-operated test equipment used for system checkout. Hidden paths are particularly difficult to sort out when several pieces of test equipment are used but can be minimized by using current probes or the new isolated oscilloscope preamplifiers. Eliminating any direct ground connection between the signal generator and the oscilloscope synchronization input solves one common problem.

output clamp diodes

When a push-pull amplifier goes into power limit while driving an inductive load, the energy stored in the inductance can drive the output beyond the supplies. *Figure 1* shows the overload response of the LM12 driving ±36V at 40 Hz into a 4Ω load in series with 24 mH to illustrate the point.

The IC has internal supply-clamp diodes, but these clamps have a parasitic current that dissipates roughly half the clamp current across the total supply voltage. This dissipation cannot be controlled by the internal protection circuitry and will result in catastrophic failure if sustained. Therefore, the use of external diodes to clamp the output to the power supplies is strongly recommended.

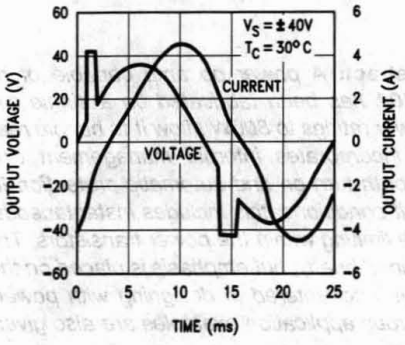

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Figure 1. Output voltage and current waveforms with dynamic safe-area protection activated on an inductive load. Stored energy in the inductor drives the output beyond the supplies.

Experience has demonstrated that hard-wire shorting the output to the supplies can induce random failures if these external clamp diodes are not used. Therefore, it is prudent to use output clamp diodes even when the load is not obviously inductive. Failure is particularly violent when operating from low-impedance supplies: the V^+ pin can vaporize, with a hole being blown through the top of the can. If there are failures, install diodes before proceeding.

Heat sinking of the clamp diodes is usually unimportant in that they only clamp current transients. Forward drop with 15A transients is of greater concern. The clamp to the negative supply can have somewhat reduced effectiveness should the forward drop exceed 0.8V. Mounting this diode to the op amp heat sink improves the situation. Although the need has not been demonstrated, including a third diode, D_3 in *Figure 2*, will eliminate any concern about the clamp diodes. This diode, however, must be capable of dissipating continuous power as determined by the negative supply current of the op amp.

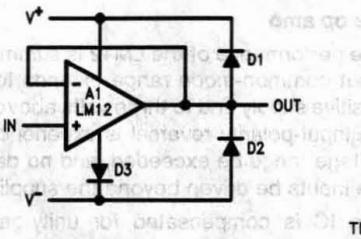

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Figure 2. Output clamp diodes, D_1 and D_2, dump inductive-load current into the supplies when op amp goes into power limit. A third diode, D_3, may be required if the forward drop of D_2 is excessive.

reactive loading

The LM12 is normally stable with resistive, inductive or smaller capacitive loads. Larger capacitive loads interact with the open-loop output resistance (about 1Ω) to reduce the phase margin of the feedback loop, ultimately causing oscillation. The critical capacitance depends upon the feedback applied around the amplifier; a unity-gain follower can handle about 0.01 μF, while more than 1 μF does not cause problems if the loop gain is ten. With loop gains greater than unity, a speedup capacitor across the feedback resistor will aid stability. In all cases, the op amp will behave predictably only if the supplies are properly bypassed, ground loops are controlled and high-frequency feedback is derived directly from the output terminal, as recommended earlier.

So-called capacitive loads are not always capacitive. A high-Q capacitor in combination with long leads can present a series-resonant load to the op amp. In practice, this is not usually a problem; but the situation should be kept in mind.

Large capacitive loads (including series-resonant) can be accommodated by isolating the feedback amplifier from the load as shown in *Figure 3*. The inductor gives low output impedance at lower frequencies while providing an isolating impedance at high frequencies. The resistor kills the Q of series resonant circuits formed by capacitive loads. A low inductance, carbon-composition resistor is recommended. Optimum values of L and R depend upon the feedback gain and expected nature of the load, but are not critical. A 4 μH inductor is obtained with 14 turns of number 18 wire, close spaced, around a one-inch-diameter form.

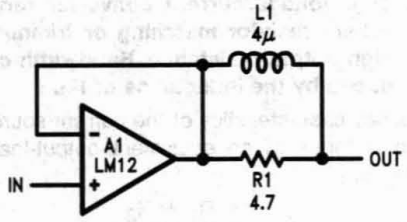

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Figure 3. Isolating capacitive loads with an inductor. The non-inductive resistor avoids resonance problems with load capacitance by dropping Q.

The LM12 can be made stable for all loads with a large capacitor on the output, as shown in *Figure 4*. This compensation gives the lowest possible closed-loop output impedance at high frequencies and the best load-transient response. It is appropriate for such applications as voltage regulators.

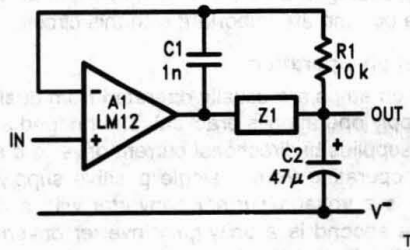

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Figure 4. Using a large output capacitor to stabilize for all capacitive loads. The impedance, Z_1, is the wire connecting the IC output to the load-capacitor terminal.

A feedback capacitor, C_1, is connected directly to the output pin of the IC. The output capacitor, C_2, is connected at the output terminal with relatively short leads. Single-point grounding to avoid dc and ac ground loops is advised.

The impedance, Z_1, is the wire connecting the op amp output to the load capacitor. About 3 inches of number-18 wire (70 nH) gives good stability and 18-inches (400 nH) begins to degrade load-transient response. The minimum load capacitance is 47 μF, if a plastic film or solid-tantalum capacitor with an equivalent series resistant (ESR) of 0.1Ω is used. Electrolytic capacitors work as well, although capacitance may have to be increased to 200 μF to bring ESR below 0.1Ω.

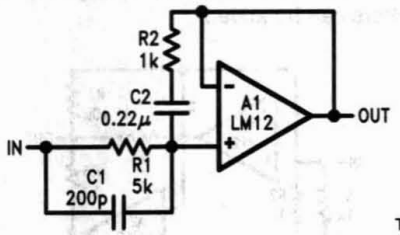
Loop stability is not the only concern when op amps are operated with reactive loads. With time-varying signals, power dissipation can also increase markedly. This is particularly true with the combination of capacitive loads and high-frequency excitation.

input compensation

The LM12 is prone to low-amplitude oscillation bursts coming out of saturation if the high-frequency loop gain is near unity. The voltage follower connection is most susceptible. This glitching can be eliminated at the expense of small-signal bandwidth using input compensation. Input compensation can also be used in combination with LR load isolation to improve capacitive load stability.

An example of a voltage follower with input compensation is shown in *Figure 5a*. The R_2C_2 combination across the input works with R_1 to reduce feedback at high frequencies without greatly affecting response below 100 kHz. A lead capacitor, C_1, improves phase margin at the unity-gain crossover frequency. Proper operation requires that the output impedance of the circuitry driving the follower be well under 1 kΩ at frequencies up to a few hundred kilohertz.

Extending input compensation to the integrator connection is shown in *Figure 5b*. Both the follower and this integrator will handle 1 μF capacitive loading without LR output isolation.



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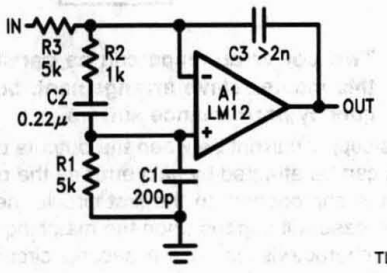
a) follower



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b) inverter

Figure 5. Using input compensation to reduce bandwidth and increase stability with capacitive loads a) for a voltage follower and b) for an integrating inverter.

parallel operation

Load current beyond the capability of one power amplifier can be obtained with parallel operation as shown in *Figure 6*. The power op amps, A_2 and A_3 are wired as followers and connected in parallel with the outputs coupled through equalization resistors, R_4 and R_5. More output buffers, with individual equalization resistors, may be added to meet even higher drive requirements. A standard, high-voltage op amp is used to provide voltage gain. Overall feedback compensates for the voltage dropped across the equalization resistors.

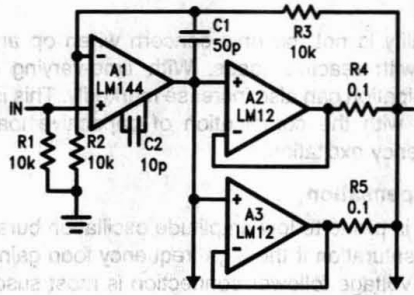

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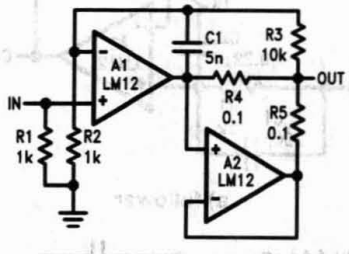
Figure 6. Paralleling the outputs of two op amps. The power amplifiers, A_2 and A_3, are wired as followers and connected in parallel with the outputs coupled through equalization resistors.

With parallel operation there will be an increase in unloaded supply current related to the offset voltage of A_2 and A_3 across the equalization resistors. In some cases, it may be desirable to use input compensation on the followers for increased stability. It is important that the source resistance introduced by input compensation not increase the offset voltage overmuch.

A method of paralleling op amps that does not require a separate control amplifier is shown in *Figure 7*. The output buffer, A_2, provides load current through R_5 equal to that supplied by the main amplifier, A_1, through R_4. Again, more output buffers can be added.



TL/H/8710–13

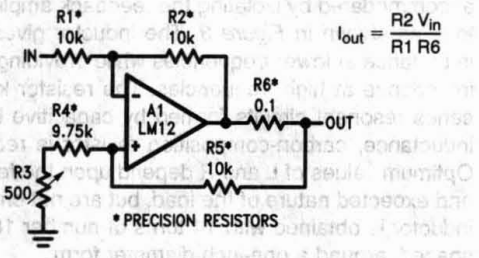
Figure 7. Two power op amps can be paralleled using this master/slave arrangement, but high frequency performance suffers.

The cross-supply current between the outputs of paralleled amplifiers can be affected by gain error as the power-bandwidth limit is approached. In the first circuit, the operating-current increase will depend upon the matching of the high-frequency characteristics. In the second circuit, however, the entire input error of A_2 appears across R_4 and R_5. The supply current increase can cause the power limiting to be activated as the slew limit is approached. This will not damage the LM12. It can be avoided in both cases by connecting A_1 as an inverting amplifier and restricting bandwidth with C_1.

current drive

The circuit in *Figure 8* provides an output current proportional to the input voltage. Current drive is sometimes preferred for servo motors because it aids in stabilizing servo loops by reducing phase lag caused by motor inductance. In applications requiring high output resistance, such as operational power supplies running in the current mode, matching of the feedback resistors to 0.01 percent or better is required. Alternately, an adjustable resistor, R_3, can be used for trimming. Offsetting R_3 from its optimum value will give decreasing positive or negative output resistances.

The current source input is actually differential. It can be driven as shown, or from the bottom of R_3 to obtain the opposite output sense. Both inputs should be connected to a low source impedance like ground or an op amp output. Otherwise, the source resistance will imbalance the feedback, changing output resistance. Alternately, an input can be driven by a known source resistance, like a voltage divider, if this resistance is made part of the feedback network.



TL/H/8710–11

Figure 8. This voltage/current converter requires excellent resistor matching or trimming to get high output resistance. Bandwidth can be reduced by the inductance of R_6.

The frequency characteristics of the current source can be expressed in terms of an equivalent output-load capacitance given by

$$C_{eq} = \frac{R_1 + R_2}{2\pi f_o R_1 R_6}, \quad (1)$$

where f_o is the extrapolated unity gain bandwidth of the op amp (in this case about 2 MHz for the LM12). The equation is only valid for $Z_L \gg R_6$.

This output capacitance can resonate with inductive loads such as motors, causing some peaking. Inductive loads can oscillate should the feedback network be imbalanced to give sufficient negative output resistance.

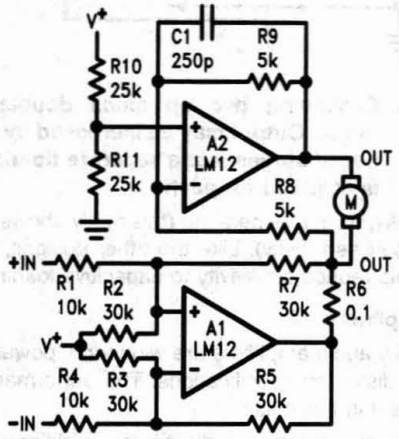
Inductance of the current sense resistor, R_6, can affect operation. With a 0.1Ω resistor, 3 μH series inductance will reduce the maximum obtainable bandwidth to 5 kHz. Proper supply bypassing and connecting R_2 directly to the output pin of the op amp are important with this circuit.

single-supply operation

Although op amps are usually operated from dual supplies, single-supply operation is practical. The bridged amplifier in *Figure 9* supplies bi-directional current drive to a servo motor while operating from a single positive supply. One op amp, A_1, is a voltage/current converter with a differential input. The second is a unity-gain inverter driven from the output of the first. It has its non-inverting input referred to half the supply voltages so that the two outputs swing symmetrically about this voltage.

Either input may be grounded, with bi-directional drive provided to the other. It is also possible to connect one input to a positive reference, with the signal to the other input varying about this voltage. If this reference voltage is above 5V, R_2 and R_3 are not required.

The output is easily converted to voltage drive by shorting R_6 and connecting R_7 to the output of A_2, rather than A_1. Although not shown, clamp diodes to V^+ and ground on the output of both amplifiers are recommended for motor loads.



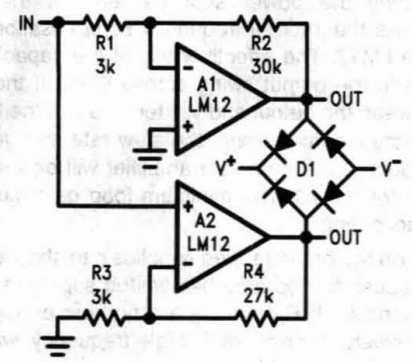
TL/H/8710–14

Figure 9. The output current of this bridged amplifier is proportional to differential input voltage. Although not shown, output clamp diodes are recommended with a motor load.

high voltage amplifiers

Using two amplifiers in a bridge connection also doubles the voltage swing delivered to the load. The configuration in *Figure 10* gives good results with split supplies. One op amp is an inverting amplifier while the other is a non-inverting amplifier with equal gain. A load connected between the outputs sees twice the swing of either amplifier. Understandably, the output slew rate doubles while the full-power bandwidth stays the same.

The current limit of two op amps cannot be expected to be the same. Therefore, a short between the outputs of a bridge amplifier can result in one amplifier saturating while the output transistor of the second handles the overload at the full supply voltage. Not all power amplifiers can take this kind of treatment; the LM12 will.



TL/H/8710–15

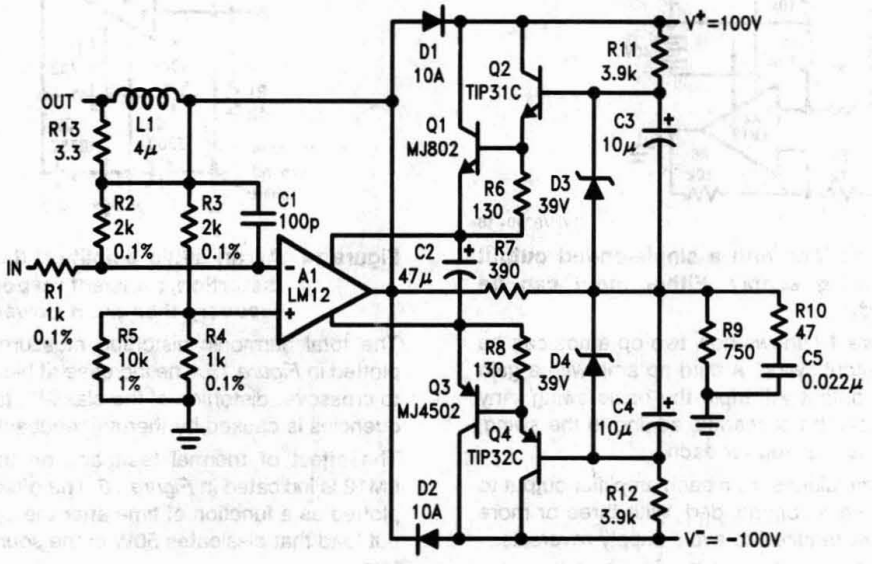
Figure 10. Bridge connection gives differential output approaching twice the total supply voltage. Diode bridge clamps outputs to supplies.

Figure 10 shows how a bridge-rectifier module can be used to provide output clamping for both outputs.

The LM12 can be operated in cascode with external transistors to get output swings several times higher than the basic op amp. The design in *Figure 11* drives ±90V at ±10A. Significantly, the IC provides current and power limiting for the external transistors.

The transistors and zener diodes form a simple voltage regulator that is driven at 70 percent of the output swing from the R_7/R_9 divider. Thus, the total supply voltage of the IC stays constant while the voltage to ground swings some ±60V.

The supply terminals of the LM12 swing both above and below ground at full output. Therefore, the input terminals must be bootstrapped to the output to keep them within the common-mode range. The R_1–R_4 bridge does this. The bridge is unbalanced by R_5 to set the gain near 30. Naturally, R_4 and R_5 can be combined.



TL/H/8710–18

Figure 11. This amplifier can drive ±90V at ±10A, more than twice the output swing of the LM12. The IC provides current and power limiting for the discrete transistors.

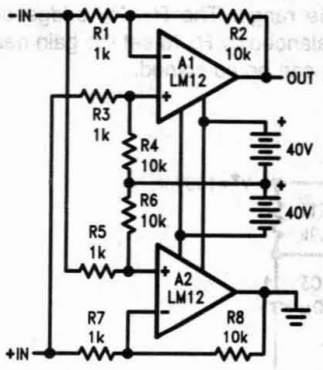
Bootstrapping the power supplies reduces the voltage swing across the internal frequency compensation capacitors of the LM12. The effectiveness of the capacitors is in proportion to the output swing across them. If the voltage swing between the output and V^- terminals of the IC is one-third the actual output swing, the slew rate and gain-bandwidth product of the complete amplifier will be three times that listed for the IC. The minimum loop gain must be increased accordingly.

Distortion on the bootstrapped supplies can show up on the output because the op amp has limited supply rejection at high frequencies. If R_6 and R_8 are not low enough, these power followers cannot track high frequency waveforms and performance will suffer.

This circuit is more sensitive to capacitive loading than the basic op amp because the supply terminals of the IC cannot be bypassed directly to ground. The effects of this can be mitigated by using an appropriate LR network in the output.

When the IC goes into power limit, current will likewise be cut back in the external transistors. The voltage on these external transistors is not necessarily regulated, so the discrete transistors must be enough stronger than the IC transistors to handle the extra voltage. The IC can handle orders of magnitude more power cycling than commercial power transistors with soft-solder die attach. Cycling in and out of power limit at low frequencies could be a problem and should not be ignored.

The output swing can be increased using more-conventional circuitry if floating supplies are available. *Figure 12* shows a bridged amplifier that drives a ground-referred load. A differential input is provided, but one input can be grounded and the other driven from a low-impedance source. If the non-inverting input is grounded, R_7 and R_8 can be replaced by a single resistor. Operation is like a standard bridge, except that it is a bit more sensitive to capacitive loading. Output swing is ±70V at ±10A.



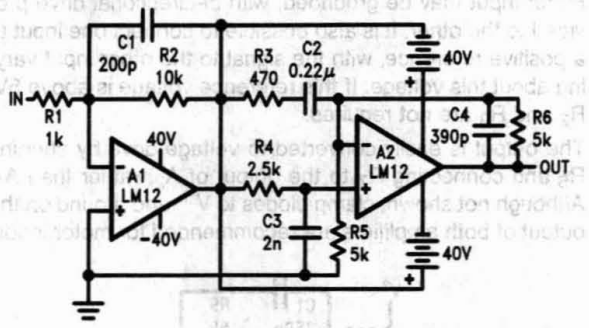
TL/H/8710–16

Figure 12. Bridge amplifier with a single-ended output uses floating supply. Either input can be grounded.

A final circuit in *Figure 13* shows how two op amps can be stacked to double output swing. A third op amp with a gain of 0.5 added to the output will triple the basic swing. Any number of op amps can be cascaded, adding to the swing, but a floating supply is required for each.

With two stages, clamp diodes from each amplifier output to its supply terminals are recommended. With three or more stages, the diodes are required to avoid supply reversals.

The bandwidth is limited by R_4 and C_3. This isolation also prevents load transients on the output, reflected back to the



TL/H/8710–17

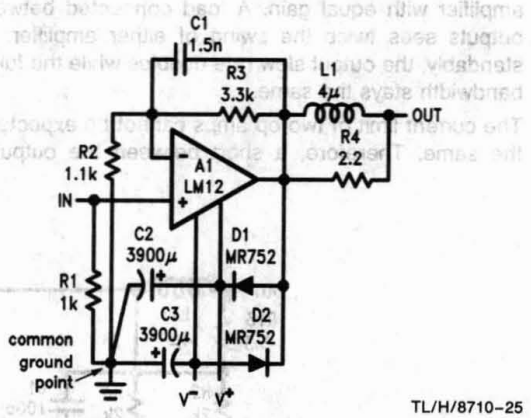
Figure 13. Cascading two op amps doubles output swing. Output may be increased by any number of stages, but a separate floating supply is required for each.

output of A_1, from regenerating (this really shows up as capacitive load sensitivity). Like the other designs, an output LR will help reduce sensitivity to capacitive loading.

audio amplifiers

High quality audio amplifiers are wideband, power op amps with tight distortion specifications. The performance of the LM12 puts it in this class.

A practical design for an audio power amplifier is shown in *Figure 14*. Output-clamp diodes are mandatory because loudspeakers are inductive loads. Output LR isolation is also used because audio amplifiers are usually expected to handle up to 2 μF load capacitance. Large, supply-bypass capacitors located close to the IC are used so that the rectified load current in the supply leads does not get back into the amplifier, increasing high-frequency distortion. Single-point grounding for all internal leads plus the signal source and load is recommended to avoid ground loops that can increase distortion.

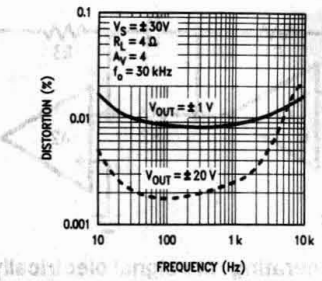


TL/H/8710–25

Figure 14. As an audio amplifier, the LM12 has better distortion, transient response and saturation recovery than most power op amps.

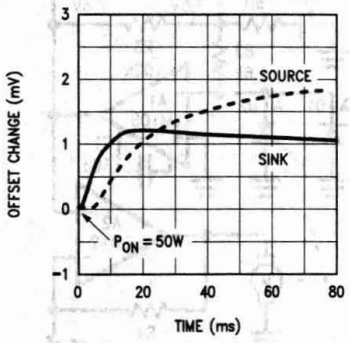
The total harmonic distortion measured for this circuit is plotted in *Figure 15*. The increase at high frequencies is due to crossover distortion of the class-B stage. That at low frequencies is caused by thermal feedback within the LM12.

The effect of thermal feedback on the response of the LM12 is indicated in *Figure 16*. The offset voltage change is plotted as a function of time after the application of an output load that dissipates 50W in the source and sink transistors.



TL/H/8710–30

Figure 15. Total harmonic distortion of the circuit in *Figure 14* is plotted here for both low- and high-level outputs.



TL/H/8710–31

Figure 16. The offset voltage change after the application of a load that dissipates 50W in each output transistor is plotted here. This thermal feedback causes increased distortion below 100 Hz.

Unlike crossover distortion, the low-frequency distortion can be virtually eliminated by using the LM12 as a buffer inside the feedback loop of a low-level op amp. However, the low-frequency harmonic distortion, being generated thermally, is slow and does not cause the more objectionable intermodulation distortion. The latter measured 0.015 percent with ±10V into a 4Ω load under the standard 60 Hz/7 kHz, 4:1 test conditions.

The transient response of the circuit in *Figure 14* is clean; and saturation characteristics are glitch-free even at high frequencies. In addition, the 9V/μs slew rate of the LM12 virtually eliminates transient intermodulation distortion.

The availability of a low-cost power amplifier that is suitable as a high-quality audio amplifier can be expected to generate interest in using a separate amplifier to drive each speaker. Not only does this eliminate high-level crossover networks and attenuators, but also it prevents overloading at low frequencies from causing intermodulation distortion at high frequencies. With separate amplifiers, such clipping is far less noticeable.

servo amplifiers

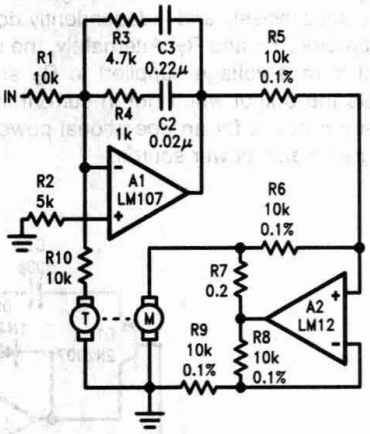
When making servo systems with a good power op amp, there is a temptation to use it for frequency shaping to stabilize the servo loop. Sometimes this works; other times there are better ways; and occasionally it just doesn't fly. Usually it's a matter of how quickly and to what accuracy the servo must stabilize. A couple of examples should make the point.

With fast motor-driven servos, it is best to make the motor current proportional to the servo amplifier drive. With current drive, motor response is basically unaffected by the series inductance of the motor windings. At higher frequencies, current drive can give 90 degrees less phase shift in the motor transfer function when compared to voltage drive. Should the servo loop go through unity gain at a frequency at which motor inductance is unimportant, the advantage of current drive is lost.

The motor/tachometer speed control shown in *Figure 17* gives an example of optimizing performance using a current drive that is supplied by A_2, connected as a voltage/current converter. The tachometer, on the same shaft as the dc motor, is simply a generator. It gives a dc output voltage proportional to the speed of the motor. A summing amplifier, A_1, controls its output so that the tachometer voltage equals the input voltage, but of opposite sign.

With current drive to the motor, phase lag to the tachometer is 90 degrees, before second order effects come in. Compensation on A_1 is designed to give less than 90 degrees phase shift over the range of frequencies where the servo loop goes through unity gain. Should response time be of less concern, a power op amp could be substituted for A_1 to drive the motor directly. Lowering break frequencies of the compensation would, of course, be necessary.

The circuit in *Figure 17* could also be used as a position servo. All that is needed is a voltage indicating the sense and magnitude of the motor shaft displacement from a desired position. This error signal is connected to the input, and the servo works to make it zero. The tachometer is still required to develop a phase-correcting rate signal because the error signal lags the motor drive by 180 degrees.



TL/H/8710–20

Figure 17. Motor/tachometer servo gives an output speed proportional to input voltage. Using current drive to motor reduces loop phase shift due to motor inductance.

The concept of a rate signal can be understood from a simple example. The problem is to rotate a radar antenna to acquire a target from a large angle off point. When the motor has limited power and the antenna has mass, the quickest path into point is to run full bore toward point; pick the correct instant to reverse at full power before getting there; and shut down in just the right place. In a servo, the rate signal added to the error signal is what tells it when to reverse in order to acquire the target without overshooting.

With a fixed target, a tachometer on the drive motor will give the rate signal. If the target is moving across the antenna, it does not: it produces the rate signal plus or minus the angular velocity of the target. This disrupts acquisition and generates a pointing error.

The rate signal can be obtained by differentiating the error signal. A design that gives the required error plus rate signal at the output is shown in *Figure 18a*. Neither op amp should saturate under any condition, no matter how far off point or how fast the error changes. If it saturates, a proper rate signal is not developed; and acquisition will be degraded. This can degenerate to where the servo will oscillate continuously once a certain tracking error is exceeded.

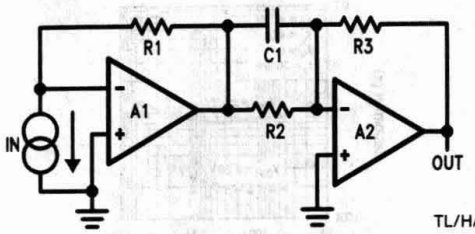
Acquiring from large errors quickly and to great accuracy requires an extremely wide dynamic range. In *Figure 18a*, it is necessary to make R_1 and R_3 so low to keep the amplifiers from saturating that chopper stabilization may be required to preserve accuracy.

In *Figure 18a*, R_3 can be raised to any value if back-to-back zeners are put across it. The waveform below the clamp level will be unchanged from the case where A_2 has unbounded output swing. Should the clamp levels be large enough to saturate the motor drive, operation is unimpaired.

This principle is developed further in *Figure 18b*. It gives identical response, except that the resistor in series with C_1 breaks back the differentiator above the unity gain frequency. Off point, the voltage at the junction of R_1 and R_2 should not get so large that the output of A_1 cannot saturate A_2 without the clamps conducting.

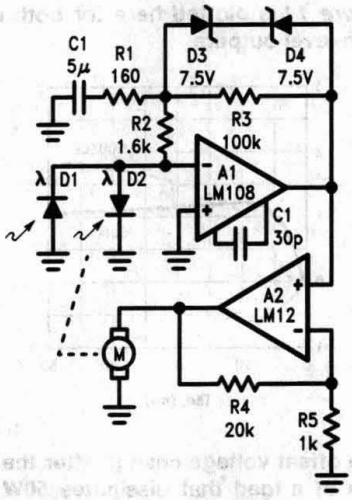
operational power supply

External current limit can be provided for an op amp as shown in *Figure 19*. The positive and negative limiting currents can be set precisely and independently down to zero with potentiometers R_3 and R_7. Alternately, the limit can be programmed from a voltage supplied to R_2 and R_6. The input controls the output when not in current limit. This is just the set-up required for an operational power supply or voltage-programmable power source.



TL/H/8710–32

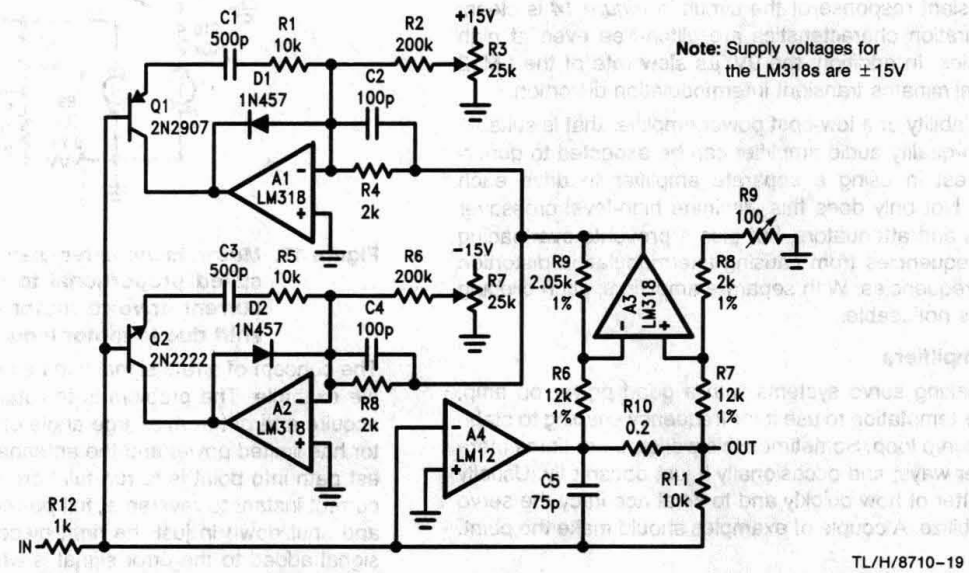
a) generating rate signal electrically



TL/H/8710–21

b) compressing dynamic range

Figure 18. When electrical rate signals must be developed with large error signals well beyond saturation of motor drive, a linear approach a) requires wide dynamic range and great precision. More practical design b) uses feedback clamps to increase effective dynamic range.



TL/H/8710–19

Figure 19. Bi-directional limiting currents of the power op amp, A_4, are set independently by R_3 and R_7. Fast response is ensured by clamp diodes, D_1 and D_2.

The power op amp, A_4, is connected as an inverting amplifier. Its output current is sensed across R_{10}. This sense voltage is level shifted to ground by A_3, a differential amplifier that is made insensitive to the op amp output level by trimming R_9.

With current below preset levels, the outputs of A_1 and A_2 are clamped by D_1 and D_2 with Q_1 and Q_2 turned off. When the current threshold is reached, the relevant amplifier will come out of clamp, saturate the transistor on its output and take over control of the summing node. The clamp diodes limit the swing on the outputs of the current-control amplifiers while the transistors disconnect frequency compensation until the summing node is engaged. This ensures fast activation of current limit. Recovery back to voltage mode is also fast. The LM318 wideband amplifier is required for A_1 through A_3.

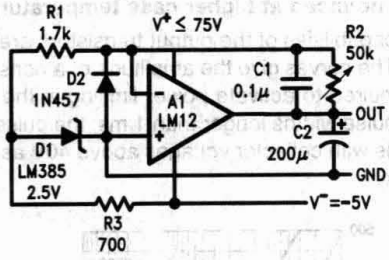
voltage regulators

An op amp can be used as a positive or negative regulator with equal ease. Unlike most dedicated voltage regulators, the output can both source or sink current to absorb energy dumped back into the supply and prevent overvoltage with certain fault conditions. Output transient response is also improved, especially overshoots.

A particular reason for using the LM12 as a regulator is its exceptional high-voltage capability. This not only gives output voltages to 70V, but also ensures startup under worst-case full-load conditions.

Compared to conventional IC regulators, using an op amp with an external reference has better accuracy: an optimum reference can be selected and thermally isolated from the power circuitry. Better regulation, temperature drift and long term stability result. Remote, output-voltage sensing at the load to further reduce errors is also practical.

A positive regulator with a 0–70V output range is shown in *Figure 20*. The op amp has one input at ground and a reference current drawn from its summing junction. With this arrangement, output voltage is proportional to the setting resistor, R_2.



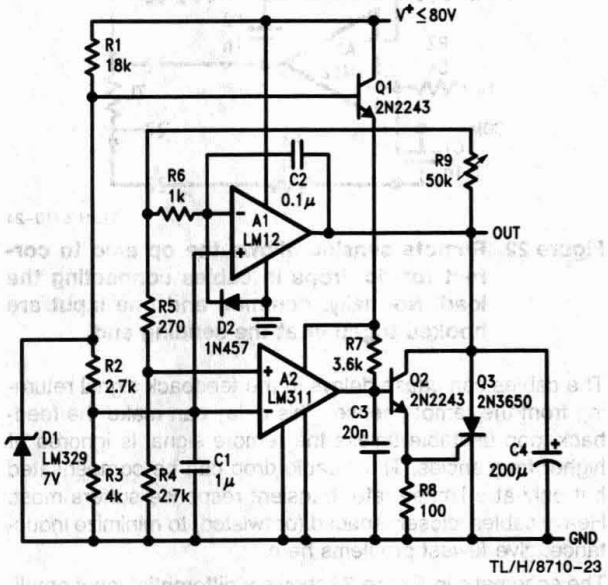
TL/H/8710–22

Figure 20. Positive regulator with 0–70V output range. Output will source or sink current, and start-up capability with higher input voltages is superior to standard IC regulators.

A negative supply is used to operate the op amp within its common-mode range, provide zero output with sink current and power a low-voltage bandgap reference, D_1. Current drawn from this supply is under 150 mA, except when sinking load current.

The output load capacitor, C_2, is part of the op amp frequency compensation. This requires that C_1 be connected directly at the op amp output and C_2 at the load, as described earlier. The reference noise is filtered by C_1, which also controls the start-up rate. The clamp diode, D_2, resets C_1 when the output is shorted and keeps the op amp input from being driven below V^-.

Dual supplies are not required to use an op amp for a regulator, as can be seen from the 4V to 70V adjustable regulator shown in *Figure 21*. This regulator also has overvoltage protection. Should an overvoltage condition exceed the current or power capabilities of the LM12, a comparator will trigger a SCR, crowbarring the output.



TL/H/8710–23

Figure 21. This 4V to 70V regulator operates from a single supply. Should the op amp not be able to control an overvoltage condition, the SCR will crowbar the output.

The reference is a low drift zener, D_1, powered from V^+ through R_1. The reference voltage is dropped to 4V and fed to the non-inverting input of the op amp, A_1, with zener noise attenuated by C_1. Thus, the output will be this 4V plus a voltage that is proportional to the resistance of R_9. As before, D_2 is a clamp while C_2 makes sure the IC input is ac coupled directly to its output terminal.

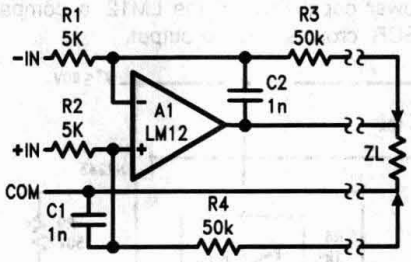
With overvoltage, a comparator, A_2, fires the SCR through a buffer, Q_2, after about a 20 μs delay from C_3 to eliminate spurious transients. The comparator receives its power from Q_1 so that V^+ can be increased above the rating of the LM311.

Should the feedback terminal of the op amp rise more than 0.4V above the regulating value for longer than 20 μs, the comparator will provide the signal required to fire the SCR. Since this can only happen if the considerable current and energy capabilities of the LM12 are exhausted, nuisance tripping is unlikely. The output trip threshold will be 0.4V above nominal as long as it happens quickly enough that the voltage across C_2 does not change appreciably. For a slow overvoltage condition, it is 10 percent above nominal.

remote sensing

With the current running at 10A, a foot of 0.1-inch-diameter copper drops 10 mV. Obviously, sizeable voltage drops will have to be accepted to run this kind of current over any distance without expensive and cumbersome cables.

Remote sensing, illustrated in *Figure 22*, can help the situation considerably. It uses a pair of small wires, in addition to the main power cables, to sense the voltage at the load. A feedback amplifier can then correct for the drop in the main cables.



TL/H/8710–24

Figure 22. Remote sensing allows the op amp to correct for dc drops in cables connecting the load. Normally, common and one input are hooked together at the sending end.

The cables can cause delays in the feedback signal returning from the remote sense. This delay can make the feedback loop unstable unless the remote signal is ignored at higher frequencies. Thus, cable drop can be compensated but only at a limited rate; transient response suffers most. Heavy cables, closely spaced (or twisted) to minimize inductance, give fewest problems here.

The schematic in *Figure 22* shows a differential-input amplifier that has dc feedback from the remotely-sensed load. The ac feedback is directly from the op amp output and the signal common at the sending end. There is no feedback from the load at high frequencies. The optimum capacitance depends upon the cable delay.

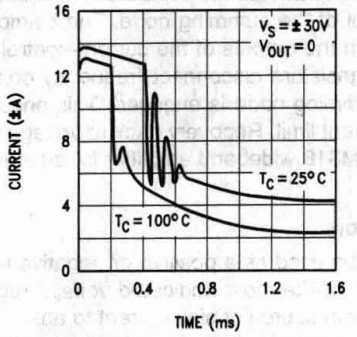
For single-ended input, the unused input terminal in the schematic would be strapped to the common. Feedback resistors should be reasonably matched to avoid second-order errors and the feedback resistors should be made enough greater than the sense line resistance to avoid gain errors.

Sometimes provision is made to control the circuit should the sense lines be disconnected. With a regulator, an imbalance current could be put into the sense lines to bring the regulator output to zero should one line go open. With bi-directional op amps, it is not obvious whether limiting the error with back-to-back diodes between the power-out and sense-in is better than having it go open loop.

power capabilities

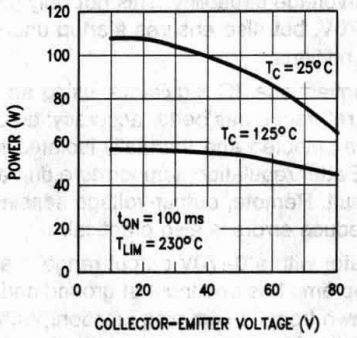
The output transistors of the LM12 will dissipate power until their peak junction temperature reaches 230°C (±15°C). When this temperature is reached, internal limiting circuitry takes over to regulate peak temperature. How this works is illustrated in *Figure 23*, which gives the peak output current waveform with the output instantaneously shorted to ground. Conventional current limiting holds the short-circuit current near 13A for a few hundred microseconds, then temperature limiting takes over as junction temperature tries to rise above 230°C. The response time of the temperature limiter is well under 100 μs.

With this type of protection, the power capabilities will depend on case temperature, transistor operating voltages and how the dissipation varies with time. *Figure 24* shows the amplitude of a power pulse required to activate power limiting in 100 ms as a function of collector-emitter voltage on the output transistors for two case temperatures. The continuous dissipation limit is about 15 percent less than the 100 ms limit.



TL/H/8710–33

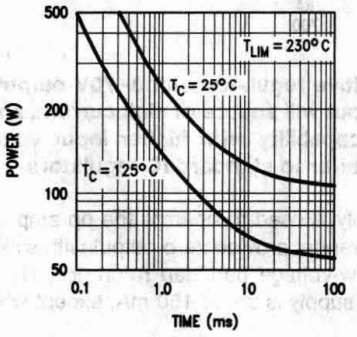
Figure 23. Output short-circuit current is reduced when power transistor junction temperature reaches 230°C and power limit takes over.



TL/H/8710–34

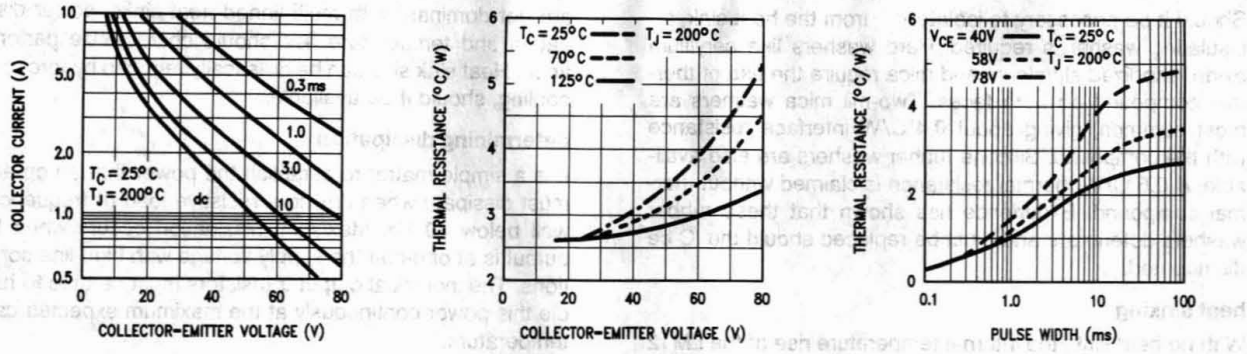
Figure 24. The power required to activate power limit is less at higher voltage, but this is not so pronounced at higher case temperatures.

The pulse capabilities of the output transistors are shown in *Figure 25*. The curves give the amplitude of a constant-power pulse required to activate power limiting in the indicated time. With pulse widths longer than 1 ms, the pulse capability decreases with collector voltages above 40V as indicated in *Figure 24*.



TL/H/8710–35

Figure 25. The peak-dissipation capabilities of the power transistor are shown here. For times greater then 100 ms, the external heat sink will determine ratings.



TL/H/8710–37

a) safe area curve **b) dc thermal resistance** **c) pulse thermal resistance**

Figure 26. The worst-case power ratings of the output transistors are described by a) a safe area curve, b) the change in dc thermal resistance with temperature and operating voltage and c) the pulse thermal resistance.

power ratings

The guaranteed power ratings of the LM12 are based on a peak junction temperature of 200°C rather than the 230°C limiting temperature. Test accuracy, guard bands and unit-to-unit variations are also taken into account. The result is that the guaranteed ratings are about 40 percent less than the power required to activate thermal limit.

The worst-case, safe-area curves for a peak junction temperature of 200°C with a 25°C case temperature are shown in *Figure 26a*. The guaranteed-maximum, dc thermal resistance is given as a function of collector-emitter voltage in *Figure 26b*. It can be seen from this figure that the increase in thermal resistance with voltage is much less at higher case temperatures. Finally, the equivalent thermal resistance for power pulses is given in *Figure 26c*. Again, these are worst-case numbers. The voltage dependency of thermal resistance in *Figure 26c* is for a 25°C case temperature. At higher case temperatures this dependency will be moderated as shown in *Figure 26b*.

The guaranteed power ratings are not established by statistical methods from sample tests. Instead, they are interpolated from actual measurements of power capability into thermal limit: these are standard production tests.

With ac loading, both power transistors share the dissipation; and the worst-case thermal resistance can drop to 1.9°C/W. However, it is necessary that the frequency be sufficiently high that the peak ratings of neither output transistor are exceeded.

thermal derating

It is not unusual to derate the maximum junction temperature of semiconductors below the manufacturer's specified value in worst-case design. The derating is often dictated by unpredictable operating conditions and design uncertainties. An equipment manufacturer does not want his product failing because of some obscure stress that is not apparent to the customer.

Company policies, equipment requirements and individual preferences vary as to what constitutes appropriate derating. When pressure is on for the best performance at lowest cost, a 200°C junction temperature for power semiconductors has been accepted, although this might well be influenced by whether hermetic or plastic packaging is used. Continuous operation at 200°C should also be treated differently than infrequent excursions to this temperature. Nonetheless, reducing temperature is a recognized method for increasing reliability; and ultra-reliable military and space applications have required that maximum junction temperatures be under 125°C.

The protection circuitry of the LM12 brings a new dimension to derating. Such conditions as out-of-spec line voltage or lack of air circulation cause the equipment to stop working temporarily; excessive stress or catastrophic failure does not result. It should be recognized, however, that there are certain applications where a temporary misfunction can be the same as a permanent one, definitely recommending derating.

Derating also reflects the user's faith in the ability of the manufacturer to adequately test the parts. Dynamic safe-area protection helps out here. Should a die-attach void or other defect produce hot spots in the power transistor, it will be rejected during production testing as having reduced dissipation capability, rather than being passed on as a reliability risk. This cannot be done with conventional power semiconductors.

No short-term failure mode has been found with modern IC power transistors even with peak junction temperatures of 300°C. However, power cycling can cause problems. Die-attach failures at 3×10^4 cycles with a 70°C temperature rise are possible with power transistors having a soft-solder die attach. The LM12 avoids this by using a gold-eutectic die attach to a molybdenum spacer. Even so, metalization failures have been experienced with the LM12 at 10^6 cycles from 50°C to power limit at 230°C with 200W dissipation.

Thermal derating is more applicable to the control circuitry of the LM12. Operating the control circuitry above 150°C can be expected to affect reliability. Fortunately, the control circuitry is exposed to only a fraction of the temperature rise in the power transistor. Derating may be based on a thermal resistance of 0.9°C/W independent of operating voltage. With ac loading, where power is being dissipated in both power transistors, this thermal resistance drops, finally approaching 0.6°C/W.

package mounting

The ratings of the LM12 are based on the case temperature as measured on the bottom of the TO-3 package near the center. Proper mounting is required to minimize the thermal resistance between this region and the heat sink.

A good thermal compound such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package directly to the heat sink. Without this compound, thermal resistance will be no better than 0.5°C/W, and possibly much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005-inch combined flatness run-out for the package and the heat sink. Proper torquing of the mounting bolts is important. Four to six inch-pounds is recommended.

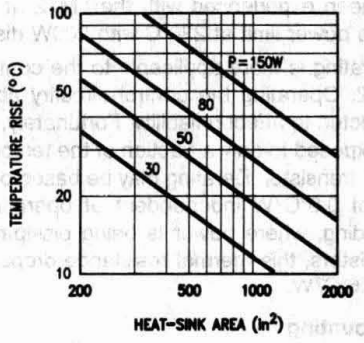
Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like beryllium oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound. Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

heat sinking

With no heat sink, the internal temperature rise of the LM12 can be as high as 160°C with ±40V supplies and no load. A heat sink is required. Heat sinks are commercially available, with data on their power rating and temperature rise supplied by the manufacturer. The types most suitable for dissipation in the order of 50W are made from extruded aluminum channel equipped with multiple fins. It is important that the heat sink have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

The power rating of a multi-finned heat sink is determined largely by the surface area subject to convection cooling and the allowable temperature rise above ambient. Heat loss due to radiation can also be important with simple heat sinks. However, with multiple fins radiating toward each other, the significance of the radiation term drops. Nonetheless, heat sinks are usually black anodized to maximize radiation losses.

The surface area required for a given temperature rise and power dissipation can be estimated with fair accuracy from *Figure 27*. The area efficiency is affected by heat sink orientation, length and fin spacing. The figure assumes that the surfaces are located in a vertical plane. With the surfaces horizontal, temperature rise is increased by perhaps 20 percent. Vertical dimensions longer than 4 inches are less efficient. Commercial heat sinks are normally designed so that fin spacing is not so close as to affect the results of the figure.



TL/H/8710–28

Figure 27. A heat sink is required to cool the IC package. This curve gives the rise in case temperature as a function of heat-sink fin area with convection cooling.

It is not possible to specify an unqualified thermal resistance for a convection or radiation cooled heat sink. Both mechanisms will give a lower thermal resistance with increasing temperature rise, while heat losses to radiation also increase with absolute temperature. Since radiation losses are not dominant with multi-finned heat sinks, power dissipation and temperature rise should characterize performance. Heat sink size can be drastically reduced by forced air cooling, should it be available.

determining dissipation

It is a simple matter to establish the power that an op amp must dissipate when driving a resistive load at frequencies well below 10 Hz. Maximum dissipation occurs when the output is at one-half the supply voltage with high-line conditions. The individual output transistors must be able to handle this power continuously at the maximum expected case temperature.

If there is ripple on the supply bus, it is valid to use the average value in worst-case calculations as long as the peak rating of the power transistor is not exceeded at the ripple peak. With 120 Hz ripple, the peak rating is 1.5 times the continuous power rating.

Dissipation requirements are not so easily established with time-varying output signals, especially with reactive loads. Both peak- and continuous-dissipation ratings must be taken into account, and these depend on the signal waveform as well as load characteristics.

With a sine wave output, analysis is fairly straightforward. With supply voltages of $\pm V_S$, the maximum average power dissipation of both output transistors is

$$P_{MAX} = \frac{2V_S^2}{\pi^2 Z_L \cos\theta}, \quad \theta < 40°; \tag{2}$$

and

$$P_{MAX} = \frac{V_S^2}{2Z_L}\left[\frac{4}{\pi} - \cos\theta\right], \quad \theta \geq 40°, \tag{3}$$

where Z_L is the magnitude of the load impedance and θ its phase angle. Maximum average dissipation occurs for a peak output swing, E_P, given by

$$E_P = \frac{2V_S}{\pi \cos\theta}, \quad \cos\theta > \frac{2V_S}{\pi V_P}; \tag{4}$$

or

$$E_P = V_P, \quad \cos\theta \leq \frac{2V_S}{\pi V_P}; \tag{5}$$

where V_P is the maximum available output swing.

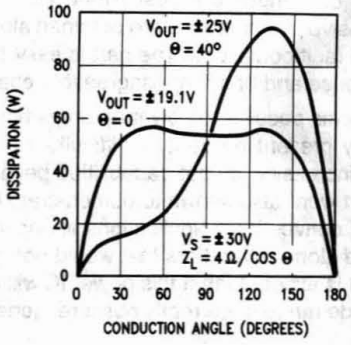
The instantaneous power dissipation is

$$P = \frac{E_P}{Z_L}\cos\omega t\,[V_S - E_P \cos(\omega t + \theta)]. \tag{6}$$

For $E_P = V_S$, the power peak occurs for $\omega t = \frac{1}{3}(\pi - \theta)$.

With practical amplifiers $E_P < V_S$, and a numerical solution is required.

The instantaneous power dissipation over the conducting half cycle of one output transistor is shown in *Figure 28*. Power dissipation is near zero on the other half cycle. The output level is that resulting in maximum peak and average dissipation. Plots are given for a resistive and a series R-L load. The latter is representative of a 4Ω loudspeaker operating below resonance and would be the worst-case condition in most audio applications. The peak dissipation of each transistor is about four times average. In ac applications, power capability is often limited by the peak ratings of the power transistor.



TL/H/8710–26

Figure 28. Instantaneous power dissipation of one output transistor over its conducting half cycle with a resistive and an inductive load.

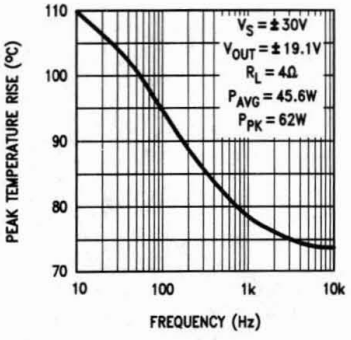
The pulse thermal resistance of the LM12 is specified for constant power-pulse duration. Establishing an exact equivalency between constant-power pulses and those encountered in practice is not easy. However, for sine waves, reasonable estimates can be made at any frequency by assuming a constant power pulse amplitude given by:

$$P_{PK} \cong \frac{V_S^2}{2Z_L} [1 - \cos(\phi - \theta)], \qquad (7)$$

where $\phi = 60°$ and θ is the absolute value of the phase angle of Z_L. Equivalent pulse width is $t_{ON} \cong 0.4\tau$ for $\theta = 0$ and $t_{ON} \cong 0.2\tau$ for $\theta > 20°$, where τ is the period of the output waveform.

With the LM12, the peak junction-temperature rise for any given waveform can actually be measured. This is done by raising case temperature until power limiting is activated. Temperature rise is then computed from the measured case temperature based on a power-limit temperature of 230°C. Alternately, the power-limit temperature may be determined directly by measuring the dc dissipation at a collector-emitter voltage of 20V required to activate power limit. If this is done over a range of case temperatures, the results can be plotted and extrapolated to the power-limit temperature.

This procedure was used to give the peak temperature rise as a function of frequency for an op amp driving a resistive load under conditions of worst-case dissipation. The results are plotted in *Figure 29*.



TL/H/8710–36

Figure 29. Peak junction-temperature rise as a function of frequency with an op amp driving a resistive load under conditions of worst-case dissipation.

dissipation driving motors

A motor with a locked rotor looks like an inductance in series with a resistance, for purposes of determining driver dissipation. With slow-response servos, the maximum signal amplitude at frequencies where motor inductance is significant can be so small that motor inductance does not have to be taken into account. If this is the case, the motor can be treated as a simple, resistive load as long as the rotor speed is low enough that the back emf is small by comparison to the supply voltage of the driver transistor.

A permanent-magnet motor can build up a back emf that is equal to the output swing of the op amp driving it. Reversing this motor from full speed requires the output drive transistor to operate, initially, along a loadline based upon the motor resistance and total supply voltage. Worst case, this loadline will have to be within the continuous dissipation rating of the drive transistor; but system dynamics may permit taking advantage of the higher pulse ratings. Motor inductance can cause added stress if system response is fast.

Shunt-and series-wound motors can generate back emfs that are considerably more than the total supply voltage, resulting in even higher peak dissipation than a permanent-magnet motor having the same locked-rotor resistance.

voltage regulator dissipation

The pass transistor dissipation of a voltage regulator is easily determined in the operating mode. Maximum continuous dissipation occurs with high line voltage and maximum load current. As discussed earlier, ripple voltage can be averaged if peak ratings are not exceeded; however, a higher average voltage will be required to ensure that the pass transistor does not saturate at the ripple minimum.

Conditions during start-up can be more complex. If the input voltage increases slowly such that the regulator does not go into current limit charging output capacitance, there are no problems. If not, load capacitance and load characteristics must be taken into account. This is also the case if automatic restart is required in recovering from overloads.

Automatic restart or start-up with fast-rising input voltages cannot be guaranteed unless the continuous dissipation rating of the pass transistor is adequate to supply the load current continuously at all voltages below the regulated output voltage. In this regard, the LM12 performs much better than IC regulators using foldback current limit, especially with high-line input voltages above 20V.

power supplies

Power op amps do not require regulated supplies. However, the worst-case output power is determined by the low-line supply voltage in the ripple trough. The worst-case power dissipation is established by the average supply voltage with high-line conditions. The loss in power output that can be guaranteed is the square of the ratio of these two voltages.

Relatively simple off-line switching power supplies can provide voltage conversion, line isolation and 5-percent regulation while reducing size and weight. The regulation against ripple and line variations may provide a substantial increase in the power output that can be guaranteed under worst-case conditions. In addition, switching power supplies can convert low-voltage power sources such as automotive batteries up to regulated, dual, high-voltage supplies optimized for powering power op amps.

checking thermal design

Thermal design margins can be established by determining how far the part can be pushed beyond nominal worst-case before power limiting is activated. This extra stress can be applied by increasing case temperature, supply voltage or output loading.

Raising case temperature with worst-case electrical conditions has the advantage of giving results that are easily interpreted in terms of thermal design margins. If the case temperature, as measured at the center of the package bottom, must be raised 50°C above the maximum design value to activate power limiting, the worst-case, peak-junction temperature is 180°C, or 50°C below the power-limit temperature.

With this technique, it is important that the case temperature be kept below 140°C. At 150°C, the case-temperature limit activates, shutting the IC down completely.

conclusions

A new concept for power limiting and advances in IC design have been combined to produce a monolithic, high-power op amp that challenges the best hybrid and discrete designs. Impressive power ratings are obtained along with better control of fault conditions. The part is easy to use, quite tolerant of abuse and has few disagreeable characteristics.

Design problems peculiar to power op amps have been discussed. They present no serious difficulty if kept in mind. Methods of increasing output capabilities beyond those of the basic part were also shown to demonstrate its flexibility. A number of conventional applications for power op amps were detailed along with others that would not normally use an op amp. It is expected that this power IC will recommend itself for a wide range of currently obscure, general-purpose applications.

One of the more onerous tasks with power devices is establishing that a design operates components within ratings. Guidelines were given for determining continuous and transient dissipation. In addition, the basic problems of providing adequate heat sinking were outlined. Dynamic safe-area protection is of particular help here in that design margins can actually be measured, rather than inferred from published data.

Protection Schemes for BI-FET™ Amplifiers and Switches

National Semiconductor
Application Note 447
Wanda Garrett

To use integrated circuits in real applications, designers must know the limitations of the devices. The majority of the limitations are published in the datasheets, and these fall into two categories: Absolute Maximums—which, if violated, can cause damage or destruction of the device; and Electrical Characteristics—which indicate the performance limitations. Unfortunately, these specifications don't explain the consequences of a violation, nor what may happen between the violation of an Electrical Characteristic limit and an Abs. Max. limit. This information is needed so the designer can design an appropriate protection scheme.

This article will focus on National Semiconductor Corp. BI-FET op amps: how to improve their reliability and performance. In most cases, the results are similar for bipolar op amps also.

THE BI-FET FAMILIES

Our BI-FET op amps are divided into families: LF411, LF441 and LF356. The LF411 family consists of LF411, LF351, and TL081 (all singles); LF412, LF353, and TL082 (duals); and LF347 (quad). This is a good general purpose set of op amps that all have the same internal design, differing only by grade.

The LF441 family consists of the LF441 (single), LF442 (dual), and LF444 (quad). This family gives nearly the same DC performance as the LF411's for 1/12th the supply current. However, because they are low-power devices, they are also proportionally slower than the 411's.

The LF356 family includes the LF355, LF356, and LF357 (in the commercial temperature range). The 355 is the low-I_{CC} part, and the 357 is the wide-bandwidth part. All of the family have good DC specs and can drive a lot of capacitance (to .01 μF, typically). They are also among our faster op amps, having slew rates which vary from 5V/μs (for the 355) to 50V/μs (for the 357).

The operating restrictions for these families are nearly all the same, as are the methods of protection. In some cases (as will be pointed out) certain families are better at surviving the abuses than others.

EXCEEDING COMMON-MODE INPUT VOLTAGE RANGE

The input common-mode range of any operational amplifier is the range of voltages on the input terminals for which the amplifier operates correctly. To understand what happens when the common-mode range is exceeded, four cases must be considered: open- and closed-loop operation at both the positive and negative common-mode limits.

Exceeding Negative Common-Mode Limit

In open-loop operation (i.e., no feedback from output to inverting input, or, during any time that the op amp is slew-rate limited), taking the non-inverting input below the inverting input causes the output to slew toward the negative supply rail. If the voltage at the non-inverting input is more negative than the negative common-mode limit, the input stage ceases to function properly and the output swings to its positive limit. This apparent "phase-reversal" is temporary; bringing the non-inverting input back within the legal input common-mode range restores the part's normal operation.

If the inverting input is taken below the non-inverting input while the op amp is operated open-loop, the output slews toward the positive rail. Exceeding the negative common-mode limit in this condition does not cause a "phase reversal", as the output will still head toward, or remain at, the positive rail.

In closed-loop operation, exceeding the negative common-mode at either input limit, also causes the output to swing to the positive supply rail.

Exceeding Positive Common-Mode Limit

In general, the positive common-mode limit is at or beyond the positive supply. Taking either input above the positive common-mode limit while in open-loop operation does not cause a "phase reversal" at the output; the output will slew toward whichever rail one might expect. However, if both inputs are driven above the positive common-mode limit, the output will slew to the positive rail. In addition, while operating in a closed-loop mode, taking either input above the positive common-mode limit will also drive the output to the positive rail.

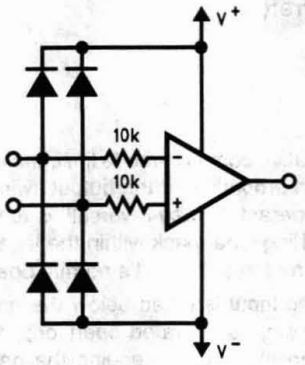
INPUTS EXCEEDING SUPPLY RAILS

If either input is pulled above V+, nothing happens until the difference between the input and V+ gets near the breakdown voltage, typically 50V. At this point, the FET's gate-source junction avalanches and will draw all the current it can. Limiting this input current to something less than 3 mA helps prevent damage. The best protection (in addition to limiting the input current) is a diode clamp from each input to V+. If transients are expected, use a fast-recovery diode, such as a IN4148. For low-leakage (but less speed), the C-B junction of a good transistor (i.e. 2N3904) is recommended.

Failure to clamp the voltage or limit the current adequately may not destroy the part, but the offset voltage and bias current will be permanently degraded.

If either input is pulled more than a few tenths of a Volt below V− (even if this pin is floating), a lightly-doped parasitic substrate transistor turns on. This transistor's collector current cannot be controlled externally, so allowing it to turn on can cause metal migration and destruction of the input stage (or at least a major unbalancing). In the newer LF411 and LF441 families, this transistor has been controlled by the addition of a diode from base to emitter which kills the gain of the transistor and keeps its current low. Any input current should still be limited to 1 mA or less. However, the older parts and members of the LF356 family are still

susceptible, so it is best to protect all the BI-FETs from this potential abuse by using the clamp diodes (see *Figure 1* below).



TL/H/8744–1

FIGURE 1. Clamping Inputs of Op Amp

Since this parasitic transistor turns on easily, the best way to keep it turned off is to use a Schottky diode, its on-voltage being less than that required to turn on the transistor. For lower leakage, a short-base switching diode (such as the Fairchild FD200 series) may be used. Its forward drop will be larger at low currents, but will stay constant for a wide current range, as opposed to the relatively leaky Schottky diodes.

POWER SUPPLY SEQUENCING

Adding the clamp diodes shown in *Figure 1* not only protects the inputs from transients when the circuit is operating, but protects them as power is being applied to the circuit. Because the parasitic transistor appears when the input voltage is less than the negative supply, applying the positive supply or input voltage before the negative supply is applied can cause this problem. For this reason, it is always recommended that the negative supply be turned on **first**, if the supplies can be turned on independently. This is especially important for protection of the BI-FET switches.

Also, even if the input stage is well protected with clamp diodes and current limiting, the inputs should not be allowed to be heavily unbalanced (for example, one input at ground and the other at the rail) for extended periods of time (for example, many hours). The long-term effects of an unbalanced differential pair are increased offset voltage and offset current.

SUPPLY VOLTAGES OUT OF RECOMMENDED RANGE

Attempting to run a BI-FET on supply voltages less than the recommended total of 10V will narrow the common-mode input and output ranges, and slow the part down. In the LF411 family, at supply voltages less than 7V, an internal biasing zener turns off and the entire part quits working. With the LF441 family, a supply voltage of less than 6V is not enough to support the internal current source biasing, so eventually these also turn off. And the LF356 family needs all of the 10V to stay in operation.

Running the BI-FETs on supply voltages greater than the Abs. Max limit generally does no harm until the parasitic diode from V+ to the substrate breaks down (in LV_{ceo}) or the input gate-source junction breaks down (BV_{gso}). Limiting the supply current to something less than 10 mA improves the chances of the op amp's survival. These breakdowns typically occur at about 50V, but the devices are only tested up to 36V or 40V, depending on the device. In addition, power dissipation must be considered when the supply voltage is large.

OPERATING TEMPERATURE OUT OF ABSMAX RANGE

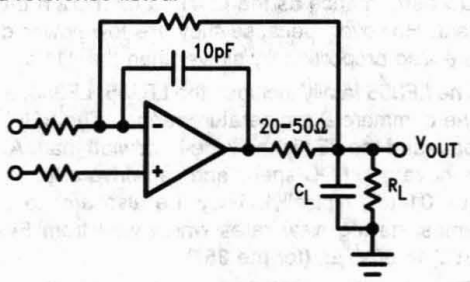
BI-FETs generally operate well when the ambient temperature is cold. The bias current becomes minimal, the input noise often decreases, and the bandwidth increases. However, if the device is in a marginally stable design, it may oscillate as its phase margin will also decrease.

Conversely, running the BI-FETs at temperatures greater than 100°C brings the bias current into the nanoamp range, and drops the gain-bandwidth product by 20% or more (compared to 25°C performance). Most op amps quit working between 180°C and 250°C due to excessive leakage currents or internal thermal shutdown mechanisms, and the BI-FETs are no exception. The maximum guaranteed junction (die) temperature of our ICs is 150°C, and some lower-grade parts and those in plastic DIP packages are guaranteed to as low as 100°C.

The type of package used affects the maximum ambient temperature allowed, since the junction temperature must remain in the "legal" range and the different packages have different heat-sinking properties. The metal can packages have the lowest thermal resistance, and have the additional advantage that heat-sink fins are easy to find and attach to the package (when needed).

DRIVING CAPACITANCE

Both the LF411 and LF441 families have a lot of trouble driving more than about 200 pF without oscillating. Standard techniques to get around this problem are to add a small resistor (about 50Ω) in series with the output (see *Figure 2*) or to use one of the LF356 family (the 356 itself being the most popular for this purpose). An explanation of why the 356 output stage is so unusually strong is provided in the second reference listed.



TL/H/8744–2

FIGURE 2. Isolating a Capacitive Load

When extra output filtering is desired, a series RC damper will often be more effective than just a large filter capacitor.

POWER SUPPLY BYPASSING

Another potential cause of oscillation is inadequate power supply bypassing.

In addition to the familiar problem of noise added through the supply inputs (due to poor high-frequency rejection), the inductance of the power supply leads degrades the effectiveness of the op amp's internal compensation, which invites oscillation.

The BI-FETs need the supply bypassing most on their V− terminals, as do many of the bipolar-input amplifiers. Good bypassing techniques include (1) putting the bypass capacitors right next to the IC, and (2) using an appropriate type and size of capacitor. Ceramic types are often used because of their small size and low cost, but their effective-

ness is limited to about 1 MHz. Typical values used are between 0.01 μF and 0.47 μF.

Tantalum capacitors are often used for high-frequency bypassing. However, their lead inductance can sometimes aggravate the situation instead of correcting it. Adding a small (0.01 μF) ceramic disc capacitor in parallel with the tantalum improves the overall performance. Typical values used for tantalum bypass capacitors range from 2.2 μF to 10 μF.

Mylar capacitors are also used for bypassing, but the monolithic ceramics have better high frequency performance and cost less.

Where the supply voltages have poor load regulation, electrolytic capacitors (typically 10 μF to 47 μF) can provide additional filtering.

DEALING WITH THE OFFSET VOLTAGE

If the offset voltage of a BI-FET op amp is first measured in a test circuit, and then again after the device is installed in the final circuit, a change in V_{OS} will often be detected. This is due to a difference in stress put on the die when the device (packaged or not) is installed in the two circuits. Because the input JFETs are largely surface devices, any stress on them changes their characteristics noticeably. This, then, changes the V_{OS} of the input stage. This problem is more apparent with the larger devices and packages, i.e. when there is more surface to be stressed. Thus, the most sensitive would be a large quad in a 14-pin DIP; the least, a small single op amp in a metal can (TO-5) package.

To improve the accuracy of the BI-FET op amps, the offset voltage should be nulled after the devices are in their final circuits. The BI-FET offset voltage has an associated drift of between 2 μV/°C and 10 μV/°C (depending on the device) for every millivolt of offset at room temperature. The V_{OS} null schemes will affect the offset drift; it is equally likely that the drift will increase rather than decrease, because the sources of BI-FET V_{OS} are complex.

The easiest V_{OS} cancelling technique is the trim scheme provided in the op amp's datasheet. The LF411 and LF441 require a 10k potentiometer between the trim pins (1 and 5), with the wiper to V−. The LF356 family requires a 25k pot with the wiper to V+. A larger pot would extend the trim range, but this is not necessary since the specified resistance is sufficient to correct even the worst case V_{OS}.

Dual and quad op amps have no trim pins, so they are used most often when small offsets can be tolerated. An external bias voltage can be added at the input to cancel the V_{OS} at a given ambient temperature (T_A). Typical trim schemes are given in Applications Note AN-3.

In general, the reasons for the Abs. Max. ratings and recommendations are a combination of convention and necessity. Exceeding the ratings and recommendations does not always mean death of the op amp, but the reliability and performance of the amplifier are kept at their highest when the part is used properly and protected from excesses.

References:

Brokaw, Paul: "An IC Amplifier Users' Guide to Decoupling & Grounding or Making Things Go Right", Electronic Products, December 1977, pp. 45–53.

Frederiksen, Thomas M: "Intuitive IC Op Amps", R. R. Donnelley & Sons, 1984, p. 40: explanation of LF356 output stage; pp. 271–272: power supply sequencing.

Pease, Robert A: "Bounding, Clamping Techniques Improve Circuit Performance", EDN, November 10, 1983, pp. 277–289.

LM34/LM35 Precision Monolithic Temperature Sensors

National Semiconductor
Application Note 460

INTRODUCTION

Most commonly-used electrical temperature sensors are difficult to apply. For example, thermocouples have low output levels and require cold junction compensation. Thermistors are nonlinear. In addition, the outputs of these sensors are not linearly proportional to any temperature scale. Early monolithic sensors, such as the LM3911, LM134 and LM135, overcame many of these difficulties, but their outputs are related to the Kelvin temperature scale rather than the more popular Celsius and Fahrenheit scales. Fortunately, in 1983 two I.C.'s, the LM34 Precision Fahrenheit Temperature Sensor and the LM35 Precision Celsius Temperature Sensor, were introduced. This application note will discuss the LM34, but with the proper scaling factors can easily be adapted to the LM35.

The LM34 has an output of 10 mV/°F with a typical nonlinearity of only ±0.35°F over a −50 to +300°F temperature range, and is accurate to within ±0.4°F typically at room temperature (77°F). The LM34's low output impedance and linear output characteristic make interfacing with readout or control circuitry easy. An inherent strength of the LM34 over other currently available temperature sensors is that it is not as susceptible to large errors in its output from low level leakage currents. For instance, many monolithic temperature sensors have an output of only 1 μA/°K. This leads to a 1°K error for only 1 μ-Ampere of leakage current. On the other hand, the LM34 may be operated as a current mode device providing 20 μA/°F of output current. The same 1 μA of leakage current will cause an error in the LM34's output of only 0.05°F (or 0.03°K after scaling).

Low cost and high accuracy are maintained by performing trimming and calibration procedures at the wafer level. The device may be operated with either single or dual supplies. With less than 70 μA of current drain, the LM34 has very little self-heating (less than 0.2°F in still air), and comes in a TO-46 metal can package, a SO-8 small outline package and a TO-92 plastic package.

FORERUNNERS TO THE LM34

The making of a temperature sensor depends upon exploiting a property of some material which is a changing function of temperature. Preferably this function will be a linear function for the temperature range of interest. The base-emitter voltage (V_{BE}) of a silicon NPN transistor has such a temperature dependence over small ranges of temperature.

Unfortunately, the value of V_{BE} varies over a production range and thus the room temperature calibration error is not specified nor guaranteeable in production. Additionally, the temperature coefficient of about −2 mV/°C also has a tolerance and spread in production. Furthermore, while the tempo may appear linear over a narrow temperature, there is a definite nonlinearity as large as 3°C or 4°C over a full −55°C to +150°C temperature range.

Another approach has been developed where the difference in the base-emitter voltage of two transistors operated at different current densities is used as a measure of temperature. It can be shown that when two transistors, Q1 and Q2, are operated at different emitter current densities, the difference in their base-emitter voltages, ΔV_{BE}, is

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln \frac{(J_{E1})}{J_{E2}} \quad (1)$$

where k is Boltzman's constant, q is the charge on an electron, T is absolute temperature in degrees Kelvin and J_{E1} and J_{E2} are the emitter current densities of Q1 and Q2 respectively. A circuit realizing this function is shown in *Figure 1*.

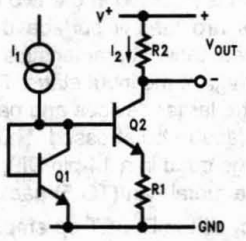


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FIGURE 1

Equation 1 implies that as long as the ratio of I_{E1} to I_{E2} is held constant, then ΔV_{BE} is a linear function of temperature (this is not exactly true over the whole temperature range, but a correction circuit for the nonlinearity of V_{BE1} and V_{BE2} will be discussed later). The linearity of this ΔV_{BE} with temperature is good enough that most of today's monolithic temperature sensors are based upon this principle.

An early monolithic temperature sensor using the above principle is shown in *Figure 2*. This sensor outputs a voltage which is related to the absolute temperature scale by a factor of 10 mV per degree Kelvin and is known as the LM135. The circuit has a ΔV_{BE} of approximately

$$(0.2\ mV/°K) \times (T)$$

developed across resistor R. The amplifier acts as a servo to enforce this condition. The ΔV_{BE} appearing across resistor R is then multiplied by the resistor string consisting of R

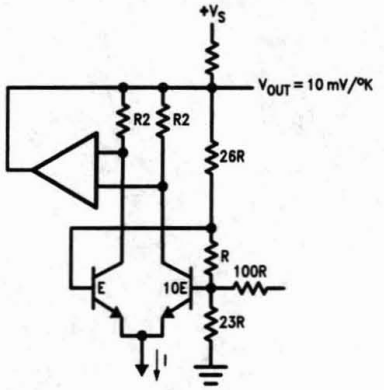

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FIGURE 2

and the 26R and 23R resistors for an output voltage of (10 mV/°K) × (T). The resistor marked 100R is used for offset trimming. This circuit has been very popular, but such Kelvin temperature sensors have the disadvantage of a large constant output voltage of 2.73V which must be subtracted for use as a Celsius-scaled temperature sensor.

Various sensors have been developed with outputs which are proportional to the Celsius temperature scale, but are rather expensive and difficult to calibrate due to the large number of calibration steps which have to be performed. Gerard C.M. Meijer[4] has developed a circuit which claims to be inherently calibrated if properly trimmed at any one temperature. The basic structure of Meijer's circuit is shown in *Figure 3*. The output current has a temperature coefficient of 1 μA/°C. The circuit works as follows: a current which is proportional to absolute temperature, I_{PTAT}, is generated by a current source. Then a current which is proportional to the V_{BE} drop of transistor Q4 is subtracted from I_{PTAT} to get the output current, I_O. Transistor Q4 is biased by means of a PNP current mirror and transistor Q3, which is used as a feedback amplifier. In Meijer's paper it is claimed that the calibration procedure is straightforward and can be performed at any temperature by trimming resistor R4 to adjust the sensitivity, dI_O/dT, and then trimming a resistor in the PTAT current source to give the correct value of output current for the temperature at which the calibration is being performed.

Meijer's Celsius temperature sensor has problems due to its small output signal (i.e., the output may have errors caused by leakage currents). Another problem is the trim scheme requires the trimming of two resistors to a very high degree of accuracy. To overcome these problems the circuits of *Figure 4* (an LM34 Fahrenheit temperature sensor) and *Figure 5* (an LM35 Celsius temperature sensor) have been developed to have a simpler calibration procedure, an output voltage with a relatively large tempco, and a curvature compensation circuit to account for the non-linear characteristics of V_{BE} versus temperature. Basically, what happens is transistors Q1 and Q2 develop a ΔV_{BE} across resistor R1. This voltage is multiplied across resistor nR1. Thus at the non-inverting input of amplifier A2 is a voltage two diode drops below the voltage across resistor nR1. This voltage is then amplified by amplifier A2 to give an output proportional to whichever temperature scale is desired by a factor of 10 mV per degree.

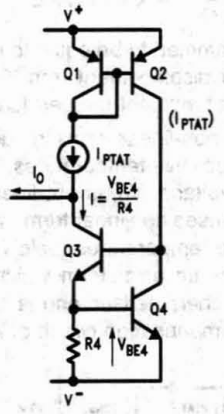

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FIGURE 3

CIRCUIT OPERATION

Since the two circuits are very similar, only the LM34 Fahrenheit temperature sensor will be discussed in greater detail. The circuit operates as follows:

Transistor Q1 has 10 times the emitter area of transistor Q2, and therefore, one-tenth the current density. From *Figure 4*, it is seen that the difference in the current densities of Q1 and Q2 will develop a voltage which is proportional to absolute temperature across resistor R_1. At 77°F this voltage will be 60 mV. As in the Kelvin temperature sensor, an amplifier, A1, is used to insure that this is the case by servoing the base of transistor Q1 to a voltage level, V_{PTAT}, of $\Delta V_{BE} \times n$. The value of n will be trimmed during calibration of the device to give the correct output for any temperature.

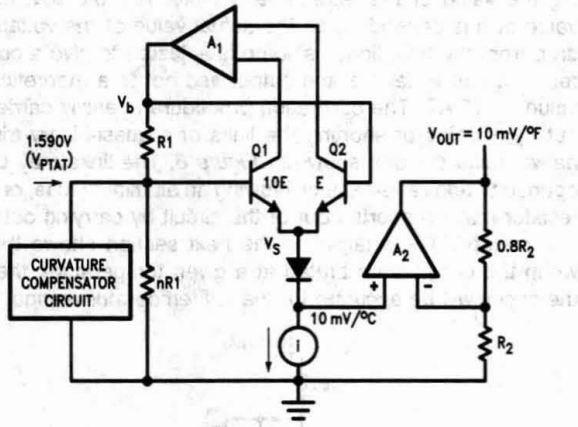

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FIGURE 4

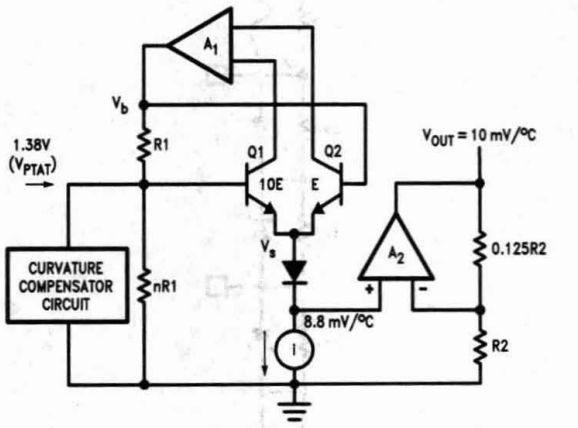

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FIGURE 5

For purposes of discussion, suppose that a value of V_{PTAT} equal to 1.59V will give a correct output of 770 mV at 77°F. Then n will be equal to $V_{PTAT}/\Delta V_{BE}$ or 1.59V/60 mV = 26.5, and V_{PTAT} will have a temperature coefficient (tempco) of:

$$\frac{nk}{q} \ln \frac{I_1}{I_2} = 5.3 \text{ mV/°C}.$$

Subtracting two diode drops of 581 mV (at 77°F) with tempcos of −2.35 mV/°C each, will result in a voltage of 428 mV with a tempco of 10 mV/°C at the non-inverting input of amplifier A2. As shown, amplifier A2 has a gain of 1.8 which provides the necessary conversion to 770 mV at 77°F (25°C). A further example would be if the temperature were 32°F (0°C), then the voltage at the input of A2 would be 428 mV−(10 mV/°C) (25°C) = 0.178, which would give V_{OUT} = (0.178) (1.8) = 320 mV—the correct value for this temperature.

EASY CALIBRATION PROCEDURE

The circuit may be calibrated at any temperature by adjusting the value of the resistor ratio factor n. Note that the value of n is dependent on the actual value of the voltage drop from the two diodes since n is adjusted to give a correct value of voltage at the output and not to a theoretical value for PTAT. The calibration procedure is easily carried out by opening or shorting the links of a quasi-binary trim network like the one shown in *Figure 6*. The links may be opened to add resistance by blowing an aluminum fuse, or a resistor may be shorted out of the circuit by carrying out a "zener-zap". The analysis in the next section shows that when the circuit is calibrated at a given temperature, then the circuit will be accurate for the full temperature range.

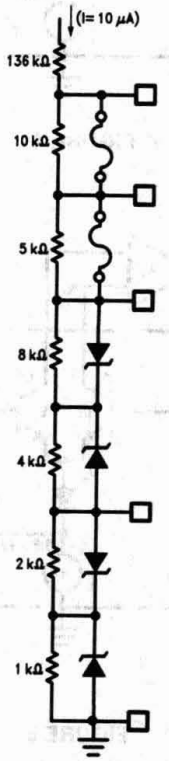

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FIGURE 6

How The Calibration Procedure Works

Widlar[5] has shown that a good approximation for the base-emitter voltage of a transistor is:

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{beo}\left(\frac{T}{T_0}\right) + \frac{nkT}{q} \ln\left(\frac{T_0}{T}\right) + \frac{kT}{q} \ln \frac{I_C}{I_{co}} \quad (1)$$

where T is the temperature in °Kelvin, T_0 is a reference temperature, V_{GO} is the bandgap of silicon, typically 1.22V, and V_{beo} is the transistor's base-emitter voltage at the reference temperature, T_0. The above equation can be re-written as

$$V_{BE} = (\text{sum of linear temp terms}) + (\text{sum of non-linear temp terms}) \quad (2)$$

where the first two terms of equation 1 are linear and the last two terms are non-linear. The non-linear terms were shown by Widlar to be relatively small and thus will be considered later.

Let us define a base voltage, V_b, which is a linear function of temperature as: $V_b = C_1 \bullet T$. This voltage may be represented by the circuit in *Figure 1*. The emitter voltage is $V_e = V_b - V_{be}$ which becomes:

$$V_e = C_1 T - V_{G0}\left(1 - \frac{T}{T_0}\right) - V_{beo}\left(\frac{T}{T_0}\right).$$

If V_e is defined as being equal to C_2 at $T = T_0$, then the above equation may be solved for C_1. Doing so gives:

$$C_1 = \frac{V_{beo} + C_2}{T_0} \quad (3)$$

Using this value for C_1 in the equation for V_e gives:

$$V_e = C_2 \frac{T}{T_0} + V_{G0}\left(\frac{T - T_0}{T_0}\right) \quad (4)$$

If V_e is differentiated with respect to temperature, T, equation 4 becomes $dV_e/dT = (C_2 + V_{G0})/T_0$.

This equation shows that if V_b is adjusted at T_0 to give $V_e = C_2$, then the rate of change of V_e with respect to temperature will be a constant, independent of the value of V_b, the transistor's beta or V_{be}.

To proceed, consider the case where $V_e = C_2 = 0$ at $T_0 = 0$°C. Then $\frac{dV_e}{dT} = \frac{V_{G0}}{273.7} = 4.47$ mV/°C.

Therefore, if V_e is trimmed to be equal to (4.47 mV) T (in °C) for each degree of displacement from 0°C, then the trimming can be done at ambient temperatures.

In practice, the two non-linear terms in equation 1 are found to be quadratic for positive temperatures. Tsividis[6] showed that the bandgap voltage, V_0, is not linear with respect to temperature and causes nonlinear terms which become significant for negative temperatures (below 0°C). The sum of these errors causes an error term which has an approximately square-law characteristic and is thus compensated by the curvature compensation circuit of *Figure 7*.

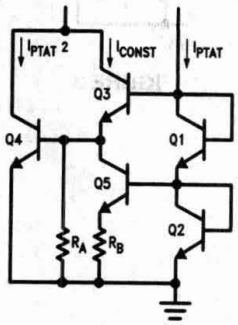

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FIGURE 7

A UNIQUE COMPENSATION CIRCUIT

As mentioned earlier, the base-emitter voltage, V_{BE}, is not a linear function with respect to temperature. In practice, the nonlinearity of this function may be approximated as having a square-law characteristic. Therefore, the inherent non-linearity of the transistor and diode may be corrected by introducing a current with a square-law characteristic into the indicated node of *Figure 4*. Here's how the circuit of *Figure 7* works: transistors Q1 and Q2 are used to establish currents in the other three transistors. The current through Q1 and Q2 is linearly proportional to absolute temperature, I_{PTAT}, as is the current through transistor Q5 and resistor R_B. The current through resistor R_A is a decreasing function of temperature since it is proportional to the V_{BE} of transistor Q4. The emitter current of Q3 is equal to the sum of the current through Q5 and the current through R_A, and thus Q3's collector current is a constant with respect to temperature. The current through transistor Q4, I_{C4}, will be used to compensate for the V_{BE} nonlinearities and is found with the use of the following equation:

$$I_{C4} = I_S \left(e^{\frac{qV_{BE4}}{KT}} - 1 \right) \cong I_S\, e^{\frac{qV_{BE4}}{KT}}$$

where $V_{BE4} = V_{BE1} + V_{BE2} - V_{BE3}$.

From the above logarithmic relationship, it is apparent that I_{C4} becomes

$$I_{C4} = \frac{I_{C1}\, I_{C2}}{I_{C3}} = \frac{I_{PTAT}{}^2}{I_{CONST}}.$$

Thus, a current which has a square law characteristic and is $PTAT^2$, is generated for use as a means of curvature correction.

PROCESSING AND LAYOUT

The sensor is constructed using conventional bipolar epitaxial linear processing. SiCr thin-film resistors are used in place of their diffused counterparts as a result of their better tempco matching, an important consideration for resistors which must track over temperature. Such resistors include R1 and nR1 of the bandgap circuit.

Another point of interest in the construction of the device centers around transistors Q1 and Q2 of *Figure 4*. In order for the circuit to retain its accuracy over temperature, the leakage currents of each transistor, which can become quite significant at high temperatures, must be equal so that their effects will cancel one another. If the geometries of the two transistors were equivalent, then their leakage currents would be also, but since Q1 has ten times the emitter area of Q2, the accuracy of the device could suffer. To correct the problem, the circuit is built with Q1 and Q2 each replaced by a transistor group consisting of both Q1 and Q2. These transistor groups have equivalent geometries so that their leakage currents will cancel, but only one transistor of each group, representing Q1 in one group and Q2 in the other pair is used in the temperature sensing circuit. A circuit diagram demonstrating this idea is shown in *Figure 8*.

USING THE LM34

The LM34 is a versatile device which may be used for a wide variety of applications, including oven controllers and remote temperature sensing. The device is easy to use (there are only three terminals) and will be within 0.02°F of a surface to which it is either glued or cemented. The TO-46 package allows the user to solder the sensor to a metal surface, but in doing so, the GND pin will be at the same potential as that metal. For applications where a steady reading is desired despite small changes in temperature, the user can solder the TO-46 package to a thermal mass. Conversely, the thermal time constant may be decreased to speed up response time by soldering the sensor to a small heat fin.

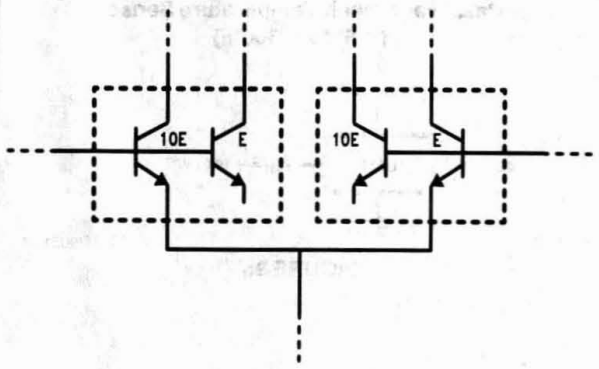

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FIGURE 8

FAHRENHEIT TEMPERATURE SENSORS

As mentioned earlier, the LM34 is easy to use and may be operated with either single or dual supplies. *Figure 9a* shows a simple Fahrenheit temperature sensor using a single supply. The output in this configuration is limited to positive temperatures. The sensor can be used with a single supply over the full −50°F to +300°F temperature range, as seen in *Figure 9b*, simply by adding a resistor from the output pin to ground, connecting two diodes in series between the GND pin and the circuit ground, and taking a differential reading. This allows the LM34 to sink the necessary current required for negative temperatures. If dual supplies are available, the sensor may be used over the full temperature range by merely adding a pull-down resistor from the output to the negative supply as shown in *Figure 9c*. The value of this resistor should be $|-V_S|/50\ \mu A$.

For applications where the sensor has to be located quite a distance from the readout circuitry, it is often expensive and inconvenient to use the standard 3-wire connection. To overcome this problem, the LM34 may be connected as a two-wire remote temperature sensor. Two circuits to do this are shown in *Figure 10a* and *Figure 10b*. When connected as a remote temperature sensor, the LM34 may be thought of as a temperature-dependent current source. In both configurations the current has both a relatively large value,

$$(20\ \mu A/°F) \times (T_A + 3°F),$$

and less offset when compared to other sensors. In fact, the current per degree Fahrenheit is large enough to make the output relatively immune to leakage currents in the wiring.

TEMPERATURE TO DIGITAL CONVERTERS

For interfacing with digital systems, the output of the LM34 may be sent through an analog to digital converter (ADC) to provide either serial or parallel data outputs as shown in *Figure 11* and *Figure 12*. Both circuits have a 0 to +128°F scale. The scales are set by adjusting an external voltage reference to each ADC so that the full 8 bits of resolution

Basic Fahrenheit Temperature Sensor
(+5° to +300°F)

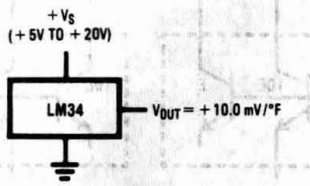

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FIGURE 9a

Temperature Sensor, Single Supply,
−50° to +300°F

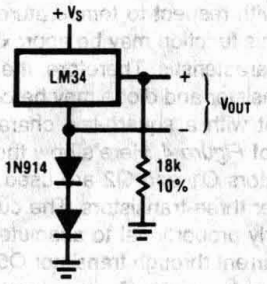

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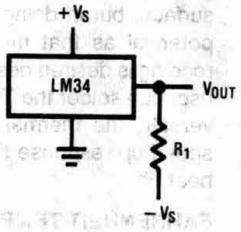
FIGURE 9b

Full-Range Fahrenheit Temperature Sensor



CHOOSE $R_1 = (-V_S)/50\ \mu A$
$V_{OUT} = +3{,}000$ mV AT +300°F
$= +750$ mV AT +75°F
$= -500$ mV AT −50°F

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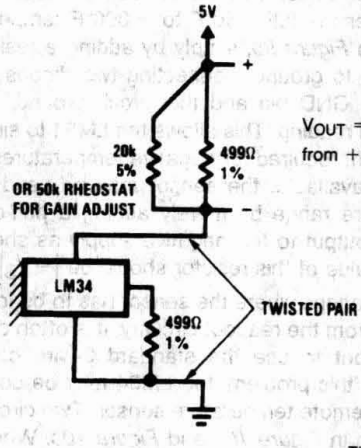
FIGURE 9c

Two-Wire Remote Temperature Sensor
(Grounded Sensor)



$V_{OUT} = 10$ mV/°F (T_A + 3°F)
from +3°F to +100°F

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FIGURE 10a

Two-Wire Temperature Sensor
(Output Referred to Ground)

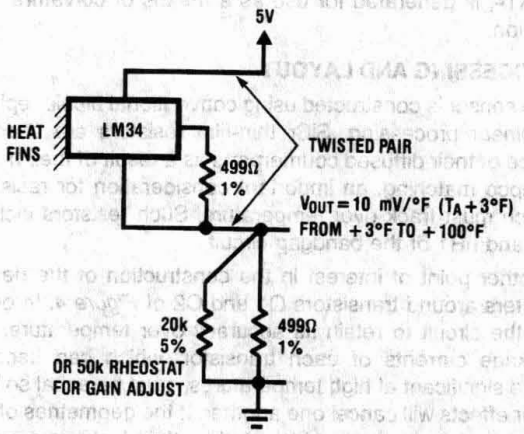

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FIGURE 10b

Temperature-to-Digital Converter (Serial Output, +128°F Full Scale)

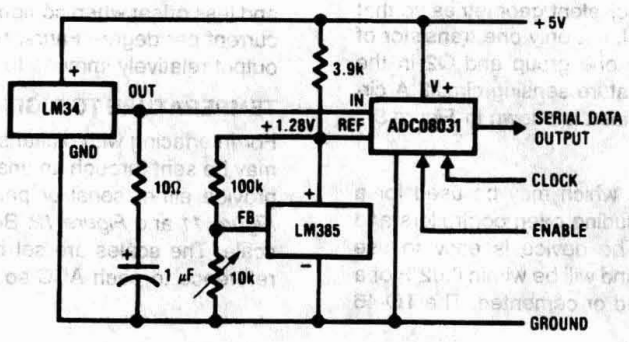

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FIGURE 11

Temperature-to-Digital Converter
(Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface, 128°F Full Scale)

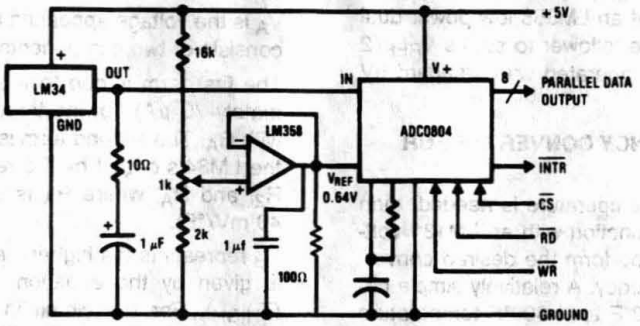

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FIGURE 12

LM34 with Voltage-to-Frequency Converter and Isolated Output
(3°F to +300°F; 30 Hz to 3000 Hz)

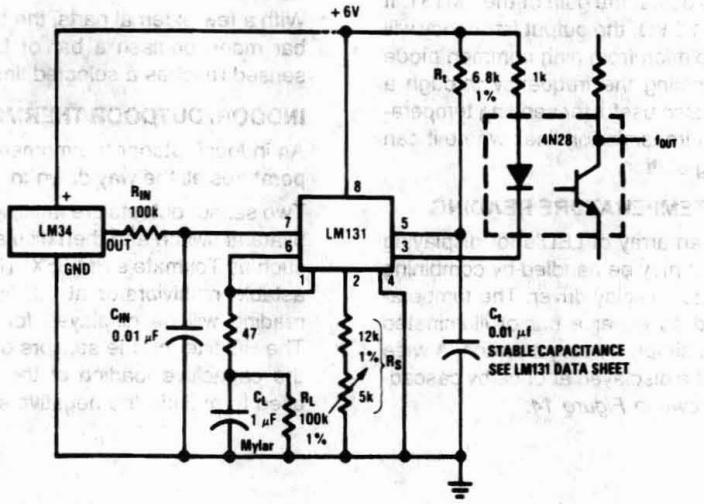

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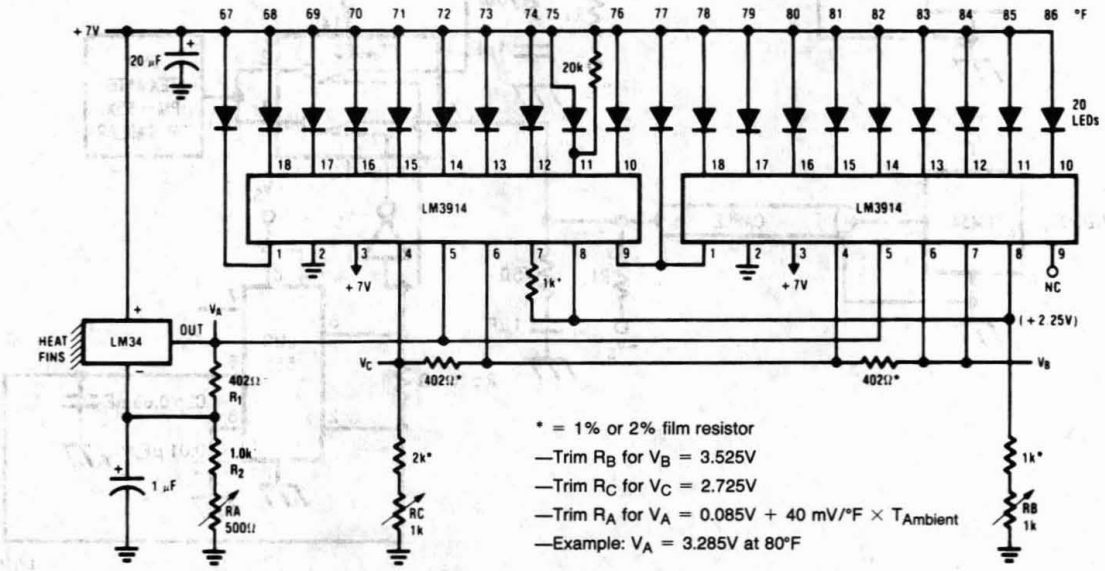
FIGURE 13

Bar-Graph Temperature Display (Dot Mode)



* = 1% or 2% film resistor
—Trim R_B for V_B = 3.525V
—Trim R_C for V_C = 2.725V
—Trim R_A for $V_A = 0.085V + 40\ mV/°F \times T_{Ambient}$
—Example: V_A = 3.285V at 80°F

FIGURE 14

TL/H/9051–17

will be applied over a reduced analog input range. The serial output ADC uses an LM385 micropower voltage reference diode to set its scale adjust (V_{REF} pin) to 1.28V, while the parallel output ADC uses half of an LM358 low power dual op amp configured as a voltage follower to set its $V_{REF}/2$ pin to 0.64V. Both circuits are operated with standard 5V supplies.

TEMPERATURE-TO-FREQUENCY CONVERTER FOR REMOTE SENSING

If a frequency proportional to temperature is needed, then the LM34 can be used in conjunction with an LM131 voltage-to-frequency converter to perform the desired conversion from temperature to frequency. A relatively simple circuit which performs over a +3°F to +300°F temperature range is shown in *Figure 13*. The output frequency of this circuit can be found from the equation:

$$f_{OUT} = \left(\frac{V_{IN}}{2.09V}\right)\left(\frac{R_S}{R_L}\right)\left(\frac{1}{R_t C_t}\right)$$

where resistor R_S is used to adjust the gain of the LM131. If R_S is set to approximately 14.2 kΩ, the output frequency will have a gain of 10 Hz/°F. Isolation from high common mode levels is provided by channeling the frequency through a photoisolator. This circuit is also useful for sending temperature information across long transmission lines where it can be decoded at the receiving station.

LED DISPLAY FOR EASY TEMPERATURE READING

It is often beneficial to use an array of LED's for displaying temperature. This application may be handled by combining the LM34 with an LM3914 dot/display driver. The temperature may then be displayed as either a bar of illuminated LED's or as a single LED by simply flipping a switch. A wide range of temperatures may be displayed at once by cascading several LM3914's as shown in *Figure 14*.

Without going into how the LM3914 drivers function internally, the values for V_A, V_B, and V_C can be determined as follows:

V_A is the voltage appearing at the output pin of the LM34. It consists of two components, 0.085V and (40 mV/°F) (T_A).

The first term is due to the LM34's bias current (approximately 70 μA) flowing through the 1 kΩ resistor in series with R_A. The second term is a result of the multiplication of the LM34's output by the resistive string composed of R_1, R_2, and R_A, where R_A is set for a gain factor of 4 (i.e.; 40 mV/°F).

V_B represents the highest temperature to be displayed and is given by the equation $V_B = 0.085V + (40\ mV/°F)(T_{HIGH})$. For the circuit in *Figure 14*, $V_B = 0.085V + (40\ mV/°F)(86°F) = 3.525V$.

V_C represents the lowest temperature to be displayed minus 1°F. That is, $V_C = 0.085V + (T_{LOW} - 1°F)(40\ mV/°F)$ which in this case becomes $V_C = 0.085V + (67°F - 1°F)(40\ mV/°F) = 2.725V$.

With a few external parts, the circuit can change from dot to bar mode or flash a bar of LED's when the temperature sensed reaches a selected limit (see LM3914 data sheet).

INDOOR/OUTDOOR THERMOMETER

An indoor/outdoor thermometer capable of displaying temperatures all the way down to −50°F is shown in *Figure 15*.

Two sensor outputs are multiplexed through a CD4066 quad bilateral switch and then displayed one at a time on a DVM such as Texmate's PM-35X. The LMC555 timer is run as an astable multivibrator at 0.2 Hz so that each temperature reading will be displayed for approximately 2.5 seconds. The RC filter on the sensors outputs are to compensate for the capacitive loading of the cable. An LMC7660 can be used to provide the negative supply voltage for the circuit.

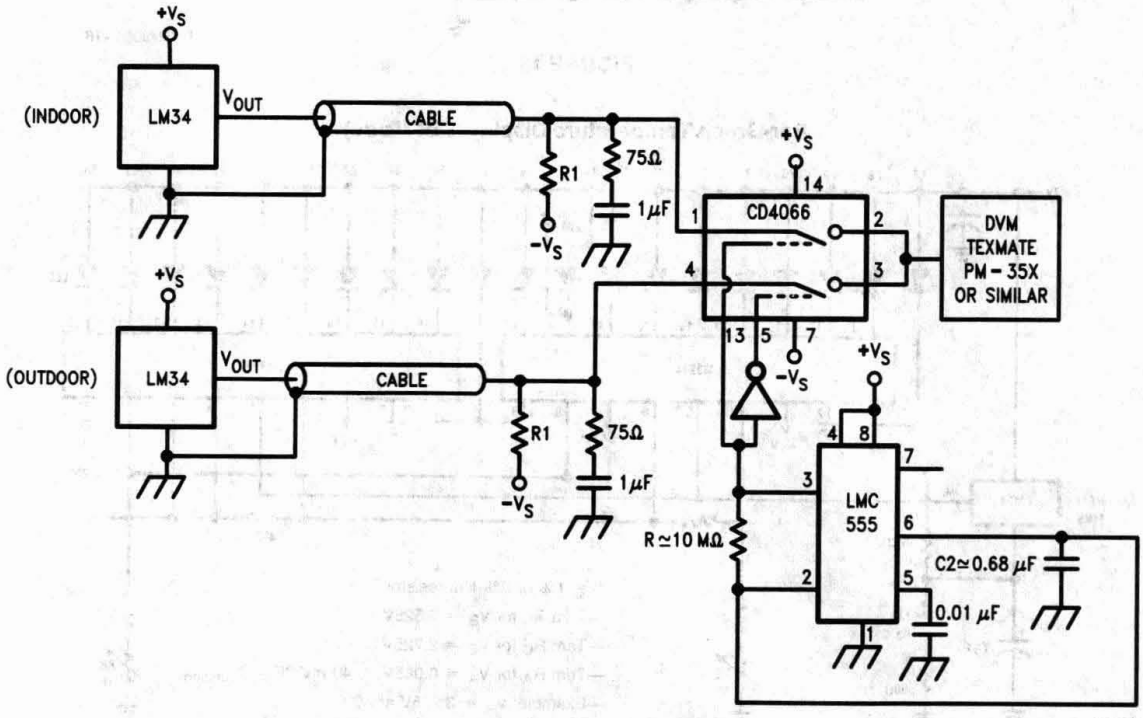


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FIGURE 15

TEMPERATURE CONTROLLER

A proportional temperature controller can be made with an LM34 and a few additional parts. The complete circuit is shown in *Figure 16*. Here, an LM10 serves as both a temperature setting device and as a driver for the heating unit (an LM395 power transistor). The optional lamp, driven by an LP395 Transistor, is for indicating whether or not power is being applied to the heater.

When a change in temperature is desired, the user merely adjusts a reference setting pot and the circuit will smoothly make the temperature transition with a minimum of overshoot or ringing. The circuit is calibrated by adjusting R2, R3 and C2 for minimum overshoot. Capacitor C2 eliminates DC offset errors. Then R1 and C1 are added to improve loop stability about the set point. For optimum performance, the temperature sensor should be located as close as possible to the heater to minimize the time lag between the heater application and sensing. Long term stability and repeatability are better than 0.5°F.

DIFFERENTIAL THERMOMETER

The differential thermometer shown in *Figure 17* produces an output voltage which is proportional to the temperature difference between two sensors. This is accomplished by using a difference amplifier to subtract the sensor outputs from one another and then multiplying the difference by a factor of ten to provide a single-ended output of 100 mV per degree of differential temperature.

Temperature Controller

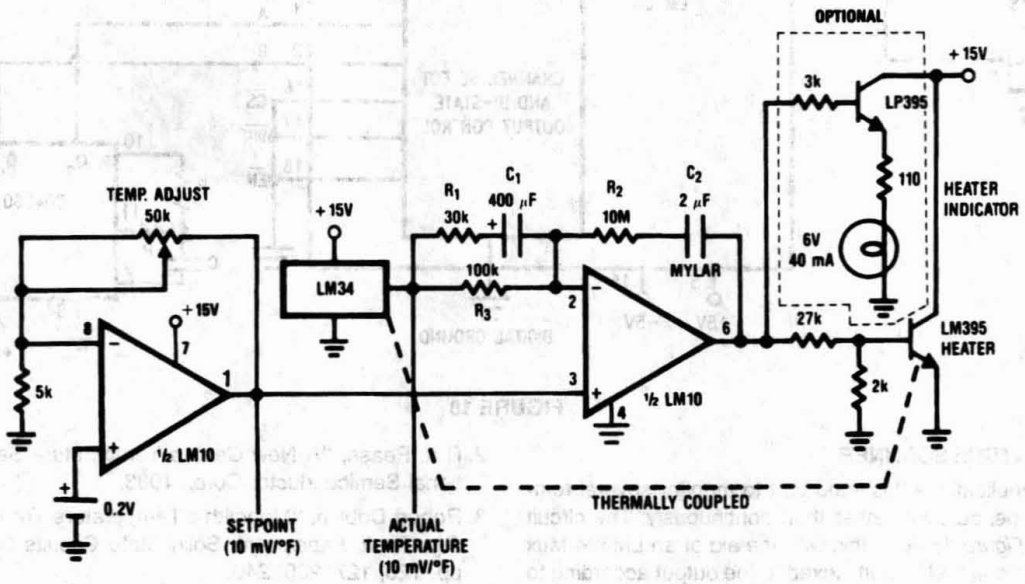

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FIGURE 16

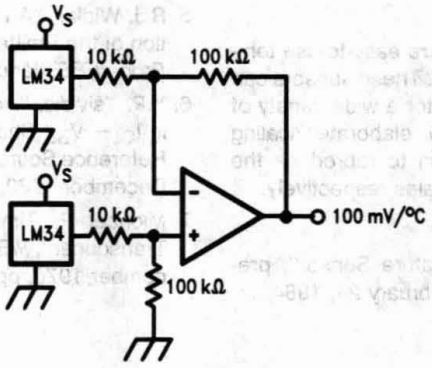

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FIGURE 17

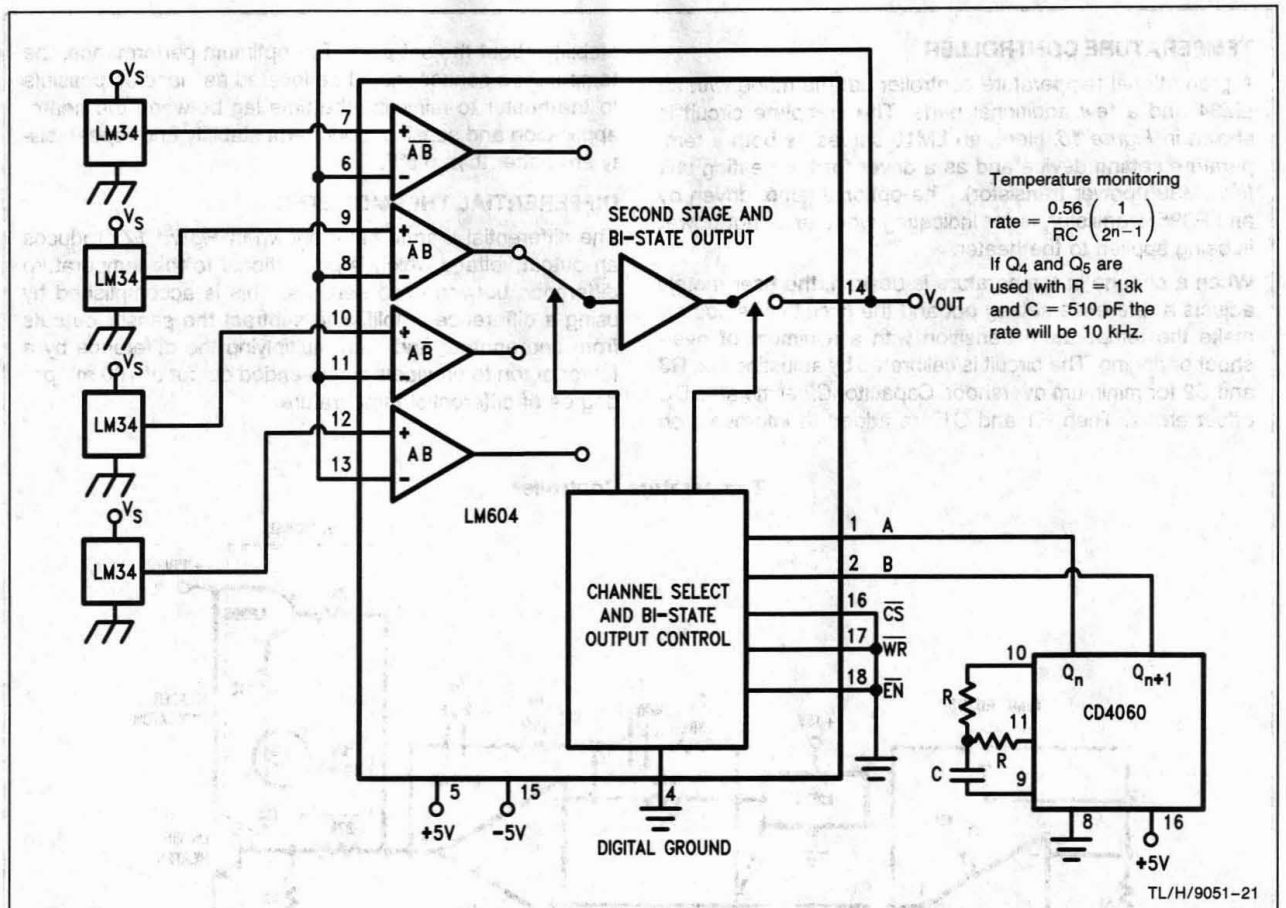

FIGURE 18

TEMPERATURE SCANNER

In some applications it is important to monitor several temperatures periodically, rather than continuously. The circuit shown in *Figure 18* does this with the aid of an LM604 Mux Amp. Each channel is multiplexed to the output according to the AB channel select. The CD4060 ripple binary counter has an on-board oscillator for continuous updating of the channel selects.

CONCLUSION

As can be seen, the LM34 and LM35 are easy-to-use temperature sensors with excellent linearity. These sensors can be used with minimal external circuitry for a wide variety of applications and do not require any elaborate scaling schemes nor offset voltage subtraction to reproduce the Fahrenheit and Celsius temperature scales respectively.

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Understanding The Operation of a CRT Monitor

National Semiconductor
Application Note 656
Zahid Rahim

Computer technology is going to see major advances in the 1990s. Users will see desk top computers with the computational power of today's super-computers. Even graphics capabilities for sophisticated 3 dimensional modeling and image processing would be available to the average user at a reasonable cost. In the area of electronic publishing; users will be able to store video images in the computer, merge the images with text and graphics and produce true color photorealistic hardcopies. Ultra high resolution monitors will be required to make such graphics capabilities available.

Display systems are available in various technologies such as cathode ray tubes (CRTs), liquid crystal displays (LCDs), electroluminescent displays (EL), plasma displays, and light emitting diodes (LEDs). However, for high resolution monitors the CRT has been and continues to be the technology of choice. Besides its awkward shape, weight and high voltage requirements, the CRT offers many advantages over its competitors. As opposed to other display systems that require a driver for each picture element (pixel), the CRT requires a single driver to drive the tube's cathode or three drivers for a color display. CRTs also offer excellent contrast, luminance and better display resolution than its counterparts. Even though the brightness of the CRT's screen is not uniform across the face of the screen, the variation from the center to the corners is gradual and may be unnoticeable to most viewers. In the case of LCD or LED displays, however, a very tight brightness level matching is required among the adjacent pixels. Continued improvements over the years and declining prices have made the CRT a popular choice for high resolution monitors.

The operation of a CRT monitor is basically very simple. A heating element in a CRT heats the cathode and causes it to emit electrons which are accelerated and focused on a phosphor screen by means of high voltage grids. An image (raster) is displayed by scanning the electron beam across the screen. Since the phosphor's luminance begins to fade after a short time, the image needs to be refreshed continually. In order to eliminate flicker, most monitors refresh the screen at a 60 Hz rate.

Figure 1 shows a simplified block diagram of a color CRT monitor. The entire circuitry within the monitor can be grouped into three main categories: video signal processing and amplification, horizontal/vertical deflection and synchronizing, and power supply. As shown in *Figure 1*, a transmission line or a coaxial cable carries the video signal from the host computer to the monitor. The video signal is usually a 1 V_{PP} signal and thus requires amplification before the signal can be applied to the CRT's cathode. The amplification of the video signal is usually done in two stages. A low voltage amplifier, often called a preamplifier, amplifies the 1 V_{PP} signal to a 4–6 V_{PP} signal. In addition to amplification, the preamplifier also provides contrast and brightness control. Contrast control allows the user to vary the gain of the video amplifier. Increasing the contrast for instance increases the video signal's level and thus causes the lighter portions of the raster to be brighter than the darker portions. The result is a sharp picture with contrasting light and dark. Brightness control on the other hand allows the user to change the brightness of the raster by varying the DC offset of the video signal. Increasing brightness in effect makes both the light and dark portions of the image brighter. Most preamplifiers also provide DC restoration or black level clamping which makes the brightness control possible. This will be described later in the text.

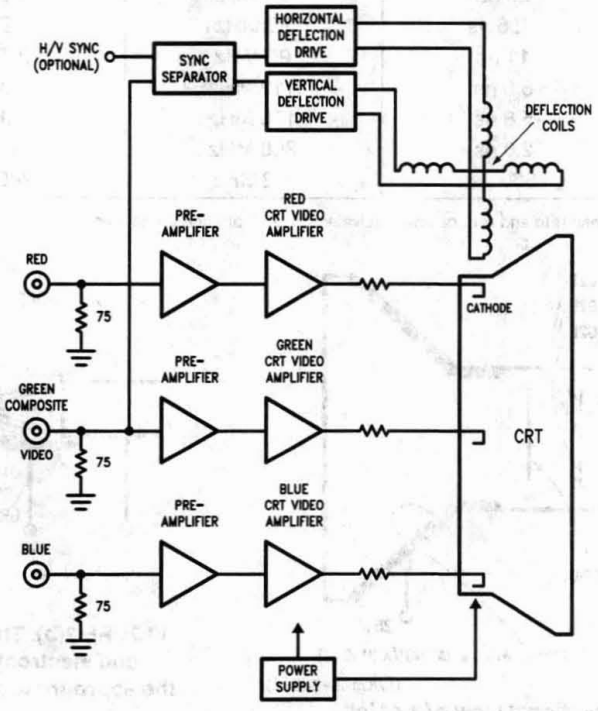

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FIGURE 1. Simplified Block Diagram of an RBG Monitor

CRT VIDEO AMPLIFIER PROVIDES HIGH VOLTAGE AMPLIFICATION

The CRT video amplifier is the second stage amplifier, it amplifies the preamplifier's 4–6 V_{PP} signal to a 40–60 V_{PP} signal that the cathode requires to energize each phosphor dot on the screen. In a color monitor, there is a trio of red, green and blue phosphor dots. Together, each trio constitutes a picture element, often called a pixel for short. The light emitted by the phosphor dot is proportional to the number of electrons striking the phosphor. Thus by modulating the voltage of each of the three cathodes in a color monitor, the corresponding phosphor dot is energized at varying intensities, thereby producing various shades of color. To change a pixel from black to peak white, the CRT video amplifier may be required to swing as much as 40 V_{PP}. The higher the display resolution of a monitor, the shorter the time available to energize each pixel. Thus high resolution monitors demand wide bandwidth amplifiers, which is generally not a problem when designing preamplifiers because of its low voltage swings of 4–6 V_{PP}. However, achieving wide bandwidth from a CRT video amplifier is no trivial task. The transistors required should not only have breakdown voltages of 70–80V but must also maintain f_T of 1 GHz to 2 GHz at high collector currents.

Table I illustrates the key requirements for various pixel display resolution monitors currently available in the market. Note that the maximum pixel time is derived assuming a 60 Hz frame refresh rate and retrace time equivalent to 30% of each frame time. Also as a rule of thumb, 33% of the pixel time is generally allocated to the rise/fall time of the signal at the CRT cathode. For ease of analysis we may assume that the CRT video amplifier is linear and has a single pole roll off. Thus the amplifier's bandwidth may be approximated as $f_{-3\ dB} = (0.35)/t_r$, where t_r is the signal rise time.

Figure 2(a) shows a simplified cross-sectional view of a color CRT. A heating element biased at approximately 6V and 500 mA to 2A (depending on the tube) heats up the cathodes. Heating the cathodes energizes the electrons in the cathodes and greatly aids in the emission of electrons. A large DC potential, on the order of several hundred volts more positive than the cathode is applied at the second grid, G2. This causes the electron beam to be accelerated towards the screen. Since the beam emerging from the cathode tends to diverge, a negative potential with respect to the cathode is applied at grid G1. By making G1 (also called control grid) more negative than the cathode, the electron beam begins to converge as shown in *Figure 2(b)*. This action is similar to beam focusing using an optical lense. Furthermore, by modulating the potential difference between the cathode and the control grid, the beam intensity and hence the brightness level is modulated. Finally the beam is electrostatically focused on the screen by adjusting grid G3's potential until the desired focus is achieved.

TABLE I

Display Resolution	Maximum Pixel Time	Minimum Pixel Clock Frequency	Required Rise Time at CRT Cathode	Required System Bandwidth ($f_{-3\ dB}$)
320 x 200	182 ns	5 MHz	60 ns	6 MHz
640 x 350	52 ns	19 MHz	17 ns	20 MHz
640 x 480	38 ns	26 MHz	12.5 ns	28 MHz
800 x 560	26 ns	38 MHz	8.6 ns	41 MHz
1024 x 900	12.6 ns	80 MHz	4.2 ns	84 MHz
1024 x 1024	11 ns	90 MHz	3.7 ns	95 MHz
1280 x 1024	8.9 ns	112 MHz	2.9 ns	120 MHz
1664 x 1200	5.8 ns	170 MHz	1.9 ns	180 MHz
2048 x 2048	2.8 ns	360 MHz	1 ns	380 MHz
4096 x 3300	860 ps	1.2 GHz	280 ps	1.23 GHz

Note: This table assumes 60 Hz refresh rate and retrace time equivalent to 30% of each frame time.

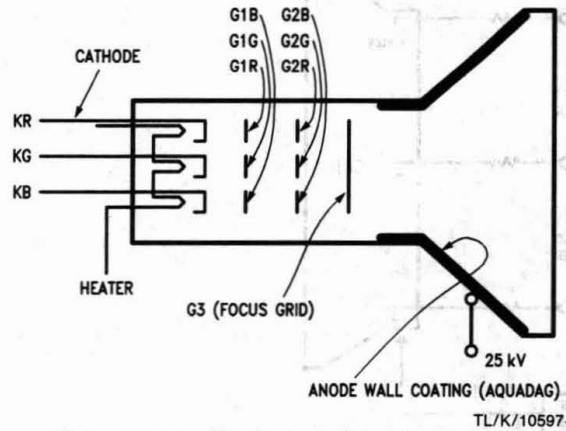

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FIGURE 2(a). A cross-sectional view of a color tube shows the arrangement of the grids.

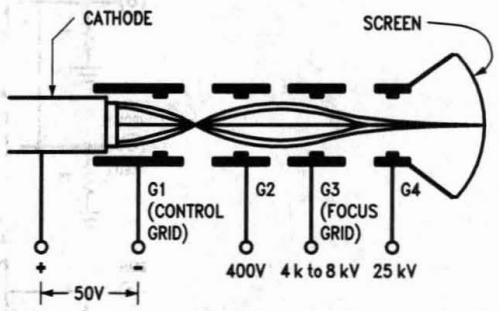

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FIGURE 2(b). The electron beam is accelerated and electrostatically focused by applying the appropriate potential at the respective grids.

COLOR TUBES REQUIRE ADJUSTMENTS TO BALANCE THE GUNS

As the cathode potential is increased with respect to G1, a potential is reached at which the beam spot on the screen disappears. This potential is called the spot cutoff voltage and thus corresponds to the voltage that produces the black level. The cutoff voltage is usually different for each of the three guns in a color tube. Thus the cutoff voltage needs to be individually adjusted for each gun so that at cutoff all three guns are at the black level. For a picture tube of the type shown in *Figure 2*, the adjustment can be made by individually adjusting the potential at the corresponding control grid, G1. However, most modern day color tubes uses a unitized gun in which G1 and G2 are common to all three guns. Among the advantages of a unitized gun are that it produces a better spot size resulting in bright pictures and better gray scale tracking. Cutoff voltage adjustment in a unitized gun now requires that the cathode voltages be adjusted. This places a burden on the CRT video amplifier because the large variation of cutoff voltages within the tube must now be compensated by adjusting the video amplifier's DC offset. The spot cutoff design curves for a typical unitized tube is shown in *Figure 3*. At grid 2 to grid 1 voltage ($V_{G2}-V_{G1}$) of 400V the cathode to grid 1 cutoff voltage varies from 50V to 70V as shown by the curves. Thus if the CRT video amplifiers are coupled directly to the cathodes and with V_{G1} = 0V, the amplifiers must be designed to be able to swing at least as high as 70V because of the 20V variation between the guns within the tube. Note that biasing G2 at a higher potential would be desirable because of the improved spot size, consequently a brighter picture. However, doing so would require a higher cutoff voltage and thus place a heavier burden on the amplifier driving the cathode. In contrast, a monochrome CRT doesn't have this problem because of the single gun.

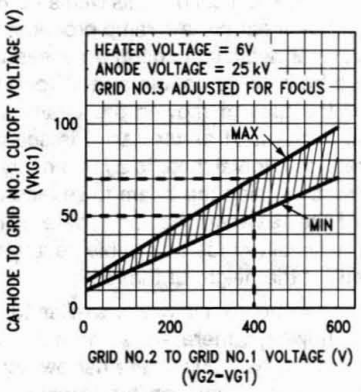

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FIGURE 3. Spot Cutoff Characteristics for a Typical Color Tube

Neutral white is the most difficult color to produce in a color monitor because the light emitting efficiency of R, G and B phosphors is different. Thus a specific proportion of R, G and B drive levels are required at the three cathodes to produce neutral white. The peak amplitude of the cathode drive signal determines the shade of white that will be displayed. Thus neutral white is produced by adjusting the AC gain of each of the three preamplifiers. Usually the red gun is driven at maximum gain because of red phosphors's lowest efficiency, and, the gain of the green and blue guns are reduced until the desired balance is achieved. Keep in mind that once the gain adjustments have been made, the contrast control will vary the gain of all three guns simultaneously. Also the color on the screen should not change as the screen's brightness level is changed, this is often referred to as gray scale tracking. Good gray scale tracking requires that the amplifiers have good differential gain characteristics as well as good DC output tracking capability. Furthermore, the amplifiers should also track well over a wide range of contrast adjustment.

Manufacturers of computers and monitors generally follow the EIA standard RS-343 for video signal. The RS-343 standard specifies the various video signal levels relative to a reference level. It is interesting to note that no DC component is specified, the reason is that the standard was developed for television. Since the video signal in broadcast television travels through air, the DC component of the signal is lost. At the receiving end the signal is AC coupled. However, a DC restoration circuit is required to reinsert the DC component of the video signal. By reinserting the DC component of the video signal, brightness of each line is restored since the brightness may be different for each line. DC restoration is thus essential for producing the correct background illumination or shading. Likewise for monitors, the video signal is AC coupled at the input so that the monitor can easily interface with computers from various manufacturers.

Figure 4a shows the 1 V_{PP} composite video signal with sync tip. The signal at the cathode is an amplified signal of opposite phase as shown in *Figure 4b*. The video signal for three

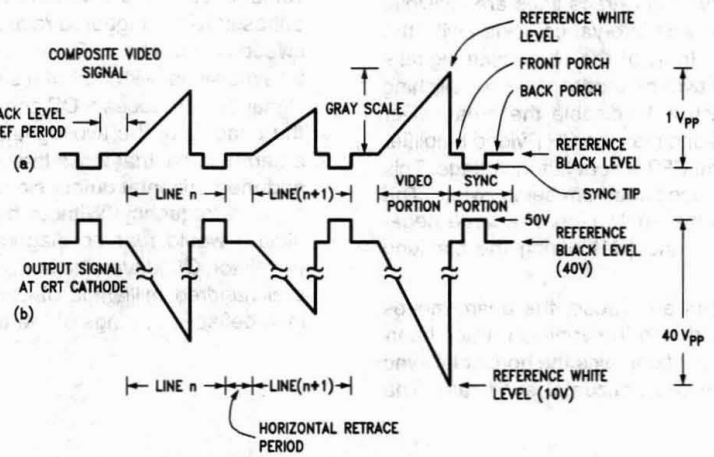

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FIGURE 4. The composite video signal is a 1 V_{PP} signal that carries both the amplitude and sync information (a). A wide bandwidth inverting amplifier amplifies the signal at the cathode (b).

lines of the raster are shown. Since the video signal is amplitude modulated, the signal's amplitude relative to the reference black level specifies the relative DC component of each line on the raster. The DC component of the video signal is thus restored by clamping the black level at a fixed reference potential (e.g., 40V), corresponding to the CRT's beam cutoff voltage. The video signal's video portion contains the gray scale information (i.e., the signal's amplitude) whereas the sync portion contains the timing information required for horizontal and vertical synchronization.

DC restoration of the video signal can be done in two ways. The first method is to use a simple diode clamp to clamp the signal at the reference black level. Diode clamping can be done either at the AC coupled input of the preamplifier or at the AC coupled output of the CRT video amplifier. The disadvantage of diode clamping is that the black level is sensitive to fluctuations in the power supply as well as noise coupling and temperature drift of the diode's forward drop. A more effective approach for DC restoration is to do a dynamic black level clamping at the back porch of each video signal. This requires the use of comparator within the feedback loop of the CRT video amplifier and the preamplifier. During the horizontal retrace period, the comparator compares the DC feedback taken from the CRT video amplifier's output with the voltage set by the brightness control potentiometer. Depending on the CRT video amplifier's output voltage, a clamping capacitor at the output of the comparator is either charged or discharged so that the feedback loop is stabilized and the video signal is restored to the black level. During the video portion of the signal, the comparator is disabled and the clamping capacitor holds the black level reference voltage until it is refreshed at the beginning of the next line. The beginning of each new line always starts from a fixed reference black level and the DC component of each line is restored. This approach not only offers excellent power supply rejection but also there is minimal black level drift because the black level is brought back to the correct reference potential during each horizontal retrace period.

WITHOUT DEFLECTION CIRCUITRY THERE WOULD BE NO RASTER

An image is displayed in a CRT by scanning the electron beam across the face of the screen. The beam is scanned from left to right on each line, moreover, at the end of each line the beam drops down to the beginning of the next line. The motion from right to left is called horizontal retrace. During the horizontal retrace interval the electron gun is biased at a potential such that the retrace lines are invisible. Note that the horizontal retrace interval coincides with the horizontal blanking interval (part of the composite signal's sync portion). There are two methods of accomplishing blanking. The first approach is to disable the preamplifier during the blanking interval and bias the CRT video amplifier at a potential higher than the CRT's spot cutoff voltage. This effectively prevents the retrace lines from being visible. The second approach involves the application of a large negative potential at the control grid (G1) during the blanking interval.

Once all lines on the screen are traced, the beam moves from the bottom to the top during the vertical retrace interval. The composite video signal contains the horizontal sync pulse which is repeated at the horizontal scan rate. The horizontal scan rate may be anywhere from 15 kHz to 240 kHz depending on the resolution of the monitor. The vertical sync pulse is much wider than the horizontal sync pulse and occurs at the end of the raster, i.e., after all lines in the frame have been traced. The vertical sync pulse is repeated at a 60 Hz rate. For proper operation, a sync separator separates the horizontal and vertical sync pulses from the composite video signals.

The simplified block diagram of *Figure 5* shows the circuitry required for horizontal and vertical scanning, also shown is a high voltage flyback power supply. The composite video signal is AC coupled to the input of the sync amplifier Q1, whose gain is determined by the ratio of its collector and emitter resistors. The inverted video signal appears at the collector of Q1 and is buffered by the emitter follower Q2. Q3 is essentially a saturating sync switch that removes the signals' video portion and leaves only the sync pulses. Resistors R8 and R9 bias Q3's base at a potential below the cutin voltage of the transistor so that Q3 is normally off. When the composite video signal's level is between the blanking level and the sync tip, Q3 saturates and produces a negative going pulse at Q3's collector. The buffered output of Q4 is a composite sync signal that contains both the horizontal and vertical sync pulses. A two stage RC low pass filter separates the 60 Hz vertical sync pulses from the composite signal.

The vertical sync pulses trigger the vertical oscillator so that the oscillator is locked at 60 Hz. The vertical oscillator is usually a relaxation oscillator and drives the power transistor Q5 with a 60 Hz sawtooth voltage waveform. Q5 in turn energizes the vertical deflection coils with a 60 Hz sawtooth current ramp. The linear current ramp produces a magnetic field in the vertical deflection coil and causes the electron beam to move from top to bottom at a uniform speed. This accomplishes the task of moving the beam progressively from one line to the next as the raster is scanned. During the vertical retrace interval there is a rapid decrease in Q5's collector current, causing the beam to retrace rapidly from the bottom of the raster to the top. The amplitude of the current ramp is usually made adjustable because this allows the user to adjust the height of the raster.

The horizontal sweep circuit works similar to the vertical sweep circuit, however, there are some major differences. Since the horizontal sync pulses are narrow and operate at high frequency, they are susceptible to noise impulses. In order to maintain trouble free synchronization, an automatic frequency control (AFC) circuit is used. Moreover, the horizontal oscillator is a voltage controlled oscillator (VCO) as opposed to the triggered relaxation oscillator for the vertical sweep circuit. The AFC compares the phase of the horizontal sync signal with that of a sample of the horizontal output signal and produces a DC correction voltage proportional to the phasing of the two signals. The AFC's output signal is an error signal that locks the VCO such that the sync signal and the horizontal output signal are maintained at the sync signal's frequency. Without horizontal synchronization, the picture would tear up diagonally. Finally, a power output transistor, Q6, drives the horizontal deflection coils with several hundred milliamps of current depending on the mA/inch deflection ratings of the tube.

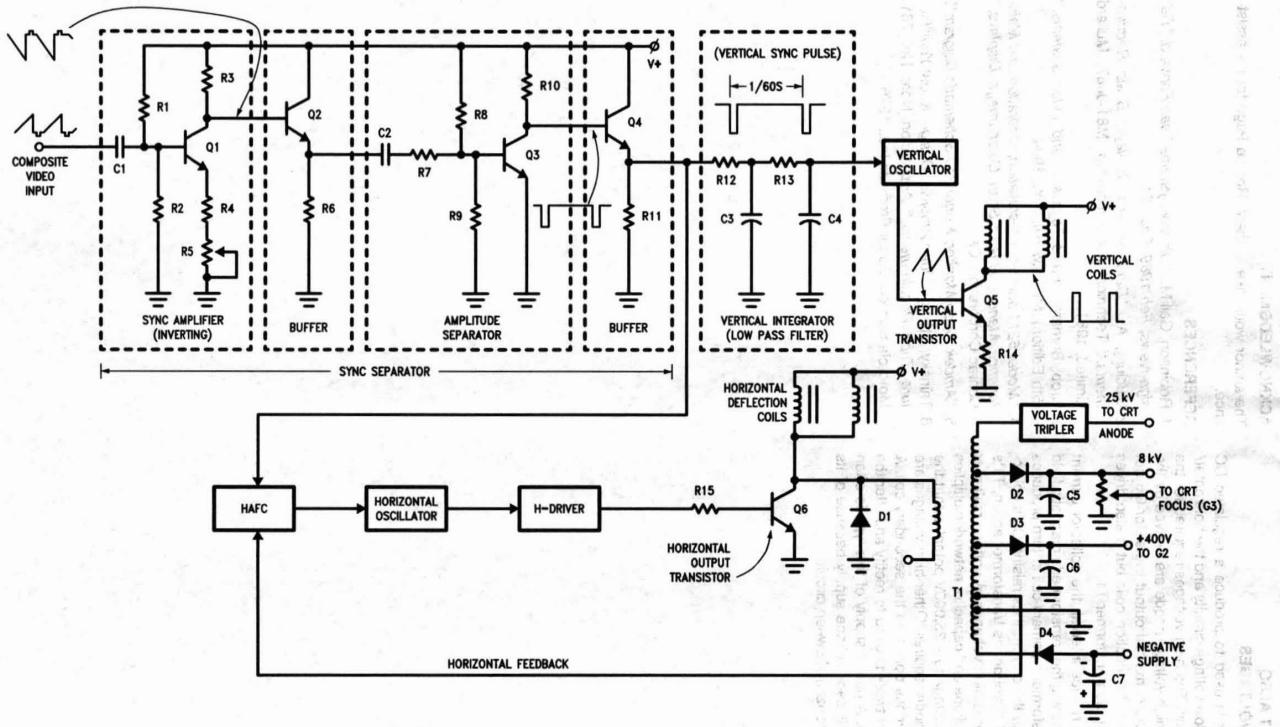

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FIGURE 5. Simplified Block Diagram of the Deflection Circuitry and the Flyback Power Supply

THE SWEEP CIRCUIT ALSO GENERATES HIGH VOLTAGES

A switching regulator is used to produce a regulated DC voltage to power the low voltage circuits and the horizontal/vertical scanning circuit. The high voltages required for the CRT's grids and the high voltage anode are derived by the transformer action. The horizontal output transistor Q6 not only drives the horizontal deflection coils but it also drives the primary of the step up transformer T1.

During the horizontal retrace interval, the collector current of Q6 drops rapidly causing the transformer's magnetic field to collapse. The transformer's primary coil in turn produces a back EMF to sustain the current thus raising Q6's collector to a high potential. Through the transformer action, T1's secondary coil produces high voltages. A voltage multiplier circuit consisting of a diode and capacitor network multiplies the secondary coil's voltage to a 25,000V potential that the tube's high voltage anode requires. Other high voltages are derived by tapping various points on the secondary coil. A diode and capacitor network is used to rectify and filter the power supply voltage. A power supply of this type is often called a scanning or flyback voltage supply because of its association with the horizontal sweep circuit.

ACKNOWLEDGMENT

The author would like to thank Ronald Page for his assistance.

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LM628 Programming Guide

National Semiconductor
Application Note 693
Steven Hunt

INTRODUCTION

The LM628/LM629 are dedicated motion control processors. Both devices control DC and brushless DC servo motors, as well as, other servomechanisms that provide a quadrature incremental feedback signal. Block diagrams of typical LM628/LM629-based motor control systems are shown in *Figures 1* and *2*.

As indicated in the figures, the LM628/LM629 are bus peripherals; both devices must be programmed by a host processor. This application note is intended to present a concrete starting point for programmers of these precision motion controllers. It focuses on the development of short programs that test overall system functionality and lay the groundwork for more complex programs. It also presents a method for tuning the loop-compensation PID filter.†

REFERENCE SYSTEM

Figure 18 is a detailed schematic of a closed-loop motor control system. All programs presented in this paper were developed using this system. For application of the programs in other LM628-based systems, changes in basic programming structure are not required, but modification of filter coefficients and trajectory parameters may be required.

I. PROGRAM MODULES

Breaking programs for the LM628 into sets of functional blocks simplifies the programming process; each block executes a specific task. This section contains examples of the principal building blocks (modules) of programs for the LM628.

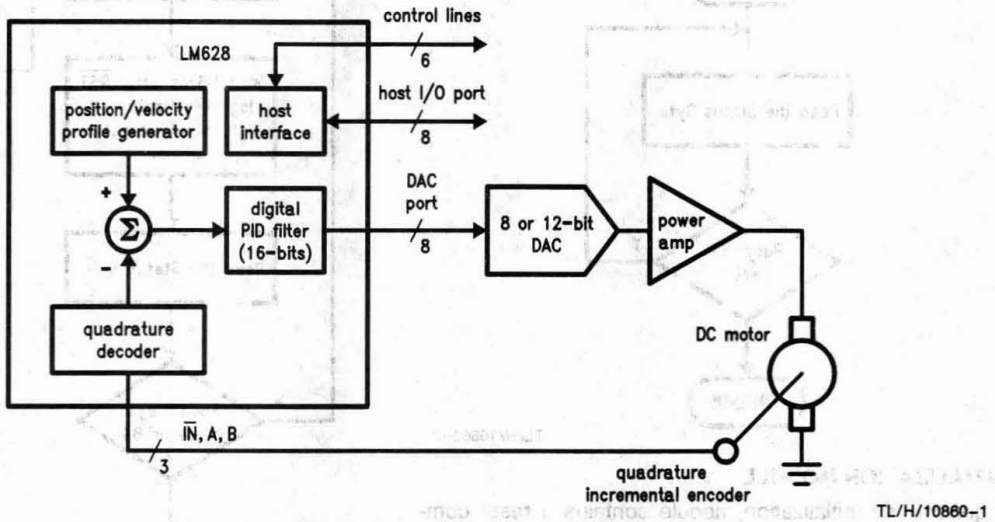


FIGURE 1. LM628-Based Motor Control System

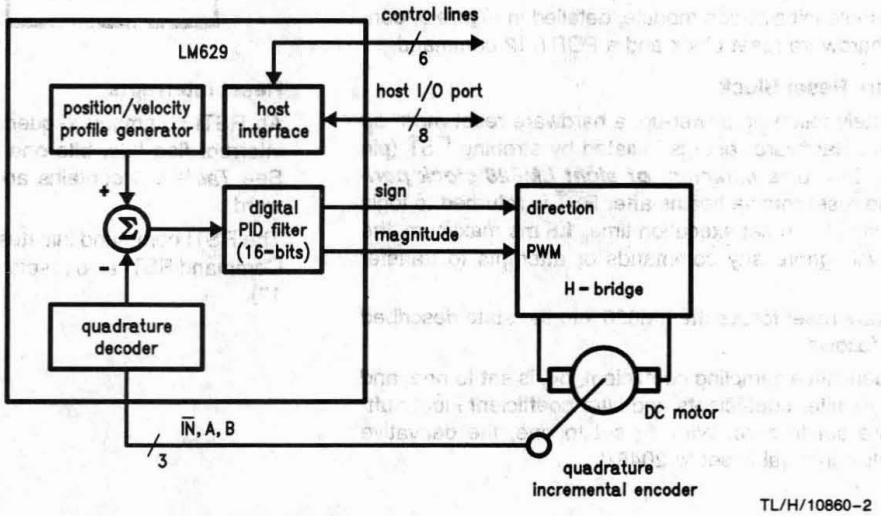


FIGURE 2. LM629-Based Motor Control System

†**Note:** For the remainder of this paper, all statements about the LM628 also apply to the LM629 unless otherwise noted.

BUSY-BIT CHECK MODULE

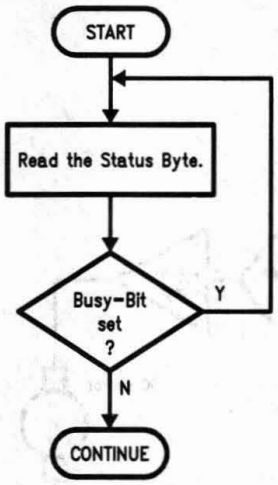
The first module required for successful programming of the LM628 is a busy-bit check module.

The busy-bit, bit zero of the status byte, is set immediately after the host writes a command byte, or reads or writes the second byte of a data word. See *Table I*. While the busy-bit is set, the LM628 will ignore any commands or attempts to transfer data.

A busy-bit check module that polls the Status Byte and waits until the busy-bit is reset will ensure successful host/LM628 communications. ***It must be inserted after a command write, or a read or write of the second byte of a data word.*** *Flow diagram 1* represents such a busy-bit check module. This module will be used throughout subsequent modules and programs.

Reading the Status Byte is accomplished by executing a RDSTAT command. RDSTAT is directly supported by LM628 hardware and is executed by pulling $\overline{CS}$, $\overline{PS}$, and $\overline{RD}$ logic low.

Flow Diagram 1. Busy-bit Check Module



TL/H/10860–3

INITIALIZATION MODULE

In general, an initialization module contains a reset command and other initialization, interrupt control, and data reporting commands.

The example initialization module, detailed in *Figure 3*, contains a hardware reset block and a PORT 12 command.

Hardware Reset Block

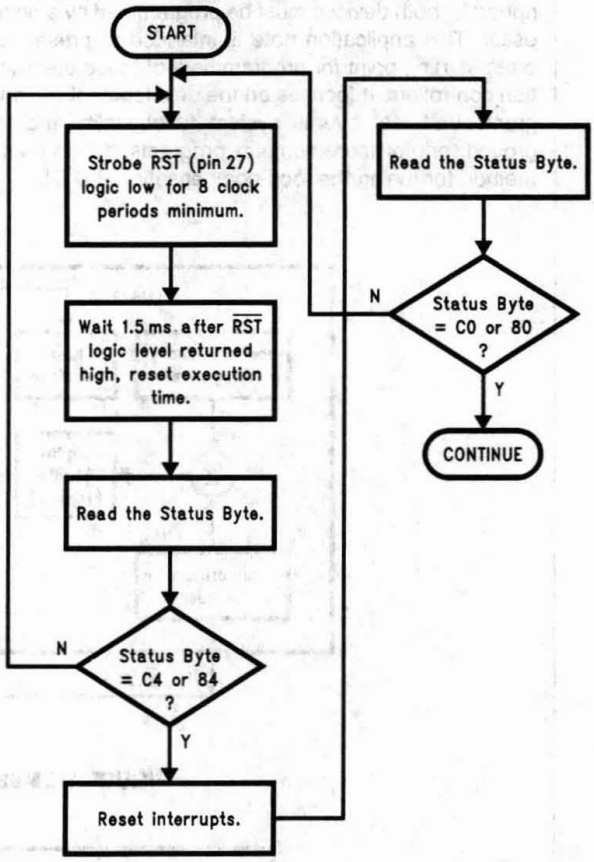
Immediately following power-up, a hardware reset ***must be*** executed. Hardware reset is initiated by strobing $\overline{RST}$ (pin 27) logic low for ***a minimum of eight LM628 clock periods.*** The reset routine begins after $\overline{RST}$ is returned to logic high. During the reset execution time, **1.5 ms** maximum, the LM628 will ignore any commands or attempts to transfer data.

A hardware reset forces the LM628 into the state described in what follows.

1. The derivative sampling coefficient, d_S, is set to one, and all other filter coefficients and filter coefficient input buffers are set to zero. With d_S set to one, the derivative sampling interval is set to $2048/f_{CLK}$.
2. All trajectory parameters and trajectory parameters input buffers are set to zero.
3. The current absolute position of the shaft is set to zero ("home").
4. The breakpoint interrupt is masked (disabled), and the remaining five interrupts are unmasked (enabled).
5. The position error threshold is set to its maximum value, 7FFF hex.
6. The DAC output port is set for an 8-bit DAC interface.

Flow diagram 2 illustrates a hardware reset block that includes an LM628 functionality test. This test *should be* completed immediately following all hardware resets.

Flow Diagram 2. Hardware Reset Block


START
Strobe RST (pin 27) logic low for 8 clock periods minimum.
Wait 1.5 ms after RST logic level returned high, reset execution time.
Read the Status Byte.
Status Byte = C4 or 84 ?
N
Y
Reset Interrupts.
Read the Status Byte.
Status Byte = C0 or 80 ?
N
Y
CONTINUE

TL/H/10860–5

Reset Interrupts

An RSTI command sequence allows the user to reset the interrupt flag bits, bits one through six of the status byte. See *Table I*. It contains an RSTI command and one data word.

The RSTI command initiates resetting the interrupt flag bits. Command RSTI also resets the host interrupt output pin (pin 17).

Port	Bytes	Command	Comments
	(Note 4)	hardware reset	Strobe $\overline{RST}$, pin 27, logic low for eight clock periods minimum.
		wait	The maximum time to complete hardware reset tasks is 1.5 ms. During this reset execution time, the LM628 will ignore any commands or attempts to transfer data.
c (Note 1)	xx (Note 2)	RDSTAT	This command reads the status byte. It is directly supported by LM628 hardware and can be executed at any time by pulling $\overline{CS}$, $\overline{PS}$, and $\overline{RD}$ logic low. Status information remains valid as long as $\overline{RD}$ is logic low.
		decision	If the status byte is C4 hex or 84 hex, continue. Otherwise loop back to hardware reset.
c	1D	RSTI	This command resets *only* the interrupts indicated by zeros in bits one through six of the next data word. It also resets bit fifteen of the Signals Register and the host interrupt output pin (pin 17).
		Busy-bit Check Module	
d	xx	HB (Note 3)	don't care
d	00	LB	Zeros in bits one through six indicate *all* interrupts will be reset.
		Busy-bit Check Module	
c	xx	RDSTAT	This command reads the status byte.
		decision	If the status byte is C0 hex or 80 hex, continue. Otherwise loop back to hardware reset.
c	06	PORT12	The reset default size of the DAC port is eight bits. This command initializes the DAC port for a 12-bit DAC. It should not be issued in systems with an 8-bit DAC.
		Busy-bit Check Module	

FIGURE 3. Initialization Module (with Hardware Reset)

Note 1: The 8-bit host I/O port is a dual-mode port; it operates in command or data mode. The logic level at $\overline{PS}$ (pin 16) selects the mode. Port c represents the LM628 command port-commands are written to the command port and the Status Byte is read from the command port. A logic level of "0" at $\overline{PS}$ selects the command port. Port d represents the LM628 data port—data is both written to and read from the data port. A logic level of "1" at $\overline{PS}$ selects the data port.

Note 2: x - don't care

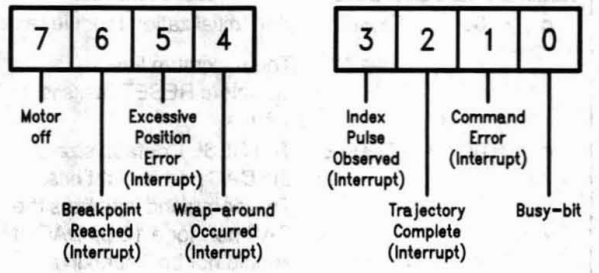
Note 3: HB - high byte, LB - low byte

Note 4: All values represented in hex.

Immediately following the RSTI command, a single data word is written. The first byte is not used. Logical zeros in bits one through six of the second byte reset the corresponding interrupts. See *Table II*. Any combination of the interrupt flag bits can be reset within a single RSTI command sequence. This feature allows interrupts to be serviced according to a user-programmed priority.

In the case of the example module, the second byte of the RSTI data word, 00 hex, resets *all* interrupt flag bits. See *Figure 3*.

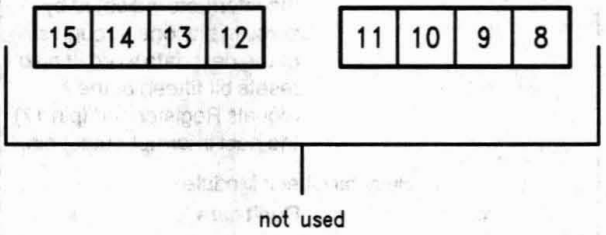
TABLE I. Status Byte Bit Allocation



TL/H/10860–6

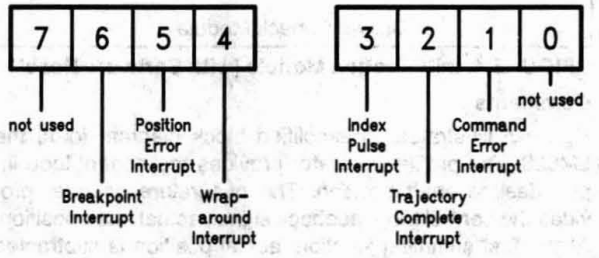
TABLE II. Interrupt Mask/Reset Bit Allocations

high byte



TL/H/10860–7

low byte



TL/H/10860–8

DAC Port Size

During both hardware and software resets, the DAC output port defaults to 8-bit mode. If an LM628 control loop utilizes a 12-bit DAC, command PORT12 should be issued immediately following the hardware reset block and all subsequent resets. Failure to issue command PORT12 will result in erratic, unpredictable motor behavior.

If the control loop utilizes an 8-bit DAC, command PORT12 must not be executed; this too will result in erratic, unpredictable motor behavior.

An LM629 will ignore command PORT8 (as it provides an 8-bit sign/magnitude PWM output). Command PORT12 *should not* be issued in LM629-based systems.

Software Reset Considerations

After the initial hardware reset, resets can be accomplished with either a hardware reset or command RESET (software reset). Software and hardware resets execute the same tasks† and require the same execution time, 1.5 ms maximum. During software reset execution, the LM628 will ignore any commands or attempts to transfer data.

The hardware reset module includes an LM628 functionality test. This test is ***not*** required after a software reset.

Figure 4 details an initialization module that uses a software reset.

†In the case of a software reset, the position error threshold remains at its pre-reset value.

Port	Bytes	Command	Comments
c	00	RESET	See Initialization Module text.
		wait	The maximum time to complete RESET tasks is 1.5 ms.
c	06	PORT12	The RESET default size of the DAC port is eight bits. This command initializes the DAC port for a 12-bit DAC. It should not be issued in a system with an 8-bit DAC.
		Busy-bit Check Module	
c	1D	RSTI	This command resets *only* the interrupts indicated by zeros in bits one through six of the next data word. It also resets bit fifteen of the Signals Register and (pin 17) the host interrupt output pin.
		Busy-bit Check Module	
d	xx	HB	Don't care
d	00	LB	Zeros in bits one through six indicate *all* interrupts will be reset.
		Busy-bit Check Module	

FIGURE 4. Initialization Module (with Software Reset)

Comments

Figure 5 illustrates, in simplified block diagram form, the LM628. The profile generator provides the control loop input, desired shaft position. The quadrature decoder provides the control loop feedback signal, actual shaft position. At the first summing junction, actual position is subtracted from desired position to generate the control loop error signal, position error. This error signal is filtered by the PID filter to provide the motor drive signal.

After executing the example initialization module, the following observations are made. With the integration limit term (i_L) and the filter gain coefficients (k_p, k_i, and k_d) initialized to zero, the filter gain is zero. Moreover, after a reset, desired shaft position tracks actual shaft position. Under these conditions, the motor drive signal is zero. The control system can not affect shaft position. The shaft should be stationary and "free wheeling". If there is significant drive amplifier offset, the shaft may rotate slowly, but with minimal torque capability.

Note: Regardless of the free wheeling state of the shaft, the LM628 continuously tracks shaft absolute position.

FILTER PROGRAMMING MODULE

The example filter programming module is shown in *Figure 6*.

Load Filter Parameters (Coefficients)

An LFIL (Load FILter) command sequence includes command LFIL, a filter control word, and a variable number of data words.

The LFIL command initiates loading filter coefficients into input buffers.

The two data bytes, written immediately after LFIL, comprise the filter control word. The first byte programs the derivative sampling coefficient, d_s (i.e. selects the derivative sampling interval). The second byte indicates, with logical ones in respective bit positions, which of the remaining four filter coefficients will be loaded. See *Tables III* and *IV*. Any combination of the four coefficients can be loaded within a single LFIL command sequence.

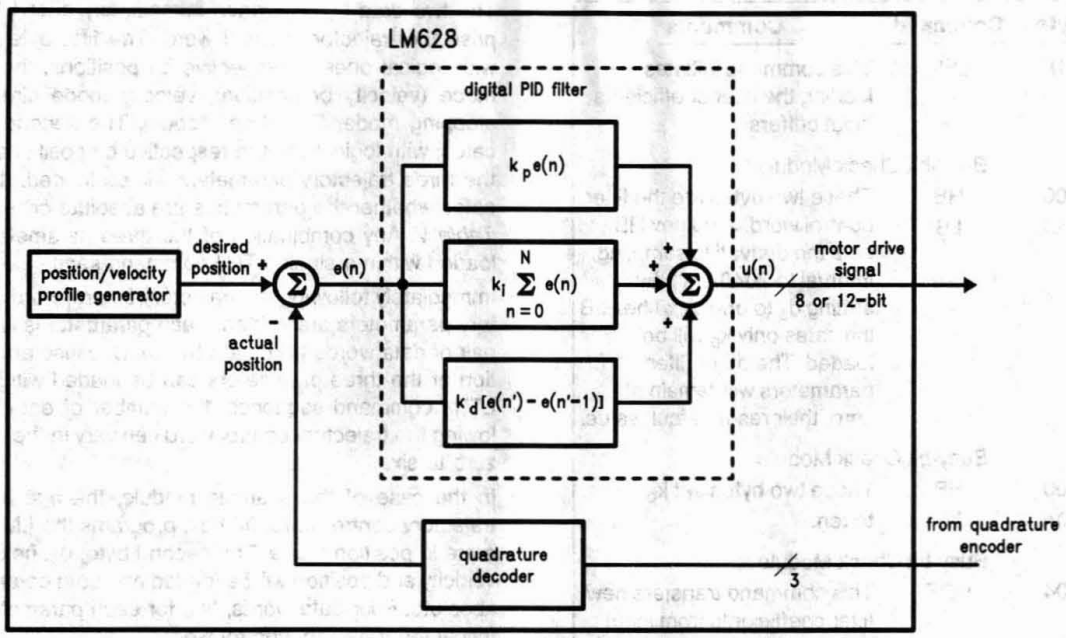
Immediately following the filter control word, the filter coefficients are written. Each coefficient is written as a pair of data bytes, a data word. Because any combination of the four coefficients can be loaded within a single LFIL command sequence, the number of data words following the filter control word can vary in the range from zero to four.

In the case of the example module, the first byte of the filter control word, 00 hex, programs a derivative sampling coefficient of one. The second byte, x8 hex, indicates only the proportional gain coefficient will be loaded.

Immediately following the filter control word, the proportional gain coefficent is written. In this example, k_p is set to ten with the data word 000A hex. The other three filter coefficients remain at zero, their reset value.

Update Filter

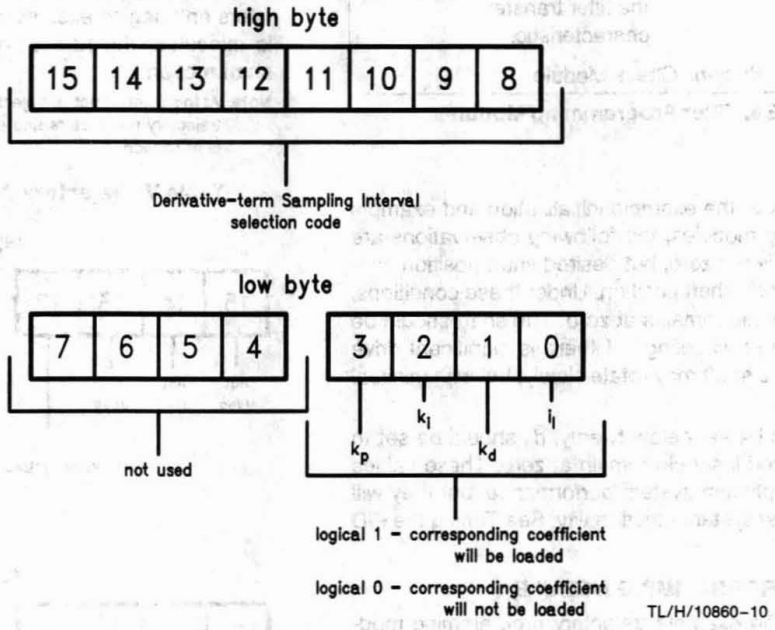
The update filter command, UDF, transfers new filter coefficients from input buffers to working registers. Until UDF is executed, the new filter coefficients do not affect the transfer characteristic of the filter.



TL/H/10860–9

FIGURE 5. LM628—Simplified Block Diagram Form

TABLE III. Filter Control Word Bit Allocation



TL/H/10860–10

TABLE IV. Derivative—Term Sampling Interval Selection Codes

Filter Control Word Bit Position								d_s	Selected Derivative-Term Sampling Interval—T_d
15	14	13	12	11	10	9	8		
0	0	0	0	0	0	0	0	1	T_s
0	0	0	0	0	0	0	1	2	$2T_s$
0	0	0	0	0	0	1	0	3	$3T_s$
0	0	0	0	0	0	1	1	4	$4T_s$
			•					•	•
			•					•	•
			•					•	•
1	1	1	1	1	1	1	1	256	$256T_s$

$T_s = (2048) \times \left(\frac{1}{f_{CLK}}\right)$ System Sample Period

$T_d = d_s \times T_s$ Derivative-term Sampling Interval

Port	Bytes	Command	Comments
c	1E	LFIL	This command initiates loading the filter coefficients input buffers.
		Busy-bit Check Module	
d	00	HB	These two bytes are the filter control word. A 00 hex HB sets the derivative sampling interval to $2048/f_{CLK}$ by setting d_s to one. A x8 hex LB indicates only k_p will be loaded. The other filter parameters will remain at zero, their reset default value.
d	x8	LB	
		Busy-bit Check Module	
d	00	HB	These two bytes set k_p
d	0A	LB	to ten.
		Busy-bit Check Module	
c	04	UDF	This command transfers new filter coefficients from input buffers to working registers. Until UDF is executed, coefficients loaded via the LFIL command do not affect the filter transfer characteristic.
		Busy-bit Check Module	

FIGURE 6. Filter Programming Module

Comments

After executing both the example initialization and example filter programming modules, the following observations are made. Filter gain is nonzero, but desired shaft position continues to track actual shaft position. Under these conditions, the motor drive signal remains at zero. The shaft should be stationary and "free wheeling". If there is significant drive amplifier offset, the shaft may rotate slowly, but with minimal torque capability.

Initially, k_p should be set below twenty, d_s should be set to one, and k_i, k_d, and i_l should remain at zero. These values will not provide optimum system performance, but they will be sufficient to test system functionality. See Tuning the PID Filter.

TRAJECTORY PROGRAMMING MODULE

Figure 7 details the example trajectory programming module.

Load Trajectory Parameters.

An LTRJ (Load TRaJectory) command sequence includes command LTRJ, a trajectory control word, and a variable number of data words.

The LTRJ command initiates loading trajectory parameters into input buffers.

The two data bytes, written immediately after LTRJ, comprise the trajectory control word. The first byte programs, with logical ones in respective bit positions, the trajectory mode (velocity or position), velocity mode direction, and stopping mode. See Stop Module. The second byte indicates, with logical ones in respective bit positions, which of the three trajectory parameters will be loaded. It also indicates whether the parameters are absolute or relative. See *Table V*. Any combination of the three parameters can be loaded within a single LTRJ command sequence.

Immediately following the trajectory control word, the trajectory parameters are written. Each parameter is written as a pair of data words (four data bytes). Because any combination of the three parameters can be loaded within a single LTRJ command sequence, the number of data words following the trajectory control word can vary in the range from zero to six.

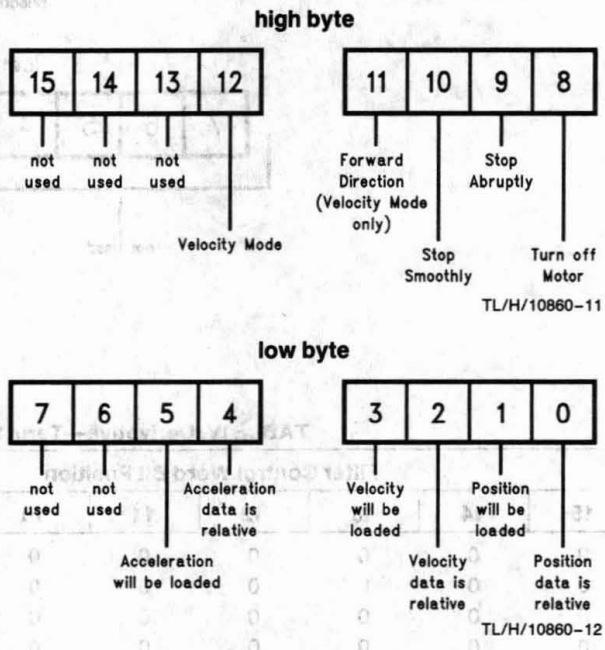
In the case of the example module, the first byte of the trajectory control word, 00 hex, programs the LM628 to operate in position mode. The second byte, 0A hex, indicates velocity and position will be loaded and both parameters are absolute. Four data words, two for each parameter loaded, follow the trajectory control word.

Start Motion Control

The start motion control command, STT (STarT), transfers new trajectory parameters from input buffers to working registers and begins execution of the new trajectory. Until STT is executed, the new trajectory parameters do not affect shaft motion.

Note: At this point no actual trajectory parameters are loaded. Calculation of trajectory parameters and execution of example moves is left for a later section.

Table V. Trajectory Control Word Bit Allocation



Port	Bytes	Command	Comments
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
		Busy-bit Check Module	
d	00	HB	These two bytes are the trajectory control word. A 0A hex LB indicates velocity and position will be loaded and both parameters are absolute.
d	0A	LB	
		Busy-bit Check Module	
d	xx	HB	Velocity is loaded in two data words. These two bytes are the high data word.
d	xx	LB	
		Busy-bit Check Module	
d	xx	HB	velocity data word (low)
d	xx	LB	
		Busy-bit Check Module	
d	xx	HB	Position is loaded in two data words. These two bytes are the high data word.
d	xx	LB	
		Busy-bit Check Module	
d	xx	HB	position data word (low)
d	xx	LB	
		Busy-bit Check Module	
c	01	STT	STT must be issued to execute the desired trajectory.
		Busy-bit Check Module	

FIGURE 7. Trajectory Programming Module

STOP MODULE

This module demonstrates the programming flow required to stop shaft motion.

While the LM628 operates in position mode, normal stopping is always smooth and occurs automatically at the end of a specified trajectory (i.e. no stop module is required). Under exceptional conditions, however, a stop module can be used to affect a premature stop.

While the LM628 operates in velocity mode, stopping is always accomplished via a stop module.

The example stop module, shown in *Figure 8*, utilizes an LTRJ command sequence and an STT command.

Load Trajectory Parameters

Bits eight through ten of the trajectory control word select the stopping mode. See *Table V*.

In the case of the example module, the first byte of the trajectory control word, x1 hex, selects motor-off as the desired stopping mode. This mode stops shaft motion by setting the motor drive signal to zero (the appropriate offset-binary code to apply zero drive to the motor).

Setting bit nine of the trajectory control word selects stop abruptly as the desired stopping mode. This mode stops shaft motion (at maximum deceleration) by setting the target position equal to the current position.

Setting bit ten of the trajectory control word selects stop smoothly as the desired stopping mode. This mode stops shaft motion by decelerating at the current user-programmed acceleration rate.

Note: Bits eight through ten of the trajectory control word must be used exclusively; only one of them should be logic one at any time.

Start Motion Control

The start motion control command, STT, must be executed to stop shaft motion.

Comments

After shaft motion is stopped with either an "abrupt" or a "smooth" stop module, the control system will attempt to hold the shaft at its current position. If forced away from this desired resting position and released, the shaft will move back to the desired position. Unless new trajectory parameters are loaded, execution of another STT command will restart the specified move.

After shaft motion is stopped with a "'motor-off" stop module, desired shaft position tracks actual shaft position. Consequently, the motor drive signal remains at zero and the control system can not affect shaft position; the shaft should be stationary and free wheeling. If there is significant drive amplifier offset, the shaft may rotate slowly, but with minimal torque capability. Unless new trajectory parameters are loaded, execution of another STT command will restart the specified move.

Port	Bytes	Command	Comments
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
		Busy-bit Check Module	
d	x1	HB	These two bytes are the trajectory control word. A x1 hex HB selects motor-off as the desired stopping mode. A 00 hex LB indicates no trajectory parameters will be loaded.
d	00	LB	
		Busy-bit Check Module	
c	01	STT	The start motion control command, STT, must be executed to stop shaft motion.
		Busy-bit Check Module	

FIGURE 8. Stop Module (Motor-Off)

II. PROGRAMS

This section focuses on the development of four brief LM628 programs.

LOOP PHASING PROGRAM

Following initial power-up, the correct polarity of the motor drive signal must be determined. If the polarity is incorrect (loop inversion), the drive signal will push the shaft away

from its desired position rather than towards it. This results in "motor runaway", a condition characterized by the motor running continuously at high speed.

The loop phasing program, detailed in *Figure 9*, contains both the example initialization and filter programming modules. It also contains an LTRJ command sequence and an STT command.

Note: Execution of this simple program is only required the *first* time a new system is used.

Load Trajectory Parameters

An LTRJ (Load TRaJectory) command sequence includes command LTRJ, a trajectory control word, and a variable number of data words.

In the case of the Loop Phasing Program, the first byte of the trajectory control word, 00 hex, programs the LM628 to operate in position mode. The second byte, 00 hex, indicates no trajectory parameters will be loaded (i.e. in this program, zero data words follow the trajectory control word). The three trajectory parameters will remain at zero, their reset value.

Start Motion Control

The start motion control command, STT (STarT), transfers new trajectory parameters from input buffers to working registers and begins execution of the new trajectory. Until STT is executed, the new trajectory parameters do not affect shaft motion.

Port	Bytes	Command	Comments
		Initialization Module	
		Filter Programming Module	
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
		Busy-bit Check Module	
d	00	HB	These two bytes are the trajectory control word. A 00 hex LB indicates no trajectory parameters will be loaded.
d	00	LB	
		Busy-bit Check Module	
c	01	STT	STT must be issued to execute the desired trajectory.

FIGURE 9. Loop Phasing Program

Comments

Execution of command STT results in execution of the desired trajectory. With the acceleration set at zero, the profile generator generates a desired shaft position that is both constant and equal to the current absolute position. See *Figure 5*. Under these conditions, the control system will attempt to hold the shaft at its current absolute postion. The shaft will feel lightly "spring loaded". If forced (CAREFULLY) away from its desired position and released, the shaft will spring back to the desired position.

If the polarity of the motor drive signal is incorrect (loop inversion), motor runaway will occur immediately after execution of command STT, or after the shaft is forced (CAREFULLY) from its resting position.

Loop inversion can be corrected with one of three methods: interchanging the shaft position encoder signals (channel A and channel B), interchanging the motor power leads, or inverting the motor command signal before application to the motor drive amplifier. For LM629 based systems, loop inversion can be corrected by interchanging the motor power leads, interchanging the shaft position encoder signals, or logically inverting the PWM sign signal.

SIMPLE ABSOLUTE POSITION MOVE

The Simple Absolute Position Move Program, detailed in *Figure 13*, utilizes both the initialization and filter programming modules, as well as, an LTRJ command sequence and an STT command.

Factors that influenced the development of this program included the following: the program must demonstrate simple trajectory parameters calculations, the program must demonstrate the programming flow required to load and execute an absolute position move, and correct completion of the move must be verifiable through simple observation.

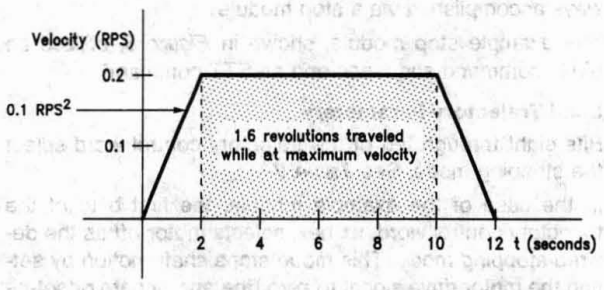
Move: The shaft will accelerate at 0.1 rev/sec^2 until it reaches a maximum velocity of 0.2 rev/sec, and then decelerate to a stop exactly two revolutions from the starting position. See *Figure 10*.

Note: Absolute position is position measured relative to zero (home). An absolute position move is a move that ends at a specified absolute position. For example, independent of the current absolute position of the shaft, if an absolute position of 30,000 counts is specified, upon completion of the move the absolute position of the shaft will be 30,000 counts (i.e. 30,000 counts relative to zero). The example program calls for a position move of two revolutions. Because the starting absolute position is 0 counts, the move is accomplished by specifying an absolute position of 8000 counts. See *Figure 13*.

The Quadrature Incremental Encoder

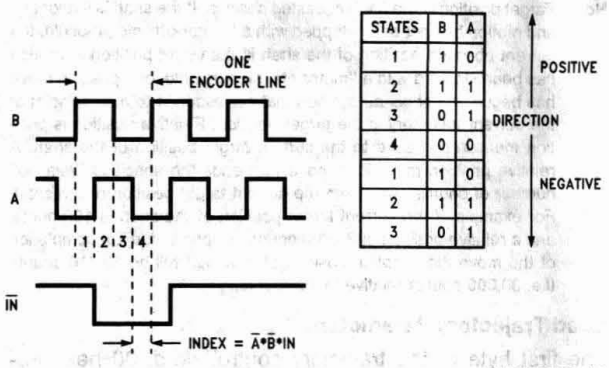
As a supplement to the trajectory parameters calculations, a brief discussion is provided here to differentiate between encoder ***lines*** and encoder ***counts***.

A quadrature incremental shaft encoder encodes shaft rotation as electrical pulses. *Figure 11* details the signals generated by a 3-channel quadrature incremental encoder. The LM628 decodes (or "counts") a quadrature incremental signal to determine the absolute position of the shaft.



TL/H/10860–13

FIGURE 10. Velocity Profile for Simple Absolute Position Move Program



TL/H/10860–14

FIGURE 11. 3-Channel Quadrature Encoder Signals

The resolution of a quadrature incremental encoder is usually specified as a number of ***lines***. This number indicates the number of cycles of the output signals for each complete shaft revolution. For example, an N-line encoder generates N cycles of its output signals during each complete shaft revolution.

By definition, two signals that are in quadrature are 90° out of phase. When considered together, channels A and B *(Figure 11)* traverse four distinct digital states during each full cycle of either channel. Each state transition represents one ***count*** of shaft motion. The leading channel indicates the direction of shaft rotation.

Each line, therefore, represents one cycle of the output signals, and each cycle represents four encoder counts.

$$\left(N\frac{\text{CYCLES}}{\text{REVOLUTION}}\right)\times\left(4\frac{\text{COUNTS}}{\text{CYCLE}}\right)=4N\frac{\text{COUNTS}}{\text{REVOLUTION}}$$

The reference system uses a one thousand line encoder.

$$\left(1000\frac{\text{CYCLES}}{\text{REVOLUTION}}\right)\times\left(4\frac{\text{COUNTS}}{\text{CYCLE}}\right)=4000\frac{\text{COUNTS}}{\text{REVOLUTION}}$$

Sample Period

Sampling of actual shaft position occurs at a fixed frequency, the reciprocal of which is the system sample period. The system sample period is the unit of time upon which shaft acceleration and velocity are based.

$$T_S=(2048)\times\left(\frac{1}{f_{CLOCK}}\right)\ \text{System Sample Period}$$

The reference system uses an 8 MHz clock. The sample period of the reference system follows directly from the definition.

$$T_S=(2048)\times\left(\frac{1}{8\times10^6\ \text{Hz}}\right)=256\times10^{-6}\frac{\text{SECONDS}}{\text{SAMPLE}}$$

Trajectory Parameters Calculations

The shaft will accelerate at 0.1 rev/sec^2 until it reaches a maximum velocity of 0.2 rev/sec, and then decelerate to a stop exactly two revolutions from the starting position.

Trajectory parameters calculations for this move are detailed in *Figure 12*.

Comments

After completing the move, the control system will attempt to hold the shaft at its current absolute position. The shaft will feel lightly "spring loaded". If forced away from its desired resting position and released, the shaft will move back to the desired position.

$$A=\left(4000\frac{\text{COUNTS}}{\text{REVOLUTION}}\right)\times\left(256\times10^{-6}\frac{\text{SECONDS}}{\text{SAMPLE}}\right)^2\times\left(0.1\frac{\text{REVOLUTIONS}}{\text{SECOND}^2}\right)=2.62\times10^{-5}\frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

$$A=\left(2.62\times10^{-5}\frac{\text{COUNTS}}{\text{SAMPLE}^2}\right)\times(65{,}536)=1.718\frac{\text{COUNTS}}{\text{SAMPLE}^2}\qquad\text{Acceleration Scaled}$$

$$A=2\frac{\text{COUNTS}}{\text{SAMPLE}^2}\qquad\text{Acceleration Rounded}$$

$$A=00\ 00\ 00\ 02\ \text{hex}\frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

$$V=\left(4000\frac{\text{COUNTS}}{\text{REVOLUTION}}\right)\times\left(256\times10^{-6}\frac{\text{SECONDS}}{\text{SAMPLE}}\right)\times\left(0.2\frac{\text{REVOLUTIONS}}{\text{SECOND}}\right)=0.2048\frac{\text{COUNTS}}{\text{SAMPLE}}$$

$$V=\left(0.2048\frac{\text{COUNTS}}{\text{SAMPLE}}\right)\times(65{,}536)=13{,}421.77\frac{\text{COUNTS}}{\text{SAMPLE}}\qquad\text{Velocity Scaled}$$

$$V=13{,}422\frac{\text{COUNTS}}{\text{SAMPLE}}\qquad\text{Velocity Rounded}$$

$$V=00\ 00\ 34\ 6E\ \text{hex}\frac{\text{COUNTS}}{\text{SAMPLE}}$$

$$P=\left(4000\frac{\text{COUNTS}}{\text{REVOLUTION}}\right)\times(2.0\ \text{REVOLUTIONS})=8000\ \text{COUNTS}$$

$$P=00\ 00\ 1F\ 40\ \text{hex COUNTS}$$

FIGURE 12. Calculations of Trajectory Parameters for Simple Absolute Position Move

Port	Bytes	Command	Comments
		Initialization Module	
		Filter Programming Module	
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers
		Busy-bit Check Module	
d	00	HB	These two bytes are the trajectory control word. A 2A hex LB indicates acceleration, velocity, and position will be loaded and all three parameters are absolute.
d	2A	LB	
		Busy-bit Check Module	
d	00	HB	Acceleration is loaded in two data words. These two bytes are the high data word. In this case, the acceleration is 0.1 rev/sec^2.
d	00	LB	
		Busy-bit Check Module	
d	00	HB	acceleration data word (low)
d	02	LB	
		Busy-bit Check Module	
d	00	HB	velocity is loaded in two data words. These two bytes are the high data word. In this case, the velocity is 0.2 rev/sec.
d	00	LB	
		Busy-bit Check Module	
d	34	HB	velocity data word (low)
d	6E	LB	
		Busy-bit Check Module	
d	00	HB	Position is loaded in two data words. These two bytes are the high data word. In this case, the position loaded is eight thousand counts. This results in a move of two revolutions in the forward direction.
d	00	LB	
		Busy-bit Check Module	
d	1F	HB	position data word (low)
d	40	LB	
		Busy-bit Check Module	
c	01	STT	STT must be issued to execute the desired trajectory.

FIGURE 13. Simple Absolute Position Move Program

SIMPLE RELATIVE POSITION MOVE

This program demonstrates the programming flow required to load and execute a relative position move. See *Figure 14*.

Move: Independent of the current resting position of the shaft, the shaft will complete thirty revolutions in the reverse direction. Total time to complete the move is fifteen seconds. Total time for acceleration and deceleration is five seconds.

Note: Target position is the final requested position. If the shaft is stationary, and motion has not been stopped with a "motor-off" stop module, the current absolute position of the shaft is the target position. If motion has been stopped with a "motor-off" stop module, or a position move has begun, the absolute position that corresponds to the endpoint of the current trajectory is the target position. Relative position is position measured relative to the current target position of the shaft. A relative position move is a move that ends the specified "relative" number of counts away from the current target position of the shaft. For example, if the current target position of the shaft is 10 counts, and a relative position of 30,000 counts is specified, upon completion of the move the absolute position of the shaft will be 30,010 counts (i.e. 30,000 counts relative to 10 counts).

Load Trajectory Parameters

The first byte of the trajectory control word, 00 hex, programs position mode operation. The second byte, 2B hex, indicates all three trajectory parameters will be loaded. It also indicates both acceleration and velocity will be absolute values while position will be a relative value.

Trajectory Parameters Calculations

Independent of the current resting position of the shaft, the shaft will complete thirty revolutions in the reverse direction. Total time to complete the move is fifteen seconds. Total time for acceleration and deceleration is five seconds.

The reference system utilizes a one thousand line encoder. The number of counts for each complete shaft revolution and the total counts for this position move are determined.

$$\left(1000\,\frac{\text{CYCLES}}{\text{REVOLUTION}}\right)\times\left(4\,\frac{\text{COUNTS}}{\text{CYCLE}}\right)=4000\,\frac{\text{COUNTS}}{\text{REVOLUTION}}$$

$$\left(4000\,\frac{\text{COUNTS}}{\text{REVOLUTION}}\right)\times(30\ \text{REVOLUTIONS})=120{,}000\ \text{COUNTS}$$

With respect to time, two-thirds of the move is made at maximum velocity and one-third is made at a velocity equal to one-half the maximum velocity.† Therefore, total counts traveled during acceleration and deceleration periods is one-fifth the total counts traveled. See *Figure 15*.

$$\frac{120{,}000\ \text{COUNTS}}{5}=24{,}000\ \text{COUNTS}\quad\text{total counts traveled during acceleration and deceleration}$$

$$\frac{24{,}000\ \text{COUNTS}}{2}=12{,}000\ \text{COUNTS}\quad\text{counts traveled during acceleration}$$

The reference system uses an 8 MHz clock. The sample period of the reference system is determined.

$$T_S=(2048)\times\left(\frac{1}{8\times10^6\text{Hz}}\right)=256\times10^{-6}\,\frac{\text{SECONDS}}{\text{SAMPLE}}$$

The number of samples during acceleration (and deceleration) is determined.

$$\frac{2.5\ \text{SECONDS}}{256\times10^{-6}\,\frac{\text{SECONDS}}{\text{SAMPLE}}}=9766\ \text{SAMPLES}\quad\text{number of samples during acceleration}$$

Using the number of counts traveled during acceleration and the number of samples during acceleration, acceleration is determined.

$$s=\frac{at^2}{2}\quad\text{distance traveled during time t at acceleration a}$$

$$a=\frac{2s}{t^2}=\frac{(2)\times(12{,}000\ \text{COUNTS})}{(9766\ \text{SAMPLES})^2}=0.000252\,\frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

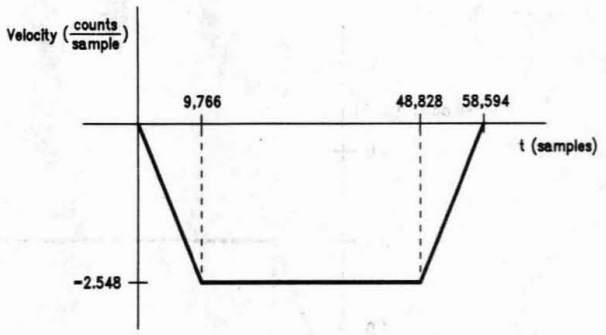
Total counts traveled while at maximum velocity is four-fifths the total counts traveled.

$$\frac{(4)\times(120{,}000\ \text{COUNTS})}{5}=96{,}000\ \text{COUNTS}$$

†Average velocity during acceleration and deceleration periods is one-half the maximum velocity.

Port	Bytes	Command	Comments
		Initialization Module	
		Filter Programming Module	
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
		Busy-bit Check Module	
d	00	HB	These two bytes are the trajectory control word. A 2B hex LB indicates all three parameters will be loaded and both acceleration and velocity will be absolute values while position will be a relative value.
d	2B	LB	
		Busy-bit Check Module	
d	00	HB	Acceleration is loaded in two data words. These two bytes are the high data word. In this case, the acceleration is 17 counts/sample^2.
d	00	LB	
		Busy-bit Check Module	
d	00	HB	acceleration data word (low)
d	11	LB	
		Busy-bit Check Module	
d	00	HB	Velocity is loaded in two data words. These two bytes are the high data word. In this case, velocity is 161,087 counts/sample.
d	02	LB	
		Busy-bit Check Module	
d	75	HB	velocity data word (low)
d	3F	LB	
		Busy-bit Check Module	
d	FF	HB	Position is loaded in two data words. These two bytes are the high data word. In this case, the position loaded is −120,000 counts. This results in a move of thirty revolutions in the reverse direction.
d	FE	LB	
		Busy-bit Check Module	
d	2B	HB	position data word (low)
d	40	LB	
		Busy-bit Check Module	
c	01	STT	STT must be issued to execute the desired trajectory.

FIGURE 14. Simple Relative Position Move Program



TL/H/10860–15

FIGURE 15. Velocity Profile for Simple Relative Position Move Program

The number of samples while at maximum velocity is determined.

$$\frac{10 \text{ SECONDS}}{256 \times 10^{-6} \frac{\text{SECONDS}}{\text{SAMPLE}}} = 39{,}062 \text{ SAMPLES}$$ number of samples while at maximum velocity

Using the total counts traveled while at maximum velocity and the number of samples while at maximum velocity, velocity is determined.

$$\frac{96{,}000 \text{ COUNTS}}{39{,}062 \text{ SAMPLES}} = 2.458 \frac{\text{COUNTS}}{\text{SAMPLE}}$$

Both acceleration and velocity values are scaled.

$$\left(0.000252 \frac{\text{COUNTS}}{\text{SAMPLE}^2}\right) \times (65{,}536) = 16.515 \frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

$$\left(2.458 \frac{\text{COUNTS}}{\text{SAMPLE}}\right) \times (65{,}536) = 161{,}087.488 \frac{\text{COUNTS}}{\text{SAMPLE}}$$

Acceleration and velocity are rounded to the nearest integer and all three trajectory parameters are converted to hexadecimal.

$$A = 17 = 00\ 00\ 00\ 11 \text{ hex} \frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

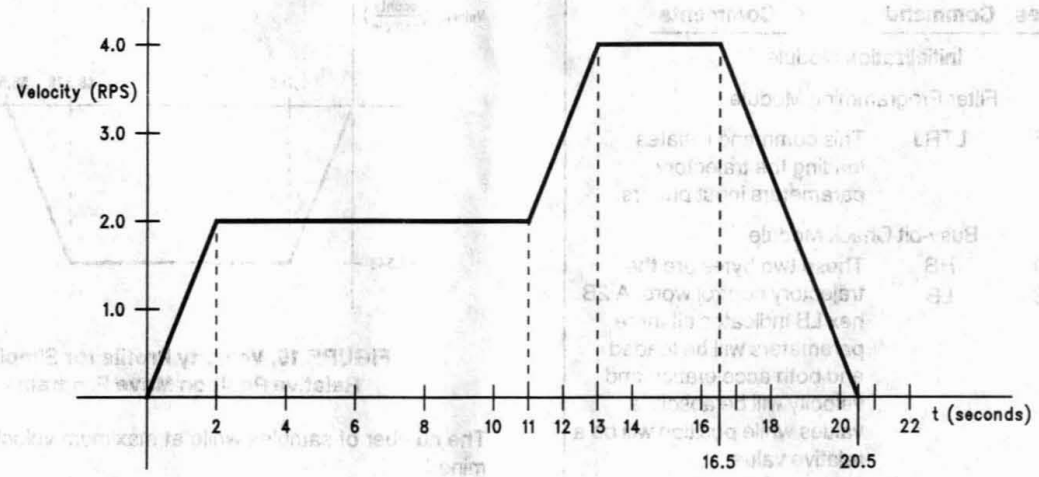
$$V = 161{,}087 = 00\ 02\ 75\ 3F \text{ hex} \frac{\text{COUNTS}}{\text{SAMPLE}}$$

$$P = -120{,}000 = \text{FF FE 2B 40 hex COUNTS}$$

BASIC VELOCITY MODE MOVE WITH BREAKPOINTS

This program demonstrates basic velocity mode programming and the (typical) programming flow required to set both absolute and relative breakpoints. See *Figure 17*.

Move: The shaft will accelerate at 1.0 rev/sec^2 until it reaches a maximum velocity of 2.0 rev/sec. After completing twenty forward direction revolutions (including revolutions during acceleration), the shaft will accelerate at 1.0 rev/sec^2 until it reaches a maximum velocity of 4.0 rev/sec. After completing twenty forward direction revolutions (including revolutions during acceleration), the shaft will decelerate (at 1.0 rev/sec^2) to a stop. See *Figure 16*.



TL/H/10860–16

FIGURE 16. Velocity Profile for Basic Velocity Mode with Breakpoints Program

Mask Interrupts

An MSKI command sequence allows the user to determine which interrupt conditions result in host interrupts; interrupting the host via the host interrupt output (pin 17). It contains an MSKI command and one data word.

The MSKI command initiates interrupt masking.

Immediately following the MSKI command, a single data word is written. The first byte is not used. Bits one through six of the second byte determine the masked/unmasked status of each interrupt. See *Table II*. Any zeros in this 6-bit field mask (disable) the corresponding interrupts while any ones unmask (enable) the corresponding interrupts.

In the case of the examlple program, the second byte of the MSKI data word, 40 hex, enables the breakpoint interrupt. All other interrupts are disabled (masked).

When interrupted, the host processor can read the Status Byte to determine which interrupt condition(s) occurred. See *Table I*.

Note: Command MSKI controls only the host interrupt process. Bits one through six of the Status Byte reflect actual conditions independent of the masked/unmasked status of individual interrupts. This feature allows interrupts to be serviced with a polling scheme.

Set Breakpoints (Absolute and Relative)

An SBPA command sequence enables the user to set breakpoints in terms of absolute shaft position. An SBPR command sequence enables setting breakpoints relative to the current target position. When a breakpoint position is reached, bit six of the status byte, the breakpoint interrupt flag, is set to logic high. If this interrupt is enabled (unmasked), the host will be interrupted via the host interrupt output (pin 17).

An SBPA (or SBPR) command initiates loading/setting a breakpoint. The two data words, written immediately following the SBPA (or SBPR) command, represent the breakpoint position.

The example program contains a relative breakpoint set at 80,000 counts relative to position zero (the current target position). This represents a move of twenty forward direction revolutions. When this position is reached, the LM628 interrupts the host processor, and the host executes a sequence of commands that increases the maximum velocity, resets the breakpoint interrupt flag, and loads an absolute breakpoint.

The example program contains an absolute breakpoint set at 160,000 counts. When this absolute position is reached, the LM628 interrupts the host processor, and the host executes a Smooth Stop Module.

Breakpoint positions for this example program are determined.

$$\left(4000\,\frac{\text{COUNTS}}{\text{REVOLUTION}}\right) \times (20\ \text{REVOLUTIONS})$$

$$= 80{,}000\ \text{COUNTS} \quad \text{relative breakpoint}$$

$$\left(4000\,\frac{\text{COUNTS}}{\text{REVOLUTION}}\right) \times (40\ \text{REVOLUTIONS})$$

$$= 160{,}000\ \text{COUNTS} \quad \text{absolute breakpoint}$$

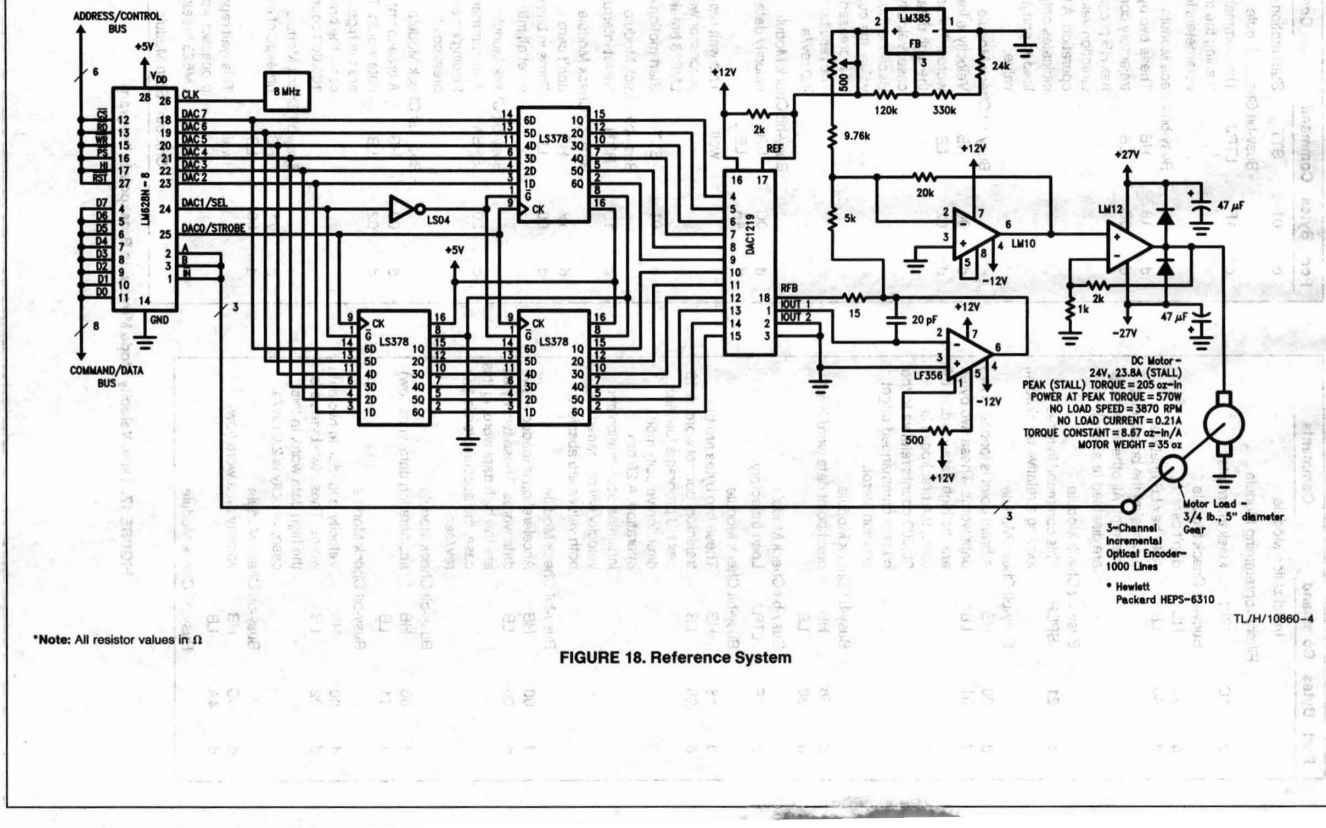
Load Trajectory Parameters

This example program contains two LTRJ command sequences. The trajectory control word of the first LTRJ command sequence, 1828 hex, programs forward direction velocity mode, and indicates an absolute acceleration and an absolute velocity will be loaded. The trajectory control word of the second LTRJ command sequence, 180C hex, programs forward direction velocity mode, and indicates a relative velocity will be loaded. See *Table V*.

Trajectory parameters calculations follow the same format as those detailed for the simple absolute position move. See *Figure 12*.

Port	Bytes	Command	Comments
		Initialization Module	
		Filter Programming Module	
c	1C	MSKI	Mask interrupts.
		Busy-bit Check Module	
d	xx	HB	don't care
d	40	LB	A 40 hex LB enables (unmasks) the breakpoint interrupt. All other interrupts are disabled (masked).
		Busy-bit Check Module	
c	21	SPBR	This command initiates loading a relative breakpoint.
		Busy-bit Check Module	
d	00	HB	A breakpoint is loaded in two
d	01	LB	data words. These two bytes are the high data word. In this case, the breakpoint is 80,000 counts relative to the current commanded target position (zero).
		Busy-bit Check Module	
d	38	HB	breakpoint data word (low)
d	80	LB	
		Busy-bit Check Module	
c	1F	LTRJ	Load trajectory.
		Busy-bit Check Module	
d	18	HB	These two bytes are the
d	28	LB	trajectory control word. A 18 hex HB programs forward direction velocity mode operation. A 28 hex LB indicates acceleration and velocity will be loaded and both values are absolute.
		Busy-bit Check Module	
d	00	HB	Acceleration is loaded in two
d	00	LB	data words. These two bytes are the high data word. In this case, the acceleration is 1.0 rev/sec^2.
		Busy-bit Check Module	
d	00	HB	acceleration data word (low)
d	11	LB	
		Busy-bit Check Module	
d	00	HB	Velocity is loaded in two data
d	02	LB	words. These two bytes are the high data word. In this case, velocity is 2.0 rev/s.
		Busy-bit Check Module	
d	0C	HB	velocity data word (low)
d	4A	LB	
		Busy-bit Check Module	
c	01	STT	Start motion control.
		Busy-bit Check Module	
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
		Busy-bit Check Module	
d	18	HB	These two bytes are the
d	0C	LB	trajectory control word. A 18 hex HB programs forward direction velocity mode operation. A 0C hex LB indicates only velocity will be loaded and it will be a relative value.
		Busy-bit Check Module	
d	00	HB	Velocity is loaded in two data
d	02	LB	words. These two bytes are the high data word. In this case, velocity is 2.0 rev/s. Because this is a relative value, the current velocity will be increased by 2.0 rev/s. The resultant velocity will be 4.0 rev/s.
		Busy-bit Check Module	
d	0C	HB	velocity data word (low)
d	4A	LB	
		wait	This wait represents the host processor waiting for an LM628 breakpoint interrupt.
c	01	STT	Start motion control.
		Busy-bit Check Module	
c	1D	RSTI	Reset interrupts.
		Busy-bit Check Module	
d	xx	HB	don't care
d	00	LB	Zeros in bits one through six reset **all** interrupts.
		Busy-bit Check Module	
c	20	SPBA	This command initiates loading an absolute breakpoint.
		Busy-bit Check Module	
d	00	HB	A breakpoint is loaded in two
d	02	LB	data words. These two bytes are the high data word. In this case, the breakpoint is 160,000 counts absolute.
		Busy-bit Check Module	
d	71	HB	breakpoint data word (low)
d	00	LB	
		wait	This wait represents the host processor waiting for an LM628 breakpoint interrupt.
		"Smooth" Stop Module	

FIGURE 17. Basic Velocity Mode Move with Breakpoints Program



TL/H/10860–4

*Note: All resistor values in Ω

FIGURE 18. Reference System

III. TUNING THE PID FILTER

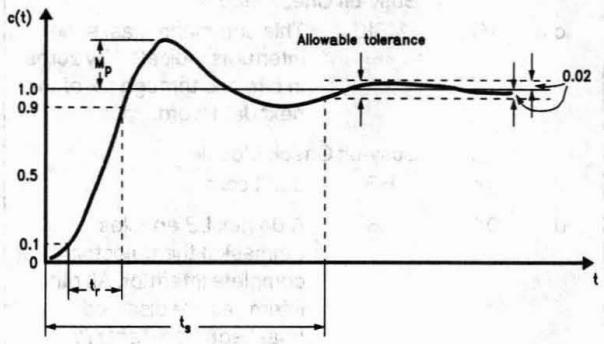
BACKGROUND

The transient response of a control system reveals important information about the "quality" of control, and because a step input is easy to generate and sufficiently drastic, the transient response of a control system is often characterized by the response to a step input, the system step response.

In turn, the step response of a control system can be characterized by three attributes: maximum overshoot, rise time, and settling time. These step response attributes are defined in what follows and detailed graphically in *Figure 19*.

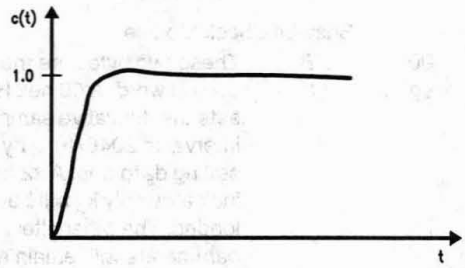
1. The maximum overshoot, Mp, is the maximum peak value of the response curve measured from unity. The amount of maximum overshoot directly indicates the relative stability of the system.
2. The rise time, t_r, is the time required for the response to rise from ten to ninety percent of the final value.
3. The settling time, t_s, is the time required for the response to reach and stay within two percent of the final value.

A critically damped control system provides optimum performance. The step response of a critically damped control system exhibits the minimum possible rise time that maintains zero overshoot and zero ringing (damped oscillations). *Figure 20* illustrates the step response of a critically damped control system.



TL/H/10860–17

FIGURE 19. Unit Step Response Curve Showing Transient Response Attributes



TL/H/10860–18

FIGURE 20. Unit Step Response of a Critically Damped System

INTRODUCTION

The LM628 is a digital PID controller. The loop-compensation filter of a PID controller is usually tuned experimentally, especially if the system dynamics are not well known or defined.

The ultimate goal of tuning the PID filter is to critically damp the motor control system—provide optimum tracking and settling time.

As shown in *Figure 5*, the response of the PID filter is the sum of three terms, a proportional term, an integral term, and a derivative term. Five variables shape this response. These five variables include the three gain coefficients (k_p, k_i, and k_d), the integration limit coefficient (i_l), and the derivative sampling coefficient (d_s). *Tuning the filter equates to determining values for these variable coefficients, values that critically damp the control system.*

Filter coefficients are best determined with a two-step experimental approach. In the first step, the values of k_p, k_i, and k_d (along with i_l and d_s) are systematically varied until reasonably good response characteristics are obtained. Manual and visual methods are used to evaluate the effect of each coefficient on system behavior. In the second step, an oscilloscope trace of the system step response provides detailed information on system damping, and the filter coefficients, determined in step one, are modified to critically damp the system.

Note: In step one, adjustments to filter coefficient values are inherently coarse, while in step two, adjustments are inherently fine. Due to this coarse/fine nature, steps one and two complement each other, and the two-step approach is presented as the "best" tuning method. The PID filter can be tuned with either step one or step two alone.

STEP ONE—MANUAL VISUAL METHOD

Introduction

In the first step, the values of k_p, k_i, and k_d (along with i_l and d_s) are systematically varied until reasonably good response characteristics are obtained. Manual and visual methods are used to evaluate the effect of each coefficient on system behavior.

Note: The next four numbered sections are ordered steps to tuning the PID filter.

1. Prepare the System

The initialization section of the filter tuning program is executed to prepare the system for filter tuning. See *Figure 22*. This section initializes the system, presets the filter parameters (k_p, k_i, il = 0, k_d = 2, d_s = 1), and commands the control loop to hold the shaft at the current position.

After executing the initialization section of the filter tuning program, both desired and actual shaft positions equal zero; the shaft should be stationary. Any displacement of the shaft constitutes a position error, but with both k_p and k_i set to zero, the control loop can not correct this error.

2. Determine the Derivative Gain Coefficient

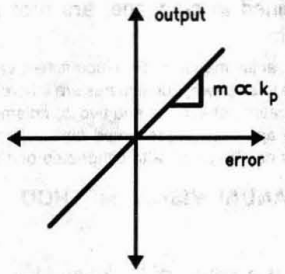
The filter derivative term provides damping to eliminate oscillation and minimize overshoot and ringing, stabilize the system. Damping is provided as a force proportional to the rate of change of position error, and the constant of proportionality is $k_d \times d_s$. See *Figure 21*.

Coefficients k_d and d_s are determined with an iterative process. Coefficient k_d is systematically increased until the shaft begins high frequency oscillations. Coefficient d_s is then increased by one. The entire process is repeated until d_s reaches a value appropriate for the system.

The system sample period sets the time interval between updates of position error. The derivative sampling interval is an integer multiple of the system sample period. See *Table IV*. It sets the time interval between successive position error samples used in the derivative term, and, therefore, directly affects system damping. The derivative sampling interval should be five to ten times smaller than the system mechanical time constant — this means many systems will require low d_s. In general, however, k_d and d_s should be set to give the largest $k_d \times d_s$ product that maintains acceptably low motor vibrations.

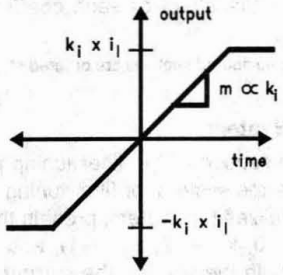
Note: Starting k_d at two and doubling it is a good method of increasing k_d. Manually turning the shaft reveals that with each increase of k_d, the resistance of the shaft to turning increases. The shaft feels increasingly sluggish and, because k_d provides a force proportional to the rate of change of position error, the faster the shaft is turned the more sluggish it feels. For the reference system, the final values of k_d and d_s are 4000 and 4 respectively.

Proportional Term



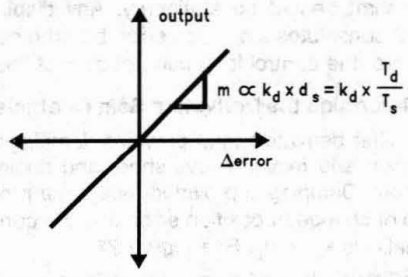
TL/H/10860–19

Integral Term



TL/H/10860–20

Derivative Term



TL/H/10860–21

FIGURE 21. Proportional, Integral, and Derivative (PID) Force Components

Port	Bytes	Command	Comments
c	00	RESET	See Initialization Module Text
		wait	The maximum time to complete RESET tasks is 1.5 ms.
c	06	PORT12	The RESET default size of the DAC port is eight bits. This command initializes the DAC port for a 12-bit DAC. It should not be issued in systems with an 8-bit DAC.
		Busy-bit Check Module	
c	1D	RSTI	This command resets **only** the interrupts indicated by zeros in bits one through six of the next data word. It also resets bit fifteen of the Signals Register and the host interrupt pin (pin 17).
		Busy-bit Check Module	
d	xx	HB	don't care
d	00	LB	Zeros in bits one through six indicate **all** interrupts will be reset.
		Busy-bit Check Module	
c	1C	MSKI	This command masks the interrupts indicated by zeros in bits one through six of the next data word.
		Busy-bit Check Module	
d	xx	HB	don't care
d	04	LB	A 04 hex LB enables (unmasks) the trajectory complete interrupt. All other interrupts are disabled (masked). See *Table II*.
		Busy-bit Check Module	
c	1E	LFIL	This command initiates loading the filter coefficients input buffers.
		Busy-bit Check Module	
d	00	HB	These two bytes are the filter
d	x2	LB	control word. A 00 hex HB sets the derivative sampling interval to $2048/f_{CLK}$ by setting d_s to one. A x2 hex LB indicates only k_d will be loaded. The other filter parameters will remain at zero, their reset default value.
		Busy-bit Check Module	
d	00	HB	These two bytes set k_d to
d	02	LB	two.
		Busy-bit Check Module	

FIGURE 22. Initialization Section— Filter Tuning Program

(Continued on Next Page)

Port	Bytes	Command	Comments
c	04	UDF	This command transfers new filter coefficients from input buffers to working registers. Until UDF is executed, coefficients loaded via the LFIL command do not affect the filter transfer characteristic.
		Busy-bit Check Module	
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
		Busy-bit Check Module	
d	00	HB	These two bytes are the trajectory control word. A 00 hex LB indicates no trajectory parameters will be loaded.
d	00	LB	
		Busy-bit Check Module	
c	01	STT	STT must be issued to execute the desired trajectory.

FIGURE 22. Initialization Section—Filter Tuning Program (Continued)

3. Determine the Proportional Gain Coefficient

Inertial loading causes following (or tracking) error, position error associated with a moving shaft. External disturbances and torque loading cause displacement error, position error associated with a stationary shaft. The filter proportional term provides a restoring force to minimize these position errors. The restoring force is proportional to the position error and increases linearly as the position error increases. See *Figure 21.* The proportional gain coefficient, k_p, is the constant of proportionality.

Coefficient k_p is determined with an iterative process—the value of k_p is increased, and the system damping is evaluated. This is repeated until the system is critically damped.

System damping is evaluated manually. Manually turning the shaft reveals each increase of k_p increases the shaft "stiffness". The shaft feels spring loaded, and if forced away from its desired holding position and released, the shaft "springs" back. If k_p is too low, the system is over damped, and the shaft recovers too slowly. If k_p is too large, the system is under damped, and the shaft recovers too quickly. This causes overshoot, ringing, and possibly oscillation. The proportional gain coefficient, k_p, is increased to the largest value that does not cause excessive overshoot or ringing. At this point the system is critically damped, and therefore provides optimum tracking and settling time.

Note: Starting k_p at two and doubling it at each iteration is a good method of increasing k_p. The final value of k_p for the reference system is 40.

4. Determine the Integral Gain Coefficient

The filter proportional term minimizes the errors due to inertial and torque loading. The integral term, however, provides a corrective force that can eliminate following error while the shaft is spinning and the deflection effects of a static torque load while the shaft is stationary. This corrective force is proportional to the position error and increases linearly with time. See *Figure 21.* The integral gain coefficient, k_i, is the constant of proportionality.

High values of k_i provide quick torque compensation, but increase overshoot and ringing. In general, k_i should be set to the smallest value that provides the appropriate compromise between three system characteristics: overshoot, settling time, and time to cancel the effects of a static torque load. In systems without significant static torque loading, a k_i of zero may be appropriate.

The corrective force provided by the integral term increases linearly with time. The integration limit coefficient, i_l, acts as a clamping value on this force to prevent integral wind-up, a backlash effect. As noted in *Figure 21*, i_l limits the summation of error (over time), not the product of k_i and this summation. In many systems i_l can be set to its maximum value, 7FFF hex, without any adverse effects. The integral term has no effect if i_l is set to zero.

For the test system, the final values of k_i and i_l are 5 and 1000 respectively.

STEP TWO—STEP RESPONSE METHOD

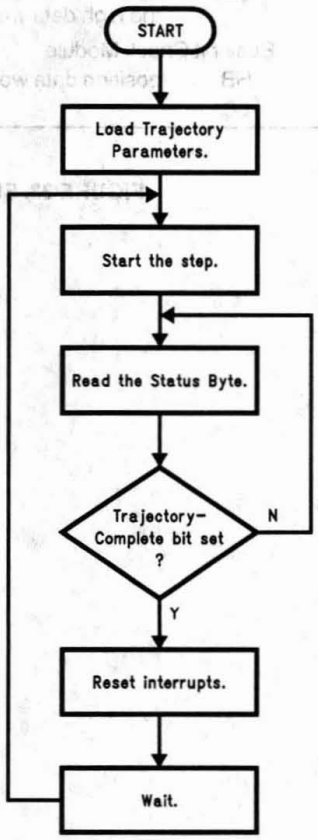
Introduction

The step response of a control system reveals important information about the "quality" of control—specifically, detailed information on system damping.

In the second step to tuning the PID filter, an oscilloscope trace of the control system step response is used to accurately evaluate system damping, and the filter coefficients, determined in step one, are fine tuned to critically damp the system.

Software Considerations

The step generation section of the filter tuning program provides the control loop with a repetitive small-signal step input. This is accomplished by repeatedly executing a small position move with high maximum velocity and high acceleration. See *Flow Diagram 3* and *Figure 23.*



TL/H/10860–22

Flow Diagram 3. Step Generation Section of Filter Tuning Program

Port	Bytes	Command	Comments
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
		Busy-bit Check Module	
d	00	HB	These two bytes are the
d	2B	LB	trajectory control word. A 2B hex LB indicates acceleration, velocity, and position will be loaded and both acceleration and velocity are absolute while position is relative.
		Busy-bit Check Module	
d	00	HB	Acceleration is loaded in two
d	04	LB	data words. These two bytes are the high data word.
		Busy-bit Check Module	
d	93	HB	acceleration data word (low)
d	E0	LB	
		Busy-bit Check Module	
d	00	HB	Velocity is loaded in two data
d	07	LB	words. These two bytes are the high data word.
		Busy-bit Check Module	
d	A1	HB	velocity data word (low)
d	20	LB	
		Busy-bit Check Module	
d	00	HB	Position is loaded in two data
d	00	LB	words. These two bytes are the high data word.
		Busy-bit Check Module	
d	00	HB	position data word (low)
d	C8	LB	

Port	Bytes	Command	Comments
		Busy-bit Check Module	
c	01	STT	STT must be issued to execute the desired trajectory.
		Busy-bit Check Module	
c	xx	RDSTAT	This command reads the Status Byte. It is directly supported by LM628 hardware and can be executed at any time by pulling $\overline{CS}$, $\overline{PS}$, and $\overline{RD}$ logic low. Status information remains valid as long as $\overline{RD}$ is logic low.
		decision	If the Trajectory Complete interrupt bit is set, continue. Otherwise loop back to RDSTAT.
c	1D	RSTI	This command resets **only** the interrupts indicated by zeros in bits one through six of the next data word. It also resets bit fifteen of the Signals Register and the host interrupt pin (pin 17).
d	xx	HB	don't care
d	00	LB	Zeros in bits one through six indicate **all** interrupts will be reset.
		wait	This wait block inserts a delay between repetitions of the step input. The delay is application specific, but a good range of values for the delay is 5 ms to 5000 ms.
		loop	Loop back to STT.

FIGURE 23. Step Generation Section—Filter Tuning Program

Hardware Considerations

For a motor control system, an oscilloscope trace of the system step response is a graph of the real position of the shaft versus time after a small and instantaneous change in desired position.

For an LM628-based system, no extra hardware is needed to view the system step response. During a step, the voltage across the motor represents the system step response, and an oscilloscope is used to generate a graph of this response (voltage).

For an LM629-based system, extra hardware is needed to view the system step response. *Figure 24* illustrates a circuit for this purpose. During a step, the voltage output of this circuit represents the system step response, and an oscilloscope is used to generate a graph of this response.

The oscilloscope trigger signal, a rectangular pulse train, is taken from the host interrupt output pin (pin 17) of the LM628/LM629. This signal is generated by the combination of a trajectory complete interrupt and a reset interrupts (RSTI) command. See *Flow Diagram 3*.

Note: The circuit of *Figure 24* can be used to view the step response of an LM628-based system.

Observations

What follows are example oscilloscope traces of the step response of the reference system.

Note 1: All traces were generated using the circuit of *Figure 24*.

Note 2: All traces were generated using the following "step" trajectory parameters: relative position, 200 counts; absolute velocity, 500,000 counts/sample; acceleration, 300,000 counts/sample/sample. These values generated a good small-signal step input for the reference system; other systems will require different trajectory parameters. In general, step trajectory parameters consist of a small relative position, a high velocity, and a high acceleration.

The position parameter must be relative. Otherwise, a define home command (DFH) must be added to the main loop of the step generation section—filter tuning program. See *Flow Diagram 3*.

The circuit for viewing the system step response uses an 8-bit analog-to-digital converter. See *Figure 24*. To prevent converter overflow, the step position parameter must not be set higher than 200 counts.

Note 3: The circuit of *Figure 24* produces an "inverted" step response graph. The oscilloscope input was inverted to produce a positive-going (more familiar) step response graph.

Figure 25 represents the step response of an under damped control system; this response exhibits excessive overshoot and long settling time. The filter parameters used to generate this response were as follows: k_p, 35; k_i, 5; k_d, 600; d_s, 4; i_l, 1000. *Figure 25* indicates the need to increase k_d, the derivative gain coefficient.

Figure 26 represents the step response of an over damped control system; this response exhibits excessive rise time which indicates a sluggish system. The filter parameters used to generate this response were as follows: k_p, 35; k_i, 5; k_d, 10,000; d_s, 7; i_l, 1000. *Figure 26* indicates the need to decrease k_d and d_s.

Figure 27 represents the step response of a critically damped control system; this response exhibits virtually zero overshoot and short rise time. The filter parameters used to generate this response were as follows: k_p, 40; k_i, 5; k_d, 4000; d_s, 4; i_l, 1000.

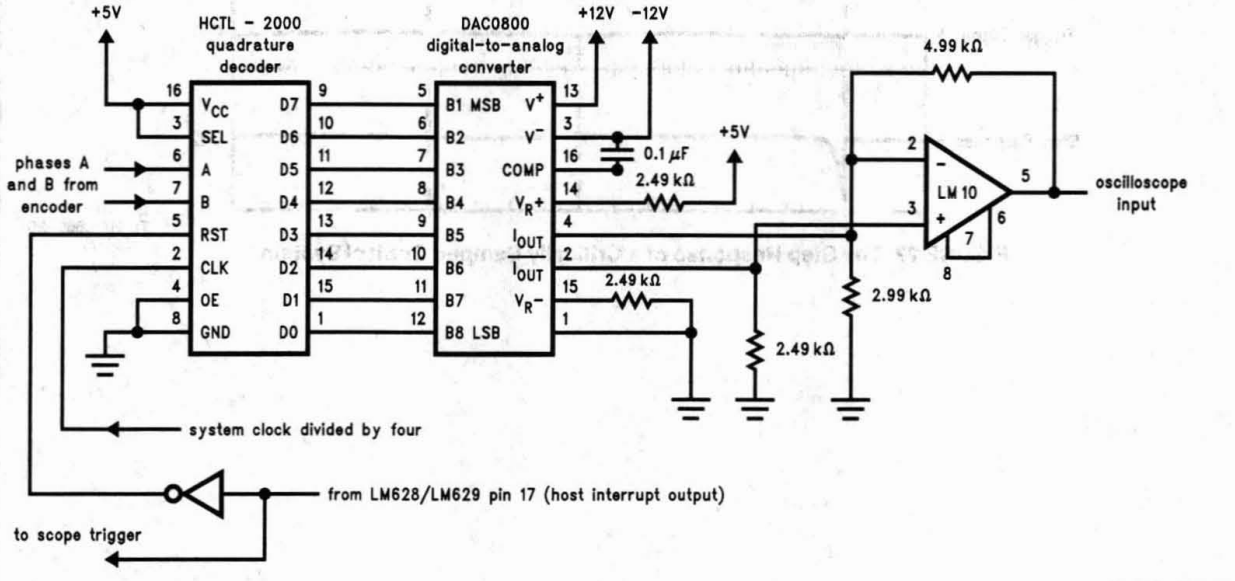


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FIGURE 24. Circuit for Viewing the System Step Response with an Oscilloscope

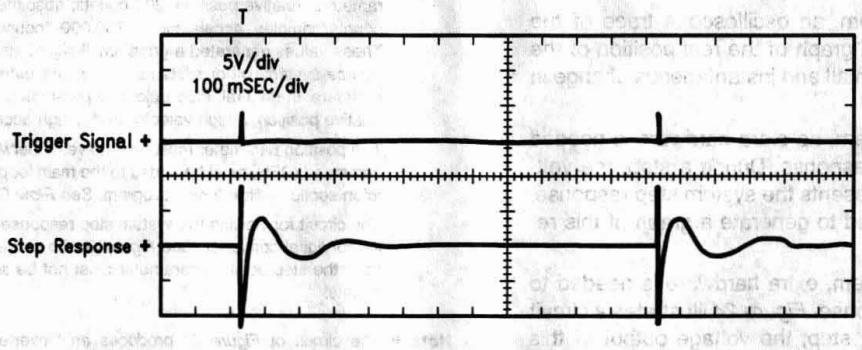

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FIGURE 25. The Step Response of an Under Damped Control System

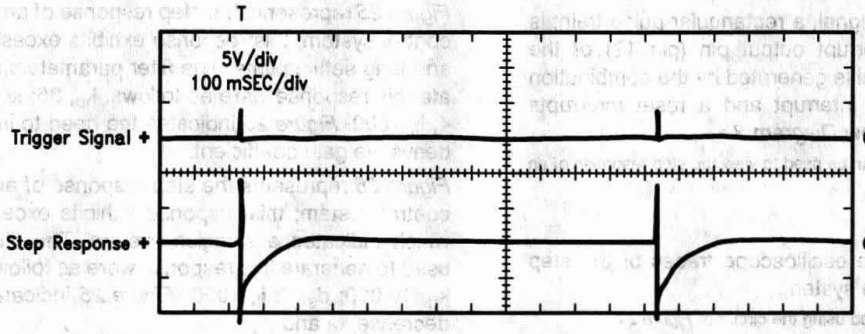

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FIGURE 26. The Step Response of an Over Damped Control System

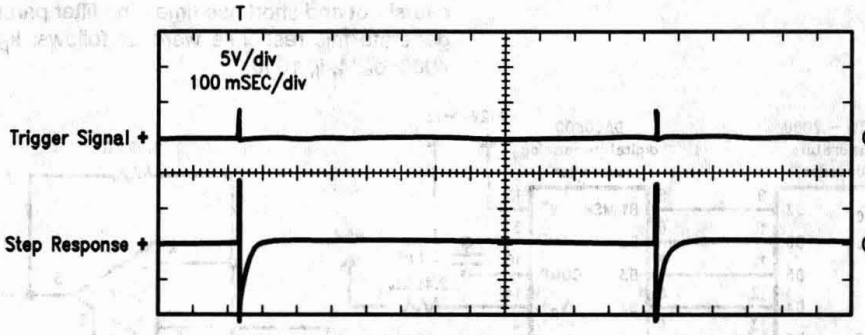

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FIGURE 27. The Step Response of a Critically Damped Control System

A DMOS 3A, 55V, H-Bridge: The LMD18200

National Semiconductor
Application Note 694
Tim Regan

INTRODUCTION

The switching power device shown in *Figure 1* is called an H-Bridge. It takes a DC supply voltage and provides 4-quadrant control to a load connected between two pairs of power switching transistors. Because the switches allow current to flow bidirectionally, the voltage across the load and the direction of current through the load can be of either polarity.

H-Bridges are often used to control the speed, position or torque of DC and stepper motors. Traditionally implemented with either discrete or monolithic bipolar transistors, fully integrated solutions are becoming increasingly popular in printer, plotter, robotics and process control applications that require 0.5A to 3.0A and operate from 12V to 55V. The LMD18200 was designed to operate within this range and was optimized for such applications.

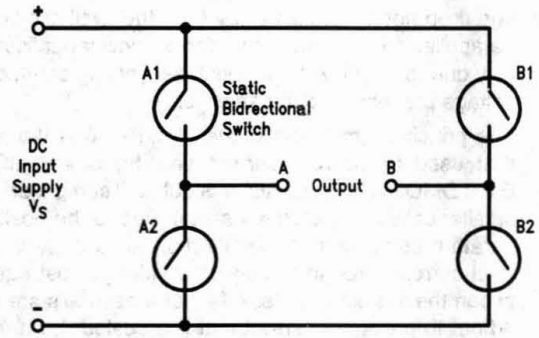

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FIGURE 1. Basic H-Bridge Circuit

The LMD18200 was implemented in a process that allows bipolar, CMOS and DMOS devices to be incorporated together on one die. As each of these types of transistor structures has its own unique characteristics, each is ideally suited for a different function. By integrating them together, this allowed us to take advantage of several innovative design techniques to provide easy to use benefits typically unassociated with a simple motor driver.

Figure 2 shows a functional block diagram of the LMD18200. The circuit contains four DMOS power switching transistors, with intrinsic clamp diodes, connected in an H-Bridge configuration. All level shifting and drive circuits are included to permit control of the H-Bridge from standard logic compatible signal levels. Other unique features include current sense circuitry, overcurrent and under-voltage protection, thermal warning and thermal shutdown. Each is discussed in more detail in the following section.

KEY FEATURES

DMOS Power Drivers

DMOS power transistors allow current to flow bidirectionally and provide a lower voltage drop than similarly rated bipolar power transistors by virtue of a greatly reduced on resistance for each switch. They also have the potential to operate at much faster switching speeds for more efficient operation. And, as each switch contains its own intrinsic protection diode, the additional external protection diodes that are required for bipolar transistor implementations are no longer necessary.

Low On Resistance

Unlike bipolar transistors, which have a relatively high voltage drop across them, even at lower currents, the DMOS devices in the LMD18200 have a voltage drop that is essentially a linear function of temperature. The on resistance, $R_{DS(on)}$, of each output transistor is typically 0.3Ω at a junction temperature of 25°C and 0.6Ω at 125°C. At 100°C and 1A of current, a comparable bipolar transistor will have a voltage drop from collector to emitter of about 1.1V whereas with the LMD18200 this voltage drop will only be 0.45V. At higher current levels the lower voltage drop across a DMOS power device provides an appreciable reduction in power dissipation resulting in smaller heat sink requirements and better efficiency with more power throughput to the load.

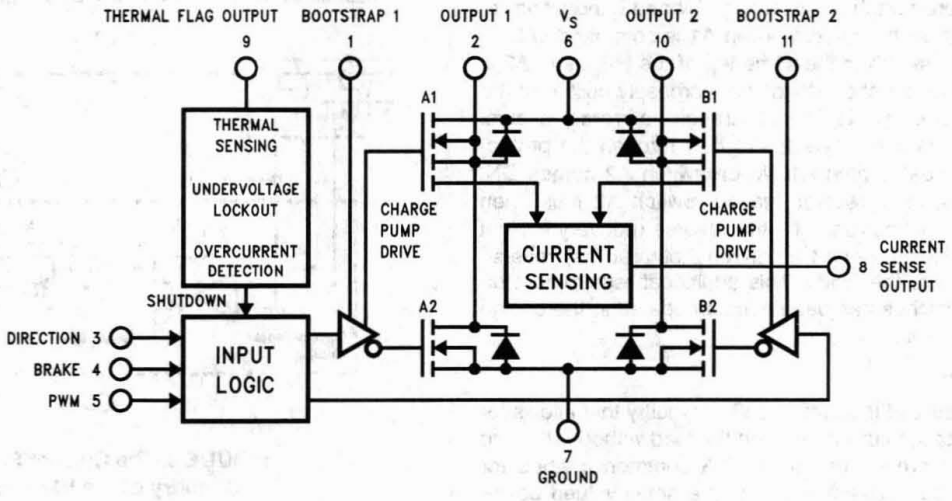

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FIGURE 2. Block Diagram of the LMD18200

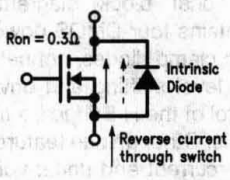

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FIGURE 3. A DMOS Switch with Intrinsic Protection Diode

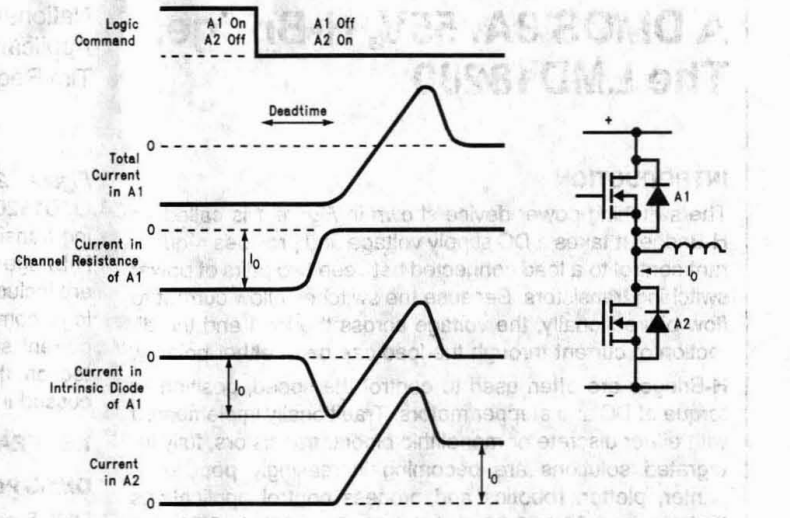

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FIGURE 4. Waveforms Illustrating the Commutation of "Reverse" Current in One Switch (A1) to "Forward" Current in Another Switch (A2)

Bidirectional Current Switches with Intrinsic Protection Diodes

When driving inductive and inertial loads such as motors the power switches must be able to conduct "forward" as well as "reverse" current. The energy stored in these types of loads must generally be free to return to the supply.

The conventional method of providing a path for reverse current is to connect an antiparallel diode across the power switch as shown in *Figure 3*.

With the DMOS structure used in the LMD18200 this diode is intrinsic. Reverse current is actually shared between the power switch and the diode due to the fact that the DMOS switch can conduct current in either direction. For current levels less than 2A to 2.5A the voltage across the power switch, ($IxR_{DS(on)}$), is less than the forward threshold voltage of the diode and all of the current flows through the switch. At higher current levels the diode conducts and the current is shared.

An important consideration in the design of the LMD18200 was to make sure that the power switches could handle not only the load current but also the additional reverse recovery current of the protection diodes. This is illustrated in *Figure 4* where switch A1 is initially ON and conducting reverse current. At the interval when A1 is commanded OFF and the lower switch in the same leg of the H-Bridge, A2 is commanded ON, a short deadtime (purposely built in to the LMD18200 to eliminate "shoot-through" currents) occurs. During this time current begins to flow through the protection diode across switch A1. When switch A2 comes ON, the diode becomes reverse biased. Switch A2 must then conduct the load current plus the reverse recovery current of the diode for the short (approximately 100 ns) reverse recovery time of the diode. This additional requirement on the power switches has been accommodated in the design of the LMD18200.

Current Sensing

A unique feature of the LMD18200 is circuitry that allows for the sensing of the current through the load without affecting the supply or ground return lines. A common method for sensing the load current is to insert a small valued power resistor in series with either the V_{CC} supply or ground lines and detect the voltage drop across this resistor. This voltage drop not only takes away from the available voltage to be applied to the load but is also somewhat difficult to amplify due to very low or possibly fast varying common mode voltage presented to the amplifier.

The principle employed in the LMD18200 is the same as that used in discrete current sensing power MOSFETs. Each DMOS power transistor is actually comprised of many smaller cells connected in parallel. Due to the positive temperature coefficient of the ON resistance of each cell, the total current through the switch divides almost equally between the individual cells. A few of these cells are separated out to provide a current that is a scaled down replica of the total switch current. *Figure 5* shows a simplified functional diagram of the current sensing circuitry.

The current sourced by the Current Sense Output pin is a current proportional to the sum of the total forward current conducted by the two upper DMOS switches of the H-Bridge. This sense current has a typical value of 377 μA per Amp of current through the power devices. Simply connecting a resistor between the sense output pin and ground converts this current to a voltage proportional to the current being delivered to the load. This voltage is then suitable for feedback control or load over-current protection purposes.

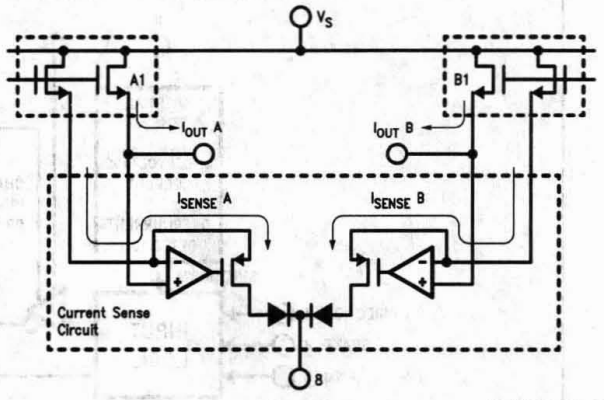

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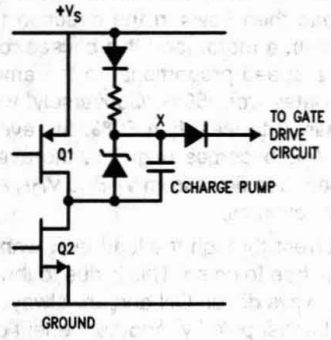
FIGURE 5. The Current Sensing Circuitry of the LMD18200

Charge Pump and Bootstrap Circuitry

In order to drive a DMOS switch ON, its gate must be driven approximately 10V more positive than its source voltage. The lower switches of the H-Bridge have their source terminals connected to ground and their gate drive is derived from the V_S supply voltage to the device. The two upper switches however have their source terminals connected to the output pins which are continually being switched between ground and V_S. In order to generate the gate drive voltage for these switches a charge pump circuit is used. *Figure 6a* illustrates this circuitry.

Transistors Q1 and Q2 are toggled at an internally generated clock frequency of 300 kHz. When Q2 is ON, the on-chip charge pump capacitor, C_{CP}, is charged to approximately 14V. When Q1 is switched ON the bottom of this capacitor is connected to the supply voltage, V_S. This causes the voltage at point X, which connects to the gate of the upper DMOS power switch, to rise to about 14V more positive than the supply. This ensures that the upper device switches ON even if its source is at the V_S potential.



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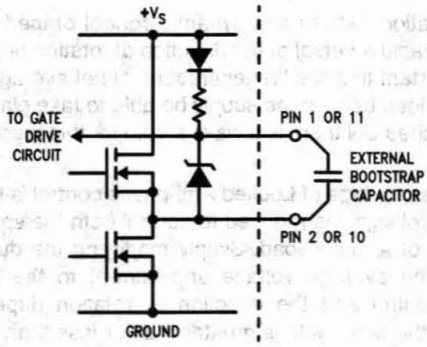
(a)



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(b)

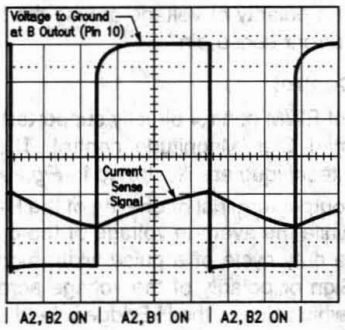
FIGURE 6. Internal Charge Pump Used in the LMD18200 (a); the Use of External Bootstrap Capacitors (b)

Capacitor C_{CP} is limited in value for practical considerations. Due to the limited charge that can be stored in C_{CP} the turn-on time of the upper DMOS transistors is relatively slow but nevertheless satisfactory for operating frequencies up to around 1 kHz. Once the DMOS device is turned ON the 300 kHz oscillator keeps the charge pump circuit running thereby holding the power device ON as long as it is commanded by the input control to do so. This charge pump circuit takes care of all the necessary voltage conditioning required by the DMOS transistors so that the external logic control applied to the LMD18200 can be simple TTL compatible signals.

For higher frequency operation, faster turn-on of the upper DMOS switches is necessary. This can be obtained through the use of external bootstrap capacitors. The bootstrap circuit is shown in *Figure 6b*. The operating principle is similar to that of the charge pump circuitry except that the switching of the bootstrap capacitor, C_B, is assumed by the DMOS power switches of the H-Bridge itself. With plenty of current available to charge these external capacitors they can have a relatively large value (10 nF is recommended) and still be charged in typically less than one microsecond. Since C_B is much larger than the input capacitance of the DMOS power transistors, these transistors can now turn ON very rapidly, typically in about 100 ns, thus allowing operating the LMD18200 at switching frequencies up to 500 kHz. *Figure 7* illustrates the switching performance of the upper transistors with and without the use of external bootstrap capacitors.

Overcurrent Protection

The current through the upper two power DMOS switches is continually monitored and compared against a shutdown trip level (approximately 10A). In the event of a short between the two outputs or a short from either output to ground or any load condition creating excessive current to



Charge Pump
Only
Voltage 5V/Div
100 μs/Div
Current 1A/Div

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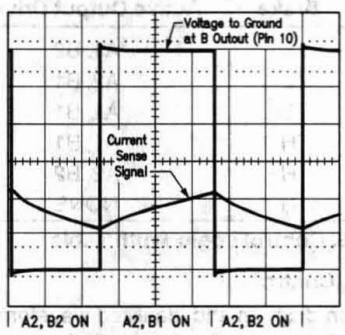

Bootstrap
Capacitors = 10 nf
Voltage 5V/Div
100 μs/Div
Current 1A/Div

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FIGURE 7. Comparison of Switching Waveforms with and without the Use of Bootstrap Capacitors

flow, the overcurrent protection circuitry will switch the upper switches OFF. A unique feature of this protection mechanism is that the protection circuitry will periodically (approximately every 8 μs) turn the upper switches back ON again, so long as the input logic is commanding the switch to be ON. This allows the H-Bridge to restart automatically following a temporary overload fault.

Thermal Warning/Thermal Shutdown

As with any power device protection against excessive operating temperature is a must. The LMD18200 continually senses the junction temperature near the DMOS switches and disables all of the switches in the event that this temperature reaches approximately 170°C thus protecting the device from catastrophic failure. There is a slight amount of hysteresis associated with this temperature threshold so that when the temperature cools slightly the device will automatically restart.

Another unique feature of the LMD18200 is the provision of an early warning flag of excessive operating temperature. This is an open collector output pin which pulls to a logic 0 state when the junction temperature reaches 145°C. This flag can signal the system controller that the power driver is getting too hot and should be either shut down or have the output power cut back. The warning flags from any number of H-Bridges can be directly wired together for an "Or'd" connection.

Undervoltage Lockout

The LMD18200 also features undervoltage lockout. This circuitry disables all of the switches when the DC power supply voltage falls below approximately 10V. The reason for this feature is that reliable, well controlled operation of the switches cannot be assured without at least 10V applied.

OPERATION

The average output voltage across the load of the H-Bridge is continuously controlled by Pulse Width Modulation (PWM). Either polarity of output voltage can be obtained and current can flow through the load in either direction as required. The LMD18200 has three logic control inputs, PWM, Direction and Brake which control the switching action of the H-Bridge. *Figure 8* outlines the effect of these control inputs. The logic control inputs can be used directly (without external logic) to implement two of the more common PWM control techniques, Locked Antiphase control and Sign/Magnitude control.

PWM	Dir	Brake	Active Output Drivers
H	H	L	A1, B2
H	L	L	A2, B1
L	X	L	A1, B1
H	H	H	A1, B1
H	L	H	A2, B2
L	X	H	NONE

FIGURE 8. Control Logic Truth Table

Locked Anti-Phase Control

The basic connection diagram and idealized waveforms for driving an inductive load using Locked Anti-phase control are illustrated in *Figure 9*. Under the control of the single PWM input signal, diametrically opposite pairs of switches (the top switch in one leg of the H-Bridge together with the bottom switch of the opposite leg) are driven ON and OFF together ("locked" together, hence the name Locked Anti-phase control). At zero average output voltage, the average voltage at each output terminal is midway between the V_{CC} supply and ground. For this condition the conduction duty cycle of each switch is 50% and the average current through the load is zero.

As the A1,B2 locked conduction interval is increased by changing the duty cycle of the control signal (75% as shown in the figure), the conduction time for the A2,B1 pair is correspondingly decreased. This duty cycle change makes the average voltage at V_OA more positive than V_OB thereby impressing a voltage across the load. The average current through the load then flows in the direction from terminal V_OA to V_OB. With a motor load this causes rotation in one direction with a speed proportional to the amount that the duty cycle deviates from 50%. Conversely, when the duty cycle is decreased to less than 50%, the average voltage from V_OA to V_OB becomes negative, the average current through the load then flows from V_OB to V_OA and the direction of rotation reverses.

If the ripple current through the load ever wants to reverse its direction it is free to do so. This is due to the fact that two switches are always driven ON and are always able to conduct current of either polarity. Another benefit of this type of control is that the voltage across the load is always defined by the state of the switches, regardless of the direction the load current wants to flow.

In applications where fast dynamic control of inertial loads (i.e., the rapid reversal of the direction of rotation of a motor) it is important that the "regeneration" of net average power from the load back to the supply be able to take place. With two switches ON there is always a path for this regenerative energy.

A major advantage of Locked Anti-phase control is that only one control signal is required to control both the speed and direction of a motor load. Simply modifying the duty cycle adjusts the average voltage and current to the load for speed control and the direction of rotation depends on whether the duty cycle is greater than or less than 50%.

One disadvantage of Locked Anti-phase control with the LMD18200 is that the current sense output is discontinuous as shown in *Figure 9*. This is because the current sensing transistors only mirror "forward" current through the upper two DMOS power devices. "Reverse" current, when the direction of current flow is in the opposite direction of what it should be for a given polarity of voltage across the load, is not output to the current sense pin.

Sign/Magnitude Control

A second method of PWM control directly supported by the LMD18200 is termed Sign/Magnitude control. The ideal waveforms for this technique are illustrated in *Figure 10*.

The voltage of the output terminal of one leg of the H-Bridge is held stationary while the average voltage of the opposite leg is varied by the duty cycle of a pulse width modulated input signal. The Sign or polarity of the voltage across the load is dictated by which side of the H-Bridge is held stationary by having one of the transistors constantly ON, and the Magnitude of the average load voltage is determined by the switching duty cycle of the two switches in the opposite leg.

LOCKED ANTIPHASE CONTROL

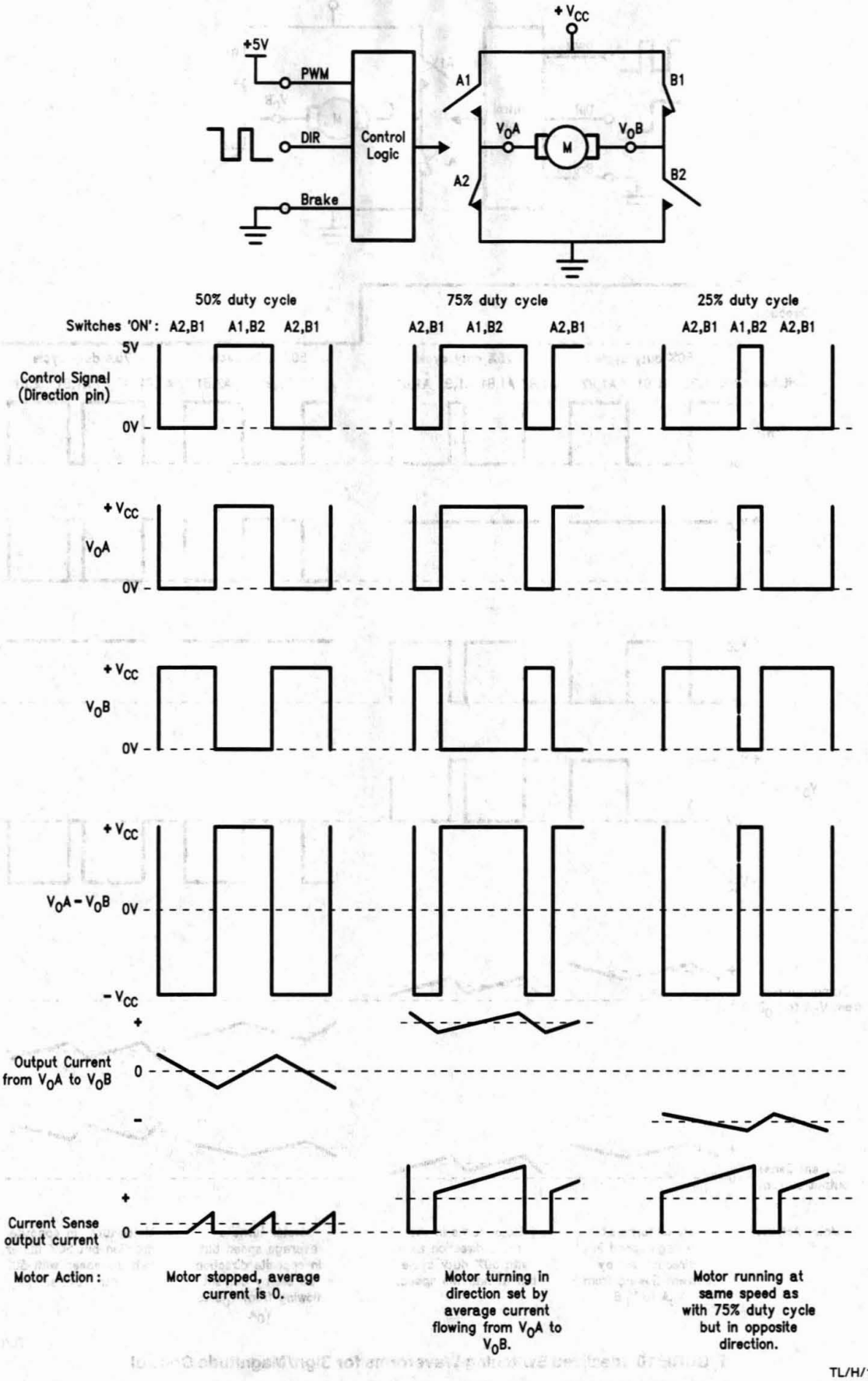

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FIGURE 9. Idealized Switching Waveforms for Locked Antiphase Control

SIGN/MAGNITUDE CONTROL

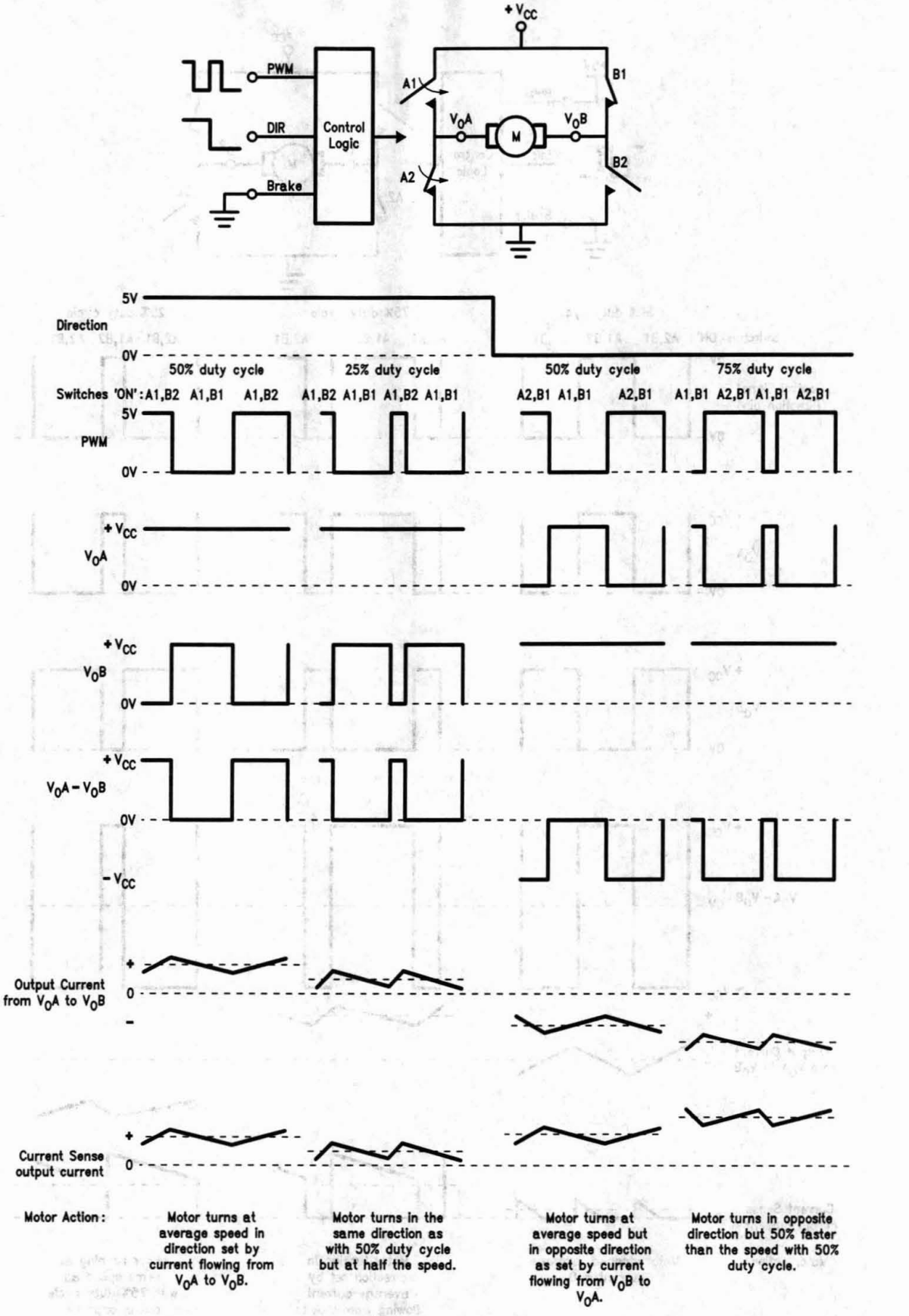

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FIGURE 10. Idealized Switching Waveforms for Sign/Magnitude Control

The logic level applied to the Direction input turns ON either switch A1 or B1. This fixes output V_OA or V_OB at the positive supply voltage potential and therefore sets the direction of current flow through the load. The duty cycle of the signal applied to the PWM pin then adjusts the average voltage and current to the load. As the duty cycle is increased, the power to the load increases causing a faster speed of rotation of motor loads.

Keeping one of the upper transistors continually ON for Sign/Magnitude control is preferred with the LMD18200 because the current sense output will remain permanently active. Current will always be flowing through one upper transistor or the other (through switch A1 or B1) which will be sensed and output to the current sense pin. This gives a continuous representation of the load current without the discontinuities of the locked anti-phase technique. This is true so long as the direction of the current through the load corresponds with the polarity of voltage across the load. If the direction of rotation of a motor load is required to reverse there will be a short interval where the load regenerates net energy back to the supply and "reverse" current flows through the upper power devices and momentarily causes a discontinuity in the current sense output signal.

Braking

Emergency braking of a motor by shorting its terminals is achieved by taking both the PWM and Brake input pins to a logic 1 level. If the Direction input is at a logic 1, then braking will be accomplished by the two upper switches (A1 and B1) turning ON and shorting the motor, if a logic 0 then the lower switches (A2 and B2) will short out the motor. It is preferable to perform braking using the upper switches because they are protected by the overcurrent trip circuitry.

CALCULATING POWER DISSIPATION

To obtain the full performance benefits of the LMD18200 it is important to consider the power dissipation of the device and provide adequate heat sinking as necessary. There are three components that make up the total power dissipation, Quiescent, Conductive and Switching power. The following equations will provide a worst case approximation of each of these components.

Quiescent Power Dissipation, P_Q

This term is simply the quiescent, no load, power dissipation:

$$PQ = I_S \times V_{CC}$$

I_S = the quiescent supply current (typically 13 mA with a maximum value of 25 mA)

V_{CC} = the supply voltage

Conductive Power Dissipation, P_{COND}

This term is the power dissipation of the switches carrying the load current. In all applications the load current is conducted by two of the switches. The equivalent series resistance of the H-Bridge is approximately twice the on-resistance of one switch. The power dissipated by the switches can be found by:

$$P_{COND} = 2 \times I^2_{RMS} \times R_{DS(on)}$$

I_{RMS} = worst case value of the RMS load current

$R_{DS(on)}$ = the ON resistance of a power switch at the operating junction temperature, 0.33Ω typically at 25°C and 0.6Ω maximum at 125°C.

Switching Power Dissipation, P_{SW}

Switching power dissipation is the combination of the energy dissipated by the switches and protection diodes during the ON/OFF switching action of the H-bridge. The combined total energy of a switch turning ON and the protection diode of a switch turning OFF can be approximated by:

$$E_{ON} = \frac{V_S I_O t_{ON}}{2} + V_S Q_{RR} + V_S I_O t_{RR}$$

When turning OFF one of the DMOS switches and transferring the current back to the protection diodes of the other switches, the turn-off energy can be approximated by:

$$E_{OFF} = \frac{V_S I_O t_{OFF}}{2}$$

The total average switching power dissipation can then be found by:

$$P_{SW} = (E_{ON} + E_{OFF}) \times f$$

This is the switching power dissipation for applications using Sign/Magnitude control where only one transistor is switched at a time. This power dissipation is **doubled** with locked anti-phase control because two transistors are always being switched simultaneously:

$P_{SW} = 2 \times (E_{ON} + E_{OFF}) \times f$, for locked anti-phase.

For these equations use the following values:

V_S = Supply voltage

I_O = peak current to the load

t_{ON} = turn ON time of the DMOS transistors, 100 ns with external bootstrap capacitors, 20 μs without

t_{OFF} = turn OFF time of the DMOS transistors, 100 ns with external bootstrap capacitors, 20 μs without

Q_{RR} = recovered charge of the intrinsic protection diode, use 150 nanocoulombs

t_{RR} = reverse recovery time of the intrinsic diode, use 100 ns

f = operating switching frequency of the H-Bridge

These values will provide a good, worst case approximation of the switching power dissipation.

Total Power Dissipation, P_{TOT}

The total power dissipation of the package is the sum of these three components:

$$P_{TOT} = P_Q + P_{COND} + P_{SW}$$

At low switching frequencies, less than 50 kHz, most of the power dissipated is conductive. When operating at higher frequencies, the switching power dissipation can become considerable and must be taken into consideration.

At 25°C ambient operating temperature with the power TO-220 package in free air, the LMD18200 can dissipate approximately 3W without requiring a heat sink.

APPLICATION EXAMPLES

Applying the LMD18200 is very easy because it is fully self-contained. The only external components required for the power stage are supply bypass capacitors and optional bootstrap capacitors and/or a current sense resistor depending on the particular application. The challenging part of any application is generating and modulating the PWM control signal. This can be achieved with dedicated PWM generators like the LM3525, with simple op amp/comparator configurations, a programmable micro-controller output line, or with a dedicated motion control device like the LM629.

Figure 11 illustrates the direct interface of an LM629 to the LMD18200 to control either the position or velocity of a DC motor. The LM629 is a digitally programmable motor controller which outputs a Sign bit and variable PWM control signal to drive the LMD18200. Feedback of the motor position is accomplished via an optical shaft encoder which generates a given number of counts per revolution of the motor shaft. The digital control algorithm is processed by the LM629 in response to commands from a host microcontroller. As shown, the thermal flag output of the LMD18200 can be used to shutdown the system or back off the drive to the motor should the IC begin to overheat. Emergency braking can also be achieved by directly driving the Brake input of the LMD18200 from an output line of the processor.

In many applications it is desired to control the torque of a motor load which is proportional to the current through the motor. Using the current sense feature of the LMD18200 provides an easy means of sensing and controlling the motor current as shown in *Figure 12*. In this application the LM3525 Regulating Pulse Width Modulator compares the voltage at the current sense output pin of the LMD18200 with an externally generated control voltage and adjusts the duty cycle of the control signal (from 0 to approximately 50%) until the motor is running at the set desired current level. In this example the switching frequency is set to 40 kHz thereby requiring the use of bootstrap capacitors. This is also an example of locked anti-phase control. By simply inverting the phase of the single control input the direction of motor rotation can be reversed.

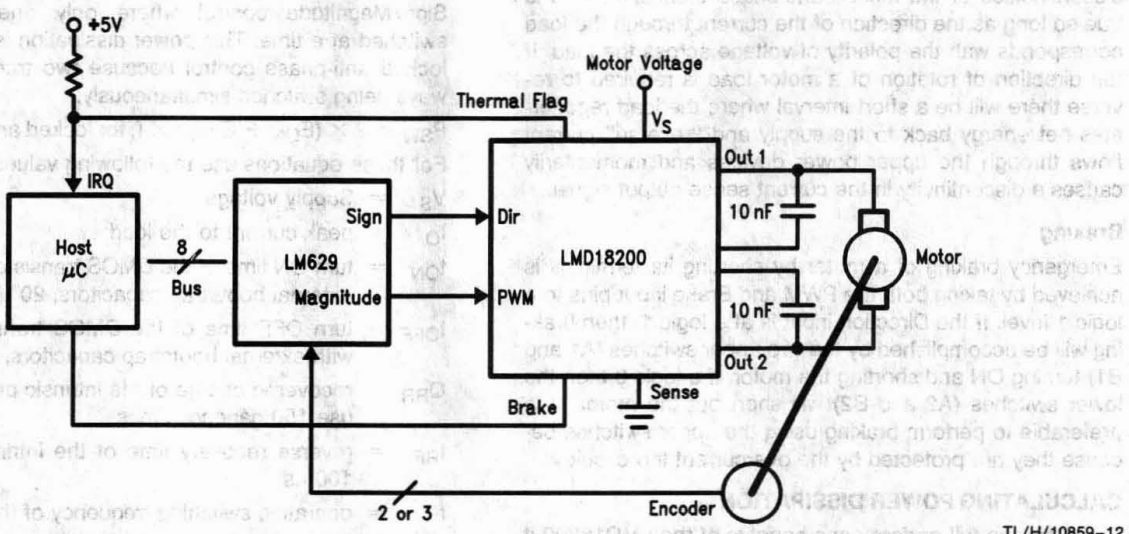

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FIGURE 11. Direct Interface of an LMD 18200 to the LM629 Motion Control Device

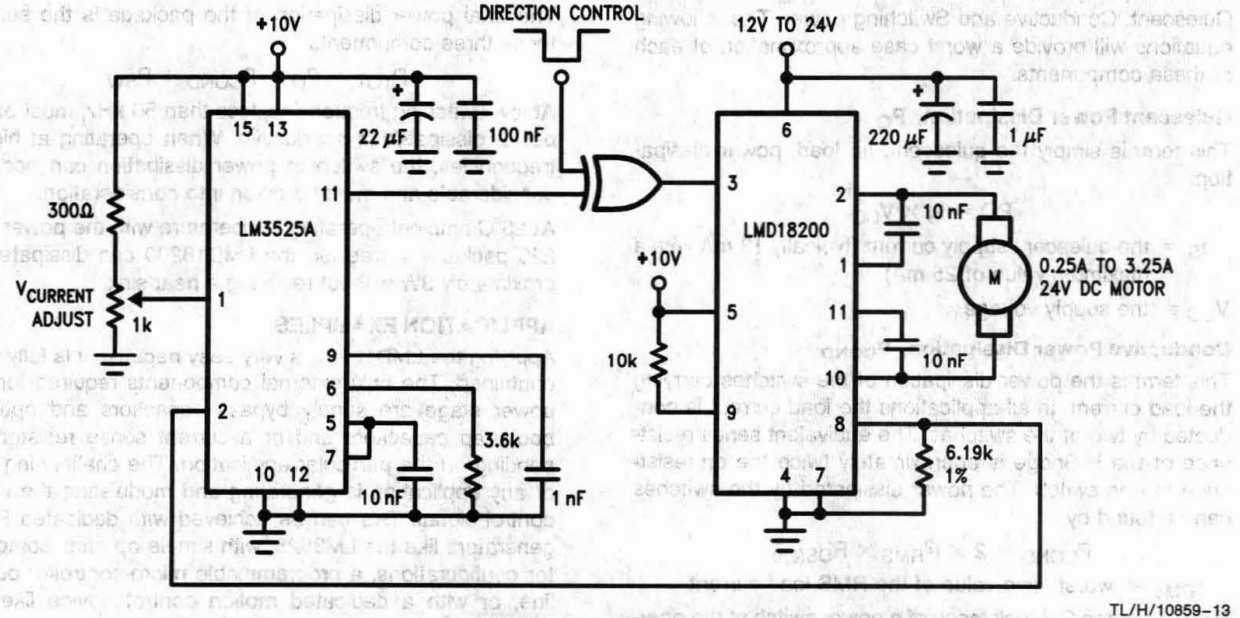

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FIGURE 12. Utilizing the Current Sense Feature to Control the Torque of a Motor Load

Figure 13 shows a conventional analog control scheme termed "Fixed Off Time Control". This again takes advantage of the current sensing feature of the LMD18200. A voltage representing the current through the motor is again compared with an externally generated control voltage. Whenever the motor current exceeds the desired set level a one shot is triggered which turns on the two upper switches of the H-Bridge, shorting out the motor for a fixed time interval. This causes the motor current to decrease. At the end of the one-shot interval, voltage is reapplied to the motor until the current once again exceeds the desired level. As shown in the accompanying waveforms, *Figure 14*, the average motor current modulates or "dithers" about the preset level. The amount of ripple current is proportional to the time interval of the one-shot. A certain minimum amount of ripple is required to prevent the voltage comparator from oscillating. The equivalent of 50 mV voltage change at the input to the comparator is sufficient.

The off time interval is equal to 1.1 RC, which are the timing components for the LM555 timer.

This application is an example of Sign/Magnitude control. To reverse the motor direction simply drive the Direction input of the LMD18200.

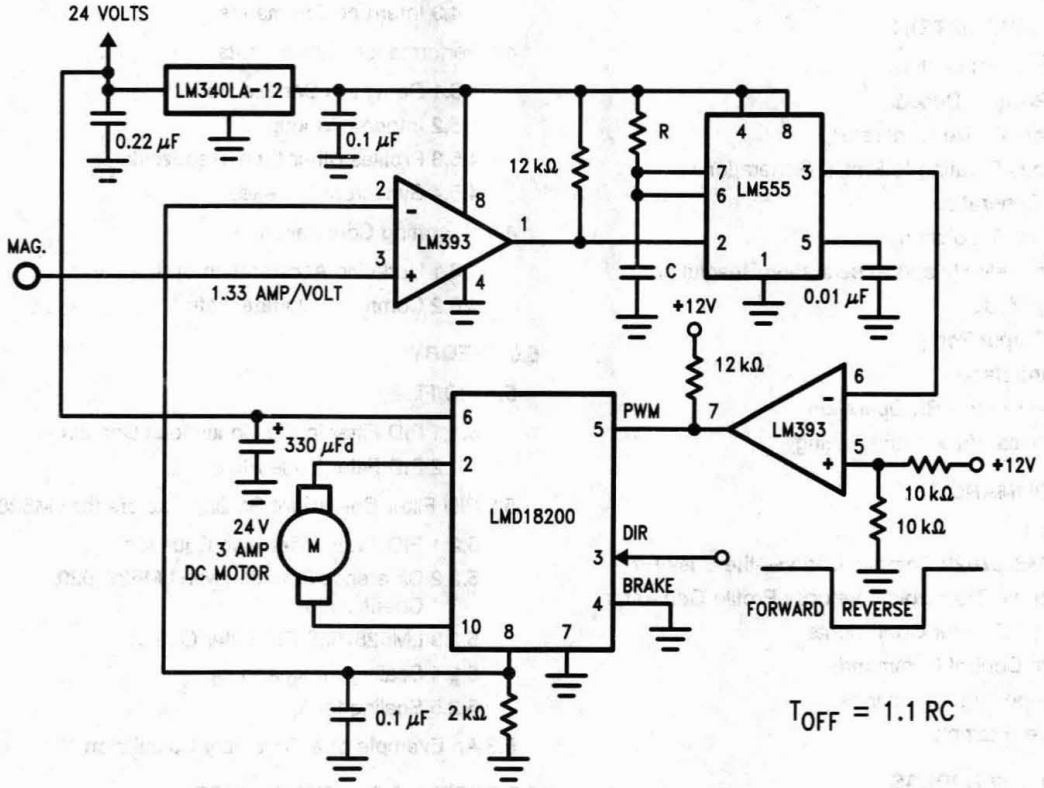

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FIGURE 13. Fixed OFF Time Control

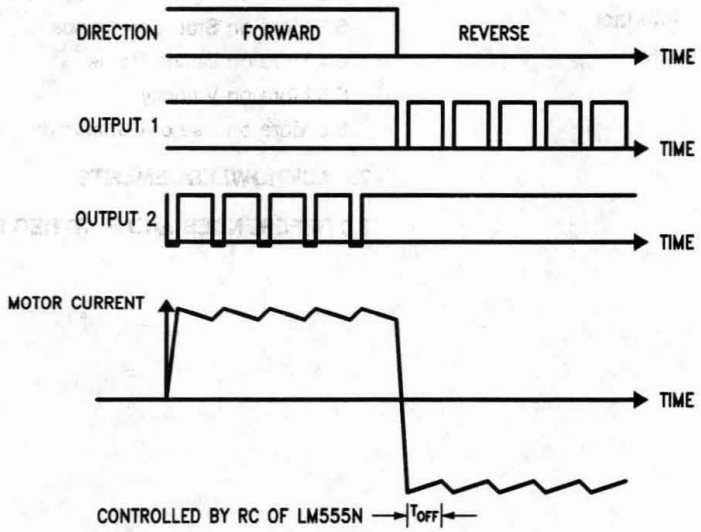

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FIGURE 14. Switching Waveforms for the Fixed OFF Time Control Loop

LM628/629 User Guide

National Semiconductor
Application Note 706

Table of Contents

1.0 INTRODUCTION

1.1 Application Note Objectives
1.2 Brief Description of LM628/629

2.0 DEVICE DESCRIPTION

2.1 Hardware Architecture
2.2 Motor Position Decoder
2.3 Trajectory Profile Generator
2.4 Definitions Relating to Profile Generation
2.5 Profile Generation
2.6 Trajectory Resolution
2.7 Position, Velocity and Acceleration Resolution
2.8 Velocity Mode
2.9 Motor Output Port
2.10 Host Interface
2.11 Hardware Busy Bit Operation
2.12 Filter Initial Values and Tuning

3.0 USER COMMAND SET

3.1 Overview
3.2 Host-LM628/629 Communication—the Busy Bit
3.3 Loading the Trapezoidal Velocity Profile Generator
3.4 Loading PID Filter Coefficients
3.5 Interrupt Control Commands
3.6 Data Reporting Commands
3.7 Software Example

4.0 HELPFUL USER IDEAS

4.1 Getting Started
4.2 Hardware
4.2.1 Host Microcontroller Interface
4.2.2 Position Encoder Interface
4.2.3 Output Interface
4.3 Software
4.4 Initialization
4.4.1 Hardware RESET Check
4.4.2 Initializing LM628 Output Port
4.4.3 Interrupt Commands
4.5 Performance Refinements
4.5.1 Derivative Sample Rate
4.5.2 Integral Windup
4.5.3 Profiles other than Trapezoidal
4.5.4 Synchronizing Axes
4.6 Operating Constraints
4.6.1 Updating Acceleration on the Fly
4.6.2 Command Update Rate

5.0 THEORY

5.1 PID Filter
5.1.1 PID Filter in the Continuous Domain
5.1.2 PID Filter Bode Plots
5.2 PID Filter Coefficient Scaling Factors for LM628/629
5.2.1 PID Filter Difference Equation
5.2.2 Difference Equation with LM628/629 Coefficients
5.2.3 LM628/629 PID Filter Output
5.2.4 Scaling for k_p and k_d
5.2.5 Scaling for k_i
5.3 An Example of a Trajectory Calculation

6.0 QUESTIONS AND ANSWERS

6.1 The Two Most Popular Questions
6.2 More on Acceleration Change
6.3 More on Stop Commands
6.4 More on Define Home
6.5 More on Velocity
6.6 More on Use of Commands

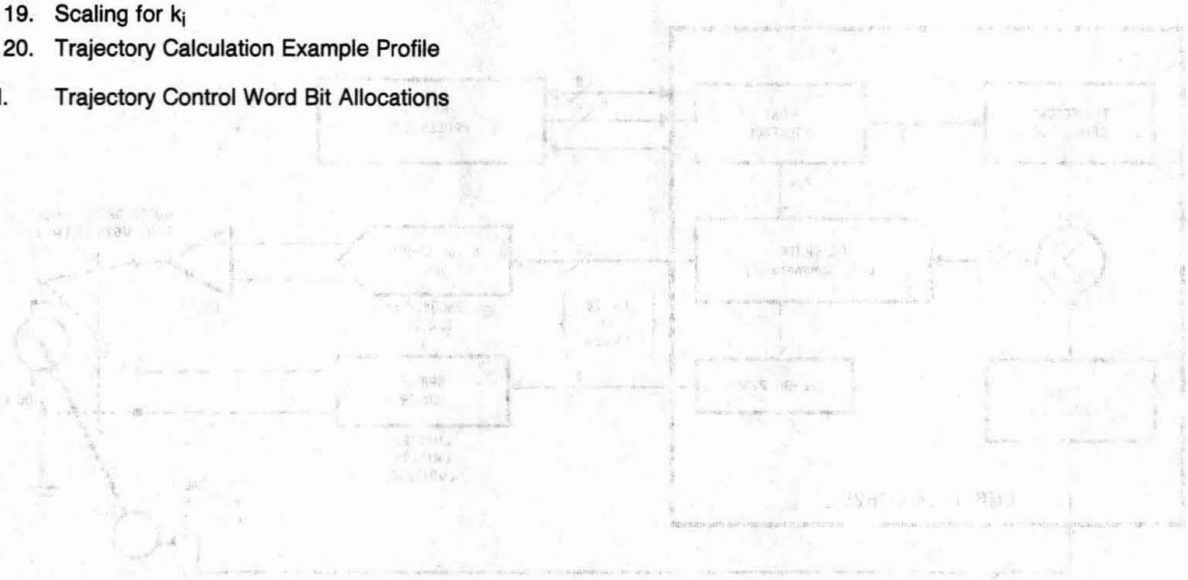
7.0 ACKNOWLEDGEMENTS

8.0 REFERENCES AND FURTHER READING

List of Illustrations

Figure 1. LM628 and LM629 Typical System Block Diagram
Figure 2. Hardware Architecture of LM628/629
Figure 3. Quadrature Encoder Output Signals and Direction Decode Table
Figure 4. LM628/629 Motor Position Decoder
Figure 5. Typical Trajectory Velocity Profile
Figure 6. Position, Velocity and Acceleration Registers
Figure 7. LM628 12-Bit DAC Output Multiplexed Timing
Figure 8. LM629 PWM Output Signal Format
Figure 9. Host Interface Internal I/O Registers
Figure 10. Busy Bit Operation during Command and Data Write Sequence
Figure 11. Position vs Time for 100 Count Step Input
Figure 12. Basic Software Flow
Figure 13. LM628 and LM629 Host, Output and Position Encoder Interfaces
Figure 14. LM628 Example of Linear Motor Drive using LM12
Figure 15. LM629 H-Bridge Motor Drive Example using LM18293
Figure 16. Generating a Non-Trapezoidal Profile
Figure 17. Bode Plots of PID Transfer Function
Figure 18. Scaling for k_p and k_d
Figure 19. Scaling for k_i
Figure 20. Trajectory Calculation Example Profile

Table I. Trajectory Control Word Bit Allocations



1.0 INTRODUCTION

1.1 Application Note Objective

This application note is intended to explain and complement the information in the data sheet and also address the common user questions. While no initial familiarity with the LM628/629 is assumed, it will be useful to have the LM628/629 data sheet close by to consult for detailed descriptions of the user command set, timing diagrams, bit assignments, pin assignments, etc.

After the following brief description of the LM628/629, Section 2.0 gives a fairly full description of the device's operation, probably more than is necessary to get going with the device. This section ends with an outline of how to tune the control system by adjusting the PID filter coefficients.

Section 3 "User Command Set" discusses the use of the LM628/629 commands. For a detailed description of each command the user should refer to the data sheet.

Section 4 "Helpful User Ideas" starts with a short description of the actions necessary to get going, then proceeds to talk about some performance enhancements and follows on with a discussion of a couple of operating constraints of the device.

Section 5 "Theory" is a short foray into theory which relates the PID coefficients that would be calculated from a continuous domain control loop analysis to those of the discrete domain including the scaling factors inherent to the LM628/629. No attempt is made to discuss control system theory as such, readers should consult the ample references available, some suggestions are made at the end of this application note. Section 5 concludes with an example trajectory calculation, reviving those perhaps forgotten ideas about acceleration, velocity, distance and time.

Section 6 "Questions and Answers", is in question and answer format and is born out of and dedicated to the many interesting discussions with customers that have taken place.

1.2 Brief Description of LM628/629

LM628/629 is a microcontroller peripheral that incorporates in one device all the functions of a sample-data motion control system controller. Using the LM628/629 makes the potentially complex task of designing a fast and precise motion control system much easier. Additional features, such as trajectory profile generation, on the "fly" update of loop compensation and trajectory, and status reporting, are included. Both position and velocity motion control systems can be implemented with the LM628/629.

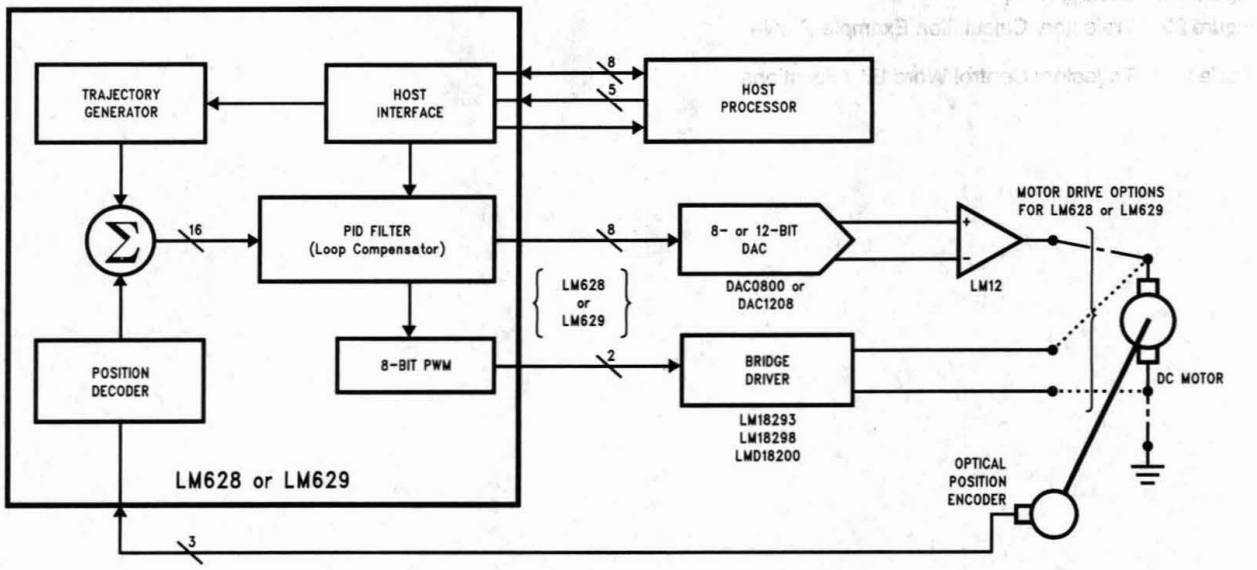


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FIGURE 1. LM628 and LM629 Typical System Block Diagram

LM628/629 is itself a purpose designed microcontroller that implements a position decoder, a summing junction, a digital PID loop compensation filter, and a trajectory profile generator, *Figure 1.* Output format is the only difference between LM628 and LM629. A parallel port is used to drive an 8- or 12-bit digital-to-analog converter from the LM628 while the LM629 provides a 7-bit plus sign PWM signal with sign and magnitude outputs. Interface to the host microcontroller is via an 8-bit bi-directional data port and six control lines which includes host interrupt and hardware reset. Maximum sampling rates of either 2.9 kHz or 3.9 kHz are available by choosing the LM6268/9 device options that have 6 MHz or 8 MHz maximum clock frequencies (device -6 or -8 suffixes).

In operation, to start a movement, a host microcontroller downloads acceleration, velocity and target position values to the LM628/629 trajectory generator. At each sample interval these values are used to calculate new demand or "set point" positions which are fed into the summing junction. Actual position of the motor is determined from the output signals of an optical incremental encoder. Decoded by the LM628/629's position decoder, actual position is fed to the other input of the summing junction and subtracted from the demand position to form the error signal input for the control loop compensator. The compensator is in the form of a "three term" PID filter (proportional, integral, derivative), this is implemented by a digital filter. The coefficients for the PID digital filter are most easily determined by tuning the control system to give the required response from the load in terms of accuracy, response time and overshoot. Having characterized a load these coefficient values are downloaded from the host before commencing a move. For a load that varies during a movement more coefficients can be downloaded and used to update the PID filter at the moment the load changes. All trajectory parameters except acceleration can also be updated while a movement is in progress.

2.0 DEVICE DESCRIPTION

2.1 Hardware Architecture

Four major functional blocks make up the LM628/629 in addition to the host and output interfaces. These are the Trajectory Profile Generator, Loop Compensating PID Filter, Summing Junction and Motor Position Decoder *(Figure 1).*

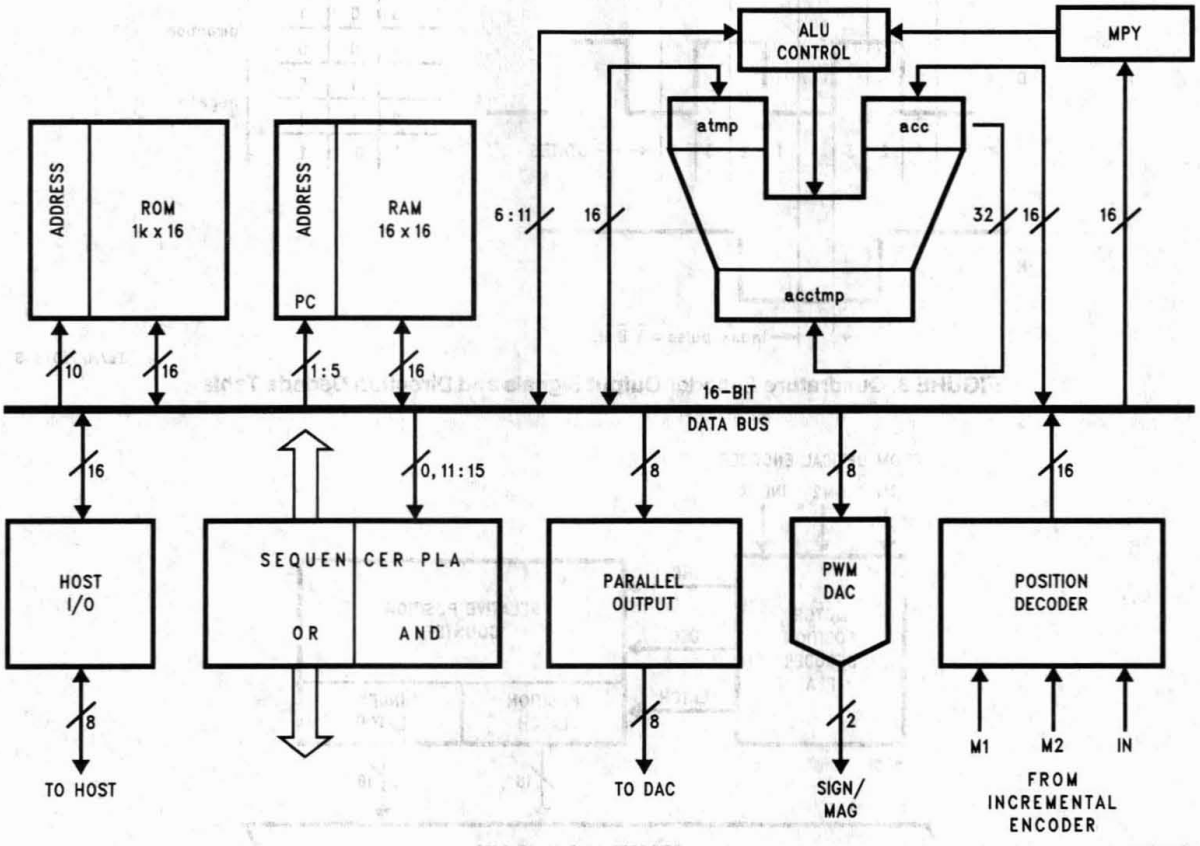

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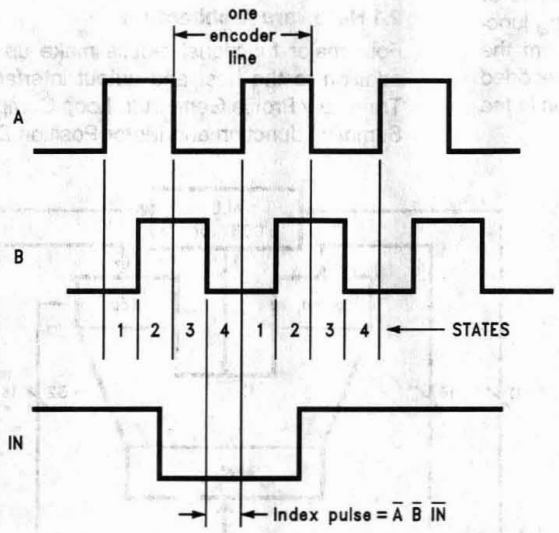
FIGURE 2. Hardware Architecture of LM628/629

Details of how LM628/629 is implemented by a purpose designed microcontroller are shown in *Figure 2.* The control algorithm is stored in a 1k x 16-bit ROM and uses 16-bit wide instructions. A PLA decodes these instructions and provides data transfer timing signals for the single 16-bit data and instruction bus. User variable filter and trajectory profile parameters are stored as 32-bit double words in RAM. To provide sufficient dynamic range a 32-bit position register is used and for consistency. 32 bits are also used for velocity and acceleration values. A 32-bit ALU is used to support the 16 x 16-bit multiplications of the error and PID digital filter coefficients.

2.2 Motor Position Decoder

LM628/629 provides an interface for an optical position shaft encoder, decoding the two quadrature output signals to provide position and direction information, *Figure 3.* Optionally a third index position output signal can be used to capture position once per revolution. Each of the four states of the quadrature position signal are decoded by the LM628/629 giving a 4 times increase in position resolution over the number of encoder lines. An "N" line encoder will be decoded as "4N" position counts by LM628/629.

Position decoder block diagram, *Figure 4,* shows three lines coming from the shaft encoder, M1, M2 and Index. From these the decoder PLA determines if the motor has moved forward, backward or stayed still and then drives a 16-bit up-down counter that keeps track of actual motor position. Once per revolution when all three lines including the index line are simultaneously low, *Figure 3,* the current position count is captured in an index latch.



State	A	B	
1	1	0	positive
2	1	1	
3	0	1	direction
4	0	0	
1	1	0	negative
2	1	1	
3	0	1	

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FIGURE 3. Quadrature Encoder Output Signals and Direction Decode Table

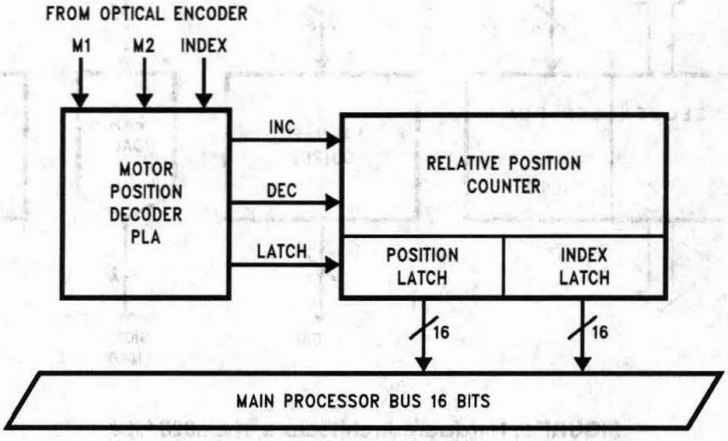

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FIGURE 4. LM628/629 Motor Position Decoder

The 16-bit up-down counter is used to capture the difference in position from one sample to the next. A position latch attached to the up-down counter is strobed at the same time in every sample period by a sync pulse that is generated in hardware. The position latch is read soon after the sync pulse and is added to the 32-bit position register in RAM that holds the actual current position. This is the value that is subtracted in the summing junction every sample interval from the new desired position calculated by the trajectory generator to form the error input to the PID filter.

Maximum encoder state capture rate is determined by the minimum number of clock cycles it takes to decode each encoder state, see *Figure 3,* this minimum number is 8 clock cycles, capture of the index pulse is also achieved during these 8 clock cycles. This gives a more than adequate 1 MHz maximum encoder state capture rate with the 8 MHz f_{CLK} devices (750 kHz for the 6 MHz f_{CLK} devices). For example, with the 1 MHz capture rate, a motor using a 500 line encoder will be moving at 30,000 rpm.

There is some limited signal conditioning at the decoder input to remove problems that would occur due to the asynchronous position encoder input being sampled on signal edges by the synchronous LM628/629. But there is no noise filtering as such on the encoder lines so it is important that they are kept clean and away from noise sources.

2.3 Trajectory Profile Generator

Desired position inputs to the summing junction, *Figure 1,* within the LM628/629 are provided by an internal independent trajectory profile generator. The trajectory profile generator takes information from the host and computes for each sample interval a new current desired position. The information required from the host is, operating mode, either position or velocity, target acceleration, target velocity and target position in position mode.

2.4 Definitions Relating to Profile Generation

The units of position and time, used by the LM628/629, are counts (4 × N encoder lines) and samples (sample intervals = $2048/f_{CLK}$) respectively. Velocity is therefore calculated in counts/sample and acceleration in counts/sample/sample.

Definitions of "target", "desired" and "actual" within the profile generation activity as they apply to velocity, acceleration and position are as follows. Final requested values are called "target", such as target position. The values computed by the profile generator each sample interval on the way to the target value are called "desired". Real values from the position encoder are called "actual".

For example, the current actual position of the motor will typically be a few counts away from the current desired position because a new value for desired position is calculated every sample interval during profile generation. The difference between the current desired position and current actual position relies on the ability of the control loop to keep the motor on track. In the extreme example of a locked rotor there could be a large difference between the current actual and desired positions.

Current desired velocity refers to a fixed velocity at any point on a on-going trajectory profile. While the profile demands acceleration, from zero to the target velocity, the velocity will incrementally increase at each sample interval.

Current actual velocity is determined by taking the difference in the actual position at the current and the previous sample intervals. At velocities of many counts per sample this is reasonably accurate, at low velocities, especially below one count per sample, it is very inaccurate.

2.5 Profile Generation

Trajectory profiles are plotted in terms of velocity versus time, *Figure 5,* and are velocity profiles by reason that a new desired position is calculated every sample interval. For constant velocity these desired position increments will be the same every sample interval, for acceleration and deceleration the desired position increments will respectively increase and decrease per sample interval. Target position is the integral of the velocity profile.

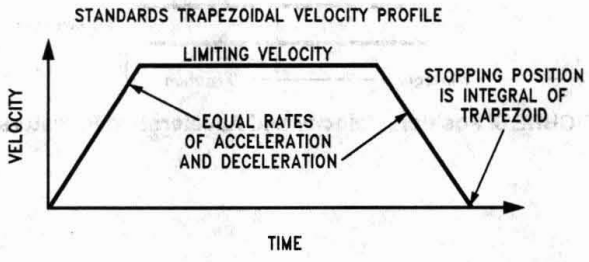

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FIGURE 5. Typical Trajectory Velocity Profile

When performing a move the LM628/629 uses the information as specified by the host and accelerates until the target velocity is reached. While doing this it takes note of the number of counts taken to reach the target velocity. This number of counts is subtracted from the target position to determine where deceleration should commence to ensure the motor stops at the target position. LM628/629 deceleration rates are equal to the acceleration rates. In some cases, depending on the relative target values of velocity, acceleration and position, the target velocity will not be reached and deceleration will commence immediately from acceleration.

2.6 Trajectory Resolution

The resolution the motor sees for position is one integral count. The algorithm used to calculate the trajectory adds the velocity to the current desired position once per sample period and produces the next desired position point. In order to allow very low velocities it is necessary to have velocities of fractional counts per sample. The LM628/629 in addition to the 32-bit position range keeps track of 16 bits of fractional position. The need for fractional velocity counts can be illustrated by the following example using a 500 line (2000 count) encoder and an 8 MHz clock LM628/629 giving a 256 μs sample interval. If the smallest resolution is 1 count per sample then the minimum velocity would be 2 revolutions per second or 120 rpm. (1/2000 revs/count $\times$ 1/256 μs counts/second). Many applications require velocities and steps in velocity less than this amount. This is provided by the fractional counts of acceleration and velocity.

2.7 Position, Velocity and Acceleration Resolution

Every sample cycle, while the profile demands acceleration, the acceleration register is added to the velocity register which in turn is added to the position register. When the demand for increasing acceleration stops, only velocity is added to the position register. Only integer values are output from the position register to the summing junction and so fractional position counts must accumulate over many sample intervals before an integer count is added and the position register changed. *Figure 6* shows the position, velocity and acceleration registers.

The position dynamic range is derived from the 32 bits of the integer position register, *Figure 6.* The MSB is used for the direction sign in the conventional manner, the next bit 30 is used to signify when a position overflow called "wraparound" has occurred. If the wraparound bit is set (or reset when going in a negative direction) while in operation the status byte bit 4 is set and optionally can be used to interrupt the host. The remaining 30 bits provide the available dynamic range of position in either the positive or negative direction ($\pm$1,073,741,824 counts).

Velocity has a resolution of $1/2^{16}$ counts/sample and acceleration has a resolution of $1/2^{16}$ counts/sample/sample as mentioned above. The dynamic range is 30 bits in both cases. The loss of one bit is due to velocity and acceleration being unsigned and another bit is used to detect wraparound. This leaves 14 bits or 16,383 integral counts and 16 bits for fractional counts.

2.8 Velocity Mode

LM628 supports a velocity mode where the motor is commanded to continue at a specified velocity, until it is told to

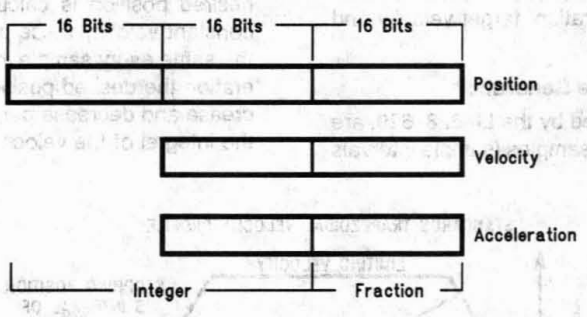

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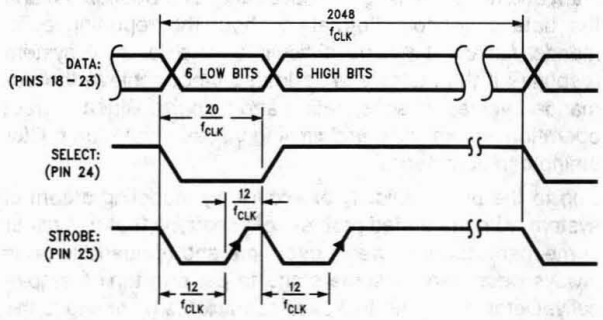
FIGURE 6. Position, Velocity and Acceleration Registers

stop (LTRJ bits 9 or 10). The average velocity will be as specified but the instantaneous velocity will vary. Velocities of fractional counts per sample will exhibit the poorest instantaneous velocity. Velocity mode is a subset of position mode where the position is continually updated and moved ahead of the motor without a specified stop position. Care should be exercised in the case where a rotor becomes locked while in velocity mode as the profile generator will continue to advance the position. When the rotor becomes free high velocities will be attained to catch-up with the current desired position.

2.9 Motor Output Port

LM628 output port is configured to 8 bits after reset. The 8-bit output is updated once per sample interval and held until it is updated during the next sample interval. This allows use of a DAC without a latch. For 12-bit operation the PORT12 command should be issued immediately after reset. The output is multiplexed in two 6-bit words using pins 18 through 23. Pin 24 is low for the least significant word and high for the most significant. The rising edge of the active low strobe from pin 25 should be used to strobe the output into an external latch, see *Figure 7.* The DAC output is offset binary code, the zero codes are hex'80' for 8 bits and hex'800' for 12 bits.

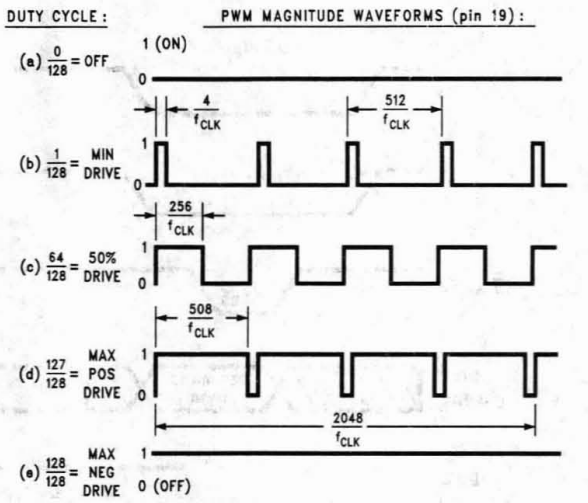


TL/H/11018–7

FIGURE 7. LM628 12-Bit DAC Output Multiplexed Timing

The choice of output resolution is dependant on the user's application. There is a fundamental trade-off between sampling rate and DAC output resolution, the LM628 8-bit output at a 256 μs sampling interval will most often provide as good results as a slower, e.g. microcontroller, implementation which has a 4 ms typical sampling interval and uses a 12-bit output. The LM628 also gives the choice of a 12-bit DAC output at a 256 μs sampling interval for high precision applications.

LM629 PWM sign and magnitude signals are output from pins 18 and 19 respectively. The sign output is used to control motor direction. The PWM magnitude output has a resolution of 8 bits from maximum negative drive to maximum positive drive. The magnitude output has an off condition, with the output at logic low, which is useful for turning a motor off when using a bridge motor drive circuit. The minimum duty cycle is 1/128 increasing to a maximum of 127/128 in the positive direction and a maximum of 128/128 in the negative direcition, i.e., a continuous output. There are four PWM periods in one LM629 sample interval. With an 8 MHz clock this increases the PWM output rate to 15.6 kHz from the LM629 maximum 3.9 kHz sample rate, see *Figure 8* for further timing information.



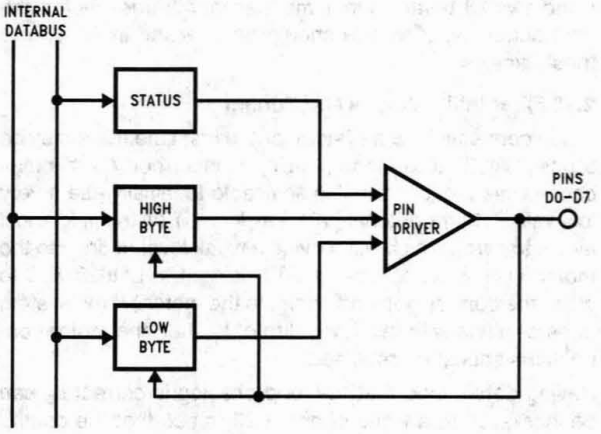
TL/H/11018–8

Note: Sign output (pin 18) not shown.

FIGURE 8. LM629 PWM Output Signal Format

2.10 Host Interface

LM628/629 has three internal registers: status, high, and low bytes, *Figure 9,* which are used to communicate with the host microcontroller. These are controlled by the $\overline{RD}$, $\overline{WR}$, and $\overline{PS}$ lines and by use of the busy bit of the status byte. The status byte is read by bringing $\overline{RD}$ and $\overline{PS}$ low, bit 0 is the busy bit. Commands are written by bringing $\overline{WR}$ and $\overline{PS}$ low. When $\overline{PS}$ is high, $\overline{WR}$ brought low writes data into LM628/629 and similarly, $\overline{RD}$ is brought low to read data from LM628/629. Data transfer is a two-byte operation written in most to least significant byte order. The above description assumes that $\overline{CS}$ is low.



TL/H/11018–9

FIGURE 9. Host Interface Internal I/O Registers

2.11 Hardware Busy Bit Operation

Before and between all command byte and data byte pair transfers, the busy bit must be read and checked to be at logic low. If the busy bit is set and commands are issued they will be ignored and if data is read it will be the current contents of the I/O buffer and not the expected data. The busy bit is set after the rising edge of the write signal for commands and the second rising edge of the respective read or write signal for two byte data transfers, *Figure 10.* The busy bit remains high for approximately 15 μs.

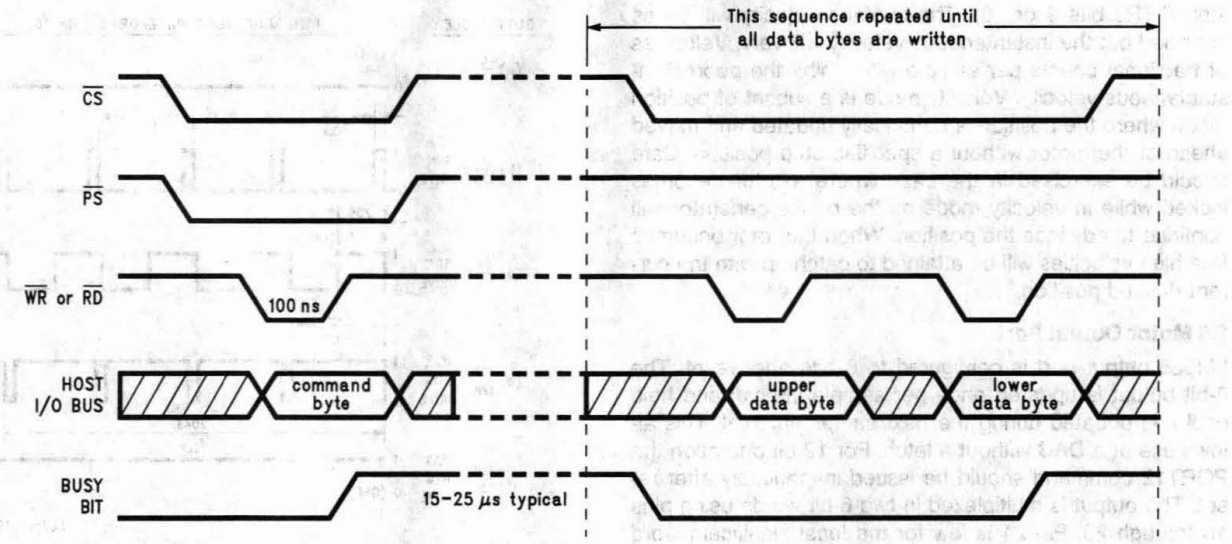


FIGURE 10. Busy Bit Operation during Command and Data Write Sequence

The busy bit reset to logic low indicates that high and low byte registers shown in *Figure 9* have been either loaded or read by the LM628/629 internal microcode. To service the command or data transfer this microcode which performs the trajectory and filter calculations is interrupted, except in critical areas, and the on-going calculation is suspended. The microcode was designed this way to achieve minimum latency when communicating with the host. However, if this communication becomes too frequent and on-going calculations are interrupted too often corruption will occur. In a 256 μs sample interval, the filter calculation takes 50 μs, outputting a sample 10 μs and trajectory calculation 90 μs. If the LM628 behaves in a manner that is unexpected the host communication rate should be checked in relation to these timings.

2.12 Filter Initial Values and Tuning

When connecting up a system for the first time there may be a possibility that the loop phasing is incorrect. As this may cause violent oscillation it is advisable to initially use a very low value of proportional gain, say $k_p = 1$ (with k_d, k_i and il all set to zero), which will provide a weak level of drive to the motor. (The Start command, STT, is sent to LM628/629 to close the control loop and energize the motor.) If the system does oscillate with this low value of k_p then the motor connections should be reversed.

Having determined that the loop phasing is correct k_p can be increased to a value of about 20 to see that the control system basically works. This value of k_p should hold the motor shaft reasonably stiffly, returning the motor to the set position, which will be zero until trajectory values have been input and a position move performed. If oscillation or unacceptable ringing occurs with a k_p value of 20 reduce this until it stops. Low values of acceleration and velocity can now be input, of around 100, and a position move commanded to say 1000 counts. All values suggested here are decimal. For details of loading trajectory and filter parameters see Section 3.0, reference (5) and the data sheet.

It is useful at this stage to try different values of acceleration and velocity to get a feel for the system limitations. These can be determined by using the reporting commands of desired and actual position and velocity, to see if the error between desired and actual positions of the motor are constant and not increasing without bound. See Section 3.6 and the data sheet for information about the reporting commands. Clearly it will be difficult to tune for best system response if the motor and its load cannot achieve the demanded values of acceleration and velocity. When correct operation is confirmed and limiting values understood, filter tuning can commence.

Due to the basic difficulty of accurately modeling a control system, with the added problem of variations that can occur in mechanical components over time and temperature, it is always necessary at some stage to perform tuning empirically. Determining the PID filter coefficients by tuning is the preferred method with LM628/629 because of the inherent flexibility in changing the filter coefficients provided by this programmable device.

Before tuning a control system the effect of each of the PID filter coefficients should be understood. The following is a very brief review, for a detailed understanding reference (2) should be consulted. The proportional coefficient, k_p, provides adjustment of the control system loop proportional gain, as this is increased the output steady state error is reduced. The error between the required and actual position is effectively divided by the loop gain. However there is a natural limitation on how far k_p can be increased on its own to reduce output position error because a reduction in phase margin is also a consequence of increasing k_p. This is first encountered as ringing about the final position in response to a step change input and then instability in the form of oscillation as the phase margin becomes zero. To improve stability, k_d, the derivative coefficient, provides a damping effect by providing a term proportional to velocity in antiphase to the ringing, or viewed in another way, adds some leading phase shift into the loop and increases the phase margin.

In the tuning process the coefficients k_p and k_d are iteratively increased to their optimum values constrained by the system constants and are trade-offs between response time, stability and final position error. When k_p and k_d have been determined the integral coefficient, k_i, can be introduced to remove steady state errors at the load. The steady state

errors removed are the velocity lag that occurs with a constant velocity output and the position error due to a constant static torque. A value of integration limit, il, has to be input with k_i, otherwise k_i will have no effect. The integral coefficient k_i adds another variable to the system to allow further optimization, very high values of k_i will decrease the phase margin and hence stability, see Section 5 and reference (2) for more details. Reference (5) gives more details of PID filter tuning and how to load filter parameters.

Figure 11 illustrates how a relatively slow response with overshoot can be compensated by adjustment of the PID filter coefficients to give a faster critically damped response.

3.0 USER COMMAND SET

3.1 Overview

The following types of User Commands are available:

Initialization
Filter control commands
Trajectory control commands
Interrupt control commands
Data reporting commands

User commands are single bytes and have a varying number of accompanying data bytes ranging from zero to fourteen depending upon the command. Both filter and trajectory control commands use a double buffered scheme to input data. These commands load primary registers with multiple words of data which are only transferred into secondary working registers when the host issues a respective single byte user command. This allows data to be input before its actual use which can eliminate any potential communication bottlenecks and allow synchronized operation of multiple axes.

3.2 Host-LM628/629 Communication—The Busy Bit

Communication flow between the LM628/629 and its host is controlled by using a busy bit, bit 0, in the Status Byte. The busy bit must be checked to be at logic 0 by the host before commands and data are issued or data is read. This includes between data byte pairs for commands with multiple words of data.

3.3 Loading the Trapezoidal Velocity Profile Generator

To initiate a motor move, trajectory generator values have to be input to the LM628/629 using the Load Trajectory Parameters, LTRJ, command. The command is followed by a trajectory control word which details the information to be loaded in subsequent data words. Table I gives the bit allocations, a bit is set to logic 1 to give the function shown.

TABLE I. Trajectory Control Word Bit Allocations

Bit Position	Function
Bit 15	Not Used
Bit 14	Not Used
Bit 13	Not Used
Bit 12	Forward Direction (Velocity Mode Only)
Bit 11	Velocity Mode
Bit 10	Stop Smoothly (Decelerate as Programmed)
Bit 9	Stop Abruptly (Maximum Deceleration)
Bit 8	Turn Off Motor (Output Zero Drive)
Bit 7	Not Used
Bit 6	Not Used
Bit 5	Acceleration Will Be Loaded
Bit 4	Acceleration Data Is Relative
Bit 3	Velocity Will Be Loaded
Bit 2	Velocity Data Is Relative
Bit 1	Position Will Be Loaded
Bit 0	Position Data Is Relative

Bits 0 to 5 determine whether any, all or none of the position, velocity or acceleration values are loaded and whether they are absolute values or values relative to those previously loaded. All trajectory values are 32-bit values, position values are both positive and negative. Velocity and acceleration are 16-bit integers with 16-bit fractions whose absolute value is always positive. When entering relative values ensure that the absolute value remains positive. The manual stop commands bits 8, 9 and 10 are intended to allow an unprogrammed stop in position mode, while a position move is in progress, perhaps by the demand of some external event, and to provide a method to stop in velocity mode. They do not specify how the motor will stop in position mode at the end of a normal position move. In position mode a programmed move will automatically stop with a deceleration rate equal to the acceleration rate at the target position. Setting a stop bit along with other trajectory parameters at the beginning of a move will result in no movement! Bits 8, 9 and 10 should only be set one at a time, bit 8 turns the motor off by outputting zero drive to the motor, bit 9 stops the motor at maximum deceleration by setting the target position equal to the current position and bit 10 stops the motor using the current user-programmed acceleration value. Bit 11 is set for operating in velocity mode and bit 12 is set for forward direction in velocity mode.

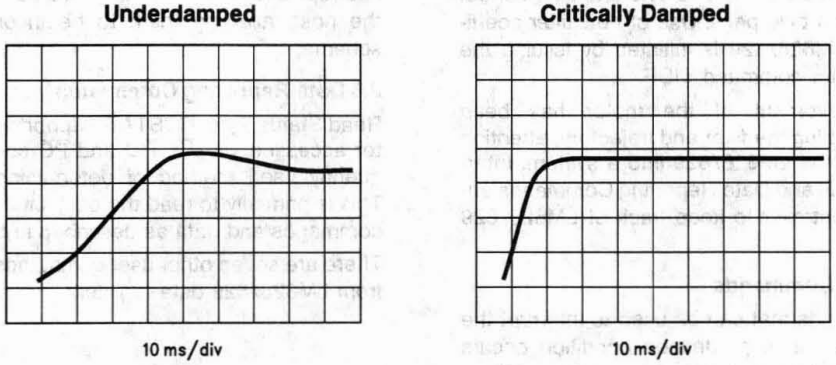


FIGURE 11. Position vs Time for 100 Count Step Input

Following immediately after the trajectory control word should be two 16-bit data words for each parameter specified to be loaded. These should be in the descending order of the trajectory control word bits, that is acceleration, velocity and position. They are written to the LM628/629 as two pairs of data bytes in most to least significant byte order. The busy bit should be checked between the command byte and the data byte pair forming the trajectory control word and the individual data byte pairs of the data. The Start command, STT, transfers the loaded trajectory data into the working registers of the double buffered scheme to initiate movement of the motor. This buffering allows any parameter, except acceleration, to be updated while the motor is moving by loading data with the LTRJ command and to be later executed by using the STT command.

New values of acceleration can be loaded with LTRJ while the motor is moving, but cannot be executed by the STT command until the trajectory has completed or the drive to the motor is turned off by using bit 8 of the trajectory control word. If acceleration has been changed and STT is issued while the drive to the motor is still present, a command error interrupt will be generated and the command ignored. Separate pairs of LTRJ and STT commands should be issued to first turn the motor off and then update acceleration. System operation when changing acceleration while the motor is moving, but with the drive removed, is discussed in Section 4.5.1.

3.4 Loading PID Filter Coefficients

PID filter coefficients are loaded using the Load Filter Parameters, LFIL, command and are the proportional coefficient k_p, derivative coefficient k_d and integral coefficient k_i. Associated with k_i, an integration limit, il, has to be loaded. This constrains the magnitude of the integration term of the PID filter to the il value, see Section 4.4.2. Associated with the derivative coefficient, a derivative sample rate can be chosen from $2048/f_{CLK}$ to $(2048 \times 256)/f_{CLK}$ in steps of $2048/f_{CLK}$, see Section 4.4.1.

The first pair of data bytes following the LFIL command byte form the filter control word. The most significant byte sets the derivative sample rate, the fastest rate, $2048/f_{CLK}$, being hex'00' the slowest rate $(2048 \times 256)/f_{CLK}$ being hex'FF'. The lower four bits of the least significant byte tell the LM628/629 which of the coefficients is going to be loaded, bit 3 is k_p, bit 2 is k_i, bit 1 is k_d and bit 0 is il. Each filter coefficient and the integration limit can range in value from hex'0000' to '7FFF', positive only. If all coefficient values are loaded then ten bytes of data, including the filter control word, will follow the LFIL command. Again the busy bit has to be checked between the command byte and filter control word and between data byte pairs. Use of new filter coefficient values by the LM628/629 is initiated by issuing the single byte Update Filter command, UDF.

When controlled movement of the motor has been achieved, by programming the filter and trajectory, attention turns to incorporating the LM628/629 into a system. Interrupt Control Commands and Data Reporting Commands enable the host microcontroller to keep track of LM628/629 activity.

3.5 Interrupt Control Commands

There are five commands that can be used to interrupt the host microcontroller when a predefined condition occurs and two commands that control interrupt operation. When the LM628/629 is programmed to interrupt its host, the event which caused this interrupt can be determined from bits 1 to 6 of the Status Byte (additionally bit 0 is the busy bit and bit 7 indicates that the motor is off). All the Interrupt Control commands are executable during motion.

The Mask Interrupts command, MSKI, is used to tell LM628/629 which of bits 1 to 6 will interrupt the host through use of interrupt mask data associated with the command. The data is in the form of a data byte pair, bits 1–6 of the least significant byte being set to logic 1 when an interrupt source is enabled. The Reset Interrupts command, $\overline{\text{RSTI}}$, resets interrupt bits in the Status Byte by sending a data byte pair, the least significant byte having logic 0 in bit positions 1 to 6 if they are to be reset.

Executing the Set Index Position command, SIP, causes bit 3 of the status byte to be set when the absolute position of the next index pulse is recorded in the index register. This can be read with the command, Read Index Position, RDIP.

Executing either Load Position Error for Interrupt, LPEI, or Load Position Error for Stopping, LPES, commands, sets bit 5 of the Status Byte when a position error exceeding a specified limit occurs. An excessive position error can indicate a serious system problem and these two commands give the option when this occurs of either interrupting the host or stopping the motor and interrupting the host. The excessive position is specified following each command by a data byte pair in most to least significant byte order.

Executing either Set Break Point Absolute, SBPA, or Set Break Point Relative, SBPR, commands, sets bit 6 of the status byte when either the specified, absolute or relative, breakpoint respectively is reached. The data for SBPA can be the full position range (hex'C0000000' to '3FFFFFFF') and is sent in two data byte pairs in most to least significant byte order. The data for the Set Breakpoint Relative command is also of two data byte pairs, but its value should be such that when added to the target position it remains within the absolute position range. These commands can be used to signal the moment to update the on-going trajectory or filter coefficients. This is achieved by transferring data from the primary registers, previously loaded using LTRJ or LFIL, to working registers, using the STT or UDF commands.

Interrupt bits 1, 2 and 4 of the Status Byte are not set by executing interrupt commands but by events occurring during LM628/629 operation as follows. Bit 1 is the command error interrupt, bit 2 is the trajectory complete interrupt and bit 4 is the wraparound interrupt. These bits are also masked and reset by the MSKI and $\overline{\text{RSTI}}$ commands respectively. The Status Byte still indicates the condition of interrupt bits 1–6 when they are masked from interrupting the host, allowing them to be incorporated in a polling scheme.

3.6 Data Reporting Commands

Read Status Byte, RDSTAT, supported by a hardware register accessed via $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{PS}}$ control, is the most frequently used method of determining LM628/629 status. This is primarily to read the busy bit 0 while communicating commands and data as described in Section 3.2.

There are seven other user commands which can read data from LM628/629 data registers.

The Read Signals Register command, RDSIGS, returns a 16-bit data word to the host. The least-significant byte repeats the RDSTAT byte except for bit 0 which indicates that a SIP command has been executed but that an index pulse has not occurred. The most significant byte has 6 bits that indicate set-up conditions (bits 8, 9, 11, 12, 13 and 14). The other two bits of the RDSIGS data word indicate that the trajectory generator has completed its function, bit 10, and that the host interrupt output (Pin 17) has been set to logic 1, bit 15. Full details of the bit assignments of this command can be found in the data sheet.

The Read Index Position, RDIP, command reads the position recorded in the 32 bits of the index register in four data bytes. This command, with the SIP command, can be used to acquire a home position or successive values. These could be used, for example, for gross error checking.

Both on-going 32-bit position inputs to the summing junction can be read. Read desired position, RDDP, reads the current desired position the demand or "set point input" from the trajectory generator and Read Real Position, RDRP, reads the current actual position of the motor.

Read Desired Velocity, RDDV, reads the current desired velocity used to calculate the desired position profile by the trajectory generator. It is a 32-bit value containing integer and fractional velocity information. Read Real Velocity, RDRV, reads the instantaneous actual velocity and is a 16-bit integer value.

Read Integration-Term Summation Value, RDSUM, reads the accumulated value of the integration term. This is a 16-bit value ranging from zero to the current, il, integration limit value.

3.7 Software Example

The following example shows the flow of microcontroller commands needed to get the LM628/629 to control a simple motor move. As it is non-specific to any microcontroller pseudo commands $\overline{WR}$,XXXXH and RD,XXXXH with hex immediate data will be used to indicate read and write operations respectively by the host to and from the LM628/629. Decisions use IF..THEN..ELSE. BUSY is a user routine to check the busy bit in the Status Byte, WAIT is a user routine to wait 1.5 ms after hardware reset.

```
LABEL     MNEMONIC          :REMARK
Initialization:
          WAIT              :Routine to wait 1.5 ms after reset.
          RDSTAT            :Check correct RESET operation by reading the
                            :Status Byte. This should be either hex'84' or 'C4'
          IF Status byte not equal hex'84' or 'C4' THEN repeat
          hardware RESET
                            :Make decision concerning validity of RESET
```

Optionally the Reset can be further checked for correct operation as follows. It is useful to include this to reset all interrupt bits in the Status Byte before further action:

```
          MSKI              :Mask interrupts
          BUSY              :Check busy bit 0 routine
          WR,0000H          :Host writes two zero bytes of data to
                            :LM628/629. This mask disables all interrupts.
          BUSY              :Check busy bit
          RSTI              :Reset Interrupts command
          BUSY              :Check busy bit
          WR,0000H          :Host writes two zero bytes of data to LM628/629
          RDSTAT            :Status byte should read either hex'80' or 'C0'
          IF Status byte not equal hex'80' or 'C0' THEN repeat
          hardware RESET
                            :
          IF Status Byte equal to hex'C0' THEN continue ELSE PORT
                            :
          BUSY              :Check busy bit
          RSTI              :Reset Interrupts
          BUSY              :Check busy bit
          WR,0000H          :Reset all interrupt bits
Set Output Port Size for a 12-bit DAC.
PORT      BUSY              :Check busy bit
          PORT12            :Sets LM628 output port to 12-bits
                             (Only for systems with 12-bit DAC)
```

```
Load Filter Parameters
        BUSY            :Check busy bit
        LFIL            :Load Filter Parameters command
        BUSY            :Check busy bit
        WR,0008H        :Filter Control Word
                        :    Bits 8 to 15 (MSB) set the derivative
                        :sample rate.
                        :    Bit 3    Loading kp data
                        :    Bit 2    Loading ki data
                        :    Bit 1    Loading kd data
                        :    Bit 0    Loading il data
                        :Choose to load kp only at maximum
                        :derivative sample rate then Filter Control
                        :Word = 0008H
        BUSY            :Check busy bit
        WR,0032H        :Choose kp = 50, load data byte pair MS
                        :byte first
Update Filter
        BUSY            :Check busy bit
        UDF             :
Load Trajectory Parameters
        BUSY            :Check busy bit
        LTRJ            :Load trajectory parameters command.
        BUSY            :Check busy bit
        WR,002AH        :Load trajectory control word:
                        :    See Table I
                        :Choose Position mode, and load absolute
                        :acceleration, velocity and position. Then
                        :trajectory control word = 002AH. This means
                        :6 pairs of data bytes should follow.
        BUSY            :Check busy bit
        WR,XXXXH        :Load Acceleration integer word MS byte first
        BUSY            :Check busy bit
        WR,XXXXH        :Load Acceleration fractional word MS byte first
        BUSY            :Check busy bit
        WR,XXXXH        :Load Velocity integer word MS byte first
        BUSY            :Check busy bit
        WR,XXXXH        :Load Velocity fractional word MS byte first
        BUSY            :Check busy bit
        WR,XXXXH        :Load Position MS byte pair first
        BUSY            :Check busy bit
        WR,XXXXH        :Load position LS byte pair
Start Motion
        BUSY            :Check busy bit
        STT             :Start command
Check for Trajectory complete.
        RDSTAT          :Check Status Byte bit 2 for trajectory
                        :complete
Busy bit check routine
BUSY    RDSTAT          :Read status byte
        If bit 0 is set THEN BUSY ELSE RETURN
        END
```

*Consult reference (5) for more information on programming the LM628/629.

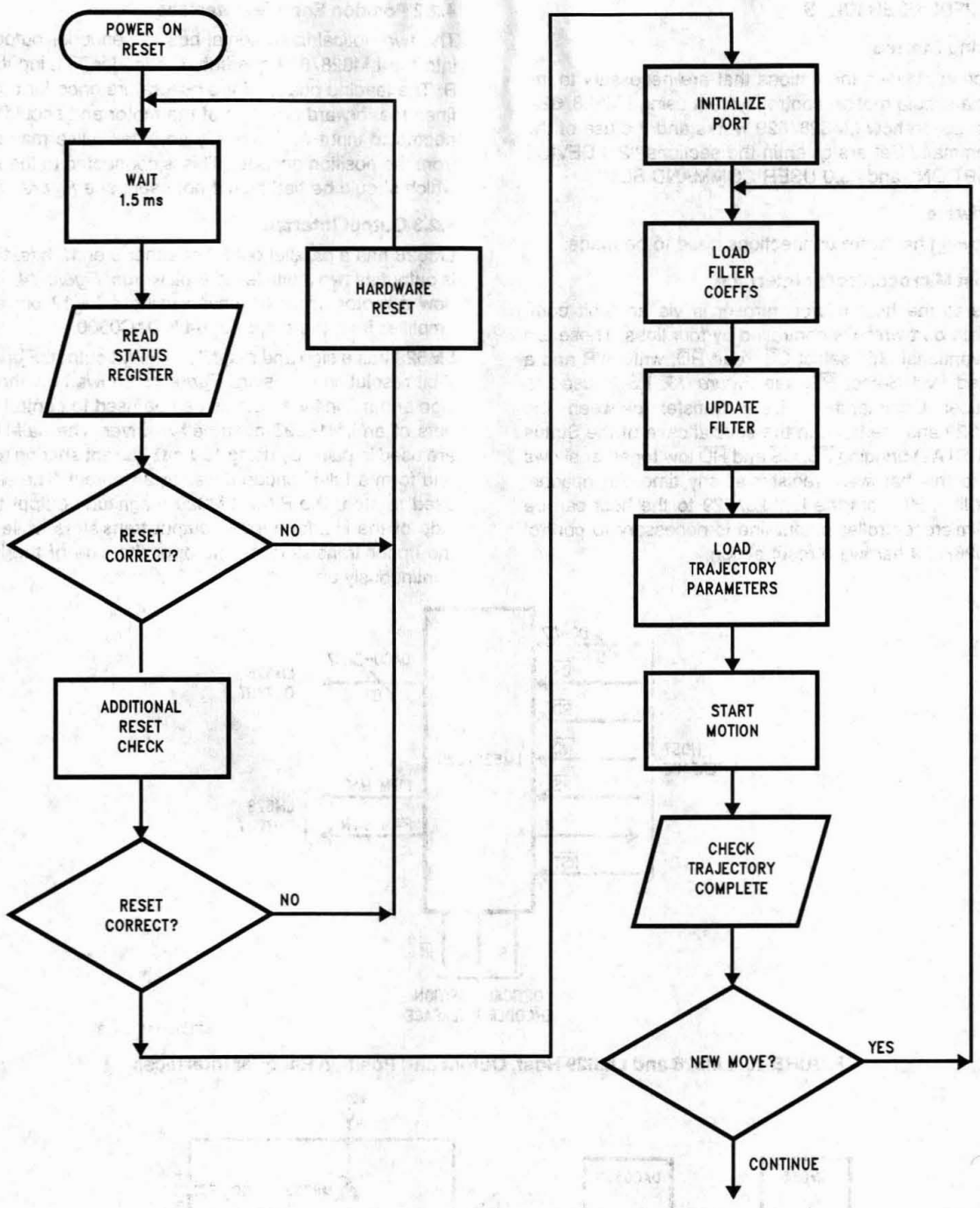


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FIGURE 12. Basic Software Flow

4.0 HELPFUL USER IDEAS

4.1 Getting Started

This section outlines the actions that are necessary to implement a simple motion control system using LM628/629. More details on how LM628/629 works and the use of the User Command Set are given in the sections "2.0 DEVICE DESCRIPTION" and "3.0 USER COMMAND SET".

4.2 Hardware

The following hardware connections need to be made:

4.2.1 Host Microcontroller Interface

Interface to the host microcontroller is via an 8-bit command/data port which is controlled by four lines. These are the conventional chip select $\overline{CS}$, read $\overline{RD}$, write $\overline{WR}$ and a line called Port Select $\overline{PS}$, see *Figure 13.* $\overline{PS}$ is used to select user Command or Data transfer between the LM628/629 and the host. In the special case of the Status Byte (RDSTAT) bringing $\overline{PS}$, $\overline{CS}$ and $\overline{RD}$ low together allows access to this hardware register at any time. An optional interrupt line, HI, from the LM628/629 to the host can be used. A microcontroller output line is necessary to control the LM628/629 hardware reset action.

4.2.2 Position Encoder Interface

The two optical incremental position encoder outputs feed into the LM628/629 quadrature decoder TTL inputs A and B. The leading phase of the quadrature encoder output defines the forward direction of the motor and should be connected to input A. Optionally an index pulse may be used from the position encoder. This is connected to the $\overline{IN}$ input, which should be tied high if not used, see *Figure 13.*

4.2.3 Output Interface

LM628 has a parallel output of either 8 or 12 bits, the latter is output as two multiplexed 6-bit words. *Figure 14* illustrates how a motor might be driven using a LM12 power linear amplifier from the output of 8-bit DAC0800.

LM629 has a sign and magnitude PWM output, *Figure 13,* of 7-bit resolution plus sign. *Figure 15* shows how the LM629 sign and magnitude outputs can be used to control the outputs of an LM18293 quad half-H driver. The half-H drivers are used in pairs, by using 100 mΩ current sharing resistors, and form a full-H bridge driver of 2A output. The sign bit is used to steer the PWM LM629 magnitude output to either side of the H-bridge lower output transistors while holding the upper transistors on the opposite side of the H-bridge continuously on.

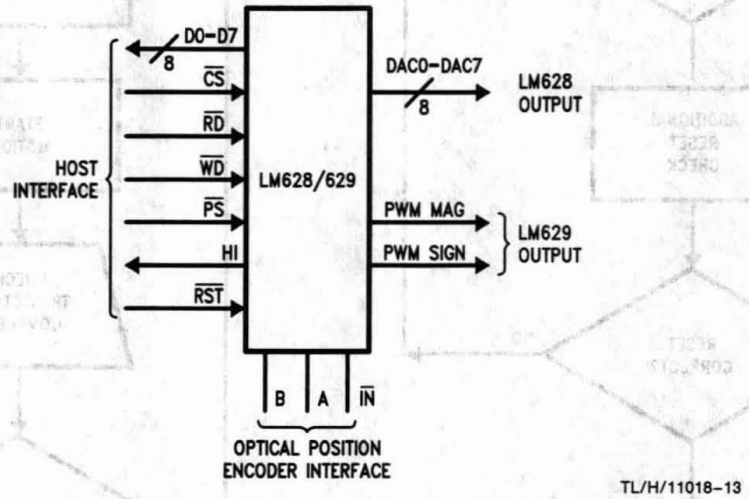


FIGURE 13. LM628 and LM629 Host, Output and Position Encoder Interfaces

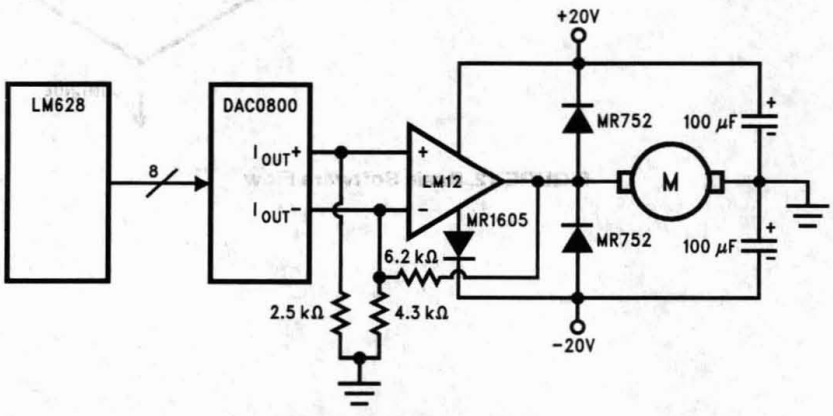
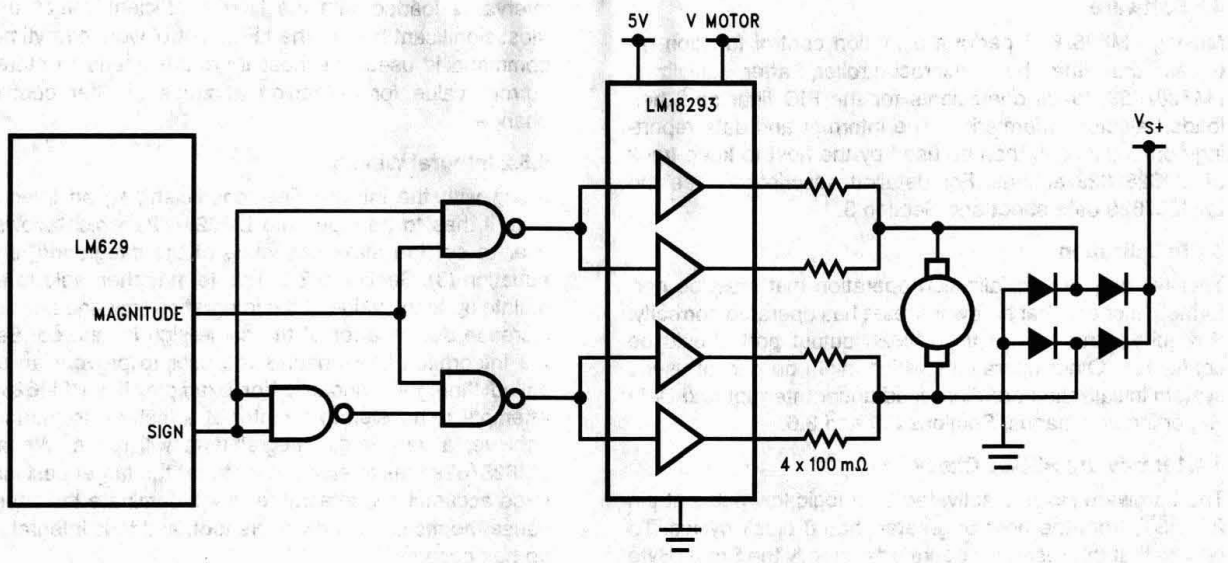


FIGURE 14. LM628 Example of Linear Motor Drive Using LM12



TL/H/11018–15

FIGURE 15. LM629 H-Bridge Motor Drive Example Using LM18293

4.3 Software

Making LM628/629 perform a motion control function requires that the host microcontroller, after initializing LM628/629, loads coefficients for the PID filter and then loads trajectory information. The interrupt and data reporting commands can then be used by the host to keep track of LM628/629 actions. For detailed descriptions see the LM628/629 data sheet and Section 3.

4.4 Initialization

There is only one initialization operation that must be performed; a check that hardware reset has operated correctly. If required, the size of the LM628 output port should be configured. Other operations which might be part of user's system initialization are discussed under Interrupt and Data Reporting commands, Sections 3.5 and 3.6.

4.4.1 Hardware RESET Check

The hardware reset is activated by a logic low pulse at pin 27, $\overline{RST}$, from the host of greater than 8 clock cycles. To ensure that this reset has operated correctly the Status Byte should be checked immediately after the reset pin goes high, it should read hex'00'. If the reset is successful this will change to hex'84' or 'C4' within 1.5 ms. If not, the hardware reset and check should be repeated. A further check can be used to make certain that a reset has been successful by using the Reset Interrupts command, RSTI. Before sending the RSTI, issue the Mask Interrupts command, MSKI, and mask data that disables all interrupts, this mask is sent as two bytes of data equaling hex'0000'. Then issue the RSTI command plus mask data that resets all interrupts, this equals hex'0000' and is again sent as two bytes. Do not forget to check the busy bit between the command byte and data byte pairs. When the chip has reset properly the status byte will change from hex'84' or 'C4' to hex'80' or 'C0'.

4.4.2 Initializing LM628 Output Port

Reset sets the LM628 output port size to 8 bits. If a 12-bit DAC is being used, then the output port size is set by the use of the PORT12 command.

4.4.3 Interrupt Commands

Optionally the commands which cause the LM628/629 to take action on a predefined condition (e.g., SIP, LPEI, LPES, SBPA and SBPR) can be included in the initialization, these are discussed under Interrupt Commands.

4.5 Performance Refinements

4.5.1 Derivative Sample Rate

The derivative sample interval is controllable to improve the stability of low velocity, high inertia loads. At low speeds, when fractional counts for velocity are used, the integer position counts, desired and actual, only change after several sample intervals of the LM628/629 ($2048/f_{CLK}$). This means that for sample intervals between integer count changes the error voltage will not change for successive samples. As the derivative term, k_d, multiplies the difference betweeen the previous and current error values, if the derivative sample interval is the same as the sample interval, several consecutive sample intervals will have zero derivative term and hence no damping contribution. Lengthening the derivative sample interval ensures a more constant derivate term and hence improved stability. Derivative sample interval is loaded with the filter coefficient values as the most significant byte of the LFIL control word everytime the command is used, the host therefore needs to store the current value for re-loading at times of filter coefficient change.

4.5.2 Integral Windup

Along with the integral filter coefficient, k_i, an integration limit, il, has to be input into LM628/629 which allows the user to set the maximum value of the integration term of equation (3), Section 5.2.2. This term is then able to accumulate up to the value of the integration limit and any further increase due to error of the same sign is ignored. Setting the integration limit enables the user to prevent an effect called "Integral Windup". For example, if an LM628/629 attempts to accelerate a motor at a faster rate than it can achieve, a very large integral term will result. When the LM628/629 tries to stop the motor at the target position the large accumulated integral term will dominate the filter and cause the motor to badly overshoot, and thus integral windup has occurred.

4.5.3 Profiles Other Than Trapezoidal

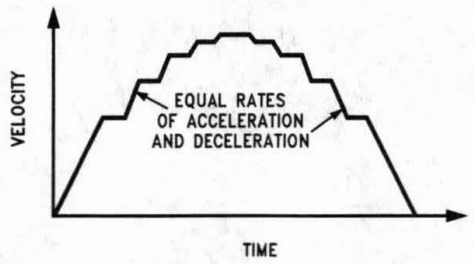


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FIGURE 16. Generating a Non-Trapezoidal Profile

If it is required to have a velocity profile other than trapezoidal, this can be accomplished by breaking the profile into small pieces each of which is part of a small trapezoid. A piecewise linear approximation to the required profile can then be achieved by changing the maximum velocity before the trapezoid has had time to complete, see *Figure 16.*

4.5.4 Synchronizing Axes

For controlling tightly coupled coordinated motion between multiple-axes, synchronization is required. The best possible synchronization that can be achieved between multiple LM628/629 is within one sample interval, ($2048/f_{CLK}$, 256 μs for an 8 MHz clock, 341 μs for a 6 MHz clock). This is achieved by using the pipeline feature of the LM628/629 where all controlled axes are loaded individually with trajectory values using the LTRJ command and then simultaneously given the start command STT. PID filter coefficients can be updated in a similar manner using LFIL and UDF commands.

4.6 Operating Constraints

4.6.1 Updating Acceleration on the Fly

Whereas velocity and target position can be updated while the motor is moving, on the "fly", the algorithm described in Section 2.5 prevents this for acceleration. To change acceleration while the motor is moving in mid-trajectory the motor off command has to be issued by setting LTRJ command bit 8. Then the new acceleration can be loaded, again using the

LTRJ command. When the start command STT is issued the motor will be energized and the trajectory generator will start generating a new profile from the actual position when the STT command was issued. In doing this the trajectory generator will assume that the motor starts from a stationary position in the normal way. If the motor has sufficient inertia and is still moving when the STT command is issued then the control loop will attempt to bring the motor on to the new profile, possibly with a large error value being input to the PID filter and a consequential saturated output until the motor velocity matches the profile. This is a classic case of overload in a feedback system. It will operate in an open loop manner until the error input gets within controllable bounds and then the feedback loop will close. Performance in this situation is unpredictable and application specific. LM628/629 was not intentionally designed to operate in this way.

4.6.2 Command Update Rate

If an LM628/629 is updated too frequently by the host it will not keep up with the commands given. The LM628/629 aborts the current trajectory calculation when it receives a new STT command, resulting in the output staying at the value of the previous sample. For this reason it is recommended that trajectory is not updated at a greater rate than once every 10 ms.

5.0 THEORY

5.1 PID Filter

5.1.1 PID Filter in the Continuous Domain

The LM628/629 uses a PID filter as the loop compensator, the expression for the PID filter in the continuous domain is:

$$H(s) = K_p + K_i/s + K_d s \quad (1)$$

Where K_p = proportional coefficient
K_i = integral coefficient
K_d = derivative coefficient

5.1.2 PID Filter Bode Plots

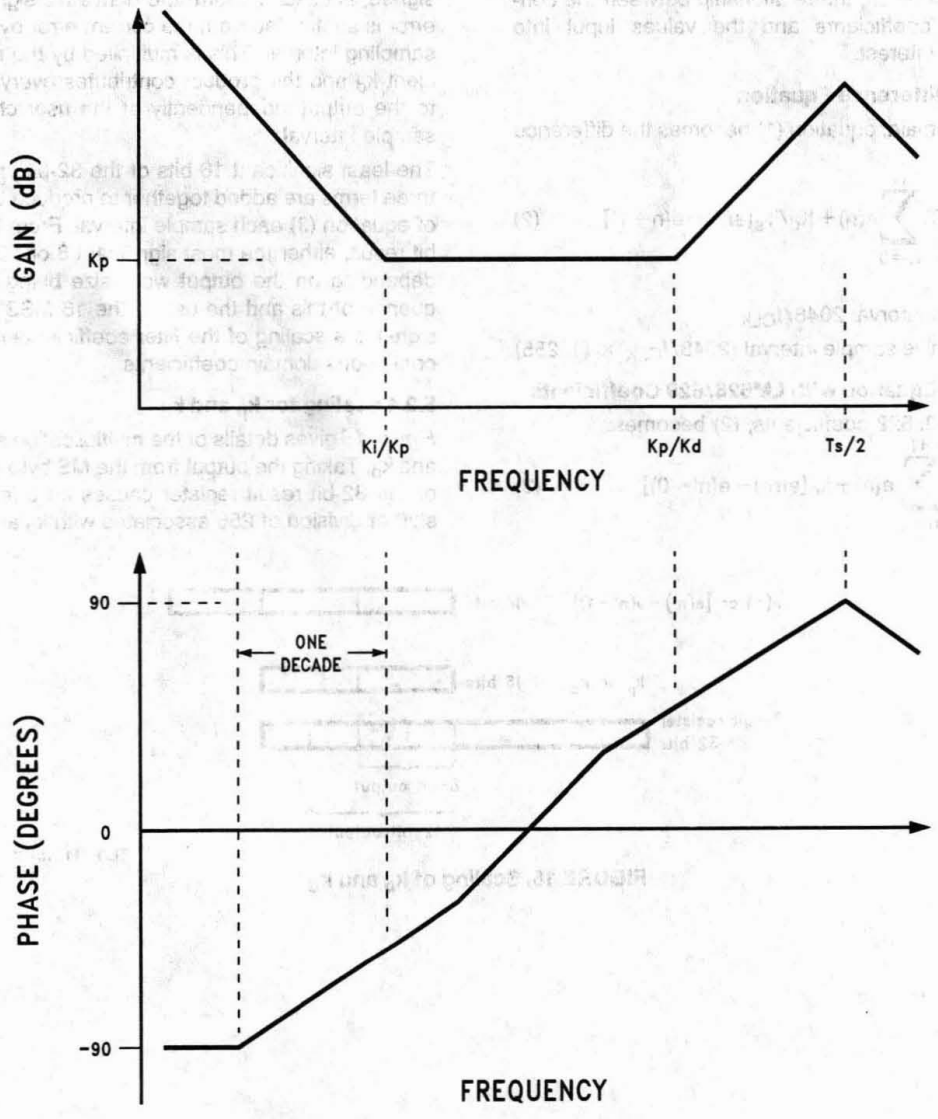

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FIGURE 17. Bode Plots of PID Transfer Function

The Bode plots for this function (shown in *Figure 17*) show the effect of the individual terms of equation (1). The proportional term, K_p provides adjustment of proportional gain. The derivative term K_d increases the system bandwidth but more importantly adds leading phase shift to the control loop at high frequencies. This improves stability by counteracting the lagging phase shift introduced by other control loop components such as the motor. The integral term, K_i, provides a high DC gain which reduces static errors, but introduces a lagging phase shift at low frequencies. The relative magnitudes of K_d, K_i and loop proportional gain have to be adjusted to achieve optimum performance without introducing instability.

5.2 PID Filter Coefficient Scaling Factors for LM628/629

While the easiest way to determine the PID filter coefficient k_p, k_d, and k_i values is to use tuning as described in Section 2.11, some users may want to use a more theoretical approach to at least find initial starting values before fine tuning. As very often this analysis is performed in the continuous (s) domain and transformed into the discrete digital domain for implementation, the relationship between the continuous domain coefficients and the values input into LM628/629 is of interest.

5.2.1 PID Filter Difference Equation

In the discrete domain, equation (1) becomes the difference equation:

$$u(n) = K_p e(n) + K_i T \sum_{n=0}^{N} e(n) + K_d / T_s [e(n) - e(n-1)] \qquad (2)$$

Where:

T is the sample interval $2048/f_{CLK}$

T_s is the derivative sample interval ($2048/f_{CLK} \times (1..255)$

5.2.2 Difference Equation with LM628/629 Coefficients

In terms of LM628/629 coefficients, (2) becomes:

$$u(n) = k_p e(n) + k_i \sum_{n=0}^{N} e(n) + k_d [e(n') - e(n'-0)] \qquad (3)$$

Where:

k_p, k_i and k_d are the discrete-time LM628/629 coefficients

e(n) is the position error at sample time n

n′ indicates sampling at the derivative sampling rate.

The error signal e(n) [or e(n′)] is a 16-bit number from the output of the summing junction and is the input to the PID filter. The 15-bit filter coefficients are respectively multiplied by the 16-bit error terms as shown in equation (3) to produce 32-bit products.

5.2.3 LM628/629 PID Filter Output

The proportional coefficient k_p is multiplied by the error signal directly. The error signal is continually summed at the sample rate to previously accumulated errors to form the integral signal and is maintained to 24 bits. To achieve a more usable range from this term, only the most significant 16 bits are used and multiplied by the integral coefficient, k_i. The absolute value of this product is compared with the integration limit, il, and the smallest value, appropriately signed, is used. To form the derivative signal, the previous error is subtracted from the current error over the derivative sampling interval. This is multiplied by the derivative coefficient k_d and the product contributes every sample interval to the output independently of the user chosen derivative sample interval.

The least significant 16 bits of the 32-bit products from the three terms are added together to produce the resulting u(n) of equation (3) each sample interval. From the PID filter 16-bit result, either the most significant 8 or 12 bits are output, depending on the output word size being used. A consequence of this and the use of the 16 MSB's of the integral signal is a scaling of the filter coefficients in relation to the continuous domain coefficients.

5.2.4 Scaling for k_p and k_d

Figure 18 gives details of the multiplication and output for k_p and k_d. Taking the output from the MS byte of the LS 16 bits of the 32-bit result register causes an effective 8-bit right-shift or division of 256 associated with k_p and k_d as follows:

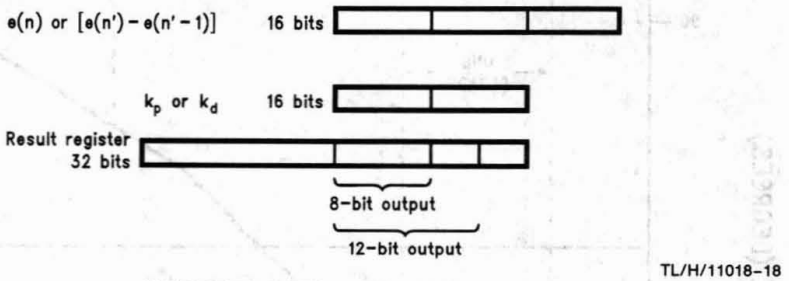

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FIGURE 18. Scaling of k_p and k_d

Result $= k_p \times e(n)/256 = K_p \times e(n)$.'. $k_p = 256 \times K_p$.

Similarly for k_d:

Result $= (k_d \times [e(n') - e(n'-1)])/256$

$= K_d/T_s \times e(n)$.'. $k_d = 256 \times K_d/T_s$

Where T_s is the derivative sampling rate.

5.2.5 Scaling for k_i

Figure 19 shows the multiplication and output for the integral term k_i. The use of a 24-bit register for the error terms summation gives further scaling:

Result $= k_i/256 \times > e(n)/256$

$= K_i \times T$.'. $k_i = 65536\ K_i \times T$.

Where T is the sampling interval $2048/f_{CLK}$.

For a 12-bit output the factors are:

$k_p = 16 \times K_p$, $k_d = 16 \times K_d/T_s$ and $k_i = 4096\ K_i \times T$.

If the 32-bit result register overflows into the most significant 16-bits as a result of a calculation, then all the lower bits are set high to give a predictable saturated output.

5.3 An Example of a Trajectory Calculation

Problem: Determine the trajectory parameters for a motor move of 500 revolutions in 1 minute with 15 seconds of acceleration and deceleration respectively. Assume the optical incremental encoder used has 500 lines.

The LM628/629 quadrature decoder gives four counts for each encoder line giving 2000 counts per revolution in this example. The total number of counts for this position move is 2000 × 500 = 1,000,000 counts.

By definition, average velocity during the acceleration and deceleration periods, from and to zero, is half the maximum velocity. In this example, half the total time to make the move (30 seconds) is taken by acceleration and deceleration. Thus in terms of time, half the move is made at maximum velocity and half the move at an average velocity of half this maximum. Therefore, the combined distance traveled during acceleration and deceleration is half that during

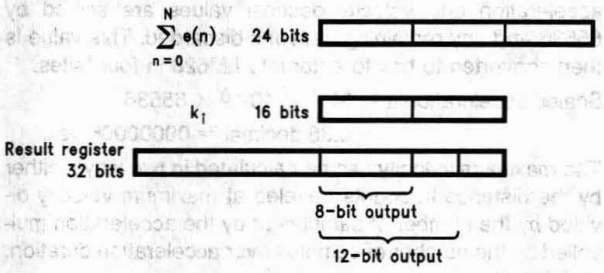

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FIGURE 19. Scaling for k_i

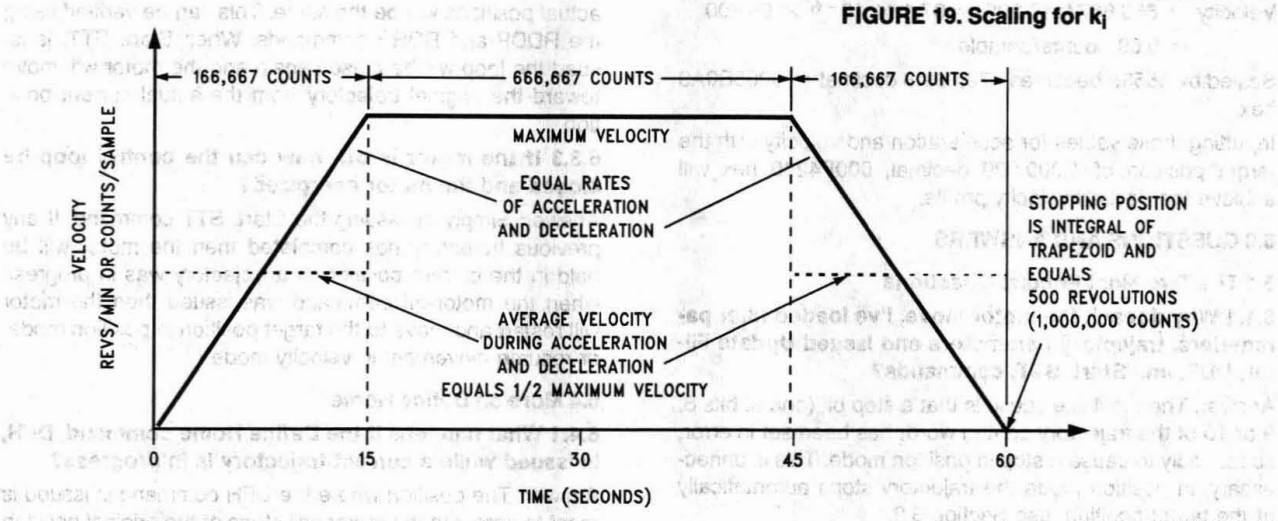

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FIGURE 20. Trajectory Calculation Example Profile

maximum velocity or ⅓ of the total, or 333,333 counts. Acceleration and deceleration takes 166,667 counts respectively.

The time interval used by the LM628/629 is the sample interval which is 256 μs for a f_{CLK} of 8 MHz.

The number of sample periods in 15 seconds = 15s/256 μs = 58,600 samples

Remembering that distance s = $at^2/2$ is traveled due to acceleration 'a' and time 't'.

Therefore acceleration a = $2S/t^2$

$= 2 \times 166{,}667/58{,}600$

$= 97.1 \times 10^{-6}$ counts/sample^2

Acceleration and velocity values are entered into LM628/629 as a 32-bit integer double-word but represents a 16-bit integer plus 16-bit fractional value. To achieve this acceleration and velocity decimal values are scaled by 65536 and any remaining fractions discarded. This value is then converted to hex to enter into LM628 in four bytes.

Scaled acceleration a = $97.1 \times 10^{-6} \times 65536$

= 6.36 decimal = 00000006 hex.

The maximum velocity can be calculated in two ways, either by the distance in counts traveled at maximum velocity divided by the number of samples or by the acceleration multiplied by the number of samples over acceleration duration, as follows:

Velocity = $666{,}667/117{,}200 = 97.1 \times 10^{-6} \times 58{,}600$

= 5.69 counts/sample

Scaled by 65536 becomes 372,899.8 decimal = 0005B0A3 hex.

Inputting these values for acceleration and velocity with the target position of 1,000,000 decimal, 000F4240 hex will achieve the desired velocity profile.

6.0 QUESTIONS AND ANSWERS

6.1 The Two Most Popular Questions

6.1.1 Why doesn't the motor move, I've loaded filter parameters, trajectory parameters and issued Update Filter, UDF, and Start, STT, commands?

Answer: The most like cause is that a stop bit (one of bits 8, 9 or 10 of the trajectory control word) has been set in error, supposedly to cause a stop in position mode. This is unnecessary, in position mode the trajectory stops automatically at the target position, see Section 3.3.

6.1.2 Can acceleration be changed on the fly?

Answer: No, not directly and a command error interrupt will be generated when STT is issued if acceleration has been changed. Acceleration can be changed if the motor is turned off first using bit 8 of the Load Trajectory Parameter, LTRJ, trajectory control word, see Section 4.6.1.

6.2.More on Acceleration Change

6.2.1 What happens at restart if acceleration is changed with the motor drive off and the motor is still moving?

Answer: The trajectory generation starting position is the actual position when the STT command is issued, but assumes that the motor is stationary. If the motor is moving the control loop will attempt to bring the motor back onto an accelerating profile, producing a large error value and less than predictable results. The LM628/629 was not designed with the intention to allow acceleration changes with moving motors.

6.2.2 Is there any way to change acceleration?

Answer: Acceleration change can be simulated by making many small changes of maximum velocity. For instance if a small velocity change is loaded, using LTRJ and STT commands, issuing these repeatedly at predetermined time intervals will cause the maximum velocity to increment producing a piecewise linear acceleration profile. The actual acceleration between velocity increments remains the same.

6.3 More on Stop Commands

6.3.1 What happens if the on-going trajectory is stopped by setting LTRJ control word bits 9 or 10, stop abruptly or stop smoothly, and then restarted by issuing Start, STT?

Answer: While stopped the motor position will be held by the control loop at the position determined as a result of issuing the stop command. Issuing STT will cause the motor to restart the trajectory toward the original target position with normal controlled acceleration.

6.3.2 What happens if the on-going trajectory is stopped by setting LTRJ control word bit 8, motor-off?

Answer: The LM628's DAC output is set to mid-scale, this puts zero volts on the motor which will still have a dynamic braking effect due to the commutation diodes. The LM629's PWM output sets the magnitude output to zero with a similar effect. If the motor freewheels or is moved the desired and actual positions will be the same. This can be verified using the RDDP and RDRP commands. When Start, STT, is issued the loop will be closed again and the motor will move toward the original trajectory from the actual current position.

6.3.3 If the motor is off, how can the control loop be closed and the motor energized?

Answer: Simply by issuing the Start, STT command. If any previous trajectory has completed then the motor will be held in the current position. If a trajectory was in progress when the motor-off command was issued then the motor will restart and move to the target position in position mode, or resume movement in velocity mode.

6.4 More on Define Home

6.4.1 What happens if the Define Home command, DFH, is issued while a current trajectory is in progress?

Answer: The position where the DFH command is issued is reset to zero, but the motor still stops at the original position commanded, i.e., the position where DFH is issued is substracted from the original target position.

6.4.2 Does issuing Define Home, DFH, zero both the trajectory and position register.

Answer: Yes, use Read Real Position, RDRP, and Read Desired Position, RDDP to verify.

6.5 More on Velocity

6.5.1 Why is a command error interrupt generated when inputting negative values of relative velocity?

Answer: Because the negative relative velocity would cause a negative absolute velocity which is not allowed. Negative absolute values of velocity imply movement in the negative direction which can be achieved by inputting a negative po-

sition value or in velocity mode by not setting bit 12. Similarly negative values of acceleration imply deceleration which occurs automatically at the acceleration rate when the LM628/629 stops the motor in position mode or if making a transition from a higher to a lower value of velocity.

6.5.2 What happens in velocity (or position) mode when the position range is exceeded?

Answer: The position range extends from maximum negative position hex'C0000000' to maximum positive position hex'3FFFFFFF' using a 32-bit double word. Bit 31 is the direction bit, logic 0 indicates forward direction, bit 30 is the wraparound bit used to control position over-range in velocity (or position) mode.

When the position increases past hex'3FFFFFFF' the wraparound bit 30 is set, which also sets the wraparound bit in the Status byte bit 4. This can be polled by the host or optionally used to interrupt the host as defined by the MSKI commands. Essentially the host has to manage wraparound by noting its occurrence and resetting the Status byte wraparound bit using the RSTI command. When the wraparound bit 30 is set in the position register so is the direction bit. This means one count past maximum positive position hex'3FFFFFFF' moves the position register onto the maximum negative position hex'C0000000'. Continued increase in positive direction causes the position register to count up to zero and back to positive values of position and on toward another wraparound.

Similarly when traveling in a negative direction, using two's complement arithmetic, position counts range from hex'FFFFFFF' (−1 decimal) to the maximum negative position of hex'C0000000'. One more negative count causes the position register to change to hex'3FFFFFFF', the maximum positive position. This time the wraparound bit 30 is reset, causing the wraparound bit 4 of the status byte to be set. Also the direction bit 31 is reset to zero. Further counts in the negative direction cause the position register to count down to zero as would be expected. With management there is no reason why absolute position should be lost, even when changing between velocity and position modes.

6.6 More on Use of Commands

6.6.1 If filter parameter and trajectory commands are pipelined for synchronization of axes, can the Update Filter, UDF, and Start, STT, commands be issued consecutively?

Answer: Yes.

6.6.2 Can commands be issued between another command and its data?

Answer: No.

6.6.3 What is the response time of the set breakpoint commands, SBPA and SBPR?

Answer: There is an uncertainty of one sample interval in the setting of the breakpoint bit 6 in the Status Byte in response to these commands.

6.6.4 What happens when the Set Index Position, SIP, command is issued?

Answer: On the next occurrence of all three inputs from the position encoder being low the corresponding position is loaded into the index register. This can be read with the Read Index Position command, RDIP. Bit 0 of the Read Signals register, shows when an SIP command has been issued but the index position has not yet been acquired. RDSIGS command accesses the Read Signals Register.

6.6.5 What happens if the motor is not able to keep up with the specified trajectory acceleration and velocity values?

Answer: A large, saturated, position error will be generated, and the control loop will be non-linear. The acceleration and velocity values should be set within the capability of the motor. Read Desired and Real Position commands, RDDP and RDRP can be used to determine the size of the error. The Load Position Error commands, for either host Interrupt or motor Stopping, LPEI and LPES, can be used to monitor the error size for controlled action where safety is a factor.

6.6.6 When is the command error bit 1 in the Status Byte set?

Answer:

a) When an acceleration change is attempted when the motor is moving and the drive on.

b) When loading a relative velocity would cause a negative absolute velocity.

c) Incorrect reading and writing operations generally.

6.6.7 What does the trajectory complete bit 2 in the Status Byte indicate?

Answer: That the trajectory loaded by LTRJ and initiated by STT has completed. The motor may or may not be at this position. Bit 2 is also set when the motor stop commands are executed and completed.

6.6.8 What do the specified minimum and maximum values of velocity mean in reality?

Answer: Assume a 500 line encoder = 1/2000 revs/count is used.

The maximum LM628/629 velocity is 16383 counts/sample and for a 8 MHz clock the LM628/629 sample rate is 3.9k samples/second, multiplying these values gives 32k revs/second or 1.92M rpm.

The maximum encoder rate is 1M counts/second multiplied by 1/2000 revs/count gives 500 revs/second or 30k rpm. The encoder capture rate therefore sets the maximum velocity limit.

The minimum LM628/629 velocity is 1/65536 counts/sample (one fractional count), multiplying this value by the sample rate and encoder revs/count gives 30×10^{-6} revs/second or 1.8×10^{-3} rpm.

The LM628 provides no limitation to practical values of velocity.

6.6.9 How long will it take to get to position wraparound in velocity mode traveling at 5000 rpm with a 500 line encoder?

Answer: 107 minutes.

7.0 REFERENCES AND FURTHER READING

1. LM628/LM629 Precision Motion Controller. Data sheet March 1989.
2. Automatic Control Systems. Benjamin C. Kuo. Fifth edition Prentice-Hall 1987.
3. DC Motors, Speed Controls, Servo Systems. Robbins & Myers/Electro Craft.
4. PID Algorithms and their Computer Implementation. D.W. Clarke. Institute of Measurement and Control, Trans. v. 6 No. 6 Oct/Dec 1984 86/178.
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LM78S40 Switching Voltage Regulator Applications

National Semiconductor
Application Note 711

CONTENTS

- Introduction
- Principle of Operation
- Architecture
- Analysis
- Design
- Inductor Design
- Transistor and Diode Selection
- Capacitor Selection
- EMI
- Design Equations

INTRODUCTION

In modern electronic systems, voltage regulation is a basic function required by the system for optimal performance. The regulator provides a constant output voltage irrespective of changes in line voltage, load requirements, or ambient temperature.

For years, monolithic regulators have simplified power-supply design by reducing design complexity, improving reliability, and increasing the ease of maintenance. In the past, monolithic regulator systems have been dominated by linear regulators because of relatively low cost, low external component count, excellent performance, and high reliability. However, limitations to applicability and performance of linear regulators can force the user to other more complex regulator systems, such as the switching regulator.

Because of improvements in components made especially for them, switching-regulated power supplies have proliferated during the past few years. The emergence of inexpensive, high-speed switching power transistors, low-loss ferrites for inductor cores, and low-cost LSI circuits containing all necessary control circuitry has significantly expanded the range of switching regulator application.

This application note describes a new integrated subsystem that contains the control circuitry, as well as the switching elements, required for constructing switching regulator systems *(Figure 1)*. The principle of operation is discussed, a complete system description provided, and the analysis and design of the basic configurations developed. Additional information concerning selection of external switching elements and design of the inductor is provided.

PRINCIPLE OF OPERATION

A D.C. power supply is usually regulated by some type of feedback circuit that senses any change in the D.C. output and develops a control signal to compensate for this change. This feedback maintains an essentially constant output.

In a monolithic regulator, the output voltage is sampled and a high-gain differential amplifier compares a portion of this voltage with a reference voltage. The output of the amplifier is then used to modulate the control element, a transistor, by varying its operating point within the linear region or between the two operating extremes, cutoff and saturation. When the pass transistor is operated at a point between cutoff and saturation, the regulator circuit is referred to as *linear* voltage regulator. When the pass transistor is operated only at cutoff or at saturation, the circuit is referred to as a *switching* regulator.

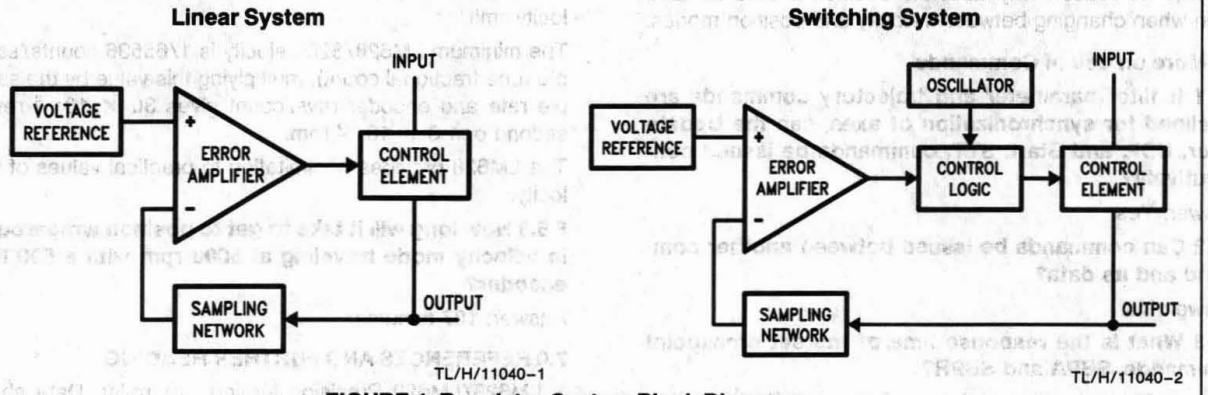


FIGURE 1. Regulator System Block Diagrams

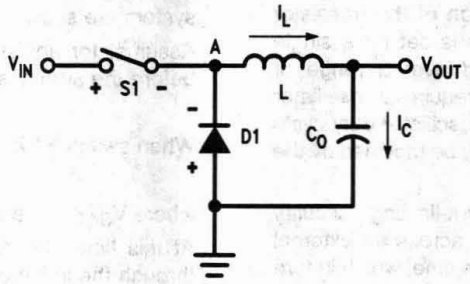
One advantage of the switching regulator over the more conventional linear regulator is greater efficiency, since cutoff and saturation modes are the two most efficient modes of operation. In the cutoff mode, there is a large voltage across the transistor but little current through it; in the saturation mode, the transistor has little voltage across it but a large amount of current. In either case, little power is wasted, most of the input power is transferred to the output, and efficiency is high. Regulation is achieved by varying the duty cycle that controls the average current transferred to the load. As long as this average current is equal to the current required by the load, regulation is maintained.

Besides high efficiency operation, another advantage of the switching regulator is increased application flexibility offered by output voltages that are less than, greater than, or of opposite polarity to the input voltage. *Figure 2* illustrates these three basic operating modes.

ARCHITECTURE

Each of the fundamental operating modes is built from the same set of functional blocks *(Figure 3)*. Additional functions are required for control and protection, but again, these functional blocks are common to each of the operational modes. The different modes are obtained by proper arrangement of these basic blocks.

Step-Down Configuration



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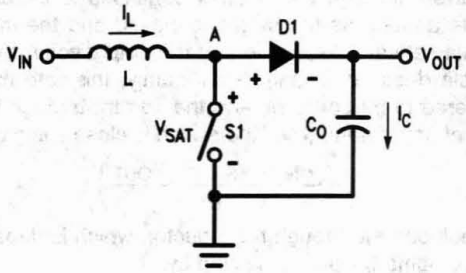
Step-Up Configuration



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Inverting Configuration

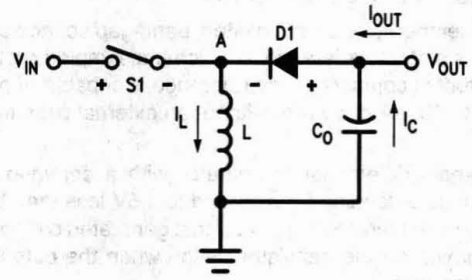

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FIGURE 2. Basic Operating Modes

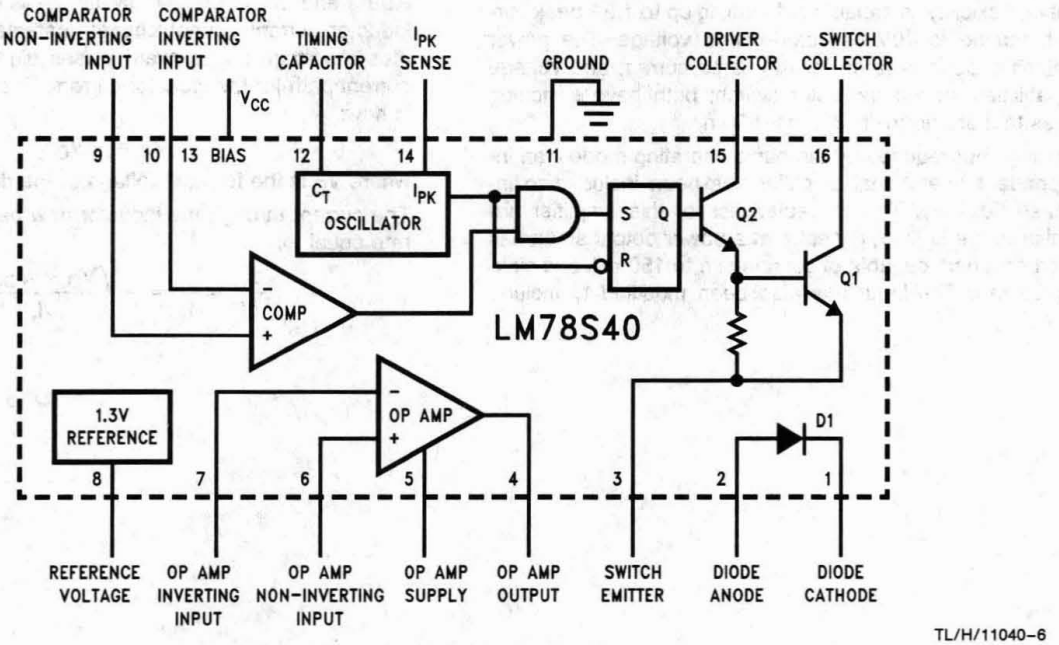

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FIGURE 3. Functional Block Diagram

For maximum design flexibility and minimum external part count, the LM78S40 was designed to include all of the fundamental building blocks in an uncommitted arrangement. This provides for a simple, cost-effective design of any switching regulator mode.

The functional blocks of the regulator, illustrated in *Figure 3,* are:

— Current-controlled oscillator
— Temperature-compensated current-limiting circuit
— Temperature-compensated voltage reference
— High-gain differential comparator
— Power switching circuit
— High-gain amplifier

The current-controlled oscillator generates the gating signals used to control the on/off condition of the transistor power switch. The oscillator frequency is set by a single external capacitor and may be varied over a range of 100 Hz to 100 kHz. Most applications require an oscillator frequency from 20 kHz to 30 kHz. The oscillator duty cycle (t_{on}/t_{off}) is internally fixed at 6:1, but may be modified by the current-limiting circuit.

The temperature-compensated, current-limiting circuitry senses the switching transistor current across an external resistor and may modify the oscillator on-time, which in turn limits the peak current. This provides protection for the switching transistor and power diode. The nominal activation voltage is 300 mV, and the peak current can be programmed by a single resistor R_{SC}.

A 1.3V temperature-compensated, band-gap voltage source provides a stable reference to which the sampled portion of the output is compared. The reference is capable of providing up to 10 mA of current without an external pass transistor.

A high-gain differential comparator with a common-mode input range extending from ground to 1.5V less than V_{CC} is used to inhibit the basic gating signal generated by the oscillator turning on the transistor switch when the output voltage is too high.

The transistor switch, in a Darlington configuration with the collectors and emitter brought out externally for maximum design flexibility, is capable of handling up to 1.5A peak current and up to 40V collector-emitter voltage. The power switching diode is rated for the same current and voltage capabilities as the transistor switch; both have switching times that are normally 300 ns–500 ns.

Although not required by the basic operating modes, an independent operational amplifier has been included to increase flexibility. The characteristics of this amplifier are similar to the LM741, except that a power output stage has been provided, capable of sourcing up to 150 mA and sinking 35 mA. The input has also been modified to include ground as part of the common-mode range. This amplifier may be connected to provide series pass regulation or a second output voltage, or configured to provide special functions for some of the more advanced applications.

The switching regulator can be operated over a wide range of power conditions, from battery power to high-voltage, high-current supplies. Low voltage operation down to 2.4V and low standby current, less than 2.5 mA at 5V, make it ideal for battery-powered systems. On the other end, high-voltage capability, up to 40V, and high-current capability, up to 1.5A peak current, offer an operating range unmatched by other switching systems.

ANALYSIS—STEP-DOWN OPERATION

Figure 2 illustrates the basic configuration for a step-down switching voltage regulator system. The waveforms for this system are shown in *Figure 4.*

Assume, for analysis, that the following condition is true: before the switch is turned on,

$$i_L = 0$$

When switch S1 is closed, the voltage at point A becomes:

$$V_A = V_{IN} - V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch.

At this time, the diode is reverse biased and the current through the inductor i_L is increasing at a rate equal to:

$$\frac{di}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT} - V_{OUT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch is closed and the inductor does not saturate. Assuming that the output voltage over a full cycle does not change significantly, this rate may be considered to be constant, and the current through the inductor at any instant, while the switch is closed, is given by:

$$i_L = \left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{L}\right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1, is given by:

$$I_{pk} = \left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{L}\right) t_{on}$$

At the end of the on-time, switch S1 is opened. Since the inductor current cannot change instantaneously, it generates a voltage that forward biases diode D1, providing a current path for the inductor current. The voltage at point A is now:

$$V_A = -V_D$$

where V_D is the forward voltage of the diode.

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\left(\frac{V_D + V_{OUT}}{L}\right)$$

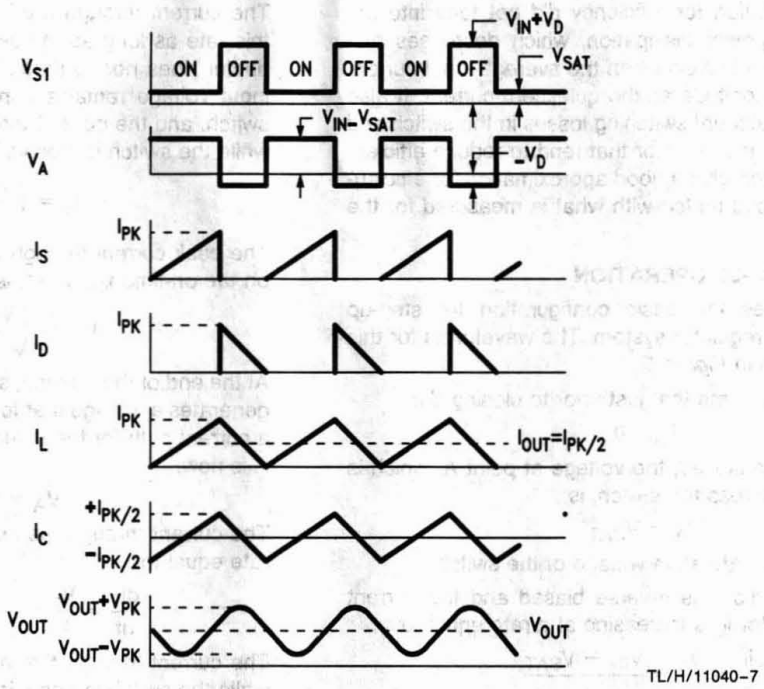


FIGURE 4. Waveforms for Step-Down Mode

The current through the inductor at any instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_D + V_{OUT}}{L}\right) t$$

Assuming that the current through the inductor reaches zero after the time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_D + V_{OUT}}{L}\right) t_{off}$$

which results in the following relationship between t_{on} and t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$$

In the above analysis, a number of assumptions were made. For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 4* (i_L waveform) shows that:

$$\left(\frac{I_{pk}}{2}\right) t_{on} + \left(\frac{I_{pk}}{2}\right) t_{off} = I_{OUT}\,(t_{on} + t_{off}),$$

$$\text{or } I_{pk} = 2\, I_{OUT}$$

For the average output voltage to remain constant, the average current through the inductor must equal the output current.

It was also assumed that the change (ripple) in the output voltage was small in comparison to the output voltage. The ripple voltage can be calculated from a knowledge of switching times, peak current and output capacitor size. *Figure 4* (i_C waveform) shows that:

$$V_{P\text{-}P} = \frac{\Delta Q}{C_O} = \frac{\frac{1}{2}\left(t_{on}\frac{I_{pk}}{4} + t_{off}\frac{I_{pk}}{4}\right)}{C_O} = \frac{I_{pk}\,(t_{on}/t_{off})}{8\,C_O}$$

The ripple voltage will be increased by the product of the output capacitor's equivalent series resistance (ESR) and i_C (though the two ripple terms do not directly add). Using large-value, low-ESR capacitors will minimize the ripple voltage, so the previous analysis will remain valid.

To calculate the efficiency of the system, n:

$$n = \frac{P_{OUT}}{P_{IN}}$$

The input power is given by:

$$P_{IN} = I_{IN}\, V_{IN}$$

The average input current can be calculated from the i_S waveform of *Figure 4*:

$$I_{IN(avg)} = \frac{t_{on}\left(\frac{I_{pk}}{2}\right)}{t_{on} + t_{off}} = I_{OUT}\left(\frac{t_{on}}{t_{on} + t_{off}}\right)$$

The output power is given by:

$$P_{OUT} = I_{OUT}\, V_{OUT}$$

Combining the above equations gives an expression for efficiency:

$$n = \left(\frac{V_{OUT}}{V_{OUT} + V_D}\right)\left(\frac{V_{IN} - V_{SAT} + V_D}{V_{IN}}\right)$$

As the forward drops in the diode and switch decrease, the efficiency of the system is improved. With variations in input voltage, the efficiency remains relatively constant.

The above calculation for efficiency did not take into account quiescent power dissipation, which decreases efficiency at low current levels when the average input current is of the same magnitude as the quiescent current. It also did not take into account switching losses in the switch and diode or losses in the inductor that tend to reduce efficiency. It does, however, give a good approximation for efficiency, providing a close match with what is measured for the system.

ANALYSIS—STEP-UP OPERATION

Figure 2 illustrates the basic configuration for step-up switching voltage regulator system. The waveforms for this system are shown in *Figure 5*.

To analyze, first assume that just prior to closing S1:

$$i_L = 0$$

When switch S1 is closed, the voltage at point A, which is also the voltage across the switch, is:

$$V_A = V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch.

At this time, the diode is reverse biased and the current through the inductor i_L is increasing at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch remains closed and the inductor does not saturate. This rate will be constant if the input voltage remains constant during the on-time of the switch, and the current through the inductor at any instant, while the switch is closed, is given by:

$$i_L = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1, is given by:

$$I_{PK} = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t_{on}$$

At the end of the on-time, switch S1 is opened. The inductor generates a voltage that forward biases diode D1, providing a current path for the inductor current. The voltage at point A is now:

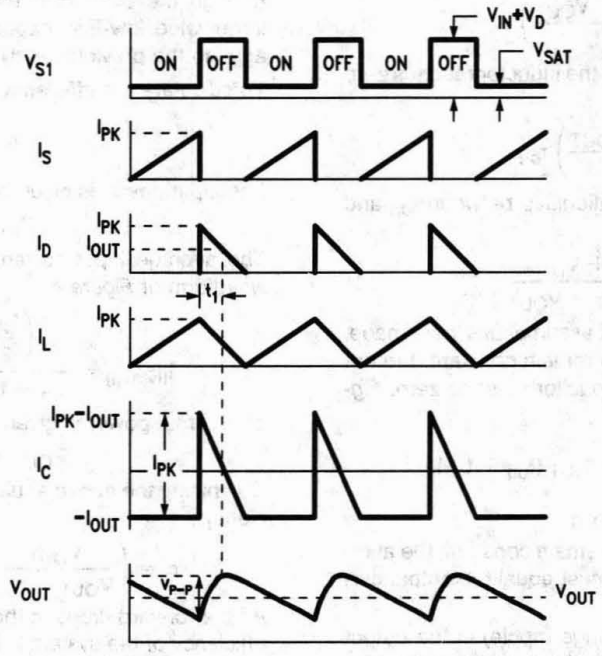
$$V_A = V_{OUT} + V_D$$

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\frac{V_{OUT} + V_D - V_{IN}}{L}$$

The current through the inductor and diode at any instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_{OUT} + V_D - V_{IN}}{L}\right) t$$



TL/H/11040–8

FIGURE 5. Waveforms for Step-Up Mode

Assuming that the current through the inductor reaches zero after the time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_{OUT} + V_D - V_{IN}}{L}\right) t_{off}$$

Thus, the relationship between t_{on} and t_{off} is given by:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}}$$

The above analysis assumes that the output voltage remains relatively constant. For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 5* (i_D waveform) shows that:

$$\left(\frac{I_{pk}}{2}\right) t_{off} = (t_{on} + t_{off})\, I_{OUT}$$

$$\text{or } I_{pk} = 2\, I_{OUT} \left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$$

Also for the average output voltage to remain constant, the average current through the diode must equal the output current. The ripple voltage can be calculated using *Figure 5* (i_D waveform) where:

$$t_1 = t_{off} - \left(\frac{I_{OUT}}{I_{pk}}\right) t_{off}$$

During time interval t_1, the output capacitor C_O charges from its minimum value to its maximum value. Therefore:

$$V_{P\text{-}P} = \frac{\Delta Q}{C_O} = \frac{1}{C_O}\left(\frac{I_{pk} + I_{OUT}}{2}\right) t_1 - \frac{I_{OUT}\, t_1}{C_O}$$

which simplifies to:

$$V_{P\text{-}P} = \frac{(I_{pk} - I_{OUT})^2}{2\, I_{pk}} \left(\frac{t_{off}}{C_O}\right)$$

As with the step-down regulator, this ripple voltage will be increased by the product of the output capacitor's ESR and the ripple current through the capacitor.

To calculate the efficiency of the system:

$$n = \frac{P_{OUT}}{P_{IN}}$$

The input power is given by:

$$P_{IN} = I_{IN}\, V_{IN}$$

The average input current can be calculated from the i_L waveform of *Figure 5*:

$$I_{IN(avg)} = \frac{I_{pk}}{2}$$

The output power is given by:

$$P_{OUT} = I_{OUT}\, V_{OUT}$$

Combining and simplifying the above equations gives an expression for efficiency:

$$n = \frac{V_{IN} - V_{SAT}}{V_{IN}} \left(\frac{V_{OUT}}{V_{OUT} + V_D - V_{SAT}}\right)$$

As the forward drops in the diode and switch are reduced, the efficiency of the system improves.

The above calculation did not take into account quiescent power dissipation or switching losses, which will reduce efficiency from the calculated value; it does, however, give a good approximation for efficiency.

ANALYSIS—INVERTING OPERATION

Figure 2 illustrates the basic configuration for an inverting regulator system. The waveforms for this system are shown in *Figure 6*.

To analyze, assume that the following condition is true just prior to turning on the switch:

$$i_L = 0$$

When switch S1 is closed, the voltage at point A is:

$$V_A = V_{IN} - V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch. At this time, diode D1 is reverse biased and the current through the inductor increases at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch is closed and the inductor does not saturate. This rate is constant if the input voltage remains constant during the on-time of the switch, and the current through the inductor at any instant, while the switch is closed, is given by:

$$i_L = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1 is given by:

$$I_{pk} = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t_{on}$$

At the end of the on-time, switch S1 is opened and the inductor generates a voltage that forward biases D1, providing a current path for the inductor current. The voltage at point A is now:

$$V_A = V_{OUT} - V_D$$

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\left(\frac{V_D - V_{OUT}}{L}\right)$$

The current through the inductor and diode at any given instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_D - V_{OUT}}{L}\right) t$$

Assuming that the current through the inductor reaches zero after a time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_D - V_{OUT}}{L}\right) t_{off}$$

Analysis shows the relationship between t_{on} and t_{off} to be:

$$\frac{t_{on}}{t_{off}} = \frac{V_D - V_{OUT}}{V_{IN} - V_{SAT}}$$

The previous analysis assumes that the output voltage remains relatively constant. For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 6* (i_D waveform) shows that:

$$\left(\frac{I_{pk}}{2}\right) t_{off} = (t_{on} + t_{off})\, I_{OUT}$$

$$\text{or } I_{pk} = 2\, I_{OUT} \left(\frac{V_{IN} + V_D - V_{OUT} - V_{SAT}}{V_{IN} - V_{SAT}}\right)$$

For average output voltage to remain constant, the average current through the diode must equal the output current.

The ripple voltage can be calculated using *Figure 6* (i_D waveform):

$$t_1 = t_{off} - \left(\frac{I_{OUT}}{I_{pk}}\right) t_{off}$$

During time interval t_1, the output capacitor C_O charges from its most positive value to its most negative value; therefore:

$$V_{P\text{-}P} = \frac{\Delta Q}{C_O} = \frac{1}{C_O}\left(\frac{I_{pk} + I_{OUT}}{2}\right) t_1 - \frac{I_{OUT}\, t_1}{C_O}$$

which simplifies to:

$$V_{P\text{-}P} = \frac{t_{off}}{C_O} \times \frac{(I_{pk} - I_{OUT})^2}{2\, I_{pk}}$$

This ripple voltage will be increased by the product of the output capacitor's ESR and the ripple current through the capacitor.

To calculate the efficiency of the system:

$$n = \frac{P_{OUT}}{P_{IN}} = \frac{I_{OUT}\, V_{OUT}}{I_{IN}\, V_{IN}}$$

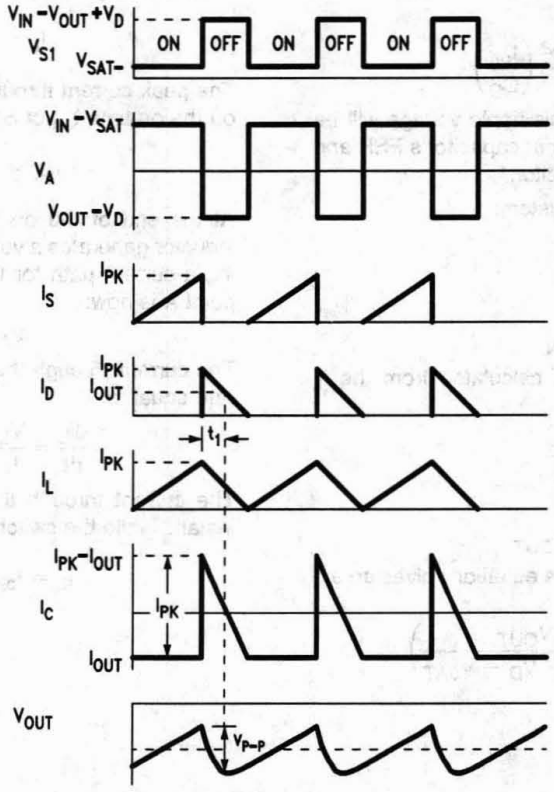
Average input current can be calculated from *Figure 6* (i_S waveform):

$$I_{IN(avg)} = \frac{I_{pk}}{2}\left(\frac{t_{on}}{t_{on} + t_{off}}\right)$$

Combining and simplifying the previous equations gives an expression for the system efficiency:

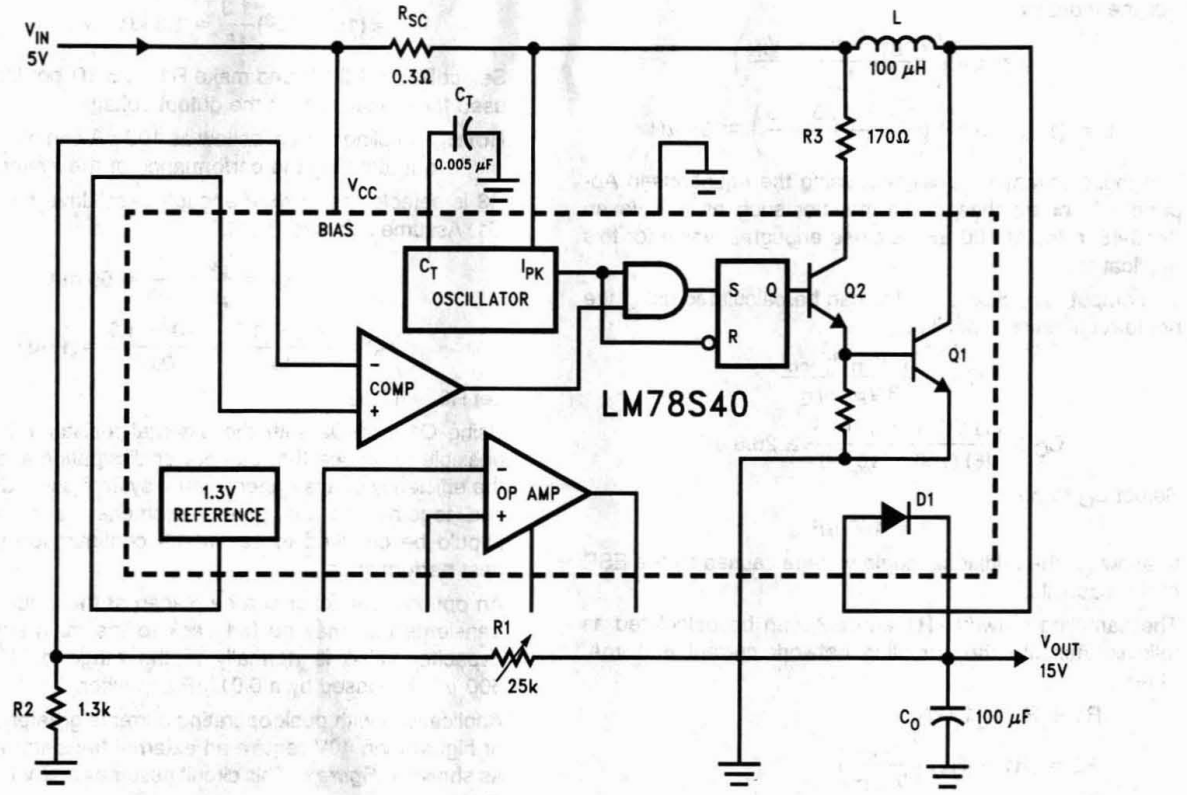
$$n = \frac{V_{IN} - V_{SAT}}{V_{IN}}\left(\frac{|V_{OUT}|}{V_D + |V_{OUT}|}\right)$$

Again, as the forward drops in the diode and switch are reduced, the efficiency of the system improves. Also, since switching losses and quiescent current power dissipation are not included in the calculations, efficiency will be somewhat lower than predicted by the above equation.



TL/H/11040–9

FIGURE 6. Voltage Inverter Waveforms



TL/H/11040–10

FIGURE 7. Step-Up Voltage Regulator

DESIGN—STEP-UP REGULATOR

A schematic of the basic step-up regulator is shown in *Figure 7*.

Conditions:

$V_{IN} = 5V$ $I_{OUT} = 150$ mA

$V_{OUT} = 15V$ $V_{RIPPLE} \leq 1\%$

Calculations:

$$I_{pk} = 2\, I_{OUT(max)} \left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}} \right)$$

$$I_{pk} = 2\,(0.15) \left(\frac{15 + 1.25 - 0.45}{5 - 0.45} \right) \approx 1\ A$$

Therefore:

$$R_{SC} = \frac{0.3}{I_{pk}} \approx 0.3\Omega$$

To calculate the ratio of t_{on}/t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}} = \frac{15 + 1.25 - 5}{5 - 0.45} \approx 1.9$$

$$t_{on} = 1.9\, t_{off}$$

At this point, a value is selected for t_{off}, which in turn defines t_{on}. In making the selection, two constraints must be considered. The first constraint comes from efforts to maintain high efficiency. Rise and fall times should be kept small in comparison to the total period ($t_{on} + t_{off}$) so that only a small portion of the total time is spent in the linear mode of operation, where losses are high. This can be achieved if both t_{on} and t_{off} are made greater than or equal to 10 μs.

The second constraint is due to the techniques used to reduce the effects of the switching mode of operation on external systems. Filtering requirements can be made less stringent by maintaining a high switching frequency, i.e., above 15 or 20 kHz. This condition can be met by specifying the total period, $t_{on} + t_{off}$, to be less than 50 μs.

Therefore, the two design constraints are:

$$t_{on} \geq 10\ \mu s;\ t_{off} \geq 10\ \mu s$$

$$(t_{on} + t_{off}) \leq 50\ \mu s$$

In some cases, both constraints cannot be met and some trade-offs will be necessary.

Following these constraints, value is selected for t_{off}:

$$t_{off} = 10\ \mu s$$

It is now possible to calculate values for the timing capacitor C_T and the inductor L.

The timing capacitor is related (by design) to the off-time by the equation:

$$C_T = (45 \times 10^{-5})\, t_{off}$$

$$C_T = (45 \times 10^{-5})\, 10^{-5} = 4500\ pF$$

Therefore, set $C_T = 5000$ pF, which results in:

$$t_{off} \approx 11\ \mu s \text{ and } t_{on} \approx 21\ \mu s$$

For the inductor

$$L = t_{off}\left(\frac{V_{OUT} + V_D - V_{IN}}{I_{pk}}\right)$$

$$L = (11 \times 10^{-6})\left(\frac{15 + 1.25 - 5}{1}\right) \approx 96\ \mu H$$

The inductor may be designed, using the equations in Appendix A, or purchased. An inductor such as a Delevan 3443-48, rated at 100 μH, is close enough in value for this application.

The output capacitor C_O value can be calculated using the ripple requirement specified:

$$C_O \geq \frac{I_{pk}\,(t_{on} + t_{off})}{8\,V_{RIPPLE}}$$

$$C_O \geq \frac{(1)\,(21 + 11)\,10^{-6}}{(8)\,(150 \times 10^{-3})} \geq 26.6\ \mu F$$

Select C_O to be:

$$C_O = 100\ \mu F$$

to allow for the additional ripple voltage caused by the ESR of the capacitor.

The sampling network, R1 and R2, can be calculated as follows. Assume the sampling network current is 1 mA. Then:

$$R1 + R2 = 15\ k\Omega$$

$$R2 = (R1 + R2)\left(\frac{V_{REF}}{V_{OUT}}\right)$$

$$R2 = (15 \times 10^3)\frac{1.3}{15} = 1.3\ k\Omega$$

Select R2 = 1.3 kΩ and make R1 a 25 kΩ pot that can be used for adjustments in the output voltage.

Note: Sampling current as low as 100 μA can be used without affecting the performance of the system.

R3 is selected to provide enough base drive for transistor Q1. Assume a forced β of 20:

$$I_{C2} \approx I_{B1} = \frac{I_{pk}}{\beta} = \frac{1}{20} = 50\ mA$$

$$R3 \approx \frac{V_{IN} - 1.3}{I_B} = \frac{10 - 1.3}{0.05} = 174\Omega$$

Let R3 = 170Ω.

Using Q1 and Q2 with the external resistor R3 makes it possible to reduce the total power dissipation and improve the efficiency of this system over a system using Q1 and Q2 tied together as the control element. Each application should be checked to see which configuration yields the best performance.

An optional capacitor can be placed at the input to reduce transients that may be fed back to the main supply. The capacitor value is normally in the range of 100 μF to 500 μF, bypassed by a 0.01 μF capacitor.

Applications with peak operating currents greater than 1.5A or higher than 40V require an external transistor and diode as shown in *Figure 8*. This circuit assumes a 15V input and a 70V output.

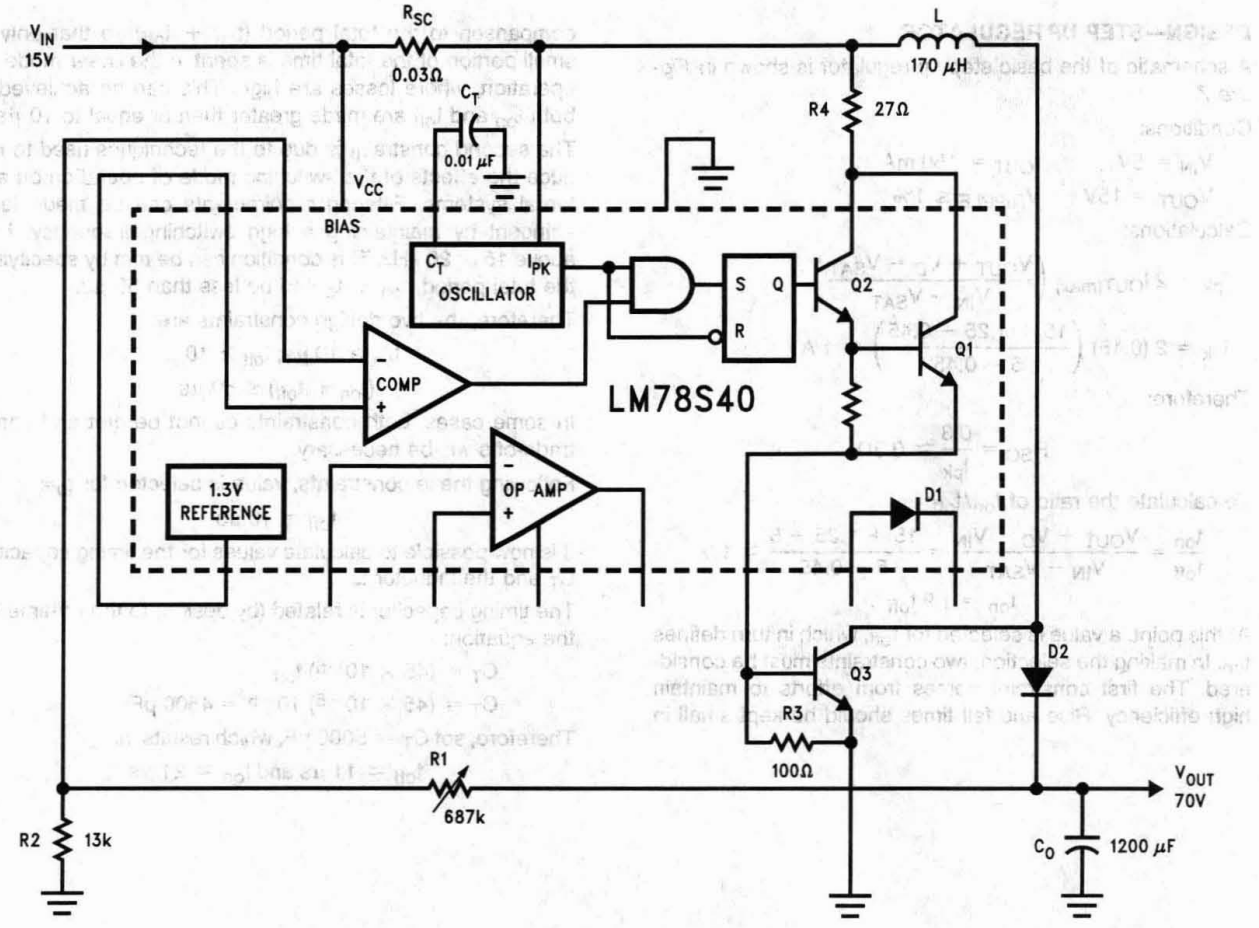


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FIGURE 8. Switching Regulator with 15V Input, 70V Output

DESIGN—STEP-DOWN REGULATOR

A schematic of the basic step-down regulator is shown in *Figure 9*.

Conditions:

$V_{IN} = 25V$ $I_{OUT(max)} = 500\ mA$

$V_{OUT} = 10V$ $V_{RIPPLE} < 1\%$

Calculations:

$I_{pk} = 2\ I_{OUT(max)}$

$I_{pk} = 2\ (0.5) = 1A$

Therefore:

$$R_{SC} = \frac{0.33}{I_{pk}} = 0.33\Omega$$

Next, calculate the ratio of t_{on} to t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$$

$$\frac{t_{on}}{t_{off}} = \frac{10 + 1.25}{25 - 1.1 - 10} \approx 0.8$$

$$t_{on} = 0.8\ t_{off}$$

Following design constraints previously discussed, a value is selected for t_{off}:

$$t_{off} = 22\ \mu s$$

$$t_{on} = 18.6\ \mu s$$

Then calculate C_T and L:

$$C_T = (45 \times 10^{-5})\ t_{off}$$

$$C_T = (45 \times 10^{-5})\ (22 \times 10^{-6}) \approx 0.1\ \mu F$$

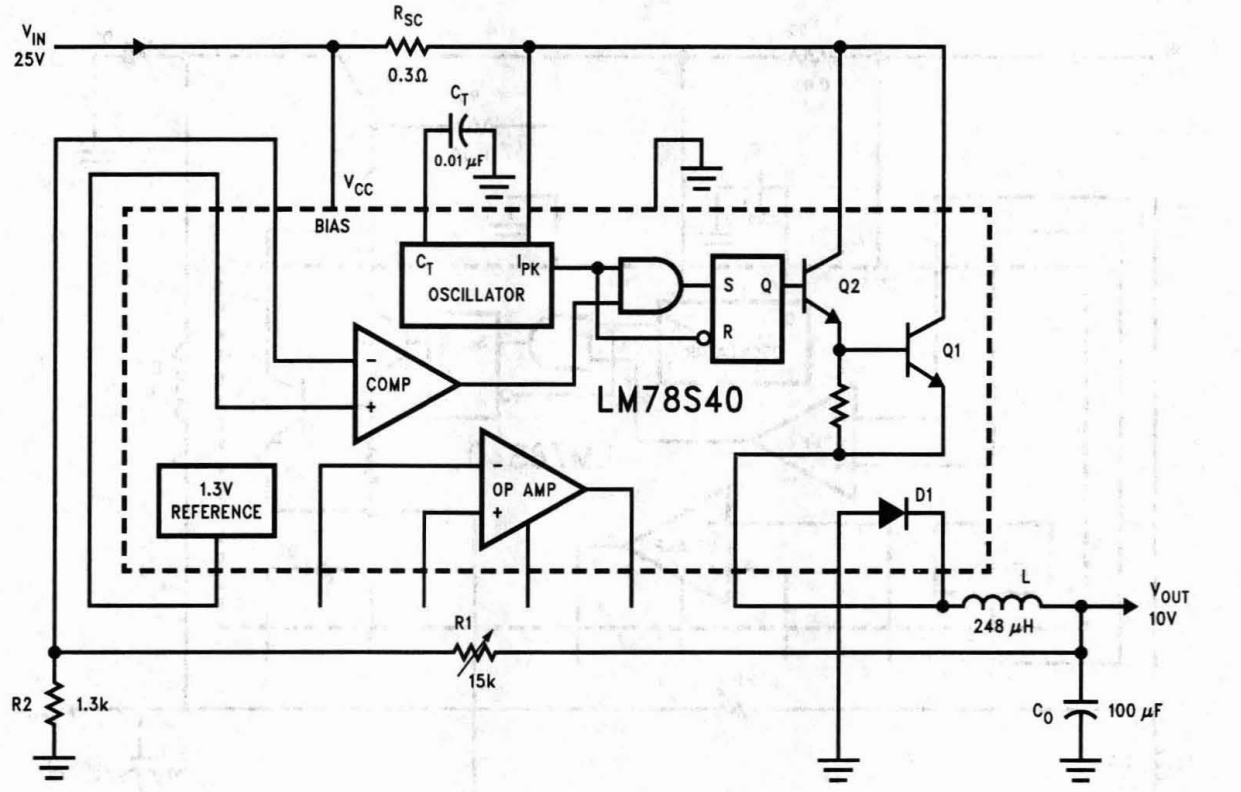


FIGURE 9. Step-Down Voltage Regulator

$$L = \left(\frac{V_{OUT} + V_D}{I_{pk}}\right) t_{off}$$

$$L = \frac{10 + 1.25}{1} (22 \times 10^{-6}) = 248\ \mu H$$

Output capacitor C_O can be calculated from ripple requirements:

$$C_O \geq \frac{I_{pk}\,(t_{on} + t_{off})}{8\,V_{RIPPLE}}$$

$$C_O \geq \frac{(1)\,(18.6 + 22)\,10^{-6}}{(8)\,(0.1)} = 50\ \mu F$$

Select C_O to be:

$$C_O = 100\ \mu F$$

Assuming that the sampling network current is 1 mA, then:

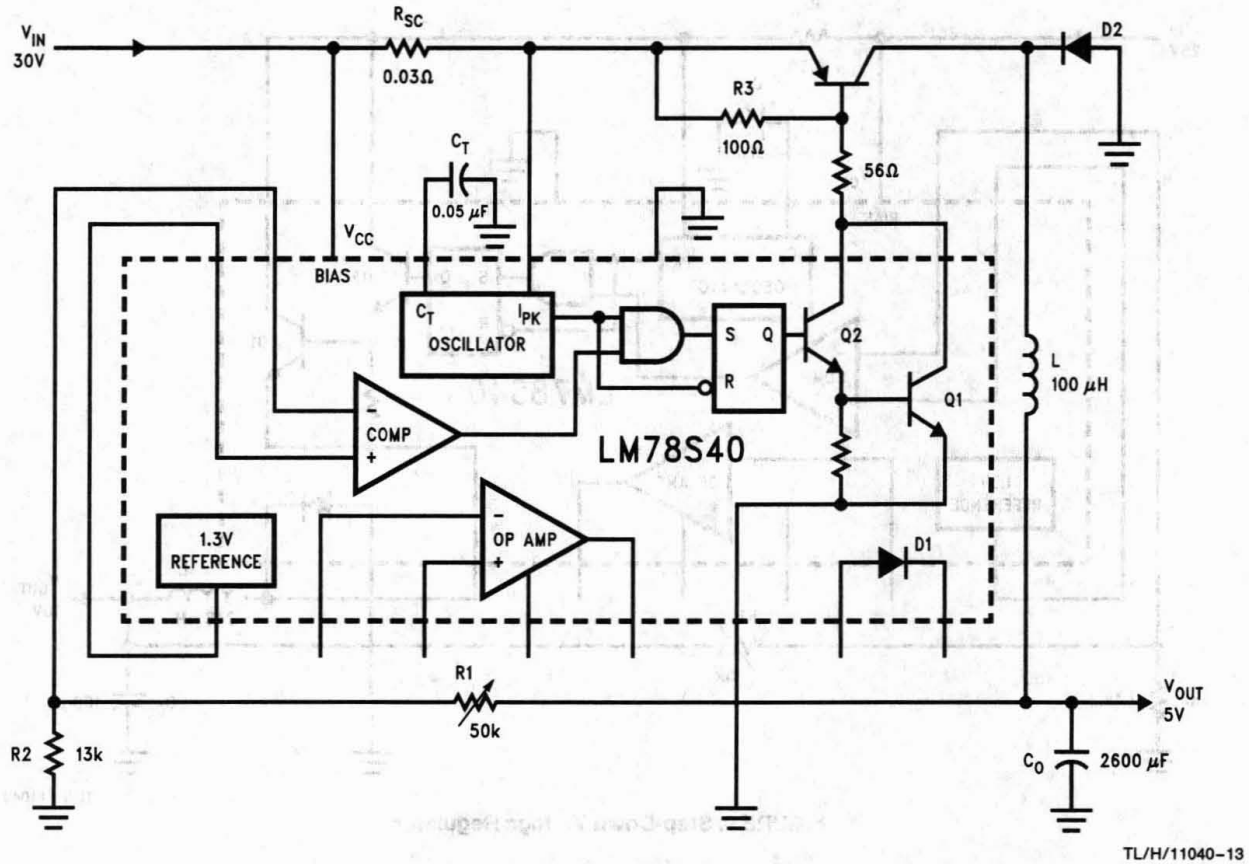
$$R1 + R2 = 10\ k\Omega$$

$$R2 = (R1 + R2)\frac{V_{REF}}{V_{OUT}} = 1.3\ k\Omega$$

Select R2 = 1.3 kΩ and make R1 a 15 kΩ pot that can be used for adjustments in output voltage.

If $I_{pk} \geq 300$ mA, during the off-time when the diode is forward biased, the negative voltage generated at pin 1 causes a parasitic transistor to turn on, dissipating excess power. Replacing the internal diode with an external diode eliminates this condition and allows normal operation.

For applications with peak currents greater than 1A or voltages greater than 40V, an external transistor and diode are required, as shown in *Figure 10,* which assumes a 30V input and a 5V output at 5A.



TL/H/11040–13

FIGURE 10. Modified Step-Down Regulator with 5A, 5V Output

DESIGN—INVERTING REGULATOR

A schematic of the basic inverting regulator is shown in *Figure 11.*

Conditions:

$V_{IN} = 12V$ $\quad I_{OUT(max)} = 500\ mA$

$V_{OUT} = -15V$ $\quad V_{RIPPLE} \leq 1\%$

Calculations:

$$I_{pk} = 2\, I_{OUT(max)} \left(\frac{V_{IN} + V_D - V_{OUT} - V_{SAT}}{V_{IN} - V_{SAT}} \right)$$

For 2N6051 $V_{SAT} \leq 2V$

$$I_{pk} = 2\,(0.5) \left(\frac{12 + 1.25 + 15 - 2)}{12 - 2} \right) \cong 2.57$$

Therefore:

$$R_{SC} = \frac{0.3}{I_{pk}} \approx 0.1\Omega$$

Calculating the ratio of t_{on} to t_{off},

$$\frac{t_{on}}{t_{off}} = \frac{V_D - V_{OUT}}{V_{IN} - V_{SAT}}$$

$$\frac{t_{on}}{t_{off}} = \frac{1.25 + 15}{10 - 2} \approx 2$$

$$t_{on} = 2\, t_{off}$$

Following design constraints, a value is selected for t_{off}:

$$t_{off} = 10\ \mu s$$

Now, calculate C_T and L:

$$C_T = (45 \times 10^{-5})\, t_{off}$$

$$C_T = (45 \times 10^{-5})\, 10^{-5} = 4500\ pF$$

Setting $C_T = 5000\ pF$ makes $t_{off} \approx 11\ \mu s$ and $t_{on} \approx 22\ \mu s$.

$$L = \left(\frac{V_D - V_{OUT}}{I_{pk}} \right) t_{off}$$

$$L = \left(\frac{1.25 + 15}{2.57} \right) (11 \times 10^{-6}) \approx 70\ \mu H$$

The output capacitor C_O again is calculated:

$$C_O \geq \frac{(I_{pk} - I_O)^2\, t_{off}}{2\, I_{pk} \times V_{RIPPLE}}$$

$$C_O \geq \frac{(2.57 - 0.5)^2\, (11 \times 10^{-6})}{(2)\,(2.57)\,(0.1)} = 97\ \mu F$$

C_O is selected to be 200 μF.

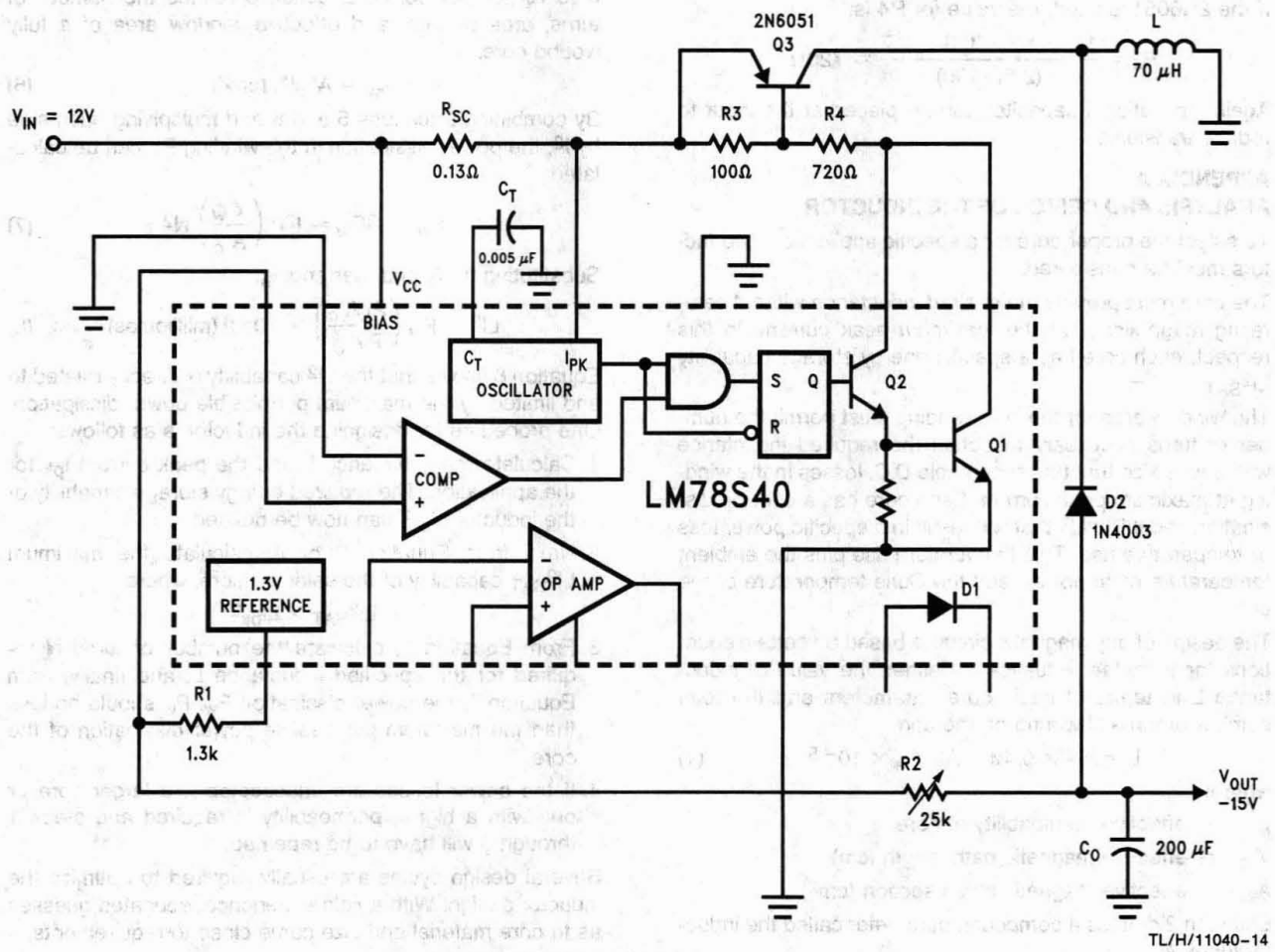


FIGURE 11. Inverting Regulator

The sampling network, R1 and R2, can easily be calculated. Assuming the sampling network current I_S is 1 mA:

$$R_1 = \frac{V_{REF}}{I_S} = 1.3\,k\Omega$$

$$R_2 = \frac{-V_{OUT}}{I_S} = 15\,k\Omega$$

Set R1 = 1.3 kΩ and use a 25 kΩ pot for R2 so that output voltage can be adjusted.

This application requires an external diode and transistor since the substrate of the regulator is referenced to ground and a negative voltage is present on the output. The external diode and transistor prevent the substrate diodes from a forward-biased condition. See Appendix B for selection of the diode and transistor.

R3 is provided for quick turn-off on the external transistor and is usually in the range of 100Ω to 300Ω. R4 can be calculated as follows:

$$R_4 \approx \frac{V_{IN} - V_{SAT} - V_T - V_{BE}}{I_{pk}/\beta}$$

where:

V_T = threshold voltage = 300 mV

V_{BE} = base emitter drop across the external transistor

$\beta \approx \frac{1}{4}\, h_{FE}$ of the external transistor

If the 2N6051 is used, the value for R4 is:

$$R_4 = \frac{12 - 1.3 - 0.3 - 0.7}{(2.57/190)} \approx 720\Omega$$

Again, an optional capacitor can be placed at the input to reduce transients.

APPENDIX A
ANALYSIS AND DESIGN OF THE INDUCTOR

To select the proper core for a specific application, two factors must be considered.

The core must provide the desired inductance without saturating magnetically at the maximum peak current. In this respect, each core has a specific energy storage capability LI^2_{SAT}.

The window area for the core winding must permit the number of turns necessary to obtain the required inductance with a wire size that has acceptable D.C. losses in the winding at maximum peak current. Each core has a specific dissipation capability LI^2 that will result in a specific power loss or temperature rise. This temperature rise plus the ambient temperature must not exceed the Curie temperature of the core.

The design of any magnetic circuit is based on certain equations for formulae. Equation 1 defines the value of inductance L in terms of basic core parameters and the total number of turns N wound on the core:

$$L = N^2 \times 0.4\pi\, \mu\, A_e\, \ell_e \times 10^{-5} \qquad (1)$$

where:

μ = effective permeability of core

ℓ_e = effective magnetic path length (cm)

A_e = effective magnetic cross section (cm^2)

Equation 2 defines a compound parameter called the inductor index A_L:

$$A_L = 0.4\pi\, \mu A_e\, \ell_e \times 10\ (mH/1000\ turns) \qquad (2)$$

Combining Equations 1 and 2 and multiplying by I^2 gives:

$$LI^2 = (NI)^2\,(A_L \times 10^{-6})\ (millijoules) \qquad (3)$$

Any specific core has a maximum ampere-turn NI capability limited by magnetic saturation of the core material. The maximum LI^2_{SAT} of the core can then be calculated from Equation 3 or, if the saturation flux density B_{SAT} is given, from Equation 4:

$$LI^2 = \frac{(B_{SAT})^2\,(A_e^2 \times 10^{-4})}{A_L}\ (millijoules) \qquad (4)$$

The core selected for an application must have an LI^2_{SAT} value greater than calculated to insure that the core does not saturate under maximum peak current conditions.

In switching regulator applications, power dissipation in the inductor is almost entirely due to D.C. losses in the winding. The dc resistance of the winding R_w can be calculated from Equation 5:

$$R_w = P(\ell_w/A_w)\,N \qquad (5)$$

where

P = resistivity of wire (Ω/cm)

ℓ_w = length of turn (cm)

A_w = effective area of wire (cm^2)

Core geometry provides a certain window area A_c for the winding. The effective area A'_c is 0.5 A_c for toroids and 0.65 A_c for pot cores. Equation 6 relates the number of turns, area of wire, and effective window area of a fully wound core.

$$A_w = A'_c/N\ (cm^2) \qquad (6)$$

By combining Equations 5 and 6 and multiplying each side by I^2, the power dissipation in the winding P_w can be calculated:

$$P_w = I^2R_w = I^2P\left(\frac{\ell_w}{A'_c}\right)N^2 \qquad (7)$$

Substituting for N and rearranging:

$$LI^2 = P_w\left(\frac{A_L A'_c}{P\,\ell_w}\right) \times 10^{-6}\ (millijoules) \qquad (8)$$

Equation 8 shows that the LI^2 capability is directly related to and limited by the maximum permissible power dissipation. One procedure for designing the inductor is as follows:

1. Calculate the inductance L and the peak current I_{pk} for the application. The required energy storage capability of the inductor LI_{pk}^2 can now be defined.
2. Next, from Equation 3 or 4, calculate the maximum LI^2_{SAT} capability of the selected core, where
$$LI^2_{SAT} > LI_{pk}^2$$
3. From Equation 1, calculate the number of turns N required for the specified inductance L, and finally, from Equation 7, the power dissipation P_w. P_w should be less than the maximum permissible power dissipation of the core.
4. If the power losses are unacceptable, a larger core or one with a higher permeability is required and steps 1 through 3 will have to be repeated.

Several design cycles are usually required to optimize the inductor design. With a little experience, educated guesses as to core material and size come close to requirements.

APPENDIX B
SELECTION OF SWITCHING COMPONENTS

The designer should be fully aware of the capabilities and limitations of power transistors used in switching applications. Transistors in linear applications operate around a quiescent point; whereas in switching applications operation is fully on or fully off. Transistors must be selected and tested to withstand the unique stress caused by this mode of operation. Parameters such as current and voltage ratings, secondary breakdown ratings, power dissipation, saturation voltage and switching times critically affect transistor performance in switching applications. Similar parameters are important in diode selection, including voltage, current, and power limitations, as well as forward voltage drop and switching speed.

Initial selection can begin with voltage and current requirements. Voltage ratings of the switching transistor and diode must be greater than the maximum input voltage, including any transient voltages that may appear at the input of the switching regulator. Transistor saturation voltage $V_{CE(SAT)}$ and diode forward voltage V_D at full load output current should be as low as possible to maintain high operating efficiency. The transistor and diode should be selected to handle the required maximum peak current and power dissipation.

Good efficiency requires fast switching diodes and transistors. Transistor switching losses become significant when the combined rise t_r plus fall time t_f exceeds:

$$0.05\ (t_{on} + t_{off})$$

For 20 kHz operation, $t_r + t_f$ should be less than 2.5 μs for maximum efficiency. While transistor delay and storage times do not affect efficiency, delays in turn-on and turn-off can result in increased output voltage ripple. For optimal operation combined delay time t_d plus storage time t_s should be less than:

$$0.05\ (t_{on} + t_{off})$$

APPENDIX C
SELECTION OF OUTPUT FILTER CAPACITORS

In general, output capacitors used in switching regulators are large (>100 μF), must operate at high frequencies (>20 kHz), and require low ESR and ESL. An excellent trade-off between cost and performance is the solid-tantalum capacitor, constructed of sintered tantalum powder particles packed around a tantalum anode, which makes a rigid assembly or slug. Compared to aluminum electrolytic capacitors, solid-tantalum capacitors have higher CV product-per-unit volume, are more stable, and have hermetic seals to eliminate effects of humidity.

APPENDIX D
EMI

Due to the wiring inductance in a circuit, rapid changes in current generate voltage transients. These voltage spikes are proportional to both the wiring inductance and the rate at which the current changes:

$$V = L\frac{di}{dt}$$

The energy of the voltage spike is proportional to the wiring inductance and the square of the current:

$$E = 1/2\ LI^2$$

Interference and voltage spiking are easier to filter if the energy in the spikes is low and the components predominantly high frequency.

The following precautions will reduce EMI:

— Keep loop inductance to a minimum by utilizing appropriate layout and interconnect geometry.

— Keep loop area as small as possible and lead lengths small and, in step-down mode, return the input capacitor directly to the diode to reduce EMI and ground-loop noise.

— Select an external diode that can hold peak recovery current as low as possible. This reduces the energy content of the voltage spikes.

APPENDIX E
DESIGN EQUATIONS

LM78S40 Design Formulae

Characteristic	Step Down	Step Up	Inverting
I_{pk}	$2\ I_{OUT(max)}$	$2\ I_{OUT(max)} \left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$	$2\ I_{OUT(max)} \left(\frac{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$
R_{SC}	$0.33\ I_{pk}$	$0.33\ I_{pk}$	$0.33\ I_{pk}$
$\frac{t_{on}}{t_{off}}$	$\frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$	$\frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}}$	$\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} - V_{SAT}}$
L	$\left(\frac{V_{OUT} + V_D}{I_{pk}}\right) t_{off}$	$\left(\frac{V_{OUT} + V_D - V_{IN}}{I_{pk}}\right) t_{off}$	$\left(\frac{\lvert V_{OUT}\rvert + V_D}{I_{pk}}\right) t_{off}$
t_{off}	$\frac{I_{pk} L}{V_{OUT} + V_D}$	$\frac{I_{pk} L}{V_{OUT} + V_D - V_{IN}}$	$\frac{I_{pk} L}{\lvert V_{OUT}\rvert + V_D}$
$C_{T\ (\mu F)}$	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$
C_O	$\frac{I_{pk}\ (t_{on} + t_{off})}{8\ V_{RIPPLE}}$	$\frac{(I_{pk} - I_{OUT})^2\ t_{off}}{2\ I_{pk}\ V_{RIPPLE}}$	$\frac{(I_{pk} - I_{OUT})^2\ t_{off}}{2\ I_{pk}\ V_{RIPPLE}}$
Efficiency	$\left(\frac{V_{IN} - V_{SAT} + V_D}{V_{IN}}\right) \frac{V_{OUT}}{V_{OUT} + V_D}$	$\frac{V_{IN} - V_{SAT}}{V_{IN}} \left(\frac{V_{OUT}}{V_{OUT} + V_D - V_S}\right)$	$\left(\frac{\lvert V_{OUT}\rvert}{V_D + \lvert V_{OUT}\rvert}\right)$
$I_{IN(avg)}$ (Max load condition)	$\frac{I_{pk}}{2} \left(\frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} + V_D}\right)$	$\frac{I_{pk}}{2}$	$\frac{I_{pk}}{2} \left(\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_{SAT}}\right)$

Note: V_{SAT}—Saturation voltage of the switching element

V_D—Forward voltage of the flyback diode

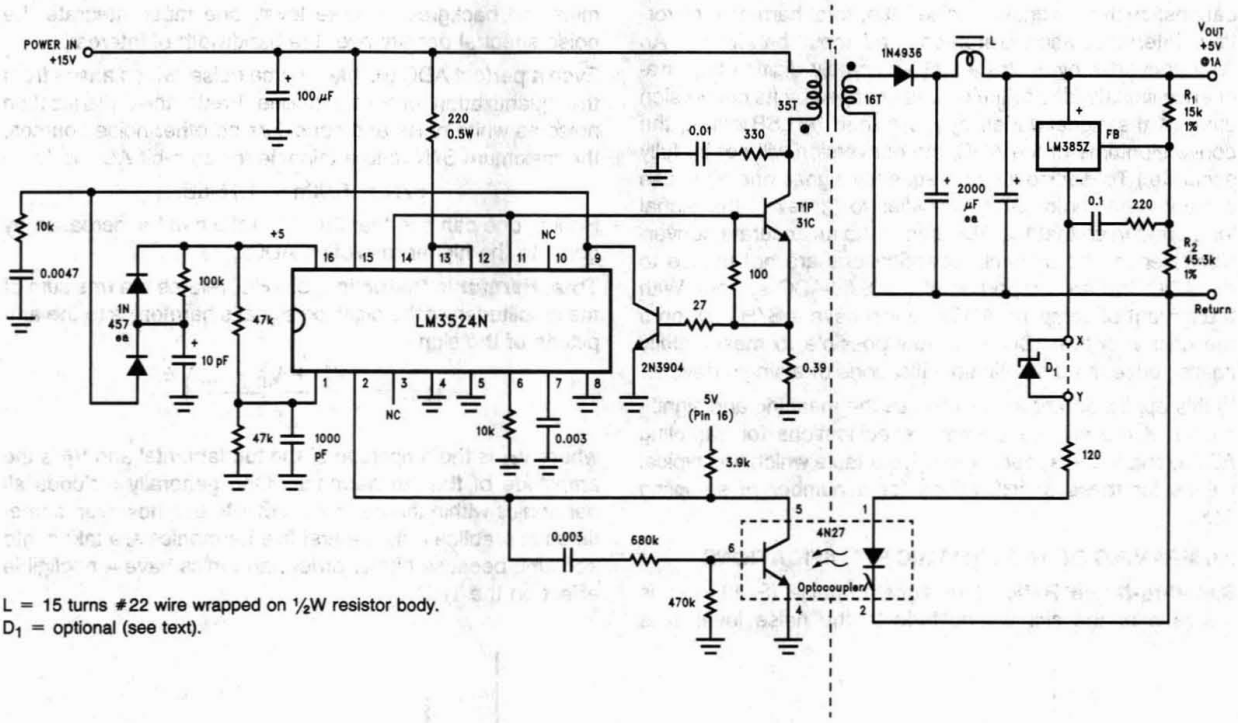
LM385 Feedback Provides Regulator Isolation

National Semiconductor
Application Note 715
Robert Pease
Fran Hoffart

You can use a conventional 4N27 optocoupler in a feedback arrangement *(Figure 1)* to design a switching regulator with a floating output. The LM3524 switch-mode-regulator IC is configured as a simple flyback power supply with transformer-isolated output. The LM385 acts as a reference and comparison amplifier that satisifes the 4N27's current demands for balancing the dc feedback to pin 2 of the LM3524, thereby closing the loop. The LM385 automatically compensates for any LED degradation or optical-coupling loss.

The 4N27 specs a 0.1 dc to 1.6 dc gain range; the ac gain varies from 0.05 to 1.0. Fortunately, the "Miller" damper from pins 5 to 6 nullifies the effect of the wide gain variance. Moreover, the damper provides excellent loop stability for a wide range of 4N27 optocouplers from several manufacturers. In the example shown, the LM385 provides 0.5 mA to 5 mA to the optocoupler.

If the 5V output available from this circuit does not meet your needs, choose $R_2 = R_1 (V_{OUT} - 1.25)/1.25$. If V_{OUT} is greater than 6V, insert a zener diode between points X and Y, with $V_Z = V_{OUT} - 5V$; this addition prevents the voltage across the LM385 from exceeding its 5.3V max limit. The circuit is suitable for regulated output voltages from 3.2V to 25V.



L = 15 turns #22 wire wrapped on ½W resistor body.
D_1 = optional (see text).

TL/H/11049–1

FIGURE 1. Optocoupler-based feedback circuit produces galvanically-isolated, regulated voltages. The heavy negative feedback compensates for wide variations in optocoupler gains. The values portrayed in this schematic yield 5V output; by varying R_2, you can obtain voltages from 3.2V to 25V.

Dynamic Specifications for Sampling A/D Converters

National Semiconductor
Application Note 769
Leon G. Melkonian

1.0 INTRODUCTION

Traditionally, analog-to-digital converters (ADCs) have been specified by their static characteristics, such as integral and differential nonlinearity, gain error, and offset error. These specifications are important for determining the DC accuracy of an A/D converter, and are very important in applications such as weighing, temperature measurement, and other situations where the input signal varies slowly over time.

Many applications, however, require digitizing a signal which varies quickly over time. These include digital signal processing (DSP) applications, such as digital audio, spectral analysis, and motion control. For these applications, DC accuracy is not as crucial as AC accuracy. The important specifications for these applications are the dynamic specifications, such as signal-to-noise ratio, total harmonic distortion, intermodulation distortion, and input bandwidth. An A/D converter by itself cannot accurately digitize high frequency signals, due to limitations imposed by its conversion time. (If the signal varies by more than ½ LSB during the conversion time of the ADC, the conversion will not be fully accurate.) To digitize a high frequency signal, one must use a sample-and-hold (S/H) amplifier to "freeze" the signal long enough so that the ADC can make an accurate conversion. Hence, the dynamic specifications are not unique to the ADC, but are properties of the S/H-ADC system. With the advent of sampling ADCs, which have a S/H built onto the chip with the ADC, it is now possible to meaningfully characterize the dynamic specifications of a single device.

In this application note, we discuss the meaning and significance of the various dynamic specifications for sampling ADCs, and in the appendix we give a table which has typical values for these specifications for a number of sampling ADCs.

2.0 MEANING OF THE DYNAMIC SPECIFICATIONS

Signal-to-Noise Ratio. The signal-to-noise (S/N) ratio is the ratio of the signal amplitude to the noise level. It is generally specified in the data sheets at a set of input signal frequencies, at a specific sampling rate, and with the signal amplitude at or near the maximum allowable level.

There is some ambiguity regarding the composition of the noise component of the S/N ratio. Some manufacturers reserve the term S/N ratio to include only the background noise and the spurious noise, whereas others also include the harmonics of the signal.

When comparing the S/N ratio for several sampling ADCs, one should look in the data sheets to see how it is measured. When the harmonics are included, the S/N specification is frequently referred to as the **Signal-to-(Noise + Distortion)** or **SINAD**. Both signal-to-noise specifications exclude any DC offset from the noise component. To determine the background noise level, one must integrate the noise spectral density over the bandwidth of interest.

Even a perfect ADC will have some noise, which arises from the quantization process. If one treats this quantization noise as white noise and considers no other noise sources, the maximum S/N ratio attainable for an n-bit ADC is [1].

$$S/N = 6.02n + 1.76\ \text{dB}.$$

Hence, one can see that the S/N ratio can be increased by going to the higher resolution ADCs.

Total Harmonic Distortion, or THD, relates the rms sum of the amplitudes of the digitized signal's harmonics to the amplitude of the signal:

$$THD = \left(\frac{V_{f2}^2 + V_{f3}^2 + \ldots}{V_{f1}^2}\right)^{1/2},$$

where V_{f1} is the amplitude of the fundamental and V_{fi} is the amplitude of the ith harmonic. One generally includes all harmonics within the bandwidth of interest; however, sometimes in practice only the first five harmonics are taken into account, because higher order harmonics have a negligible effect on the THD.

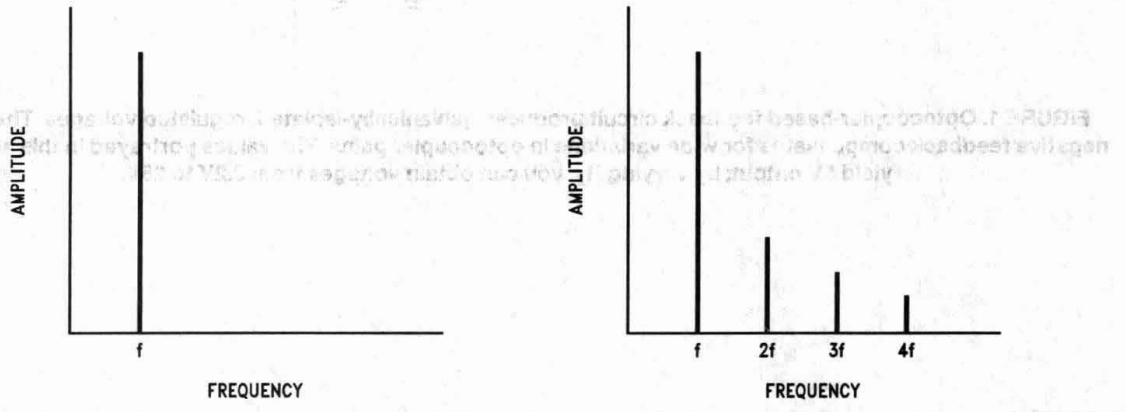


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FIGURE 1. A Signal with a Single Frequency Component (left) Suffers Harmonic Distortion after A/D Conversion (right)

ADCs produce harmonics of an input signal because an ADC is an inherently nonlinear device. This can be easily seen by looking at the transfer curve of an ideal ADC, which looks like a staircase with equal-sized steps *(Figure 2)*. In a real ADC, "bowing" and other nonlinearities add to the distortion. If the output of an ADC is fed to a perfect DAC, then the transfer function of this system can be represented in principle as a polynomial

$$V_{OUT} = a_0 + a_1(V_{IN}) + a_2(V_{IN})^2 + a_3(V_{IN})^3 + \ldots$$

A perfectly linear system would have all the a_j zero except for a_0 and a_1. The second harmonic appears, for example, because a_2 is nonzero. If one uses the trigonometric identity

$$(\cos \omega t)^2 = \frac{1 + \cos 2\omega t}{2},$$

one can see how a second-order nonlinearity produces an output that has a frequency that is twice that of the fundamental.

As one goes to higher resolution converters, the THD will decrease because the transfer curve of the ADC more closely resembles a straight line. (We are assuming that the integral and differential nonlinearities are going down, proportionately, as the resolution increases. This is generally the case.) Like the S/N ratio, the THD is generally specified in the data sheets at a set of frequencies and with the signal amplitude at or near the maximum allowable level. It is usually specified in decibels or as a percentage.

Having a low THD is especially important in applications such as audio and spectral analysis because in these applications, particularly, one does not want the conversion process to add new frequency components to the signal.

Intermodulation Distortion, or IMD, results when two frequency components in a signal interact through the nonlinearities in the ADC to produce signals at additional frequencies. If f_a and f_b are the signal frequencies at the input of the device, the possible IMD products f_{mn} are given by $f_{mn} = m f_a \pm n f_b$, where m and n take on positive integer values, and are such that f_{mn} is positive. The jth order IMD products are those for which $m + n = j$.

The second order intermodulation products of f_a and f_b, which occur when m and n both equal 1, are given by the sum and difference frequencies of f_a and f_b.

Using the formula

$(\cos \omega_1 t + \cos \omega_2 t)^2 = \cos^2\omega_1 t + 2(\cos \omega_1 t)(\cos \omega_2 t) + \cos^2\omega_2 t$

and the trigonometric identity

$2(\cos \omega_1 t)(\cos \omega_2 t) = \cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t$

one can see how a second-order nonlinearity leads to the production of an output that has components at the sum and difference frequencies of the inputs (and also at the second harmonics). The intermodulation distortion due to second order terms is commonly defined as

$$\text{IMD} = \left(\frac{V_{1,1}^2 + V_{1,-1}^2}{V_a^2 + V_b^2}\right)^{1/2},$$

where V_a and V_b are the amplitudes of the fundamentals and $V_{1,1}$ and $V_{1,-1}$ are the amplitudes of the sum and difference frequencies, respectively. *Figure 3* shows a particularly bad case of intermodulation distortion; harmonic distortion products are also visible. In calculating the IMD for this example, one must include the higher order IMD products to get an accurate measure of the distortion.

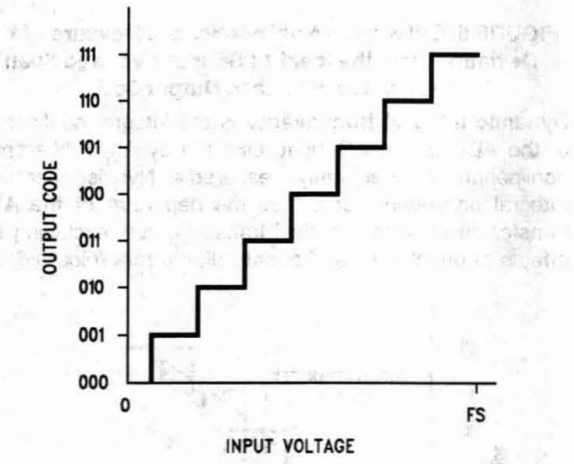

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FIGURE 2. The Nonlinear Nature of the ADC Transfer Curve is the Cause of THD and IMD

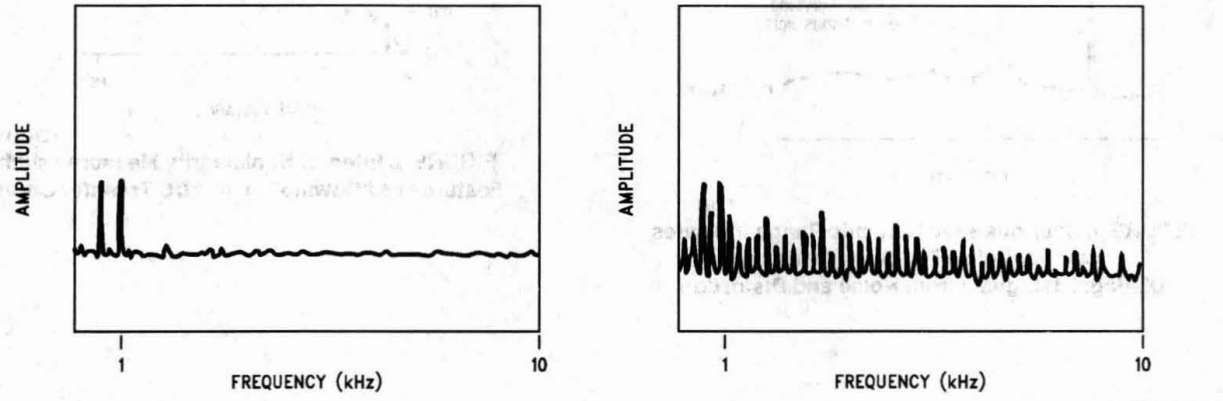

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FIGURE 3. An Input Signal with Frequency Components at 600 Hz and 1 kHz (left) Suffers Severe IMD after A/D Conversion (right)

The way IMD is specified for sampling ADCs varies from manufacturer to manufacturer. Variations occur in the number of IMD products that are included in the measurement, whether the two input frequencies have equal or unequal amplitudes, and whether the distortion is referenced to the rms sum of the input amplitudes or to the amplitude of the larger input. When comparing the IMD for several sampling ADCs, especially if they are from different manufacturers, one must know how it is measured in each case.

As one can infer from *Figure 3*, an ADC with a poor IMD specification would lead to very poor performance in an audio or spectral analysis application. Another reason for wanting a good IMD specification is to prevent the appearance of spurious signals produced by the coupling of strong out-of-band frequency components with signals in the band of interest.

Peak Harmonic is the amplitude, relative to the fundamental, of the largest harmonic resulting from the A/D conversion of a signal. The peak harmonic is usually, but not always, the second harmonic. It is usually specified in decibels.

Peak Harmonic or Spurious Noise is the amplitude, relative to the signal level, of the next largest frequency component (other than DC). Spurious noise components are noise components which are not integral multiples of the input signal, and are often aliased harmonics if the signal frequency is a significant fraction of the sampling rate. This specification is important because some applications require that the harmonics and spurious noise components be smaller than the lowest amplitude signal of interest.

Spurious-Free Dynamic Range is the ratio of the signal amplitude to the amplitude of the highest harmonic or spurious noise component; the input signal amplitude is at or near full scale *(Figure 4)*. This specification is simply the reciprocal of the "Peak harmonic or spurious noise" if in the measurement of that specification the input signal amplitude is at full scale.

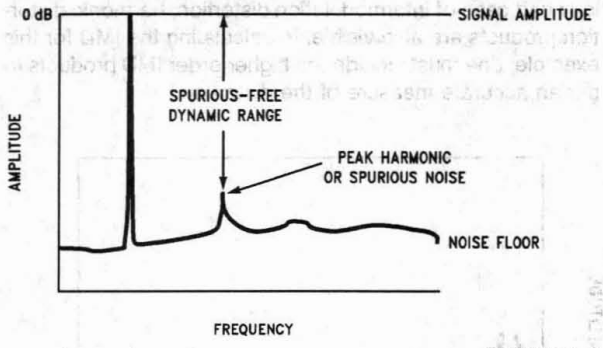

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FIGURE 4. Spurious-Free Dynamic Range Indicates How Far below Full Scale One Can Distinguish Signals from Noise and Distortion

Dynamic Differential Nonlinearity is the differential nonlinearity of the ADC for an AC input. It is frequently measured at the maximum sampling rate and with an input that is at the Nyquist frequency (half the sampling rate). Differential nonlinearity is the deviation from the ideal 1 LSB input voltage span that is associated with each output code *(Figure 5)*. It is measured using the histogram test.

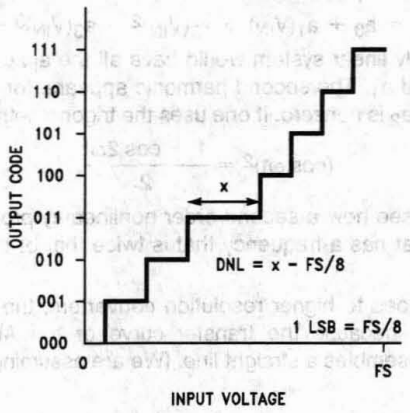

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FIGURE 5. Differential Nonlinearity is a Measure of the Deviation from the Ideal 1 LSB Input Voltage Span Associated with Each Output Code

Dynamic Integral Nonlinearity is the integral nonlinearity of the ADC for an AC input. Like the dynamic differential nonlinearity, it is frequently measured at Nyquist operation. Integral nonlinearity describes the departure of the ADC transfer curve from the ideal transfer curve, excluding the effects of offset, gain and quantization errors *(Figure 6)*.

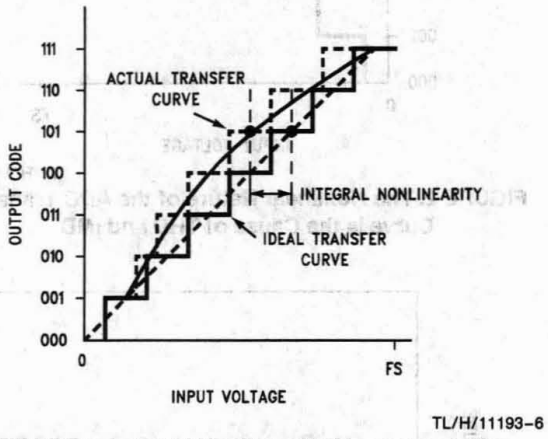

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FIGURE 6. Integral Nonlinearity Measures such Features as "Bowing" in an ADC Transfer Curve

Effective Number of Bits (ENOB) is a specification that is closely related to the signal-to-noise ratio. It is determined by measuring the S/N and using the equation

$$\text{ENOB} = \frac{\text{S/N} - 1.76}{6.02}$$

Some manufacturers define the effective number of bits using the SINAD instead of the signal-to-noise ratio. The ENOB generally decreases at high frequencies, and one frequently sees it plotted as a function of frequency, along with the SINAD *(Figure 7)*. The effective number of bits specification combines the effects of many of the other dynamic specifications. Errors resulting from dynamic differential and integral nonlinearity, missing codes, total harmonic distortion, and aperture jitter show up in the effective number of bits specification.

Full Power Bandwidth has several definitions. A common definition is that it is the frequency at which the S/N ratio has dropped by 3 dB (relative to its low frequency level) for an input signal that is at or near the maximum allowable level. This corresponds to a drop in the ENOB by ½ bit relative to its low-frequency level. Another definition is that it is the frequency at which the input signal appears to have been attenuated by 3 dB. Some manufacturers of flash converters define full power bandwidth as the frequency at which spurious or missing codes begin to appear. (Missing codes will occur if the dynamic differential nonlinearity is greater than +1 LSB.)

Small Signal Bandwidth is the frequency at which the S/N ratio has dropped by 3 dB for an input signal that is much smaller than the full-scale input, 20 dB or 40 dB below full-scale, for example. The small signal bandwidth is generally larger than the full power bandwidth. This will be the case if the bandwidth is slew rate limited, for example. The small signal bandwidth is important for those applications which do not require the conversion of large amplitude, high frequency signals. Relying on the full power bandwidth specification in these cases would constrain one to a smaller bandwidth than can actually be attained.

Sampling Rate, or throughput rate, depends on the length of the conversion time, acquisition time, and other time delays associated with carrying out a conversion. Signals which have frequencies exceeding the Nyquist frequency (half the sampling rate) will be aliased to frequencies below the Nyquist frequency. In order to prevent this signal degradation, one must sample the signal at a rate that is more than twice the highest frequency component in the signal, and/or process the signal through a low pass (anti-aliasing filter) before it reaches the ADC. In some applications one wants to sample at a rate much higher than the highest frequency component of interest in order to reduce the complexity of the anti-aliasing filter that is required.

SAMPLE-AND-HOLD CIRCUITRY SPECIFICATIONS

Aquisition time, aperture time, and aperture jitter are specifications that relate to the internal sampling circuitry within the ADC. These specifications can be easily explained with the aid of the simple sample-and-hold circuit shown in *Figure 8*. The S/H amplifier is in "Sample" mode when the switch is closed. In this case, the output of the amplifier is following the input. When the switch is opened, the S/H amplifier is in "Hold" mode; in this case, the output retains the input voltage that was present before the switch was opened.

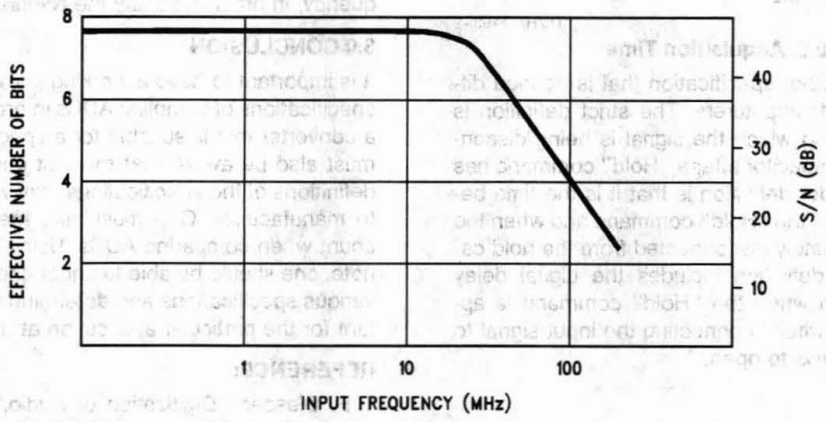

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FIGURE 7. Effective Number of Bits and S/N Generally Drop at High Frequencies

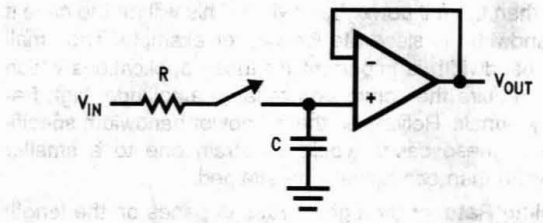

FIGURE 8. Simple S/H Circuit

Acquisition Time is the maximum time required to acquire a new input voltage once a "Sample" command has been given *(Figure 9)*. A signal is "acquired" when it has settled to within a specified tolerance, usually ½ LSB, of the input voltage. The maximum value of the acquisition time occurs when the hold capacitor must charge up from zero to its full-scale value (or the other way around, if it is larger). Acquisition time is important because it makes a significant contribution to the total time required to make a conversion.

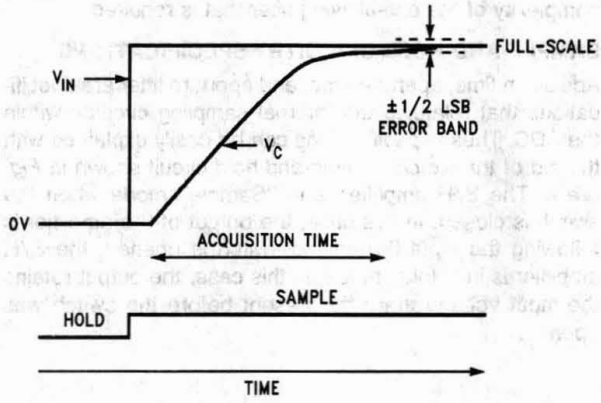

FIGURE 9. Acquisition Time

Aperture Time is another specification that is defined differently by different manufacturers. The strict definition is that it is the time during which the signal is being disconnected from the hold capacitor after a "Hold" command has been given. The broader definition is that it is the time between the application of the "Hold" command and when the signal has been completely disconnected from the hold capacitor. The second definition includes the digital delay which occurs between when the "Hold" command is applied and when the "switch" connecting the input signal to the hold capacitor *begins* to open.

Aperture time is important if one needs to acquire the value of a signal at a precise time. Since the signal is not held instantaneously upon application of the "Hold" command, this command must be given roughly an "aperture time" before one wants the signal to be "frozen".

The aperture time is not a limiting factor on the frequency for sinusoidal signals because for a sinusoidal signal, the voltage error caused by the aperture time manifests itself as a phase change, not an amplitude or frequency change.

Aperture Jitter is the uncertainty in the aperture time. Aperture jitter results from noise which is superimposed on the "Hold" command, which affects its timing. Aperture jitter is generally specified as an rms value, which represents the standard deviation in the aperture time.

The aperture jitter sets an upper limit on the maximum frequency sinusoidal signal that can be accurately converted.

In order not to lose accuracy, the rule of thumb is that the signal must not change by more than ±½ LSB during the aperture jitter time. Using a full-scale sinusoidal signal $V = A \sin(2\pi ft)$, we have

$$\frac{dV}{dt} = 2\pi fA \cos(2\pi ft) < \frac{\pm \frac{1}{2}\,LSB}{t_{aj}}$$

where t_{aj} is the aperture jitter. Since ½ LSB = $A/2^n$, where n is the resolution of the converter, we get

$$f < \frac{1}{2\pi \bullet 2^n \bullet t_{aj}}$$

As an example of using lthis criterion, a 12-bit converter whose S/H amplifier has an aperture jitter of 100 ps could convert full-scale signals having frequencies as high as 388 kHz. Of course, this would only be possible if the converter's sampling rate is at least twice as high as this frequency, in order to satisfy the Nyquist criterion.

3.0 CONCLUSION

It is important to have a working knowledge of the dynamic specifications of sampling ADCs in order to be able to select a converter that is suitable for a specific system need. One must also be aware that the test conditions and even the definitions of the specifications may vary from manufacturer to manufacturer. One must take these variations into account when comparing ADCs. Using the information in this note, one should be able to understand the meanings of the various specifications and determine which ones are important for the particular application at hand.

REFERENCE:

1. B. Blesser, "Digitization of Audio," *J. Audio Eng. Soc.*, vol. 26, no. 10, pp. 742-743 (1978).

APPENDIX

What follows is a table which presents values of the dynamic specifications for a number of National's sampling ADCs. Additional information, such as the values of S/N and THD at frequencies not listed here, can be found in the data sheets. The reference voltage that all of these parts are specified at is +5V, and the supply voltage is +5V for the ADC10461 and ADC10662 and ±5V for the ADC12441 and ADC12451. The only other test conditions included here are the input frequencies and signal amplitudes. Additional test conditions, such as the ambient temperature, can be found in the data sheets. Only the sampling ADCs whose dynamic specifications are tested and guaranteed are included here[1,2]. Additional sampling ADCs made by National are the ADC0820, ADC1061, ADC1241, ADC1251; and the ADC08031, ADC08061, ADC08131, ADC08161, ADC08231, ADC10061, and ADC1031 families.

Dynamic Specifications for Selected Sampling ADCs

Spec	ADC10461 (Note 1)	ADC10662 (Note 2)	ADC12441	ADC12451
Resolution	10	10	12 + sign	12 + sign
Conversion Time	900 ns	466 ns	13.8 μs	7.7 μs
S/N Unipolar (Note 3) Bipolar (Note 4)	58 dB	58 dB	71.5 dB 76.5 dB	68.7 dB 73.5 dB
THD Unipolar (Note 5) Bipolar (Note 6)	−60 dB	−60 dB	−75 dB −75 dB	−73.1 dB −78.0 dB
IMD Unipolar (Note 7) Bipolar (Note 8)			−73 dB −74 dB	−78 dB −78 dB
ENOB Unipolar (Note 9) Bipolar (Note 10)	9	9	11.6 12.4	11.1 11.9
Peak Harmonic Uni. (Note 11) or Spurious Noise Bi. (Note 12)			−82 dB −80 dB	−82 dB −80 dB
Full Power BW			20 kHz	20.67 kHz
Sampling Rate	800 kHz	1.5 MHz	55 kHz	83 kHz
Acquisition Time			3.5 μs	3.5 μs
Aperture Time			100 ns	100 ns
Aperture Jitter			100 ps_{rms}	100 ps_{rms}

Note 1: There are two and four input channel members of the ADC10461 family, namely the ADC10462 and ADC10464. These products have the same dynamic specifications as the ADC10461.

Note 2: The ADC10664 is a 4-input channel member of the ADC10662 family (the ADC10662 has two input channels). These two products have the same dynamic specifications.

Note 3: ADC10461: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC10662: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC12441: f_{IN} = 20 kHz; V_{IN} = 4.85 V_{p-p}
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = 4.85 V_{p-p}

Note 4: ADC12441: f_{IN} = 20 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = ±4.85V

Note 5: ADC10461: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC10662: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC12441: f_{IN} = 19.688 kHz; V_{IN} = 4.85 V_{p-p}
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = 4.85 V_{p-p}

Note 6: ADC12441: f_{IN} = 19.688 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = ±4.85V

Note 7: ADC12441: f_{IN1} = 19.375 kHz; f_{IN2} = 20.625 kHz; V_{IN} = 4.85 Vp-p
ADC12451: f_{IN1} = 19.375 kHz; f_{IN2} = 20 kHz; V_{IN} = 4.85 Vp-p

Note 8: ADC12441: f_{IN1} = 19.375 kHz; f_{IN2} = 20.625 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN1} = 19.375 kHz; f_{IN2} = 20 kHz; V_{IN} = ±4.85V

Note 9: ADC10461: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC10662: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC12441: f_{IN} = 20 kHz; V_{IN} = 4.85 V_{p-p}
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = 4.85 V_{p-p}

Note 10: ADC12441: f_{IN} = 20 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = ±4.85V

Note 11: ADC12441: f_{IN} = 20 kHz; V_{IN} = 4.85 V_{p-p}
ADC12451: f_{IN} = 20 kHz; V_{IN} = 4.85 V_{p-p}

Note 12: ADC12441: f_{IN} = 20 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN} = 20 kHz; V_{IN} = ±4.85V

Specifications and Architectures of Sample-and-Hold Amplifiers

National Semiconductor
Application Note 775

I. INTRODUCTION

Sample-and-Hold (S/H) amplifiers track an analog signal, and when given a "hold" command they hold the value of the input signal at the instant when the "hold" command was issued, thereby serving as an analog storage device. An ideal S/H amplifier would be able to track any kind of input signal, and upon being given a hold command store at its output, without delay, the precise value of the signal, and maintain this value indefinitely. Unfortunately, ideal S/H amps do not yet exist, and to be able to pick a S/H amp to suit a particular application, one must be familiar with how S/H amps are characterized, and how the S/H specifications will affect performance. In addition, it is helpful to be familiar with the common architectures that are used for S/H amps, as the architecture has a profound effect on the performance.

In this application note, we discuss the meaning and significance of the various specifications for S/H amps, and we also discuss several common S/H architectures, and how the performance is influenced by the architectures. In the appendix, we give a table which lists the key specifications for a number of S/H amps. Since the primary use of S/Hs is in data conversion, we will refer to such applications when discussing some of the specifications.

II. MEANING OF THE SPECIFICATIONS

When discussing S/H specifications, it is helpful to have the circuit diagram of a S/H amp at hand. *Figure 1* shows a schematic of the open loop configuration, which will be discussed later in more detail. Since a S/H amp has two modes (the sample mode and the hold mode), and two transitions between the modes (sample-to-hold and hold-to-sample), it is convenient to discuss the specifications in these four groupings. *Figure 2* shows a S/H timing diagram that displays these two modes and two mode transitions.

SAMPLE MODE SPECIFICATIONS

Offset Voltage is the deviation from zero of the output voltage when the input voltage is zero and the S/H amp is in sample mode. To maintain absolute accuracy in an A/D converter application, the offset voltage must be less than ½ LSB, or

$$V_{OS} < \frac{FS}{2^{n+1}},$$

where FS is full scale and n is the resolution of the analog-to-digital converter (ADC). Many S/H amps have provision for nulling the offset voltage; however, manual nulling can be expensive. Sometimes the offset is specified as an input offset voltage; this is particularly useful if the S/H can be configured for a gain other than unity.

Gain Error is the fractional voltage difference between the input voltage and the output voltage (excluding the effects of offset voltage) when the S/H amp is in sample mode; here we assume the ideal gain is unity. If absolute accuracy is required in an A/D application, the gain error should be less than ½ LSB, or

$$\Delta A_V = \frac{V_{OUT} - V_{IN}}{V_{IN}} < \frac{1}{2^{n+1}},$$

where n is the resolution of the converter.

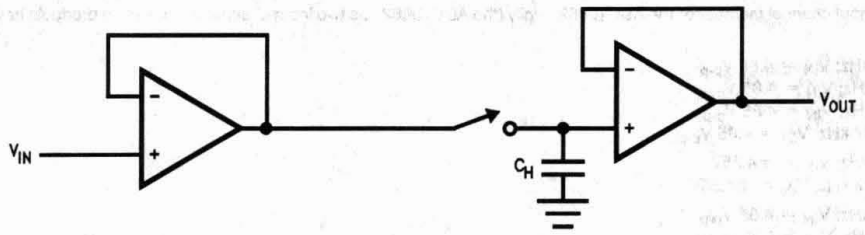

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FIGURE 1. A Simple S/H Amplifier Consists of a Switch, Hold Capacitor, and Input and Output Buffers

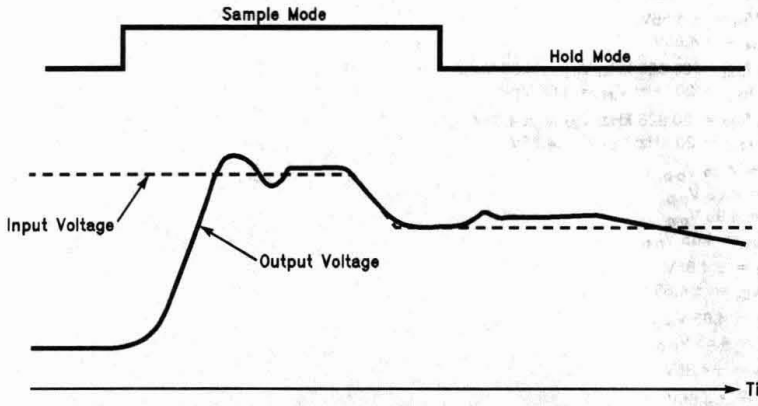

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FIGURE 2. S/H Timing Diagram Showing the Two Modes and the Two Transitions Between the Modes

Gain Linearity Error is the maximum deviation of the S/H's transfer curve from an ideal straight line connecting the end points of the transfer curve (the effects of offset and gain error are excluded). Spectral distortion is a consequence of gain linearity error in the S/H.

Full-Power Bandwidth is commonly defined in two ways. Some manufacturers define it as the frequency at which the voltage gain of the S/H amplifier drops by 3 dB relative to the gain at dc for a full-scale input. Others derive the full power bandwidth from a measurement of the S/H's slew rate. According to this definition, the full power bandwidth is equal to the frequency of the full-scale sine wave which has its maximum rate of change equal to the slew rate. This is given by

$$BW_{fp} = \frac{SR}{2\pi V_p}$$

where $2V_p$ is full scale and SR is the slew rate of the S/H.

Small Signal Bandwidth is the frequency at which the voltage gain of the S/H amplifier drops 3 dB relative to the gain at dc for an input that is much smaller than full scale, such as 20 dB or 40 dB below full scale. The small signal bandwidth is generally larger than the full power bandwidth; this would be the case if the full-power bandwidth is slew rate limited, for example. The small signal bandwidth is important for those applications which do not require the conversion of large amplitude, high frequency signals. Relying on the full power bandwidth specification in these cases would constrain one to a smaller bandwidth than can actually be attained in practice.

Slew Rate is the maximum rate of change of the output voltage when the S/H amplifier is in sample mode. Because the slew rate depends on the value of the hold capacitor, this capacitance must be specified if the hold capacitor is external. The slew rate is important because it affects the full-power bandwidth and acquisition time of the S/H.

SAMPLE-TO-HOLD TRANSITION SPECIFICATIONS

Aperture Time, also known as aperture delay, is a specification that is defined differently by different manufacturers. The strict definition is that it is the time during which the signal is being disconnected from the hold capacitor after a hold command has been given *(Figure 3).* The broader definition is that it is the time between the application of the hold command and when the signal has been completely disconnected from the hold capacitor. The second definition includes the digital delay which occurs between when the hold command is applied and when the switch connecting the input signal to the hold capacitor *begins* to open.

Unlike aperture jitter, the aperture time is not a limiting factor on the maximum frequency for sinusoidal signals because for a sinusoidal signal, the voltage error caused by the aperture time manifests itself as a phase change, not an amplitude or frequency change.

Effective Aperture Delay Time is the time delay between the generation of the hold command and the appearance at the input of the final "held" voltage that exists on the hold capacitor *(Figure 3).* If precise timing is required, the hold command must be given an "effective aperture delay time" before the instant at which the input value is desired.

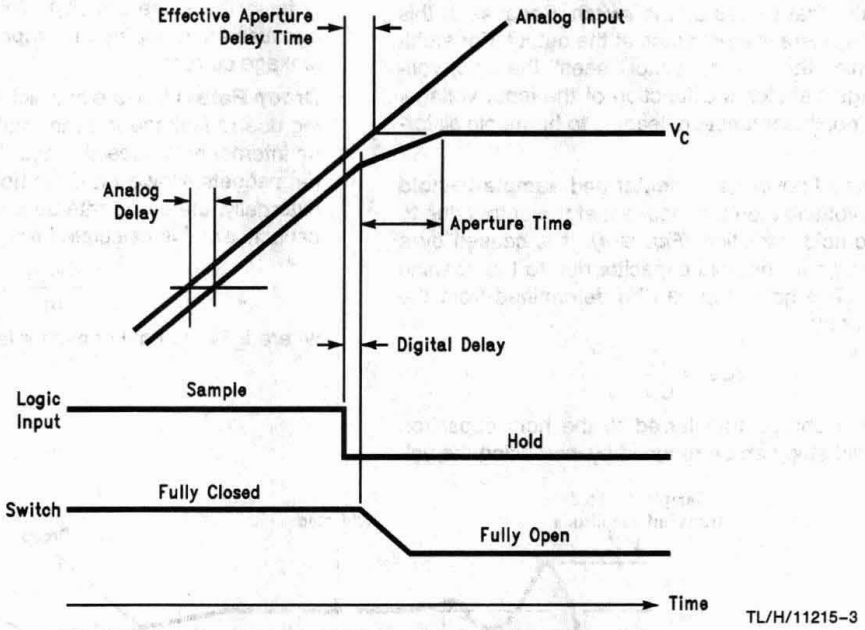

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FIGURE 3. Aperture Time and Effective Aperture Delay Time

Aperture Jitter, also known as **aperture uncertainty,** is the uncertainty in the aperture time. Aperture jitter results from noise which is superimposed on the hold command, which affects its timing. Aperture jitter is often specified as an rms value, which represents the standard deviation in the aperture time.

The aperture jitter sets an upper limit on the maximum frequency sinusoidal signal that can be accurately sampled by a S/H. In order not to lose accuracy, the rule of thumb is that the signal must not change by more than $\pm\frac{1}{2}$ LSB during the aperture jitter time. Using a full-scale sinusoidal signal $V = A \sin(2\pi ft)$, we have

$$\frac{dV}{dt} = 2\pi fA\cos(2\pi ft) < \frac{\pm\frac{1}{2}\,LSB}{t_{aj}}$$

where A is half the analog input voltage range and t_{aj} is the aperture jitter. Since $\frac{1}{2}$ LSB $= A/2^n$, where n is the resolution of the converter, we get

$$f < \frac{1}{2\pi \times 2^n \times t_{aj}}$$

As an example of using this criterion, a 12-bit converter whose S/H amplifier has an aperture jitter of 100 ps could convert full-scale signals having frequencies as high as 388 kHz. Of course, this would only be possible if the converter's sampling rate is at least twice as high as this frequency, in order to satisfy the Nyquist criterion.

Charge Transfer, or **charge injection,** is the amount of charge transferred to the hold capacitor upon opening the switch after a hold command has been given. It is caused by capacitive coupling between the hold capacitor and the gate of the transistor that serves as the switch. Because of this charge transfer, there is a hold step at the output. For architectures in which the hold capacitor "sees" the input voltage, the charge transfer is a function of the input voltage, and can be a nonlinear function, leading to harmonic distortion.

Hold Step, also known as **pedestal** and **sample-to-hold offset,** is the voltage step that appears at the output due to the sample-to-hold transition *(Figure 4).* It is caused by a transfer of charge to the hold capacitor due to the opening of the switch. The hold step can be determined from the charge transfer by

$$V_{HS} = \frac{Q}{C_H}$$

where Q is the charge transferred to the hold capacitor. Hence, the hold step can be reduced by increasing the value of the hold capacitor. This will, however, result in a larger acquisition time. For A/D applications, it is desirable that the hold step be independent of the input voltage and less than $\frac{1}{2}$ LSB.

Hold Mode Settling Time is the time required for the output to settle within a specified error band after a hold command has been given. This error band is commonly specified as 1%, 0.1% or 0.01% of a full-scale step input. For A/D converter applications, one needs the output to settle within $\pm\frac{1}{2}$ LSB before a conversion is started. The hold mode settling time is also important because the sum of the acquisition time, the hold mode settling time, and the A/D conversion time determines the maximum sampling rate of the S/H-ADC system. (If the conversions are pipelined, the sampling rate can be higher).

$$(f_s)_{max} = \frac{1}{t_{aq} + t_{HS} + t_c}$$

Sample-to-Hold Transient is the transient that appears at the output due to a sample-to-hold transition. The maximum amplitude of the transient is usually specified. S/Hs used to deglitch the output of digital-to-analog converter must have a small sample-to-hold transient.

HOLD MODE SPECIFICATIONS

Hold Capacitor Leakage Current is the current which flows in or out of the hold capacitor while the S/H amplifier is in hold mode. The leakage current consists of three parts: leakage through the dielectric of the hold capacitor, leakage through the analog switch, and the input bias current of the output amplifier. (The leakage currents do not all necessarily have the same polarity). This specification is important because the droop rate is proportional to the hold capacitor leakage current.

Droop Rate is the rate at which the output voltage is changing due to leakage from the hold capacitor. If the S/H has an internal hold capacitor, the droop rate is specified in the data sheets. However, if the hold capacitor must be added externally, the droop rate depends on the value of the hold capacitor and is calculated from the equation

$$\frac{dV_{CH}}{dt} = \frac{I_L}{C_H}$$

where I_L is the hold capacitor leakage current.

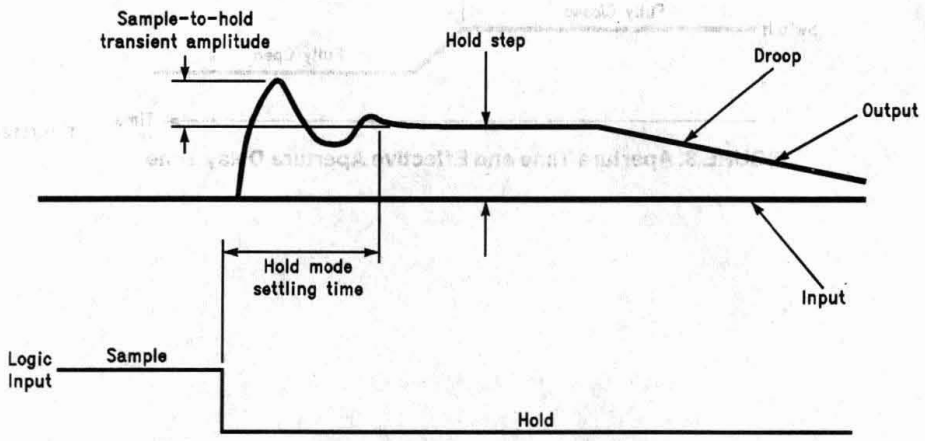

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FIGURE 4. Sources of Error in Hold Mode and during the Sample-to-Hold Transition

The droop rate is important for applications where the sampled voltage must be held within a specified error band for long periods of time. In A/D applications, one does not want the output to droop by more than ½ LSB during the conversion time. For these applications, the maximum allowable droop rate of the S/H is given by

$$\frac{dV_{CH}}{dt} < \frac{\frac{1}{2}LSB}{t_c} = \frac{FS}{(2^{n+1})\,t_c}$$

where FS is the full-scale voltage of the ADC, n is its resolution, and t_c is the ADC conversion time. The droop rate can be reduced by increasing the value of the hold capacitor, but this results in a higher acquisition time.

Feedthrough Attenuation Ratio is the fraction of the input signal that appears at the output while the S/H amplifier is in hold mode. The feedthrough attenuation ratio is generally specified for a specific frequency of input signal. For A/D applications, the feedthrough must be less than ½ LSB for a full amplitude input. Hence, the feedthrough attenuation ratio must be at least

$$A_F > 20 \log (2^{n+1})\ dB$$

which can be simplified to $A_F > 6(n+1)$ dB, where n is the resolution of the converter.

HOLD-TO-SAMPLE TRANSITION SPECIFICATIONS

Acquisition Time is the maximum time required to acquire a new input voltage once a sample command has been given *(Figure 5).* A signal is "acquired" when it has settled within a specified error band around its final value of output voltage. The error band is usually either 0.1%, 0.01%, 1 mV, or ½ LSB (in applications that involve an ADC). The maximum value of the acquisition time occurs when the hold capacitor must charge to a full-scale voltage change. The acquisition time depends on the value of the hold capacitor, and this value must be specified if the hold capacitor is supplied externally. The acquisition time can be reduced by choosing a smaller hold capacitance; however, this will increase the hold step and droop rate.

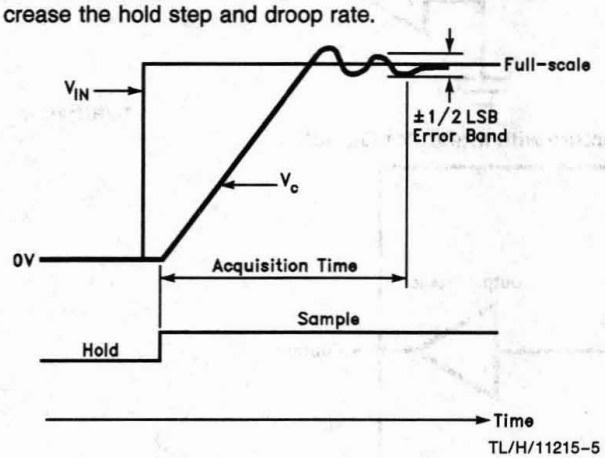

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FIGURE 5. Acquisition Time

III. SAMPLE-AND-HOLD ARCHITECTURES

The symbol that is frequently used for the S/H amplifier in system block diagrams is a switch in series with a capacitor *(Figure 6).* Although the switch can control the mode of the device, and the capacitor can store a voltage, a S/H using just these components would have very poor performance. By studying the deficiencies of such a configuration, one can better appreciate the components that are added to this basic core to comprise a practical S/H amplifier.

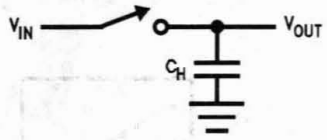

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FIGURE 6. S/H Symbol

First, when in sample mode the charging time of the hold capacitor for the S/H in *Figure 6* is dependent on the source impedance of the input. A large source impedance would give a large RC time constant, leading to a high acquisition time. To ameliorate this effect, one buffers the hold capacitor from the input with an operational amplifier (assuming that the op amp is capable of driving a capacitive load). The acquisition time will then be independent of the source impedance, and will in fact be low due to the low output impedance of an operational amplifier.

Second, when in hold mode the hold capacitor will discharge through the load. Hence, the droop rate will be load dependent and could be very high. To ameliorate this problem, one buffers the hold capacitor from the output with an op amp. the droop rate will then be independent of the load, and will actually be rather low, due to the large input impednace of an op amp.

Hence, in addition to a switch and a hold capacitor, a practical S/H amplifier must include input and output buffers. The two main variations of this structure, the open-loop and closed-loop architectures, differ in the manner of their feedback.

In the open-loop architecture *(Figure 7),* the input and output buffer amps are each configured as voltage followers. The advantage of this architecture is its speed—the acquisition time and settling time are short because there is no feedback between the buffer amps. The disadvantage of this architecture is in its accuracy, which suffers because of the lack of feedback, causing the dc errors of both amplifiers to add.

For applications requiring high accuracy, one can use the closed loop-architecture, with either a follower output *(Figure 8)* or an integrator output *(Figure 9).* The feedback significantly improves the accuracy of the S/H relative to the open-loop configuration, although the speed is somewhat less.

In both the open-loop architecture and the closed-loop architecture with follower output, the charge transfer, and hence the hold step, is a function of the input voltage. This is because the hold capacitor is connected to the input signal (through the input buffer amp). The closed-loop architecture with integrator output ameliorates this problem by connecting the hold capacitor to virtual ground instead of the nput signal. Hence the charge transfer is constant.

A new architecture which combines the speed of the open-loop configuration and the accuracy of the closed-loop configuration is the current-multiplexed architecture shown in *Figure 10*. The LF6197, National's High Performance VIP™ Sample-and-Hold Amplifier used this architecture. This architecture provides for a cancellation of charge injection, allowing one to use a small hold capacitor to get high speeds without the disadvantage of a large hold step.

In the sample mode, the transconductance input stage g_{m1} is connected to the output buffer, while switches S2 and S3 are closed, thereby shorting the dummy capacitor C_D and grounding one end of the hold capacitor, allowing it to charge. The hold command connects input stage g_{m2} to the output buffer and opens switches S2 and S3. The voltage differential caused by charge injection into the hold capacitor is cancelled by an equal but opposite polarity of charge injection into the dummy capacitor, which is the same value as the hold capacitor. Hence, the common mode rejection of g_{m2} results in a greatly reduced hold step.

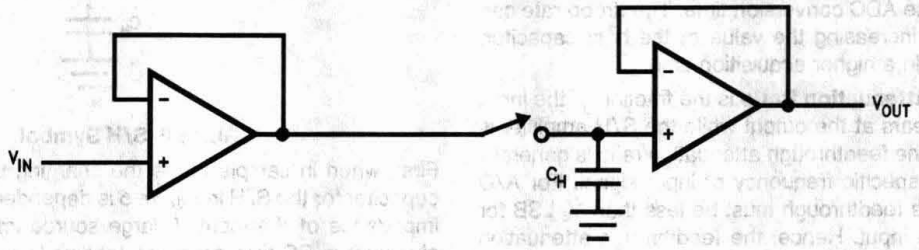

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FIGURE 7. Open-Loop Architecture

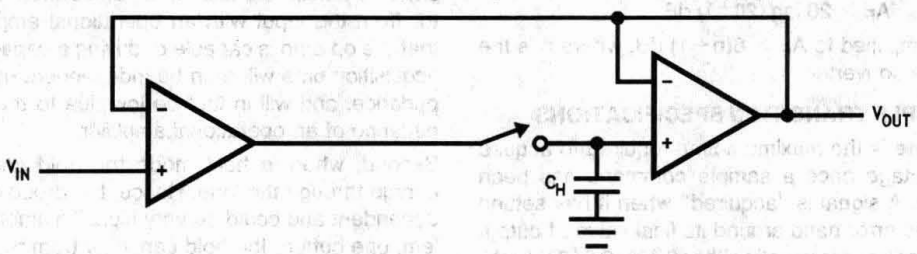

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FIGURE 8. Closed-Loop Architecture with Follower Output

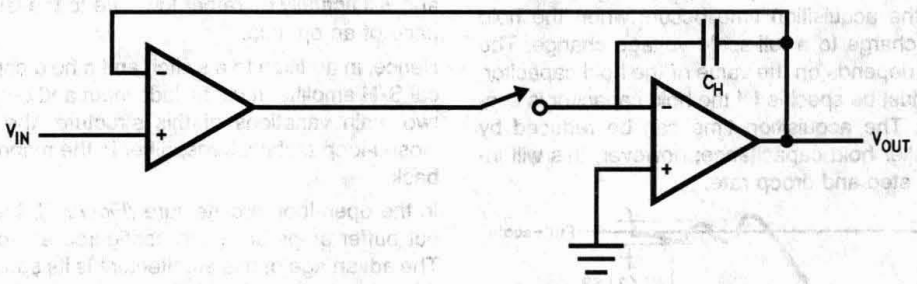

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FIGURE 9. Closed-Loop Architecture with Integrator Output

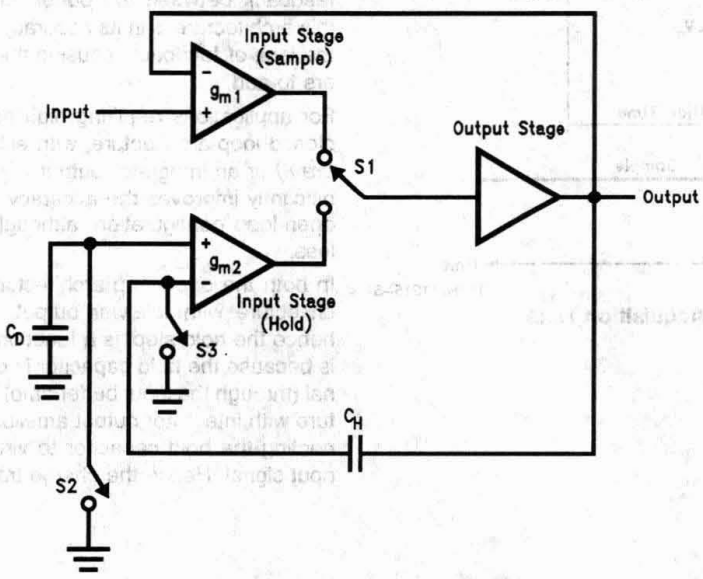

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FIGURE 10. Current Multiplexed Architecture

IV. CONCLUSION

The selection of a S/H amplifier for a particular application requires an understanding of how S/Hs are specified and how a particular specification will affect system performance. When comparing S/H amplifiers one must also be aware that the test conditions and even the definitions of the specifications may vary from manufacturer to manufacturer. A clear understanding of the meanings of the specifications should make it easier to compare S/Hs that are tested using different definitions of the specifications.

APPENDIX

What follows is a table which presents values of the specifications for a number of National's S/H amplifiers. Additional information, such as the values of the acquisition time and hold mode settling time at other hold capacitor values and to other accuracies, can be found in the data sheets. Additional S/H amplifiers made by National are the LH0023, LH0043, and LH0053.

SPECIFICATIONS FOR SELECTED S/H AMPLIFIERS

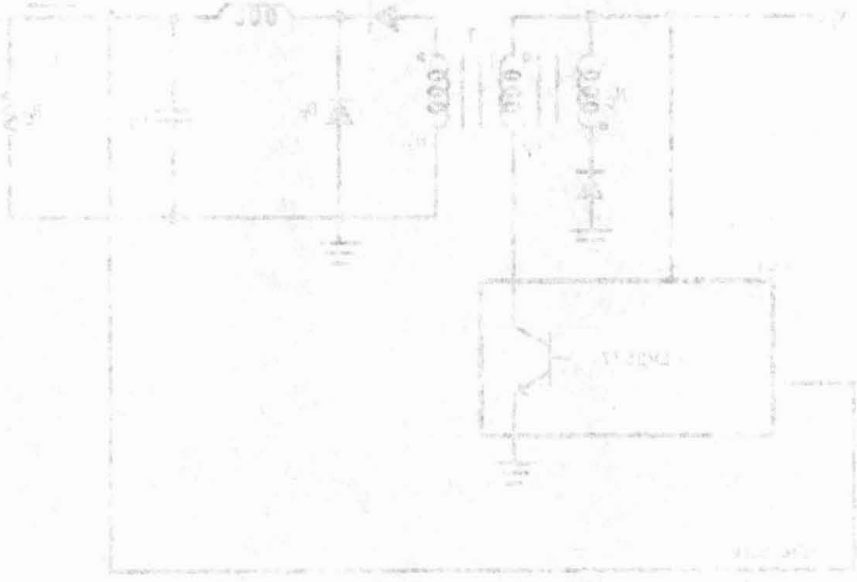
Spec (Note 1)	LF398	LH4860	LF6197
Architecture	Closed-Loop, Follower Output	Closed-Loop, Integrator Output	Current Multiplexed
Input Offset Voltage	±2 mV	±0.5 mV	±3 mV
Gain Error	0.004%	±0.005%	0.03%
Small Signal BW		16 MHz	25 MHz
Slew Rate		300 V/μs	145 V/μs
Aperture Time	200 ns	6 ns	4 ns
Aperture Jitter		35 ps_{rms}	8 ps_{rms}
Hold Step (Note 2)	±1.0 mV	±2.5 mV	±10 mV
Hold Mode Settling Time to 0.01%	1 μs	60 ns	50 ns
Hold Capacitor Leakage Current	30 pA	5 pA	6 pA
Droop Rate		±0.5 μV/μs	0.6 μV/μs
Feedthrough Attenuation Ratio at 1 kHz	90 dB		83 dB
Acquisition Time to 0.1% (Notes 3, 4)	4 μs	100 ns	130 ns

Note 1: The table lists the typical values of these specifications.

Note 2: LF398: C_H = 0.01 μF, V_{OUT} = 0V.

Note 3: ΔV_{OUT} = 10V.

Note 4: LF398: C_H = 1000 pF.



20 Watt Simple Switcher Forward Converter

National Semiconductor
Application Note 776
Frank DeStasi
Tom Gross

A 20W, 5V at 4A, step-down regulator can be developed using the LM2577 Simple Switcher IC in a forward converter topology. This design allows the LM2577 IC to be used in step-down voltage applications at output power levels greater than the 1 A LM2575 and 3 A LM2576 buck regulators. In addition, the forward converter can easily provide galvanic isolation between input and output.

The design specifications are: V_i Range : 20V–24V
V_o : 5V
$I_{o(max)}$: 4A
ΔV_o : 20 mV

With the input and output conditions identified, the design procedure begins with the transformer design, followed by the output filter and snubber circuit design.

TRANSFORMER DESIGN

1. Using the maximum switch voltage, input voltage, and snubber voltage, the transformer's primary-to-clamp windings turns ratio is calculated:

$$V_{SW} \geq V_{i_{max}} + V_{i_{max}} (N_p/N_c) + V_{snubber}$$
$$N_p/N_c \leq (V_{SW} - V_{i_{max}} - V_{snubber})/V_{i_{max}}$$
$$N_p/N_c \leq (60V - 24V - 5V)/24V = 1.29$$
$$\Delta \text{ let } N_p/N_c = 1.25$$

The $V_{snubber}$ voltage is an estimate of the voltage spike caused by the transformer's primary leakage inductance.

2. The duty cycle, t_{on}/T, of the switch is determined by the volt-second balance of the primary winding.

During t_{on};
$$V_i = L_p (\Delta i/T_{ON}) \longrightarrow \Delta i = (V_i/L_p)\, t_{on}$$
During t_{off};
$$V_i = (N_p/N_c) = L_p (\Delta i/t_{off}) \longrightarrow \Delta i = (N_p/N_c)(V_i/L_p)\, t_{off}$$
Setting Δi's equal;
$$(V_i/L_p)\, t_{on} = (N_p/N_c)(V_i/L_p)\, t_{off}$$
$$t_{on}/t_{off} = N_p/N_c$$
$$\text{Since } D = t_{on}/T = t_{on}/(t_{on} + t_{OFF})$$
$$\text{max. duty cycle} = D_{max} = (N_p/N_c)/[(N_p/N_c) + 1]$$
$$D_{max} = (1.25)/(1.25 + 1) = 0.56\ (56\%)$$

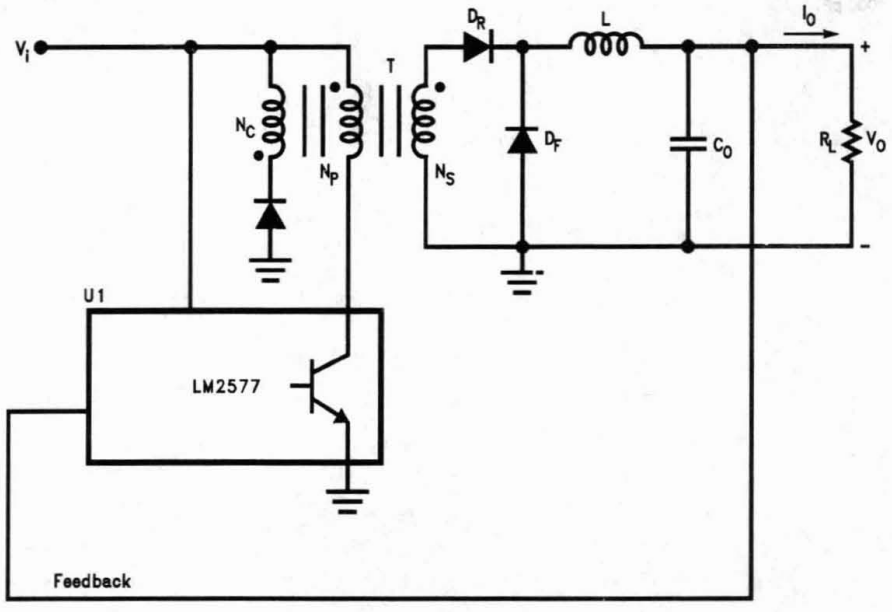
3. The output voltage equations of a forward converter provides the transformer's secondary-to-primary turns ratio:

$$V_o + V_{diode} \leq V_{i_{min}} \times D_{max} (N_s/N_p)$$
$$N_s/N_p \geq (V_o + V_{diode})/(V_{i_{min}} \times D_{max})$$
$$N_s/N_p \geq (5.5V)/(20V)(56\%) = 0.49$$
$$\Delta \text{let } N_s/N_p = 0.5$$

4. Calculate transformer's primary inductance by finding the maximum magnetizing current (Δi_{Lp}) that does not allow the maximum switch current to exceed it's 3 A limit (capital I for DC current, Δi for AC current, and lower case i for total current):

$$i_{sw} = i_{pri} = i_{Lo'} + \Delta i_{Lp}$$

Basic Forward Converter



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where i_{Lo}, is the reflected secondary current and Δi_{LP} is the primary inductance current.

$$i_{Lo'} = i_{Lo}(N_S/N_p) \quad (i_{Lo} \text{ reflected to primary})$$

$$i_{Lo} = I_{Lo} \pm \Delta i_{Lo}/2$$

Δi_{Lo} is the output inductor's ripple current

$$I_{Lo} = I_o \text{ (the load current)}$$

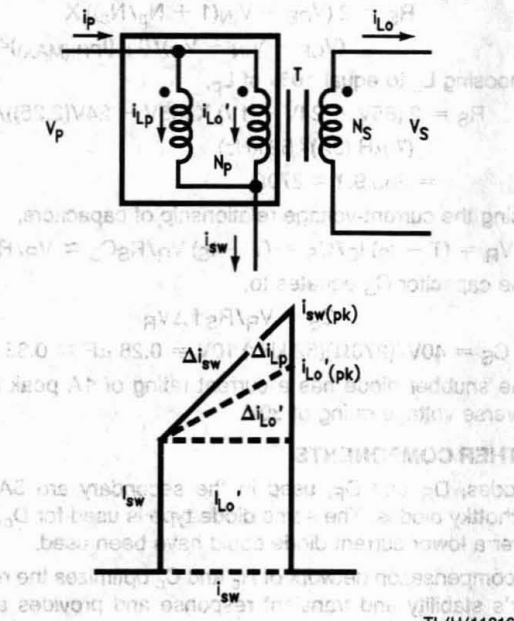
$$i_{Lo'} = (I_o \pm \Delta i_{Lo}/2)(N_S/N_p)$$

$$i_{Lo'(pk)} = (I_{o(max)} + \Delta i_{Lo}/2)(N_S/N_p)$$

$$i_{sw} = I_{sw} + \Delta i_{sw}$$

$$i_{sw(pk)} = i_{Lo'(pk)} + \Delta i_{LP(pk)}$$

$$i_{sw(pk)} = (I_{o(max)} + \Delta i_{Lo}/2)(N_S/N_p) + \Delta i_{LP(pk)}$$



TL/H/11216–2

Using standard inductors, a good practical value to set the output inductor current (Δi_{Lo}) to is 30% of the maximum load current (I_o). Thus;

$$i_{sw(pk)} = (I_{o(max)} + 0.15\Delta i_{Lo})(N_S/N_p) + \Delta i_{LP(pk)}$$

$$\Delta i_{LP(pk)} = i_{sw(pk)} - (I_{o(max)} + 0.15\Delta i_{Lo})(N_S/N_p)$$

$$\Delta i_{LP(pk)} = 3A - (4A + 0.15 \times 4A)(0.5) = 0.7A$$

$$L_p = V_{pri} \times \Delta t/\Delta i = (V_i - V_{sat})(t_{on}/\Delta i_{LP(pk)})$$

$$= (V_{i(max)} - V_{sat})(D_{max}/(\Delta i_{LP(pk)} \times f)$$

$$= (24V - 0.8V)(0.56/0.7 \times 52\ kHz)$$

$$L_p = 357\ \mu H \qquad \Delta \text{let } L_p = 350\ \mu H$$

OUTPUT FILTER—INDUCTOR

The first component calculated in the design is the output inductor, using the current-to-voltage relationship of an inductor:

$$V_L = L_o\,(\Delta i_{Lo}/t_{on})$$

Choosing an inductor ripple current value of $0.3I_o$ and a maximum output current of 4A:

$$\Delta i_{Lo} = 0.3\,(4A) = 1.2A$$

During t_{on};

$$V_L = V_S - V_D - V_o \text{ [where } V_s = (V_i - V_{sat})(N_s/N_p)]$$

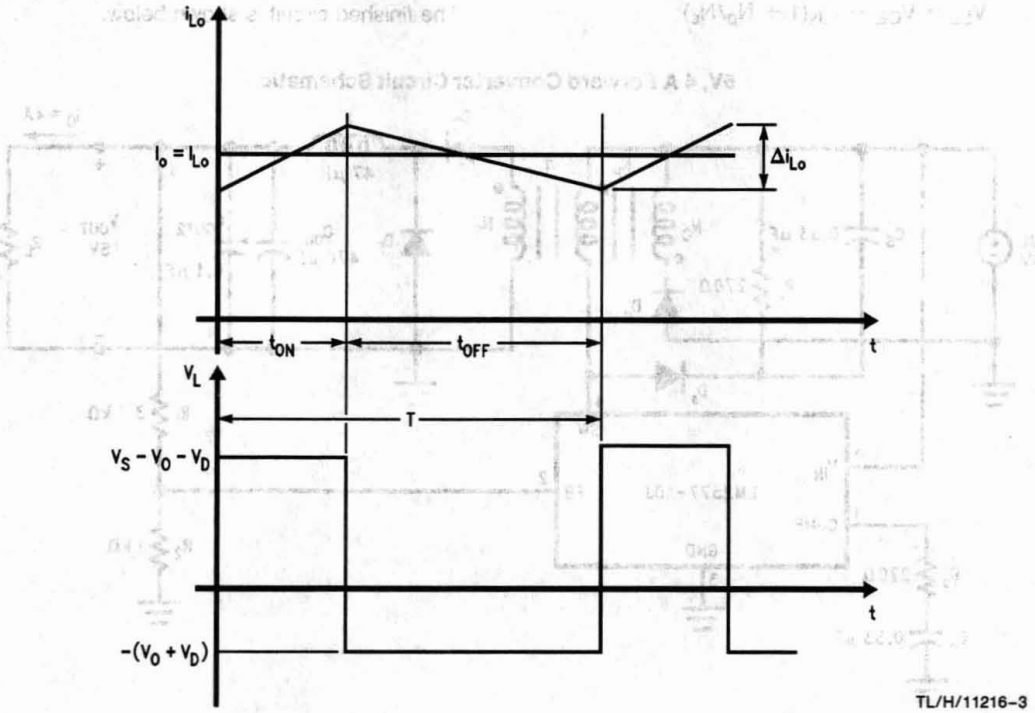
Thus,

$$[(V_i - V_{sat})(N_s/N_p) - V_d - V_o] = L_o\,(\Delta i_{Lo}/D)\,f$$

$$L_o = [(V_i - V_{sat})(N_s/N_p) - V_d - V_o] \times D/\Delta i_{Lo} \times f$$

$$L_o = [(24V - 0.8V)(0.5) - 0.5V - 5V]\ 56\%/1.2A \times 52\ kHz$$

$$L_O = 55\ \mu H \qquad \Delta \text{ let } L_o = 60\ \mu H$$



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OUTPUT FILTER—CAPACITOR

Since the output capacitor's current is equal to inductor's ripple current, the output capacitor's value can be found using the inductor's ripple current. Starting with the current-voltage relationship, the output capacitance is calculated:

$$\Delta V_O = 1/C_O \int i\,dt$$
$$= \Delta i_{LO}/\,4C_O\,(TR/2)$$
$$= (\Delta i_{LO} \bullet T)/\,8C_O$$
$$C_O = (\Delta i_{LO} \bullet T)/\,8\Delta V_O$$

However, the equivalent series resistance (ESR) of the capacitor multiplied by the inductor's ripple current creates a parasitic output ripple voltage equal to:

$$\Delta V_O = ESR_{CO} \bullet \Delta i_{LO} = ESR_{CO} \bullet 0.3\, I_O$$

This parasitic voltage is usually much larger than the inherent ripple voltage. Hence, the output capacitor parameter of interest, when calculating the output ripple voltage, is the equivalent series resistance (the capacitance of the output capacitor will be determined by the frequency response analysis). Using a standard-grade capacitor with ESR of 0.05Ω produces a total output ripple voltage of:

$$\Delta V_O = 0.05\Omega \bullet 1.2A \approx 60\ mV$$

To get output ripple voltage of 20 mV or less (as was part of the design specs) requires a capacitor with ESR of less than 17 mΩ.

SNUBBER CIRCUIT

A snubber circuit (C_S, R_S, D_S) is added to reduce the voltage spike at the switch, which is caused by the transformer's leakage inductance. It is designed as follows: when the switch is off,

$$V_R = V_{CE} - V_{IN} - V_D$$
$$V_{LL} = V_D + V_R - V_{IN}(N_p/N_c)$$

Substituting for V_R, the voltage across the leakage inductance, V_{LL}, is,

$$V_{LL} = V_{CE} - V_{IN}(1 + N_p/N_c)$$

Using the current-voltage relationship of inductors,

$$t_S = I_{PRI}(L_L/V_{LL})$$

Substituting for V_{LL},

$$t_S = I_{PRI}\, L_L/(V_{CE} - V_{IN}(1 + N_p/N_c))$$

Calculating for the average leakage inductance current, $I_{LL(AVE)}$,

$$I_{LL(AVE)} = I_{PRI(MAX)}\,(t_S)/2T$$
$$= I_{PRI(MAX)}^2\, L_L f/2(V_{CE} - V_{IN}(1 + N_p/N_c))$$

Solving for the snubber resistor;

$$R_S = V_R/I_{LL(AVE)}$$

Substituting $I_{LL(AVE)}$ and V_R results in,

$$R_S = 2\,(V_{CE} - V_{IN}(1 + N_p/N_c))\ X$$
$$(V_{CE} - V_{IN} - V_D)/(L_L\,(I_{PRI(MAX)})^2 f)$$

Choosing L_L to equal 10% of L_p,

$$R_S = 2\,(65V - 24V - 1V)\ X\ (65V - 24V(2.25))/$$
$$(7\ \mu H\ (3A)^2\ 52\ kHz)$$
$$= 268.9\Omega \approx 270\Omega$$

Using the current-voltage relationship of capacitors,

$$\Delta V_R = (T - t_S)\, I_C/C_S = (T - t_S)\, V_R/R_S C_S \approx V_R/R_S C_S f$$

The capacitor C_S equates to,

$$C_S = V_R/R_S\, f\, \Delta V_R$$
$$C_S = 40V/(270\Omega)(52\ kHz)\ 10V = 0.28\ \mu F \approx 0.33\ \mu F$$

The snubber diode has a current rating of 1A peak and a reverse voltage rating of 30V.

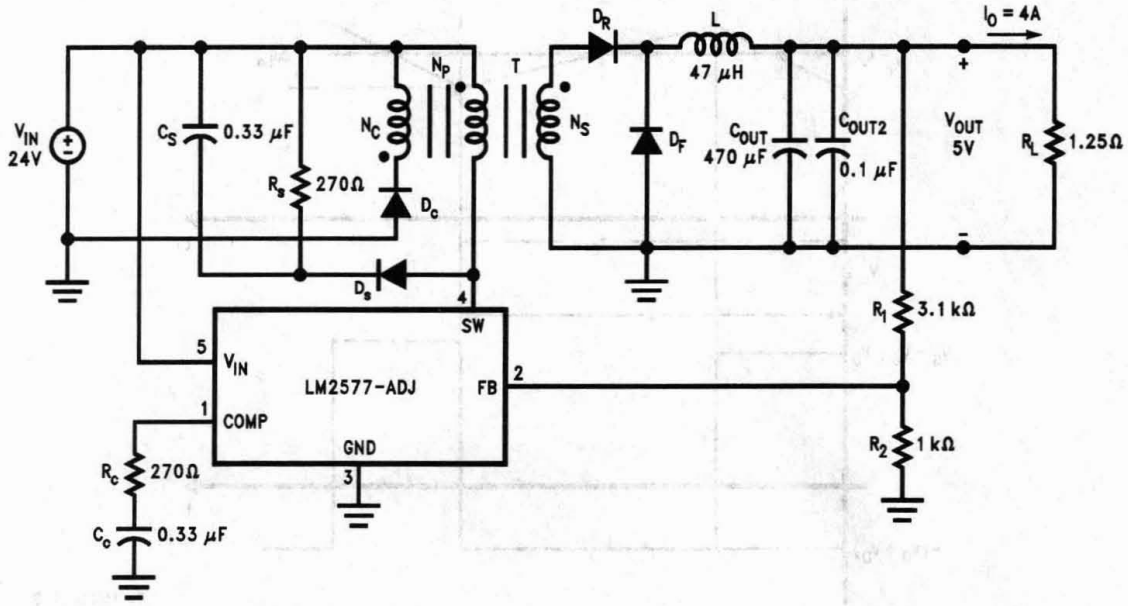
OTHER COMPONENTS

Diodes, D_R and D_F, used in the secondary are 5A, 30V Schottky diodes. The same diode type is used for D_C, however a lower current diode could have been used.

A compensation network of R_C and C_C optimizes the regulator's stability and transient response and provides a soft-start function for a well-controlled power-up.

The finished circuit is shown below.

5V, 4 A Forward Converter Circuit Schematic



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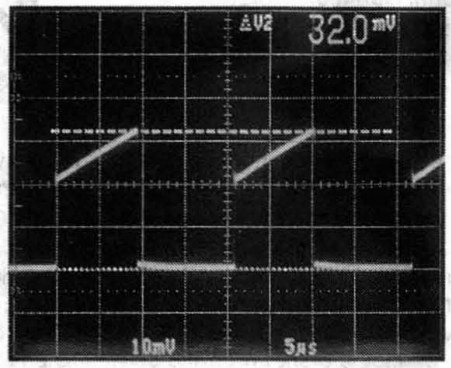

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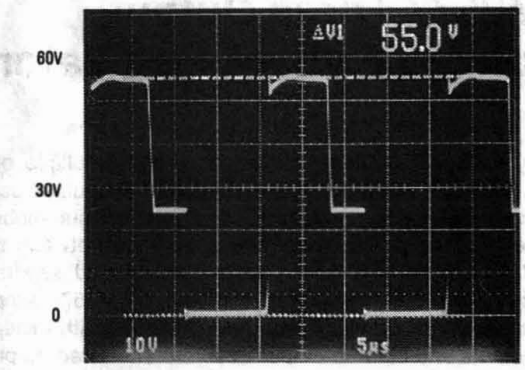
Switch Current

Vertical: 1 A/div
Horizontal: 5 μs/div



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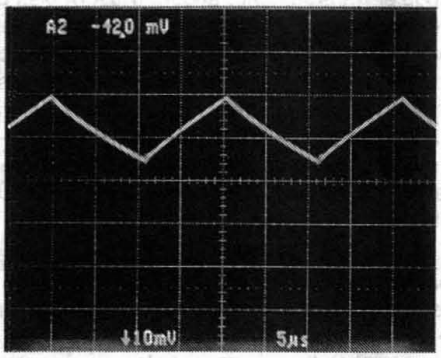
Switch Voltage

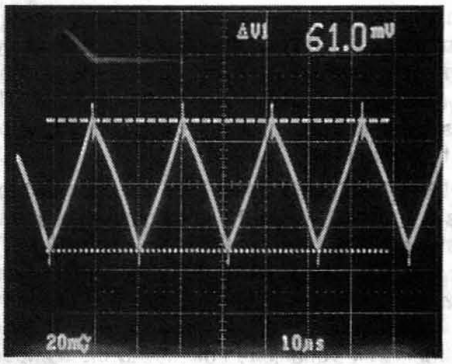
Vertical: 10 V/div
Horizontal: 5 μs/div



TL/H/11216–7

Inductor Current

Vertical: 1 A/div
Horizontal: 5 μs/div



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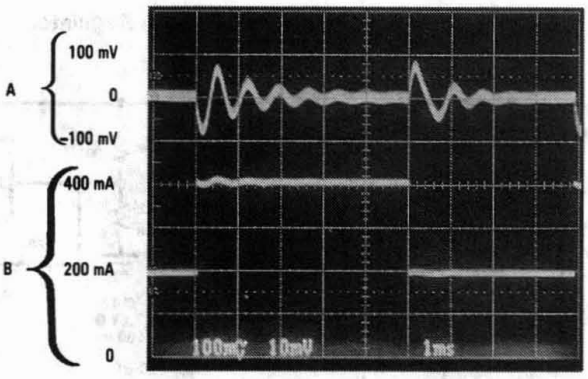
Output Ripple Voltage

Vertical: 20 mV/div
Horizontal: 10 μs/div



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Load Step Response

A: Output Voltage Change, 100 mV/div
B: Output Current, 200 mA/div
Horizontal: 10 ms/div

LM2577 Three Output, Isolated Flyback Regulator

National Semiconductor
Application Note 777
Tom Gross

Many voltage regulator applications require multiple outputs, such as a computer's power supply or a regulator used to meet the voltage requirements inside an automobile. Some of these applications require isolation between the regulator's input and output for protection and separate ground specifications. Using this criteria, a LM2577 simple switcher flyback regulator has been designed with multiple (3) outputs and input-to-output isolation. The three outputs are: 1) 5V @ 150 mA, 2) 7.5V @ 100 mA, and 3) −7.5V @ 70 mA. The table below gives the electrical specifications.

The LM2577 flyback regulator uses a 4N27 optocoupler to provide a galvanic isolation. The base resistor of the optocoupler is chosen so that it is large enough (47 kΩ) to supply a minimum base current—which in turn, demands a lower drive current to the optocoupler's diode—but not so large as to produce a pole in the regulator's frequency response. If the pole's frequency is below the regulator loop's crossover frequency, stability problems will occur. Thus, a zero must be developed, requiring extra circuitry, to compensate for the extra pole in the loop.

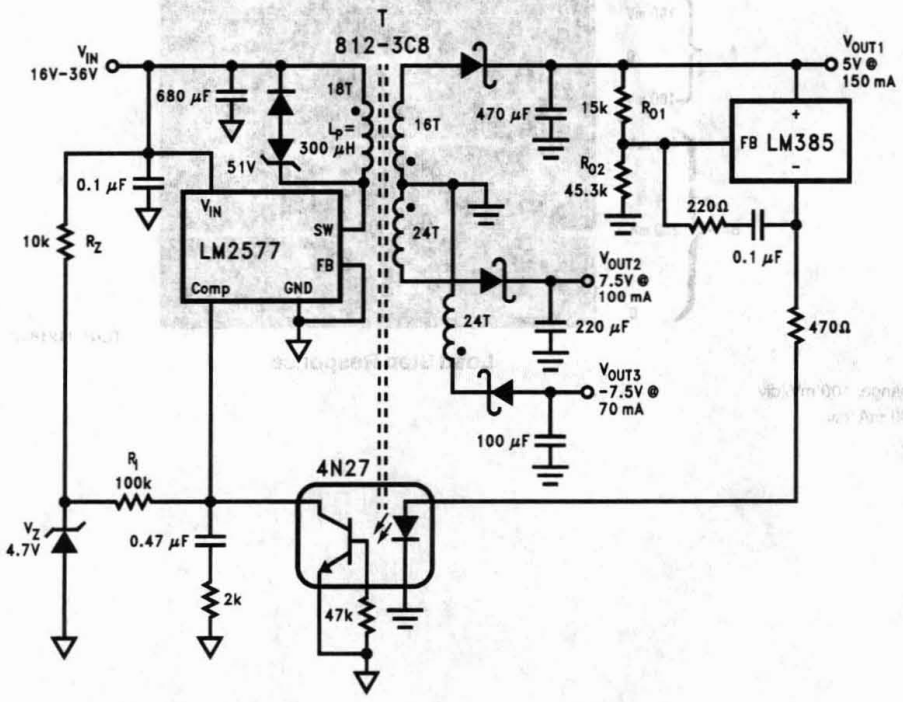
An LM385 Adjustable Voltage Reference, along with resistors R_{O1} and R_{O2}, set the main output voltage to 5V ±4% by the equation: $V_O = 1.24V\ (1 + R_{O2}/R_{O1})$. The LM385 supplies a drive current to the optocoupler (about 10 mA) proportional to the output voltage. Due to the high gain of the LM385, the LM2577's error amplifier is bypassed, and the feedback signal is fed directly to the compensation pin. Employing the error amplifier's gain block in the loop would add with the LM385 gain (the optocoupler's gain is around unity) to produce a very large overall loop gain. Such a large loop gain makes the loop too difficult to stabilize—thus the bypassed error amplifier. With the regulator input voltage of 26V and full load on all outputs, the frequency response has a crossover frequency at 1 kHz and phase margin of 90°.

The flyback regulator's mode of operation is continuous, so a large primary inductance (L_P = 300 μH) is needed for the transformer. Using a Ferroxcube 812E250-3C8 E core, the primary winding requires about 50 turns. With the turns-ratios as they are shown on the schematic and the small core size, the transformer windings must be wound tightly so that they fit the core windows. Interlaying the primary winding between the secondary windings improves the transformers coupling.

The zener diode circuit (V_Z, R_Z, R_I) is added to provide the optocoupler transistor with about 20 μA of bias current, on top of the current sourced from the compensation pin (about 7 μA). The isolation resistor, between the compensation pin and the zener diode, needs to be as large as 100 kΩ, or at start-up, the compensation pin will see too large a voltage, turning the power switch fully on—thus forcing the LM2577 into current limit. Also, to ensure good line regulation, the dynamic impedance of the zener diode must be very good.

Test data for this regulator follows the schematic. Since feedback is taken from Output 1, its load and line regulation are better than that of the other two outputs, which rely on feedback through the transformer coupling. The output ripple voltage of all three outputs is largely dependent on the filter capacitors used, and could be reduced by the use of additional high-quality filter capacitors or an additional L-C filter section.

LM2577 Three Output, Isolated Flyback Regulator



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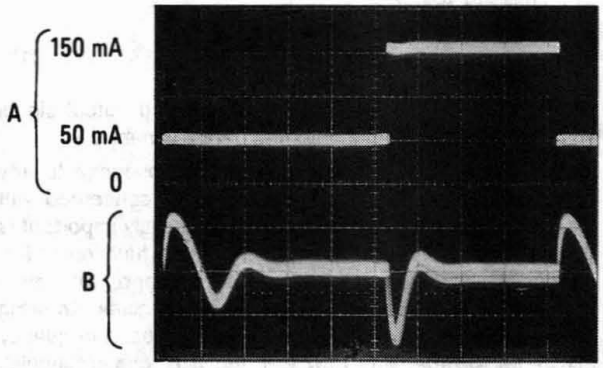
ELECTRICAL TEST DATA V_I = 16V–36V

Output Voltages	Line Regulation (I_O = Full Load)	Load Regulation (V_I = 26V)	Output Ripple Voltage (T_A = 25°C)
V_{O1} = 5V	0.2%	0.04% 30 mA–150 mA	50 mV
V_{O2} = 7.5V	0.3%	3% 20 mA–100 mA	50 mV
V_{O3} = 7.5V	0.3%	2% 12 mA–70 mA	50 mV



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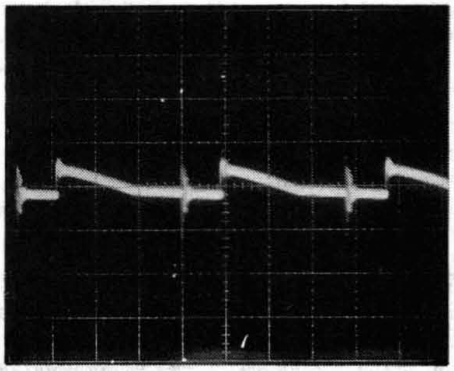
Load Transient Response
A. Load Current, 50 mA/div
B. Output Voltage Change
50 mV/div (AC-Coupled)
Horizontal: 5 ms/div



TL/H/11217–3

Output Ripple Voltage
20 mV/div (AC-Coupled)
Horizontal: 5 ms/div

A Basic Introduction to Filters—Active, Passive, and Switched-Capacitor

National Semiconductor
Application Note 779
Kerry Lacanette

1.0 INTRODUCTION

Filters of some sort are essential to the operation of most electronic circuits. It is therefore in the interest of anyone involved in electronic circuit design to have the ability to develop filter circuits capable of meeting a given set of specifications. Unfortunately, many in the electronics field are uncomfortable with the subject, whether due to a lack of familiarity with it, or a reluctance to grapple with the mathematics involved in a complex filter design.

This Application Note is intended to serve as a very basic introduction to some of the fundamental concepts and terms associated with filters. It will not turn a novice into a filter designer, but it can serve as a starting point for those wishing to learn more about filter design.

1.1 Filters and Signals: What Does a Filter Do?

In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships. Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges. Such a filter has a **gain** which is dependent on signal frequency. As an example, consider a situation where a useful signal at frequency f_1 has been contaminated with an unwanted signal at f_2. If the contaminated signal is passed through a circuit *(Figure 1)* that has very low gain at f_2 compared to f_1, the undesired signal can be removed, and the useful signal will remain. Note that in the case of this simple example, we are not concerned with the gain of the filter at any frequency other than f_1 and f_2. As long as f_2 is sufficiently attenuated relative to f_1, the performance of this filter will be satisfactory. In general, however, a filter's gain may be specified at several different frequencies, or over a band of frequencies.

Since filters are defined by their frequency-domain effects on signals, it makes sense that the most useful analytical and graphical descriptions of filters also fall into the frequency domain. Thus, curves of gain vs frequency and phase vs frequency are commonly used to illustrate filter characteristics,and the most widely-used mathematical tools are based in the frequency domain.

The frequency-domain behavior of a filter is described mathematically in terms of its **transfer function** or **network function**. This is the ratio of the Laplace transforms of its output and input signals. The voltage transfer function H(s) of a filter can therefore be written as:

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} \quad (1)$$

where $V_{IN}(s)$ and $V_{OUT}(s)$ are the input and output signal voltages and s is the complex frequency variable.

The transfer function defines the filter's response to any arbitrary input signal, but we are most often concerned with its effect on continuous sine waves. Especially important is the magnitude of the transfer function as a function of frequency, which indicates the effect of the filter on the amplitudes of sinusoidal signals at various frequencies. Knowing the transfer function magnitude (or gain) at each frequency allows us to determine how well the filter can distinguish between signals at different frequencies. The transfer function magnitude versus frequency is called the **amplitude response** or sometimes, especially in audio applications, the **frequency response**.

Similarly, the **phase response** of the filter gives the amount of **phase shift** introduced in sinusoidal signals as a function of frequency. Since a change in phase of a signal also represents a change in time, the phase characteristics of a filter become especially important when dealing with complex signals where the time relationships between signal components at different frequencies are critical.

By replacing the variable s in (1) with $j\omega$, where j is equal to $\sqrt{-1}$, and ω is the radian frequency ($2\pi f$), we can find the filter's effect on the magnitude and phase of the input signal. The magnitude is found by taking the absolute value of (1):

$$|H(j\omega)| = \left|\frac{V_{OUT}(j\omega)}{V_{IN}(j\omega)}\right| \quad (2)$$

and the phase is:

$$\arg H(j\omega) = \arg \frac{V_{OUT}(j\omega)}{V_{IN}(j\omega)} \quad (3)$$

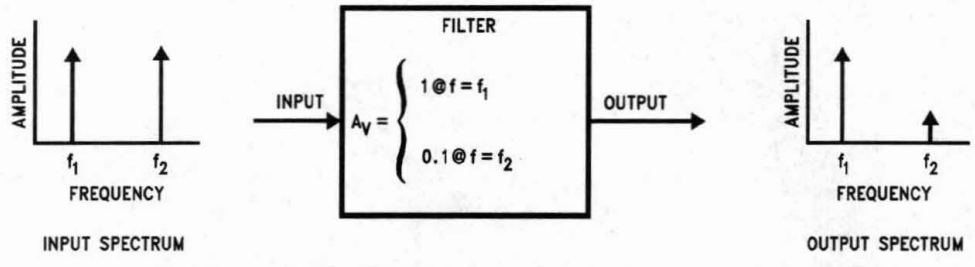


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FIGURE 1. Using a Filter to Reduce the Effect of an Undesired Signal at Frequency f_2, while Retaining Desired Signal at Frequency f_1

As an example, the network of *Figure 2* has the transfer function:

$$H(s) = \frac{s}{s^2 + s + 1} \quad (4)$$

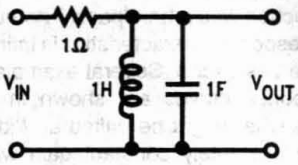

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FIGURE 2. Filter Network of Example

This is a 2nd order system. The **order** of a filter is the highest power of the variable s in its transfer function. The order of a filter is usually equal to the total number of capacitors and inductors in the circuit. (A capacitor built by combining two or more individual capacitors is still one capacitor.) Higher-order filters will obviously be more expensive to build, since they use more components, and they will also be more complicated to design. However, higher-order filters can more effectively discriminate between signals at different frequencies.

Before actually calculating the amplitude response of the network, we can see that at very low frequencies (small values of s), the numerator becomes very small, as do the first two terms of the denominator. Thus, as s approaches zero, the numerator approaches zero, the denominator approaches one, and H(s) approaches zero. Similarly, as the input frequency approaches infinity, H(s) also becomes progressively smaller, because the denominator increases with the square of frequency while the numerator increases linearly with frequency. Therefore, H(s) will have its maximum value at some frequency between zero and infinity, and will decrease at frequencies above and below the peak.

To find the magnitude of the transfer function, replace s with $j\omega$ to yield:

$$A(\omega) = |H(s)| = \left|\frac{j\omega}{-\omega^2 + j\omega + 1}\right| \quad (5)$$

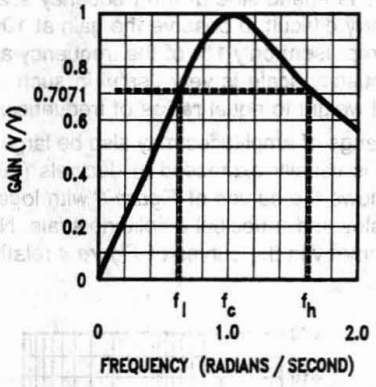
$$= \frac{\omega}{\sqrt{\omega^2 + (1 - \omega^2)^2}}$$

The phase is:

$$\theta(\omega) = \arg H(s) = 90° - \tan^{-1}\frac{\omega^2}{(1 - \omega^2)} \quad (6)$$

The above relations are expressed in terms of the radian frequency ω, in units of radians/second. A sinusoid will complete one full cycle in 2π radians. Plots of magnitude and phase versus radian frequency are shown in *Figure 3*. When we are more interested in knowing the amplitude and phase response of a filter in units of Hz (cycles per second), we convert from radian frequency using $\omega = 2\pi f$, where f is the frequency in Hz. The variables f and ω are used more or less interchangeably, depending upon which is more appropriate or convenient for a given situation.

Figure 3(a) shows that, as we predicted, the magnitude of the transfer function has a maximum value at a specific frequency (ω_0) between 0 and infinity, and falls off on either side of that frequency. A filter with this general shape is known as a **band-pass** filter because it passes signals falling within a relatively narrow band of frequencies and attenuates signals outside of that band. The range of frequencies passed by a filter is known as the filter's **passband**. Since the amplitude response curve of this filter is fairly smooth, there are no obvious boundaries for the passband. Often, the passband limits will be defined by system requirements. A system may require, for example, that the gain variation between 400 Hz and 1.5 kHz be less than 1 dB. This specification would effectively define the passband as 400 Hz to 1.5 kHz. In other cases though, we may be presented with a transfer function with no passband limits specified. In this case, and in any other case with no explicit passband limits, the passband limits are usually assumed to be the frequencies where the gain has dropped by 3 decibels (to $\sqrt{2}/2$ or 0.707 of its maximum voltage gain). These frequencies are therefore called the **−3 dB frequencies** or the **cutoff frequencies**. However, if a passband gain variation (i.e., 1 dB) is specified, the cutoff frequencies will be the frequencies at which the maximum gain variation specification is exceeded.



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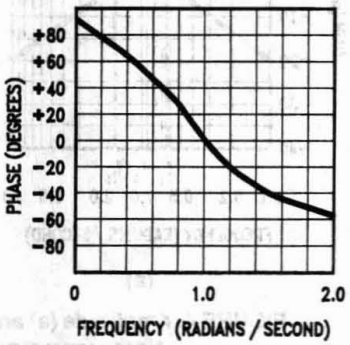
(a)



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(b)

FIGURE 3. Amplitude (a) and phase (b) response curves for example filter. Linear frequency and gain scales.

The precise shape of a band-pass filter's amplitude response curve will depend on the particular network, but any 2nd order band-pass response will have a peak value at the filter's **center frequency**. The center frequency is equal to the geometric mean of the −3 dB frequencies:

$$f_c = \sqrt{f_l f_h} \quad (8)$$

where f_c is the center frequency
f_l is the lower −3 dB frequency
f_h is the higher −3 dB frequency

Another quantity used to describe the performance of a filter is the filter's **"Q"**. This is a measure of the "sharpness" of the amplitude response. The Q of a band-pass filter is the ratio of the center frequency to the difference between the

−3 dB frequencies (also known as the **−3 dB bandwidth**). Therefore:

$$Q = \frac{f_c}{f_h - f_l} \quad (9)$$

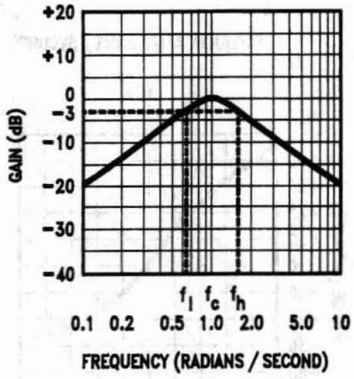
When evaluating the performance of a filter, we are usually interested in its performance over **ratios** of frequencies. Thus we might want to know how much attenuation occurs at twice the center frequency and at half the center frequency. (In the case of the 2nd-order bandpass above, the attenuation would be the same at both points). It is also usually desirable to have amplitude and phase response curves that cover a wide range of frequencies. It is difficult to obtain a useful response curve with a linear frequency scale if the desire is to observe gain and phase over wide frequency ratios. For example, if f_0 = 1 kHz, and we wish to look at response to 10 kHz, the amplitude response peak will be close to the left-hand side of the frequency scale. Thus, it would be very difficult to observe the gain at 100 Hz, since this would represent only 1% of the frequency axis. A logarithmic frequency scale is very useful in such cases, as it gives equal weight to equal **ratios** of frequencies.

Since the range of amplitudes may also be large, the amplitude scale is usually expressed in decibels ($20\log|H(j\omega)|$). *Figure 4* shows the curves of *Figure 3* with logarithmic frequency scales and a decibel amplitude scale. Note the improved symmetry in the curves of *Figure 4* relative to those of *Figure 3*.

1.2 The Basic Filter Types

Bandpass

There are five basic filter types (bandpass, notch, low-pass, high-pass, and all-pass). The filter used in the example in the previous section was a bandpass. The number of possible bandpass response characteristics is infinite, but they all share the same basic form. Several examples of bandpass amplitude response curves are shown in *Figure 5*. The curve in *5(a)* is what might be called an "ideal" bandpass response, with absolutely constant gain within the passband, zero gain outside the passband, and an abrupt boundary between the two. This response characteristic is impossible to realize in practice, but it can be approximated to varying degrees of accuracy by real filters. Curves (b) through (f) are examples of a few bandpass amplitude response curves that approximate the ideal curves with varying degrees of accuracy. Note that while some bandpass responses are very smooth, other have **ripple** (gain variations in their passbands. Other have ripple in their **stopbands** as well. The stopband is the range of frequencies over which unwanted signals are attenuated. Bandpass filters have two stopbands, one above and one below the passband.



(a)

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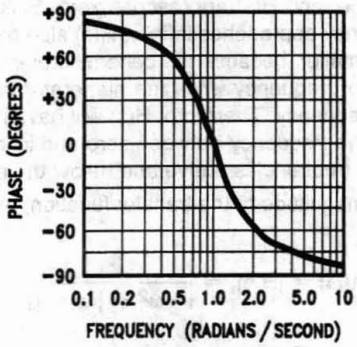

(b)

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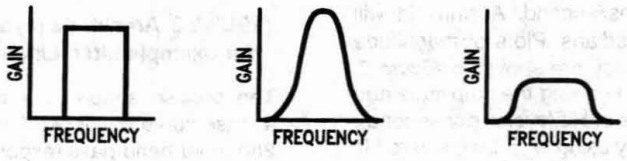
FIGURE 4. Amplitude (a) and phase (b) response curves for example bandpass filter. Note symmetry of curves with log frequency and gain scales.



(a) (b) (c)

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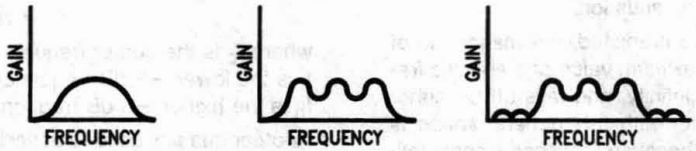

(d) (e) (f)

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FIGURE 5. Examples of Bandpass Filter Amplitude Response

Just as it is difficult to determine by observation exactly where the passband ends, the boundary of the stopband is also seldom obvious. Consequently, the frequency at which a stopband begins is usually defined by the requirements of a given system—for example, a system specification might require that the signal must be attenuated at least 35 dB at 1.5 kHz. This would define the beginning of a stopband at 1.5 kHz.

The rate of change of attenuation between the passband and the stopband also differs from one filter to the next. The slope of the curve in this region depends strongly on the order of the filter, with higher-order filters having steeper cutoff slopes. The attenuation slope is usually expressed in dB/octave (an octave is a factor of 2 in frequency) or dB/decade (a decade is a factor of 10 in frequency).

Bandpass filters are used in electronic systems to separate a signal at one frequency or within a band of frequencies from signals at other frequencies. In 1.1 an example was given of a filter whose purpose was to pass a desired signal at frequency f_1, while attenuating as much as possible an unwanted signal at frequency f_2. This function could be performed by an appropriate bandpass filter with center frequency f_1. Such a filter could also reject unwanted signals at other frequencies outside of the passband, so it could be useful in situations where the signal of interest has been contaminated by signals at a number of different frequencies.

Notch or Band-Reject

A filter with effectively the opposite function of the bandpass is the **band-reject** or **notch** filter. As an example, the components in the network of *Figure 3* can be rearranged to form the notch filter of *Figure 6*, which has the transfer function

$$H_N(s) = \frac{V_{OUT}}{V_{IN}} = \frac{s^2 + 1}{s^2 + s + 1} \qquad (10)$$

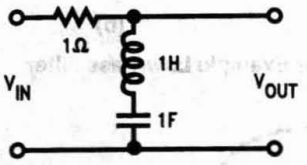

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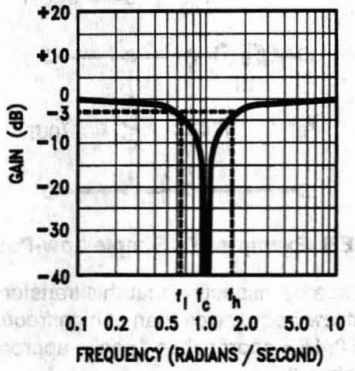
FIGURE 6. Example of a Simple Notch Filter

The amplitude and phase curves for this circuit are shown in *Figure 7*. As can be seen from the curves, the quantities f_c, f_l, and f_h used to describe the behavior of the band-pass filter are also appropriate for the notch filter. A number of notch filter amplitude response curves are shown in *Figure 8*. As in *Figure 5*, curve (a) shows an "ideal" notch response, while the other curves show various approximations to the ideal characteristic.



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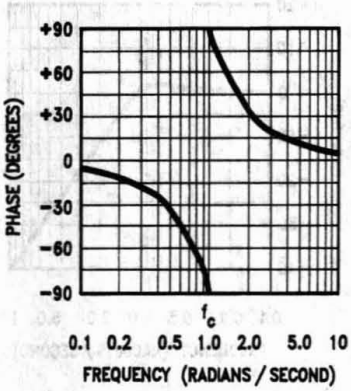
(a)



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(b)

FIGURE 7. Amplitude (a) and Phase (b) Response Curves for Example Notch Filter

Notch filters are used to remove an unwanted frequency from a signal, while affecting all other frequencies as little as possible. An example of the use of a notch filter is with an audio program that has been contaminated by 60 Hz power-line hum. A notch filter with a center frequency of 60 Hz can remove the hum while having little effect on the audio signals.

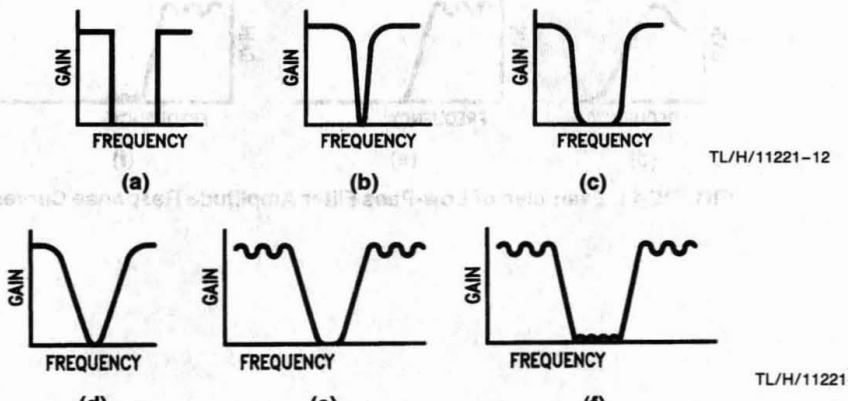

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FIGURE 8. Examples of Notch Filter Amplitude Responses

Low-Pass

A third filter type is the **low-pass**. A low-pass filter passes low frequency signals, and rejects signals at frequencies above the filter's cutoff frequency. If the components of our example circuit are rearranged as in *Figure 9*, the resultant transfer function is:

$$H_{LP}(s) = \frac{V_{OUT}}{V_{IN}} = \frac{1}{s^2 + s + 1} \quad (11)$$

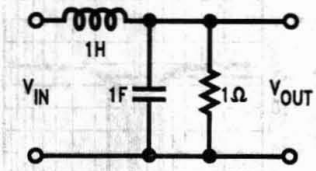

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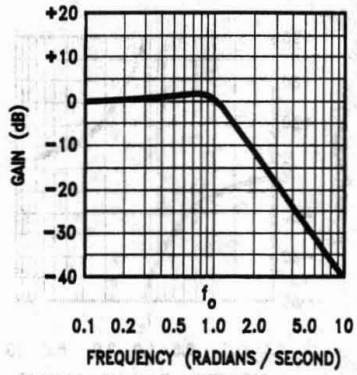
FIGURE 9. Example of a Simple Low-Pass Filter

It is easy to see by inspection that this transfer function has more gain at low frequencies than at high frequencies. As ω approaches 0, H_{LP} approaches 1; as ω approaches infinity, H_{LP} approaches 0.

Amplitude and phase response curves are shown in *Figure 10*, with an assortment of possible amplitude reponse curves in *Figure 11*. Note that the various approximations to the unrealizable ideal low-pass amplitude characteristics take different forms, some being monotonic (always having a negative slope), and others having ripple in the passband and/or stopband.

Low-pass filters are used whenever high frequency components must be removed from a signal. An example might be in a light-sensing instrument using a photodiode. If light levels are low, the output of the photodiode could be very small, allowing it to be partially obscured by the noise of the sensor and its amplifier, whose spectrum can extend to very high frequencies. If a low-pass filter is placed at the output of the amplifier, and if its cutoff frequency is high enough to allow the desired signal frequencies to pass, the overall noise level can be reduced.



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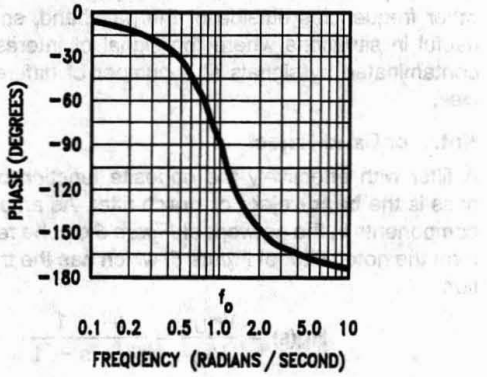
(a)



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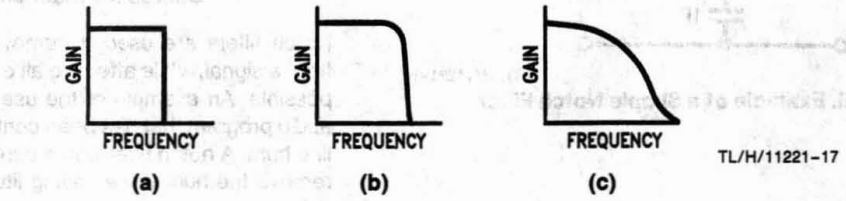
(b)

FIGURE 10. Amplitude (a) and Phase (b) Response Curves for Example Low-Pass Filter



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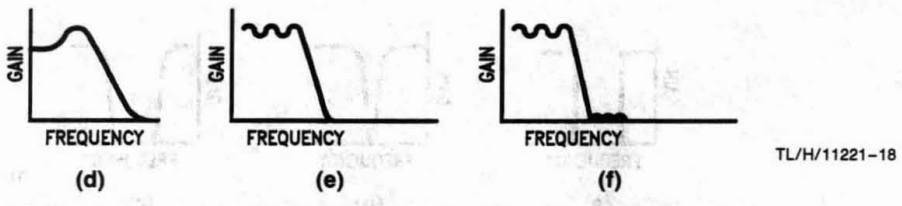

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FIGURE 11. Examples of Low-Pass Filter Amplitude Response Curves

High-Pass

The opposite of the low-pass is the **high-pass** filter, which rejects signals below its cutoff frequency. A high-pass filter can be made by rearranging the components of our example network as in *Figure 12*. The transfer function for this filter is:

$$H_{HP}(s) = \frac{V_{OUT}}{V_{IN}} = \frac{s^2}{s^2 + s + 1} \quad (12)$$

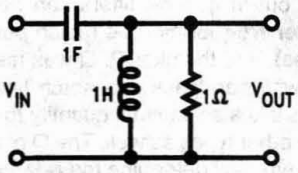

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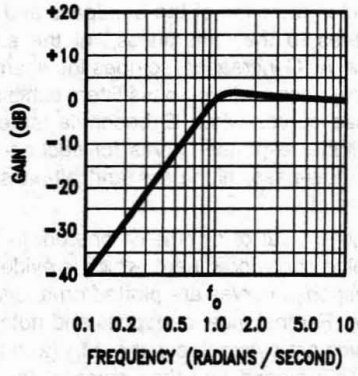
FIGURE 12. Example of Simple High-Pass Filter

and the amplitude and phase curves are found in *Figure 13*. Note that the amplitude response of the high-pass is a "mirror image" of the low-pass response. Further examples of high-pass filter responses are shown in *Figure 14*, with the "ideal" response in (a) and various approximations to the ideal shown in (b) through (f).

High-pass filters are used in applications requiring the rejection of low-frequency signals. One such application is in high-fidelity loudspeaker systems. Music contains significant energy in the frequency range from around 100 Hz to 2 kHz, but high-frequency drivers (tweeters) can be damaged if low-frequency audio signals of sufficient energy appear at their input terminals. A high-pass filter between the broadband audio signal and the tweeter input terminals will prevent low-frequency program material from reaching the tweeter. In conjunction with a low-pass filter for the low-frequency driver (and possibly other filters for other drivers), the high-pass filter is part of what is known as a "crossover network".



(a)

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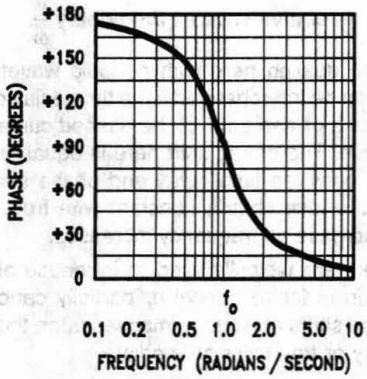

(b)

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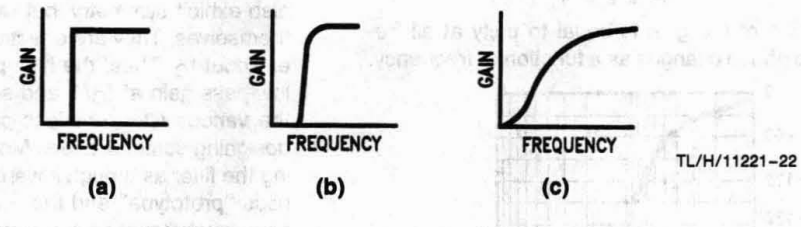
FIGURE 13. Amplitude (a) and Phase (b) Response Curves for Example High-Pass Filter



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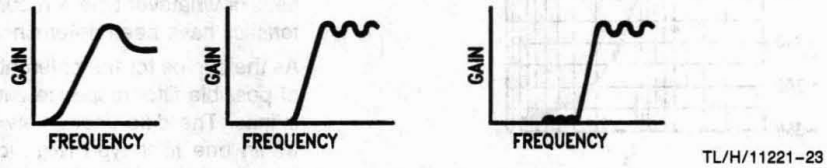

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FIGURE 14. Examples of High-Pass Filter Amplitude Response Curves

All-Pass or Phase-Shift

The fifth and final filter response type has no effect on the amplitude of the signal at different frequencies. Instead, its function is to change the phase of the signal without affecting its amplitude. This type of filter is called an **all-pass** or **phase-shift** filter. The effect of a shift in phase is illustrated in *Figure 15*. Two sinusoidal waveforms, one drawn in dashed lines, the other a solid line, are shown. The curves are identical except that the peaks and zero crossings of the dashed curve occur at later times than those of the solid curve. Thus, we can say that the dashed curve has undergone a **time delay** relative to the solid curve.

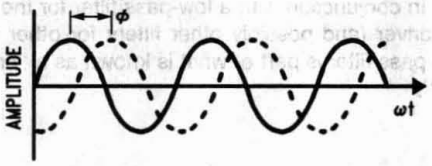

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FIGURE 15. Two sinusoidal waveforms with phase difference θ. Note that this is equivalent to a time delay $\frac{\theta}{\omega}$.

Since we are dealing here with periodic waveforms, time and phase can be interchanged—the time delay can also be interpreted as a **phase shift** of the dashed curve relative to the solid curve. The phase shift here is equal to θ radians. The relation between time delay and phase shift is $T_D = \theta/2\pi\omega$, so if phase shift is constant with frequency, time delay will decrease as frequency increases.

All-pass filters are typically used to introduce phase shifts into signals in order to cancel or partially cancel any unwanted phase shifts previously imposed upon the signals by other circuitry or transmission media.

Figure 16 shows a curve of phase vs frequency for an all-pass filter with the transfer function

$$H_{AP}(s) = \frac{s^2 - s + 1}{s^2 + s + 1}$$

The absolute value of the gain is equal to unity at all frequencies, but the phase changes as a function of frequency.

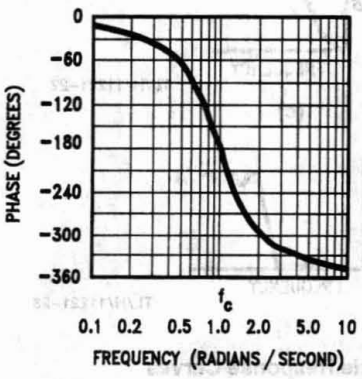

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FIGURE 16. Phase Response Curve for Second-Order All-Pass Filter of Example

Let's take another look at the transfer function equations and response curves presented so far. First note that all of the transfer functions share the same denominator. Also note that all of the numerators are made up of terms found in the denominator: the high-pass numerator is the first term (s^2) in the denominator, the bandpass numerator is the second term (s), the low-pass numerator is the third term (1), and the notch numerator is the sum of the denominator's first and third terms ($s^2 + 1$). The numerator for the all-pass transfer function is a little different in that it includes all of the denominator terms, but one of the terms has a negative sign.

Second-order filters are characterized by four basic properties: the filter **type** (high-pass, bandpass, etc.), the **passband gain** (all the filters discussed so far have unity gain in the passband, but in general filters can be built with any gain), the **center frequency** (one radian per second in the above examples), and the filter **Q**. Q was mentioned earlier in connection with bandpass and notch filters, but in second-order filters it is also a useful quantity for describing the behavior of the other types as well. The Q of a second-order filter of a given type will determine the **relative shape** of the amplitude response. Q can be found from the denominator of the transfer function if the denominator is written in the form:

$$D(s) = s^2 + \frac{\omega_O}{Q}s + \omega_O{}^2.$$

As was noted in the case of the bandpass and notch functions, Q relates to the "sharpness" of the amplitude response curve. As Q increases, so does the sharpness of the response. Low-pass and high-pass filters exhibit "peaks" in their response curves when Q becomes large. *Figure 17* shows amplitude response curves for second-order bandpass, notch, low-pass, high-pass and all-pass filters with various values of Q.

There is a great deal of symmetry inherent in the transfer functions we've considered here, which is evident when the amplitude response curves are plotted on a logarithmic frequency scale. For instance, bandpass and notch amplitude resonse curves are symmetrical about f_O (with log frequency scales). This means that their gains at $2f_O$ will be the same as their gains at $f_O/2$, their gains at $10f_O$ will be the same as their gains at $f_O/10$, and so on.

The low-pass and high-pass amplitude response curves also exhibit symmetry, but with each other rather than with themselves. They are effectively mirror images of each other about f_O. Thus, the high-pass gain at $2f_O$ will equal the low-pass gain at $f_O/2$ and so on. The similarities between the various filter functions prove to be quite helpful when designing complex filters. Most filter designs begin by defining the filter as though it were a low-pass, developing a low-pass "prototype" and then converting it to bandpass, high-pass or whatever type is required after the low-pass characteristics have been determined.

As the curves for the different filter types imply, the number of possible filter response curves that can be generated is infinite. The differences between different filter responses within one filter type (e.g., low-pass) can include, among others, characteristic frequencies, filter order, roll-off slope, and flatness of the passband and stopband regions. The transfer function ultimately chosen for a given application will often be the result of a tradeoff between the above characteristics.

1.3 Elementary Filter Mathematics

In 1.1 and 1.2, a few simple passive filters were described and their transfer functions were shown. Since the filters were only 2nd-order networks, the expressions associated with them weren't very difficult to derive or analyze. When the filter in question becomes more complicated than a simple 2nd-order network, however, it helps to have a general

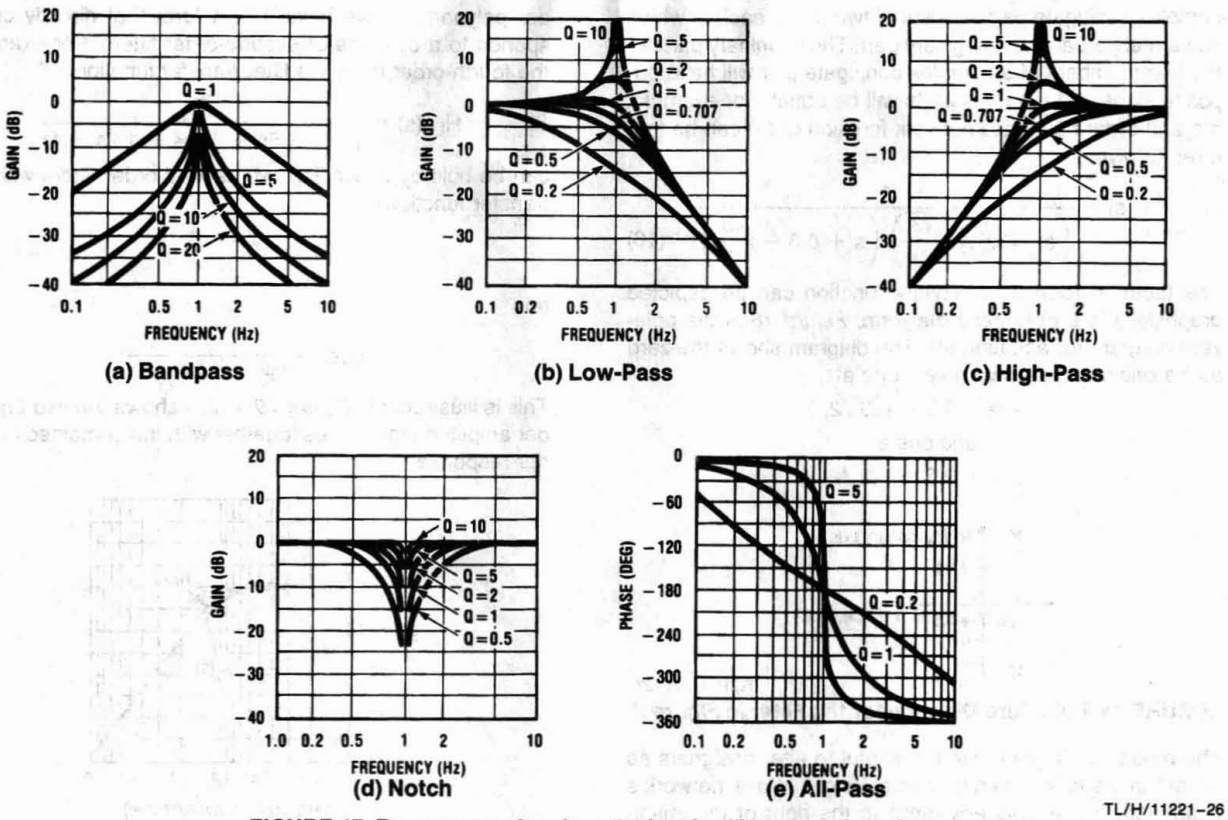

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FIGURE 17. Responses of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

mathematical method of describing its characteristics. This allows us to use standard terms in describing filter characteristics, and also simplifies the application of computers to filter design problems.

The transfer functions we will be dealing with consist of a numerator divided by a denominator, each of which is a function of s, so they have the form:

$$H(s) = \frac{N(s)}{D(s)} \qquad (13)$$

Thus, for the 2nd-order bandpass example described in (4),

$$H_{BP}(s) = \frac{s}{s^2 + s + 1},$$

we would have $N(s) = s$, and $D(s) = s^2 + s + 1$.

The numerator and denominator can always be written as polynomials in s, as in the example above. To be completely general, a transfer function for an nth-order network, (one with "n" capacitors and inductors), can be written as below.

$$H(s) = H_0 \frac{s^n + b_{n-1}s^{n-1} + b_{n-2}s^{n-2} + \ldots + b_1 s + b_0}{s^n + a_{n-1}s^{n-1} + a_{n-2}s^{n-2} + \ldots + a_1 s + a_0} \qquad (14)$$

This appears complicated, but it means simply that a filter's transfer function can be mathematically described by a numerator divided by a denominator, with the numerator and denominator made up of a number of terms, each consisting of a constant multiplied by the variable "s" to some power. The a_i and b_i terms are the constants, and their subscripts correspond to the order of the "s" term each is associated with. Therefore, a_1 is multiplied by s, a_2 is multiplied by s^2, and so on. Any filter transfer function (including the 2nd-order bandpass of the example) will have the general form of (14), with the values of the coefficients a_i and b_i depending on the particular filter.

The values of the coefficients completely determine the characteristics of the filter. As an example of the effect of changing just one coefficient, refer again to *Figure 17*, which shows the amplitude and phase response for 2nd-order bandpass filters with different values of Q. The Q of a 2nd-order bandpass is changed simply by changing the coefficient a_1, so the curves reflect the influence of that coefficient on the filter response.

Note that if the coefficients are known, we don't even have to write the whole transfer function, because the expression can be reconstructed from the coefficients. In fact, in the interest of brevity, many filters are described in filter design tables solely in terms of their coefficients. Using this aproach, the 2nd-order bandpass of *Figure 1* could be sufficiently specified by "$a_0 = a_1 = a_2 = b_1 = 1$", with all other coefficients equal to zero.

Another way of writing a filter's transfer function is to factor the polynomials in the numerator and denominator so that they take the form:

$$H(s) = H_0 \frac{(s - z_0)(s - z_1)(s - z_2)\ldots(s - z_n)}{(s - p_0)(s - p_1)(s - p_2)\ldots(s - p_n)} \qquad (15)$$

The roots of the numerator, $z_0, z_1, z_2, \ldots z_n$ are known as **zeros**, and the roots of the denominator, $p_0, p_1, \ldots p_n$ are called **poles**. z_i and p_i are in general complex numbers, i.e., $R + jI$, where R is the real part, $j = \sqrt{-1}$, and I is the imaginary part. All of the poles and zeros will be either real roots (with no imaginary part) or complex conjugate pairs. A

complex conjugate pair consists of two roots, each of which has a real part and an imaginary part. The imaginary parts of the two members of a complex conjugate pair will have opposite signs and the reals parts will be equal. For example, the 2nd-order bandpass network function of (4) can be factored to give:

$$H(s) = \frac{s}{\left(s + 0.5 + j\frac{\sqrt{3}}{2}\right)\left(s + 0.5 - j\frac{\sqrt{3}}{2}\right)} \quad (16)$$

The factored form of a network function can be depicted graphically in a **pole-zero diagram**. *Figure 18* is the pole-zero diagram for equation (4). The diagram shows the zero at the origin and the two poles, one at

$$s = -0.5 - j\sqrt{3}/2,$$

and one at

$$s = -0.5 + j\sqrt{3}/2.$$

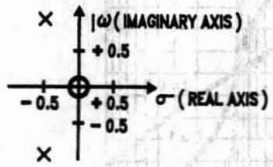

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FIGURE 18. Pole-Zero Diagram for the Filter in *Figure 2*

The pole-zero diagram can be helpful to filter designers as an aid in visually obtaining some insight into a network's characteristics. A pole anywhere to the right of the imaginary axis indicates instability. If the pole is located on the positive real axis, the network output will be an increasing exponential function. A positive pole not located on the real axis will give an exponentially increasing sinusoidal output. We obviously want to avoid filter designs with poles in the right half-plane!

Stable networks will have their poles located on or to the left of the imaginary axis. Poles on the imaginary axis indicate an undamped sinusoidal output (in other words, a sine-wave oscillator), while poles on the left real axis indicate damped exponential response, and complex poles in the negative half-plane indicate damped sinusoidal response. The last two cases are the ones in which we will have the most interest, as they occur repeatedly in practical filter designs.

Another way to arrange the terms in the network function expression is to recognize that each complex conjugate pair is simply the factored form of a second-order polynomial. By multiplying the complex conjugate pairs out, we can get rid of the complex numbers and put the transfer function into a form that essentially consists of a number of 2nd-order transfer functions multiplied together, possibly with some first-order terms as well. We can thus think of the complex filter as being made up of several 2nd-order and first-order filters connected in series. The transfer function thus takes the form:

$$H(s) = H_0 \frac{(s^2+b_{11}s+b_{10})(s^2+b_{21}s+b_{20})\ldots}{(s^2+a_{11}s+a_{10})(s^2+a_{21}s+a_{20})\ldots} \quad (17)$$

This form is particularly useful when you need to design a complex active or switched-capacitor filter. The general approach for designing these kinds of filters is to cascade second-order filters to produce a higher-order overall response. By writing the transfer function as the product of second-order polynomials, we have it in a form that directly corresponds to a cascade of second-order filters. For example, the fourth-order low-pass filter transfer function

$$H_{LP}(s) = \frac{1}{(s^2 + 1.5s + 1)(s^2 + 1.2s + 1)} \quad (18)$$

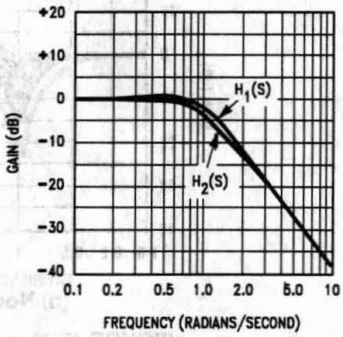
can be built by cascading two second-order filters with the transfer functions

(19)

and

$$H_2(s) = \frac{1}{(s^2 + 1.2s + 1)} \quad (20)$$

This is illustrated in *Figure 19*, which shows the two 2nd-order amplitude responses together with the combined 4th-order response.



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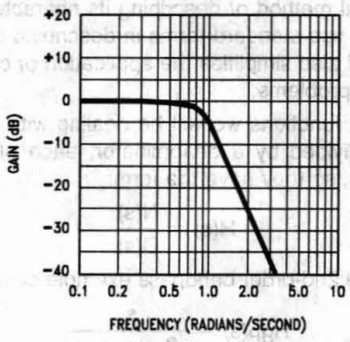
(a)



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(b)

FIGURE 19. Two Second-Order Low-Pass Filters (a) can be Cascaded to Build a Fourth-Order Filter (b).

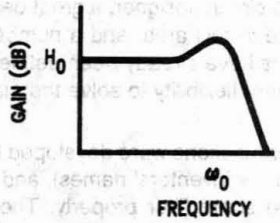
Instead of the coefficients a_0, a_1, etc., second-order filters can also be described in terms of parameters that relate to observable quantities. These are the filter gain H_0, the characteristics radian frequency ω_O, and the filter Q. For the general second-order low-pass filter transfer function we have:

$$H(s) = \frac{H_0 a_0}{(s^2 + a_1 s + a_0)} = \frac{H_0 \omega_0^2}{(s^2 + \frac{\omega_0}{Q}s + \omega_0^2)} \quad (21)$$

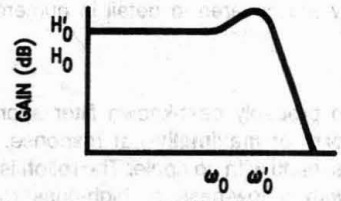
which yields: $\omega^2_0 = a_0$, and $Q = \omega_0/a_1 = \sqrt{a_0}/a_1$.

The effects of H_0 and ω_0 on the amplitude response are straightforward: H_0 is the gain scale factor and ω_0 is the frequency scale factor. Changing one of these parameters will alter the amplitude or frequency scale on an amplitude

response curve, but the shape, as shown in *Figure 20*, will remain the same. The basic shape of the curve is determined by the filter's Q, which is determined by the denominator of the transfer function.



(a) TL/H/11221–30



(b) TL/H/11221–31

FIGURE 20. Effect of changing H_0 and ω_0. Note that, when log frequency and gain scales are used, a change in gain or center frequency has no effect on the shape of the response curve. Curve shape is determined by Q.

1.4 Filter Approximations

In Section 1.2 we saw several examples of amplitude response curves for various filter types. These always included an "ideal" curve with a rectangular shape, indicating that the boundary between the passband and the stopband was abrupt and that the rolloff slope was infinitely steep. This type of response would be ideal because it would allow us to completely separate signals at different frequencies from one another. Unfortunately, such an amplitude response curve is not physically realizable. We will have to settle for the best **approximation** that will still meet our requirements for a given application. Deciding on the best approximation involves making a compromise between various properties of the filter's transfer function. The important properties are listed below.

Filter Order. The order of a filter is important for several reasons. It is directly related to the number of components in the filter, and therefore to its cost, its physical size, and the complexity of the design task. Therefore, higher-order filters are more expensive, take up more space, and are more difficult to design. The primary advantage of a higher-order filter is that it will have a steeper rolloff slope than a similar lower-order filter.

Ultimate Rolloff Rate. Usually expressed as the amount of attenuation in dB for a given ratio of frequencies. The most common units are "dB/octave" and "dB/decade". While the ultimate rolloff rate will be 20 dB/decade for every filter pole in the case of a low-pass or high-pass filter and 20 dB/decade for every pair of poles for a bandpass filter, some filters will have steeper attenuation slopes near the cutoff frequency than others of the same order.

Attenuation Rate Near the Cutoff Frequency. If a filter is intended to reject a signal very close in frequency to a signal that must be passed, a sharp cutoff characteristic is desirable between those two frequencies. Note that this steep slope may not continue to frequency extremes.

Transient Response. Curves of amplitude response show how a filter reacts to steady-state sinusoidal input signals. Since a real filter will have far more complex signals applied to its input terminals, it is often of interest to know how it will behave under transient conditions. An input signal consisting of a step function provides a good indication of this. *Figure 21* shows the responses of two low-pass filters to a step input. Curve (b) has a smooth reaction to the input step, while curve (a) exhibits some **ringing**. As a rule of thumb, filters will sharper cutoff characteristics or higher Q will have more pronounced ringing.

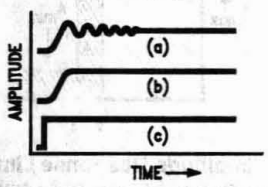


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FIGURE 21. Step response of two different filters. Curve (a) shows significant "ringing", while curve (b) shows none. The input signal is shown in curve (c).

Monotonicity. A filter has a monotonic amplitude response if its gain slope never changes sign—in other words, if the gain always increases with increasing frequency or always decreases with increasing frequency. Obviously, this can happen only in the case of a low-pass or high-pass filter. A bandpass or notch filter can be monotonic on either side of the center frequency, however. *Figures 11(b)* and *(c)* and *14(b)* and *(c)* are examples of monotonic transfer functions.

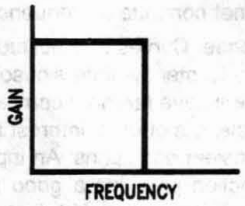
Passband Ripple. If a filter is not monotonic within its passband, the transfer function within the passband will exhibit one or more "bumps". These bumps are known as "ripple". Some systems don't necessarily require monotonicity, but do require that the passband ripple be limited to some maximum value (usually 1 dB or less). Examples of passband ripple can be found in *Figures 5(e)* and *(f)*, *8(f)*, *11(e)* and *(f)*, and *14(e)* and *(f)*. Although bandpass and notch filters do not have monotonic transfer functions, they can be free of ripple within their passbands.

Stopband Ripple. Some filter responses also have ripple in the stopbands. Examples are shown in *Figure 5(f)*, *8(g)*, *11(f)*, and *14(f)*. We are normally unconcerned about the amount of ripple in the stopband, as long as the signal to be rejected is sufficiently attenuated.

Given that the "ideal" filter amplitude response curves are not physically realizable, we must choose an acceptable approximation to the ideal response. The word "acceptable" may have different meanings in different situations.

The acceptability of a filter design will depend on many interrelated factors, including the amplitude response characteristics, transient response, the physical size of the circuit and the cost of implementing the design. The "ideal" low-pass amplitude response is shown again in *Figure 22(a)*. If we are willing to accept some deviations from this ideal in order to build a practical filter, we might end up with a curve like the one in *Figure 22(b)*, which allows ripple in the pass-

band, a finite attenuation rate, and stopband gain greater than zero. Four parameters are of concern in the figure:



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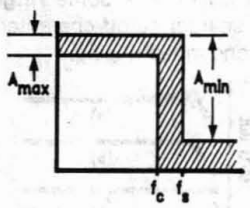
(a) "ideal" Low-Pass Filter Response



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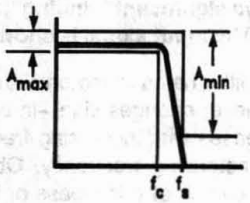
(b) Amplitude Response Limits for a Practical Low-Pass Filter



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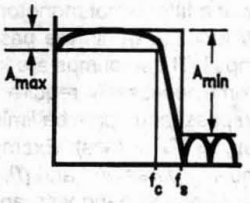
(c) Example of an Amplitude Response Curve Falling with the Limits Set by f_c, f_s, A_{min}, and A_{max}



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(d) Another Amplitude Response Falling within the Desired Limits

FIGURE 22

A_{max} is the maximum allowable change in gain within the passband. This quantity is also often called the maximum passband ripple, but the word "ripple" implies non-monotonic behavior, while A_{max} can obviously apply to monotonic response curves as well.

A_{min} is the minimum allowable attenuation (referred to the maximum passband gain) within the stopband.

f_c is the cutoff frequency or passband limit.

f_s is the frequency at which the stopband begins.

If we can define our filter requirements in terms of these parameters, we will be able to design an acceptable filter using standard "cookbook" design methods. It should be apparent that an unlimited number of different amplitude response curves could fit within the boundaries determined by these parameters, as illustrated in *Figure 22(c) and (d)*. Filters with acceptable amplitude response curves may differ in terms of such characteristics as transient response, passband and stopband flatness, and complexity. How does one choose the best filter from the infinity of possible transfer functions?

Fortunately for the circuit designer, a great deal of work has already been done in this area, and a number of standard filter characteristics have already been defined. These usually provide sufficient flexibility to solve the majority of filtering problems.

The "classic" filter functions were developed by mathematicians (most bear their inventors' names), and each was designed to optimize some filter property. The most widely-used of these are discussed below. No attempt is made here to show the mathematical derivations of these functions, as they are covered in detail in numerous texts on filter theory.

Butterworth

The first, and probably best-known filter approximation is the **Butterworth** or **maximally-flat** response. It exhibits a nearly flat passband with no ripple. The rolloff is smooth and monotonic, with a low-pass or high-pass rolloff rate of 20 dB/decade (6 dB/octave) for every pole. Thus, a 5th-order Butterworth low-pass filter would have an attenuation rate of 100 dB for every factor of ten increase in frequency beyond the cutoff frequency.

The general equation for a Butterworth filter's amplitude response is

$$H(\omega) = \frac{1}{1 + \left(\frac{\omega}{\omega_0}\right)^{2n}} \qquad (22)$$

where n is the order of the filter, and can be any positive whole number (1, 2, 3, . . .), and ω is the -3 dB frequency of the filter.

Figure 23 shows the amplitude response curves for Butterworth low-pass filters of various orders. The frequency scale is normalized to $f/f_{-3\ dB}$ so that all of the curves show 3 dB attenuation for $f/f_c = 1.0$.

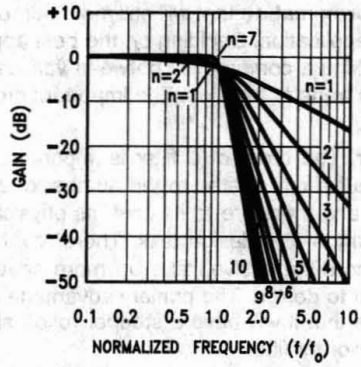

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FIGURE 23. Amplitude Response Curves for Butterworth Filters of Various Orders

The coefficients for the denominators of Butterworth filters of various orders are shown in Table 1(a). Table 1(b) shows the denominators factored in terms of second-order polynomials. Again, all of the coefficients correspond to a corner frequency of 1 radian/s (finding the coefficients for a different cutoff frequency will be covered later). As an example,

TABLE 1(a). Butterworth Polynomials

Denominator coefficients for polynomials of the form $s^n + a_{n-1}s^{n-1} + a_{n-2}s^{n-2} + \ldots + a_1 s + a_0$.

n	a_0	a_1	a_2	a_3	a_4	a_5	a_6	a_7	a_8	a_9
1	1									
2	1	1.414								
3	1	2.000	2.000							
4	1	2.613	3.414	2.613						
5	1	3.236	5.236	5.236	3.236					
6	1	3.864	7.464	9.142	7.464	3.864				
7	1	4.494	10.098	14.592	14.592	10.098	4.494			
8	1	5.126	13.137	21.846	25.688	21.846	13.137	5.126		
9	1	5.759	16.582	31.163	41.986	41.986	31.163	16.582	5.759	
10	1	6.392	20.432	42.802	64.882	74.233	64.882	42.802	20.432	6.392

TABLE 1(b). Butterworth Quadratic Factors

n	
1	$(s + 1)$
2	$(s^2 + 1.4142s + 1)$
3	$(s + 1)(s^2 + s + 1)$
4	$(s^2 + 0.7654s + 1)(s^2 + 1.8478s + 1)$
5	$(s + 1)(s^2 + 0.6180s + 1)(s^2 + 1.6180s + 1)$
6	$(s^2 + 0.5176s + 1)(s^2 + 1.4142s + 1)(s^2 + 1.9319)$
7	$(s + 1)(s^2 + 0.4450s + 1)(s^2 + 1.2470s + 1)(s^2 + 1.8019s + 1)$
8	$(s^2 + 0.3902s + 1)(s^2 + 1.1111s + 1)(s^2 + 1.6629s + 1)(s^2 + 1.9616s + 1)$
9	$(s + 1)(s^2 + 0.3473s + 1)(s^2 + 1.0000s + 1)(s^2 + 1.5321s + 1)(s^2 + 1.8794s + 1)$
10	$(s^2 + 0.3129s + 1)(s^2 + 0.9080s + 1)(s^2 + 1.4142s + 1)(s^2 + 1.7820s + 1)(s^2 + 1.9754s + 1)$

the tables show that a fifth-order Butterworth low-pass filter's transfer function can be written:

$$H(s) = \frac{1}{s^5 + 3.236s^4 + 5.236s^3 + 5.236s^2 + 3.236s + 1} \quad (22)$$

$$= \frac{1}{(s + 1)(s^2 + 0.6180s + 1)(s^2 + 1.6180s + 1)}$$

This is the product of one first-order and two second-order transfer functions. Note that neither of the second-order transfer functions alone is a Butterworth transfer function, but that they both have the same center frequency.

Figure 24 shows the step response of Butterworth low-pass filters of various orders. Note that the amplitude and duration of the ringing increases as n increases.

Chebyshev

Another approximation to the ideal filter is the **Chebyshev** or **equal ripple** response. As the latter name implies, this sort of filter will have ripple in the passband amplitude response. The amount of passband ripple is one of the parameters used in specifying a Chebyshev filter. The Chebyschev characteristic has a steeper rolloff near the cutoff frequency when compared to the Butterworth, but at the expense of monotonicity in the passband and poorer transient response. A few different Chebyshev filter responses are shown in *Figure 25*. The filter responses in the figure have 0.1 dB and 0.5 dB ripple in the passband, which is small compared to the amplitude scale in *Figure 25(a)* and *(b)*, so it is shown expanded in *Figure 25(c)*.

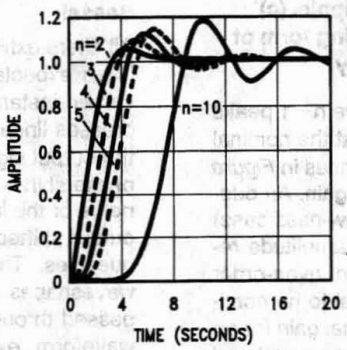

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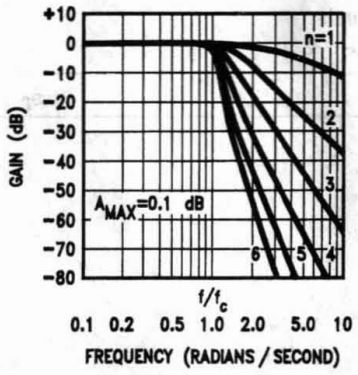
FIGURE 24. Step responses for Butterworth low-pass filters. In each case $\omega_0 = 1$ and the step amplitude is 1.0.



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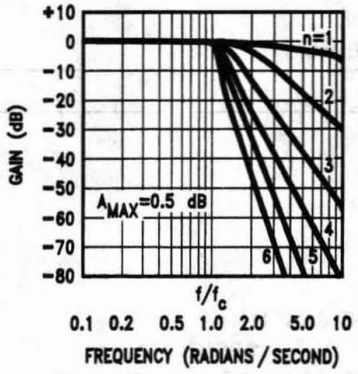
(a)



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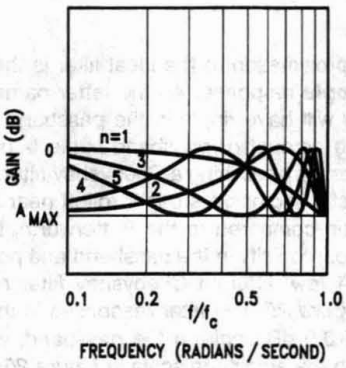
(b)



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(c)

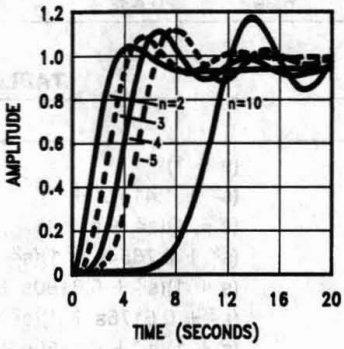
FIGURE 25. Examples of Chebyshev amplitude responses. (a) 0.1 dB ripple (b) 0.5 dB ripple. (c) Expanded view of passband region showing form of response below cutoff frequency.

Note that a Chebyshev filter of order n will have n−1 peaks or dips in its passband response. Note also that the nominal gain of the filter (unity in the case of the responses in *Figure 25*) is equal to he filter's maximum passband gain. An odd-order Chebyshev will have a dc gain (in the low-pass case) equal to the nominal gain, with "dips" in the amplitude response curve equal to the ripple value. An even-order Chebyshev low-pass will have its dc gain equal to he nominal filter gain **minus** the ripple value; the nominal gain for an even-order Chebyshev occurs at the peaks of the passband ripple. Therefore, if you're designing a fourth-order Chebyshev low-pass filter with 0.5 dB ripple and you want it to have unity gain at dc, you'll have to design for a nominal gain of 0.5 dB.

The cutoff frequency of a Chebyshev filter is not assumed to be the −3 dB frequency as in the case of a Butterworth filter. Instead, the Chebyshev's cutoff frequency is normally the frequency at which the ripple (or A_{max}) specification is exceeded.

The addition of passband ripple as a parameter makes the specification process for a Chebyshev filter a bit more complicated than for a Butterworth filter, but also increases flexibility.

Figure 26 shows the step response of 0.1 dB and 0.5 dB ripple Chebyshev filters of various orders. As with the Butterworth filters, the higher order filters ring more.



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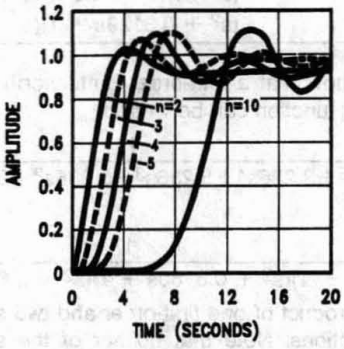
(a) 0.1 dB Ripple



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(b) 0.5 dB Ripple

FIGURE 26. Step responses for Chebyshev low-pass filters. In each case, $\omega_0 = 1$, and the step amplitude is 1.0.

Bessel

All filters exhibit phase shift that varies with frequency. This is an expected and normal characteristic of filters, but in certain instances it can present problems. If the phase increases linearly with frequency, its effect is simply to delay the output signal by a constant time period. However, if the phase shift is not directly proportional to frequency, components of the input signal at one frequency will appear at the output shifted in phase (or time) with respect to other frequencies. The overall effect is to distort non-sinusoidal waveshapes, as illustrated in *Figure 27* for a square wave passed through a Butterworth low-pass filter. The resulting waveform exhibits ringing and overshoot because the square wave's component frequencies are shifted in time with respect to each other so that the resulting waveform is very different from the input square wave.

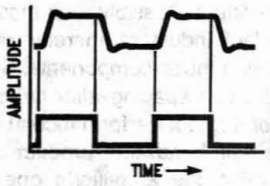

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FIGURE 27. Response of a 4th-order Butterworth low-pass (upper curve) to a square wave input (lower curve). The "ringing" in the response shows that the nonlinear phase shift distorts the filtered wave shape.

When the avoidance of this phenomenon is important, a **Bessel** or **Thompson** filter may be useful. The Bessel characteristic exhibits approximately linear phase shift with frequency, so its action within the passband simulates a delay line with a low-pass characteristic. The higher the filter order, the more linear the Bessel's phase response. *Figure 28* shows the square-wave response of a Bessel low-pass filter. Note the lack of ringing and overshoot. Except for the "rounding off" of the square wave due to the attenuation of high-frequency harmonics, the waveshape is preserved.

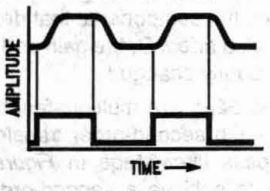

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FIGURE 28. Response of a 4th-order Bessel low-pass (upper curve) to a square wave input (lower curve). Note the lack of ringing in the response. Except for the "rounding of the corners" due to the reduction of high frequency components, the response is a relatively undistorted version of the input square wave.

The amplitude response of the Bessel filter is monotonic and smooth, but the Bessel filter's cutoff characteristic is quite gradual compared to either the Butterworth or Chebyshev as can be seen from the Bessel low-pass amplitude response curves in *Figure 29*. Bessel step responses are plotted in *Figure 30* for orders ranging from 2 to 10.

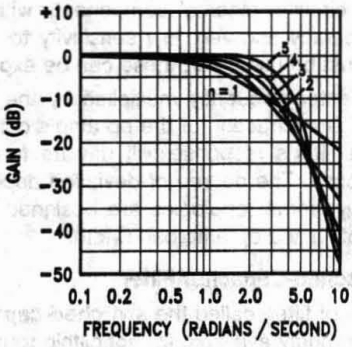

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FIGURE 29. Amplitude response curves for Bessel filters of various orders. The nominal delay of each filter is 1 second.

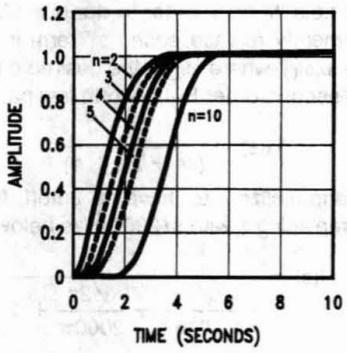

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FIGURE 30. Step responses for Bessel low-pass filters. In each case, $\omega_0 = 1$ and the input step amplitude is 1.0.

Elliptic

The cutoff slope of an **elliptic** filter is steeper than that of a Butterworth, Chebyshev, or Bessel, but the amplitude response has ripple in both the passband and the stopband, and the phase response is very non-linear. However, if the primary concern is to pass frequencies falling within a certain frequency band and reject frequencies outside that band, regardless of phase shifts or ringing, the elliptic response will perform that function with the lowest-order filter.

The elliptic function gives a sharp cutoff by adding notches in the stopband. These cause the transfer function to drop to zero at one or more frequencies in the stopband. Ripple is also introduced in the passband (see *Figure 31*). An elliptic filter function can be specified by three parameters (again excluding gain and cutoff frequency): passband ripple, stopband attenuation, and filter order n. Because of the greater complexity of the elliptic filter, determination of coefficients is normally done with the aid of a computer.

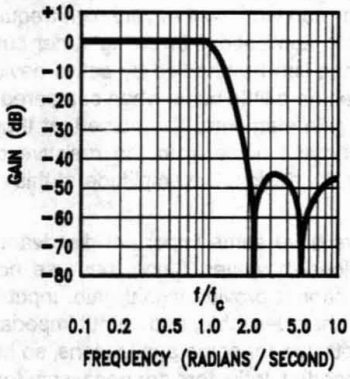

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FIGURE 31. Example of a elliptic low-pass amplitude response. This particular filter is 4th-order with A_{max} = 0.5 dB and $f_s/f_c = 2$. The passband ripple is similar in form to the Chebyshev ripple shown in *Figure 25(c)*.

1.5 Frequency Normalization and Denormalization

Filter coefficients that appear in tables such as Table 1 are **normalized** for cutoff frequencies of 1 radian per second, or $\omega_O = 1$. Therefore, if these coefficients are used to generate a filter transfer function, the cutoff (or center) frequency of the transfer function will be at $\omega = 1$. This is a convenient way to standardize filter coefficients and transfer functions. If this were not done, we would need to produce a different set of coefficients for every possible center frequency. Instead, we use coefficients that are normalized for $\omega_O = 1$ because it is simple to rescale the frequency be-

havior of a 1 r.p.s. filter. In order to **denormalize** a transfer function we merely replace each "s" term in the transfer function with s/ω_O, where ω_O is the desired cutoff frequency. Thus the second-order Butterworth low-pass function

$$H(s) = \frac{1}{(s^2 + 2s + 1)} \quad (23)$$

could be denormalized to have a cutoff frequency of 1000 Hz by replacing s with $s/2000\pi$ as below:

$$H(s) = \frac{1}{\frac{s^2}{4 \times 10^6 \pi^2} + \frac{\sqrt{2}s}{2000\pi} + 1}$$

$$= \frac{4 \times 10^6 \pi^2}{s^2 + 2828.4\pi s + 4 \times 10^6 \pi^2}$$

$$= \frac{3.948 \times 10^7}{s^2 + 8885.8s + 3.948 \times 10^7}$$

If it is necessary to normalize a transfer function, the opposite procedure can be performed by replacing each "s" in the transfer function with $\omega_O s$.

APPROACHES TO IMPLEMENTING FILTERS: ACTIVE, PASSIVE, AND SWITCHED-CAPACITOR

2.1 Passive Filters

The filters used for the earlier examples were all made up of passive components: resistors, capacitors, and inductors, so they are referred to as **passive filters**. A passive filter is simply a filter that uses no amplifying elements (transistors, operational amplifiers, etc.). In this respect, it is the simplest (in terms of the number of necessary components) implementation of a given transfer function. Passive filters have other advantages as well. Because they have no active components, passive filters require no power supplies. Since they are not restricted by the bandwidth limitations of op amps, they can work well at very high frequencies. They can be used in applications involving larger current or voltage levels than can be handled by active devices. Passive filters also generate little nosie when compared with circuits using active gain elements. The noise that they produce is simply the thermal noise from the resistive components, and, with careful design, the amplitude of this noise can be very low.

Passive filters have some important disadvantages in certain applications, however. Since they use no active elements, they cannot provide signal gain. Input impedances can be lower than desirable, and output impedances can be higher the optimum for some applications, so buffer amplifiers may be needed. Inductors are necessary for the synthesis of most useful passive filter characteristics, and these can be prohibitively expensive if high accuracy (1% or 2%, for example), small physical size, or large value are required. Standard values of inductors are not very closely spaced, and it is diffcult to find an off-the-shelf unit within 10% of any arbitrary value, so adjustable inductors are often used. Tuning these to the required values is time-consuming and expensive when producing large quantities of filters. Futhermore, complex passive filters (higher than 2nd-order) can be difficult and time-consuming to design.

2.2 Active Filters

Active filters use amplifying elements, especially op amps, with resistors and capacitors in their feedback loops, to synthesize the desired filter characteristics. Active filters can have high input impedance, low output impedance, and virtually any arbitrary gain. They are also usually easier to design than passive filters. Possibly their most important attribute is that they lack inductors, thereby reducing the problems associated with those components. Still, the problems of accuracy and value spacing also affect capacitors, although to a lesser degree. Performance at high frequencies is limited by the gain-bandwidth product of the amplifying elements, but within the amplifier's operating frequency range, the op amp-based active filter can achieve very good accuracy, provided that low-tolerance resistors and capacitors are used. Active filters will generate noise due to the amplifying circuitry, but this can be minimized by the use of low-noise amplifiers and careful circuit design.

Figure 32 shows a few common active filter configurations (There are several other useful designs; these are intended to serve as examples). The second-order Sallen-Key low-pass filter in (a) can be used as a building block for higher-order filters. By cascading two or more of these circuits, filters with orders of four or greater can be built. The two resistors and two capacitors connected to the op amp's non-inverting input and to V_{IN} determine the filter's cutoff frequency and affect the Q; the two resistors connected to the inverting input determine the gain of the filter and also affect the Q. Since the components that determine gain and cutoff frequency also affect Q, the gain and cutoff frequency can't be independently changed.

Figures 32(b) and *32(c)* are multiple-feedback filters using one op amp for each second-order transfer function. Note that each high-pass filter stage in *Figure 32(b)* requires three capacitors to achieve a second-order response. As with the Sallen-Key filter, each component value affects more than one filter characteristic, so filter parameters can't be independently adjusted.

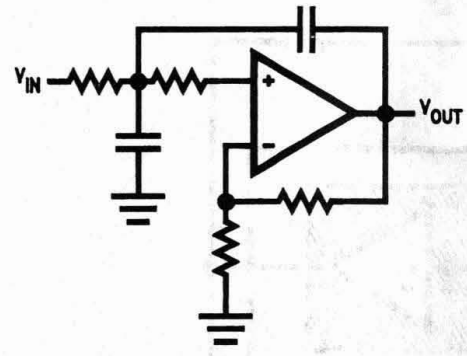
The second-order state-variable filter circuit in *Figure 32(d)* requires more op amps, but provides high-pass, low-pass, and bandpass outputs from a single circuit. By combining the signals from the three outputs, any second-order transfer function can be realized.

When the center frequency is very low compared to the op amp's gain-bandwidth product, the characteristics of active RC filters are primarily dependent on external component tolerances and temperature drifts. For predictable results in critical filter circuits, external components with very good absolute accuracy and very low sensitivity to temperature variations must be used, and these can be expensive.

When the center frequency multiplied by the filter's Q is more than a small fraction of the op amp's gain-bandwidth product, the filter's response will deviate from the ideal transfer function. The degree of deviation depends on the filter topology; some topologies are designed to minimize the effects of limited op amp bandwidth.

2.3 The Switched-Capacitor Filter

Another type of filter, called the **switched-capacitor filter**, has become widely available in monolithic form during the last few years. The switched-capacitor approach overcomes some of the problems inherent in standard active filters, while adding some interesting new capabilities. Switched-capacitor filters need no external capacitors or inductors, and their cutoff frequencies are set to a typical accuracy of ±0.2% by an external clock frequency. This allows consistent, repeatable filter designs using inexpensive crystal-controlled oscillators, or filters whose cutoff frequencies are variable over a wide range simply by changing the clock frequency. In addition, switched-capacitor filters can have low sensitivity to temperature changes.



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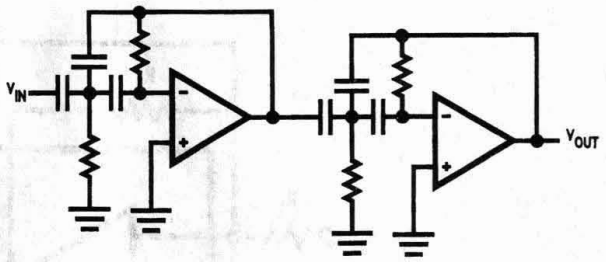
(a) Sallen-Key 2nd-Order Active Low-Pass Filter



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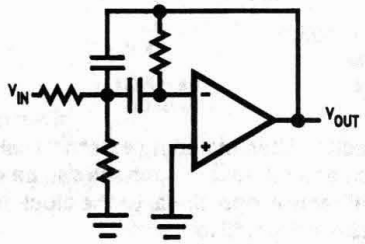
(b) Multiple-Feedback 4th-Order Active High-Pass Filter. Note that there are more capacitors than poles.



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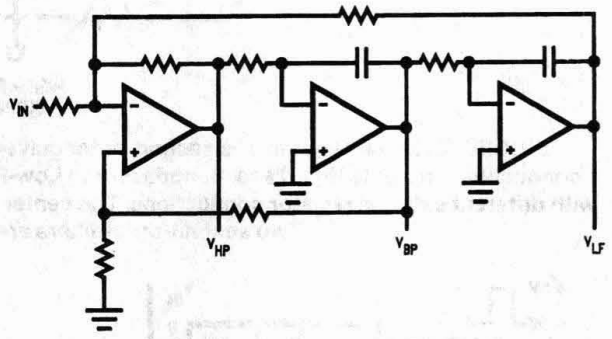
(c) Multiple-Feedback 2nd-Order Bandpass Filter



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(d) Universal State-Variable 2nd-Order Active Filter

FIGURE 32. Examples of Active Filter Circuits Based on Op Amps, Resistors, and Capacitors

Switched-capacitor filters are clocked, sampled-data systems; the input signal is sampled at a high rate and is processed on a discrete-time, rather than continuous, basis. This is a fundamental difference between switched-capacitor filters and conventional active and passive filters, which are also referred to as "continuous time" filters.

The operation of switched-capacitor filters is based on the ability of on-chip capacitors and MOS switches to simulate resistors. The values of these on-chip capacitors can be closely matched to other capacitors on the IC, resulting in integrated filters whose cutoff frequencies are proportional to, and determined only by, the external clock frequency. Now, these integrated filters are nearly always based on state-variable active filter topologies, so they are also active filters, but normal terminology reserves the name "active filter" for filters built using non-switched, or continuous, active filter techniques. The primary weakness of switched-capacitor filters is that they have more noise at their outputs—both random noise and clock feedthrough—than standard active filter circuits.

National Semiconductor builds several different types of switched-capacitor filters. Three of these, the LMF100, the MF5, and the MF10, can be used to synthesize any of the filter types described in Section 1.2, simply by appropriate choice of a few external resistors. The values and placement of these resistors determine the basic shape of the amplitude and phase response, with the center or cutoff frequency set by the external clock. *Figure 33* shows the filter block of the LMF100 with four external resistors connected to provide low-pass, high-pass, and bandpass outputs. Note that this circuit is similar in form to the universal state-variable filter in *Figure 32(d)*, except that the switched-capacitor filter utilizes **non-inverting** integrators, while the conventional active filter uses **inverting** integrators. Changing the switched-capacitor filter's clock frequency changes the value of the integrator resistors, thereby proportionately changing the filter's center frequency. The LMF100 and MF10 each contain two universal filter blocks, while the MF5 has a single second-order filter.

While the LMF100, MF5, and MF10 are **universal filters**, capable of realizing all of the filter types, the LMF40, LMF60, MF4, and MF6 are configured only as fourth- or sixth-order Butterworth low-pass filters, with no external components necessary other than a clock (to set f_O) and a power supply. *Figures 34* and *35* show typical LMF40 and LMF60 circuits along with their amplitude response curves.

Some switched-capacitor filter products are very specialized. The LMF380 *(Figure 36)* contains three fourth-order Chebyshev bandpass filters with bandwidths and center frequency spacings equal to one-third of an octave. This filter is designed for use with audio and acoustical instrumentation and needs no external components other than a clock. An internal clock oscillator can, with the aid of a crystal and two capacitors, generate the master clock for a whole array of LMF380s in an audio real-time analyzer or other multi-filter instrument.

Other devices, such as the MF8 fourth-order bandpass filter *(Figure 37)* and the LMF90 fourth-order notch filter *(Figure 38)* have specialized functions but may be programmed for a variety of response curves using external resistors in the case of the MF8 or logic inputs in the case of the LMF90.

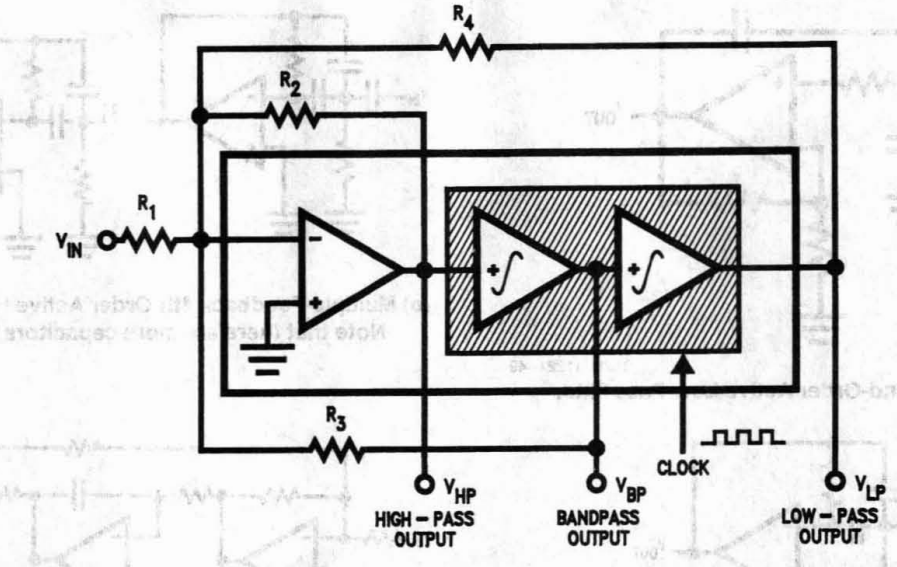


FIGURE 33. Block diagram of a second-order universal switched-capacitor filter, including external resistors connected to provide High-Pass, Bandpass, and Low-Pass outputs. Notch and All-Pass responses can be obtained with different external resistor connections. The center frequency of this filter is proportional to the clock frequency. Two second-order filters are included on the LMF100 or MF10.

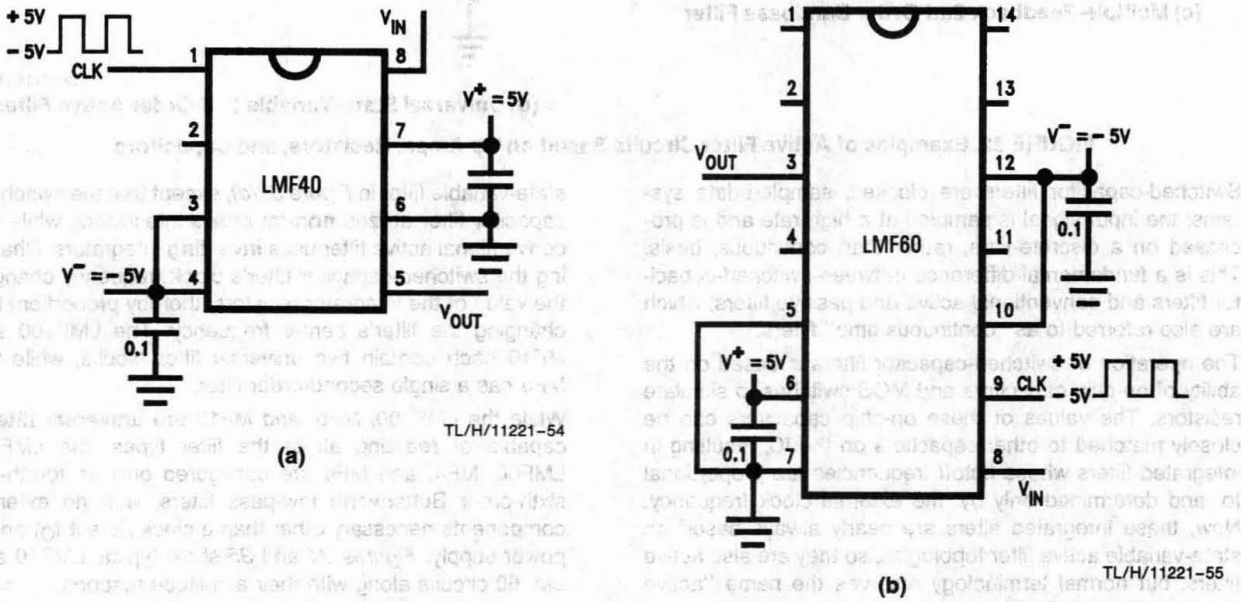


FIGURE 34. Typical LMF40 and LMF60 application circuits. The circuits shown operate on ±5V power supplies and accept CMOS clock levels. For operation on single supplies or with TTL clock levels, see Sections 2.3 and 2.4.

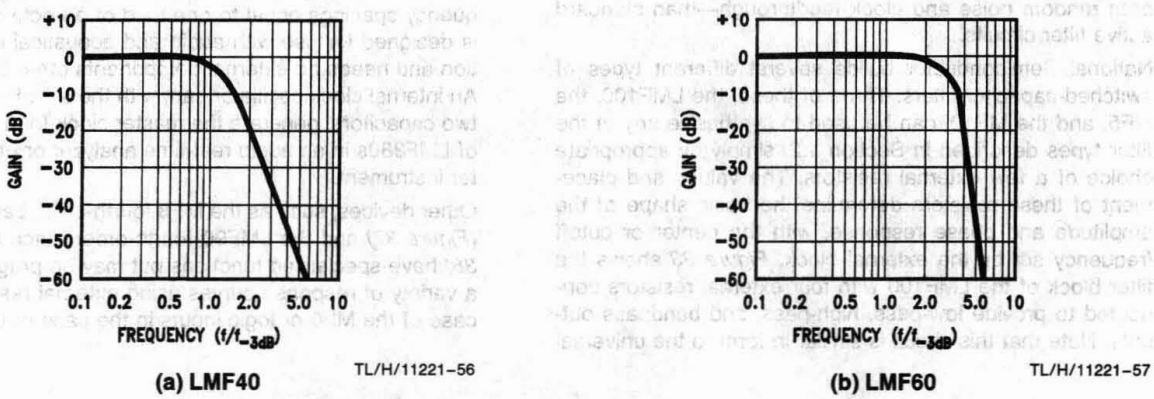
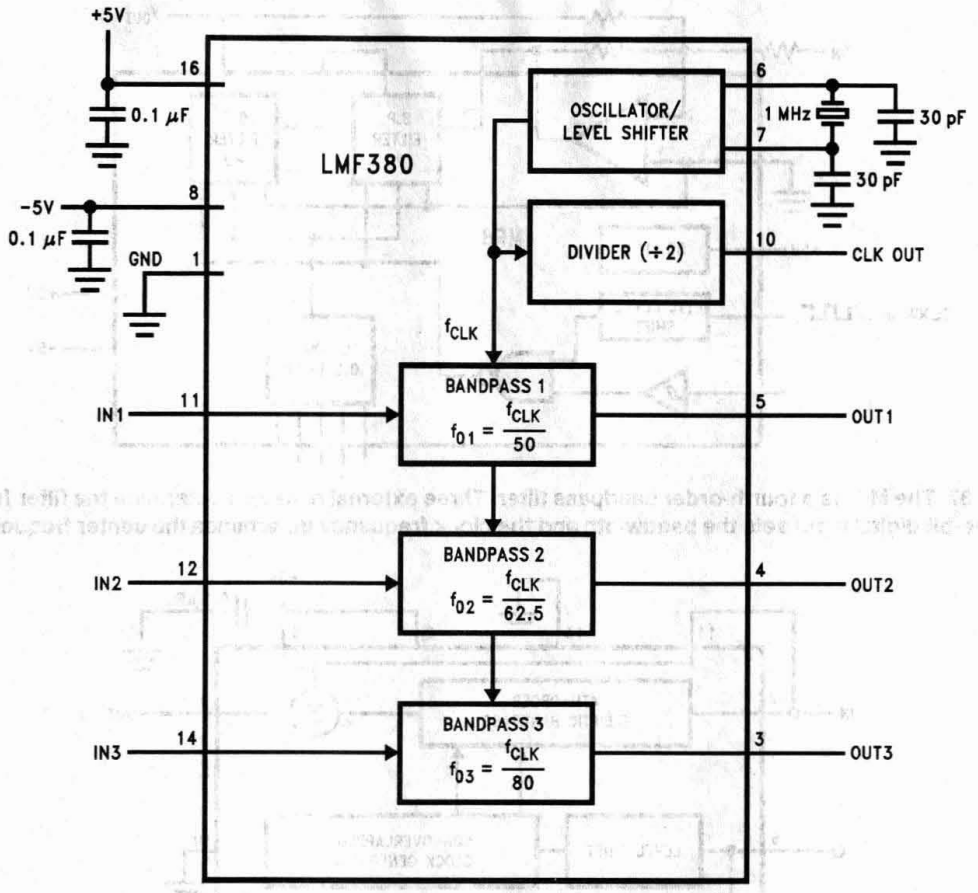


FIGURE 35. Typical LMF40 and LMF60 amplitude response curves. The cutoff frequency has been normalized to 1 in each case.



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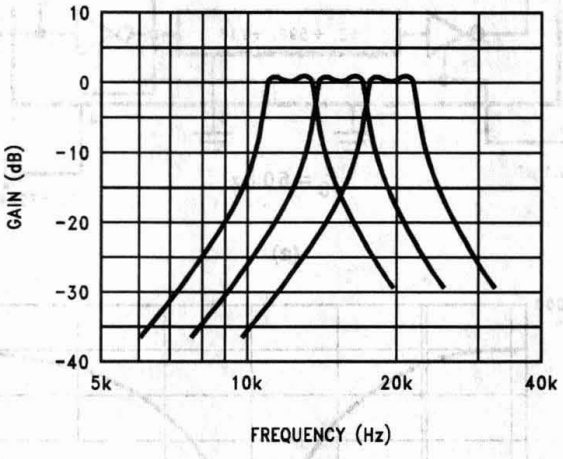
(a)



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(b)

FIGURE 36. LMF380 one-third octave filter array. (a) Typical application circuit for the top audio octave. The clock is generated with the aid of the external crystal and two 30 pF capacitors. (b) Response curves for the three filters.

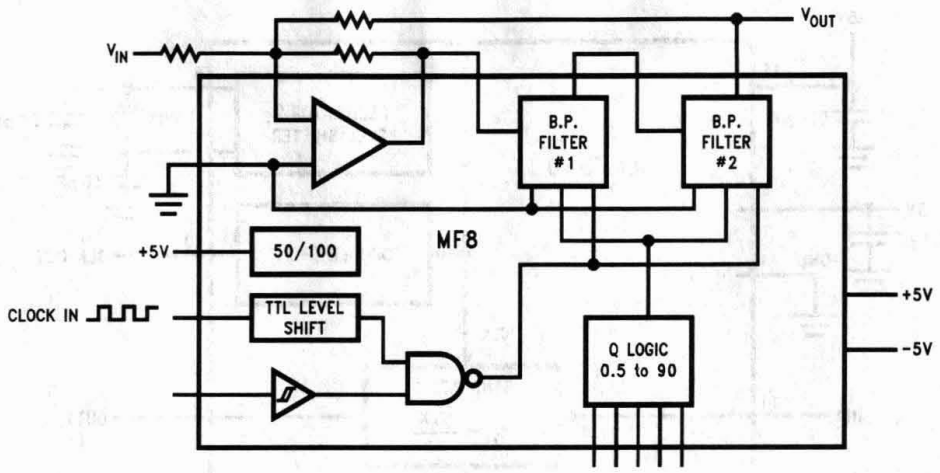

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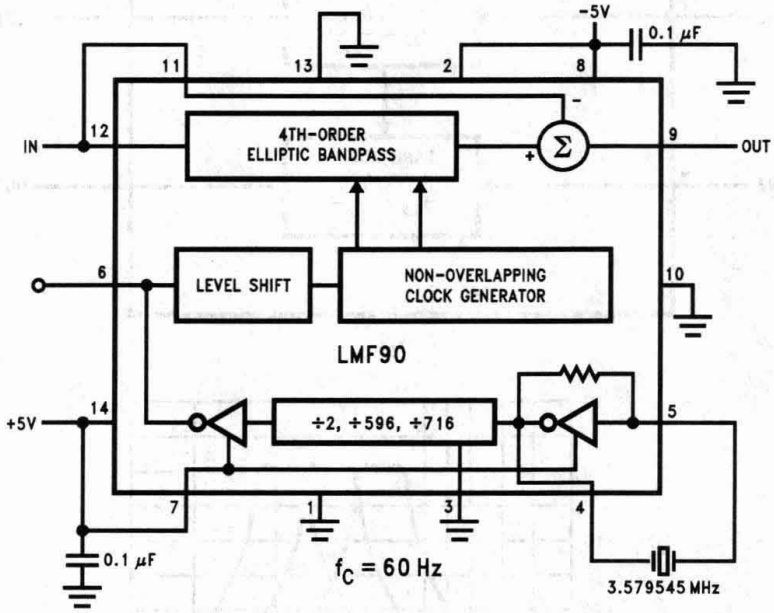
FIGURE 37. The MF8 is a fourth-order bandpass filter. Three external resistors determine the filter function. A five-bit digital input sets the bandwidth and the clock frequency determines the center frequency.



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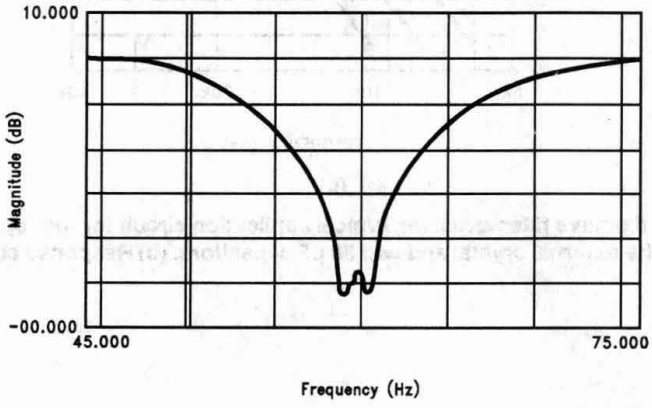
(a)



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(b)

FIGURE 38. LMF90 fourth-order elliptic notch filter. The clock can be generated externally, or internally with the aid of a crystal. Using the circuit as shown in (a), a 60 Hz notch can be built. Connecting pin 3 to V+ yields a 50 Hz notch. By tying pin to ground or V+, the center frequency can be doubled or tripled. The response of the circuit in (a) is shown in (b).

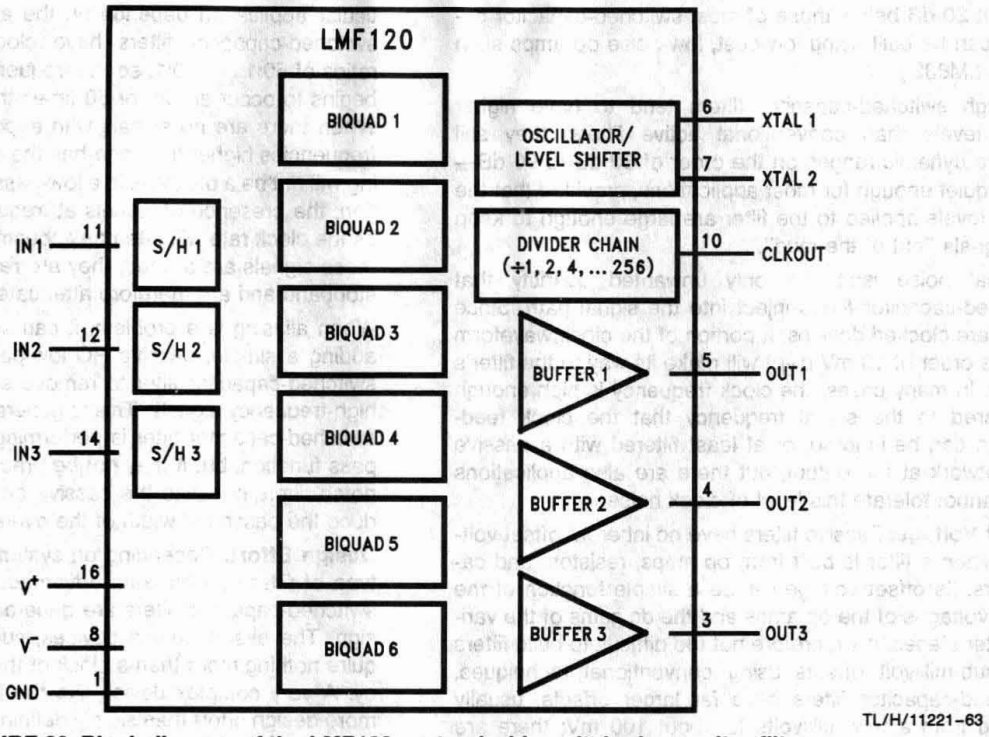

FIGURE 39. Block diagram of the LMF120 customizable switched-capacitor filter array. The internal circuit blocks can be internally configured to provide up to three filters with a total of 12 poles. Any unused circuitry can be disconnected to reduce power consumption.

Finally, when a standard filter product for a specific application can't be found, it often makes sense to use a cell-based approach and build an application-specific filter. An example is the LMF120, a 12th-order customizable switched-capacitor filter array that can be configured to perform virtually any filtering function with no external components. A block diagram of this device is shown in *Figure 39*. The three input sample-and-hold circuits, six second-order filter blocks, and three output buffers can be interconnected to build from one to three filters, with a total order of twelve.

2.4 Which Approach is Best—Active, Passive, or Switched-Capacitor?

Each filter technology offers a unique set of advantages and disadvantages that makes it a nearly ideal solution to some filtering problems and completely unacceptable in other applications. Here's a quick look at the most important differences between active, passive, and switched-capacitor filters.

Accuracy: Switched-capacitor filters have the advantage of better accuracy in most cases. Typical center-frequency accuracies are normally on the order of about 0.2% for most switched-capacitor ICs, and worst-case numbers range from 0.4% to 1.5% (assuming, of course, that an accurate clock is provided). In order to achieve this kind of precision using passive or conventional active filter techniques requires the use of either very accurate resistors, capacitors, and sometimes inductors, or trimming of component values to reduce errors. It is possible for active or passive filter designs to achieve better accuracy than switched-capacitor circuits, but additional cost is the penalty. A resistor-programmed switched-capacitor filter circuit can be trimmed to achieve better accuracy when necessary, but again, there is a cost penalty.

Cost: No single technology is a clear winner here. If a single-pole filter is all that is needed, a passive RC network may be an ideal solution. For more complex designs, switched-capacitor filters can be very inexpensive to buy, and take up very little expensive circuit board space. When good accuracy is necessary, the passive components, especially the capacitors, used in the discrete approaches can be quite expensive; this is even more apparent in very compact designs that require surface-mount components. On the other hand, when speed and accuracy are not important concerns, some conventional active filters can be built quite cheaply.

Noise: Passive filters generate very little noise (just the thermal noise of the resistors), and conventional active filters generally have lower noise than switched-capacitor ICs. Switched-capacitor filters use active op amp-based integrators as their basic internal building blocks. The integrating capacitors used in these circuits must be very small in size, so their values must also be very small. The input resistors on these integrators must therefore be large in value in order to achieve useful time constants. Large resistors produce high levels of thermal noise voltage; typical output noise levels from switched-capacitor filters are on the order of 100 μV to 300 μVrms over a 20 kHz bandwidth. It is interesting to note that the integrator input resistors in switched-capacitor filters are made up of switches and capacitors, but they produce thermal noise the same as "real" resistors.

(Some published comparisons of switched-capacitor vs. op amp filter noise levels have used very noisy op amps in the op amp-based designs to show that the switched-capacitor filter noise levels are nearly as good as those of the op amp-based filters. However, filters with noise levels

at least 20 dB below those of most switched-capacitor designs can be built using low-cost, low-noise op amps such as the LM833.)

Although switched-capacitor filters tend to have higher noise levels than conventional active filters, they still achieve dynamic ranges on the order of 80 dB to 90 dB—easily quiet enough for most applications, provided that the signal levels applied to the filter are large enough to keep the signals "out of the mud".

Thermal noise isn't the only unwanted quantity that switched-capacitor filters inject into the signal path. Since these are clocked devices, a portion of the clock waveform (on the order of 10 mV p–p) will make its way to the filter's output. In many cases, the clock frequency is high enough compared to the signal frequency that the clock feedthrough can be ignored, or at least filtered with a passive RC network at the output, but there are also applications that cannot tolerate this level of clock noise.

Offset Voltage: Passive filters have no inherent offset voltage. When a filter is built from op amps, resistors and capacitors, its offset voltage will be a simple function of the offset voltages of the op amps and the dc gains of the various filter stages. It's therefore not too difficult to build filters with sub-millivolt offsets using conventional techniques. Switched-capacitor filters have far larger offsets, usually ranging from a few millivolts to about 100 mV; there are some filters available with offsets over 1V! Obviously, switched-capacitor filters are inappropriate for applications requiring dc precision unless external circuitry is used to correct their offsets.

Frequency Range: A single switched-capacitor filter can cover a center frequency range from 0.1 Hz or less to 100 kHz or more. A passive circuit or an op amp/resistor/capacitor circuit can be designed to operate at very low frequencies, but it will require some very large, and probably expensive, reactive components. A fast operational amplifier is necessary if a conventional active filter is to work properly at 100 kHz or higher frequencies.

Tunability: Although a conventional active or passive filter can be designed to have virtually any center frequency that a switched-capacitor filter can have, it is very difficult to vary that center frequency without changing the values of several components. A switched-capacitor filter's center (or cutoff) frequency is proportional to a clock frequency and can therefore be easily varied over a range of 5 to 6 decades with no change in external circuitry. This can be an important advantage in applications that require multiple center frequencies.

Component Count/Circuit Board Area: The switched-capacitor approach wins easily in this category. The dedicated, single-function monolithic filters use no external components other than a clock, even for multipole transfer functions, while passive filters need a capacitor or inductor per pole, and conventional active approaches normally require at least one op amp, two resistors, and two capacitors per second-order filter. Resistor-programmable switched-capacitor devices generally need four resistors per second-order filter, but these usually take up less space than the components needed for the alternative approaches.

Aliasing: Switched-capacitor filters are sampled-data devices, and will therefore be susceptible to aliasing when the input signal contains frequencies higher than one-half the clock frequency. Whether this makes a difference in a particular application depends on the application itself. Most switched-capacitor filters have clock-to-center-frequency ratios of 50:1 or 100:1, so the frequencies at which aliasing begins to occur are 25 or 50 times the center frequencies. When there are no signals with appreciable amplitudes at frequencies higher than one-half the clock frequency, aliasing will not be a problem. In a low-pass or bandpass application, the presence of signals at frequencies nearly as high as the clock rate will often be acceptable because although these signals are aliased, they are reflected into the filter's stopband and are therefore attenuated by the filter.

When aliasing is a problem, it can sometimes be fixed by adding a simple, passive RC low-pass filter ahead of the switched-capacitor filter to remove some of the unwanted high-frequency signals. This is generally effective when the switched-capacitor filter is performing a low-pass or bandpass function, but it may not be practical with high-pass or notch filters because the passive anti-aliasing filter will reduce the passband width of the overall filter response.

Design Effort: Depending on system requirements, either type of filter can have an advantage in this category, but switched-capacitor filters are generally much easier to design. The easiest-to-use devices, such as the LMF40, require nothing more than a clock of the appropriate frequency. A very complex device like the LMF120 requires little more design effort than simply defining the desired performance characteristics. The more difficult design work is done by the manufacturer (with the aid of some specialized software). Even the universal, resistor-programmable filters like the LMF100 are relatively easy to design with. The procedure is made even more user-friendly by the availability of filter software from a number of vendors that will aid in the design of LMF100-type filters. National Semiconductor provides one such filter software package free of charge. The program allows the user to specify the filter's desired performance in terms of cutoff frequency, a passband ripple, stopband attenuation, etc., and then determines the required characteristics of the second-order sections that will be used to build the filter. It also computes the values of the external resistors and produces amplitude and phase vs. frequency data.

Where does it make sense to use a switched-capacitor filter and where would you be better off with a continuous filter? Let's look at a few types of applications:

Tone Detection (Communications, FAXs, Modems, Biomedical Instrumentation, Acoustical Instrumentation, ATE, etc.): Switched-capacitor filters are almost always the best choice here by virtue of their accurate center frequencies and small board space requirements.

Noise Rejection (Line-Frequency Notches for Biomedical Instrumentation and ATE, Low-Pass Noise Filtering for General Instrumentation, Anti-Alias Filtering for Data Acquisition Systems, etc.): All of these applications can be handled well in most cases by either switched-capacitor or conventional active filters. Switched-capacitor filters can run into trouble if the signal bandwidths are high enough relative to the center or cutoff frequencies to cause aliasing, or if the system requires dc precision. Aliasing problems can often be fixed easily with an external resistor and capacitor, but if dc precision is needed, it is usually best to go to a conventional active filter built with precision op amps.

Topics on Using the LM6181—A New Current Feedback Amplifier

National Semiconductor
Application Note 813

Use your imagination . . . that's what jazz is all about. If you make a mistake, make it loud so you won't make it next time. **—Art Blakey**

INTRODUCTION

High-speed analog system design can often be a daunting task. Typically, after the initial system definition and the design approach is established, the task of component selection commences. Unfortunately, simple reliance on data sheet parameters provides only a partial feel for the device's actual operating nuances. This is unfortunately true no matter how complete a high-speed amplifier data sheet is written. Only by experimenting i.e., spending some time on the bench with the part, will the requisite experience be obtained for reliably using high-speed amplifiers. The high-speed demonstration board, described herein, can be effectively used to accelerate this process. In developing the LM6181 application program, the key focus areas for making high-speed design a little easier included:

- Designing a product that is more forgiving—for example it can directly drive backmatched cables (a heavy dc load), and significant capacitive loads (without oscillating).
- Developing a high-speed demonstration board that is easily reconfigurable for either inverting or non-inverting amplifier operation.
- Incorporate a highly accurate SPICE macromodel of the LM6181 into National's macromodeling library. This macromodel can be used in conjunction with bench results to more quickly converge on a reliable high-speed design.

Although it may seem that evaluation of high-speed circuit operation can be more quickly performed with computer simulation, full bench evaluation can not be supplanted. By integrating *both* of these complementary tools, the cycle time from component selection to finalized design can be reduced.

SOME BACKGROUND INFORMATION ON THE LM6181

The LM6181 is a high-speed current feedback amplifier with typical slew rates of 2000 V/μs, settling time of 50 ns for 0.1%, and is fully specified and characterized for ±5V, and ±15V operation. Current feedback operational amplifiers, like the LM6181, offer two significant advantages over the more popular voltage feedback topology. These advantages include a bandwidth that is relatively independent of closed-loop gain (see *Figure 1*), and a large signal response that is closer to ideal. "Ideal" specifically means that the large signal response is not overtly dominated by non-linear slewing behavior (Ref. 1), as is typically found for voltage feedback amplifiers. An obvious consequence is dramatic improvement in distortion performance versus the signal amplitude, and settling time.

The high-speed demonstration board can be used to either examine the time domain, or frequency domain. However, the discussion will focus on using this board for the purpose of compensating the time domain response of the LM6181 for popular applications.

LM6181 Closed-Loop Frequency Response
$V_S = \pm 15V$; $R_f = 820\Omega$; $R_L = 1\,k\Omega$

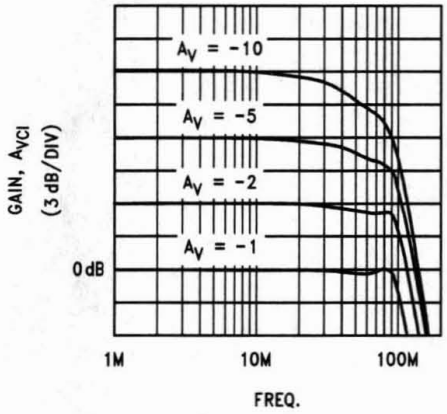

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FIGURE 1. Unlike voltage feedback amplifiers which directly trade bandwidth for gain, current feedback amplifiers provide consistently wideband performance regardless of moderate closed-loop gain levels.

Examples of this includes driving cables, dealing with capacitive loads, and generally obtaining a user specified fidelity to the pulse response. Essentially, the demonstration board simplifies the evaluation of high speed operational amplifiers in either the inverting, or the non-inverting circuit configurations. Appendix A includes the board schematic with the associated configuration options. Layout of the board included a host of mandatory high speed design considerations. These principles have been summarized in Appendix B (also see Ref. 2 to 4).

A popular application for high speed amplifiers includes driving backmatched cables as illustrated in *Figure 2*. Due to loading and typical bandwidth requirements this particular application places heavy demands on an amplifier. The LM6181 output stage incorporates a high-current-gain output stage that provides a lower output impedance into heavy loads, such as 100Ω and 150Ω. This enhances the amplifier's ability to drive backmatched cables (±10V, into 100Ω) since the internal current drive to the amplifiers output stage is used more efficiently. Additionally, the benefits of the current feedback topology of the LM6181 allows for wideband operation of 100 MHz, even when configured in closed-loop gain configuration of +2.

Controllable, Variable Frequency Filtering (Spectrum Analysis, Multiple-Function Filters, Software-Controlled Signal Processors, etc.): Switched-capacitor filters excel in applications that require multiple center frequencies because their center frequencies are clock-controlled. Moreover, a single filter can cover a center frequency range of 5 decades. Adjusting the cutoff frequency of a continuous filter is much more difficult and requires either analog switches (suitable for a small number of center frequencies), voltage-controlled amplifiers (poor center frequency accuracy) or DACs (good accuracy over a very limited control range).

Audio Signal Processing (Tone Controls and Other Equalization, All-Pass Filtering, Active Crossover Networks, etc.): Switched-capacitor filters are usually too noisy for "high-fidelity" audio applications. With a typical dynamic range of about 80 dB to 90 dB, a switched-capacitor filter will usuallly give 60 dB to 70 dB signal-to-noise ratio (assuming 20 dB of headroom). Also, since audio filters usually need to handle three decades of signal frequencies at the same time, there is a possibility of aliasing problems. Continuous filters are a better choice for general audio use, although many communications systems have bandwidths and S/N ratios that are compatible with switched capacitor filters, and these systems can take advantage of the tunability and small size of monolithic filters.

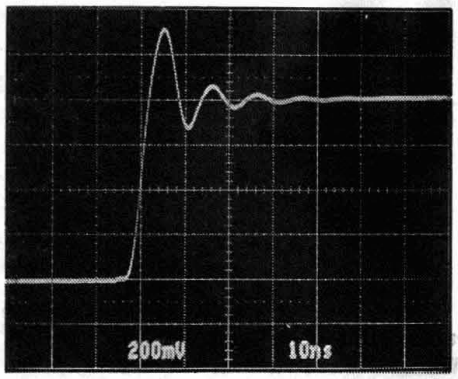

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FIGURE 4. Output response of a real LM6181, $A_V = +2$, $R_f = R_G = 820\Omega$. Output load is oscilloscope probe, Tektronix P6106A, 10 MΩ, 8.7 pF.

COMPENSATING THE PULSE RESPONSE

Degradation in the phase margin, due to direct capacitive loading of high-speed amplifiers can potentially induce oscillation. The output impedance of the amplifier, coupled with the load capacitance, forms a lag network in the loop transmission of the amplifier. Since this network delays the feedback, phase margin is reduced such that even when a system is not oscillating excessive ringing can occur, as illustrated in *Figure 6* where the capacitive load is 48 pF.

A direct solution to reducing the ringing for driving capacitive loads is to indirectly drive the load i.e., isolate the load with a real impedance, such as a moderately small value of resistance. In *Figure 7* a 47Ω resistor was used to isolate the capacitor's complex impedance from the amplifier's output, thereby preserving the amplifier's phase margin. An obvious tradeoff exists between taming the time domain response, and maintaining the amplifier's bandwidth, since this form of compensation directly slows down the amplifier's response.

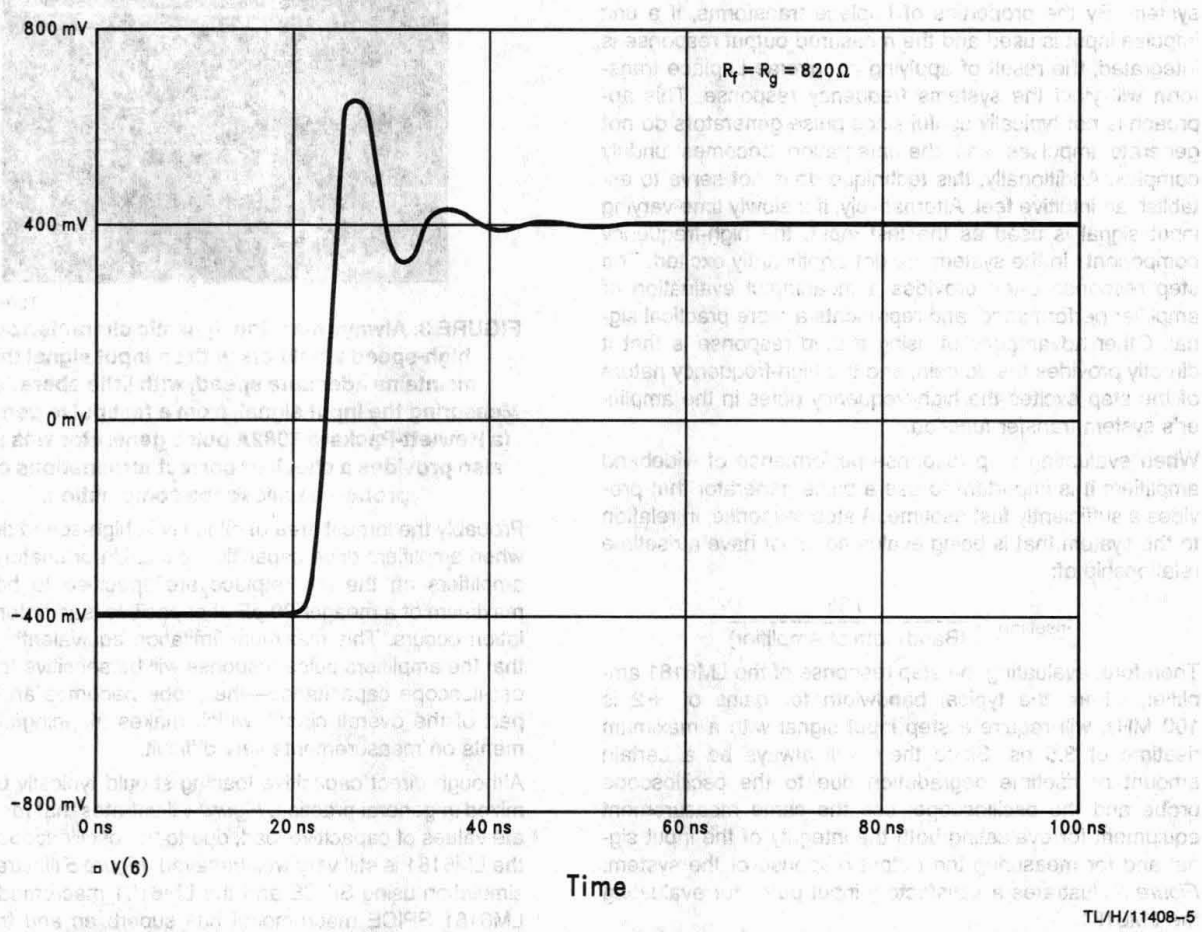

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FIGURE 5. Simulated output response of the circuit in *Figure 3* using the LM6181 macromodel. See Appendix C for more information regarding the LM6181 macromodel and National's Macromodel library.

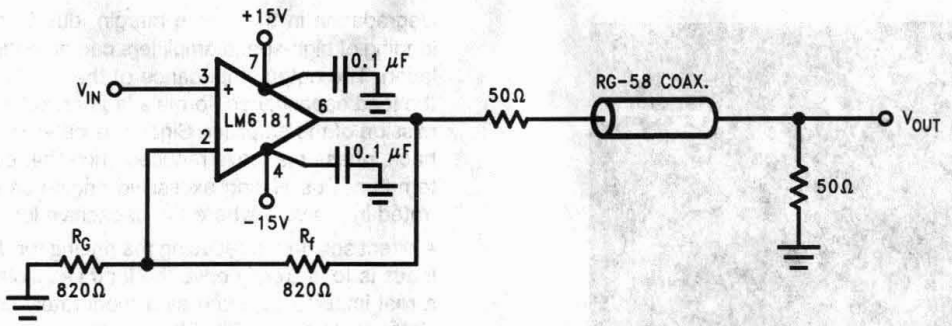

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FIGURE 2. Backmatching of a cable is a clean way of terminating the source to the characteristic impedance. The LM6181 can deliver ±10V into the resulting dc load of 100Ω, at 100 MHz, typically.

EXPERIMENTING WITH THE TIME DOMAIN

Some consideration needs to be addressed for the test signal chosen to evaluate the transient response of a linear system. By the properties of Laplace transforms, if a unit impulse input is used and the measured output response is integrated, the result of applying an inverse Laplace transform will yield the systems frequency response. This approach is not typically useful since pulse generators do not generate impulses and the integration becomes unduly complex. Additionally, this technique does not serve to establish an intuitive feel. Alternatively, if a slowly time-varying input signal is used as the test input, the high-frequency components in the system are not significantly excited. The step response often provides a meaningful evaluation of amplifier performance, and represents a more practical signal. Other advantages of using a step response is that it directly provides the dc gain, and the high-frequency nature of the step excites the high-frequency poles in the amplifier's system transfer function.

When evaluating step response performance of wideband amplifiers it is important to use a pulse generator that provides a sufficiently fast risetime. A step response, in relation to the system that is being evaluated, must have a risetime relationship of:

$$t_{risetime} < \frac{0.35}{(\text{Bandwidth of Amplifier})}$$

Therefore, evaluating the step response of the LM6181 amplifier, where the typical bandwidth for gains of +2 is 100 MHz, will require a step input signal with a maximum risetime of 3.5 ns. Since there will always be a certain amount of risetime degradation due to the oscilloscope probe and the oscilloscope, use the same measurement equipment for evaluating both the integrity of the input signal and for measuring the output response of the system. *Figure 3* illustrates a satisfactory input pulse for evaluating the LM6181.

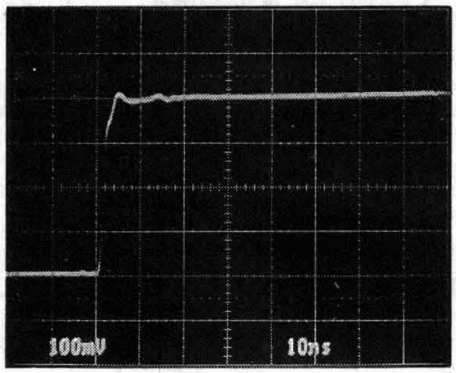

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FIGURE 3. Always start the dynamic characterization of high-speed amplifiers with an input signal that maintains adequate speed, with little aberation. Measuring the input signal, from a fast pulse generator, (a Hewlett-Packard 8082A pulse generator was used), also provides a check of correct terminations of the probe—oscilloscope combination.

Probably the largest area of difficulty in high-speed design is when amplifiers drive capacitive loads. Unfortunately, many amplifiers on the marketplace are specified to handle a maximum of a meager 20 pF of capacitive load before oscillation occurs. This maximum limitation equivalently implies that the amplifiers pulse response will be sensitive to typical oscilloscope capacitance—the probe becomes an integral part of the overall circuit, which makes meaningful judgements on measurements very difficult.

Although direct capacitive loading should typically be minimized in general practice, *Figure 4* illustrates that for moderate values of capacitive load, due to the oscilloscope probe, the LM6181 is still very well behaved. *Figure 5* illustrates the simulation using SPICE and the LM6181 macromodel. The LM6181 SPICE macromodel has superb ac and transient response characteristics. For availability information concerning the complete macromodeling library, including the LM6181, along with an outline of the model's capabilities, refer to Appendix C.

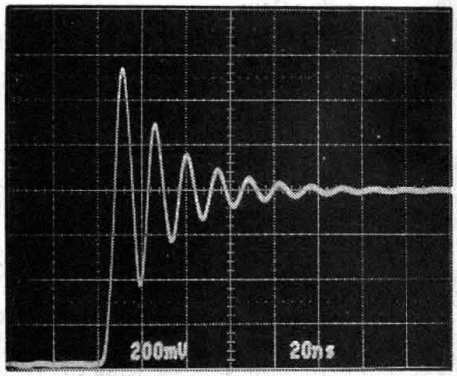

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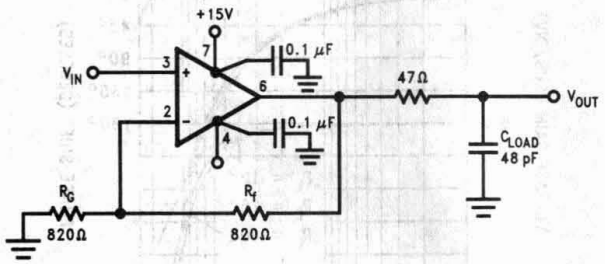
FIGURE 6. Direct capacitive loading will reduce the phase margin and resulting pulse fidelity of any amplifier. A pole is created by the combination of the op amp's output impedance and the capacitive load. This results in delaying the feedback or loop transmission. In this example the LM6181 is directly driving a 48 pF load. High-speed current-feedback amplifiers can handle capacitive loads, and maintain pulse fidelity, by indirectly driving them. This is illustrated in *Figure 7*.



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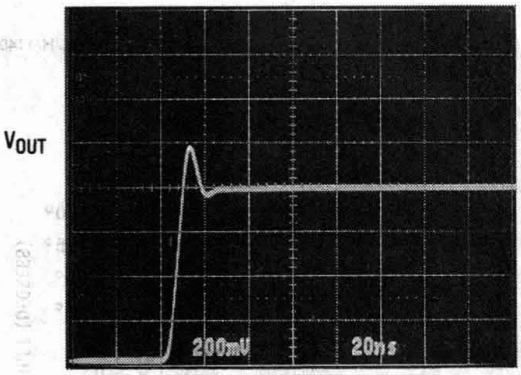

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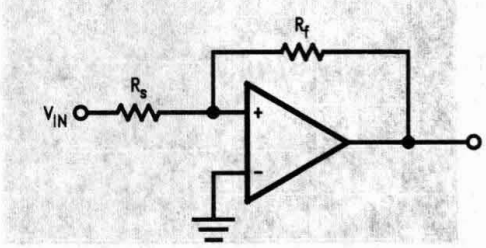
FIGURE 7. A small resistor can be used, such as 47Ω, at the output of the amplifier to indirectly drive capacitive loads.

For general applications of the LM6181, the suggested feedback resistance, R_f, is 820Ω. However, a characteristic unique to current-feedback amplifiers is that they will have different bandwidths depending on the feedback resistor R_f. This results in current-feedback amplifiers maintaining a net closed-loop bandwidth that remains (this is of course an approximation; second order effects do take their toll, of course) the same for moderate variations of closed-loop gain. This feature of current feedback amplifiers actually makes them relatively easy to compensate. By simply scaling the gain setting and the feedback impedance, the appropriate bandwidth can be obtained at the desired value of closed-loop gain. *Figure 8* was cut from the LM6181 data sheet, and describes this relationship.



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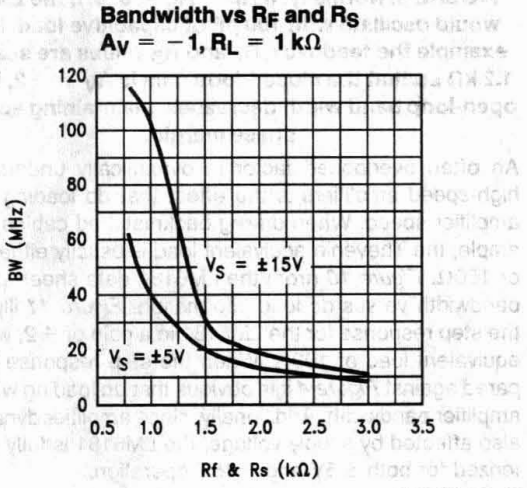

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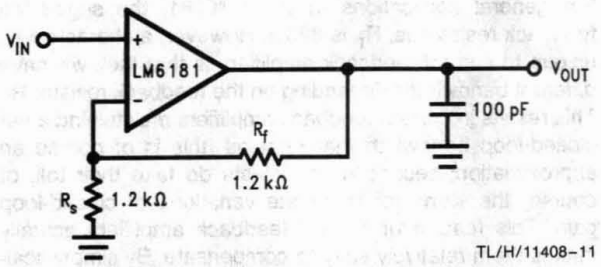
FIGURE 8. By scaling both R_F and R_S the closed-loop gain stays constant but the bandwidth changes.

A practical application of using altered feedback values for compensating the LM6181 when driving a 100 pF capacitive load is illustrated in *Figure 9*. By reducing the open-loop bandwidth of the amplifier, the resulting degradation of phase margin is reduced, thereby improving the pulse response fidelity.



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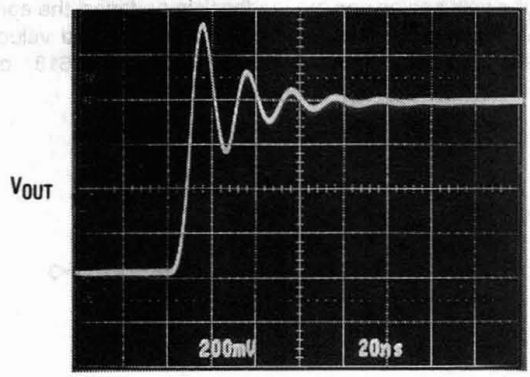

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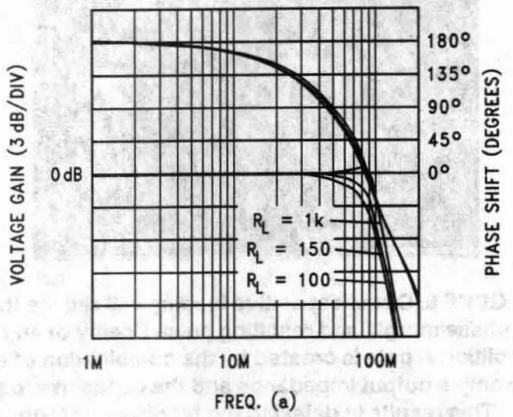
FIGURE 9. Normally, if $R_F = R_S = 820\Omega$, the LM6181 would oscillate with 100 pF of capacitive load. In this example the feedback, R_F and R_S values are scaled to 1.2 kΩ so that the closed-loop gain is $A_V = +2$, but the open-loop band width decreases, maintaining adequate phase margin.

An often overlooked factor in dynamically understanding high-speed amplifiers is the effect that dc loading has on amplifier speed. When driving backmatched cables, for example, the Thevenin equivalent load is usually either 100Ω, or 150Ω. *Figure 10* (from the LM6181 data sheet) provides bandwidth versus dc load information. *Figure 11* illustrates the step response for the LM6181 in a gain of +2, with a dc equivalent load of 100Ω. When the step response is compared against *Figure 4* it is obvious that dc loading will affect amplifier bandwidth. Additionally, since amplifier dynamics is also affected by supply voltage, the LM6181 is fully characterized for both ±5V and ±15V operation.

Inverting Gain
Frequency Response
$V_S = \pm 15V$; $A_V = -1$;
$R_F = 820\Omega$



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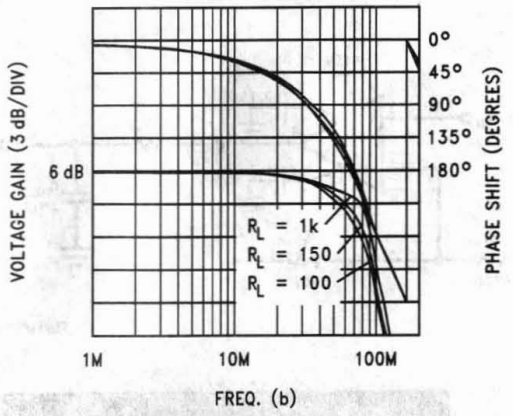
Non-Inverting Gain
Frequency Response
$V_S = \pm 15V$; $A_V = +2$;
$R_f = 820\Omega$



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Inverting Gain
Frequency Response
$V_S = \pm 15V$; $A_V = -10$;
$R_F = 820\Omega$

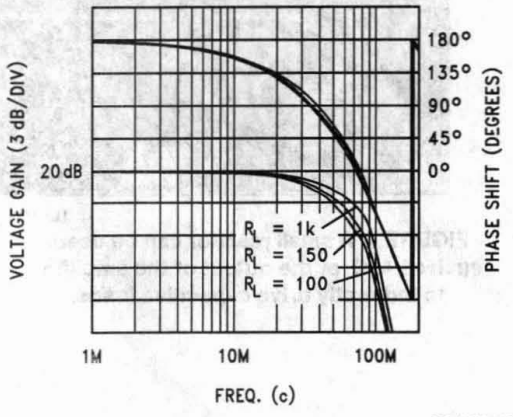

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FIGURE 10. DC loading of a high-speed amplifier will affect bandwidth. (Refer to the LM6181 data sheet for ±5V bandwidth vs loading characteristic curves.)

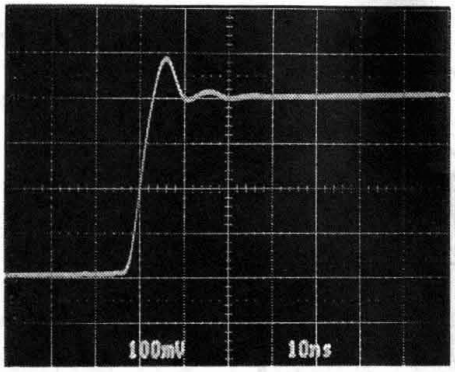

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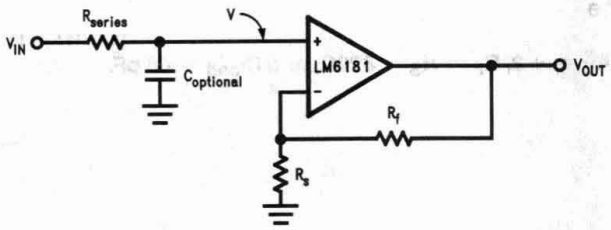
FIGURE 11. Output step response of LM6181 when driving backmatched cables. Comparing this step response to *Figure 4* illustrates the bandwidth reduction due to the 100Ω resistive load.

COMPENSATING NON-INVERTING CF AMPLIFIERS

Often, for the inverting amplifier configuration, simply scaling the feedback and gain setting resistor is the easiest way of compensating for peaking and overshoot in the step response. The non-inverting configuration, however, can alternatively be compensated by adding a series input resistor, as shown in *Figure 12*. This resistor, in combination with the input and stray input capacitances of the amplifier bandwidth limit the input step response, and accordingly reduce peaking in the output response. This effect is equivalent to increasing the risetime of the leading edge of the input pulse (some pulse generators have this adjustment).



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$$f_{-3\,dB\ of\ V} \approx \frac{1}{2\pi\,(C_{optional} + 3\,pF) \bullet R_{series}}$$

FIGURE 12. Peaking and ringing for non-inverting amplifier configurations can be reduced by adding a series input resistor, R_{series}. This resistor interacts with the amplifiers input capacitance to provide a low pass bandwidth limit for the input pulse. If more bandwidth reduction is required $C_{optional}$ can be used.

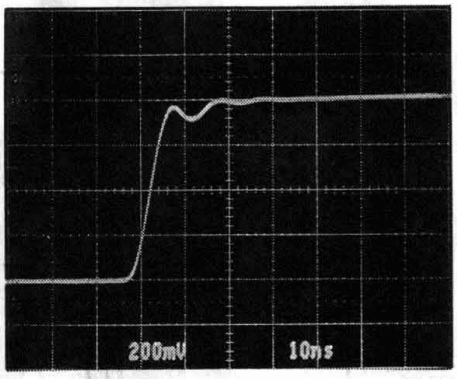

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FIGURE 13. Resulting pulse response for LM6181 using $R_{series} = 680\Omega$, $A_V = +2$, $R_S = R_F = 820\Omega$, $C_{LOAD} \approx 8.7$ pF. Compare this response with *Figure 4*, overshoot and ringing has been dramatically reduced.

SNAKE OIL AND SPICE MACROMODELS CURE ALL EVILS

Not all amplifier macromodels are created equal. For example, driving capacitive loads with high-speed amplifiers is a good way of evaluating and comparing op-amp macromodels. Capacitive loading directly affects the loop dynamics of a closed-loop amplifier system. And since this capacitive load interacts with the output impedance of the amplifier to delay the feedback (or loop transmission), the phase margin is reduced, as stated earlier.

Simulating high-speed systems when driving capacitive loads places a demand on the amplifier's macromodel. Constructing an accurate macromodel is not simple. Unfortunately, parameterized models (an efficient method of using a computer to generate many inaccurate models per a typical workday) lack the extensive software testing and bench measurement analysis required for sophisticated simulation work. The amplifier's output stage, the frequency response, and the input parasitic structures need to be carefully measured on the bench, then accurately mimicked in the macromodel. The moral is to be aware, and :

ALWAYS TEST YOUR MACROMODEL!

Compare the similarity between results in *Figure 14* with the bench results of *Figure 6*. Increased confidence in using a specific high-speed amplifier macromodel can be obtained by corresponding bench results of driving capacitive loads with simulation results.

Driving reactive loads, such as capacitive loads, can be used not only to indicate limitations for the associated SPICE macromodel, but also to reveal some of the amplifier's high-speed personality. Never assume that a macromodel of an operational amplifier includes characteristics that are germane to your particular simulation.

SUMMING THINGS UP

The focus has been on high-speed analog design methodology, as opposed to generating a plethora of varied application circuits. By establishing a foundation—understanding the amplifier, referring to the typical characterization curves, using correct high-speed layout techniques, knowing the SPICE macromodels limitations, and adopting some basic compensation techniques, a large fraction of everyday high-speed design challenges can be addressed confidently.

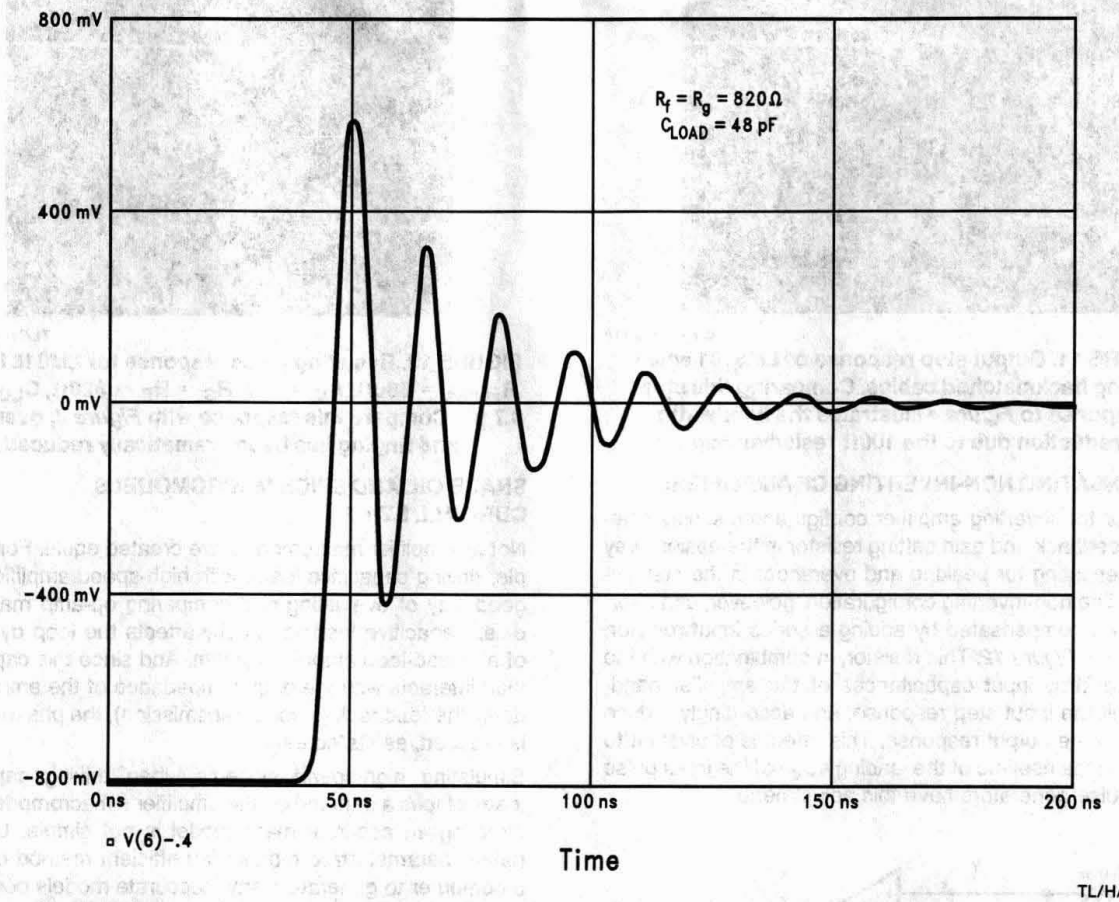

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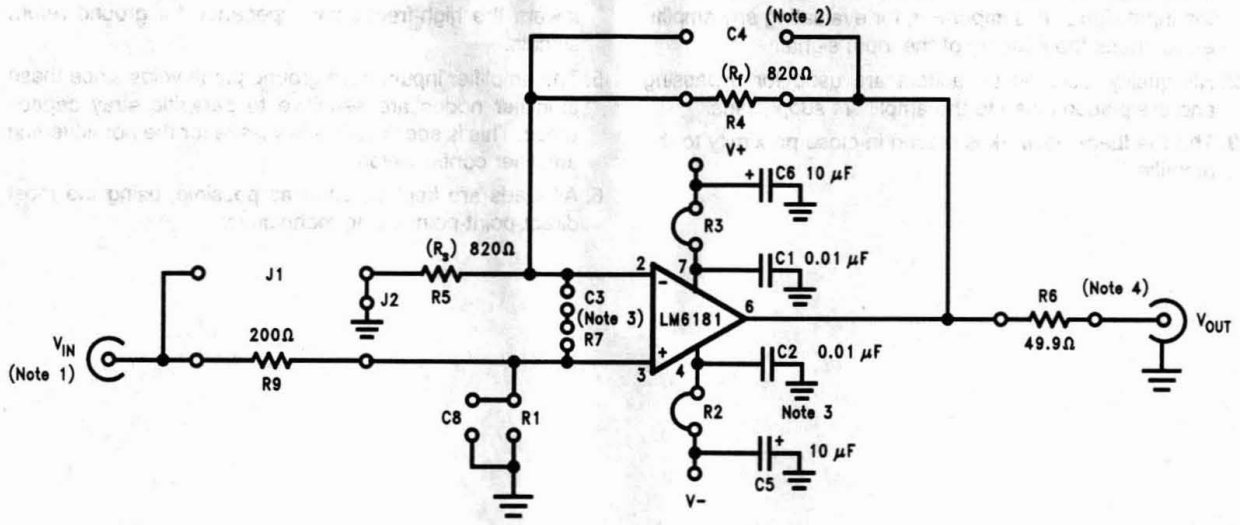
FIGURE 14. Simulation of LM6181 step response with $A_V = +2$, $R_F = R_S = 820\Omega$, and $C_{load} = 48$ pF.

Appendix A



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The LM6181 high speed demonstration board can be configured for either inverting or non-inverting amplifier configurations. This board was intentionally embellished with options so that it can be used as a general-purpose 8-pin opamp evaluation board.

Note 1: Terminate this BNC connection with the appropriate connector. Otherwise ringing due to high-frequency reflections will occur.

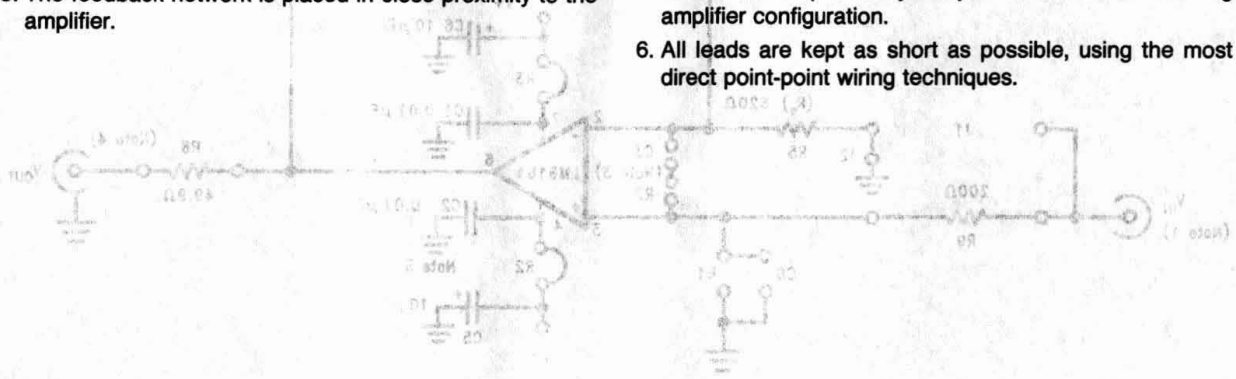
Note 2: Do not lead compensate current feedback amplifiers—oscillation will result. Lead compensation uses a feedback capacitor, C_4.

Note 3: C3 and R7 are optional lag-compensation network points.

Note 4: R6 is for back matched driving of cables.

Appendix B: High Speed Board Design Caveats

1. Good high frequency termination is always required for the input signal. It is important, for evaluating any amplifier, to check the integrity of the input signal.
2. RF quality, ceramic capacitors are used for bypassing and are placed close to the amplifiers supply pins.
3. The feedback network is placed in close proximity to the amplifier.
4. The entire top side of the board is ground planed. This lowers the high-frequency impedance for ground return signals.
5. The amplifier inputs have ground plane voids since these amplifier nodes are sensitive to parasitic stray capacitance. This is specifically a key issue for the non-inverting amplifier configuration.
6. All leads are kept as short as possible, using the most direct point-point wiring techniques.



Appendix C: Features Modeled For LM6181 Macromodel

Supply-Voltage-Dependent Input Offset Voltage (V_{OS})

Temperature-Dependent Input Offset Voltage (TCV_{OS})

Supply-Voltage-Dependent Input Bias Current (I_{b+} & I_{b-} PSR)

Temperature-Dependent Input Bias Current (TCI_{B+} & TCI_{B-})

Input-Voltage-Dependent Input Bias Current (I_{b-} CMRR)

Non-Inverting Input Resistance

Asymmetrical Output Swing

Output Short Circuit Current (I_{SC})

Supply-Voltage-Dependent Supply Current

Quiescent and Dynamic Supply Current

Input-Voltage-Dependent Input Slew Rate

Input-Voltage-Dependent Output Slew Rate

Multiple Poles and Zeroes in Open-Loop Transimpedance (Z_t)

Supply-Voltage-Dependent Input Buffer Impedance

Supply-Voltage-Dependent Open-Loop Voltage Gain (A_{VOL})

Feedback-Resistance-Dependent Bandwidth

Accurate Small-Signal Pulse Response

Large-Signal Pulse Response

DC and AC Common Mode Rejection Ratio (CMRR)

DC and AC Power Supply Rejection Ratio (PSRR)

White and 1/f Voltage Noise (e_n)

White and 1/f Current Noise (i_n)

For information related to obtaining National's SPICE macromodeling library, including the LM6181, call a National sales office.

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Increasing the High Speed Torque of Bipolar Stepper Motors

National Semiconductor
Application Note 828
Steven Hunt

INTRODUCTION

To successfully follow a velocity profile, a motor and drive combination must generate enough torque to: accelerate the load inertia at the desired rates, and drive the load torque at the desired speeds. While the size of a bipolar stepper motor generally dictates the low speed torque, the ability of the drive electronics to force current through the windings of the motor dictates the high speed torque. This application note shows that increasing the slew rates of the winding currents in a bipolar stepper motor pushes the motor to deliver more torque at high speeds. Simple voltage drives, L/R drives, and chopper drives are explained. L/R drives and chopper drives achieve slew rates higher than those achieved by simple voltage drives. Finally, an example chopper drive is presented.

BACKGROUND

In standard full-step operation, quadrature (out of phase by 90°) bipolar currents (*Figure 1*) energize the windings of a bipolar stepper motor. One step occurs at each change of direction of either winding current, and the motor steps at four times the frequency of the currents. The ideal winding currents of *Figure 1* exhibit infinite slew rates.

Ideally, each phase contributes a sinusoidal torque;

$$T_1 = -i_1\, T\sin(N\theta) \text{ and} \quad (1)$$

$$T_2 = i_2\, T\cos(N\theta), \quad (2)$$

with the winding currents, i(t), in amps and the torque constants, $-T\sin(N\cdot\theta)$ and $T\cos(N\cdot\theta)$, in newton•centimeters per amp. θ represents the angular displacement of the rotor relative to a stable detent (zero torque) position. N represents the number of motor poles; that is, the number of electrical cycles per mechanical cycle or revolution. $N\cdot\theta$, therefore, represents the electrical equivalent of the mechanical rotor position. The torque contributions add directly to yield a total torque of

$$T_t = T_1 + T_2 = T\,(i_2 \cos(N\theta) - i_1 \sin(N\theta)). \quad (3)$$

Integrating (3) over a full period of one of the torque constants and multiplying the result by the reciprocal of that period gives the average torque generated by the motor. Assuming ideal square wave winding currents and sinusoidal torque constants (*Figure 2*), the motor generates an average torque of

$$T_{avg} = \frac{1}{2\pi}\left[\int_0^{2\pi} -i_1\, T\sin(N\theta)\, dN\theta + \int_0^{2\pi} i_2\, T\cos(N\theta)\, d\,N\theta\right] = \quad (4)$$

$$= \frac{2}{\pi} I_{rated}\, T\cos\phi. \quad (5)$$

In open loop applications, ϕ adjusts automatically to match the average torque generated by the motor with that required to execute a motion task. When the winding currents and their respective torque constants are in phase (ϕ is zero), the motor generates the maximum average torque or *pull-out torque;*

$$T_{pull\text{-}out} = T_{avg\,(max)} = \frac{2}{\pi} I_{rated}\, T. \quad (6)$$

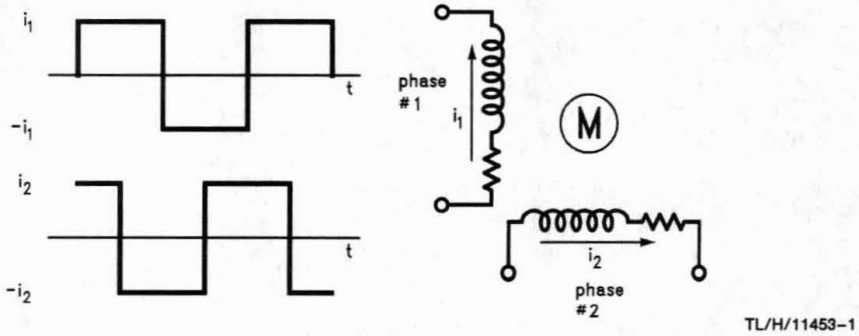

FIGURE 1. Ideal Quadrature Currents Drive the Windings of a Bipolar Stepper Motor

Square waves make good approximations for the winding currents at low speeds only, and (6), therefore, makes a good approximation of the pull-out torque at low speeds only. Real winding currents have an exponential shape dictated by the L/R-time constants of the windings, the voltage applied across the windings, and, to a lesser extent, the back emf generated by the motor as the rotor spins. For either winding,

$$i(t) = \left(I_o - \frac{V_{CC} - V_{emf}}{R}\right) e^{\frac{-R}{L}t} + \frac{V_{CC} - V_{emf}}{R} \qquad (7)$$

describes the winding current at a change in the direction of that current, where I_o is the initial winding current, V_{CC} is the voltage applied across the winding, V_{emf} is the back emf, and R and L are the winding resistance and inductance. At low step rates, assuming $V_{CC} = V_{rated} >> V_{emf}$, the current easily slews to the peak value of V_{rated}/R before a subsequent direction change *(Figure 3a).* At higher step rates, because the time between direction changes is shorter, the current cannot reach the peak value *(Figure 3b).* V_{rated} is the rated voltage of the windings.

Clearly from (4) and *Figure 3*, as the speed increases, decreases in the winding currents result in decreases in $T_{pull\text{-}out}$. The torque vs. speed characteristic of a typical bipolar stepper motor (*Figure 4*) reflects this phenomenon. Each pull-out torque curve bounds (on the right) a region of torque-speed combinations inside which the stepper motor runs and outside which the stepper motor stalls.

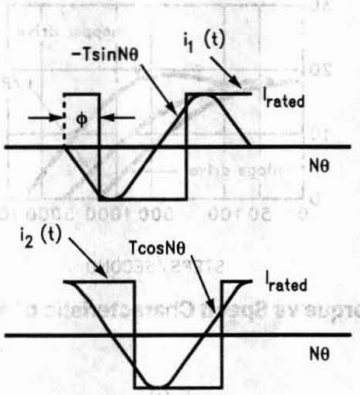

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FIGURE 2. Ideal Square Wave Winding Currents and Sinusoidal Torque Constants for Average Torque Calculation

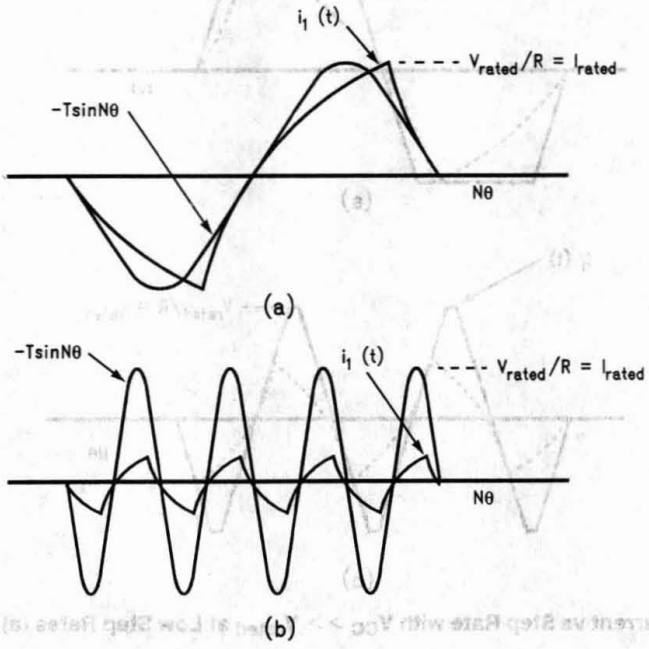

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FIGURE 3. Real Winding Current and Sinusoidal Torque Constant vs Step Rate at Low Step Rates (a) and at High Step Rates (b)

It follows then, that the goal of increasing the high speed torque is achieved by increasing the winding currents at high speeds. This, in turn, is achieved by increasing the slew rates of the winding currents; for example, with the increased slew rates realized by raising V_{CC} well above V_{rated}, the winding current easily slews to the peak value of V_{rated}/R at both low and high step rates (*Figure 5*). Winding currents realized with $V_{CC} = V_{rated}$ are represented with dashed lines, and, assuming a means for limiting at V_{rated}/R, winding currents realized with $V_{CC} >> V_{rated}$ are represented with solid lines.

Both decreasing the L/R-time constants of the windings and increasing the voltage applied across the windings increases the slew rates of the winding currents. L/R drives and chopper drives take these tactics to raise the slew rates of the winding currents well above those realized by simply applying the rated voltage to the windings. The torque vs. speed characteristic of a typical bipolar stepper motor (*Figure 4* again) reflects the resulting high speed torque gains.

It is important to note, however, that applying $V_{CC} >> V_{rated}$ also results in excessive winding currents at low speeds. The winding currents must be held at or below the rated limit (usually V_{rated}/R per winding) to hold power dissipated inside the motor at or below the rated limit (usually $2 \times V_{rated} \times I_{rated}$).

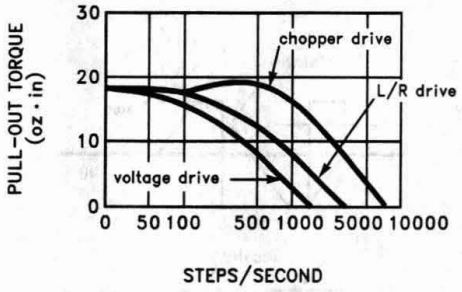

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FIGURE 4. A Typical Torque vs Speed Characteristic of a Bipolar Stepper Motor

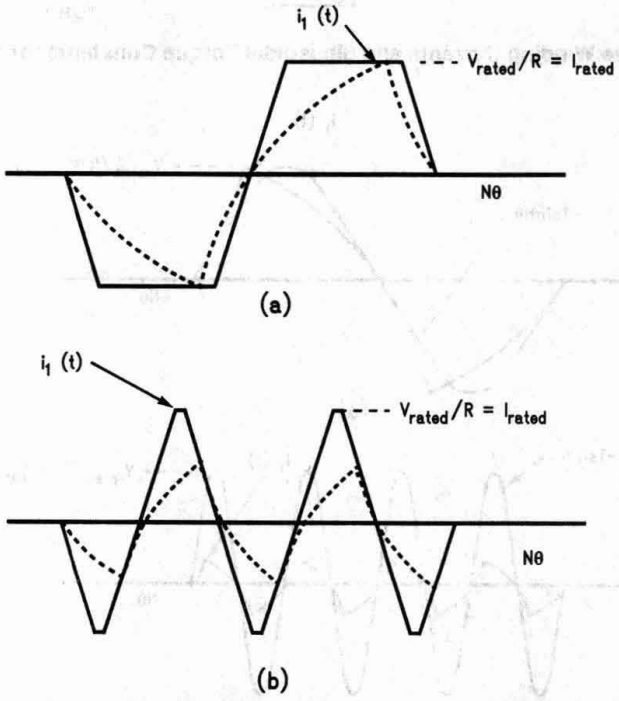

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FIGURE 5. Real Winding Current vs Step Rate with $V_{CC} >> V_{rated}$ at Low Step Rates (a) and at High Step Rates (b)

SIMPLE VOLTAGE DRIVES

Simple drives employ two H-bridge power amplifiers to drive bipolar currents through the phase windings (*Figure 6*). For either amplifier, closing switches S1 and S4 forces the rated voltage (less two switch drops) across the winding, and current flows from supply to ground via S1, the winding, and S4. After opening S1 and S4, closing S2 and S3 reverses the direction of current in the winding. This drive scheme is commonly referred to as simple voltage drive. Because only the winding resistances limit the winding currents, V_{CC} cannot exceed V_{rated}.

L/R DRIVES

L/R drives employ two series power resistors to decrease the L/R-time constants of the windings; for example, a 45Ω power resistor in series with each of two 15Ω winding resistances divdes the L/R-time constants by four and allows the rated supply voltage to be increased by a factor of four. Both the crispness of the response and the high speed torque are increased. While the rotor holds position or moves at low step rates, the series power resistors protect the motor by holding the winding currents to the rated limit.

Since both the L/R-time constants of the phase windings and the rated supply voltage were increased by a factor of four, the example drive would commonly be referred to as an L/4R drive.

The maximum operating supply voltage of the power amplifiers can limit the factor by which the supply voltage is increased above the rated voltage of the windings, but power losses in the series resistors more likely limit this factor. If, for example, 60V is applied across two 0.5A, 15Ω phase windings, two 105Ω series resistors are required to hold the winding currents to the 0.5A/phase limit. This is an L/8R drive. Power dissipated in the series resistors while the rotor holds position is $105 \times 0.5 \times 0.5 \times 2 = 52.5W$, while power dissipated in the entire drive is $60 \times 0.5 \times 2 = 60W$. The drive efficiency approaches 12.5%. After looking at these numbers, the drive designer may opt to cut losses by using the 30V power supply/45Ω series resistor combination of an L/4R drive. Unfortunately, while the rotor holds position, total power dissipated in the series resistors remains high at 22.5W and drive efficiency remains low at 25%.

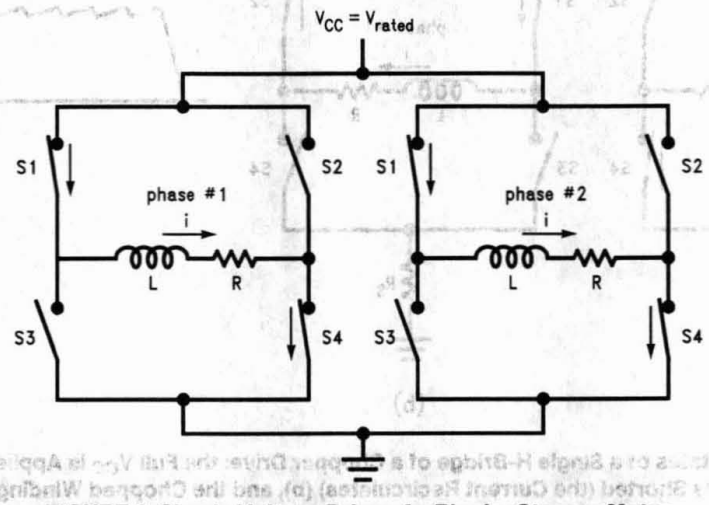

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FIGURE 6. Simple Voltage Drive of a Bipolar Stepper Motor

CHOPPER DRIVES

Chopper drives increase the slew rates of the winding currents by applying $V_{CC} >> V_{rated}$. Feedback-driven switching of the H-bridges holds the winding currents to the rated limit. *Figure 7* shows the chopping states of a single H-bridge of a chopper drive. A low value resistor in the ground lead of the H-Bridge converts the winding current into a proportional feedback voltage, and the feedback voltage is compared to a reference voltage (not shown). While the feedback voltage is less than the reference voltage, switches S1 and S4 apply the full supply voltage across the winding (*Figure 7a*), and the winding current increases rapidly. When the feedback voltage is equal to the reference voltage; that is, when the winding current reaches the desired limit, S1 and S2 short the winding for a fixed period or *off-time* (*Figure 7b*). During the off-time, the winding current *recirculates* and decays slowly. At the end of the off-time, S1 and S4 reapply the full supply voltage across the winding, and the winding current again increases. Repetition of this sequence results in a *current chopping action* that limits the peak winding current to a level determined by the reference voltage and the resistor in the ground lead of the amplifier (*Figure 7c*), limit = $V_{reference}/R_S$. Chopping of the current only occurs when the current reaches the desired limit (usually the rated current of the winding). When the winding current changes direction to step the motor, the general operation remains the same except S2 is held closed and S1 and S3 are switched to limit the winding current. Because the H-bridge shorts the winding for a fixed period, this type of chopper drive is commonly referred to as a *fixed off-time* drive. By eliminating the series resistors required by L/R drives, chopper drives increase dramatically the drive efficiency. Typical efficiencies of chopper drives range from 75% to 90%.

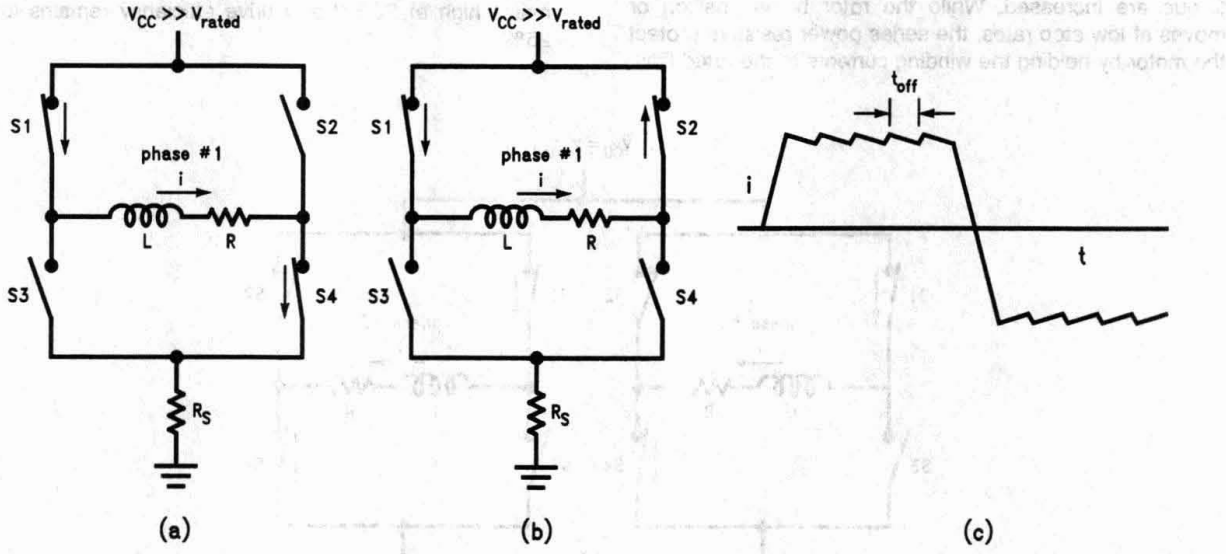

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FIGURE 7. The Chopping States of a Single H-Bridge of a Chopper Drive: the Full V_{CC} is Applied Across the Winding (a), the Winding is Shorted (the Current Recirculates) (b), and the Chopped Winding Current (c)

AN LMD18200-BASED CHOPPER DRIVE

The LMD18200 is a 3A, 55V H-bridge (*Figure 8*). It is built using a multi-technology process which combines bipolar and CMOS control (logic) and protection circuitry with DMOS power switches on the same monolithic structure. The LMD18200 data sheet and AN-694 contain more information about the operation of the LMD18200.

Two LMD18200 H-bridges form the core of an example chopper drive (*Figure 9*). The PWM input (pin #5) of each LMD18200 accepts a logic signal that controls the state of that device. While the signal at PWM is logic-high, the H-bridge applies the full supply voltage across the winding, and while the signal at PWM is logic-low, the upper two switches of the H-bridge short the winding. The feedback voltage associated with either H-bridge is directly proportional to the current in the winding driven by that device. One half of an LM319 dual comparator compares the feedback voltage to the reference voltage. While the feedback voltage is less than the reference voltage, the signal at PWM is logic-high, the LMD18200 applies the full supply voltage across the winding, and the winding current increases. When the winding current increases to the point the feedback voltage and the reference voltage are equal, the LM319 triggers the LMC555-based one-shot. For the duration of the one-shot timing pulse, the signal at PWM is logic-low, the LMD18200 shorts the winding, and the winding current *recirculates* and decays. After the timing pulse, the signal, a PWM returns to logic-high, the LMD18200 reapplies the full supply voltage across the winding, and the winding current again increases. Repetition of this sequence results in a current chopping action (*Figure 10*) that limits the winding current to the 0.5A rating while allowing the 12V, 24Ω winding to be driven with 36V. **Note:** the RC components associated with the LMC555 set the one-shot timing pulse. To best illustrate the current chopping action, the one-shot timing pulse or off-time was set at approximately 100μs. Shorter off-times yield smoother winding currents.

The Dir input (pin #3) of each LMD18200 accepts a logic signal that controls the direction of the current in the winding driven by that device; in other words, changing the logic level of the signal at Dir commands the motor to take a step.

This chopper drive takes advantage of the current sense amplifier on board the LMD18200. The current sense amplifier sources a signal level current that is proportional to the total forward current conducted by the two upper switches of the LMD18200. This *sense* current has a typical value of 377 μA per Amp of load current. A standard ¼W resistor connected between the output of the current sense amplifier (pin #8) and ground converts the sense current into a voltage that is proportional to the load current. This proportional voltage is useful as a feedback signal for control and/or overcurrent protection purposes. The 18 kΩ resistors (*Figure 9*) set the gain of the drive at approximately 0.15A per volt of reference voltage (simply the reciprocal of the product of 377 μA/A and 18 kΩ).

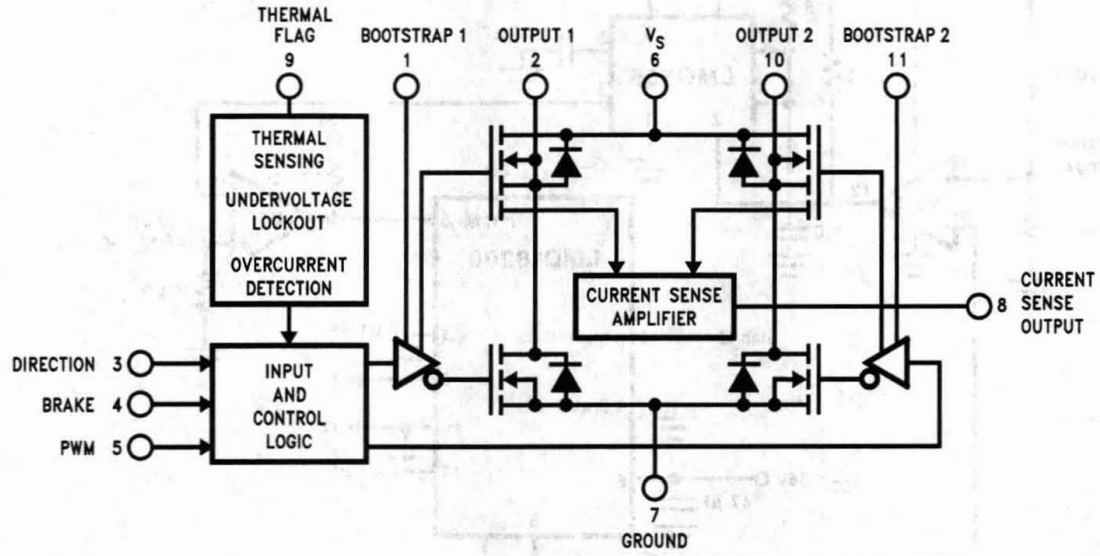

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FIGURE 8. The LMD18200 3A, 55V Full H-Bridge

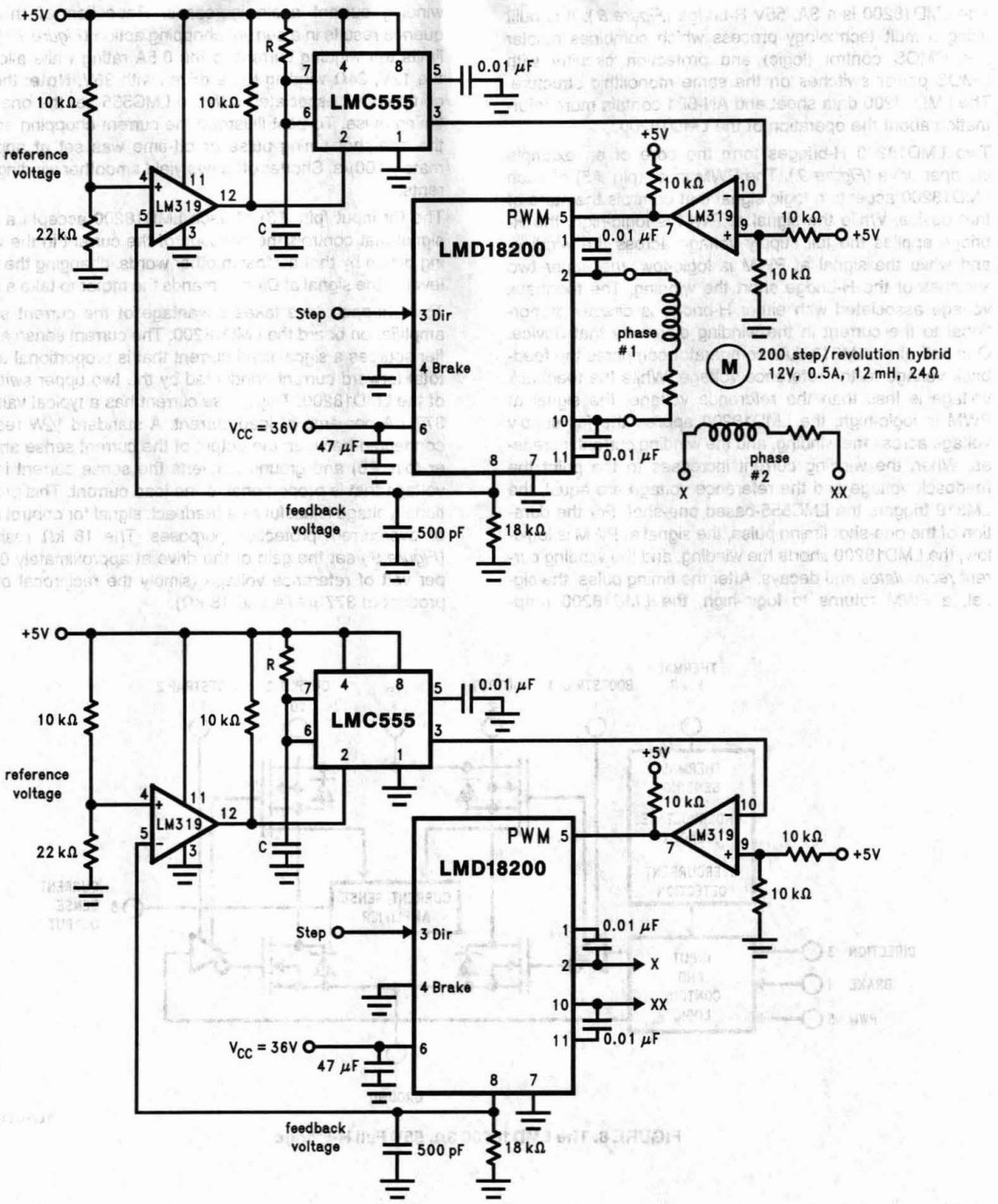

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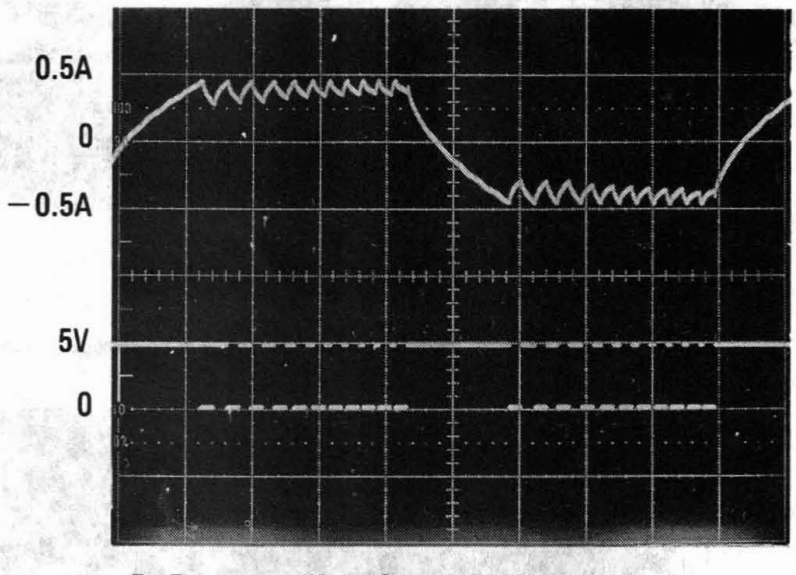
FIGURE 9. An LMD18200-Based Chopper Drive

During the current chopping action, the feedback voltage tracks the winding current (*Figure 11*). When the signal at Dir initiates a change in the direction of the winding current, the feedback voltage ceases tracking the winding current until the winding current passes through zero. This phenomenon occurs because the current sense amplifier only sources a current proportional to the total *forward* current conducted by the two upper switches of the LMD18200. During the period the feedback voltage does not track the winding current, the winding current actually flows from ground to supply as reverse current through a lower and an upper switch of the H-bridge. Only after the winding current passes through zero does it once again become forward current in one of the upper switches (see AN-694). The feedback voltage is ground referenced; thus, it appears the same regardless of the direction of the winding current.

The same 200 step/revolution hybrid stepper (*Figure 9*) was used to generate *Figures 10* through *13*. *Figure 12* shows the winding current for simple voltage drive with $V_{CC} = V_{rated} = 12V$. *Figure 13* shows the winding current for L/4R drive with added series resistance of 72Ω/phase and $V_{CC} = 4V_{rated} = 48V$.



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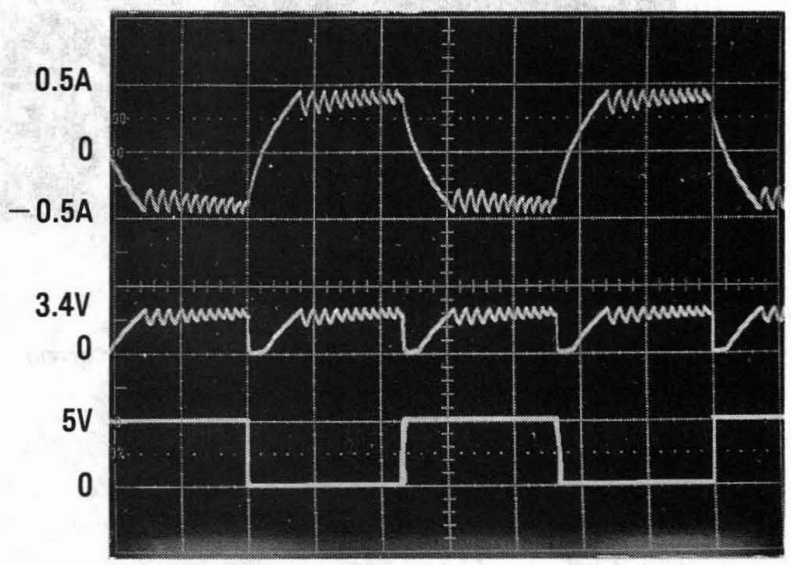
Top Trace: Winding Current at 0.5A/div
Bottom Trace: PWM Signal at 5V/div
Horizontal: 0.5 ms/div

FIGURE 10. The Chopped Winding Current and the Logic Signal at PWM



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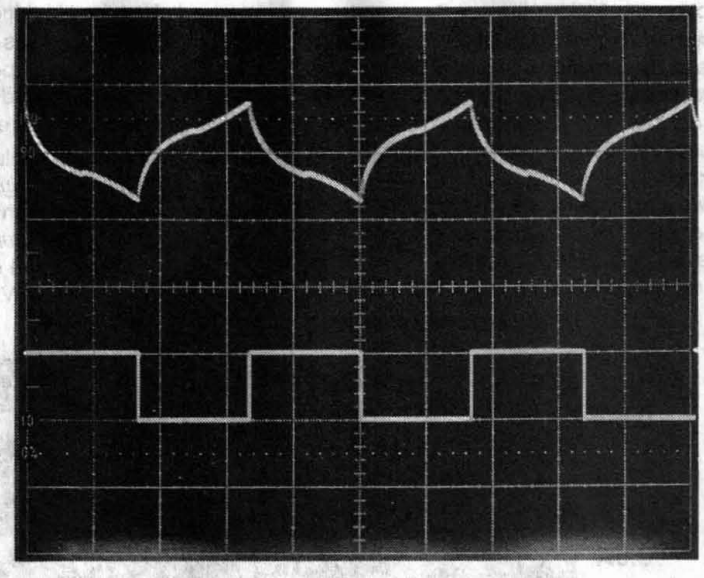
Top Trace: Winding Current at 0.5A/div
Middle Trace: Feedback Voltage at 5V/div
Bottom Trace: Step Logic Signal at 5V/div
Horizontal: 1 ms/div

FIGURE 11. The Chopped Winding Current and Feedback Voltage at 860 Steps/Second



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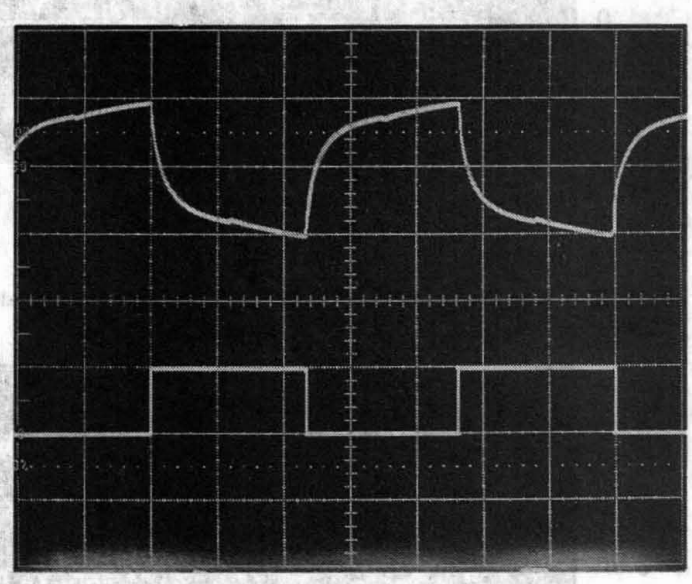
Top Trace: Winding Current at 0.5A/div
Bottom Trace: Step Logic Signal at 5V/div
Horizontal: 2 ms/div

FIGURE 12. The Winding Current for Simple Voltage Drive at 600 Steps/Second



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Top Trace: Winding Current at 0.5A/div
Bottom Trace: Step Logic Signal at 5V/div
Horizontal: 1 ms/div

FIGURE 13. The Winding Current for L/4R Drive at 860 Steps/Second

Development of an Extensive SPICE Macromodel for "Current-Feedback" Amplifiers

National Semiconductor
Application Note 840

ABSTRACT

A current-feedback amplifier macromodel has been developed which simulates the more common small-signal effects such as small-signal transient response and frequency response as well as temperature effects, noise, and power supply rejection ratio. Also modeled are large-signal effects such as non-linear input transfer characteristics and input/output slew rate limiting.

Detailed descriptions of each stage in the model will be presented with examples of model performance and correlation to actual device behavior.

INTRODUCTION

With the increasing complexity and shorter design cycles of today's designs, computer modeling with SPICE (Simulation Program with Integrated Circuit Emphasis) is becoming more popular. This is especially true with high-speed designs utilizing the latest in current-feedback amplifiers. However, an accurate, detailed macromodel for current-feedback amplifiers with good convergence characteristics has not yet been available.

MACROMODELING PHILOSOPHY

The philosophy used in creating this macromodel was a desire to design a model that would simulate the typical behavior of a current-feedback amplifier to within 10% of typical parameters while executing much faster than a device level model. Also, the macromodel would act as a development platform for effects not normally included in other models such as temperature effects, noise, and many of the other second and third order effects that are characteristic in current-feedback amplifiers such as the LM6181.

THE LM6181

National Semiconductor's monolithic current-feedback amplifier, the LM6181, offers the designer an amplifier with the high-performance advantages of current-feedback topology without the high cost associated with hybrid devices. The LM6181 has a bandwidth of 100 MHz, slew rate of 2000 V/μs, settling time of 50 ns (0.1%), and 100 mA of output current drive. A special output stage allows the LM6181 to directly drive a 50Ω or 75Ω back-terminated coax cable. To understand how this device functions, a description of current-feedback amplifiers is in order.

CURRENT-FEEDBACK AMPLIFIERS

Figure 1 shows the block diagram for the current-feedback amplifier. The main difference when compared to voltage-feedback amplifiers (VFA's) is that in the current-feedback topology, a unity gain buffer drives the inverting input. Since this is an inherently low impedance, the feedback error signal is treated as a current rather than a voltage. During input transients, an error current will flow into or out of the input buffer. This current is then mirrored to a current-to-voltage converter (Zt(s)) which consists of a large ($\approx$ 2 MΩ) transimpedance and an output buffer. Since the large transimpedance is analogous to the large voltage gain of VFA's, the output voltage is servo'ed to a value which causes the current through Rf and Rg to cancel the current in the input buffer.

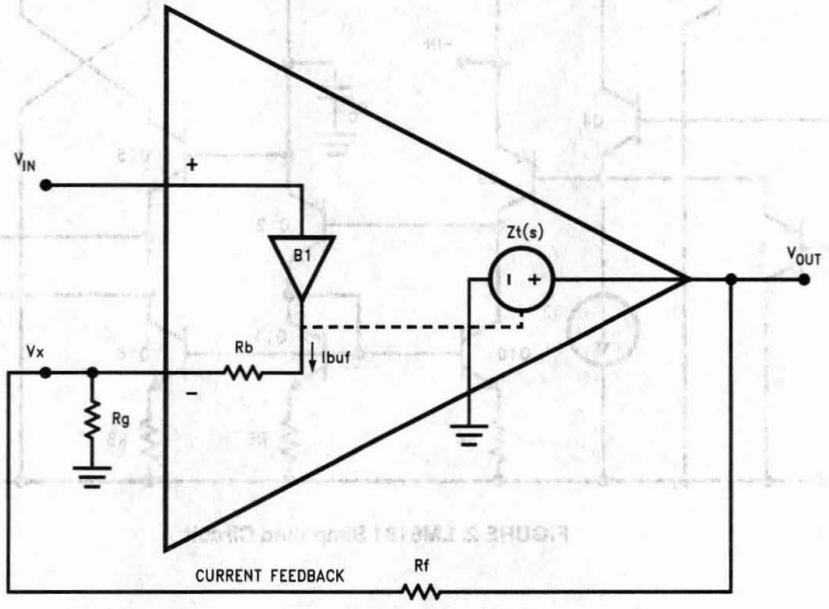

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FIGURE 1. Block Diagram of a Current-Feedback Amplifier

ANALYSIS OF CURRENT-FEEDBACK TOPOLOGY

From the simplified current-feedback amplifier schematic in *Figure 2*, it can be observed that the inverting (−IN) terminal is driven by a unity gain buffer stage. Transistors Q3 and Q4 make up the high-impedance input (+IN) to the buffer while Q5 and Q9 comprise a push-pull stage whose low output impedance is determined by $V_T/(I_CQ5 + I_CQ9) = V_T/(I1 + I2)$ assuming I1 and I2 are equal. The function of the input buffer is to drive the inverting input to the same voltage as the non-inverting input much like a voltage-feedback amplifier does via negative feedback. Transistors Q6, Q7, Q8, Q10, Q11 and Q12 form a pair of Wilson current mirrors which transfer the output current of the input buffer to a high-impedance (Zt) node. The equivalent capacitance (C_C) at this node is charged to the value of the output voltage. This voltage is then conveyed to a second buffer made up of Q14, Q15, Q17 and Q18 which drives the output pin of the amplifier. Short-circuit current limiting is performed by transistors Q19 and Q20. Back on the input of the amplifier, Q1 and Q2 provide a slew rate enhancement effect. For low closed-loop gains and large input steps these transistors turn on and increase the current available to the input buffer. This causes a transient increase in the current available to charge the compensation capacitor via the current mirrors, resulting in a faster slew rate for low gains. Now that the simplified circuit has been described, it will be informative to analyze the block diagram for the model.

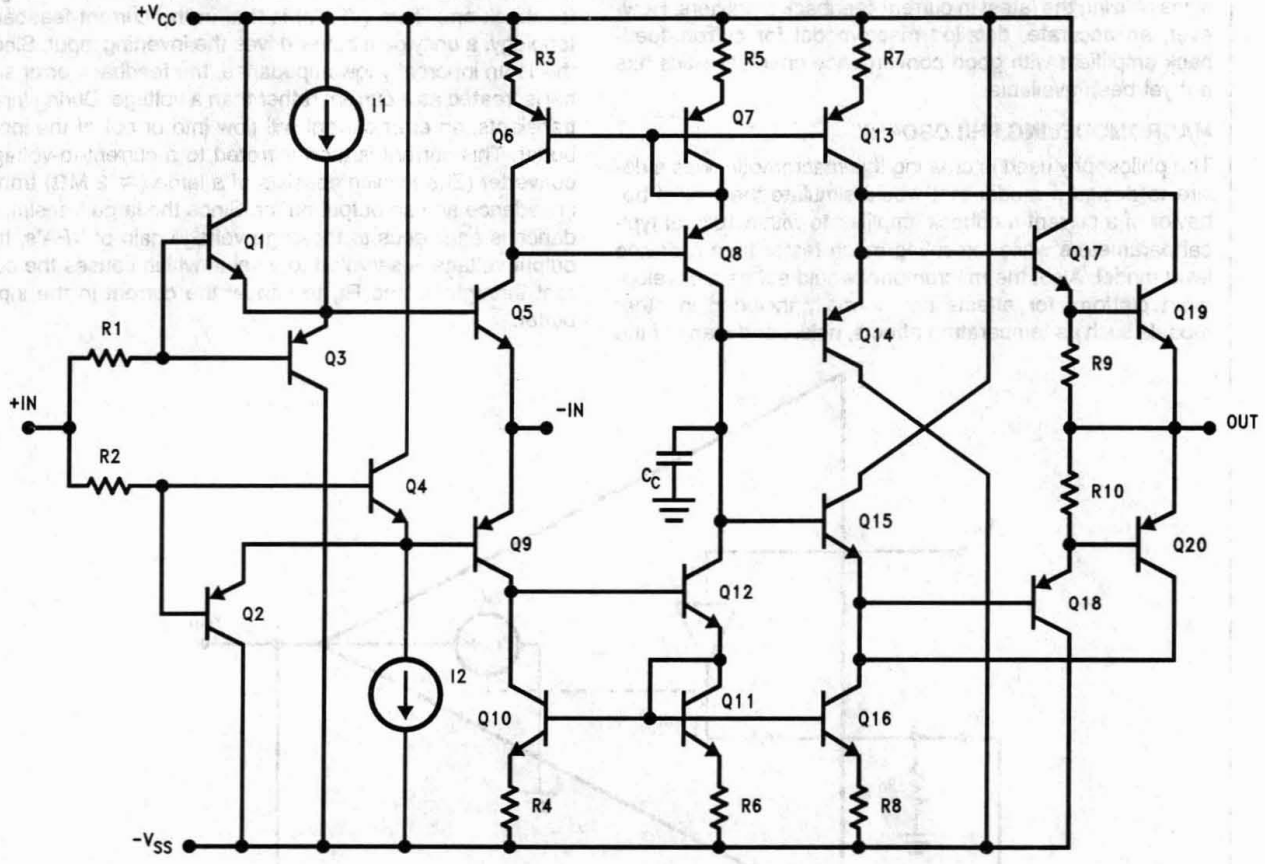
By summing the currents at node Vx in *Figure 1* and using the fact that $V_O = I_{buf} \times Zt(s)$, the transfer function of the non-inverting configuration can be determined to be:

$$\frac{V_o}{V_{in}} = \left(1 + \frac{Rf}{Rg}\right) \times \left[\frac{1}{1 + \dfrac{Rf + \left[1 + \dfrac{Rf}{Rg}\right] \times Rb}{Zt(s)}}\right] \quad (1)$$

where Zt(s) is the open-loop transimpedance as a function of complex frequency. Notice, in equation 1, the 1 + Rf/Rg term on the left is the standard closed-loop voltage gain equation for non-inverting amplifiers while the term on the right is an error term. The 1 + Rf/Rg in the error term is the noise gain of the amplifier and Rb is the input buffer's quiescent output impedance (≈ 30Ω for the LM6181). If Zt(s) is assumed to be large, the error term goes to 1. The closed-loop bandwidth is defined as the frequency at which the magnitude of the error term equals $1/\sqrt{2}$ (−3 dB). If Zt(s) is approximated to be a single pole function, then:

$$Zt(s) = \frac{Zt(dc)}{1 + s \times Zt(dc) \times C_C} \quad (2)$$

where C_C is the value of the internal compensation capacitor in *Figure 2*. By substituting equation 2 for Zt(s) in equa-



TL/H/11488–2

FIGURE 2. LM6181 Simplified Circuit

tion 1 and assuming Zt(dc) is much larger than Rf, the closed-loop bandwidth can now be found to be:

$$bw = \frac{1}{2 \times \pi \times C_C \left[Rf + \left(1 + \frac{Rf}{Rg}\right) \times Rb \right]} \quad (3)$$

If the input buffer output resistance (Rb) times the noise gain of the amplifier (1 + Rf/Rg) is assumed to be small compared to Rf, equation 3 reduces to:

$$bw = \frac{1}{2 \times \pi \times C_C \times Rf} \quad (4)$$

Notice that the ideal closed-loop bandwidth in equation 4 is dependent only on the value of the internal compensation capacitor (C_C) and the feedback impedance (Rf). A recommended value for Rf is usually specified in the manufacturer's datasheet (Rf = 820Ω for the LM6181). Therefore, if the above assumptions are valid, there is theoretically no reduction in bandwidth as Rg is decreased to increase closed-loop gain.

Another special feature of the current-feedback amplifier is the theoretical absence of slew-rate limiting. Since the total output current of the input buffer is available to charge the compensation capacitor (C_C), the slew rate is proportional to the output voltage [4].

$$SR = \frac{I_{buf}}{C_C} = \frac{V_{OUT}}{C_C \times Rf} \quad (5)$$

This simplified analysis is adequate for small closed-loop gains; however, since Rb is typically several tens of ohms, the bandwidth and slew rate will be less than ideal for large gains. Also, there are slew-rate characteristics associated with the input buffer that are dominated by the slew-rate enhancement transistors (Q1 and Q2 in *Figure 2*) and stray package capacitances. All these second order effects are included in the macromodel input stage to achieve accurate simulation results.

THE INPUT STAGE

Figure 3 shows the macromodel input stage which performs many important functions such as the simulation of input buffer output impedance, input/output slew rate, supply voltage dependent input bias current and offset voltage, input capacitance, CMRR and noise [2]. Voltage-controlled current-sources GI1 and GI2 establish the input buffer's output impedance depending on supply voltage. For a given supply voltage, these current-sources can be determined by rearranging the standard bipolar transistor output resistance equation:

$$I1 = I2 = \frac{k \times T}{2 \times q \times Rb} \quad (6)$$

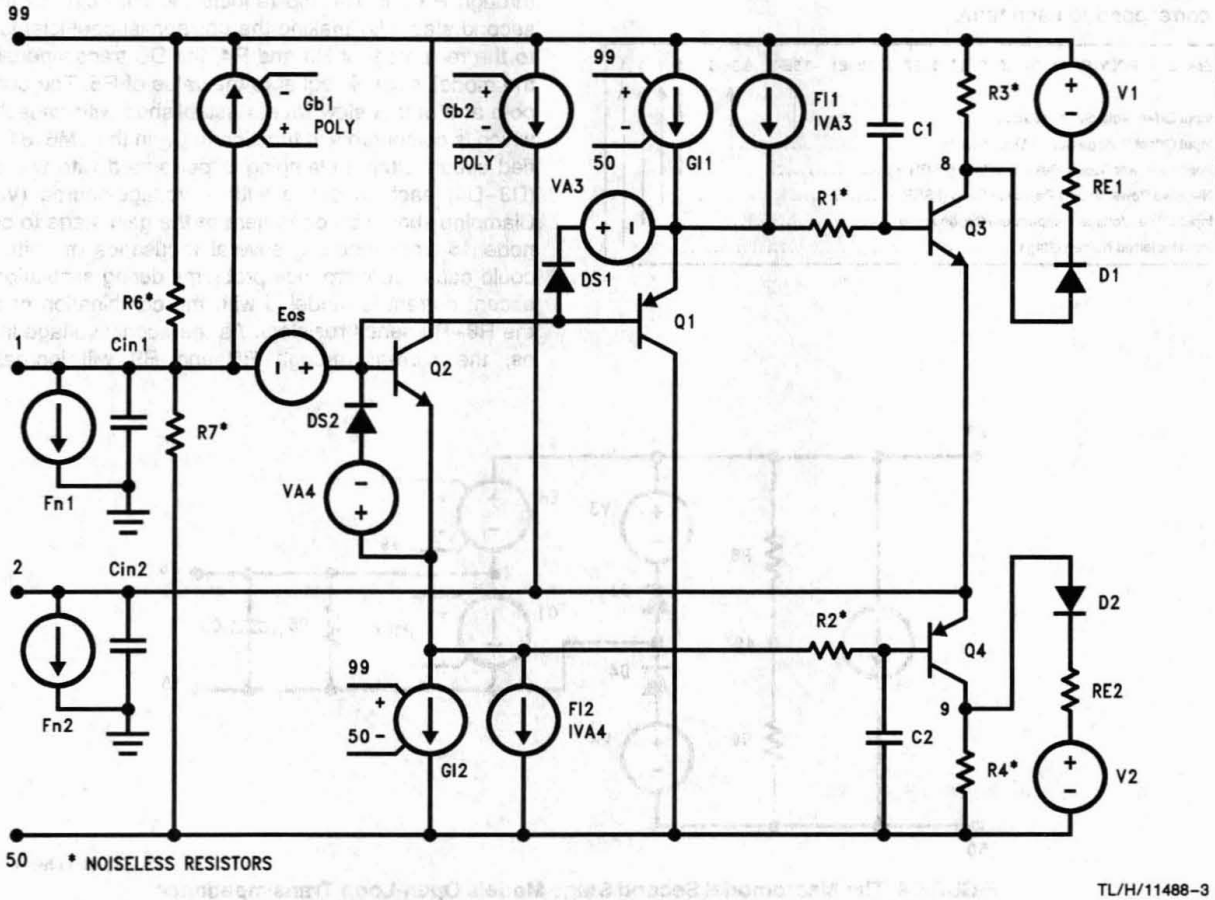


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FIGURE 3. Macromodel Input Stage. Simulates Input Impedances, Input Errors, CMRR, Input/Output Slew Rate, Input Capacitance, and Noise.

Rb is the output impedance of the input buffer and may be approximated with:

$$Rb = \frac{Zt}{A_{VOL}} \quad (7)$$

where A_{VOL} is the differential open-loop voltage gain of the amplifier from input to output. Equation 7 can be derived by shorting Rg and solving the transfer function in Equation 1.

The input stage slew rate is controlled by R1, R2, C1 and C2. The total current available to charge the capacitors C1 and C2 determines the maximum slew rate of the input stage. To reduce the number of PN junctions in the model, the slew rate enhancement transistors were modeled with diodes DS1 and DS2 and current-sources FI1 and FI2.

Input bias currents are simulated with polynomial-controlled current-sources Gb1 and Gb2 which are dependent on both supply voltage and temperature. Current-source Gb2 also models the residual input current (Ib) caused by imbalances in the input buffer as well as the error current caused by the input common mode voltage. The latter is called Inverting Input Bias Current Common Mode Rejection and is designated IbCMR on most datasheets. Fn1 and Fn2 transfer the current from the noise-current sources to the inputs of the amplifier.

The offset voltage-source, Eos, provides a supply voltage dependent input offset voltage and reflects the error voltages from the power supply rejection ratio stage, the thermal effect stage, and the noise-voltage source. Below is a diagram of the Eos polynomial-source and the effects that correspond to each term.

```
Eos 3 1 POLY(5) 99 50 45 0 47 0 57 0 59 61 -2.8E-3 9.3E-5 1 1 1 1
```

Input Offset Voltage Constant
Input Offset Voltage Supply Dependence
Positive Power Supply Rejection Ratio (PSRR+)
Negative Power Supply Rejection Ratio (PSRR−)
Input Offset Voltage Temperature Dependence
Input Referred Noise Voltage

Stray capacitance at the inputs of the amplifier modeled by $C_{in}1$ and $C_{in}2$ has a dramatic effect on the peaking in the amplifier's high frequency response. Common Mode Rejection Ratio can be modeled in the input stage by properly setting the early voltage (Vaf) of the input transistor models. A good starting point for the value of the early voltage is given by:

$$Vaf = \frac{2 \times V_T}{10^{\left[\frac{CMRR(db)}{20}\right]}} \quad (8)$$

Also, in the transistor model, a value for beta (BF) should be chosen. It should be large enough so that the base currents do not interfere with the input bias currents of the model, but not so large as to cause convergence problems during simulation.

The output of the input stage is the sum of the currents flowing through R3 and R4. The voltage across R3 and R4 is softly clamped by the V1, RE1, D1 and V2, RE2, D2 strings respectively. This effectively limits the current to the second stage yet still allows the second stage slew rate to increase for large input signals.

THE SECOND STAGE

The second stage of the macromodel *(Figure 4)* provides the open-loop transimpedance, the first pole, output clamping and supply dependent quiescent supply current. The voltage-controlled current-source G1 is controlled by a second order polynomial equation which calculates the current through R3 and R4 and reflects the sum directly into the second stage. By making the polynomial coefficients equal to the reciprocal of R3 and R4, the DC transimpedance of the model is simply equal to the value of R5. The dominant pole and output slew rate is established with capacitor C3 which is comparable in function to C_C in the LM6181 simplified circuit. Output clamping is performed with two diodes (D3–D4) each in series with a voltage-source (V3–V4). Clamping should be done here at the gain stage to prevent node 15 from reaching several thousands of volts which could cause convergence problems during simulation. Quiescent current is modeled with the combination of I3 and the R8–R9 series resistors. As the supply voltage increases, the current through R8 and R9 will increase ef-

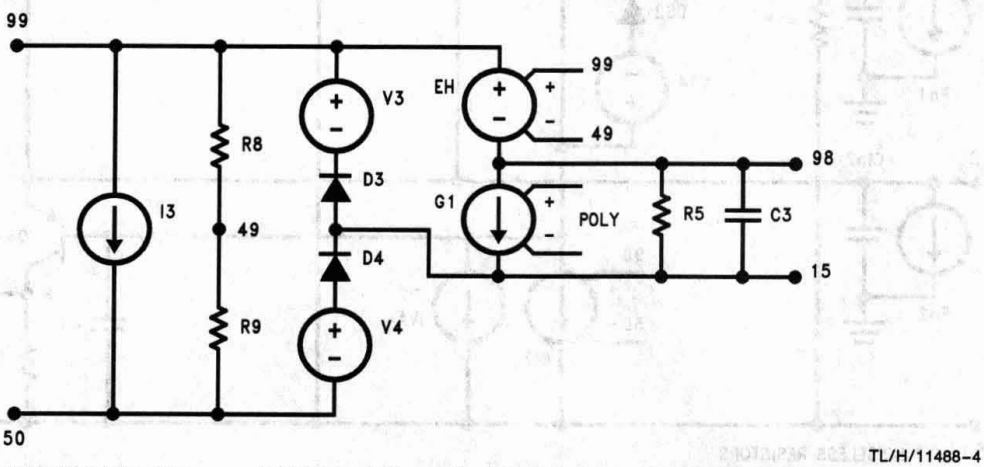

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FIGURE 4. The Macromodel Second Stage Models Open-Loop Transimpedance, First Pole, Output Swing Limiting, and Quiescent Supply Current.

fectively simulating that behavior in the real device. The value for resistors R8 and R9 can be calculated by dividing the change in supply voltage by the change in supply current ($\Delta V_S/\Delta I_S$) anywhere within the operating range of the amplifier. Current-source I3 is evaluated by taking the total supply current at a given voltage and subtracting off the current through all other significant supply loads. These loads are R8, GI1, GI2, and R3 so that:

$$I3 = Ivs\ @\ 15V - \frac{15}{R8} - 3 \times I1 \quad (9)$$

The $3 \times I1$ comes from the fact that the currents through GI1, GI2 and R3 are equal. Resistors R8 and R9 also act as a voltage divider and establish a common-mode voltage (V_H) for the model directly between the rails. If the supply rails are symmetrical, i.e., ±15V, node 49 will be at zero volts. Voltage-controlled voltage-source EH measures the voltage across R8 and subtracts an equal voltage from the positive supply rail to provide a stiff point between the rails (node 98) to which many other stages in the model are referenced.

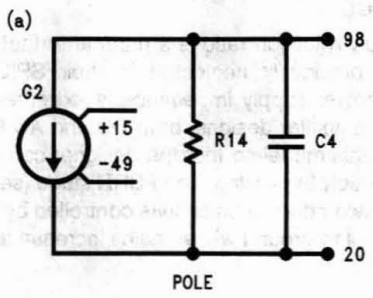
FREQUENCY-SHAPING STAGES

In keeping with the philosophy of providing a macromodel that is as accurate as possible, it has been determined that the model must be capable of easily accommodating as many poles and zeros that are necessary to precisely shape the magnitude and phase response of the model [5]. This is accomplished with telescopic frequency-shaping stages that each have unity DC gain making it easier to add poles and zeros without changing the DC gain of the model. The LM6181 macromodel has four high frequency pole stages and no zero stages, however, each of the three types of frequency-shaping stages will be discussed in detail should the reader wish to develop macromodels for other amplifiers.

The first type of frequency-shaping stage is a pole. In *Figure 5a*, resistor R14 is set to 1 kΩ. This value is chosen to reduce the thermal noise associated with this resistor and to simplify the calculations for the other components in the stage. Current-source G2 is controlled by the output voltage from the previous stage and its g_m is set to the reciprocal of R14 or 10^{-3} to maintain unity DC gain of the stage. Capacitor C4 rolls off the gain at high frequencies and is set with the standard pole equation: $C = 1/(2 \times \pi \times f_P \times R)$ where f_P is the −3 dB frequency of the pole in Hz.

Even though SPICE will attempt to process a bare zero stage, in the real world, such a circuit is actually non-causal and SPICE may not converge because an ideal inductor can generate an infinite voltage if the current though it changes instantaneously. To introduce a zero in the frequency response of the model, a pole must be combined with the zero to form a zero/pole or a pole/zero stage. The circuit for the zero/pole stage is shown in *Figure 5b*. This stage will have unity DC gain if the g_m of G5 is set to the reciprocal of R19. As the frequency increases, L1's impedance starts to increase until R18 dominates causing the gain to level off.

The last type of frequency-shaping stage is the pole/zero circuit shown in *Figure 5c*. As the frequency increases, the gain starts at unity and decreases until the impedance of the capacitor is negligible compared to its series resistor. For more information on poles and zeros, see references [7] and [8].



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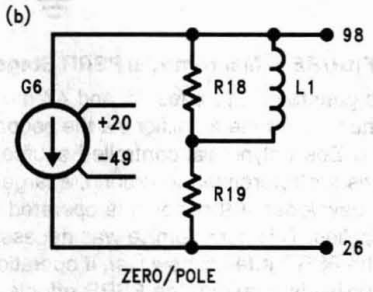
$$R14 = 1\ k\Omega$$

$$G2 = \frac{1}{R14} = 10^{-3}$$

$$C4 = \frac{1}{2 \times \pi \times f_P \times R14}$$



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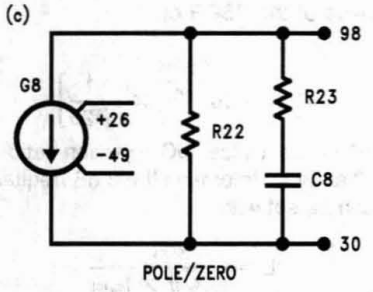
$$R19 = 1\ k\Omega$$

$$G6 = \frac{1}{R19} = 10^{-3}$$

$$R18 = \left(\frac{f_p}{f_z} - 1\right) \times R19$$

$$L1 = \frac{R18}{2 \times \pi \times f_P}$$



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$$R22 = 1\ k\Omega$$

$$G8 = \frac{1}{R22} = 10^{-3}$$

$$R23 = \frac{R22}{\frac{f_z}{f_p} - 1}$$

$$C8 = \frac{1}{2 \times \pi \times f_z \times R2}$$

FIGURE 5. Macromodel Frequency-Shaping Stages

PSRR STAGE

Power supply rejection ratio is a parameter that many vendors have previously neglected in their SPICE models. Since AC power supply impedance is extremely critical in high-speed amplifier designs, both DC and AC PSRR were included in this model so that the designer can explore the effects of supply bypassing. The PSRR stage (see *Figure 6*) consists of two attenuation circuits controlled by the voltage from each rail to ground whose gains increase at 20 dB per decade.

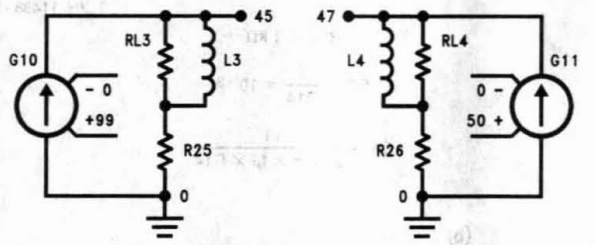

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FIGURE 6. Macromodel PSRR Stage

The signals generated at nodes 45 and 47 are directly reflected to the input of the amplifier via the second and third terms of the Eos polynomial-controlled source. Since the PSRR stages are referenced to ground, a large offset voltage will be developed if the model is operated from asymmetrical supplies. This compromise was necessary in order to include the PSRR effects; however, if operation on asymmetrical supplies is required, the PSRR effects can be disabled by changing the second and third polynomial terms in Eos from 1 to 0. For example, change:

```
Eos 3  1 POLY(5)  99  50  45  0  47  0  57  0  59  61  −2.8E-3  9.3E-5  1  1  1  1
```

to:

```
Eos 3  1 POLY(5)  99  50  45  0  47  0  57  0  59  61  −2.8E-3  9.3E-5  0  0  1  1
```

To set the component values in the PSRR stages, R25 and R26 are arbitrarily chosen to be 10Ω The g_m's of the current sources are set so that the DC gain of each stage is equal to the DC value of the PSRR or:

$$G10 = 10^{\frac{PSRR}{20}} \times \left[\frac{1}{R25}\right] \quad (10)$$

where PSRR is the typical DC rejection ratio in dB. The inductors, L3 and L4, determine the 3 dB frequency of each stage and can be set with:

$$L = \frac{R}{2 \times \pi \times f_{3dB}} \quad (11)$$

Resistors RL3 and RL4 cancel the zeros associated with the inductors at a frequency above the unity gain frequency of the amplifier. This helps with transient convergence when simulating inductive or resistive power supply lines.

THERMAL EFFECTS

The predominant thermal effects of a current-feedback amplifier are the change in offset voltage and input bias current as a function of temperature. The macromodel stages in *Figure 7* are used to simulate these effects by utilizing the SPICE temperature dependent resistor model which is controlled with the equation [9]:

$$R(\Omega) = \langle value \rangle \times (1 + TC1 \times (T - Tnom) + TC2 \times (T - Tnom)^2) \quad (12)$$

where <value> is the value of the resistor at Tnom (usually 27°C), T is the temperature in °C, TC1 is the linear temperature coefficient, and TC2 is the quadratic temperature coefficient. The equation will fit a quadratic curve through three points in a temperature graph by solving three equations with three unknowns. Since SPICE will give an error message if a resistor goes negative at any temperature, an offset bias is added to the resistor value whose voltage is then subtracted from the respective input error source (Gb1, Gb2, or Eos).

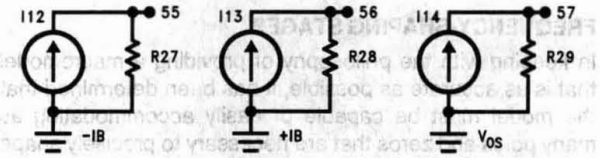

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FIGURE 7. Macromodel Thermal Effect Stages

The voltages generated at nodes 55, 56, and 57 are scaled and used to control the input error sources Gb2, Gb1, and Eos respectively. The simulated results compare quite closely to the typical curves for the actual device as can be seen in *Figures 16* and *17*.

NOISE STAGES

The addition of noise effects to any macromodel is similar to the techniques used for input offset voltage and drift. The total amplifier noise is lumped together and referred to the input of the model. Before noise sources are added, however, the model has to be rendered essentially noiseless. This is easier than it sounds, though, because noise adds vectorially. The total contribution of several noise sources can be found by:

$$En_{total} = \sqrt{(En1)^2 + (En2)^2 + (En3)^2 \ldots}$$

So, a latent noise source within the model will have to be reduced to only ¼ of the desired noise level to maintain an accuracy of less than 3% ($\sqrt{1 + 0.25^2} = 1.03$). Most of the latent amplifier model noise comes from thermal noise generated by large-value resistors commonly used in macromodels. To reduce this noise, the resistor values are scaled so their thermal noise is negligible compared to the desired noise of the amplifier. If resistor scaling is not possible, as was the case with several resistors in the input stage of the LM6181 macromodel, a *noiseless resistor* can be used. A noiseless resistor is created by utilizing a voltage-controlled current-source (G device) with the same input and output terminals whose g_m is set to the reciprocal of the required value of resistance (see *Figure 3* and the LM6181 netlist). The only caveat with using noiseless resistors is that a current-source is considered an open circuit when SPICE calculates the initial bias point of the circuit. Therefore, at least one other device must be connected to the nodes of the noiseless resistor to avoid "floating node" errors.

Now that the macromodel is rendered essentially noiseless, lumped noise sources can be added and referred to the input sources. *Figure 8* shows the equivalent noise model which consists of an ideal noiseless amplifier, two noise-current generators (i_{n+} and i_{n-}), from each input to ground and a noise-voltage generator (e_n) in series with non-inverting input.

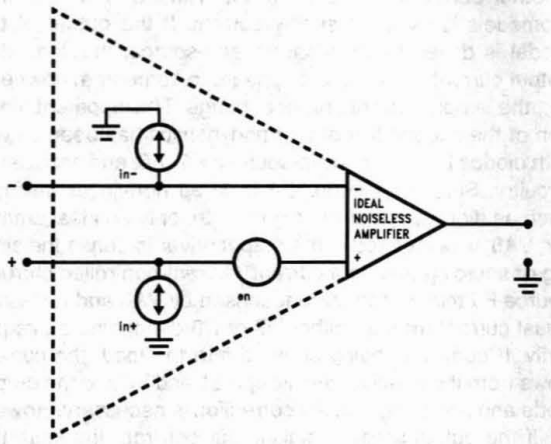

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FIGURE 8. Equivalent Amplifier Noise Model

The noise-current generators are called Fn1 and Fn2 in the macromodel input stage *(Figure 3)*, while the noise-voltage generator is included in the Eos polynomial-controlled source. The noise voltage or current which is actually referred to the input generators comes from separate noise source stages in the macromodel.

The noise-voltage circuit *(Figure 9)* generates both 1/f and white noise by using a 0.1V voltage-source which lightly biases a diode-resistor series combination. White noise is simply the thermal noise-current generated in the resistor which follows the spectral power density (per unit bandwidth) equation below:

$$i_n^2 = \frac{4 \times k \times T}{\text{Resistance}} \qquad (14)$$

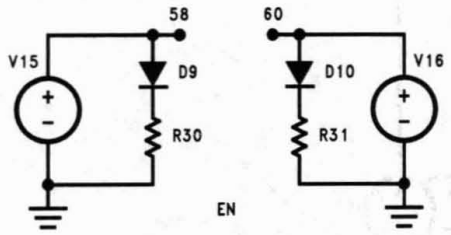

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FIGURE 9. Macromodel Noise Voltage Stage

where i_n is the noise-current through the resistor, k is Boltzmann's constant (1.381×10^{-23}), and T is the temperature in °K (°C + 273.2°). By taking the square root of both sides of the equation and multiplying by resistance, the required value of resistance can be found for a given noise-voltage spectral density with:

$$R = \frac{e_n^2}{2 \times 4 \times k \times T} \qquad (15)$$

where e_n is the white noise voltage of the amplifier per $\sqrt{\text{Hz}}$. The "2" in the denominator comes from the fact that the voltage is taken differentially across two identical circuits of the noise-voltage source (nodes 58 and 60). The reason for using two identical circuits is so that a DC voltage would not be created which would be seen as an offset voltage on the input.

Flicker noise or 1/f noise-voltage comes from the SPICE diode model. By setting the flicker noise exponent (AF) to 1 and properly setting the flicker noise coefficient (KF), the resulting noise voltage will accurately simulate the 1/f noise-voltage spectral density with the correct "corner frequency". Equation 16 shows the noise-current that results from the SPICE diode model where Id is the DC diode current and the $2 \times q \times Id$ term is negligible compared to the 1/f noise of the amplifier.

$$i_n^2 = 2 \times q \times Id + KF \times \frac{Id^{AF}}{\text{FREQUENCY}} \qquad (16)$$

To determine the value for KF in the macromodel, the following equation can be used:

$$KF = \frac{Ea^2}{R^2 \times Id \times 2} \qquad (17)$$

where Ea is the noise-voltage spectral density of the amplifier at 1 Hz and Id is the DC current through the diode which can be determined with the standard Schottky diode equation. Again, the "2" in the denominator comes from the fact that the noise output is taken differentially across two identical circuits.

The white portion of the amplifier's noise current is modeled by utilizing the thermal noise current of a resistor in series with a zero volt voltage-source (see *Figure 10*).

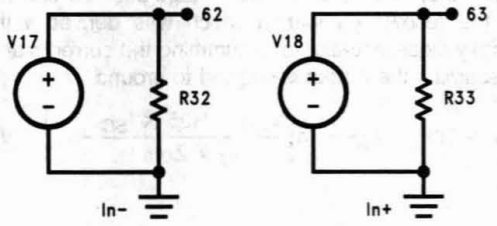

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FIGURE 10. Macromodel White Noise-Current Generators

Since the noise-current through each of the resistors is measured with the voltage-sources and directly referred to the respective current-controlled current-source on the input, the value for each resistor can be found by rearranging Equation 14 or:

$$R = \frac{4 \times k \times T}{i_n^2} \qquad (18)$$

The i_n term is the broad-band or white noise-current spectral density at the respective input of the amplifier.

To simulate the 1/f component of the noise-current, the flicker noise coefficient (KF) in the model for each pair of input transistors is set to obtain the correct corner frequency. In the LM6181 macromodel, KF is set to 4.13×10^{-13} for Q1 and Q2 while KF is set to 6.7×10^{-14} for Q3 and Q4. The flicker noise exponent (AF) is left at its default value of 1.

The macromodel's noise curves are compared to the actual amplifier's curves in *Figures 18* through *21*. The simulation results are quite close to the actual noise characteristics of the amplifier. For more information on calculating and modeling amplifier noise, see references [3] and [9].

OUTPUT STAGE

After the input signal is amplified and frequency shaped, it is further processed by the output stage shown in *Figure 11*. The output stage performs three important functions, namely, simulation of output impedance, short-circuit current limiting, and dynamic supply current.

The intermediate output signal appears at the output of the last frequency-shaping stage as a high-source-impedance voltage referenced to V_H. Voltage-controlled voltage-source, E1, level shifts the intermediate output signal down from the positive rail and provides the output drive for the model. Output impedance is modeled with the combination of R35 and L5. Resistor R35 simulates the DC output impedance which determines the behavior of the model when driving heavy loads. Additionally, inductor L5 models the characteristic rise in output impedance as a function of frequency which is common to the emitter-follower output stage found in many amplifiers. Since an ideal inductor as modeled by SPICE has infinite Q, a bare inductor in the signal path can cause convergence problems if the current through it can change instantaneously. To lower the Q of the inductor and prevent convergence problems during simulation, a large value resistor, RL5, is placed across L5. Capacitor CF1 models stray capacitance across the feedback resistor which dramatically affects the high frequency response of the amplifier.

Short-circuit current limiting is also a necessary feature of any good amplifier macromodel. The diodes D5 and D6 each in series with a voltage-source V5 and V6 accomplish this function by effectively clamping the maximum voltage across R35. The value of the voltage-sources can be set with the following equation which was derived with the Schottky diode equation and summing the currents at node 40 assuming the output is shorted to ground.

$$V = R35 \times I_{SC} - \ln\left[\frac{V_{CC} - R35 \times I_{SC}}{I_S \times Zofr} + 1\right] \times V_T \quad (19)$$

The term Zofr is the output impedance of the last frequency shaping stage (1 kΩ in this case), I_S is the saturation current of the diode, and V_T is the thermal voltage $k \times T/q$. Although it appears that the appropriate parameters are included in the equation, no attempt was made to model the dependence of short-circuit current on supply voltage or temperature.

Another behavior that is often not included in op-amp macromodels is dynamic supply current. If the output of the model is driven by an ideal voltage-source, the simulated output current of the model appears to come from nowhere, i.e., the supply currents do not change. This apparent violation of the second law of thermodynamics has been solved with diodes D7–D8, current-sources F5–F6, and associated circuitry. Since it is important to keep non-linear devices, such as diodes, out of the signal path, only an ideal ammeter, VA8, was inserted in the output driver to sense the sinking or sourcing of output current. Current-controlled current-source F5 mirrors the current sensed by VA8 and forces an equal current through either D7 or D8 depending on its polarity. If current is being sourced into the load, the current flows from the positive rail through E1 and VA8 to the output node and no supply current correction is necessary. However, if the output stage is sinking current from the load, the current flows from the output node up through VA8 and E1 into the positive rail. To compensate for this, F5 forces an equal current through D7 and ammeter VA7. This current is then mirrored to current-source F6 which pulls an equal amount of current out of the positive rail and forces it into the negative rail. Therefore, if the output stage is sourcing current, it appears to come from the positive rail, whereas current that is sinking from the load appears to go into the negative rail. The net result of all these extra devices is an output stage which closely models the behavior of the real amplifier.

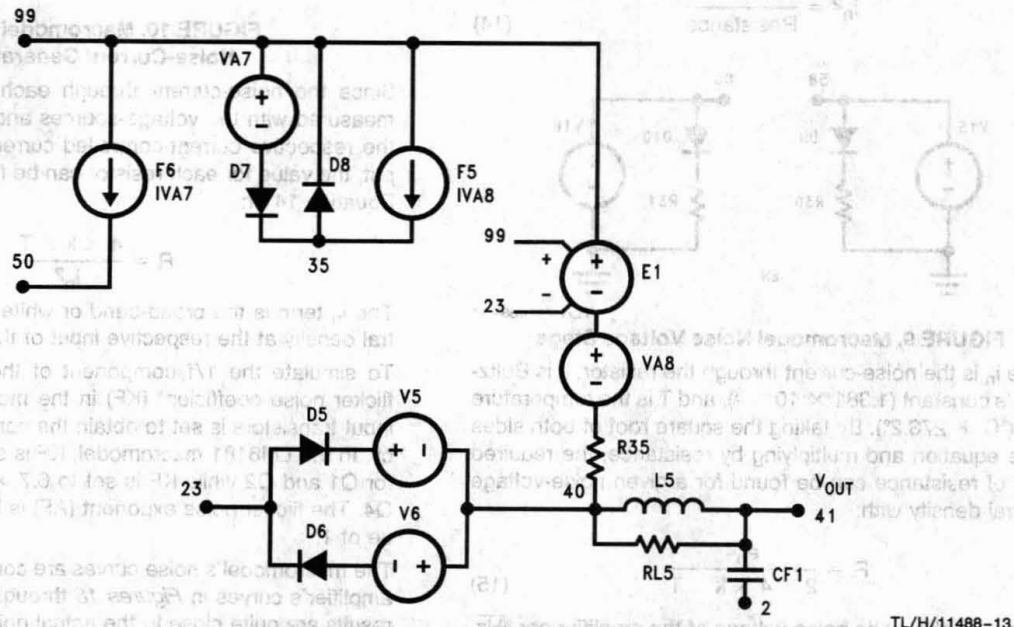

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FIGURE 11. Macromodel Output Stage

LM6181 Macromodel Netlist

```
*****************************************
*LM6181 CURRENT FEEDBACK OP-AMP MACRO-MODEL
*****************************************
*
*connections:      non-inverting input
*                  |  inverting input
*                  |  |  positive power supply
*                  |  |  |  negative power supply
*                  |  |  |  |  output
*                  |  |  |  |  |
*                  |  |  |  |  |
.SUBCKT LM6181     1  2  99 50 41
*
*Features:              (TYP.)
*High bandwidth =       100 MHz
*High slew rate =       2000 V/µs
*Current Feedback Topology
*NOTE: Due to the addition of PSRR effects, model must be operated
*      with symmetrical supply voltages. To avoid this limitation
*      and disable the PSRR effects, see Eos below.
*
********** INPUT STAGE **********
*
GI1 99  5 POLY(1) 99 50 243.75U 2.708E-6
GI2  4 50 POLY(1) 99 50 243.75U 2.708E-6
FI1 99  5 VA3 100
FI2  4 50 VA4 100
Q1 50 3 5 QPN
Q2 99 3 4 QNN
GR1  5 6 5 6 2.38E-4
*^4.2K noiseless resistor
C1  6 99 .468P
GR2 4 7 4 7 2.38E-4
*^4.2K noiseless resistor
C2  7 50 .468P
GR3 99 8 99 8 1.58E-3
*^633ohm noiseless resistor
V1 99 10 .3
RE1 10 30 130
D1 30 8 DX
GR4 50  9 50 9 1.58E-3
*^633ohm noiseless resistor
V2  11 50 .3
RE2 11 31 150
D2  9 31 DX
Q3  8 6 2 QNI
Q4  9 7 2 QPI
DS1 3 12 DY
VA3 12 5 0
DS2 13 3 DY
VA4 4 13 0
GR6 1 99 1 99 5E-8
*^20MEG noiseless resistor
GR7  1 50 1 50 5E-8
*^20MEG noiseless resistor
GB1  1 99 POLY(2) 99 50 56 0 -1.2E-6 4E-8 1E-3
FN1  1  0 V18 1
GB2 99  2 POLY(3) 99 50 1 49 55 0 18.5E-6 -1.5E-7 -1E-7 -1E-6
FN2  2  0 V17 1
EOS 3  1 POLY(5) 99 50 45 0 47 0 57 0 59 61 -2.8E-3 9.3E-5 1 1 1 1
*To run on asymmetrical supplies, change to 0..... ^ ^
```

```
CIN1 1  0 2P
CIN2 2  0 5.75P
*
******** SECOND STAGE **********
*
I3 99 50 4.47M
R8 99 49 7.19K
R9 49 50 7.19K
V3 99 16 1.7
D3 15 16 DX
D4 17 15 DX
V4 17 50 2.0
EH 99 98 99 49 1
G1 98 15 POLY(2) 99 8 50 9 0 1.58E-3 1.58E-3
*Fp1 = 27.96 KHz
R5 98 15 2.372MEG
C3 98 15 2.4P
*
********* POLE STAGE ***********
*
*Fp = 250 MHz
G2 98 20 15 49 1E-3
R14 98 20 1K
C4 98 20 .692P
*
********* POLE STAGE ***********
*
*Fp = 250 MHz
G3 98 21 20 49 1E-3
R15 98 21 1K
C5 98 21 .692P
*
********* POLE STAGE ***********
*
*Fp = 275 MHz
G4 98 22 21 49 1E-3
R16 98 22 1K
C6 98 22 .5787P
*
********* POLE STAGE ***********
*
*Fp = 500 MHz
G5 98 23 22 49 1E-3
R17 98 23 1K
C7 98 23 .3183P
*
********* PSRR STAGE ***********
*
G10 0 45 99 0 1.413E-4
L3 44 45 26.53U
R25 44  0 10
RL3 44 45 10K
G11  0 47 50 0 1.413E-4
L4  46 47 2.27364U
R26 46  0 10
RL4 46 47 10K
```

```
*
******** THERMAL EFFECTS **********
*
I12  0 55 1
R27  0 55 10 TC = 3.453E-3 7.93E-5
I13  0 56 1E-3
R28  0 56 1.5 TC = 9.303E-4 8.075E-5
I14  0 57 1E-3
R29  0 57 3.34 TC = 3.111E-3
*
********* NOISE SOURCES ***********
*
V15 58  0 .1
D9  58 59 DN
R30 59  0 726.4
V16 60  0 .1
D10 60 61 DN
R31 61  0 726.4
V17 62  0 0
R32 62  0 73.6
V18 63  0 0
R33 63  0 1840
*
********* OUTPUT STAGE ***********
*
F6 99 50 VA7 1
F5 99 35 VA8 1
D7 36 35 DX
VA7 99 36 0
D8 35 99 DX
E1 99 37 99 23 1
VA8 37 38 0
R35 38 40 50
V5 33 40 5.3V
D5 23 33 DX
V6 40 34 5.3V
D6 34 23 DX
CF1 41 2 2.1P
L5 40 41 31N
RL5 40 41 100K
*
********* MODELS USED ***********
*
.MODEL QNI NPN(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 6.7E-14)
.MODEL QPI PNP(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 6.7E-14)
.MODEL QNN NPN(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 4.13E-13)
.MODEL QPN PNP(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 4.13E-13)
.MODEL DX D(IS = 1E-15)
.MODEL DY D(IS = 1E-17)
.MODEL DN D(KF = 1.667E-9 AF = 1 XTI = 0 EG = .3)
.ENDS
```

SIMULATION ACCURACY

The real test of a macromodel is how the simulation results compare with the real-world device. The table below shows some of the amplifier parameters and how the simulation compares to actual device behavior. As can be seen, the goal of a 10% match between the model and the actual device was achieved.

A good figure of merit for a macromodel is the accuracy of its small-signal transient response. *Figures 14* and *15* show the small-signal response of the real LM6181 and the simulation output. Notice that the simulated over-shoot and frequency of ringing closely match that of the actual device. This is due to the accurate modeling of the frequency response and output impedance capabilities of the model.

CONCLUSION

A truly comprehensive SPICE compatible macromodel for current-feedback amplifiers has been developed. The macromodel includes effects such as accurate input transfer response, accurate AC response, temperature effects, DC and AC PSRR, and noise. Even with the addition of all these features, the macromodel's simulation speed is still more than twice as fast as a device level micromodel. The speed advantage of this macromodel mainly comes from the fact that it converges extremely well. Since careful attention was paid to convergence during the development of the model, there is no difficulty establishing a bias point or dealing with large input signals. With detailed and accurate vendor supplied macromodels such as the one described in this paper, the designer can easily verify the effects of strays and amplifier limitations in his circuit.

Parameter	Typical Value	Simulation Results	% Error
$Z_{t(dc)}$ $Rl = 1\ k\Omega$	127 dBΩ	126.6 dBΩ	4.5%
$BW_{3\ dB}$ $A_V = -1$ $Rl = 1\ k\Omega$	100 MHz	103.9 MHz	3.9%
I_{B+}	1.5 μA	1.5 μA	0.0%
I_{B-}	−4.0 μA	−4.0 μA	0.0%
V_{OS}	−3.34 mV	−3.3 mV	1.2%
Isupp	7.5 mA	7.7 mA	2.7%
Pulse Resp. Overshoot	35%	34.8%	0.6%
Slew Rate $V_{IN} = \pm 10V$	1400 V/μs	1468 V/μs	4.8%
I_{SC}	130 mA	136.8 mA	5.2%
e_n	5 nV/√Hz	4.9 nV/√Hz	2.0%
i_{n+}	3 pA/√Hz	2.96 pA/√Hz	1.3%
i_{n-}	16 pA/√Hz	15.1 pA/√Hz	5.6%

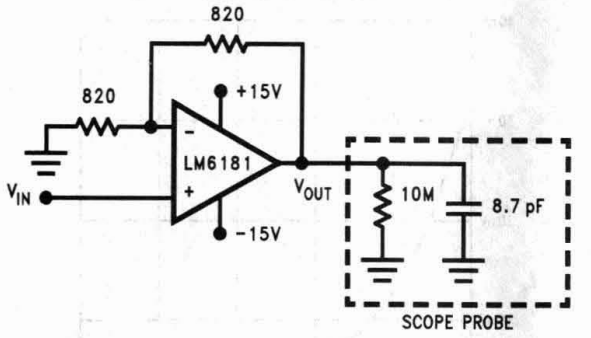

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FIGURE 12. Non-inverting amplifier. $A_V = +2$. It is very important to include a model of the scope probe on the output of the amplifier to obtain reasonable results from the simulation.

```
*LM6181 Small-Signal Response. Av = +2.
*Rf = Rg = 820ohm.
*
XAR1 3 2 7 4 6 LM6181
VP  7 0  15V
VN  4 0 -15V
VIN 3 0 PULSE (-.2V .2V 40N .2N .2N)
RF  6 2 820ohm
RI  2 0 820ohm
RL  6 0 10MEG
CL  6 0 8.7pF
.LIB CF.LIB
.OPTIONS RELTOL = .0001 CHGTOL = 1E-20
.TRAN/OP .1N 200N
.PROBE
.END
```

FIGURE 13. Non-Inverting Amplifier Netlist [9]

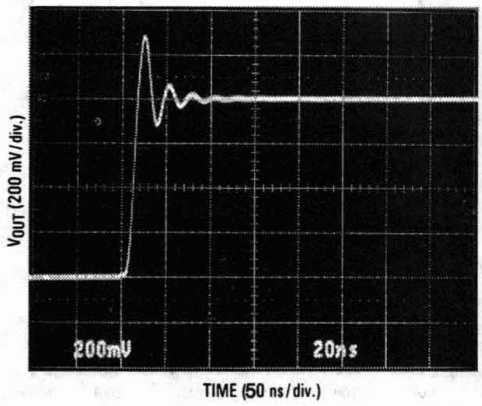

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FIGURE 14. LM6181 Small-Signal Transient Response

LM6181 Small-Signal Response
$A_V = +2$
$Rf = Rg = 820\Omega$

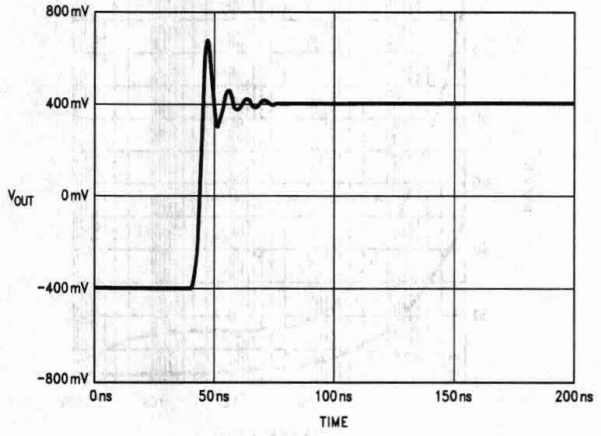

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FIGURE 15. LM6181 Simulated Transient Response

LM6181
V_{OS}, $+I_B$, $-I_B$ vs Temperature

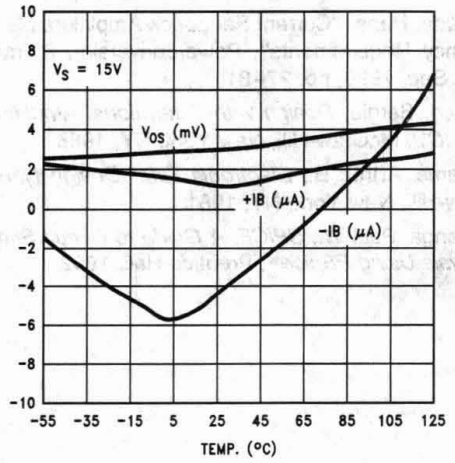

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FIGURE 16. LM6181 Temperature Effects

LM6181 V_{OS}, $+I_B$, $-I_B$

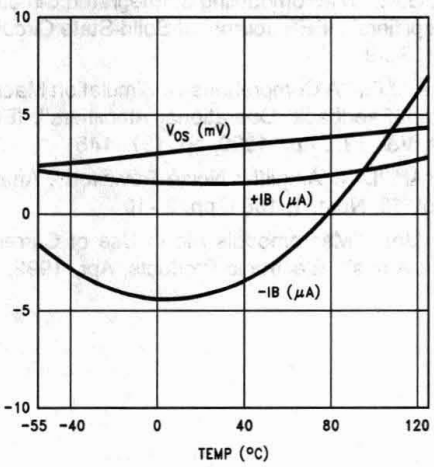

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FIGURE 17. LM6181 Simulated Temperature Effects

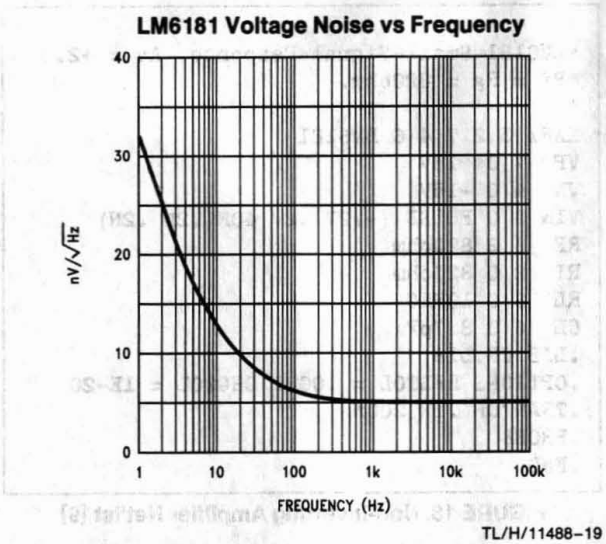

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FIGURE 18. LM6181 Voltage-Noise Response

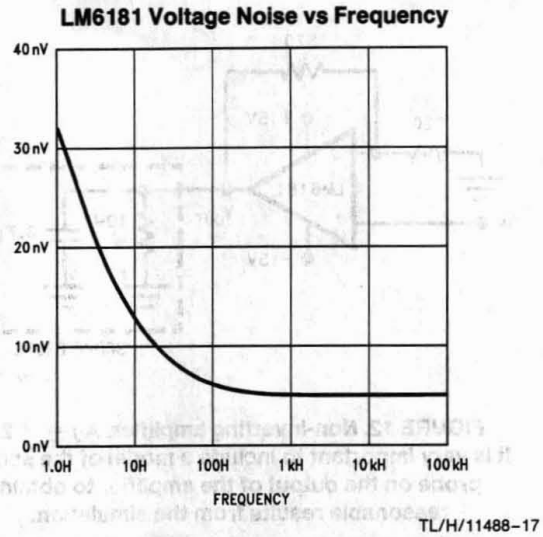

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FIGURE 19. LM6181 Simulated Voltage-Noise Response

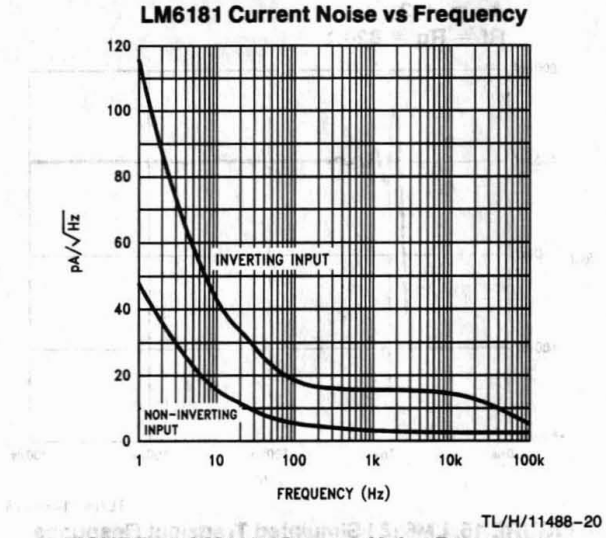

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FIGURE 20. LM6181 Current-Noise Response

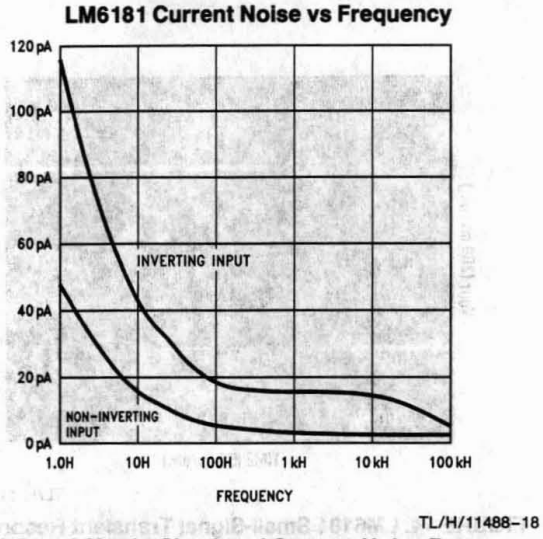

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FIGURE 21. LM6181 Simulated Current-Noise Response

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A SPICE Compatible Macromodel for CMOS Operational Amplifiers

National Semiconductor
Application Note 856
David Hindi

ABSTRACT

A SPICE macromodel that captures the "personality" of National Semiconductor's CMOS op-amps has been developed. The salient features of the macromodel are a MOSFET input stage, Miller compensation, and a current-source output stage. A description of the model will be given along with correlation to actual device behavior.

INTRODUCTION

Recently, there has been a major thrust in lowering power dissipation and supply voltages for analog system level design. In response to this, National Semiconductor has developed a family of CMOS op-amps which feature rail-to-rail output swing, extremely low input bias current (10 fA typ.), single supply operation, low power consumption, and an input common-mode range that includes the negative supply rail [1]. Due to the unique topology that makes these features possible, a new SPICE macromodel was required in order to achieve accurate simulation results.

MACROMODELING PHILOSOPHY

The philosophy used in creating this macromodel was a desire to design a model that would accurately simulate the typical behavior of a CMOS op-amp while executing much faster than a device level model (commonly referred to as a micromodel). The "personality" of an op-amp can be captured by individually hand crafting and thoroughly testing each model to ensure that it accurately simulates the behavior of the real device.

CMOS MACROMODEL INPUT STAGE

The input stage performs several important functions including non-linear input transfer characteristics, offset voltage, input bias currents, second pole, and quiescent power supply current. The heart of the input stage consists of a differential amplifier which is made up of two simplified MOSFET models (see *Figure 1*) [2]. Input common-mode range can be modeled by properly setting the zero bias threshold voltage (V_{TO}) in the MOSFET model. In the case of the LMC6484, which has rail-to-rail input common-mode range, V_{TO} is left at its default value of zero. Offset voltage is modeled with an ideal voltage source, E_{OS}, while input bias/offset currents are modeled by properly setting the leakage currents on the input protection diodes DP1–DP4. Quiescent current is modeled with the combination of I2 and the R8–R9 series resistors. As the supply voltage increases, the current through R8 and R9 will increase, effectively simulating that behavior in the real device. Resistors R8 and R9 also act as a voltage divider and establish a common-mode voltage (V_H) for the model directly between the rails. If the supply rails are symmetrical, i.e. ±5V, node 49 will be at 0V. Voltage-controlled voltage-source, EH, measures the voltage across R8 and subtracts an equal voltage from the positive supply rail to provide a stiff point between the rails (node 98) to which many other stages in the model are referenced. Voltage-controlled current-source G0 and resistor R0 model the gain of the input stage. The signal is then passed to the frequency shaping stages for further conditioning.

FREQUENCY SHAPING STAGES

In keeping with the philosophy of providing a macromodel that is as accurate as possible, it has been determined that the model must be capable of easily accommodating as many poles and zeros that are necessary to precisely shape the magnitude and phase response of the model [3]. This is accomplished with telescopic frequency shaping stages that each have unity DC gain, making it easier to add poles and zeros without changing the low-frequency gain of the model. Each of the three types of frequency-shaping stages is shown in *Figure 1*.

COMMON-MODE STAGE

Common-mode gain is modeled with a common-mode zero stage whose gain increases as a function of frequency. A voltage-controlled current-source, G4, is controlled with a polynomial equation which adds the voltage at each input (nodes 1 and 2) and divides the sum by two. This result is the input common-mode voltage. The DC gain of the stage is set to the reciprocal of the CMRR for the amplifier. An inductor, L2, increases the gain of the stage at 20 dB/decade to model the roll-off of CMRR that occurs in most amplifiers. The output of the common-mode zero stage (node 16) is reflected to the E_{OS} source to provide an input-referred common-mode error.

Characteristics of National Semiconductor's CMOS Operational Amplifiers

Common Characteristics	Rail-to-rail output swing, ultra-low input bias current (10 fA typ.), low drift (1.3 μV/°C), single supply operation, input common-mode range includes ground, low power consumption, and high voltage gain.
LMC660	Drives 600Ω load, high bandwidth (1.4 MHz), high slew rate (1.1 V/μs), comes in quad and dual (LMC662).
LPC660	Low power (215 μW/amp), comes in quad and dual (LPC662).
LMC6044	Low power (70 μW/amp), comes in quad, single (LMC6041) and dual (LMC6042).
LMC6062	High precision dual (V_{OS} = 100 μV), low power (80 μW/amp).
LMC6082	High precision dual (V_{OS} = 150 μV), drives 600Ω loads, high bandwidth (1.3 MHz).
LMC6484	Rail-to-rail input common-mode range, operates on 3V single supply, drives 600Ω loads, high bandwidth (1.3 MHz), comes in quad and dual (LMC6482).

National's CMOS Op-Amp Macromodel

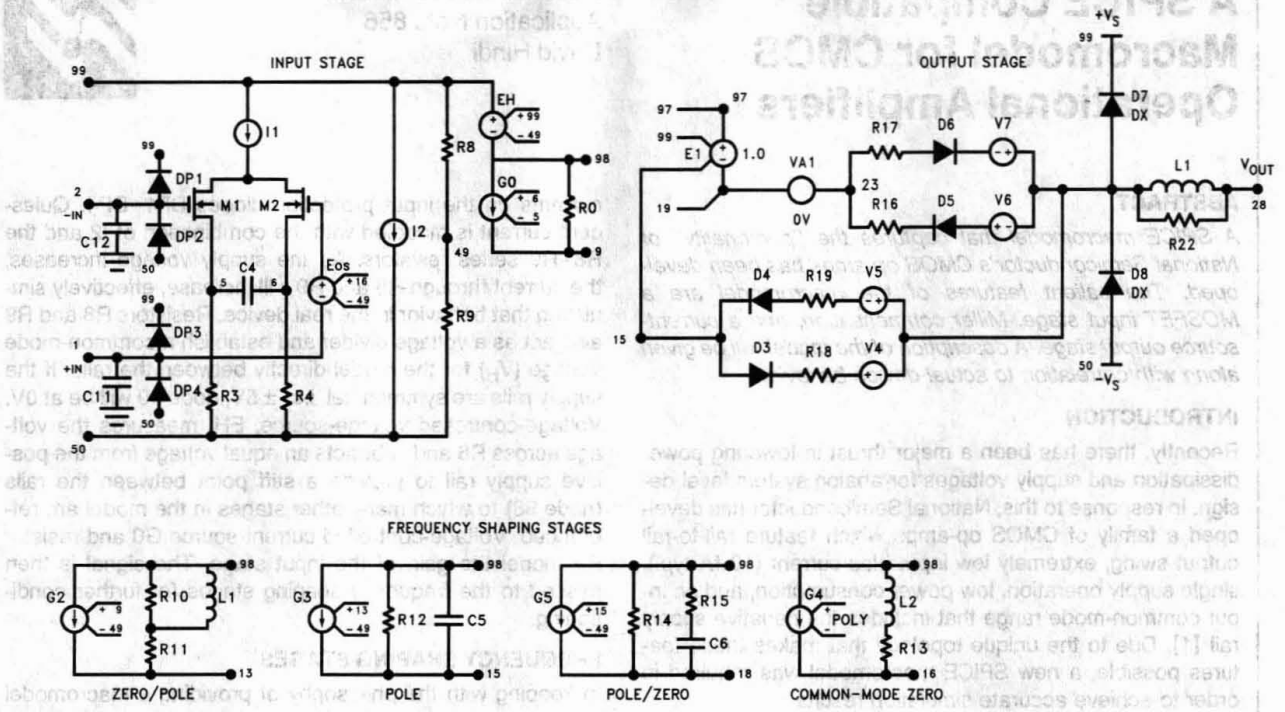

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FIGURE 1

OUTPUT STAGE

After the last frequency-shaping stage, the intermediate signal is sent to the output stage. The output stage performs several important functions including dominant pole, slew rate limiting, dynamic supply current, short-circuit current limiting, the balance of the open-loop gain, output swing limiting, and output impedance. The output stage of the macromodel incorporates several new innovations in order to accommodate the unique topology of National's CMOS op-amps. To understand the unique features of this topology, a description of the actual amplifier output stage is in order.

The main feature of National's CMOS amplifiers is that the output can swing rail-to-rail. This is accomplished by removing the traditional output buffer and taking the output directly from the integrator. The output portion of the integrator is a common-source complementary push-pull gain stage which functions as a current source. Depending on load resistance, the output stage can have a considerable amount of gain. However, since the internal compensation capacitor is referenced to the output node, the slew rate does not significantly change as the output is loaded. Also, loading the output will reduce the open-loop gain of the amplifier so that the first pole will increase in frequency in order to maintain the gain-bandwidth product of the amplifier.

In the model, Miller compensation was used to obtain an additional degree of freedom in setting the open-loop gain, slew rate, and first pole. The slew rate is defined by:

$$SR = \frac{I1}{C3}$$

while the first pole is determined with the equation:

$$f_{p1} = \frac{1}{2 \times \pi \times R5 \times C3 \times (1 + A_{VOUT})}$$

where A_{VOUT} is the gain of the output stage. Note that the slew rate can be set with C3 while the first pole can be independently set with the gain of the output stage. A gain stage consisting of a voltage-controlled current-source G1 and resistor R5 takes the signal from the last frequency-shaping stage and amplifies it by the balance of the open-loop gain ($G1 \times R5 = A_{VOL} - A_{VIN} - A_{VOUT}$). A voltage clamp made of D1, V2, D2, and V3 limits the drive to the output current-source, G6, to provide short-circuit current limiting. Since the output stage has gain, output swing limiting is performed at the output node with a clamp consisting of D5, V4, D6, and V5. A resistor, R17, models the slight degradation in output swing as the amplifier is loaded.

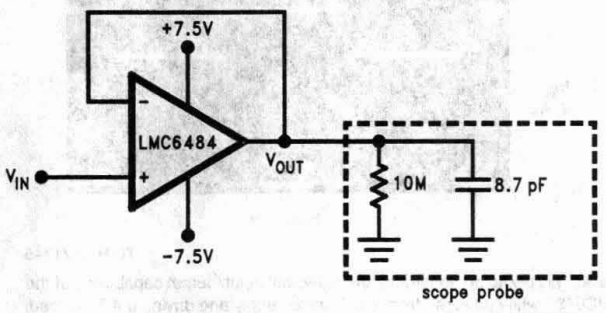
DYNAMIC SUPPLY CURRENT

A behavior that is often not included in op-amp macromodels is dynamic supply current. If the output of the model is an ideal current source, the simulated output current of the model appears to come from nowhere, i.e., the supply currents do not change. This apparent violation of the second law of thermodynamics has been solved with diodes D7–D8, current sources F5–F6, and associated circuitry. Since it is important to keep non-linear devices, such as diodes, out of the signal path, only an ideal ammeter, VA8, was inserted in the output driver to sense the sinking or sourcing of output current. Current-controlled current-source, F5, mirrors the current sensed by VA8 and forces an equal current through either D7 or D8 depending on its polarity. If current is being sourced into the load, the current flows from the positive rail through E1, VA8, and G6 to the output node and no supply current correction is necessary. However, if the output stage is sinking current from the load, the current flows from the output node up through G6, VA8 and E1 into the positive rail. To compensate for this, F5 forces an equal current through D7 and ammeter VA7. This current is then mirrored to current-source F6 which pulls an equal amount of current out of the positive rail and forces it into the negative rail. Therefore, if the output stage is sourcing current, it appears to come from the positive rail, whereas current that is sinking from the load appears to go into the negative rail. The net result of all these extra devices is an output stage which closely models the behavior of the real amplifier.

SIMULATION ACCURACY

To ensure the accuracy of the macromodel, the simulation results are compared to lab data taken from an actual device. *Figure 2* shows a typical voltage follower transient response test circuit and *Figure 3* shows a SPICE netlist [4] for simulating the small-signal transient response of the LMC6484. Notice that the simulated response shown in *Figure 5* compares quite closely with the actual response shown in *Figure 4* with the correct amount of over-shoot and frequency of ringing.

Figures 6 and *7* demonstrate the rail-to-rail input and ouput capabilities of the actual LMC6484 and the model respectively. The amplifier was configured as a voltage follower and powered from a 3V single supply. Then, a 3 V_{PP} square-wave was applied to the non-inverting input. The amplifier is clearly capable of handling this rail-to-rail input and reproducing it on the output while driving a 4.7 kΩ load. The simulation results show that the macromodel accurately models the slew rate and output swing of the amplifier.



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Note: It is very important to include a model of the scope probe on the output of the amplifier to obtain reasonable results from the simulation.

FIGURE 2. Non-Inverting Amplifier ($A_V = +1$)

```
* LMC6484 S.S. Pulse Response. V(6)
* Cload = scope
*
XAR1 3 6 7 4 6 LMC6484
VP 7 0 7.5V
VN 4 0 −7.5V
VIN 3 0 PULSE (−.1V .1V 3U 20N 20N 5U)
Rout 6 0 10MEGohm
Cout 6 0 8.7pF
.LIB CMOSOA.LIB
.TRAN/OP .1N 10U
.PROBE
.END
```

FIGURE 3. Non-Inverting Amplifier Netlist to Simulate the Small-Signal Response of the LMC6484 [4]

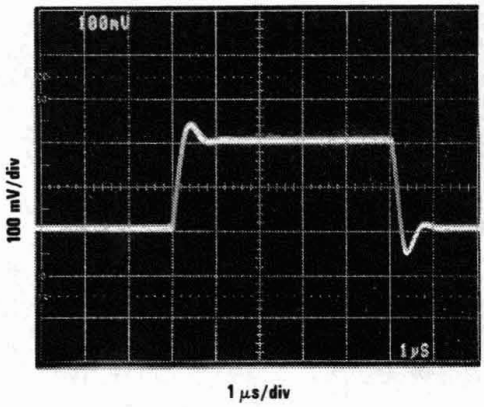

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FIGURE 4. LMC6484 Small-Signal Transient Response

LMC6484 S.S. Pulse Response (V(6) C_{LOAD} = scope)

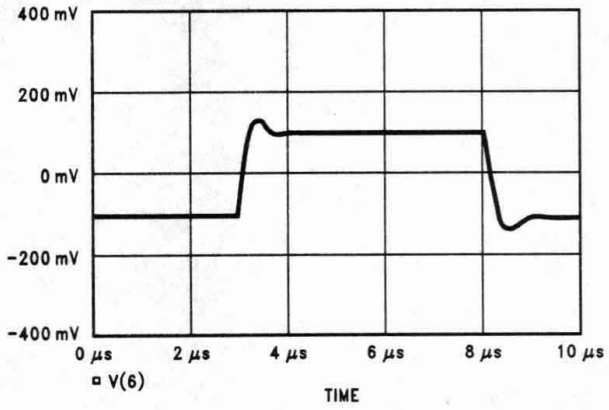

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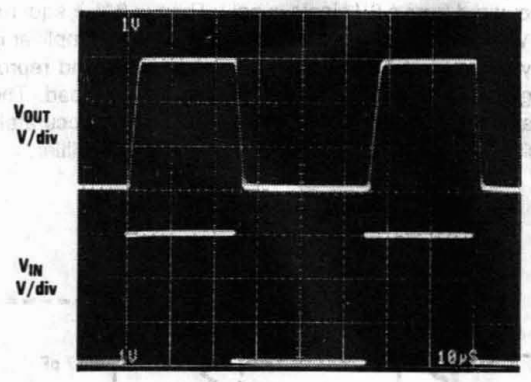
FIGURE 5. Simulated Small-Signal Transient Response



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Note: This photo demonstrates the rail-to-rail input/output capabilities of the LMC6484 while powered from a 3V single supply and driving a 4.7 kΩ load. Don't try this with an ordinary op-amp.

FIGURE 6. Large-Signal Transient Response

LMC6484 L.S. Pulse Response
(Av = +1, V_{SUPP} = 0, +3, R1 = 4.7k)

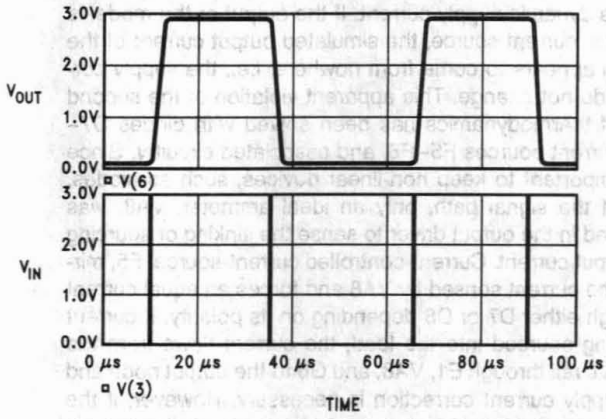

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FIGURE 7. LMC6484 Simulated Large-Signal Transient Response

CONCLUSION

An accurate SPICE macromodel has been developed that captures the "personality" of National Semiconductor's CMOS operational amplifiers. The macromodel includes effects such as rail-to-rail output swing, input common-mode range, MOSFET input stage transfer characteristics, accurate frequency and transient response, slew rate and output short-circuit current. The model is not capable of simulating PSRR, thermal effects, or noise at this time.

Since the macromodels are much less complex and have fewer p-n junctions than a transistor level micromodel, simulation speed is much faster. For example, an LMC6484 macromodel simulation executed 34 times faster than its transistor level model. With accurate macromodels, the designer can quickly determine the dominant effects of a circuit and explore effects that are difficult to obtain with lab bench evaluation.

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Guide to CRT Video Design

National Semiconductor
Application Note 861
Zahid Rahim

INTRODUCTION

This application note provides a design guide for successfully designing high frequency CRT video boards. For better illustration, an example of a complete video board design using the LM1203N RGB preamplifier and the LM2419 RGB CRT driver is provided. The design includes: DC restoration, contrast control, brightness control, cutoff adjustment, delta gain adjustment (for white balance) and blanking at grid G1. The complete circuitry for the video board is shown in *Figure 13*. *Figure 1* shows the pulse response at the cathode for a 45 V_{PP} output signal. Rise and Fall times at the cathode were measured at 6 ns and 7.5 ns respectively and settling time (to within ±5% of final value) was measured at 20 ns. The overshoot and undershoot were measured at 5V. An NEC-5D multi-sync monitor was used to evaluate the video board, the performance of the video board was very good at 1024 x 1024 display resolution. Various sections of *Figure 13's* circuit are described below in detail.

1.0 RGB PREAMPLIFIER (LM1203)

The LM1203 is a wideband video amplifier system specifically designed for RGB CRT monitor applications (Reference 1—LM1203 Data Sheet). The device includes three matched video amplifiers, three matched attenuator circuits for contrast control, and three gated differential input clamp comparators for black level clamping of the video signal. In addition, each video amplifier includes a gain adjustment or "drive" pin for individual gain adjustment of each video channel to allow white balance adjustment.

1.1 RGB Video Signals

The RGB video signals are AC coupled to the inputs of the LM1203 preamplifier. As shown for the Green channel (see *Figure 13*), C1 AC couples the video signal and R8 references the signal to 2.4 V_{DC} reference voltage from pin 11. The 75Ω resistor, R1, is a termination resistor whose value matches the characteristic impedance of the 75Ω coaxial cable. Note that if a 50Ω video generator is used with 50Ω coaxial cables to test the video board then 50Ω termination resistors should be used.

In the absence of R2, the stray input capacitance of the LM1203 would effectively short R1 at high frequencies causing reflections. The 33Ω resistor, R2 maintains reasonable termination at high frequencies thereby minimizing reflections. Note that the value of R2 should not be much larger than 33Ω otherwise the rise and fall times of the output signal would be degraded.

1.2 Gain Adjustment and Black Level Clamping

Potentiometers R16 and R25 allow the user to adjust the gain of the Blue and Green channels respectively for achieving correct white balance. The gain of the Red channel is fixed by resistor R20. Once white balance is achieved, the contrast control potentiometer R11A allows the user to adjust the gain of all three channels simultaneously.

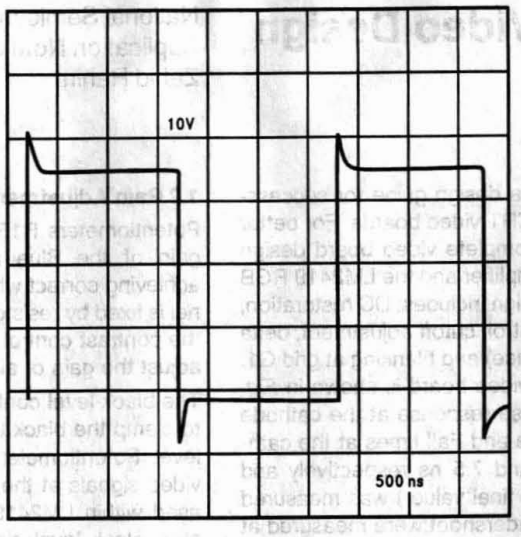
The black level control potentiometer, R27, allows the user to clamp the black level of the video signals to the desired level. Potentiometer R27 should be adjusted such that the video signals at the output of LM2419 (CRT driver) are biased within LM2419's linear operating region. To accomplish black level clamping, however, a back porch clamp signal must be applied to the clamp gate input (pin 14) of LM1203. The MM74HC86 quad exclusive-or gate generates the required back porch clamp signal (see section 4.0).

1.3 Preamplifier Gain Peaking for Improved Rise and Fall Times

Connecting a small capacitor from LM1203's drive pins (pins 18, 22 and 27) to ground peaks the amplifier's high frequency gain and increases the −3 dB frequency. Using 18 pF peaking capacitors (C100, C101 and C102 in *Figure 13*), LM1203's bandwidth is 70 MHz and rise/fall times under 7 ns. If the LM1203 is used to directly drive the LM2419 without the buffer transistors Q1, Q2 and Q3 then 33 pF peaking capacitors should be used. Refer to the LM1203 data sheet for information on frequency response using various peaking capacitor values. To minimize overshoot, the peaking capacitor should be less than 60 pF.

1.4 Buffered Output

Some CRT drivers have large input capacitance which makes it difficult for the preamplifier to directly drive the CRT driver and yet maintain the required bandwidth. In such applications, a buffer transistor is used between the preamplifier and the CRT driver (for example, transistor Q1 for the Green channel in *Figure 13*). The buffer transistor used should have a high f_T at high currents. The LM1203 can directly drive the LM2419 without sacrifice in bandwidth. However, buffer transistors have been used in our design to illustrate a complete design. The overall response of *Figure 13's* circuit is similar with or without the buffer transistors. A 2N5770 transistor was selected which has a minimum f_T of 900 MHz. Note that for fast fall time, the emitter resistor of the buffer transistor should not be much larger than 330Ω.



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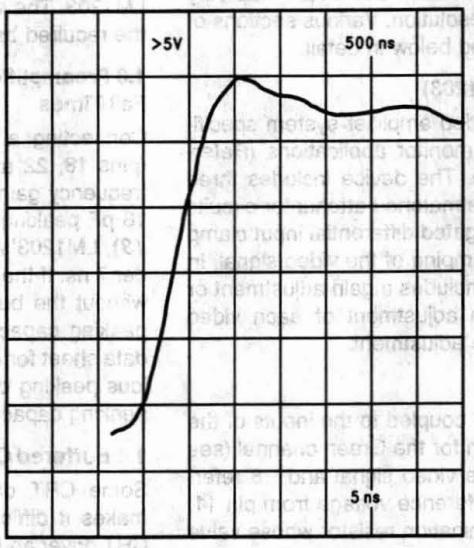
(a)



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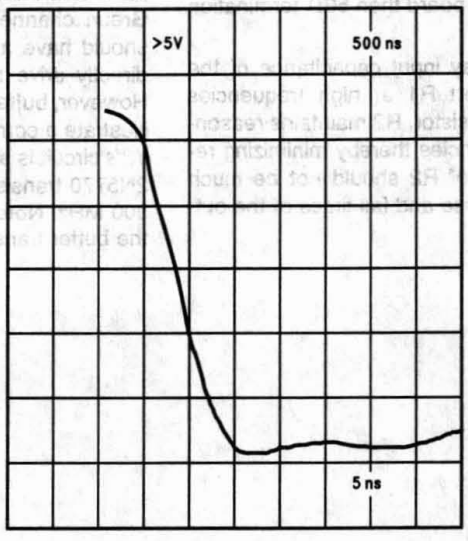

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(c)

FIGURE 1. Pulse Response at the Cathode for *Figure 13*'s Circuit

2.0 RGB CRT DRIVER (LM2419)

The LM2419 is a high-voltage, wide-bandwidth amplifier that drives the CRT's cathodes (Reference 2—LM2419 Data Sheet). The outputs of the LM2419 are AC coupled to the cathodes (see *Figure 13*) so that cutoff voltages greater than 80V can be accommodated at the cathodes. Furthermore, large variation in cutoff voltages can be accommodated because of the 120V supply. With the video signal AC coupled to the cathode, the signal's DC information is lost. To restore the DC information of the video signal, the video signal's black level is clamped at the cathode.

2.1 Black Level Clamping (DC Restoration)

Figure 2 shows the black level clamping circuitry for the Green channel. Capacitor C25 AC couples the video signal to the cathode. Transistor Q4 and diode D8 clamp the signal's black level to a voltage two diode drops greater than the voltage at the base of Q4. Adjusting the voltage at the base of Q4 using potentiometer R44 adjusts the clamp voltage thereby providing cutoff adjustment. Note that if the video signal has a sync tip then the clamp circuit will clamp the sync tip to the clamp voltage. The transistor selected for Q4 should have a BVCEO rating greater than 120V and low junction capacitance. For our design, an MPSA92 PNP transistor was selected. Diode D7 is used to protect transistor Q4 from an arc-over. D7 clamps Q4's emitter to a diode drop above 120V and provides a low impedance path for the arc-over current to flow through D8 and D7 to the 120V supply. The diodes used should have a high current rating, low series impedance and low shunt capacitance. An FDH400 diode is recommended.

2.2 Arc Protection

The CRT driver must be protected from arcing within the CRT. To limit the arc-over voltage, a 200V spark gap should be used at each cathode. Diodes D1 and D2 (see *Figure 3*) clamp the voltage at the output of LM2419 to a safe level. The clamp diodes used should have a high current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. Resistor R54 in *Figure 3* limits the arc-over current while R33 limits the current into the CRT driver. Limiting the current into the CRT driver limits the power dissipation of the output transistors when the output is stressed beyond the supply voltage. The resistor values for R33 and R54 should be large enough to provide optimum arc protection but not too large that the amplifier's bandwidth is adversely affected.

Grids G1 and G2 should also have spark gaps. A 300V and a 1 kV spark gap are recommended for G1 and G2 respectively. The PC board should have separate circuit ground and CRT ground. The board's CRT ground is connected to the CRT's ground pin and also directly connected to the chassis ground. The spark gap's ground return should be to the CRT ground so that high arc-over ground does not directly flow through the circuit ground and damage sensitive circuitry. At some point on the PC board, the circuit ground and the CRT ground should be connected. Often a small resistor is connected between the two grounds to isolate them (see *Figure 3*).

2.3 Overshoot Compensation

LM2419's overshoot is a function of both the input signal rise and fall times and the capacitive loading. The overshoot is increased by either more capacitive loading or faster rise and fall times of the input signal. The circuitry to reduce overshoot is shown in *Figure 4*. Without the compensation circuit (i.e. without R2 and C1) the overshoot and undershoot for the PC board of *Figure 10* were measured at 10% and 15% respectively (V_{OUT} = 40 V_{P-P}). With the compensation circuit in place (i.e. with R1 = 24Ω, R2 = 3.9 kΩ and C1 = 3 pF), overshoot and undershoot were reduced to 0% and 3.8% respectively. Inclusion of the compensation circuitry caused the rise and fall times to increase by 1 ns.

The values for the compensation circuit will depend on PC-board layout and LM2419 loading. Here's how to select the correct component values for the compensation circuit shown in *Figure 4*:

(a) R1 and R2 reduce the gain of the CRT driver at high frequencies thereby reducing overshoot.

(b) C1 determines the frequency at which gain is reduced and introduces a time constant in the pulse response.

(c) The time constant, τ = R2 × C1 should be less than 20 ns. Capacitor C1 should be selected to be 3 pF or slightly larger so as to eliminate the effect of stray capacitance. If C1 is too large such that $\tau \gg$ 20 ns then the pulse response will be damped, causing long rise and fall times and therefore picture smearing.

(d) Making R2 too large will cause a damped pulse response, giving rise to picture smearing. If there is a need to change the high frequency gain to adjust the level of overshoot then the value of R1 should be changed since this will not affect the time constant.

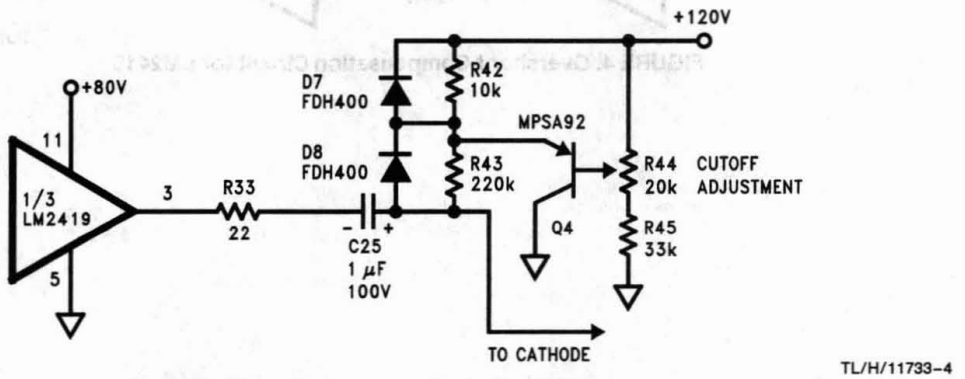


FIGURE 2. Black Level Clamp Circuit for DC Restoration

(e) With the value of R2 fixed, increasing the value of R1 will decrease the high frequency gain and therefore reduce the amplitude of the overshoot. Conversely, decreasing the value of R1 will increase the high frequency gain and therefore increase the amplitude of the overshoot.

(f) Suggested initial starting values for *Figure 4*'s circuit are: R1 = 24Ω to 100Ω, C1 = 3 pF to 6 pF, R2 × C1 < 20 ns.

Figure 5 shows the pulse response at the output of LM2419, with and without compensation.

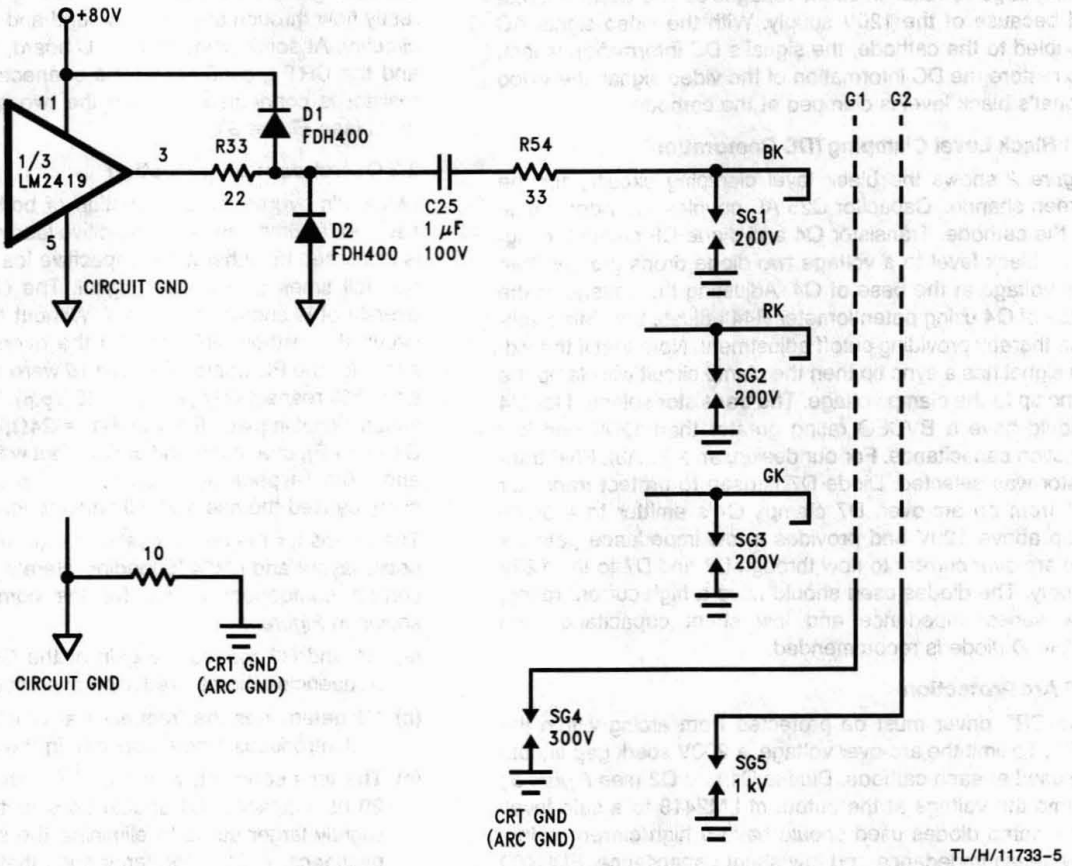


FIGURE 3. Arc Protection Circuit

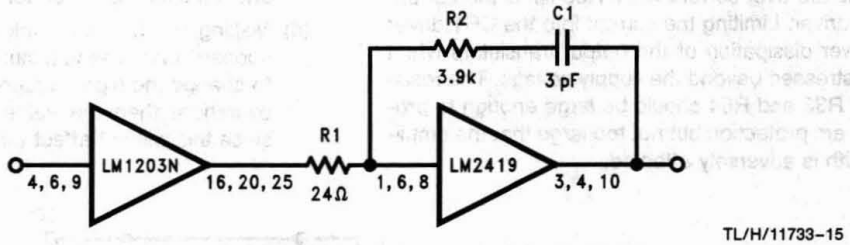
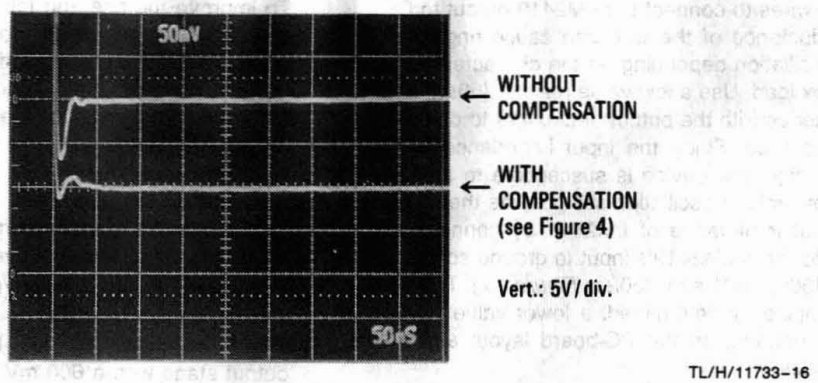


FIGURE 4. Overshoot Compensation Circuit for LM2419



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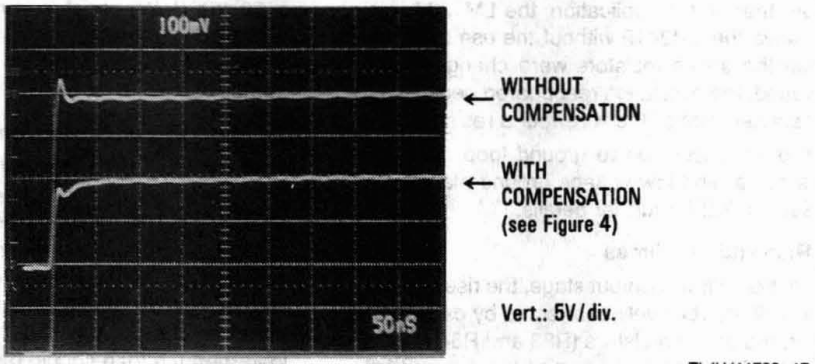
(a)



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(b)

FIGURE 5. Pulse Response with and without Overshoot Compensation

2.4 Suppressing Oscillation

As is the case with all wideband amplifiers, PC-board layout precautions must be taken to prevent oscillation. Experimentation had shown that when the LM2419's output was probed with a passive probe (100:1, 5 kΩ probe) connected to a 50Ω oscilloscope, the LM2419's output burst into oscillation. However, when probed with a high input impedance (1 MΩ) FET probe the oscillation was not present. Further investigation showed that the oscillation was caused by: the inductance of the trace connected between the LM1203's output and the LM2419's input; type of loading—in this case, the complex impedance of the 5 kΩ passive probe; and high frequency channel-to-channel cross-talk internal to LM2419. The oscillation can be eliminated by applying the following guidelines:

(a) Minimize trace length between the preamplifier output and LM2419 input. If long trace length is unavoidable then use low value (22Ω for example) series resistors with short lead length in the signal path to damp the inductance of the trace. Use carbon resistors and avoid using wire wound resistors because they are inductive.

(b) Avoid long wires to connect the LM2419 output to CRT socket. Inductance of the wire can cause ringing and possible oscillation depending on the characteristics of the complex load. Use a low value resistor (50Ω for example) in series with the output of LM2419 to damp the wire's inductance. Since the input impedance of the LM2419 is high, the device is susceptible to high frequency cross-talk. If oscillation still persists then lowering the input impedance of LM2419 by connecting a 1 kΩ resistor from LM2419's input to ground solves the problem (R500, R501 and R502 in *Figure 13*). The 1 kΩ value is empirically determined, a lower value may be required depending on the PC-board layout and load characteristics.

Two 50Ω series resistors between LM1203 output and LM2419 input were required to damp the inductance of the signal trace. Note that in this application, the LM1203 was used to directly drive the LM2419 without the use of buffer transistors. When the series resistors were changed from carbon to wirewound, the oscillation reappeared because of the inductive characteristics of the wirewound resistors.

Oscillations can often occur due to ground loop currents. Having separate power and low voltage ground planes will help. Refer to Section 7.2 for further details.

2.5 Improving Rise and Fall Times

Because of an emitter follower output stage, the rise and fall times of the LM2419 are relatively unaffected by capacitive loading. However, the series resistors (R33 and R54 for the Green channel, see *Figure 13*) will increase the rise and fall times when driving the CRT's cathode which appears as a capacitive load. The capacitance at the cathode typically ranges from 8 pF to 12 pF and every effort is made to minimize this capacitance.

To improve the rise and fall times at the cathode, a small inductor is often placed in series with the output of the amplifier. The series peaking inductor peaks the amplifier's frequency response at the cathode thus improving the rise and fall times. The value of the inductor is empirically determined. An inductor value of 50 nH is a good initial starting value. Note that peaking the amplifier's frequency response will increase the overshoot. Therefore the value of the inductor selected is a compromise between optimum rise and fall times and acceptable overshoot.

At low output voltage swing (for ex: $V_{OUT} < 5\ V_{P-P}$), the rise and fall times may degrade by as much as 50% or more. This is caused by the fact that LM2419 has a class "B" output stage with a 600 mV dead band, thus giving rise to cross-over distortion. Increased rise and fall times may give rise to picture smearing at low contrast settings. Connecting a 20 kΩ (½W) resistor from LM2419's output to ground biases the output stage in class "A" mode thus maintaining similar rise/fall times at both small and large output voltage swing.

2.6 Short Circuit Protection

The output of the LM2419 is not short circuit protected. Shorting the output to either ground or to V_+ will destroy the device. The minimum DC load resistance the LM2419 can drive without damage is 1.6 kΩ to ground or to V_+. However, driving a 1.6 kΩ load for an extended period of time is not recommended because of power dissipation considerations. If the LM2419 is used to drive a resistive load then the load should be 10 kΩ or greater.

3.0 BLANKING AT GRID G1

The circuit used to accomplish blanking is shown in *Figure 6*. A negative voltage is applied to grid G1 using the resistor divider comprised of R58 and R60. Brightness control is achieved by varying the bias at G1 using potentiometer R60. Blanking at the grid is accomplished by R59, R62, D13 and C34.

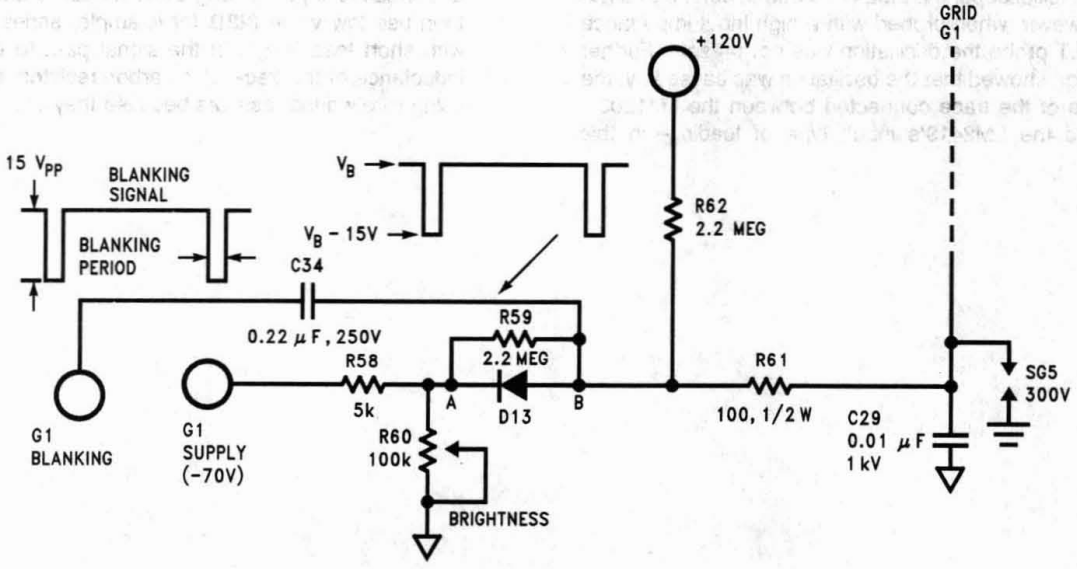

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FIGURE 6. Circuitry for Blanking at the Grid

Resistor R62 biases the clamp diode D13. A 15 V_{PP} blanking signal is AC coupled through C34. Since the voltage at node "B" can not go more than one diode drop above the voltage at node "A", the blanking signal at G1 is clamped at the G1 bias voltage.

During the blanking portion of the video signal, the blanking signal goes low thus reverse biasing D13 and pulling G1 15V negative with respect to its normal bias voltage. This action cuts off the CRT's beam current during the blanking interval and accomplishes blanking.

4.0 BACK PORCH CLAMP GENERATOR

A versatile backporch clamp generator circuit is shown in *Figure 7.* A quad exclusive-or gate (MM74HC86) is used to generate the back porch clamp signal from the composite H-Sync input signal. The composite H-Sync input signal may have either positive or negative polarity. The logic level at pin 11 (Flag Out) indicates the polarity of the H-Sync signal applied to the clamp generator. The Flag output is a logic low (less than 0.8V) if the H-Sync input signal has a negative polarity and is a logic high (greater than 2.4V) if the H-Sync input signal has a positive polarity.

Regardless of the H-Sync input signal's polarity, a negative polarity H-Sync signal is output at pin 8. Furthermore, a negative polarity back porch clamp pulse is output at pin 3. The width of the back porch clamp pulse is determined by the time constant due to R28 and C12. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R28 or C12 or both. Note that an MM74C86 exclusive-or gate may also be used, however, the pin out is different than that of the MM74HC86.

5.0 THERMAL CONSIDERATIONS

The LM1203 preamplifier does not require a heat sink. However, the LM2419 requires a heat sink under all operating conditions. For the LM2419, the worst case power dissipation occurs when a white screen is displayed on the CRT. Considering a 20% black retrace time in a 1024 x 768 display resolution application, the average power dissipation for continuous white screen is less than 4W per channel with 50 V_{PP} output signal (black level at 75V and white level at 25V). Although the total power dissipation is typically 12W for a continous white screen, the heat sink should be selected for 13W power dissipation because of the variation in power dissipation from part to part.

For thermal and gain linearity considerations, the output low voltage (white level) should be maintained above 20V. If the device is operated at an output low voltage below 20V, the power dissipation might exceed 4.7W per channel (i.e., 14W power dissipation for the device). Note that the device can be operated at lower power by reducing the peak-to-peak video output voltage to less than 50V and keeping the clamped video black level close to the supply voltage.

Maximum ratings require that the device case temperature be limited to 90°C maximum. Thus for 50°C maximum ambient temperature and 13W maximum power dissipation, the thermal resistance of the heat sink should be:

$$\theta_{SA} \leq (90 - 50)°C/13W = 3°C/W$$

5.1 Designing the Proper Heat Sink

Once the required thermal resistance of the heat sink has been determined, the process of designing the heat sink can begin. *Figure 8* shows the thermal resistance versus the required volume for an anodized or painted aluminum heat sink. Note that the curve in *Figure 8* is based on lab measurement of 1/8" and 1/16" thick sheet aluminum and is only intended as a design guide. The actual thermal resistance of the heat sink is affected by many factors such as the shape of the heat sink, the orientation of the heat sink, etc. Once a heat sink is fabricated, its thermal resistance should be measured under actual operating conditions. The following calculations show how to design a heat sink for the LM2419.

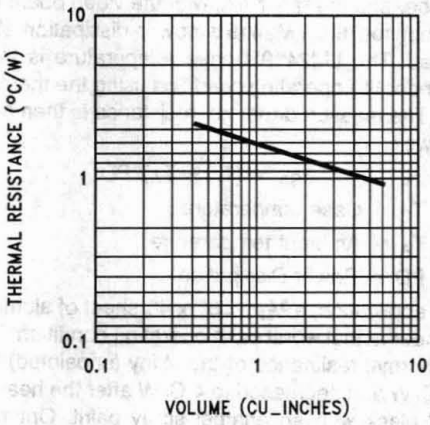

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FIGURE 8. Heat Sink Volume vs Thermal Resistance for Anodized Sheet Aluminum

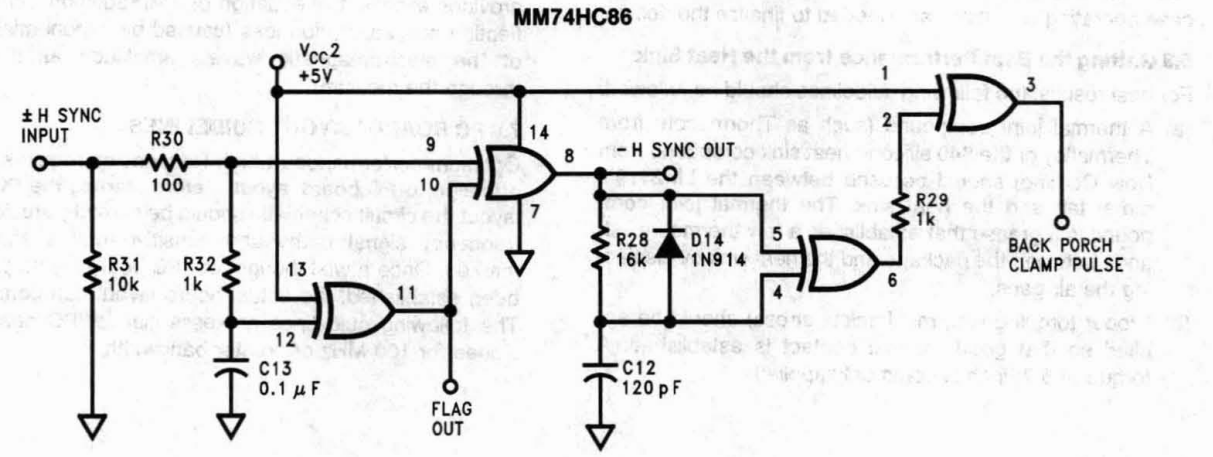

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FIGURE 7. Backporch Clamp Pulse Generator Circuit

Worst case power dissipation for LM2419 (White screen) = 13W

Required heat sink thermal resistance, θ_{SA} = 3°C/W

From thermal resistance curve in *Figure 6,* required volume of Aluminum (Al) = 2.2 cu″

For a sheet of Al with thickness, T = 3⁄32″, required area, A = 2.2 cu″ /(3⁄32)″ = 24 sq″ = 8″ x 3″

Therefore select an anodized or painted black aluminum heat sink of dimension 8″ x 3″ x 3⁄32″. Note that if the heat sink surface is bright or shiny then the thermal resistance is going to be higher than an anodized or black painted surface because of the heat sink's lower emissivity.

5.2 Measuring the Thermal Resistance of the Heat Sink

Whether a heat sink is designed or a commercially designed heat sink is used, the thermal resistance of the heat sink should be measured under actual operating condition to ensure that the measured thermal resistance meets the specification. If the heat sink's thermal resistance is higher than the required thermal resistance then the CRT driver's case may operate at a temperature higher than the recommended operating temperature thereby adversely affecting the long term reliability of the device.

To measure the heat sink's thermal resistance, a thermocouple may be used. The LM2419's metal tab is bolted on to the heat sink with a screw, a washer and a lock nut. The thermocouple's wire should be securely tightened between the washer and the tab. Next, with the video board mounted in the monitor, the LM2419's power dissipation should be measured. The LM2419's case temperature is then measured under the operating condition using the thermocouple device. The measured thermal resistance is then calculated as follows :

$$\theta_{SA} = (T_C - T_A)/PD$$

where, T_C = Case temperature

T_A = Ambient temperature

PD = Power Dissipation

For our application, a 3⁄32″ x 6″ x 4″ sheet of aluminum was used under actual worst case operating condition. The measured thermal resistance of the shiny (unpainted) heat sink was 5°C/W and decreased to 4°C/W after the heat sink was painted black with an enamel spray paint. Optimizing the shape of the heat sink could have improved the thermal resistance to less than 4°C/W. This excercise illustrates that the guidelines of section 5.1 can be used to design a heat sink and proper characterization under actual worst case operating conditions are needed to finalize the design.

5.3 Getting the Best Performance from the Heat Sink

For best results, the following guidelines should be followed:

(a) A thermal joint compound (such as Thermacote from Thermalloy or the 340 silicone heat sink compound from Dow Corning) should be used between the LM2419's metal tab and the heat sink. The thermal joint compound is a grease that establishes a low thermal resistance between the package and the heat sink by displacing the air gaps.

(b) Proper torquing (i.e., mechanical stress) should be applied so that good thermal contact is established. A torque of 6 lb-inch is commonly applied.

(c) The heat sink should be mounted vertically. This causes the heat sink to lose heat most effectively because cold air is drawn to the bottom of the heat sink, heated and moved to the top of the heat sink by convection. Furthermore, mounting the heat sink vertically is especially useful for heat sinks with fins.

(d) Either an anodized heat sink should be used or black oil paint or a dark varnish should be applied to the heatsink. This further reduces the heat sink's thermal resistance due to improved radiation heat transfer.

6.0 CONTROLLING ELECTROMAGNETIC INTERFERENCE (EMI)

There are stringent requirements on the manufacturers of electronic products to control the emission of electromagnetic waves. Electromagnetic waves not only interfere with radio and TV reception but may also affect other electronic devices in the vicinity of the source of radiation.

Voltage spikes caused by fast switching currents and the impedance of the supply line and ground connection can give rise to EMI radiation. An effective way to combat such a cause of EMI is by making use of power supply filtering and generous use of ground plane on the printed circuit board. The ground plane provides a low impedance return for the fast switching current, thereby suppressing EMI radiation.

Sometimes an undetected very high frequency (several hundred MHz) oscillation in the circuitry can give rise to significant EMI radiation. Such high frequency oscillation may not be noticeable when viewing images on the screen or may go undetected if the oscilloscope used is bandwidth limited when compared with the frequency of oscillation. By looking at the amplitude and frequency spectrum of the EMI radiation, one can discern the presence of high frequency oscillation within the circuitry.

Often long wires carrying high frequency signals can be a big contributor of EMI radiation. If that is the case then shielded cables should be used and the shield should be grounded at both ends. Grounding the shield at both ends allows the signal's return current to flow through the shield at high frequencies. The return current on the shield generates a field that tends to cancel the conductor's field thereby minimizing EMI radiation.

Some very high frequency designs require the use of conductive shield enclosures to minimize EMI radiation. In response to the offending electromagnetic field, the shield produces currents which in turn produce magnetic fields that oppose and cancel the inducing field. A steel enclosure provides excellent attenuation of EMI radiation through reflection and absorption loss (caused by exponential decay of the electromagnetic wave's amplitude as it travels through the medium).

7.0 PC BOARD LAYOUT GUIDELINES

Optimum performance at high frequencies requires careful attention to PC board layout. Before starting the PC board layout the circuit schematic should be carefully studied, high frequency signal paths and sensitive nodes should be marked. Once a well thought out PC board layout plan has been established, the actual board layout can commence. The following guidelines are essential for PC boards designed for 100 MHz or greater bandwidth.

7.1 Adequate Ground Plane

For high frequency layouts, a solid ground plane is a must. The ground plane provides a low inductance path for the circuit's return current. Moreover, a ground strip between two high frequency signal traces can reduce cross talk by referring the stray capacitance between the traces to ground.

Because of the many restrictions placed on the layout, a two sided board is recommended for bandwidths greater than 100 MHz. On a two sided PC board, a full ground plane is placed on the component side, for example the top side of the board. Signal traces are then routed on the bottom side of the board, this minimizes stray capacitance and improves the isolation between high frequency signal paths because the traces can be widely separated without affecting PC board real estate. Furthermore, a two sided board also greatly reduces the number of jumpers required when compared with a single sided board thus allowing optimum layout. A double sided board, however, adds to the cost of the board. A double sided board may cost 30% more than a single sided board. Increasing competition for high volume and low cost consumer products often necessitate the choice of a single sided board. If designed right, a single sided PC board can provide acceptable performance at 100 MHz.

When laying out a single sided PC board, every attempt should be made to layout a solid unbroken ground plane. *Figure 9(a)* shows ground voids along each column of pins of the IC and is not recommended for high frequency layout because it breaks up the flow of ground plane from the left to the right. Such a layout may also compromise the stability of the video amplifiers. The layout is improved by placing a ground void around each pin (see *Figure 9b*) thus ensuring a continuous flow of the ground plane from left to right. Some designers use pin sockets to avoid soldering the IC to the PC board. Pin sockets should be avoided if they reduce the clearance between the pins and make it difficult to achieve the layout of *Figure 9(b)*.

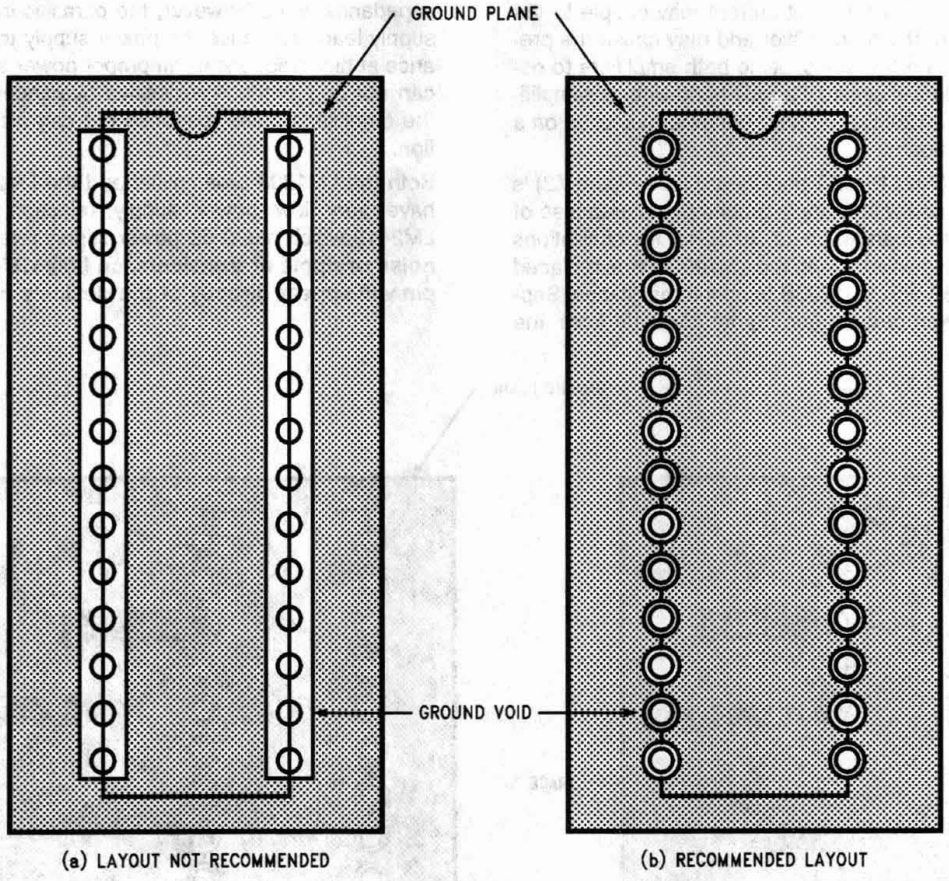

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FIGURE 9. Optimize High Frequency Layout by Having Ground Void around Each Pin (b) instead of Ground Voids along the Entire Column of Pins (a).

Figure 10(a) shows another common error made in many PC board layouts. Trace "a" as shown in *Figure 10(a)* runs both in the horizontal and the vertical direction thus breaking up the flow of the ground plane. Too many zig-zag traces in the horizontal and vertical direction can render the ground plane rather ineffective. *Figure 10(b)* shows that using jumpers to connect traces in the vertical direction maintains the flow of the ground plane from left to right. This technique is especially necessary for single sided PC boards. Note that the effect of jumpers in the signal path must be considered. Normally jumpers are used in low frequency signal paths. Furthermore, with careful planning, passive components can often be used as crossunders such that signal traces can pass under the components thereby minimizing the number of jumpers required.

7.2 Avoiding Ground Loop

Often oscillations can occur due to ground loop currents. When the CRT driver's output slews at high frequencies, large transient current is injected to the ground plane. If both the preamplifier and the CRT driver share a common ground plane then the transient current may couple to the sensitive inputs of the preamplifier and may cause the preamplifier to oscillate thereby causing both amplifiers to oscillate. The problem is severe if a wide bandwidth preamplifier such as the LM1203B (100 MHz bandwidth) is used on a single sided PC-board.

The LM1203 + LM2419 CRT neck board (see *Figure 12*) is a single sided board with a single ground plane. Because of LM1203N's limited bandwidth of 70 MHz, no oscillations were observed. However, when the LM1203N was replaced with the LM1203B, the LM1203B burst into oscillation. Separating the power ground (pin 5) of LM2419 from the low voltage ground plane and making a single point ground connection with the low voltage ground eliminated the oscillation. So, the recommendations for laying out the PC-board ground plane are as follows:

(a) The PC-board should be laid out with a separate power ground plane for the CRT driver.

(b) The CRT driver's power supply bypass capacitors should be connected to the power ground plane.

(c) The power ground plane should be connected to the low voltage ground plane at some point on the PC-board. The best place to connect the two ground planes should be empirically determined during the prototype design phase.

Use of above guidelines may also reduce ringing at the preamplifier's output and therefore further improve the overall system performance.

7.3 Power Supply Bypassing

Proper power supply bypassing is very critical for high frequency PC board layout. The power supply should be a low impedance point. However, the parasitic inductance of the supply lead can cause the power supply to be high impedance at high frequencies. Improper power supply bypassing can not only produce excessive overshoot and ringing on the amplifier's pulse response but can also cause oscillation.

Both the LM1203 preamplifier and the LM2419 CRT driver have very low power supply rejection, especially the LM2419 which has 0 dB power supply rejection. **Thus any noise or ripple or transients, on LM2419's power supply pin will appear directly at the device's output.**

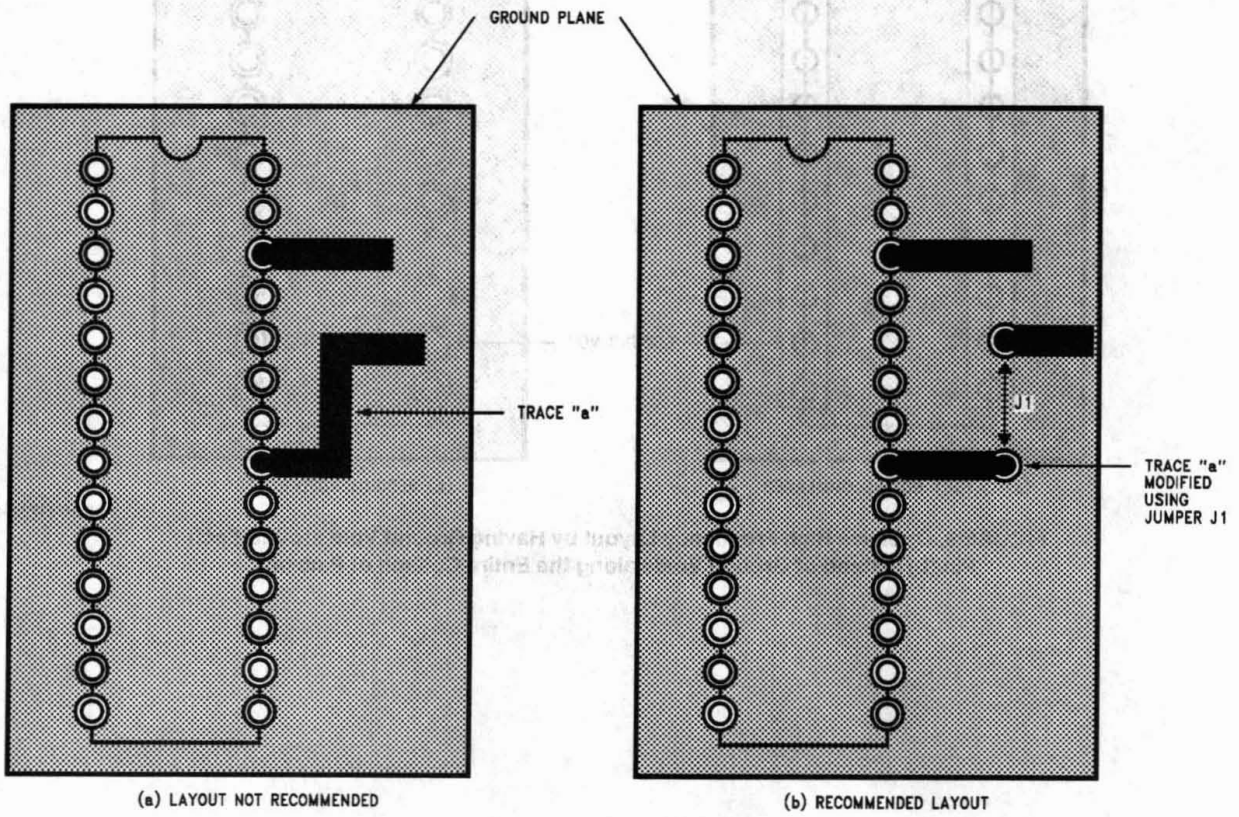

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FIGURE 10. Maintain a Continuous Flow of Ground Plane by Avoiding Zig-Zag Traces (a) and by Making Use of Jumpers (b).

A high-frequency ceramic capacitor of value 0.01 μF should be connected less than 1/4 inch from the power supply pin of the LM1203 and the LM2419. Note that for some wide-bandwidth video amplifiers, the series inductance of the 0.01 μF capacitor is large enough to cause the amplifier to oscillate and a 0.001 μF capacitor may be needed to suppress the oscillations. Since power supply bypassing is so critical, one of the first things to do when starting the PC board layout is to place the bypass capacitors first. Having done so, the designer can then position the rest of the components on the board.

In addition to a high frequency bypass capacitor, a large bypass capacitor of value 10 μF or higher is also required. The large bypass capacitor can be placed a reasonable distance from the supply pin. For LM1203 and the LM2419, 10 μF electrolytic or tantalum capacitor should be connected as close to each supply pin as is practical (see *Figure 13*). The large bypass capacitor acts as an energy storage element and is the source of large transient currents when driving capacitive loads. For example, 5 ns rise and fall times when driving a 12 pF capacitive load at the output of LM2419 would require 120 mA ($i = C\ dV/dt = 12\ pF \times 50V/5\ ns$) current per channel. The 10 μF bypass capacitor provides the 360 mA charge and discharge current for the load while the voltage change on the power supply is only 180 μV

$$\Delta V = 3 \times i \times \Delta t/C = 3 \times 120\ mA \times 5\ ns/10\ \mu F$$

Also note that the supply connector of LM1203 and LM2419 are bypassed with a 100 μF and a 47 μF capacitor respectively (see *Figure 13*).

Once the video board has been designed and is ready for evaluation, the power supply pin of each IC should be probed and the waveform observed on an oscilloscope. The waveform on the power supply should be observed with the video board operating at the maximum frequency. In a well-designed and well-bypassed board, power supply ripple, noise and transients would be minimum.

7.4 Optimizing the Layout of the High-Frequency Signal Path

Figure 11(a) shows that the components connected to the video input and output pins are placed above the ground plane. In wide bandwidth applications, the stray capacitance from the component to the ground plane can reduce the amplifier's bandwidth. *Figure 11(b)* shows an improved layout where a ground void (absense of ground plane) is placed along the high frequency signal path. Note the large ground void under the components and along the periphery of the signal trace (see *Figure 11(b)*). Furthermore, a large ground void is also placed around all components connected to the CRT socket as well as the CRT driver's outputs.

Every effort should be made to minimize the length of the video signal path. A long trace for instance will behave as a transmission line if the trace length is greater than 1/15th the wavelength of the highest frequency signal. Long trace lengths along the high-frequency signal path can introduce unwanted ringing and overshoot. If a long trace length is unavoidable, then the trace length may be broken up by resistors in series. By minimizing stray capacitance in the layout and using small value series resistors, the reduction in the amplifier's bandwidth can be made negligible.

7.5 Minimizing Crosstalk

Capacitive coupling between two adjacent traces will give rise to crosstalk. The greater the slew rate of the signal propagating through the trace the larger the crosstalk. Crosstalk can be minimized by increasing the separation between traces. Also, a ground strip between high-frequency signal traces can reduce crosstalk by breaking up the inter-trace stray capacitances and referring them to ground. Lowering the impedance of the trace can also reduce crosstalk but this may not always be practical. The following guidelines are recommended:

a. Place a ground void along the high-frequency signal trace (see *Figure 11b*).
b. Keep as much separation between high-frequency signal traces as is possible.
c. Include ground plane between high-frequency signal traces.
d. Keep output signals away from the inputs of the amplifier and from other sensitive nodes in the circuit.

8.0 COMPLETE PC BOARD LAYOUT

A complete PC board layout of *Figure 13's* circuit is shown in *Figure 12*. The ground plane and signal traces are on the bottom side of the board while the silk screen covers the top side. The board makes generous use of ground plane in and around the preamplifier and CRT driver sections. Moreover, jumpers are used to maintain a solid unbroken ground plane.

The high frequency bypass capacitors are placed less than 1/4 inch from the power supply pins. Also, there is ground void along the high frequency signal path and around the CRT socket.

ACKNOWLEDGEMENT:

The author would like to acknowledge the contribution of Ron Page for the backporch clamp generator circuit (see *Figure 7*) and Tom Mills for the thermal resistance curve (see *Figure 8*).

REFERENCE:

1. LM1203 data sheet, National Semiconductor Corporation.
2. LM2419 data sheet, National Semiconductor Corporation.

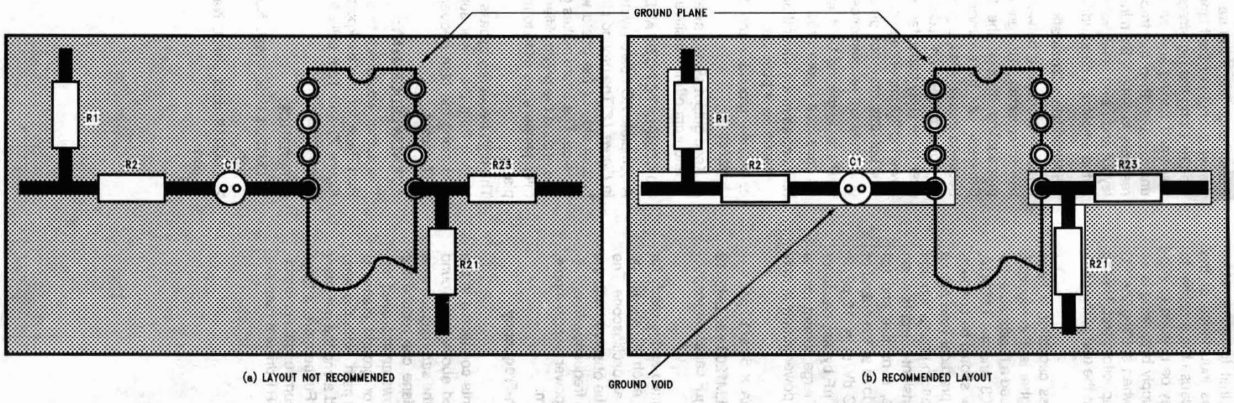

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FIGURE 11. Using Ground Voids along the High-Frequency Signal Path Minimizes the Effect of Stray Capacitance

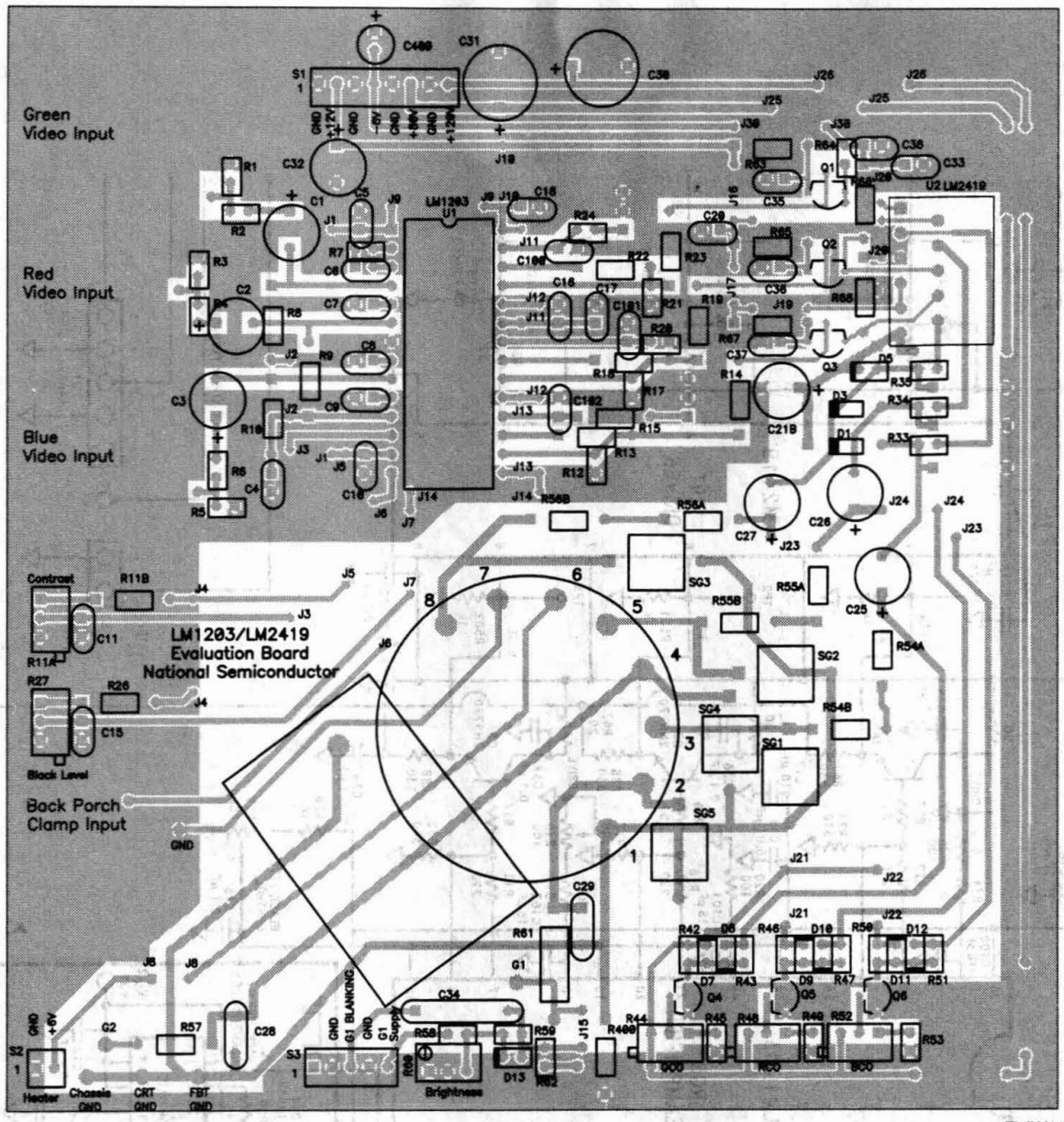

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FIGURE 12. Single Sided PC Board Layout of *Figure 13*'s Circuit

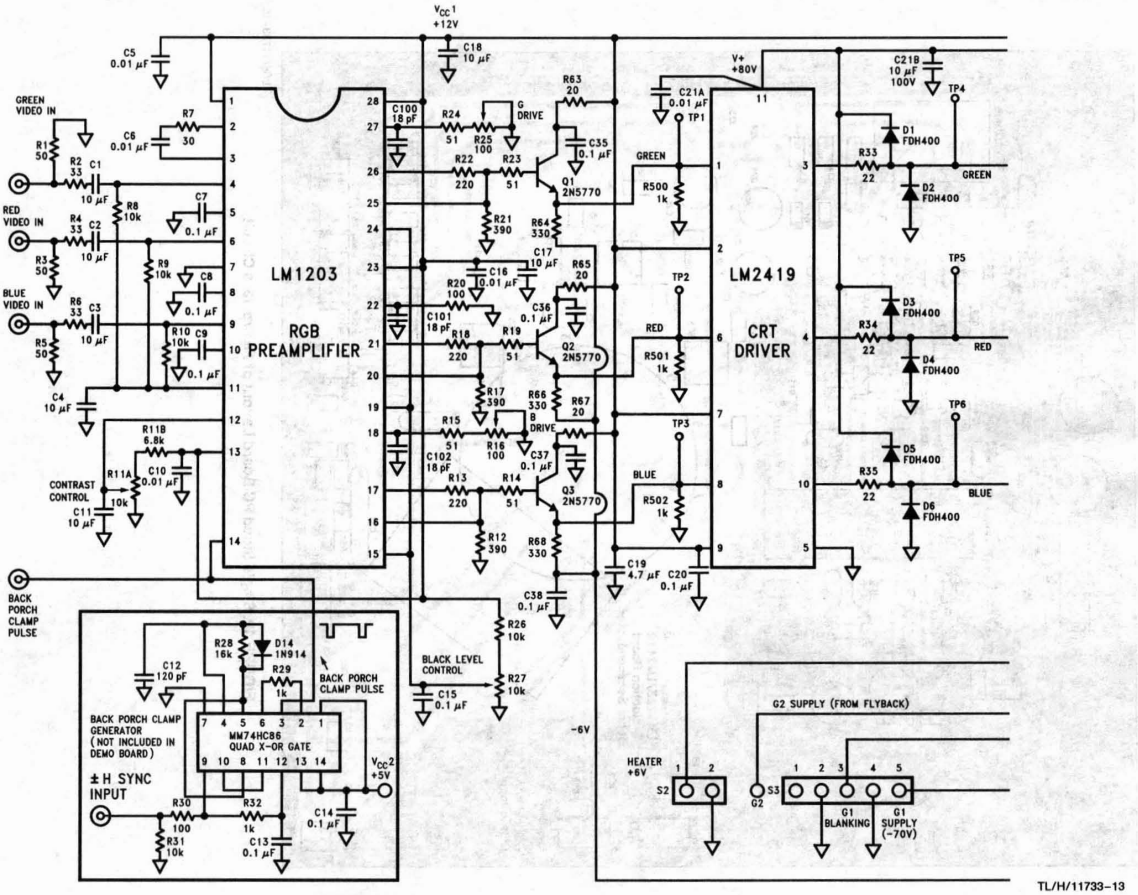

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FIGURE 13. Complete Circuit of CRT Video Board

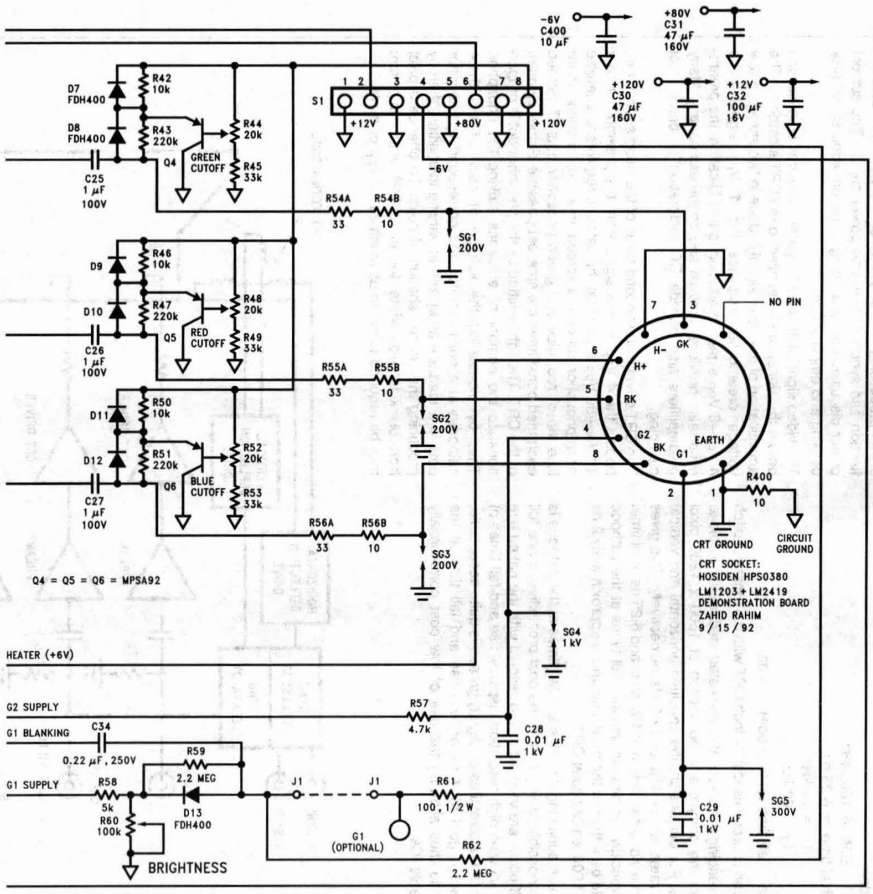

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FIGURE 13. Complete Circuit of CRT Video Board (Continued)

Designing the Video Section of 1600 x 1280-Pixel CRTs

National Semiconductor
Application Note 867
Zahid Rahim

DESIGN OBJECTIVES

- Design the complete video section for a 1600 x 1280 display resolution CRT monitor
- Video:
  B.W = 160 MHz
  Pixel time = 6.25 ns
  f_H = 74 kHz
  f_V = 60 Hz
  Rise/Fall time (at Cathode) < 4 ns
- Tube characteristics: 27 inch CRT with 0.37 mm dot pitch

After reading this paper, the interested reader will be able to design the complete video section of 1600 x 1280 pixel CRTs. For our design, the specified horizontal and vertical scan rates are 74 kHz and 60 Hz respectively. This gives rise to a video bandwidth of 160 MHz and 6.25 ns pixel time. Theoretically the desired rise and fall times at the cathode should be a third of the pixel time and is approximately 2 ns for a 1600 x 1280-pixel CRT.

Although achieving 2 ns rise and fall times at the cathode is not impossible, doing so may be cost prohibitive. Since full on-off pixels are very difficult to resolve with the naked eye when viewing high resolution displays, rise and fall times of one half the pixel time or slightly greater is quite acceptable. We set a goal of 4 ns or less rise and fall time at the cathode thus allowing the use of low cost commercially available ICs.

Figure 1 shows a simplified block diagram of a color CRT (Cathode Ray Tube) monitor. The entire circuitry within the monitor can be grouped into three main categories: video signal processing and amplification, horizontal/vertical deflection and synchronizing, and power supply. The subject of our discussion here is going to be on video signal processing and amplification.

The video signal is usually 1 V_{PP} and requires amplification before the signal can be applied to the CRT's cathode. The amplification of the video signal is done in two stages. A low voltage preamplifier amplifies the 1 V_{PP} signal to a 4 V_{PP}–6 V_{PP} signal. In addition to amplification, the preamplifier also provides contrast and brightness control. Many preamplifiers also provide DC restoration or black level clamping.

The CRT driver is the second stage of the video section that boosts the 4 V_{PP}–6 V_{PP} signal from the preamplifier to a 40 V_{PP}–60 V_{PP} signal that the cathode requires to energize each phosphor dot on the screen. In a color monitor, there is a trio of red, blue and green phosphor dots. Together, each triad constitutes the smallest possible picture element of the CRT. The light emitted by the phosphor dot is proportional to the number of electrons striking the phosphor. Thus by modulating the voltage of each of the three cathodes in a color monitor, the corresponding phosphor dots in a triad are energized at varying intensities, thereby producing the various shades of color. To change a pixel from black to peak white, the three CRT video amplifiers may be required to swing as much as 40 V_{PP} or more.

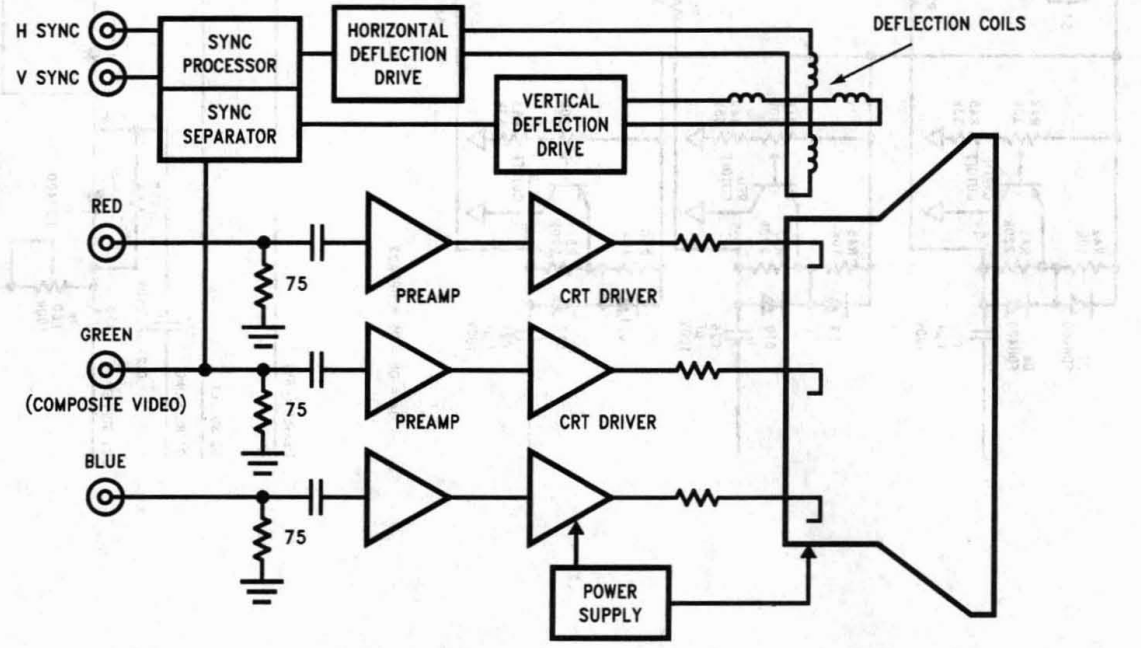

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FIGURE 1. Simplified Block Diagram of an RGB CRT Monitor

Functions Needed on a CRT Video Board

- Video signal amplification
- DC restoration
- H/V sync and/or sync on green processing
- Contrast and brightness control
- Δ gain and cutoff adjustments
- Video blanking

The CRT video board accomplishes the task of video signal processing and amplification. Video signal amplification is required to amplify the 1 V_{PP} video signal from the computer to a 40 V_{PP}–60 V_{PP} signal at the cathode. The input video signal is normally AC coupled since it is difficult to match DC references of an unknown source. Therefore DC restoration circuitry is needed to restore the DC component of each line on the screen. This is accomplished by clamping the video signal to the black level. Horizontal and vertical (H/V) sync processing circuitry is employed to generate the clamp pulse required for DC restoration.

The CRT board must also have contrast (AC gain) and brightness (DC offset) controls. These controls are usually accessible to the user so that he may adjust them. For color monitors, the board must also make provisions for Δ gain adjustment for white balance. Also, color monitors require independent cutoff adjustments to match the normally mismatched guns in a color tube.

Additional features that would be desirable are: "Sync on Green" and video blanking. Some computers transmit a composite video signal on the green channel. The composite video signal carries both video and sync information. A "Sync on Green" feature in the monitor directly extracts the necessary sync signals from the composite video signal without the need for an external H/V sync signal. During horizontal and vertical retrace, the screen is blanked to make the retrace lines invisible. Normally blanking is done by applying a large negative pulse at grid G1 during the blanking interval.

Before starting our design lets partition the system into functional blocks and create a roadmap. A system block diagram of the video section is shown in *Figure 2*. Since the required cutoff voltage at the cathodes is greater than the supply voltage of the CRT driver, the video signal is AC coupled. To restore the video signal's DC component at the cathode, a black level clamp circuit operating from +120V supply clamps the signal's black level to the desired cutoff voltage. And, to ensure that the CRT guns are completely cutoff during retrace, grid (G1) blanking is employed. The circuitry for grid blanking also provides the appropriate G1 bias and brightness control. Finally to DC restore the video signal at the preamplifier section, a back porch clamp signal is required. The back porch clamp pulse generator generates the back porch clamp signal from the externally supplied H-sync signal.

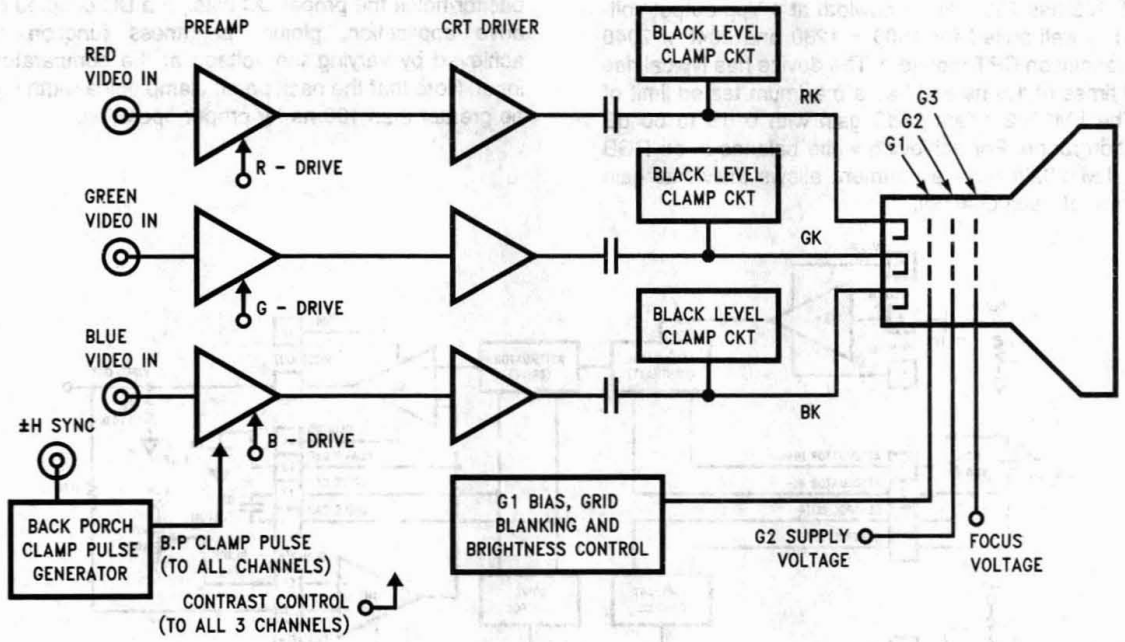

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FIGURE 2. System Block Diagram of Video Section

DESIGNING THE PREAMPLIFIER SECTION

PREAMPLIFIER SELECTION

LM1202 230 MHz VIDEO AMPLIFIER SYSTEM

- Video preamplifier for 1600 x 1200 and 2048 x 2048 display resolution
- Single channel CRT video preamplifier
- Includes DC restoration of video signal
- Includes drive adjustment for use in RGB systems
- Can parallel three LM1202s for optimum contrast tracking in RGB systems
- 0V–4V DC control of contrast, drive and brightness.

The LM1202 is a single channel high frequency video amplifier system designed for use in high resolution monochrome or RGB monitors. The device includes contrast, brightness, drive controls and DC restoration circuitry for black level clamping. All DC controls operate from 0V to 4V range for easy interface to bus controlled alignment systems. Three LM1202s can be paralled so that one IC provides master contrast control thus achieving better than 0.1 dB contrast tracking in RGB systems.

LM1202—KEY SPECIFICATIONS

- 230 MHz large signal bandwidth (at V_O = 4 V_{PP})
- 1.5 ns rise/fall times
- 26 dB gain with 0 db to 60 dB attenuation range
- ±3 dB drive adjustment range

The LM1202 has 230 MHz bandwidth at 4 V_{PP} output voltage and is well suited for 1600 x 1280 and 2048 x 2048 display resolution CRT monitors. The device has typical rise and fall times of 1.5 ns and has a maximum tested limit of 2 ns. The LM1202 offers 26dB gain with 0 dB to 60 dB attenuation range. For achieving white balance in an RGB system, LM1202's drive adjustment allows individual gain adjustment of each channel.

A block diagram of the LM1202 video amplifier is shown in *Figure 3*. Contrast control is a DC-operated attenuator which varies the AC gain of the amplifier. Signal attenuation (contrast) is achieved by varying the base drive to a differential pair and thereby unbalancing the current through the differential pair. Pin 20 provides a 5.3V bias voltage for the positive input of the attenuator (pin 1). Pin 3 provides a control voltage for the negative input (pin 2) of the attenuator. The voltage at pin 3 varies as the voltage at the contrast control input (pin 8) varies thus providing signal attenuation. The gain is maximum (0 dB attenuation) if the voltage at pin 8 is 4V and is minimum (maximum attenuation) if the voltage at pin 8 is 0V. The 0V to 4V DC-operated drive control at pin 9 provides a 6 dB gain adjustment range. This feature is necessary for RGB applications where independant adjustment of each channel is required.

The brightness or black level clamping requires a "sample and hold" circuit which holds the DC bias of the video amplifier constant during the black level reference portion of the video waveform. Black level clamping, often referred to as DC restoration is accomplished by applying a back porch clamp signal to the clamp gate input pin (pin 14). The clamp comparator is enabled when the clamp signal goes low during the black level reference period. When the clamp comparator is enabled, the clamp capacitor connected to pin 12 is either charged or discharged until the voltage at the minus input of the comparator matches the voltage set at the plus input of the comparator. During the video portion of the signal, the clamp comparator is disabled and the clamp capacitor holds the proper DC bias. In a DC coupled cathode drive application, picture brightness function can be achieved by varying the voltage at the comparator's plus input. Note that the back porch clamp pulse width (t_W) must be greater than 100 ns for proper operation.

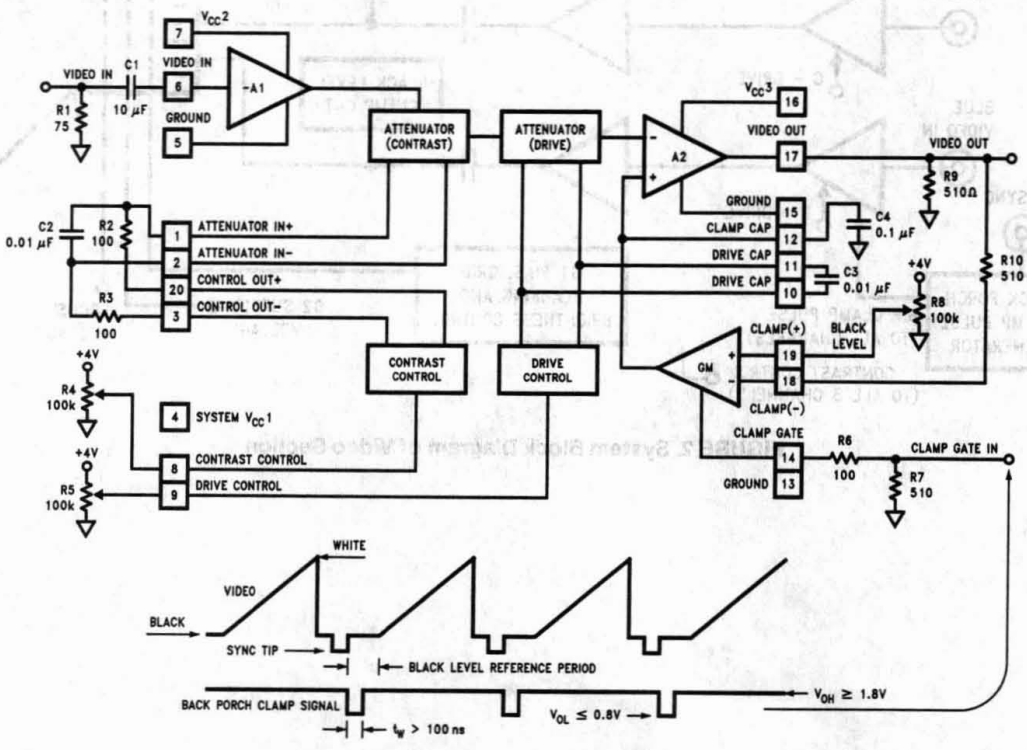

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FIGURE 3. LM1202 Block Diagram

Figure 4 shows a typical application for a single video channel. The video signal is AC coupled to pin 6. The LM1202 internally biases the video signal to 2.6 V_{DC}. Contrast control is achieved by applying a 0V to 4V DC voltage at pin 8. The amplifiers gain is minimum (i.e maximum signal attenuation) if pin 8 is at 0V and is maximum if pin 8 is at 4V. With pin 9 (drive control) at 0V, the amplifier has a maximum gain of 10.

For DC restoration, a clamp signal must be applied to the clamp gate input (pin 14). The clamp signal should be logic low (less than 0.8V) only during the back porch (black level reference period) interval. The clamp gate input is TTL compatible. Brightness control is provided by applying a 0V to 4V DC voltage at pin 19. For example, if pin 19 is biased at 1V then the video signal's black level will be clamped at 1V. A 510Ω load resistor is connected from the video output pin (pin 17) to ground. This resistor biases the emitter follower output stage of the amplifier. For power dissipation considerations, the load resistor should not be much less than 510Ω.

The complete RGB video preamplifier section is shown on in *Figure 5*. Note that pins 1 and 2 of IC1 are connected to pins 1 and 2 of IC2 and IC3 respectively. This allows IC1 to provide a master contrast control and optimum contrast tracking. Adjusting the contrast voltage at pin 8 of IC1 will vary the gain of all three video channels simultaneously. Drive control input (pin 9) of each LM1202 allows individual gain adjustment for achieving white balance.

The black level of each video channel can be individually adjusted to the desired voltage by adjusting the voltage at pin 19. In a DC coupled cathode drive application, adjusting the voltage at pin 19 of each IC will provide cutoff adjustment. In an AC coupled cathode drive application, the video signal is AC coupled and DC restored at the cathode. In such an application, the video signal's black level may be clamped to the desired level by simply biasing pin 19 using a voltage divider.

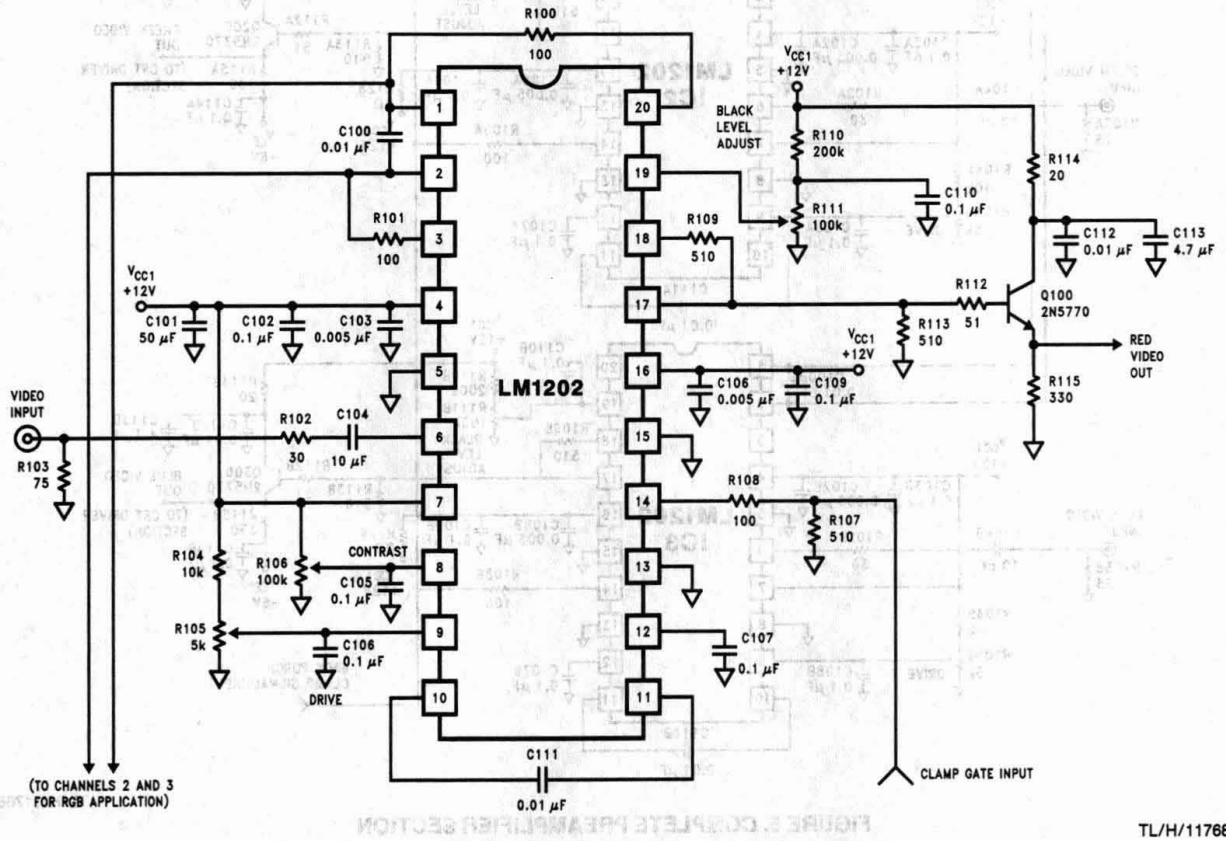

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FIGURE 4. LM1202 Connection Diagram For Single Channel Application

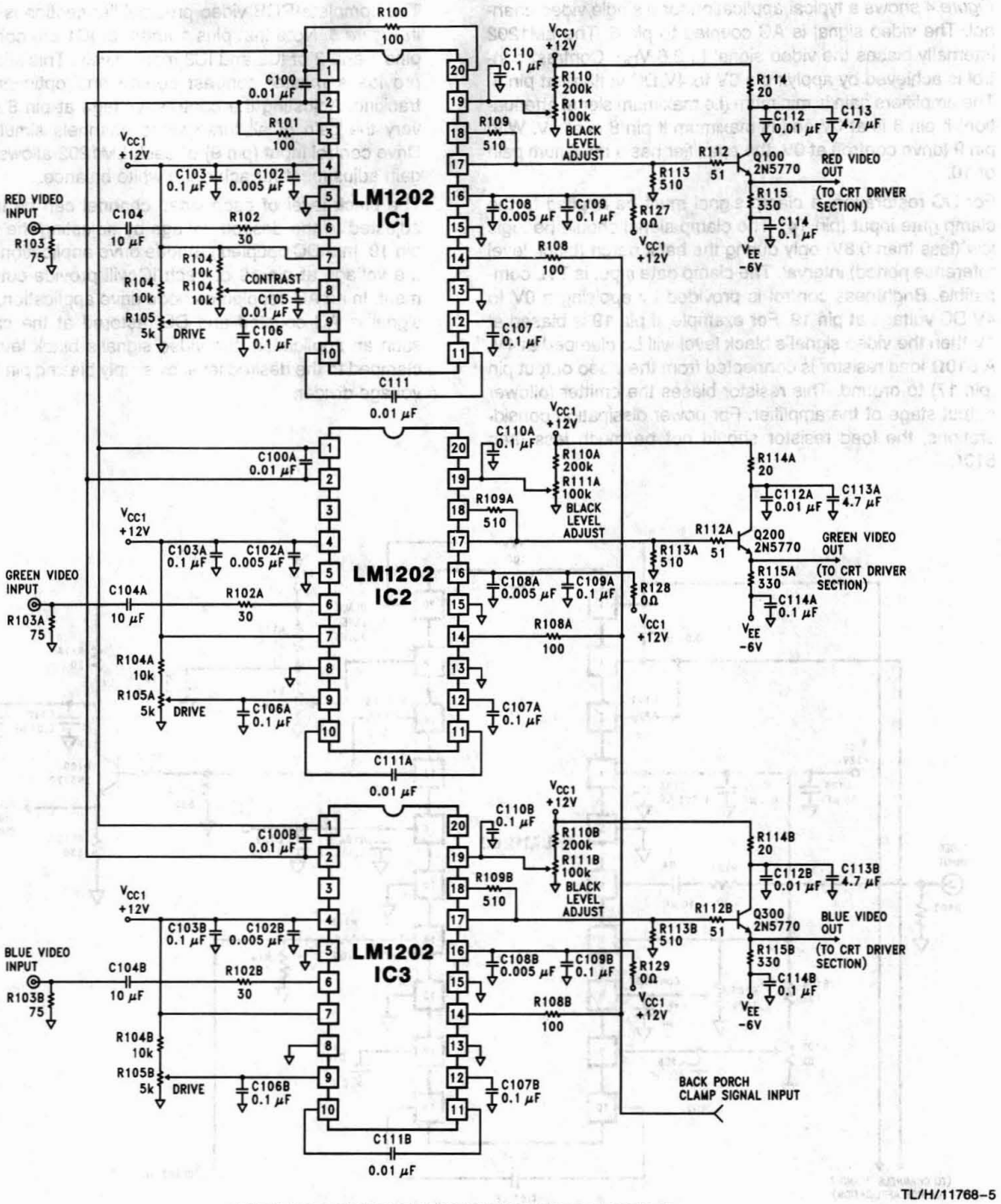

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FIGURE 5. COMPLETE PREAMPLIFIER SECTION

DESIGNING THE CRT DRIVER SECTION

CRT DRIVER SELECTION

LH2424 175 MHz CRT Driver

- CRT driver for 1600 x 1200 and 2048 x 1536 display resolution
- Single channel CRT driver
- Closed loop transimpedance amplifier
- Internal feedback resistor

Having completed the design of the preamplifier section, we can start designing the CRT driver section. The LH2424 was selected because of its 175 MHz bandwidth, low cost and ease of use. Moreover, the LH2424 is pin and function compatible with similar drivers from Motorola and Philips. The LH2424 is a transimpedance amplifier with an internal feedback resistor. One external resistor connected in series with the input accomplishes the task of voltage to voltage gain.

LH2424—KEY SPECIFICATIONS

- 175 MHz large signal bandwidth (at V_O = 40 V_{PP})
- 2 ns rise and fall times
- Voltage gain of −13
- Output can swing 50 V_{PP} (at V+ = 60V)

LH2424's 2 ns rise and fall times and 175 MHz bandwidth at 40 V_{PP} output voltage makes the device very suitable for our design. When coupled with the LM1202 (1.5 ns rise/fall times), the theoretical rise/fall time for the system is 2.5 ns and is well within our design objectives.

A simplified schematic of the LH2424 is shown in *Figure 6*. Resistors R1 and R2 set up the bias voltage at the base of Q1, giving rise to 1.2V drop across R3 when V_+ = +60V. With V_+ fixed at +60V, Q1 acts as a constant current source thus developing 1.2V across R5. The quiescent bias voltage at the base of Q2 is therefore approximately 1.7V, the measured value is closer to 1.6V. The 1.6V DC bias at the base of Q2 appears across R_B and causes 9.7 mA current to flow through R_F. If pin 1 is open circuit, 9.7 mA flowing through R_F causes the quiescent output voltage to be approximately 30V, thus biasing the output at one half the supply voltage. It can be easily shown that for any supply voltage the circuit output is biased at one half the supply voltage when pin 1 is open circuit.

Connecting a gain setting resistor, R_G in series with the input signal, V_{IN} and pin 1 accomplishes the task of voltage to voltage gain. If V_{IN} = 1.6V, the voltage across R_G is 0V and V_{OUT} = 30V. As the input voltage changes relative to the 1.6V DC bias, current is injected into the summing node (inverting input, pin 1) and flows entirely through the feedback resistor R_F because the current through R_B remains unchanged due to the fixed 1.6V DC bias voltage impressed across R_B. A current change of ±6.67 mA at the summing node causes the amplifier's output to swing ±20V from its quiescent output DC voltage of 30V. Thus when operating from V+ = 60V, the input signal should be referenced to 1.6V DC. The amplifier's AC gain is given by, $A_V = -R_F/R_G$.

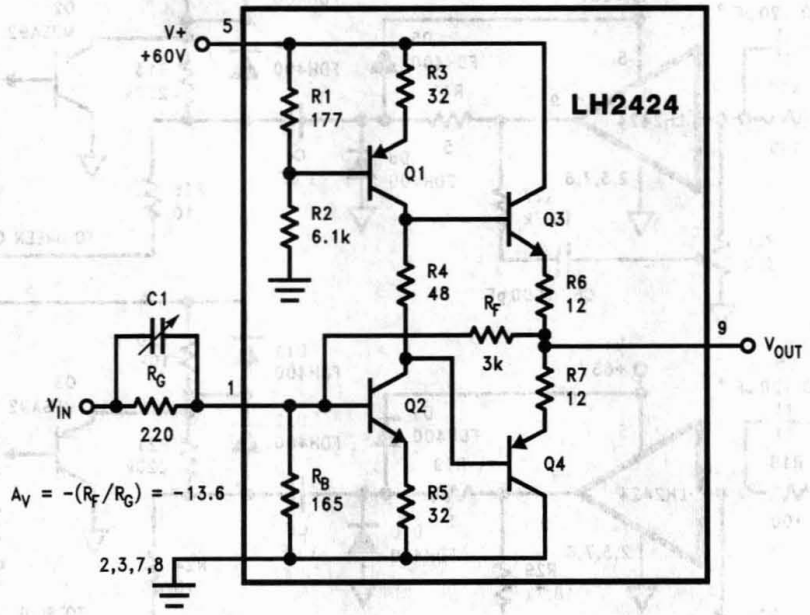

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FIGURE 6. Simplified Schematic of LH2424 CRT Driver

Figure 7 shows the schematic of the complete CRT driver section. Total series input resistance of 150Ω and LH2424's internal 3k feedback resistor configure the amplifier for a gain of −20. A peaking capacitor, for example C1 for the red video channel, is connected across the 100Ω input resistor. At high frequencies, C1 bypasses the 100Ω resistor, R2, and significantly increases the amplifier's closed loop gain thus causing high frequency peaking. Initially for prototype design, a 10 pF–120 pF variable capacitor can be selected for C1, C3 and C5. By varying the value of the peaking capacitor, the pulse response at the output of the LH2424 can be optimized for fast rise/fall time and low overshoot. Once the design is optimized, the value of the variable capacitor is measured and the capacitor is replaced with a fixed capacitor of measured value.

The LH2424's pulse response exhibits a low frequency tilt. This low frequency tilt causes picture smearing on the screen and can be observed by displaying a black box on a white background. The low frequency tilt is caused by thermal drift internal to the LH2424 and can be eliminated by feeding back a portion of the output signal back to the amplifier's input. As shown for the red video channel, R25, C7 and R26 accomplish the task of tilt compensation. One way to compensate all three channels is to display red, green and blue horizontal bars on a white background and adjust R26, R28 and R30 until picture smearing is eliminated.

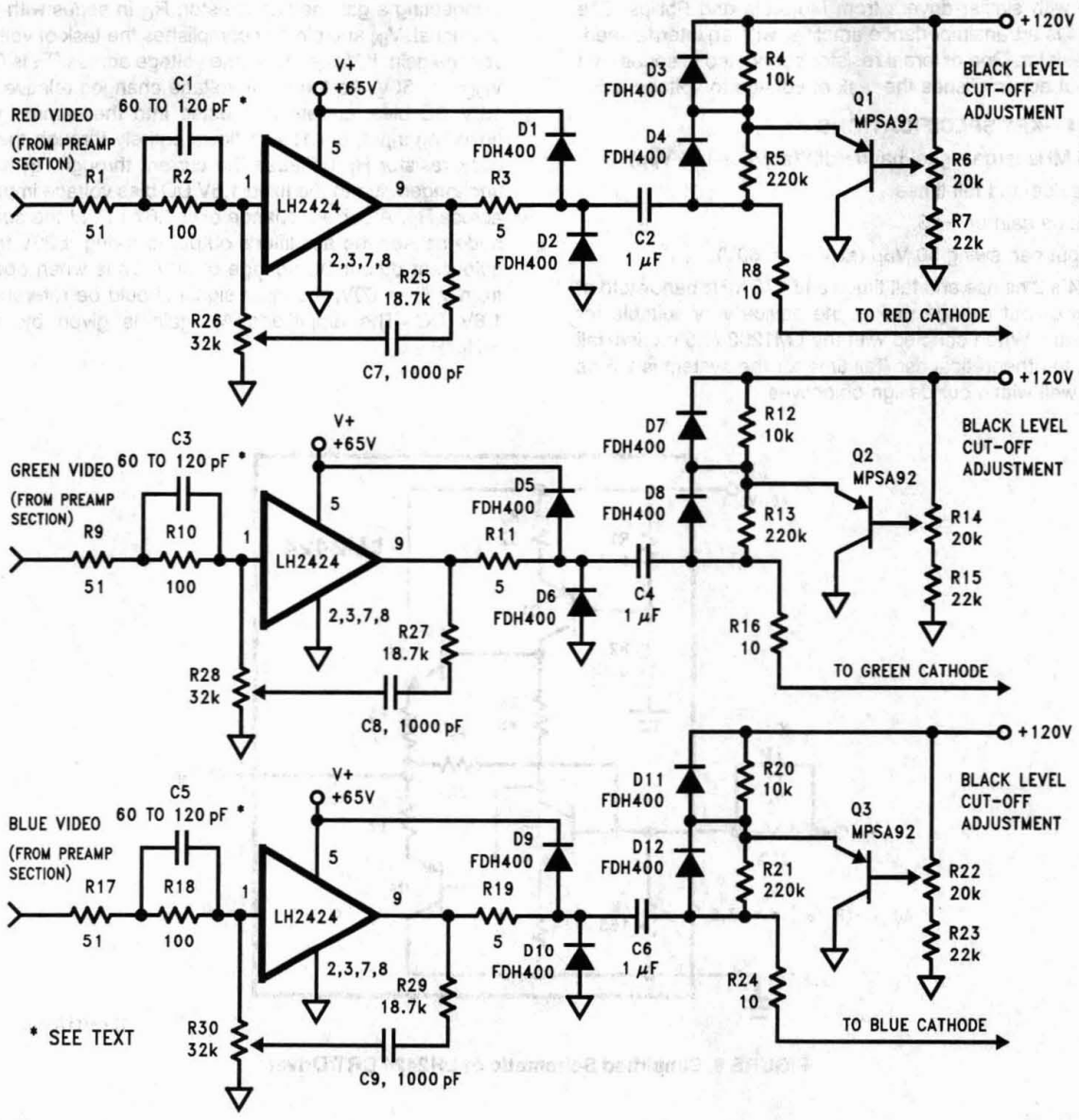

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FIGURE 7. COMPLETE CRT DRIVER SECTION

As the bandwidth of the driver amplifier is increased, it becomes more difficult to maintain high breakdown voltages. Although the video preamplifiers can provide full black level DC restoration, at high resolutions it may become more appropriate to consider AC coupling to the cathode. With AC coupling the CRT driver amplifier does not have to have a supply voltage rating high enough to accommodate the DC offsets required for individual gun matching. *Figure 8* shows the LH2424 operated from a 65V supply, whereas the AC coupled cathode is operated from a 120V supply, leaving a much larger voltage range for DC offset adjustment. A 1 μF capacitor couples the signal to the cathode. To restore the DC at the cathode, the MPSA92 high voltage transistor and the diode D4 clamp the peak signal voltage (i.e., black level or sync tip level) on the cathode side of the capacitor to 1.4V above the voltage set by the cut-off adjustment potentiometer. For arc-over protection, the second diode D3 prevents the transistor emitter from being pulled more than 0.7V above the 120V supply.

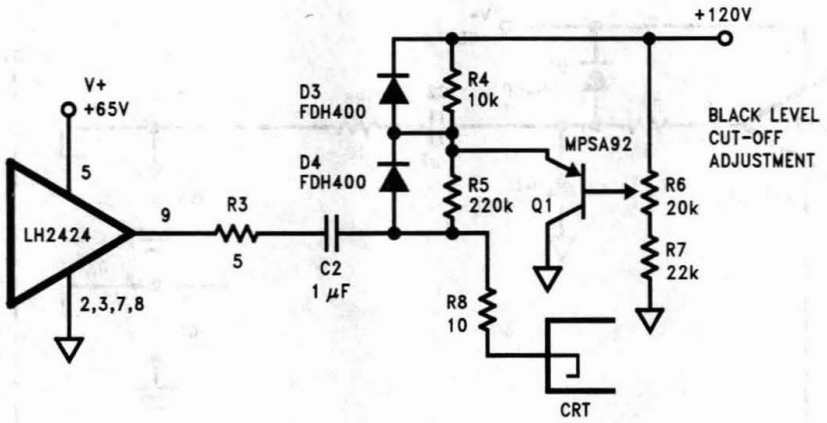

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FIGURE 8. AC Cathode Drive with Black Level Clamping

The high voltage differences between the anode of the CRT and the gun grids can often lead to arc-overs or highly destructive voltages being present on circuit elements connected to the CRT. To limit the potential arc-over voltage, spark gaps are connected from the cathodes and the grids to ground (see *Figure 9*). Even with the spark gaps, the arc-over voltage may be too high for the CRT driver. For added protection, clamp diodes are added to the driver outputs. These diodes should have a high peak current capability, low series impedance and a low shunt capacitance for them to be effective. Adding the 5Ω and 10Ω series resistors will help limit the arc-over current but this extra resistance will contribute to slower rise-times. The rise time can be improved by series peaking. A small inductor in series with the cathode can improve rise times at the expense of introducing more overshoot into the signal. The actual inductor value is selected empirically to get the best compromise between overshoot and rise time, 50 nH is a good starting value. To further protect the low voltage circuitry on the video board from high arc-over current, a small isolation resistor of value 10Ω to 100Ω is used to isolate the circuit ground from the CRT/arc ground.

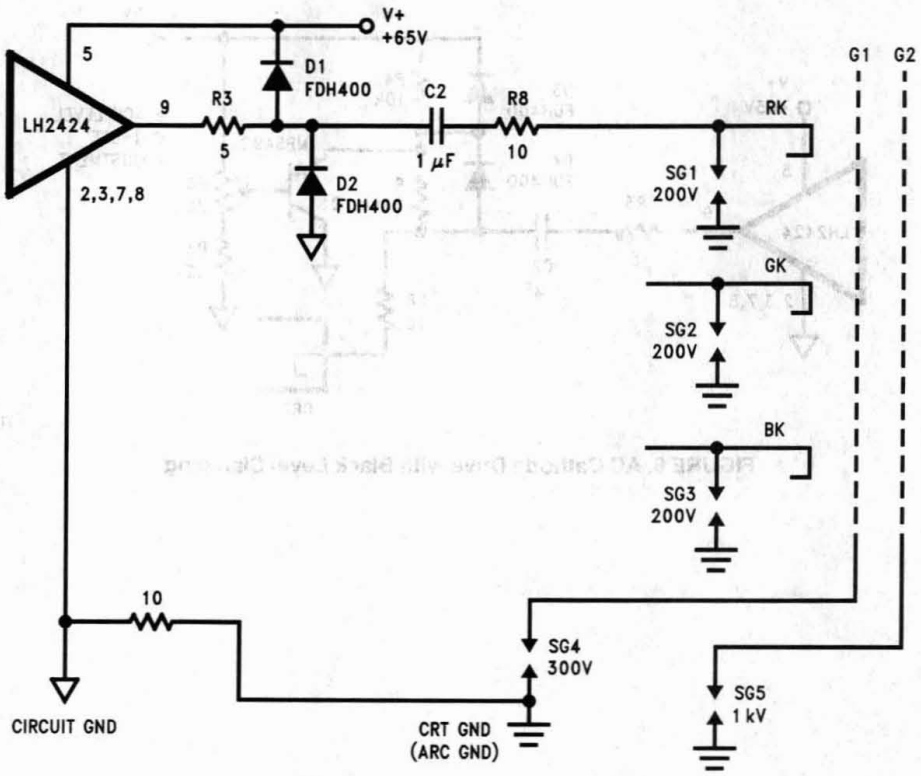

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FIGURE 9. ARC Protection

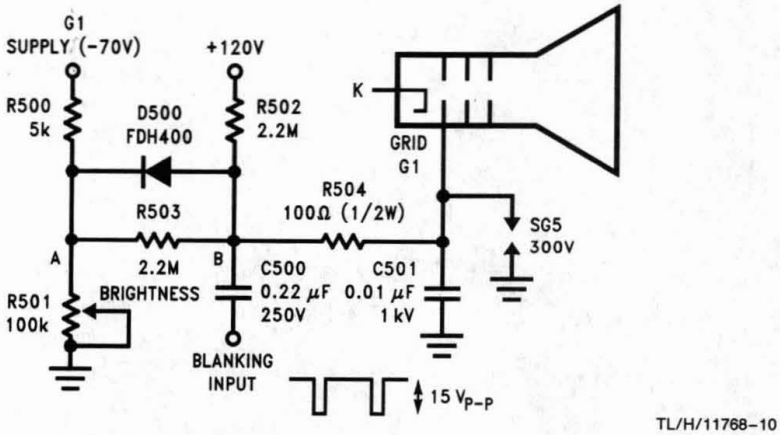

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FIGURE 10. CRT Grid Blanking and Brightness Control

The circuit used to accomplish blanking is shown in *Figure 10*. A negative voltage is applied to grid G1 using the resistor divider comprised of R500 and R501. Brightness control is achieved by varying the bias at G1 using potentiometer R501. Blanking at the grid is accomplished by R502, R503, D500 and C500. Resistor R502 biases the clamp diode D500. A 15 V_{PP} blanking signal is AC coupled through C500. Since the voltage at node "B" can not go more than one diode drop above the voltage at node "A" the blanking signal at G1 is clamped at the G1 bias voltage. During the blanking portion of the video signal, the blanking signal goes low thus reverse biasing D500 and pulling G1 15V negative with respect to its normal bias voltage. This action cuts off the CRT's beam current during the blanking interval and accomplishes blanking.

A versatile back porch clamp generator circuit is shown in *Figure 11*. A quad Exclusive-OR gate (MM74HC86) is used to generate the back porch clamp signal from the composite H-sync input signal. The composite H-sync input signal may have either positive or negative polarity. The logic level at pin 11 (Flag out) indicates the polarity of the H-sync signal applied to the clamp generator. The Flag output is a logic low (less than 0.8V) if the H-sync input signal has a negative polarity and is a logic high (greater than 2.4V) if the H-sync input signal has a positive polarity.

Regardless of the H-sync input signal's polarity, a negative polarity H-sync signal is output at pin 8. Furthermore, a negative polarity back porch clamp pulse is output at pin 3. The width of the back porch clamp pulse is determined by the time constant due to R28 and C12. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R28 or C12 or both. Note that an MM74C86 Exclusive-OR gate may also be used, however, the pin out is different than that of the MM74HC86.

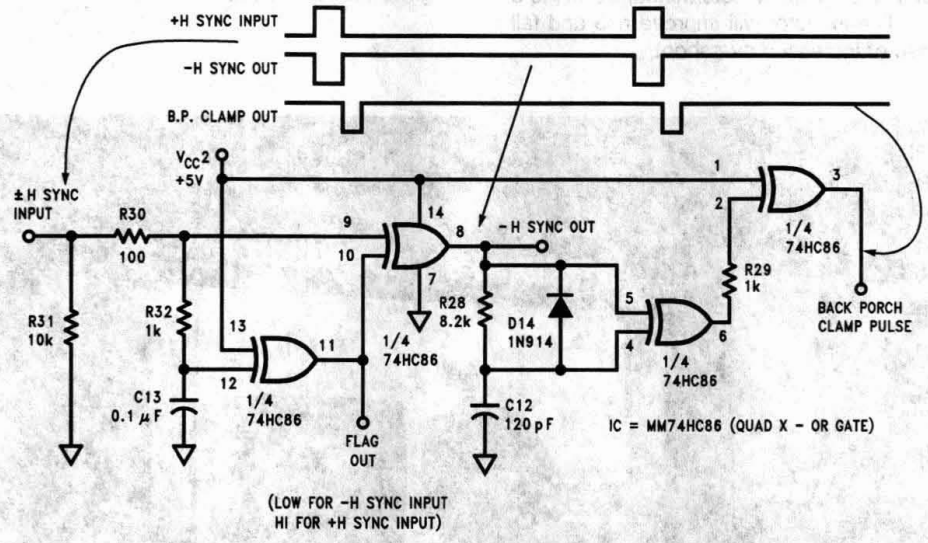

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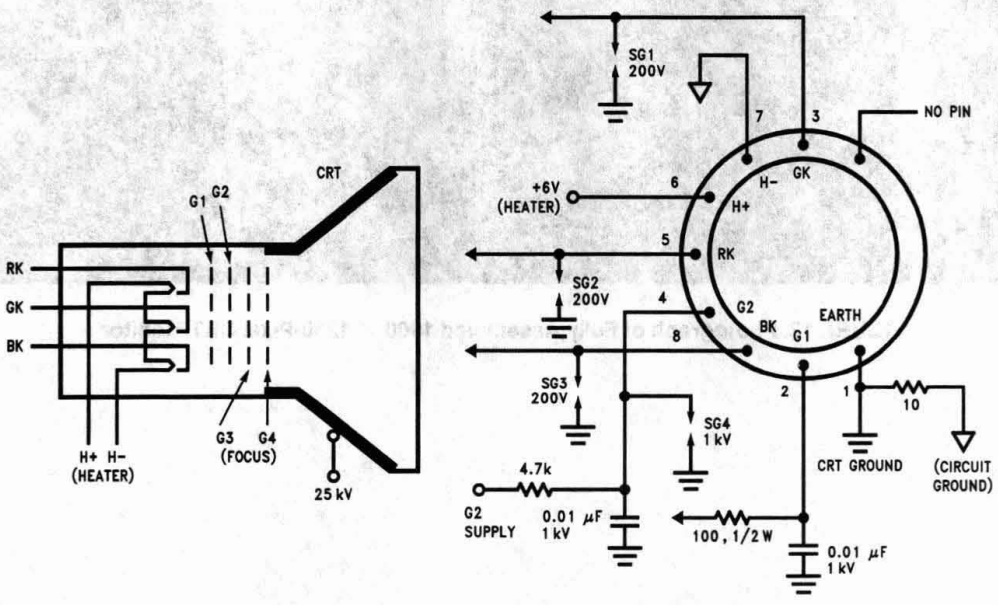
FIGURE 11. Back Porch Clamp Pulse Generator



CRT Socket: Hosiden HPS0380

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FIGURE 12. CRT Socket Connection

A typical connection diagram for the CRT socket is shown in *Figure 12*. Note that pinout for the socket may be different depending on the CRT tube used.

A photograph of the fully assembled 1600 × 1280-pixel color CRT monitor is shown in *Figure 13*. The viewable screen size is 27" with 0.37 mm dot pitch. The horizontal and vertical scan rates are 74 kHz and 60 Hz respectively. The monitor weighs 110 lbs.

MEASURED DATA

Response at cathode:
t_R = 3.5 ns
t_F = 3.4 ns
Overshoot = 0.4V
Undershoot = 0V
Settling time (±5%) = 12 ns

Sub 3 ns rise and fall times can be achieved by including an inductor in series with the output of the CRT driver. The value of the inductor is empirically determined, 50 nH is a good starting value. The inductor will improve rise and fall times at the expense of increased overshoot.

ADDITIONAL READING:

1. Grob, Bernard, "Basic Television and Video Systems," (5th edition), McGraw Hill, N.Y., 1984.
2. Rahim, Zahid, "Understanding the operation of a CRT monitor," Application Note 656, National Semiconductor Corp., Nov, 1989.
3. ———, "110 MHz CRT video amplifier fulfills demands of high resolution monitors," Application Note 598, National Semiconductor Corp., April, 1989.
4. ——— "Guide to CRT video design," Application Note 861, National Semiconductor Corp.
5. LM1202 data sheet, National Semiconductor Corp.
6. LH2424 data sheet, National Semiconductor Corp.

ACKNOWLEDGEMENTS:

The author would like to acknowledge Ron Page (National Semiconductor Corp.) for designing the back porch clamp generator circuit shown in *Figure 11*.

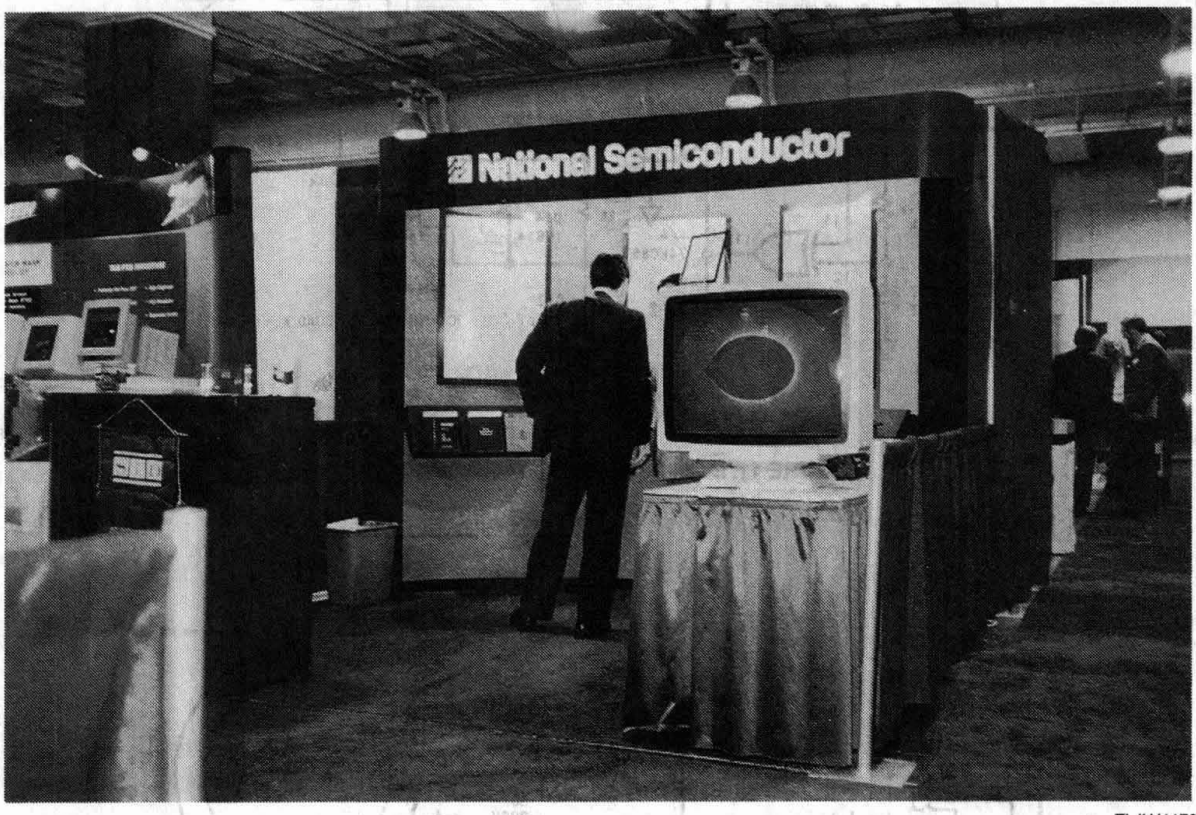

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FIGURE 13. Photograph of Fully Assembled 1600 × 1280-Pixel CRT Monitor

Audio Amplifiers Utilizing: SPiKe™ Protection

National Semiconductor
Application Note 898
John DeCelles

INTRODUCTION

As technology develops, integrated circuits continue to provide an advantage to consumers requiring products with more functionality and reliability for their money. It's been less than fifty years since the first transistor began to provide audio amplification to consumers. Technology changed, bringing to the market higher power discretes and hybrids with the later development of lower powered monolithics. Today with the development of IC technologies, high-performance monolithic audio amplifiers arrive, allowing consumers to experience high-power, high-fidelity audio systems in compact packages.

The **Overture™** Audio Power Amplifier Series possesses a unique protection system that saves audio amplifier designers components, size, and cost of their systems. This translates into higher-power, more functional, more reliable, compact audio amplification systems.

These advantages, generally provided only in high-end discrete amplifiers, are accomplished by providing a protection mechanism within a monolithic power package. Since audio amplifier designers generally need to provide some sort of protection to the output transistors in order to keep product failures to a minimum, National Semiconductor's Audio Group has designed SPiKe (Self Peak Instantaneous Temperature (°Ke)) Protection. This is a protection mechanism designed to safeguard the amplifier's output from overvoltages, undervoltages, shorts to ground or to the supplies, thermal runaway, and instantaneous temperature peaks.

The following pages will explain in detail each of the protections provided by SPiKe protected audio amplifiers, the advantages they bring to audio designers, and why they are necessary.

Each of the protection sections on the following pages will refer to *Figure 1.* (Amplifier Equivalent Schematic with Simplified SPiKe Protection Circuitry) when its functionality is described.

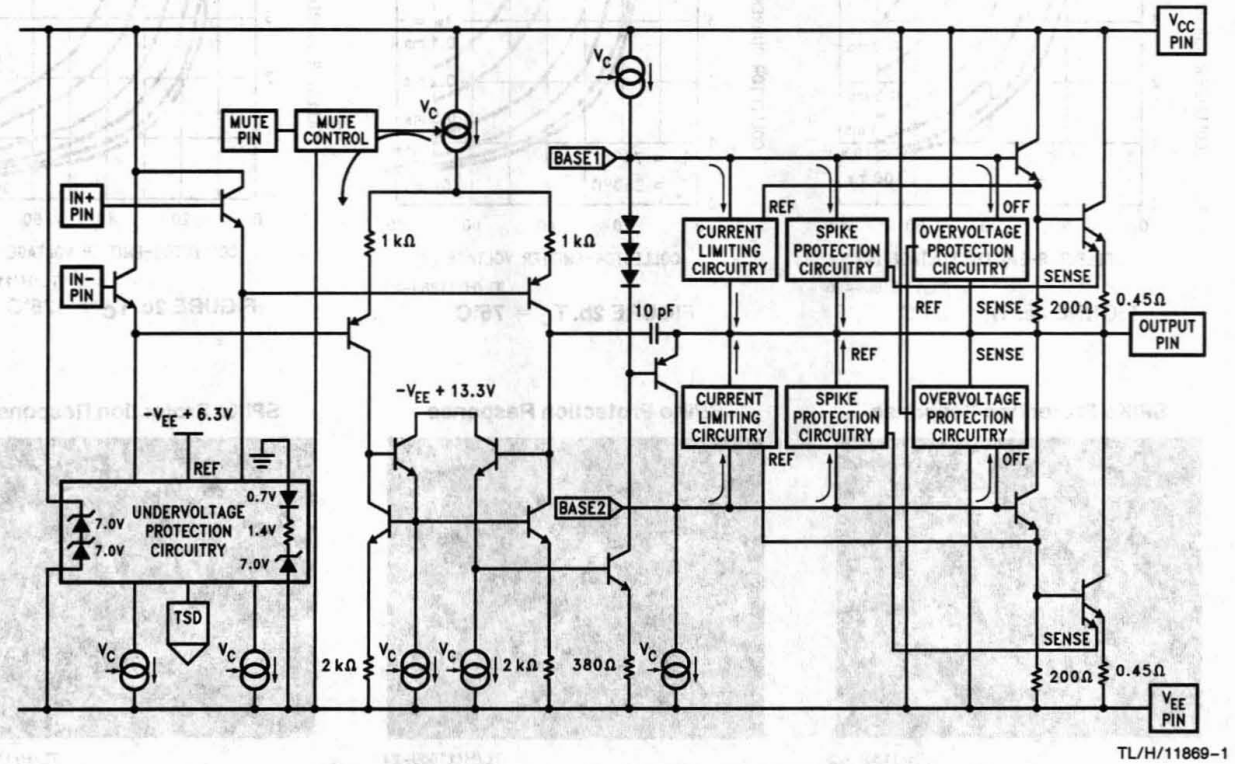

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FIGURE 1. Amplifier Equivalent Schematic with Simplified SPiKe Protection Circuitry

SELF PEAK INSTANTANEOUS TEMPERATURE LIMITING (SPiKe)

SPiKe Protection is a "uniquely-smart" protection mechanism that will adjust its output drive capability according to its output operating conditions, thus safeguarding itself against the most stringent power limiting conditions.

Other power amplifiers on the market provide SOA protection by calculating external resistances for adjustable current limiting whose primary function is to keep the amplifier within its safe operating area. Not only do these amplifiers require external components, but they aiso have a design conflict between fault protection and maximum output current drive capability. In order to keep the device from self-destructing against output shorts to either supply rail, the adjustable current limit must be significantly lowered, thus limiting the device's current drive capability.

SPiKe protected audio amplifiers provide extensive fault protection without sacrificing output current drive capability. Its circuitry functions by sensing the output transistor's temperature, enabling itself when the temperature reaches approximately 250°C. Depending upon the amplifier's present operating conditions, the device will reduce the output drive transistor's base current, as shown in *Figure 1*, keeping the transistor within its safe operating area.

The uniqueness of SPiKe protected audio amplifiers is its abillty to monitor the output drive transistor's safe operating area dynamically, regardless of an output to ground short, an output to supply short, or the reaching of its power limit by any pulse within the audio spectrum.

As can be seen from *Figures 2a–c*, the safe operating area is reduced for all pulse widths as the case temperature increases. This indicates that good heatsinking is required for optimal operation of the power amplifier. *Figures 3a–c* illustrate the reduction of the safe operating area by the increasing effect of enabling SPiKe Protection on a 100 Hz sine wave due to increasing case temperatures.

As seen in the Current Limiting section, a short to ground with an input pulse applied to the amplifier will be current limited by the conventional current limiting circuitry for a few hundred microseconds. When the junction temperature reaches its limit, SPiKe protection takes over, limiting the output current further, as the junction temperature tries to rise above 250°C.

This protection scheme results in the power capabilities being dependent upon the case temperature, the transistor operating voltages, V_{CE}, and the power dissipation versus time.

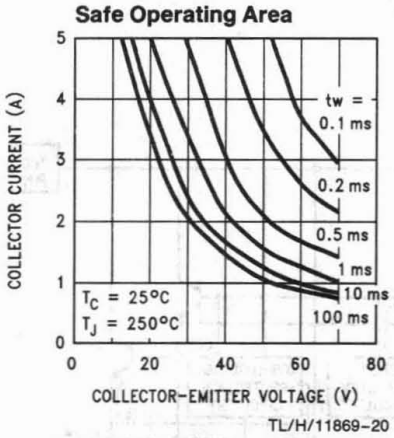

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FIGURE 2a. T_C = 25°C

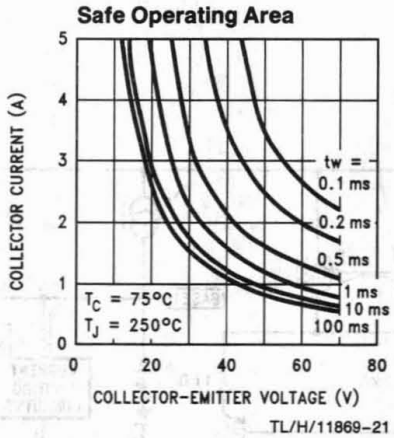

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FIGURE 2b. T_C = 75°C

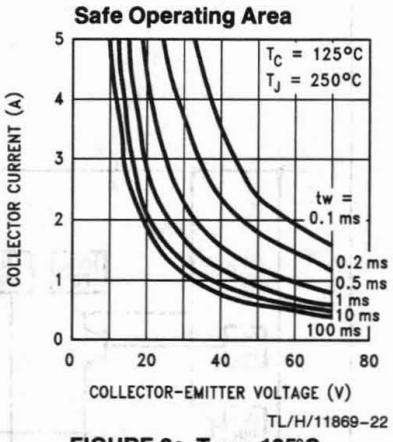

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FIGURE 2c. T_C = 125°C

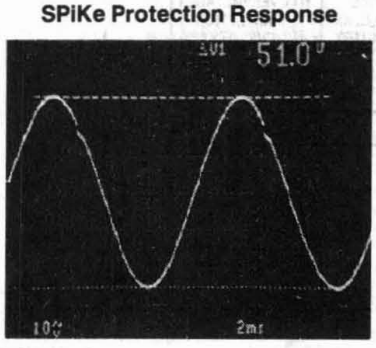

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FIGURE 3a. T_C = 75°C

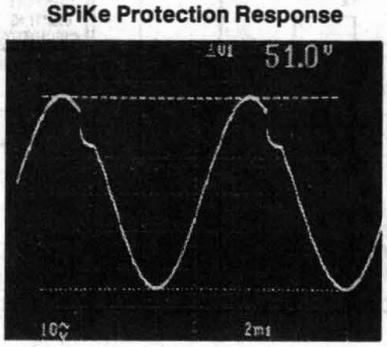

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FIGURE 3b. T_C = 80°C

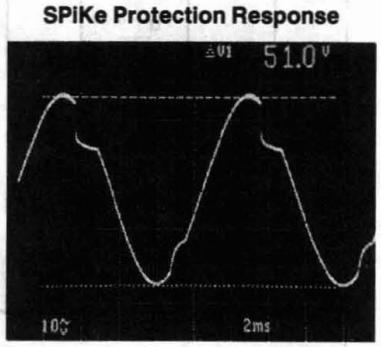

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FIGURE 3c. T_C = 85°C

Figures 4 and *5* are provided for each SPiKe Protected audio power amplifier and should be used to determine the power transistor's peak dissipation capabilities and the power required to activate the power limit. This information may help a designer to determine the maximum amount of power that SPiKe protected amplifiers may deliver into different loads before enabling SPiKe protection.

Figure 4 shows the peak power dissipation capabilities of the output drive transistor at increasing case temperatures for various output pulse widths.

Figure 5 shows the power required to activate SPiKe circuitry at increasing case temperatures over the operating voltage range.

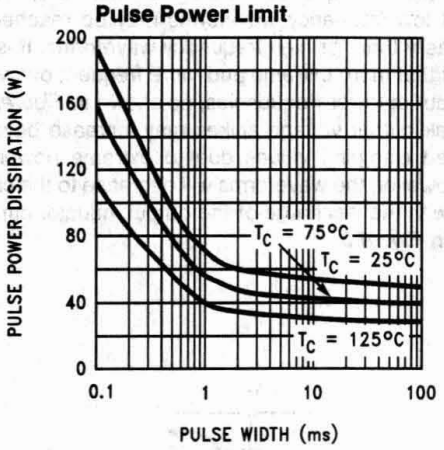

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FIGURE 4. Pulse Power Dissipation vs Pulse Width

Again, it is evident that good heatsinking and ventilation within the system are important to the design in order to achieve maximum output power from the amplifier.

SPiKe protected amplifiers provide the capability of regulating temperature peaks that may be caused by reaching the power limit of the safe operating area. The reaching of power limits may result from increased case temperatures while heavily driving a load or by conventional current limiting, resulting from the output being shorted to ground or to the supplies.

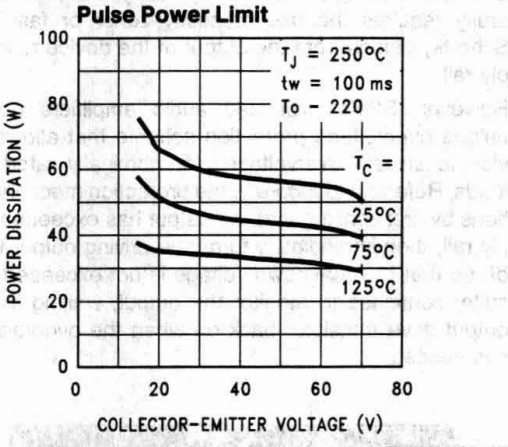

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FIGURE 5. Pulse Power Dissipation vs V_{CE}

OVERVOLTAGE—OUTPUT VOLTAGE CLAMPING

One of the most important protection schemes of an audio amplifier is the protection of the output drive transistors against large voltage flyback spikes. These spikes are created by the sudden attempt to change the current flow in an inductive load, such as a speaker. When a push-pull amplifier goes into power limit (i.e., reaching the SOA limit) while driving an inductive load, the current present in the inductor drives the output beyond the supplies. This large voltage spike may exceed the breakdown voltage rating of a typical audio amplifier and destroy the output drive transistor. In general, the amplifier should not be stressed beyond its *Absolute Maximum* (No Signal) Voltage Supply Rating and should be protected against any condition that may lead to this type of voltage stress level. This type of protection generally requires the use of costly zener or fast recovery Schottky diodes from the output of the device to each supply rail.

However, SPiKe protected audio amplifiers possess a unique overvoltage protection scheme that allows the device to sustain overvoltages for nominally rated speaker loads. Referring to *Figure 1*, the protection mechanism functions by first sensing that the output has exceeded the supply rail, then immediately turns the driving output transistor off so that its breakdown voltage is not exceeded. The circuitry continues to monitor the output, waiting to turn the output drive transistor back on when the overvoltage fault has ceased.

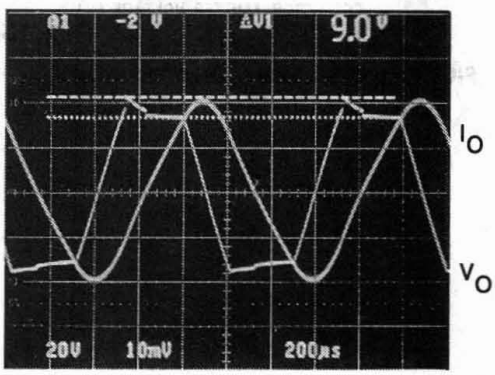

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FIGURE 6a. Positive Output Voltage Clamping Waveform

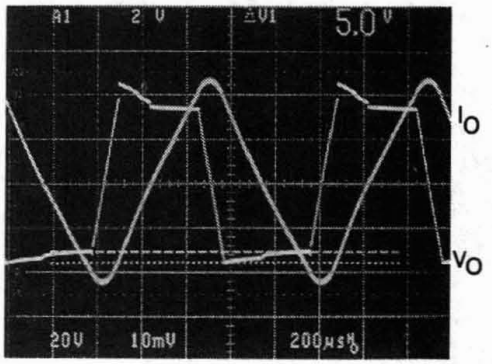

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FIGURE 6b. Negative Output Voltage Clamping Waveform

While monitoring the output, the IC also provides SPiKe protection if needed. Finally, SPiKe protected audio amplifiers possess an internal supply-clamping mechanism; a zener plus a diode drop from the output to the positive supply rail and an intrinsic diode drop from the output to the negative rail. This equates to clamping of approximately 8V on the positive rail and 0.8V on the negative rail as can be seen in *Figures 6a* and *6b*, respectively.

Figures 7a and *7b* model the output stage for each overvoltage condition exemplifying how the voltage waveforms are clamped to their respective values for high frequency waveforms. As shown in the Self Peak Instantaneous Temperature Limiting (SPiKe) section, *Figures 2a–c*, the safe operating area for lower frequency waveforms is much smaller than for higher frequency waveforms. Therefore, the power limits of low frequency waveforms may be reached much more easily than for high frequency waveforms. It is due to this fact that more extreme and more frequent overvoltages may occur at lower frequencies, as shown in *Figures 8–11*. The peak output voltage spikes may increase beyond the described clamping values due to extreme power conditions, however, the waveforms will decrease to the clamping values with the discharge of the output inductor current, as shown in *Figure 8*.

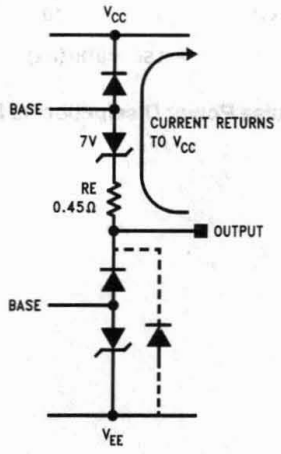

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FIGURE 7a. Output Stage Overvoltage Model (V_{CC})

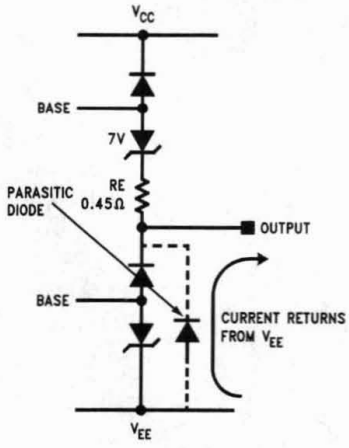

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FIGURE 7b. Output Stage Overvoltage Model ($-V_{EE}$)

The lower output stage has the advantage of an intrinsic diode from the negative rail to the output which can replace the usual external clamping diode in an audio amplifier. This intrinsic diode is an advantage of the monolithic IC, capable of handling the large current flowing through the load at the time of the power limit.

The system is not protected against all reactive loads since these clamping diodes will dissipate large amounts of power that cannot be controlled by the peak temperature limiting circuitry if the fault is sustained for a long period of time. It should also be noted that for purely reactive loads, all of the power is dissipated in the amplifier and none in the load. This implies that if the load is more reactive than resistive, at those frequencies, more power will be dissipated in the amplifier than delivered to the speaker. Since the impedance characteristics of a speaker change over frequency, it is very important to know what types of loads the amplifier can and cannot drive in order to not only match the amplifier and speaker for optimum performance, but also to protect the amplifier from trying to outperform itself. It is the mismatching of components or low dips in the resistive component of a complex speaker that can cause an amplifier to go into power limit. The likelihood of reaching the amplifier's power limit is greatly reduced when the minimum impedance that the amplifier can drive is known.

Figures 8–11 are examples of the LM3876 reaching its power limit, experiencing large flyback voltages from an inductive load, for various input signals and loads.

The test conditions for *Figures 8–11* are as follows:

— Using an LM3876
— No external compensation components
— $V_{CC} = \pm 35V$
— $Av_{CL} = 20$
— I_O/Div. = 2.0A/div
— Z_L = 7.5 mH + 4Ω for *Figure 8*
— Z_L = 7.5 mH + 2Ω for *Figures 9–11*
— f = 100 Hz for *Figures 8, 9,* and *11*
— f = 70 Hz for *Figure 10*

In *Figure 8,* the 4.5Vpk input signal applied to the amplifier with a closed-loop gain of 20, produces the severely clipped 34V output voltage waveform, as shown. The sharp 48.5V overvoltage spike that occurs at the crossover point is due to the amplifier output stage reaching the SOA (Safe Operating Area) limit. For this waveform, the collector-emitter voltage is quite large, while the output current is also quite large (4A). Referring to *Figures 2a–c*, it is easily understood that the SOA power limit has been reached.

When the SOA limit is reached, the SPiKe protection circuitry tries to limit the output current while the inductor tries to continuously supply the current it has stored. Since the current in an inductor can't change instantaneously, the current is driven back into the output up through the upper drive transistor, as shown in *Figure 7a.*

It is this current that causes the large flyback voltage spike on the output waveform. The peak of the voltage spike can be found by taking the current going through the output at the time of the power limit multiplied by the 0.45Ω emitter resistor and adding it to the zener-diode combination. In *Figure 6a* this would be (2A)(0.45Ω) + 8V which is approximately 9V, as shown by the cursors. For the lower output stage, the clamping voltage is controlled by an intrinsic diode that replaces costly output clamping diodes.

In *Figure 8,* when the current reaches close to zero, the voltage at the output tends to move towards the output voltage that it would have been if the power limit had not been reached. This is typical for all overvoltage occurrences. It should be noted that when the overvoltage fault occurs, the device is no longer functioning in the closed-loop mode.

In *Figure 9,* one waveform is actually a sinewave with SPiKe protection enabled, as in *Figures 3a–c*, with the same overvoltage spikes as in *Figure 8* and the other waveform is the output current. In the middle of the response, the current is rising toward 6A when SPiKe is enabled, causing a "bite" to be taken out of the sinewave. The device is just trying to limit the output current at this point, as explained in the SPiKe Protection section. The overvoltage flyback spike then occurs while the output current discharges to zero. However, this time when the current reaches zero, the current and voltage must make up for what it had lost and try to return to its position on the amplified input waveform. The voltage jumps up to its value, but the current must slowly and continuously charge up to its place on the current waveform, then continue downward as the lower output stage starts sinking current. It must be remembered that the current waveform would have been a sinewave if the SOA power limit hadn't been reached.

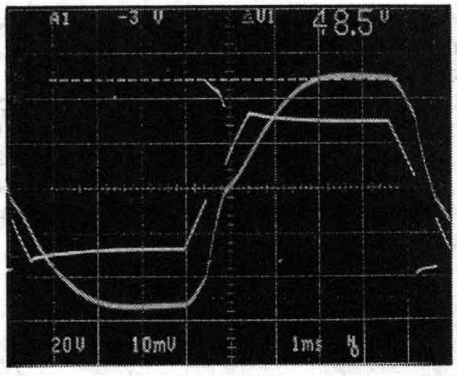

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FIGURE 8. Overvoltage Exceeding Clamping Level

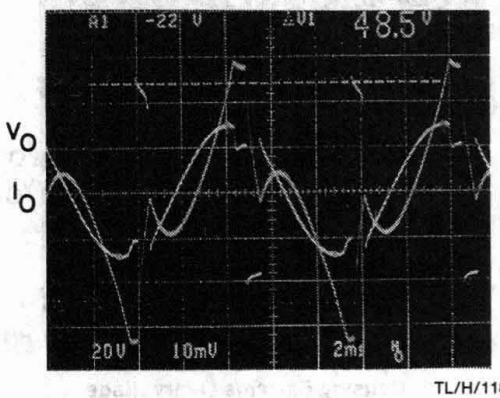

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FIGURE 9. Reaching the SOA Power Limit, f = 100 Hz, SPiKe Enabled

Multiple SOA power limits on the output waveform are the difference between *Figures 9* and *10. Figure 10* is intended to show that multiple SOA power limits can occur under extreme loading conditions. The amplifier is trying to drive a 70 Hz sinewave into a 7.5 mH inductor in series with a 2Ω resistor. As the signal frequency decreases, with a low resistance load, the number of SOA power limits will increase. The frequency of reaching power limits will depend upon the size of the reactance as the load.

Figure 11 is intended to exemplify the large current overdrive that can occur when the output waveform is driven hard into the rails. Notice that the current is over 6Apk for each voltage swing.

It must be remembered that it is the large voltage across the output drive transistors that would normally exceed a discrete output transistor's breakdown voltage. A discrete power transistor that is not protected with output clamping diodes would be destroyed if its breakdown voltage was exceeded. SPiKe protected audio amplifiers clearly show the ability to withstand overvoltages created by low impedance loads.

The integration of output overvoltage protection within monolithic audio amplifiers provides the advantage of eliminating expensive fast-recovery Schottky diodes that would be used in a discrete design, thus resulting in fewer external components and a lower system cost.

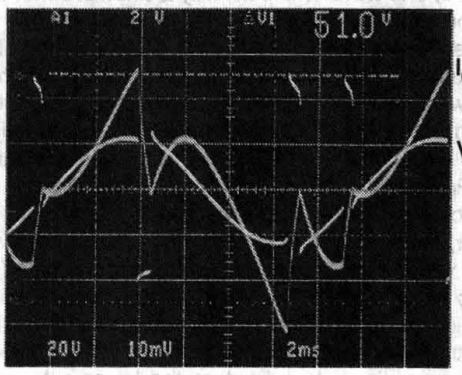

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FIGURE 10. Multiple SOA Power Limits

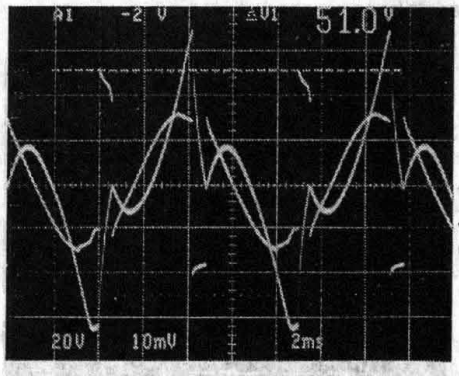

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FIGURE 11. Output Saturation Causing Extreme Overvoltage

UNDERVOLTAGE—POPLESS POWER-ON/OFF

SPiKe protected audio amplifiers possess a unique undervoltage protection circuit that eliminates the annoying and destructive pops that occur at the output of many amplifiers during power-up/down. SPiKe's undervoltage protection was designed because all DC voltage shifts or "pops" at the output should be avoided in any audio amplifier design, due to their destructive capability on a speaker. These pops are generally a result of the unstable nature of the output as internal biasing is established while the power supplies are coming up.

SPiKe Protection accomplishes this by disabling the output, placing it in a high impedance state, while its biasing is established. This function is achieved through the disabling of all current sources within the device as denoted by control signal V_C, in *Figure 1.* For the LM2876, LM3876, and LM3886, the control signal will not allow the current sources to function until 1) the total supply voltage, from the positive rail to the negative rail, is greater than 14V and 2) the negative voltage rail exceeds −9V. The LM3875 is undervoltage protected with the relative 14V total supply voltage condition only. Thus for the "6"-series, the amplifiers will not amplify audio signals until both of these conditions are met. It is this −9V protection that causes the undervoltage protection scheme to disable the output up to 18V between the positive and negative rail, assuming that both supply rails come up simultaneously. This can be seen in *Figure 12a.* The −9V undervoltage protection is ground referenced to eliminate the possibility of large voltage spikes, that occur on the supplies, which may enable the relative 14V undervoltage protection momentarily.

It should be noted that the isolation from the input to the output, when the output is in its high-impedance state, is dependent upon the interaction of external components and traces on the circuit board.

As can be seen in *Figures 12a* and *12b*, the transition from ground to $\pm V_{CC}$ and from $\pm V_{CC}$ to ground upon power-on/off is smooth and free of "pops". It can also be seen from the magnification of *Figure 12a* in *Figure 12c*, that the amplifier doesn't start amplifying the input signal until the supplies reach ±9V. It is also evident that there is no feedthrough from 0V to ±9V. It must be noted that the sinewave being amplified is clipped initially as the supplies are coming up, but after the supplies are at their full values, the output sinewave is actually below the clipping level of the amplifier.

It should also be noted that the waveforms were obtained with the mute pin of the LM3876 sourcing 0.5 mA, its 0 dB attenuation level. If the mute pin is sourcing less than 0.5 mA, the nonlinear attenuation curve may induce crossover distortion or signal clipping. The Mute Attenuation curves vs. Mute Current in the datasheets of the LM2876, LM3876, and LM3886 show this nonlinear characteristic. The LM3875 is the sister part to the LM3876 and does not have a mute function.

For optimum performance, the mute function should be either enabled or disabled upon power-up/down. Although the undervoltage protection circuitry is not dependent upon the mute pin and its external components, the mute function can be used in conjunction with the undervoltage function to provide a longer turn-on delay. It should be noted that the mute function is also popless. Of the multiple ways to set the mute current and utilize the mute function, the use of a regulator can continuously control the amount of current out of the mute pin. This regulation concept keeps the attenuation level from dropping below 0 dB when the supply is sagging. More information about mute circuit configurations will be provided later in a future application note.

The advantages of undervoltage protection in SPiKe protected audio amplifers are that no pops occur at the output upon power-up/down. Customers can also be assured that their speakers are protected against DC voltage spikes when the amplifier is turned on or off.

CURRENT LIMITING—OUTPUT SHORT TO GROUND

Whether in the lab or inside a consumer's home, the possibility of an amplifier output short to ground exists. If current limiting is not provided within the amplifier, the output drive transistors may be damaged. This means one of two things, either sending the unit to customer service for repair or if you're in the lab, throwing the discrete drive transistor or hybrid unit away and replacing it with a new one. SPiKe protected audio amplifiers eliminate this costly, time-consuming hassle by providing current limiting capability internally.

This also means that the multiple components required to provide current limiting capability in a discrete design are eliminated with the monolithic audio amplifier solution, once again, reducing the system size and cost.

The value of the current limit will vary for each particular audio amplifier and its output drive capability. Please refer to each amplifier's datasheet Electrical Characteristics section for particular current limits.

As can be seen in *Figure 13a*, the value of current limiting for the LM3876 is typically 6 Apk when $V_{CC} = \pm 35V$ and $R_L = 1\Omega$. From the scope cursors at the top of the waveform $I_{LIMIT} = Vo/R_L$. This test was performed with a closed-loop gain of 20 and an input signal of 2V (t_w = 10 ms).

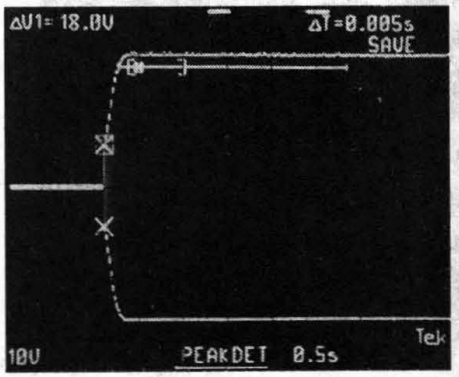

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FIGURE 12a. Output Waveform Resulting from Power-On Undervoltage Protection

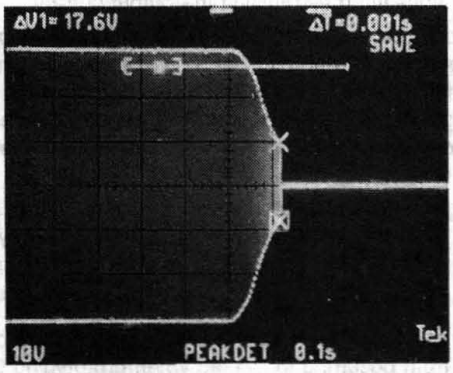

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FIGURE 12b. Output Waveform Resulting from Power-Off Undervoltage Protection

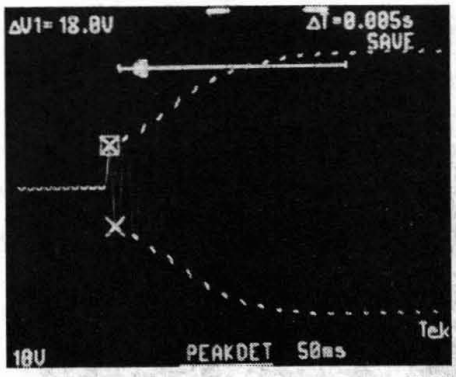

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FIGURE 12c. Output Waveform Resulting from Power-On Undervoltage Protection

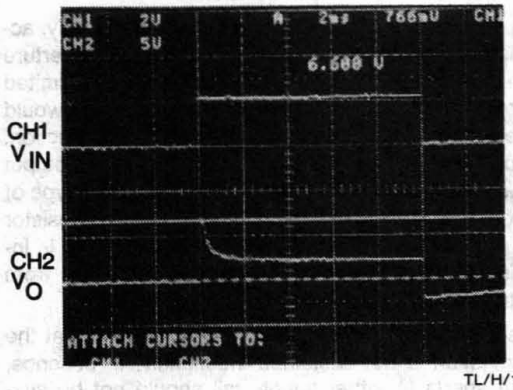

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FIGURE 13a. LM3876 Typical Current Limiting with SPiKe Protection ON

Notice that the initial current limit is at its peak value of approximately 6A, but as time increases, the final current limit decreases. This is due to the enabling of the instantaneous temperature limiting circuitry or SPiKe protection. When the IC is in current limiting, the temperature of the output drive transistor array increases to its limit of 250°C, at which time SPiKe protection is enabled, reducing the amount of output drive current. It is this further reduction of its drive current that prevents the output drive transistor from exceeding the safe operating area.

As shown in *Figures 13b–d*, as the input pulses' time increases, the level of SPiKe protection imposed on the waveform increases. It should be noted that SPiKe protection was enabled after 200 μs of current limiting in *Figures 13c* and *13d*, but is in general dependent upon the case temperature, the transistor operating current and voltage, and its power dissipation versus time.

The internal current limiting circuitry functions by monitoring the output drive transistor current. The sensing of an increase in this current signals the circuitry to pull away drive current from the base of the output drive transistor as shown in *Figure 1*. The harder the input tries to drive the output, the more current is pulled away from the output drive transistor, thus internally limiting the output current.

Another point worth mentioning is that with increasing supply voltages, the turn-on point of SPiKe protection, when in current limiting, will decrease. Since the internal power dissipation is greater, it will take a shorter amount of time before the temperature of the output drive transistor increases to the SOA limit.

Once again, SPiKe protected audio amplifiers save design time and external component count by integrating system solutions within the IC, translating into more cost reduction.

CURRENT LIMITING—OUTPUT SHORT TO SUPPLY

One feature of SPiKe Protection which can prevent costly mistakes from occurring in the lab when prototyping Overture audio amplifiers is its protection from output shorts to the supply rails. The device is protected from momentary shorts from the output to either supply rail by limiting the current flow through the output transistors.

Although accidents such as this one occur infrequently, accidents do happen and if one were to happen with Overture audio amplifiers they would be protected for a limited amount of time. Normally when an accident like this would occur in a discrete design with no current limiting protection, the output transistor would be subjected to the full output swing plus a large current draw from the supply. This type of stress would destroy an output stage discrete transistor whereas with SPiKe protected amplifiers, the current is internally limited, thus preventing its output transistors from being destroyed.

One note to make about this protection scheme is that the current limitation is not sustained indefinitely. In essence, the output shorts to either supply rail should not be sustained for any period of time greater than a few seconds. Frequent temporary shorts from the output to either supply rail will be protected, however, continued testing of the circuitry in this manner is not guaranteed and is likely to cause degradation to the functionality and long-term reliability of the device.

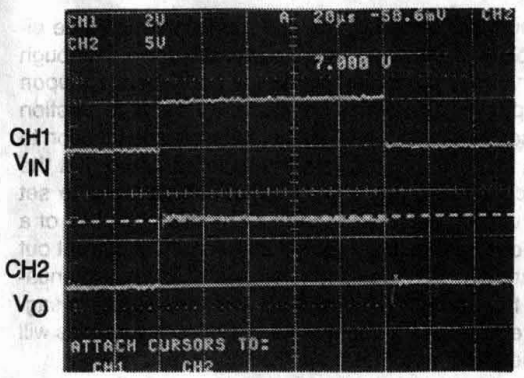

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FIGURE 13b. t_W = 100 μs, t_{SPIKe} (Not Enabled)

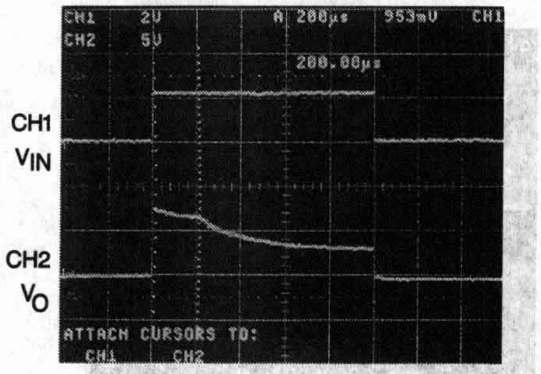

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FIGURE 13c. t_W = 1 ms, t_{SPIKe} = 200 μs

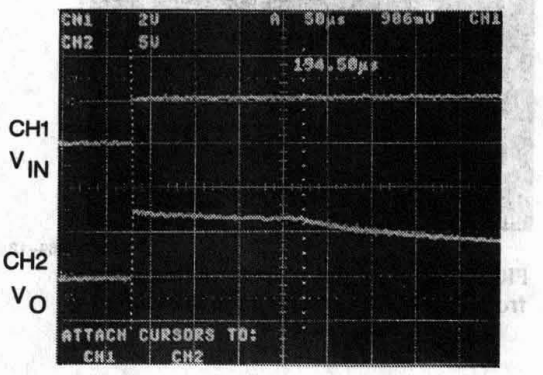

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FIGURE 13d. t_W = 10 ms, t_{SPIKe} = 195 μs

THERMAL SHUTDOWN—Continuous Temperature Rise

An audio system designer's design cycle time is reduced by eliminating the need for designing tricky thermal matching between discrete output transistors and their biasing counterparts which are physically located some distance from each other. Complex thermal sensing and control circuitry provided from the legendary Bob Widlar, and the ability of integrating it onto a monolithic amplifier, eliminates the external circuitry and long design time required in a discrete amplifier design.

SPiKe protected audio amplifiers are safeguarded from Thermal runaway, an area of concern for any complementary-symmetry amplifier. Thermal runaway is an excessive amount of heating and power dissipation of the output transistor from an increased collector current caused by the two complementary transistors not having the same characteristics or from an uncompensated V_{BE} being reduced by high temperatures.

If proper heatsinking is not utilized, the die will heat up due to the poor dissipation of power when the amplifier is being driven hard for a long period of time. Once the die reaches its upper temperature limit of approximately 165°C, the thermal shutdown protection circuitry is enabled, driving the output to ground. A pseudo "pop" at the output may occur when this point is reached, due to the sudden interruption of the flow of music to the speaker. The device will remain off until the temperature of the die decreases about 10°C to its lower temperature limit of 155°C. It is at this point that the device will turn itself on, again amplifying the input signal.

As can be seen in *Figures 14* and *15*, the junction temperature vs time graph and the response to the activation of the thermal shutdown circuitry perform in a Schmitt trigger fashion, turning the output on and off, thus regulating the temperature of the die over time when subjected to high continuous powers with improper heatsinking.

The intention of the protection circuitry is to prevent the device from being subjected to short-term fault conditions that result in high power dissipation within the amplifier and thus transgressing into thermal runaway. If the conditions that cause the thermal shutdown are not removed, the amplifier will perform in this Schmitt trigger fashion indefinitely, reducing the long-term reliability of the device.

The fairly slow-acting thermal shutdown circuitry is not intended to protect the amplifier against transient safe operating area violations. SPiKe protection circuitry will perform this function.

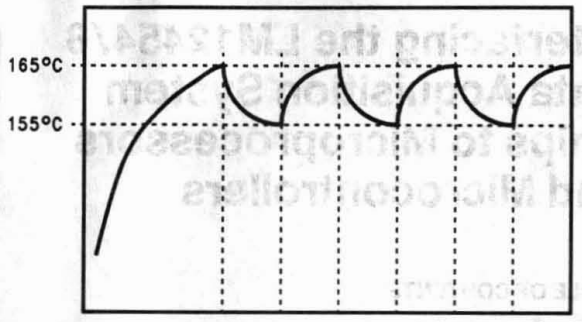

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FIGURE 14. Junction Temperature vs Time

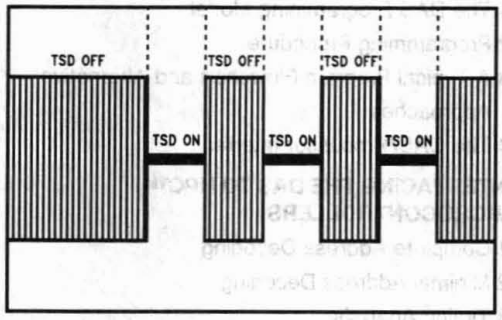

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FIGURE 15. Thermal Shutdown Waveform

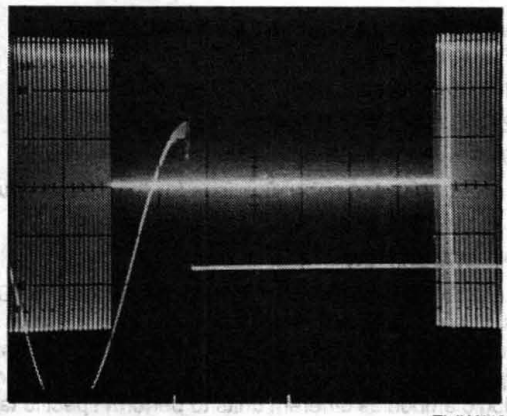

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FIGURE 16. Actual Thermal Shutdown Waveform

Interfacing the LM12454/8 Data Acquisition System Chips to Microprocessors and Microcontrollers

National Semiconductor
Application Note 906
Farid Saleh

TABLE OF CONTENTS

1.0 INTRODUCTION

2.0 GENERAL OVERVIEW

2.1 The DAS Programming Model
2.2 Programming Procedure
2.3 A Typical Program Flowchart and Alternative Approaches
2.4 The DAS/Processor Interface

3.0 INTERFACING THE DAS TO HPC™ MICROCONTROLLERS

3.1 Complete Address Decoding
3.2 Minimal Address Decoding
3.3 Timing Analysis
3.3.1 Complete Address Decoding Circuit
3.3.2 Minimal Address Decoding Circuit

4.0 A SYSTEM EXAMPLE: A SEMICONDUCTOR FURNACE

4.1 System Requirements and Assumptions
4.2 DAS Setup and Register Programming
4.3 Microcontroller Programming
4.3.1 HPC Assembly Routines for the Semiconductor Furnace Example

1.0 INTRODUCTION

The LM12454/8 family of data acquisition system (DAS) chips offers a fully differential self-calibrating 12-bit+ sign A/D converter with differential reference, 4 or 8 input analog multiplexer and extensive flexible and programmable logic. The logic embodies different units to perform specific tasks, for instance:

— An instruction RAM for stand-alone execution (after being programmed by the host) with programmable acquisition time, input selection, 8-bit or 12-bit conversion mode, etc.

— Limit registers for comparison of the inputs against high and low limits in "watchdog" mode.

— A 32-word FIFO register for storage of conversion results.

— Interrupt control logic with interrupt generation for 8 different conditions.

— A 16-bit timer register.

— Circuitry for synchronizing signal acquisition with external events.

— A parallel microprocessor interface with selectable 8-bit or 16-bit data access.

Because of its functionality and flexibility, working with the LM12454/8 family may appear to be an overwhelming task at first glance. However, this is not the case when the user gains a basic understanding of the device's functional units and the philosophy of its operation. This note shows how easy it is to use the LM12454/8 family and walks the user through the straightforward steps of the interfacing and programming of the device.

The LM12454/8 family has 6 members. The members and their differences are shown in Table I. For simplicity, the DAS abbreviation will be used throughout this Application Note as a generic name for any member of the family. Similarly, the drawings illustrate only the 8 input versions of the family. Note that this Application Note should be used in conjunction with the device data sheet and assumes the reader has some degree of familiarity with the device. However, a brief overview of the DAS and information related to the subjects being discussed are given here.

2.0 GENERAL OVERVIEW

2.1 The DAS Programming Model

Figure 1 illustrates the functional block diagram or user programming model of the DAS. (This diagram is not meant to reflect the actual implementation of the DAS internal building blocks.) The DAS model consists of the following blocks:

— A flexible analog multiplexer with differential output at the front end of the device.

TABLE I: Members of the LM12454/8 Family

Device Number	Clock Frequency (Max, MHz)	Operating Supply Voltage (V)	Number of MUX Inputs	Internal Reference	Low Voltage Flag
LM12454	5	5.0 ±10%	4	Yes	Yes
LM12458	5	5.0 ±10%	8	Yes	Yes
LM12H454	8	5.0 ±10%	4	Yes	Yes
LM12H458	8	5.0 ±10%	8	Yes	Yes
LM12L454	6	3.3 ±10%	4	No	No
LM12L458	6	3.3 ±10%	8	No	No

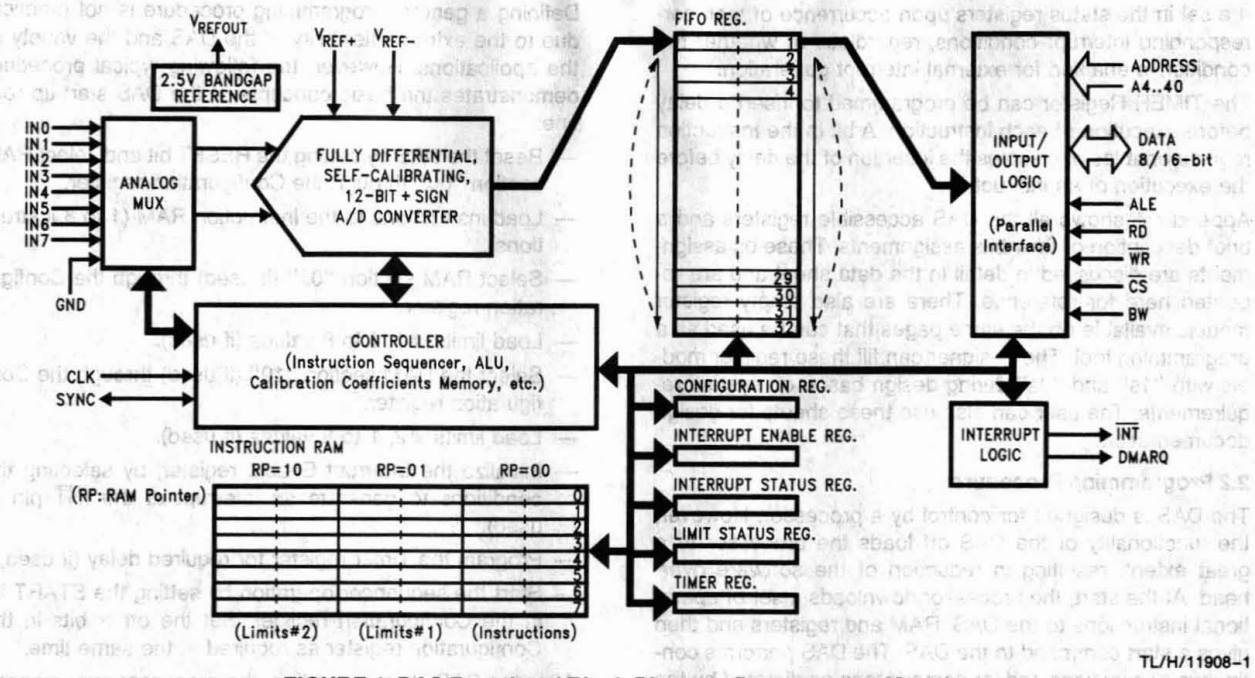

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FIGURE 1. DAS Functional Block Diagram, Programming Model

— A fully-differential, self-calibrating 12-bit+ sign A/D converter.

— A 32-word FIFO register as the output data buffer.

— An instruction RAM that can be programmed to repeatedly perform a series of conversions and comparisons on the selected input channels.

— A series of registers for overall control and configuration of the DAS operation and indication of internal operational status.

— Interrupt generation logic to request service from the processor under specified conditions.

— Parallel interface logic for input/output operations between the DAS and the processor. All the registers shown in the diagram can be read and most of them can also be written to by the user through the input/output block.

— A controller unit that controls the interactions of the different blocks inside the DAS and performs the conversion, comparison and calibration sequences.

The DAS has 3 different modes of operation: 12-bit+ sign conversion, 8-bit+ sign conversion and 8-bit+ sign comparison, (also called "watchdog" mode). In the watchdog mode no conversion is performed, but the DAS samples an input and compares it with the values of the two limits stored in the Instruction RAM. If the input voltage is above or below the limits (as defined by the user) an interrupt can be generated to indicate a fault condition.

The INSTRUCTION RAM is divided into 8 separate words, each with 48 (3x16) bit length. Each word is separated into three 16-bit sections. Each word has a unique address and different sections of the instruction are selected by the 2-bit RAM pointer (RP) in the configuration register. As shown in *Figure 1*, the Instruction RAM sections are labeled Instructions, Limits #1 and Limits #2. The Instruction section holds operational information such as; the input channels to be selected, the mode of operation for each instruction, and how long the acquisition time should be. The other two sections are used in the watchdog mode and the user defined limits are stored in them. Each watchdog instruction has 2 limits associated with it (usually the low and high limits, but two low or two high limits may be programmed instead). The DAS can start executing from Instruction 0 and continue executing the next instructions up to any user specified instruction and, then "loops back" to Instruction 0. This means that not all 8 instructions need to be executed in the loop. The cycle may be repeatedly executed until stopped by the user. The user should access the Instruction RAM only when the instruction sequencer is stopped.

The FIFO Register is used to store the results of the conversion. This register is "read only" and all the locations are accessed through a single address. Each time a conversion is performed the result is stored in the FIFO and the FIFO's internal write pointer points to the next location. The pointer rolls back to location 1 after a write to location 32. The same flow occurs when reading from the FIFO. The internal FIFO writes and the external FIFO reads do not affect each other's pointer locations.

The CONFIGURATION Register is the main "control panel" of the DAS. Writing 1s and 0s to the different bits of the Configuration Register commands the DAS to perform different actions such as start or stop the sequencer, reset the pointers and flags, enter standby mode for low power consumption, calibrate offset and linearity, and select sections of the RAM.

The INTERRUPT ENABLE Register lets the user activate up to 8 sources for interrupt generation. It also holds two user programmable values. One is the number of conversions to be stored in the FIFO register before the generation of the data ready interrupt. The other value is the instruction number that generates an interrupt when the sequencer reaches that instruction.

The INTERRUPT STATUS and LIMIT STATUS Registers are "read only" registers. They are used as vectors to indicate which conditions have generated the interrupt and what limit boundaries have been passed. Note that the bits

are set in the status registers upon occurrence of their corresponding interrupt conditions, regardless of whether the condition is enabled for external interrupt generation.

The TIMER Register can be programmed to insert a delay before execution of each instruction. A bit in the Instruction register enables or disables the insertion of the delay before the execution of an instruction.

Appendix A shows all the DAS accessible registers and a brief description of their bits assignments. These bit assignments are discussed in detail in the data sheet and are repeated here for reference. There are also empty register models available on the same pages that can be used as a programming tool. The designer can fill these register models with "1s" and "0s" during design based on system requirements. The user can also use these sheets for design documentation.

2.2 Programming Procedure

The DAS is designed for control by a processor. However, the functionality of the DAS off loads the processor to a great extent, resulting in reduction of the software overhead. At the start, the processor downloads a set of operational instructions to the DAS' RAM and registers and then gives a start command to the DAS. The DAS performs continuous conversions and/or comparisons as dictated by the instructions and loads the conversion results in the FIFO. From this point the processor has two basic options for interaction with the DAS. The DAS can generate an interrupt to the processor when the predetermined number of conversion results are stored in the FIFO or when any other interrupt conditions have occurred. The processor will then service the interrupt by reading the FIFO or taking corrective action, depending on the nature of the interrupt. Alternatively, rather than responding to an interrupt, the processor at any time can read the data or give a new command to the DAS.

Defining a general programming procedure is not practical due to the extreme flexibility of the DAS and the variety of the applications. However, the following typical procedure demonstrates the basic concepts of the DAS start-up routine:

— Reset the DAS by setting the RESET bit and select RAM section "00" through the Configuration register.

— Load instructions to the Instruction RAM (1 to 8 instructions).

— Select RAM section "01" (if used) through the Configuration register.

— Load limits #1, 1 to 8 values (if used).

— Select the RAM section "10" (if used) through the Configuration register.

— Load limits #2, 1 to 8 values (if used).

— Initialize the Interrupt Enable register, by selecting the conditions to generate an interrupt at the $\overline{INT}$ pin (if used).

— Program the Timer register for required delay (if used).

— Start the sequencer operation by setting the START bit in the Configuration register. Set the other bits in the Configuration register as required at the same time.

After the DAS starts operating, the processor may respond to interrupts from the DAS or it may interrogate the DAS at any time.

2.3 A Typical Program Flowchart and Alternative Approaches

A typical DAS program flowchart is shown in *Figure 2*. *Figure 2a* shows the initialization of the DAS and the start of the conversions. *Figure 2b* shows the general form of the DAS interrupt service routine. It is assumed that the DAS interacts with the processor through an interrupt line. This means the host processor generally is busy with other tasks and responds to the DAS through its interrupt service routine.

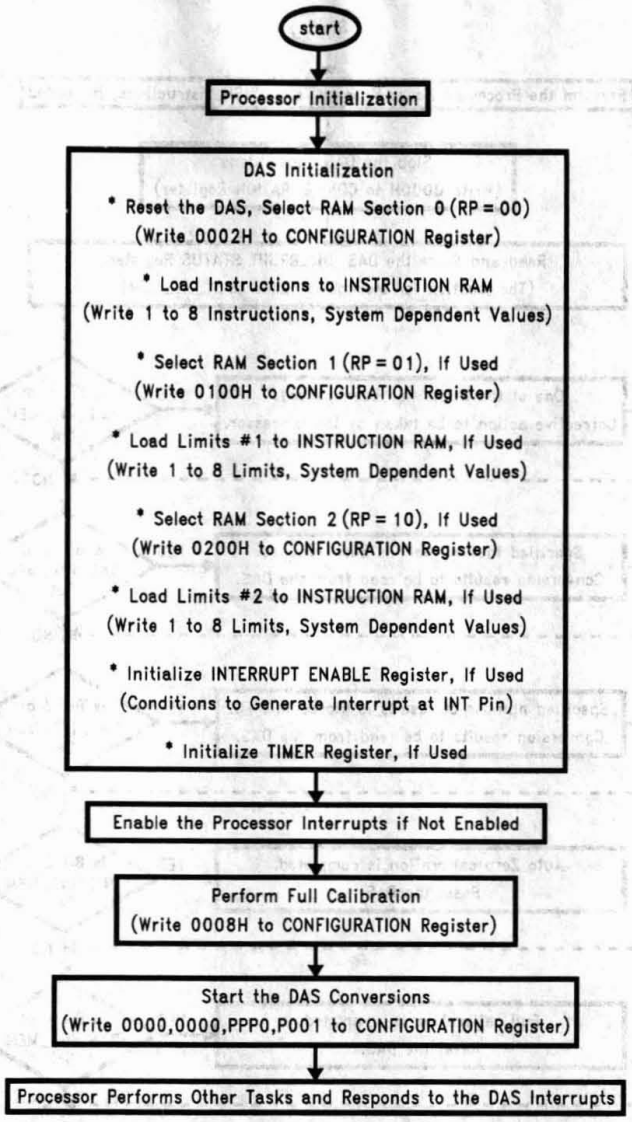
start
Processor Initialization
DAS Initialization
* Reset the DAS, Select RAM Section 0 (RP = 00)
(Write 0002H to CONFIGURATION Register)
* Load Instructions to INSTRUCTION RAM
(Write 1 to 8 Instructions, System Dependent Values)
* Select RAM Section 1 (RP = 01), If Used
(Write 0100H to CONFIGURATION Register)
* Load Limits #1 to INSTRUCTION RAM, If Used
(Write 1 to 8 Limits, System Dependent Values)
* Select RAM Section 2 (RP = 10), If Used
(Write 0200H to CONFIGURATION Register)
* Load Limits #2 to INSTRUCTION RAM, If Used
(Write 1 to 8 Limits, System Dependent Values)
* Initialize INTERRUPT ENABLE Register, If Used
(Conditions to Generate Interrupt at INT Pin)
* Initialize TIMER Register, If Used
Enable the Processor Interrupts if Not Enabled
Perform Full Calibration
(Write 0008H to CONFIGURATION Register)
Start the DAS Conversions
(Write 0000,0000,PPP0,P001 to CONFIGURATION Register)
Processor Performs Other Tasks and Responds to the DAS Interrupts

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FIGURE 2a. A Typical Program Flowchart for the DAS Initialization and Start of Conversions

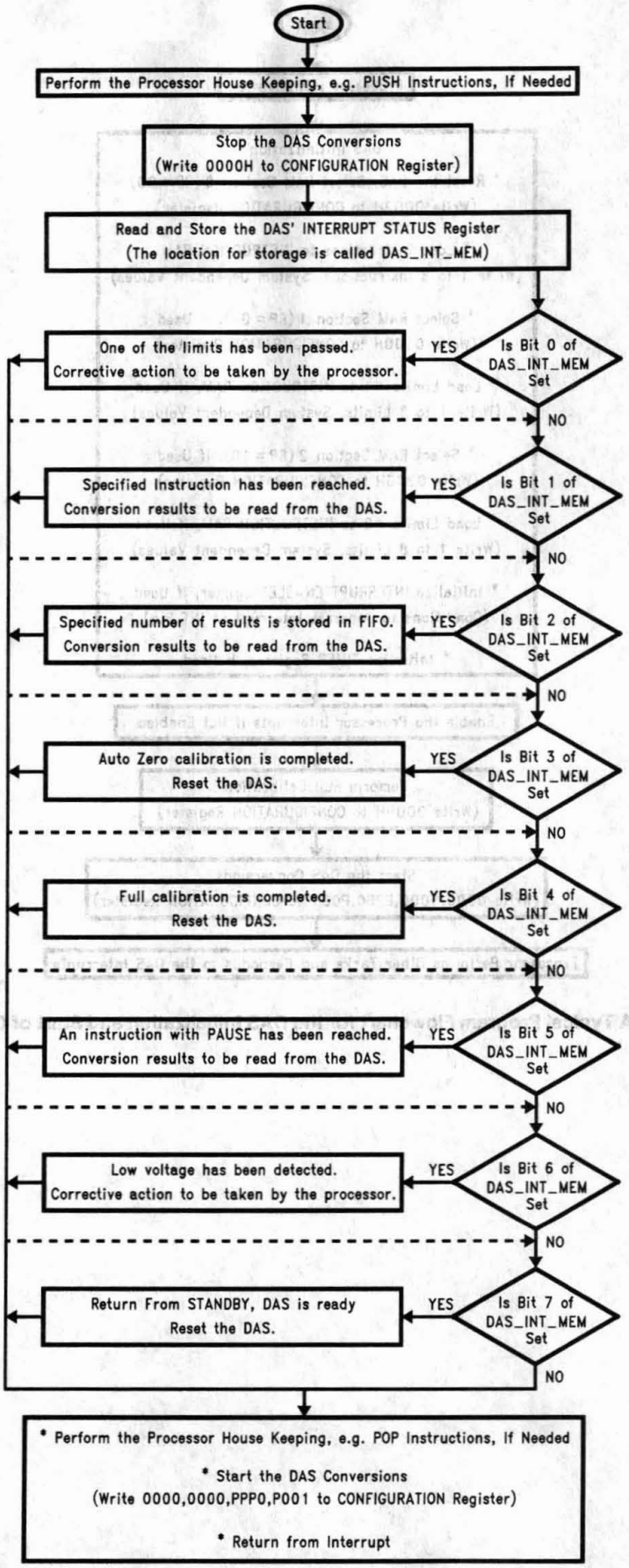
Start
Perform the Processor House Keeping, e.g. PUSH Instructions, If Needed
Stop the DAS Conversions
(Write 0000H to CONFIGURATION Register)
Read and Store the DAS' INTERRUPT STATUS Register
(The location for storage is called DAS_INT_MEM)
Is Bit 0 of DAS_INT_MEM Set
YES
One of the limits has been passed.
Corrective action to be taken by the processor.
NO
Is Bit 1 of DAS_INT_MEM Set
YES
Specified Instruction has been reached.
Conversion results to be read from the DAS.
NO
Is Bit 2 of DAS_INT_MEM Set
YES
Specified number of results is stored in FIFO.
Conversion results to be read from the DAS.
NO
Is Bit 3 of DAS_INT_MEM Set
YES
Auto Zero calibration is completed.
Reset the DAS.
NO
Is Bit 4 of DAS_INT_MEM Set
YES
Full calibration is completed.
Reset the DAS.
NO
Is Bit 5 of DAS_INT_MEM Set
YES
An instruction with PAUSE has been reached.
Conversion results to be read from the DAS.
NO
Is Bit 6 of DAS_INT_MEM Set
YES
Low voltage has been detected.
Corrective action to be taken by the processor.
NO
Is Bit 7 of DAS_INT_MEM Set
YES
Return From STANDBY, DAS is ready
Reset the DAS.
NO
* Perform the Processor House Keeping, e.g. POP Instructions, If Needed
* Start the DAS Conversions
(Write 0000,0000,PPP0,P001 to CONFIGURATION Register)
* Return from Interrupt

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FIGURE 2b. A Typical Program Flowchart for the DAS Interrupt Service Routine

There is a processor initialization step at the start of the flowchart. It is included as a reminder that some specific processor initialization may be needed just for interaction with the DAS.

The DAS initialization steps are a series of write operations to the DAS registers. These steps are the same as mentioned in Section 2.2.

A full calibration cycle is usually performed after setting the DAS' registers. This is required for 12-bit accuracy. You may choose to perform one full calibration at power up, or periodic calibrations at specified time intervals, or condition-based calibrations, e.g., calibrations after a specified change in temperature. Calibration is done by writing the appropriate control code to the Configuration register. A full calibration cycle takes about 1 ms (989 μs) with a 5 MHz clock and about 0.6 ms (618 μs) with an 8 MHz clock. You can insert a delay after starting a calibration cycle, or can detect the end of calibration by an interrupt, or by reading the Interrupt Status register for the corresponding flag bit. In the flowchart, the end-of-calibration detection is handled in the interrupt service routine. The full calibration cycle affects some of the DAS' internal flags and pointers that will influence the execution of the first instruction after calibration. To avoid false instruction execution, the DAS should be reset after a calibration cycle. This is shown on the flowchart for the interrupt service routine.

After a calibration, the DAS is ready to start conversions. Conversion is initiated by writing to the configuration register and setting the START bit to "1". The data to be written to the configuration register is shown in binary format in the flowchart. The bits shown by "P" (program) are the control bits that determine different modes of operation during conversions. All the other bits should be programmed as shown. As mentioned before, the host processor can perform data manipulation and other control tasks after starting the DAS, and will respond to the DAS interrupts as required.

At the start of the interrupt service routine (*Figure 2b*), a zero is written to START bit in the Configuration register, to stop the conversion. Stopping the conversion is not necessarily needed unless it is required for accuracy or timing purposes. Generally the results of conversions will be noisier and less accurate if reads or writes to and from the DAS are performed while it is converting. However, the degree of this inaccuracy depends on many aspects of system design and is not easy to quantify. Power supply and ground routing, supply bypassing, speed of logic transitions on the bus, the logic family being used, and the loading (resistive and capacitive) on the data bus being driven by the DAS, all can affect conversion noise. Nevertheless, reading during conversions has been shown not to cause serious accuracy problems in most systems.

There are two timing issues regarding the reading during conversion.

During any read or write from or to the DAS, the DAS internal clock will stop while the $\overline{CS}$ is low. This is done for synchronization between external and internal bus activities, thus preventing internal conflicts. Note that reads and writes are asynchronous to internal bus activities. A pause of internal clock cycles will increase the total acquisition plus conversion time for each instruction. The amount of this time increase is variable and is not easily predictable, because the processor and the DAS work asynchronously. As a result, the user should not perform reads during conversions if the fixed time intervals between the signal acquisitions are critical in the system performance.

The second timing issue depends on the speed of the conversions and the speed of the read cycles from the FIFO. The rule is to read the FIFO fast enough that old data will not be overwritten with new data during continuous conversions.

Returning to the flowchart, the main task of the interrupt service routine is to read the DAS' Interrupt Status register and test its bits for the source of the interrupt. The interrupt service routine shows all the interrupt bits in the DAS being tested. However, real systems often use only a few number of the interrupts, so the extra bit tests should be eliminated from the routine. Also, the sequence in which the bits are tested depends on the priority level of the interrupts in the system. The tasks to be performed for each interrupt are mainly system related and are not elaborated upon in the flowchart. If conversions are stopped at the start of the interrupt service, one possibility is to restart conversion before returning from the interrupt service routine. Otherwise conversions will be restarted again at some other point in the system routines.

2.4 The DAS/Processor Interface

The interface between the processor and the DAS is similar to a memory or I/O interface. Some possible DAS/microcontroller interface schemes are shown in *Figures 3*, *4* and *5*.

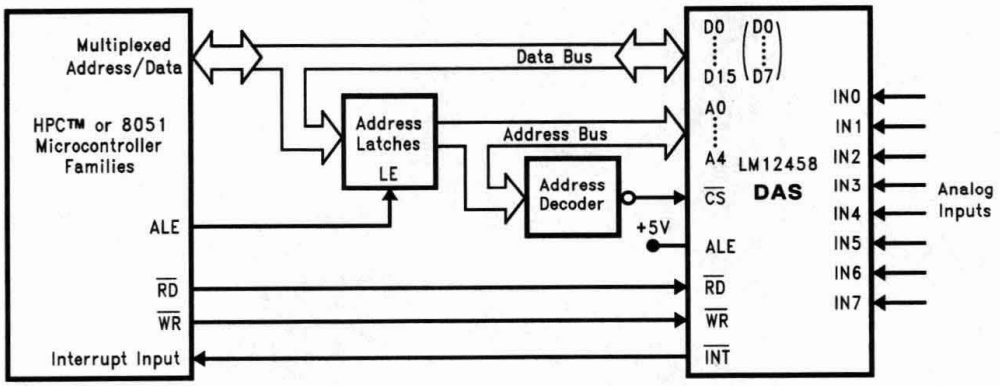

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FIGURE 3. LM12458 to HPC or 8051 Microcontroller Interface

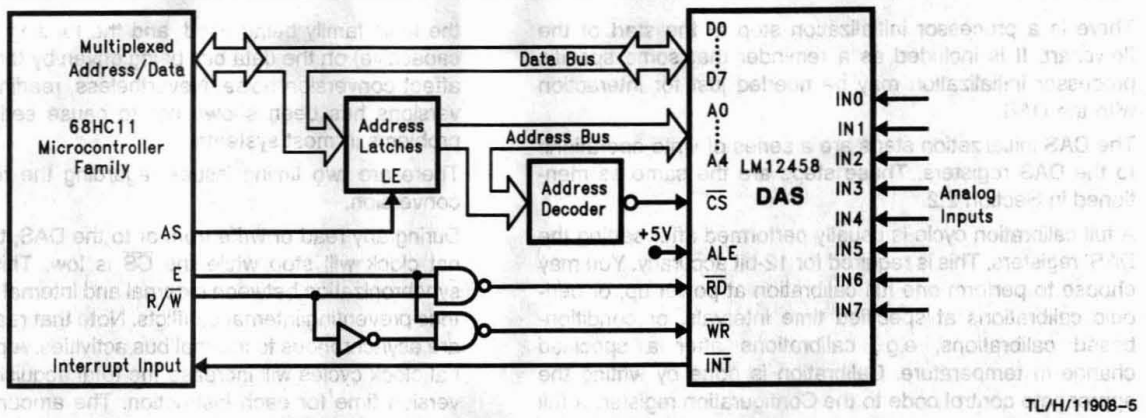

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FIGURE 4. LM12458 to 68HCII Microcontroller Interface

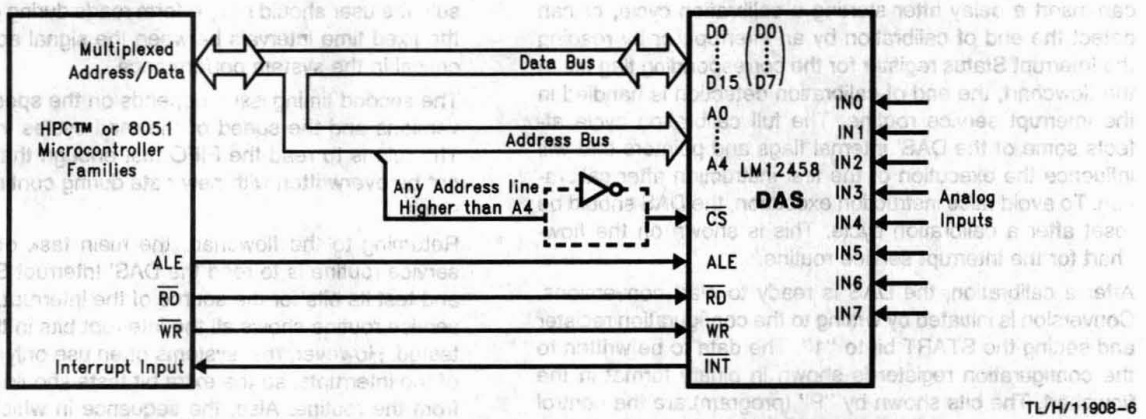

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FIGURE 5. LM12458 to HPC or 8051 Microcontroller Interface (Minimum System)

From the processor's point of view, the DAS is a group of I/O registers with specific addresses. *Figure 6* illustrates the DAS registers with their address assignments and the DAS interface buses and control signals. The DAS provides standard architecture for address, data and control buses for parallel interface to processors. The DAS can be interfaced to both multiplexed and non-multiplexed address/data bus architectures. An ALE input and internal latches allow the DAS to interface to a multiplexed address/data bus when external address latches are not required by the system. The DAS can be accessed in either 8-bit or 16-bit data width. BW (Bus Width) input pin selects the 8-bit or 16-bit access. In 8-bit access mode, each 16-bit I/O register is accessed in 2 cycles. Address line A0 selects the lower or upper portions of a 16-bit register. In 16-bit access mode, address line A0 is a "don't care". As shown in the *Figures 6a* and *6b*, the DAS appears to the processor as 14 separate 16-bit or 28 separate 8-bit I/O locations.

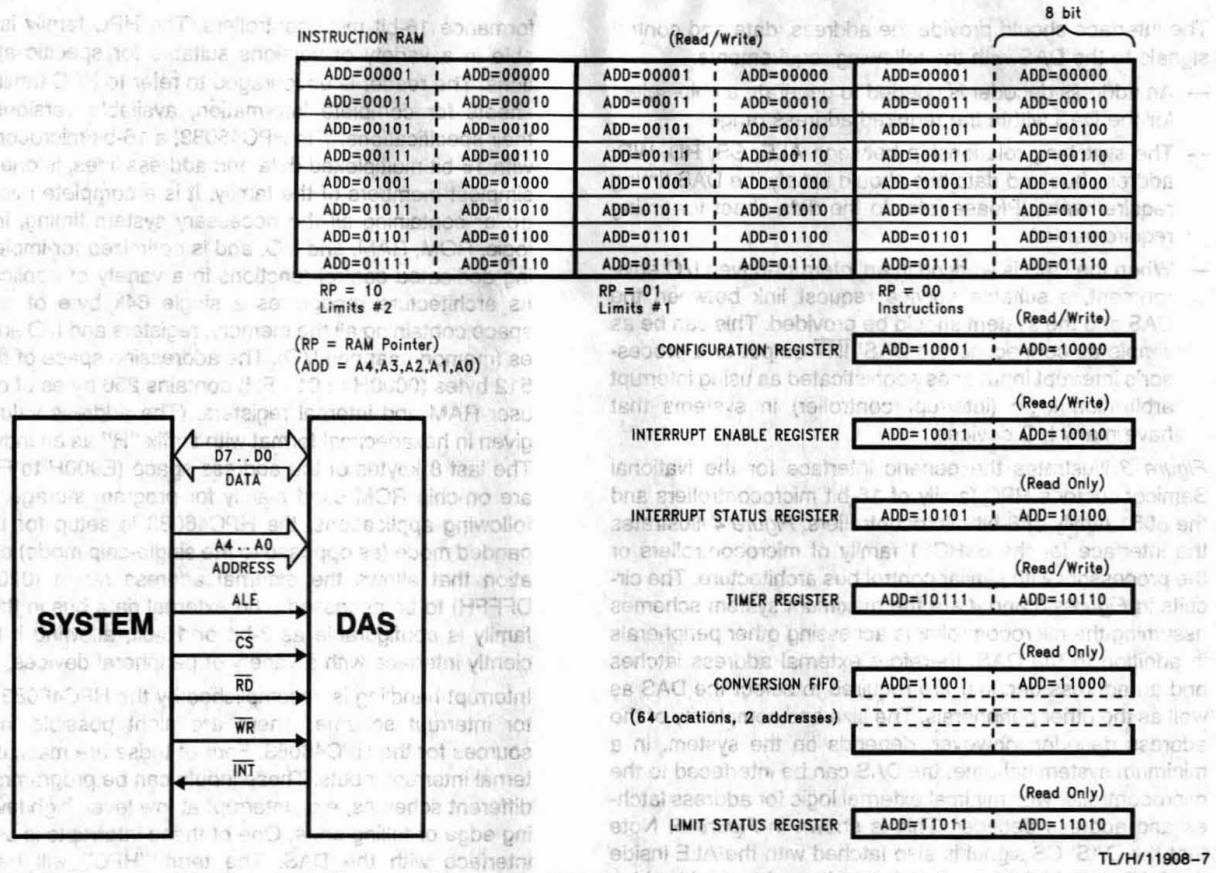

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FIGURE 6a. DAS Registers, Address Assignments, Interface Buses and Control Signals for 8-Bit Bus Width

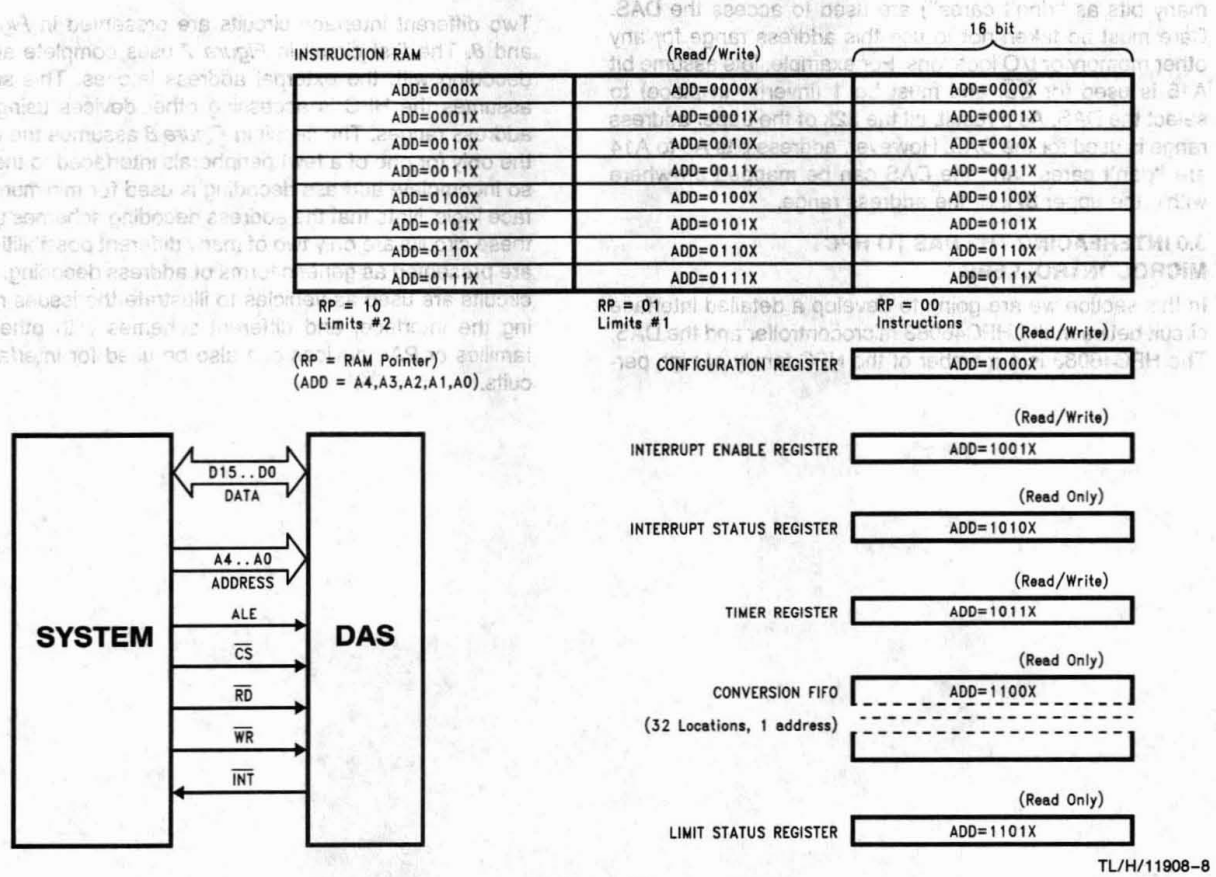

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FIGURE 6b. DAS Registers, Address Assignments, Interface Buses and Control Signals for 16-Bit Bus Width

The interface should provide the address, data and control signals to the DAS with the following requirements:

— An address decoder is needed to generate a chip-select for the DAS within the required address range.

— The switching relationship between ALE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, address bus and data bus should satisfy the DAS timing requirements. (Please refer to the data sheet for timing requirements.)

— When the DAS is working in an interrupt-driven I/O environment, a suitable service request link between the DAS and the system should be provided. This can be as simple as connecting the DAS' $\overline{INT}$ output to a processor's interrupt input or as sophisticated as using interrupt arbitration logic (interrupt controller) in systems that have many I/O devices.

Figure 3 illustrates the generic interface for the National Semiconductor's HPC family of 16-bit microcontrollers and the 8051 family of 8-bit microcontrollers. *Figure 4* illustrates the interface for the 68HC11 family of microcontrollers or the processors with similar control bus architecture. The circuits in *Figures 3* and *4* are the maximum system schemes assuming the microcontroller is accessing other peripherals in addition to the DAS, therefore external address latches and an address decoder are required to select the DAS as well as the other peripherals. The size and complexity of the address decoder, however, depends on the system. In a minimum system scheme, the DAS can be interfaced to the microcontroller with minimal external logic for address latches and address decoder. This is shown in *Figure 5*. Note that the DAS' $\overline{CS}$ signal is also latched with the ALE inside the DAS, so a higher order address bit can be used to drive $\overline{CS}$ input. In this scheme a wide range of addresses (with many bits as "don't cares") are used to access the DAS. Care must be taken not to use this address range for any other memory or I/O locations. For example, lets assume bit A15 is used for $\overline{CS}$, and must be 1 (inverter in place) to select the DAS. As a result, all the 32k of the upper address range is used for the DAS. However, address bits A5 to A14 are "don't cares" and the DAS can be mapped anywhere within the upper 32k of the address range.

3.0 INTERFACING THE DAS TO HPC MICROCONTROLLERS

In this section we are going to develop a detailed interface circuit between the HPC46083 microcontroller and the DAS. The HPC46083 is a member of the HPC family of high performance 16-bit microcontrollers. The HPC family is available in a variety of versions suitable for specific applications. The reader is encouraged to refer to HPC family data sheets for complete information, available versions, and their specifications. The HPC46083, a 16-bit microcontroller with 16-bit multiplexed data and address lines, is one of the simplest members of the family. It is a complete microcontroller containing all the necessary system timing, internal logic, ROM, RAM, and I/O, and is optimized for implementing dedicated control functions in a variety of applications. Its architecture recognizes a single 64k byte of address space containing all the memory, registers and I/O addresses (memory-mapped I/O). The addressing space of the first 512 bytes (0000H to 01 FFH) contains 256 bytes of on-chip user RAM and internal registers. (The address values are given in hexadecimal format with suffix "H" as an indicator.) The last 8 kbytes of the address space (E000H to FFFFH) are on-chip ROM used mainly for program storage. In the following applications, the HPC46083 is setup for the expanded mode (as opposed to the single-chip mode) of operation that allows the external address range (0200H to DFFFH) to be accessed. The external data bus in the HPC family is configurable as 8-bit or 16-bit, allowing it to efficiently interface with a variety of peripheral devices.

Interrupt handling is accomplished by the HPC46083's vector interrupt scheme. There are eight possible interrupt sources for the HPC46083. Four of these are maskable external interrupt inputs. These inputs can be programmed for different schemes, e.g., interrupt at low level, high level, rising edge or falling edge. One of these interrupts is used for interface with the DAS. The term "HPC" will be used throughout the remainder of this discussion to refer to the HPC46083.

Two different interface circuits are presented in *Figures 7* and *8*. The first circuit in *Figure 7* uses complete address decoding with the external address latches. This scheme assumes the HPC is accessing other devices using other address ranges. The circuit in *Figure 8* assumes the DAS is the only (or one of a few) peripherals interfaced to the HPC, so incomplete address decoding is used for minimum interface logic. Note that the address decoding schemes used in these circuits are only two of many different possibilities and are presented as generic forms of address decoding. These circuits are used as vehicles to illustrate the issues regarding the interface, and different schemes with other logic families or PAL devices can also be used for interface circuits.

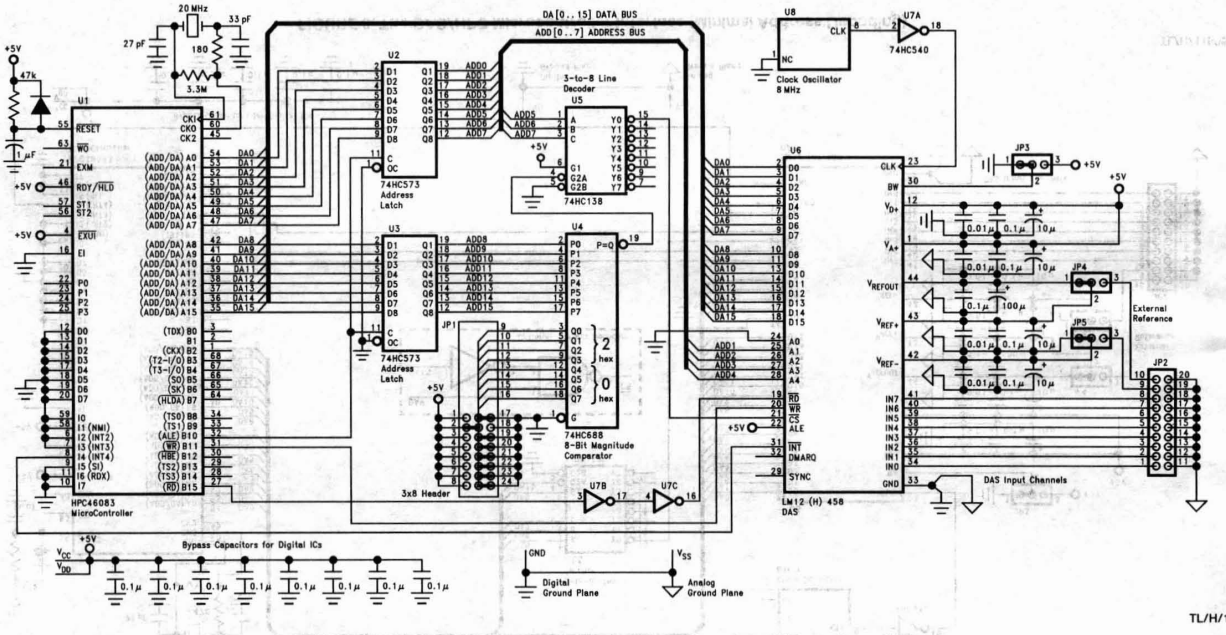

FIGURE 7. The DAS/HPC Microcontroller Interface (Complete Address Decoding)

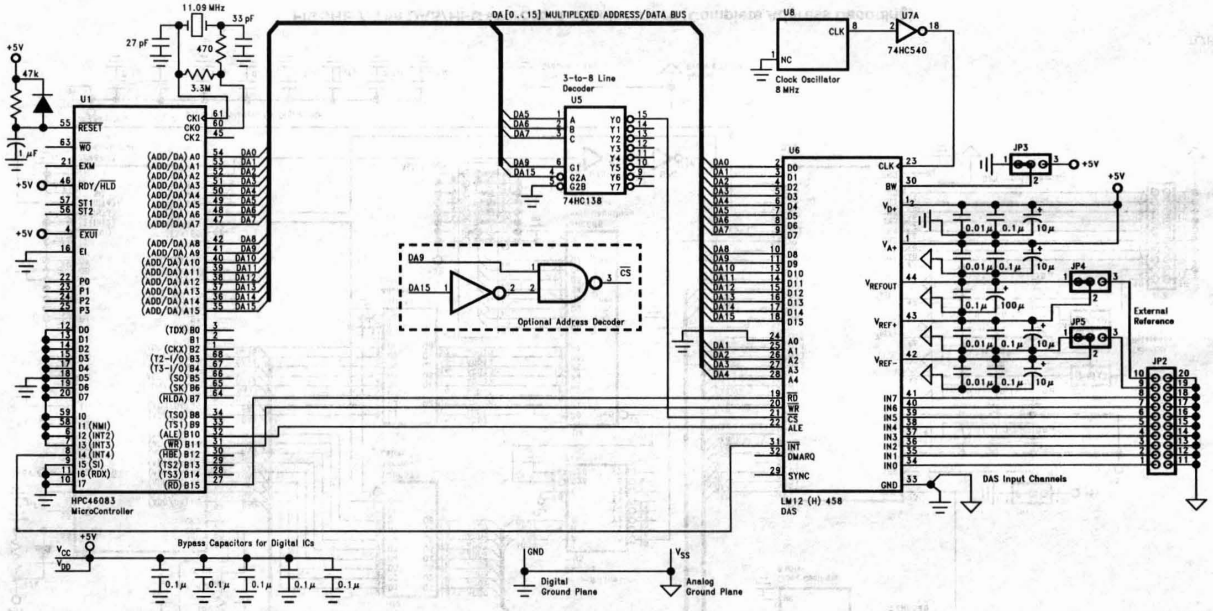

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FIGURE 8. The DAS/HPC Microcontroller Interface (Minimal Address Decoding)

3.1 Complete Address Decoding

Figure 7 shows the circuit with complete address decoding to generate the DAS' $\overline{CS}$ signal. The DAS is accessed as memory mapped I/O at the start of the external address range (0200H to 021BH), and 16-bit data access is selected for the DAS. External address latches, U2 and U3, (74HC573) are used for the HPC's multiplexed 16-bit data/address lines. As a result, the ALE input of the DAS is tied high. An 8-bit magnitude comparator, U4, (74HC688) decodes the high order address byte [A15...A8] by comparing it with the logic input from the address range selector jumpers on header JP1. The jumper setting shown in *Figure 7* is 02H. The output of the magnitude comparator enables 3-to-8 line decoder chip, U5, (74HC138). The 3-to-8 line decoder inputs are address lines A5 to A7. The output Y0 of the 3-to-8 line decoder is activated for the 32 locations of address space from 0200H to 021FH. This output (Y0) is used for the DAS' $\overline{CS}$ input. Address lines A1 to A4 are directly connected to the DAS address inputs. The A0 input of the DAS is tied to ground since 16-bit data access is used and A0 is a "don't care". The DAS uses 28 bytes of address locations with addresses from 0200H to 021BH.

The DAS signal timing requires that its $\overline{CS}$ be active at least 20 ns before $\overline{RD}$ or $\overline{WR}$. This requirement cannot be met with the HPC running at 20 MHz clock frequency. In order to compensate for the propagation delays in the address latches and decoder, 2 inverting buffers (U7), are placed in the $\overline{RD}$ control line. The need for these inverters will be discussed further in the following Timing Analysis section. The $\overline{WR}$ line does not require this delay compensation.

The DAS' $\overline{INT}$ output drives the INT4 input of the HPC. This allows the DAS to request service when acquired data is ready or for any other condition for which processor attention is needed. The selection of INT4 is arbitrary, and any other external interrupt input could have been used. In a real system, selection of a processor interrupt input will be based on the number of interrupt driven I/O devices and the priority for each device.

The DAS' clock is driven with an 8 MHz crystal clock module. The output of the clock module is separately buffered for the DAS. This keeps the DAS' clock clean and minimizes interference that might be generated and induced by other devices using the same clock line.

3.2 Minimal Address Decoding

The circuit in *Figure 8* does not use the external address latches (U2, U3), the 8-bit magnitude comparator (U4), and the address setting jumpers (JP1). The 3-to-8 line decoder (U5) is still used and is enabled by the address/data lines DA9 and DA15. DA9 should be "1" to enable U5. This is selected to prevent address conflict between the DAS and the HPC internal RAM and registers, which use the address range 0000H to 01FFH with DA9 equal to "0". DA15 should be "0" to enable U5. This is selected to prevent conflict between the DAS and the HPC internal ROM, which uses the address range E000H to FFFFH with DA15 equal to "1". The Y0 output of U5 is still driving the DAS' $\overline{CS}$ input. The ALE output of the HPC directly drives the DAS' ALE input. The ALE latches the address and $\overline{CS}$ lines on the DAS' internal latches at the start of any data transfer cycle with the DAS.

The DAS can still be accessed with the same address range in the *Figure 7* circuit, which is 0200H to 021BH. However, many address bits are "don't care" in this case. The binary form of the DAS register addresses for the circuit in *Figure 8* is: 0XXX,XX1X,000P,PPP0. The P's indicate program bits, these will be programmed to select different registers. The X's are "don't care" bits. The rest of the bits should be programmed as shown.

The 3-to-8 line decoder (U5) outputs, Y1 to Y7, can still be used to access other peripherals, those peripherals should have internal latches for the address and chip-select as well. For example, up to eight DAS chips can be interfaced to an HPC using the circuit in *Figure 8*, for monitoring and data logging of 64 analog input channels. If the interface is for one DAS only, the DAS' $\overline{CS}$ input can be generated with minimum of 2 gates, as shown within the dashed-lines on *Figure 8*, replacing the U5.

The critical DAS timing requirement for the circuit in *Figure 8* is the address and chip-select setup time to ALE going low. The HPC running at 20 MHz clock frequency cannot satisfy this timing specification. As a result, the clock speed of the HPC is lowered to 11.09 MHz to meet the DAS requirement. This point is also discussed further in the Timing Analysis section.

3.3 Timing Analysis

The user should perform a timing analysis along with the interface hardware design to ensure proper transaction of information between the processor and the DAS. For example the buffers in the $\overline{RD}$ input of the DAS in *Figure 7* are necessary to ensure proper timing. Similarly, the clock frequency of the HPC in *Figure 8* was reduced to ensure proper timing. For every new circuit design the DAS timing specifications for read and write cycles should be compared with the HPC (or the processor being used) timing specifications. Any mismatch between the timing characteristics must be compensated by hardware design changes or software techniques.

3.3.1 Complete Address Decoding Circuit

Study of the switching characteristics of the DAS and the HPC (running at 20 MHz) shows that the read cycle timing is more stringent than that of the write cycle. The timing diagram (*Figure 9*) shows the timing relationship for the signals involved in a read cycle. The first three signals are generated by the HPC (ALE, ADD/DATA, $\overline{RD}$), and are shown with their minimum timing relationships. The three other signals are $\overline{CS}$ and $\overline{RD}$ received by the DAS, and DATA(DAS) which is sent to the HPC. The $\overline{CS}$' longest propagation delay through the address latch (U3), magnitude comparator (U4), and 3-to-8 line decoder (U5) starts from the moment an address becomes valid. This propagation delay is, typically, 54 ns up to worst case of 116 ns.

Note: Maximum propagation delays for 74HC series logic devices are for 4.5V supply, 50 pF load and −40°C to 85°C temperature range. Typical values are for the same conditions at 25°C.

This delay, referred to the falling edge of the $\overline{RD}$(HPC), is 16 ns to 78 ns. The DAS requires that its $\overline{RD}$ becomes active 20 ns after its $\overline{CS}$. This requirement compels insertion of delay on the HPC's $\overline{RD}$ line before it is received by the DAS. Referenced to the HPC's $\overline{RD}$ signal falling edge the DAS' should receive a $\overline{RD}$ signal that is delayed by 36 ns to 98 ns (16 + 20 ns to 78 + 20 ns). Inverting buffers U7B and U7C

(75HC540) provide $\overline{RD}$ signal delay between the HPC and the DAS. The two buffers' propagation delay specification is typically 24 ns and the maximum is 50 ns. This is less than the 36 ns to 98 ns requirement drawn from the analysis. However, practical measurements have shown that this delay is sufficient within a temperature range of 0°C to 50°C. This discrepancy results from the fact that the operating conditions on the specification sheets (loading capacitance, supply voltage) for the logic devices are more severe than the ones in the practical circuit. However, if the circuit is to perform reliably in worst case conditions, extra delay may be inserted in the $\overline{RD}$ line.

The second timing requirement is the data setup time referenced to the rising edge of the HPC's $\overline{RD}$ line. The DAS data outputs will be valid from a typical 10 ns to a maximum of 80 ns after the falling edge of its $\overline{RD}$ line. The HPC requires 45 ns of setup time and has a $\overline{RD}$ pulse width of 140 ns (1 wait state), resulting in 95 ns of total delay in the $\overline{RD}$ buffers and data latency of the DAS. Again, at the extreme limits of the operating conditions, the valid data might miss the 45 ns of required setup time, so the insertion of 1 extra wait state (100 ns) in the read cycle of the HPC is required. The design shown here is an example to demonstrate necessary design considerations and may not be the best possible solution for every application.

The circuit of *Figure 7* was implemented and tested using the "HPC Designer's Kit" development system. The development system performs the HPC real time emulation and all of the HPC's features are available for use in the application. The HPC Designer's Kit also closely resembles the real processor's switching characteristics.

Figure 10 shows scope photos of the $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ signals from the *Figure 7* circuit, using the HPC development system. *Figure 10a* shows a read and a write cycle when no inverter is added in the $\overline{RD}$ line. There is plenty of setup time for $\overline{CS}$ to $\overline{WR}$ but not for $\overline{CS}$ to $\overline{RD}$. *Figure 10b* shows a close look of the $\overline{CS}$ to $\overline{RD}$ setup time of *Figure 10a*. The setup time is 18 ns (at room temperature), very close to 20 ns, but not enough margin for circuit and temperature variations. *Figure 10c* shows a close look of the $\overline{CS}$ and $\overline{RD}$ signals after adding the inverters in the $\overline{RD}$ line. The setup time has increased to 30 ns with 10 ns of margin to cover for circuit variations and temperature changes.

3.3.2 Minimal Address Decoding Circuit

Study of the switching characteristics for the circuit of *Figure 8* shows that the DAS address and $\overline{CS}$ setup times to ALE low are not satisfied when the HPC is running at 20 MHz. The HPC generates a valid address only 18 ns (min) before its ALE goes low at this speed (see *Figure 9*). The DAS needs 40 ns of setup time. The solution is reducing the HPC's clock frequency. The HPC running at 10 MHz will have a minimum setup time of 43 ns. There is some extra delay for the DAS' $\overline{CS}$ through U5 that must also be considered. This is the input to output propagation delay of U5, from the moment that address lines become valid to the point that the DAS' $\overline{CS}$ (Y0 output of U5) goes low.

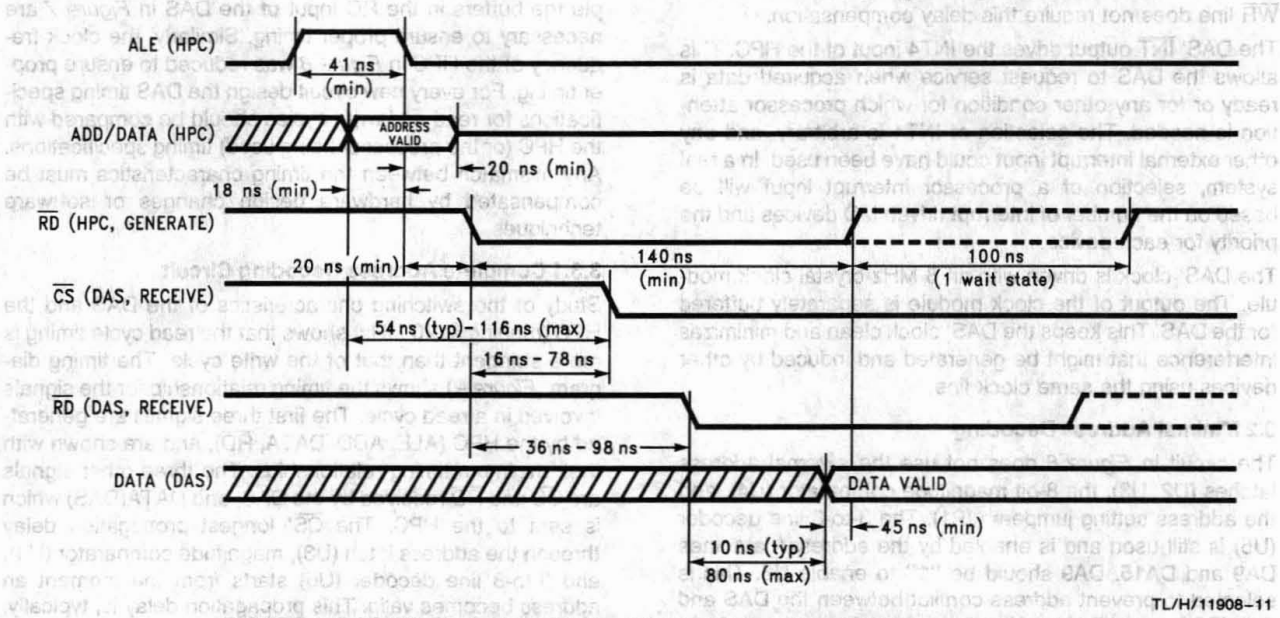
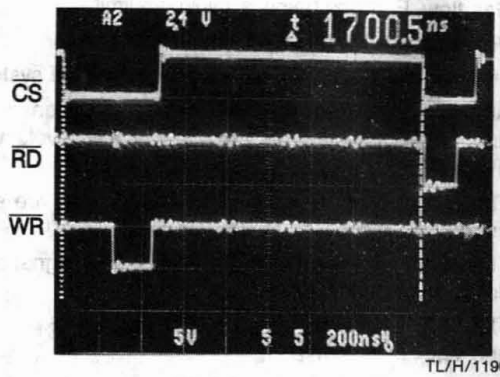


FIGURE 9. DAS/HPC Interface Timing Diagram (Complete Address Decoding)



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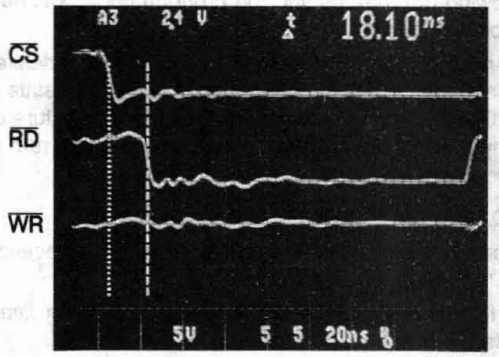
a) A Write and a Read Cycle, No Inverter in $\overline{RD}$ Line



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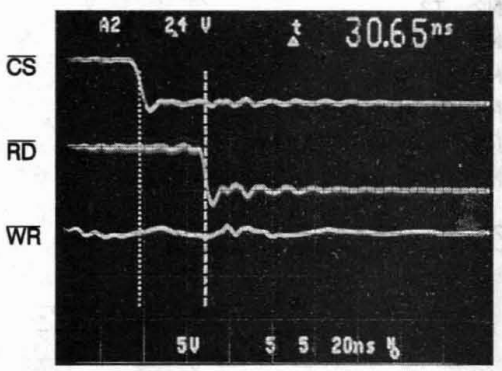
b) A Close Look at the $\overline{CS}$ to $\overline{RD}$ Setup Time, No Inverter in $\overline{RD}$ Line



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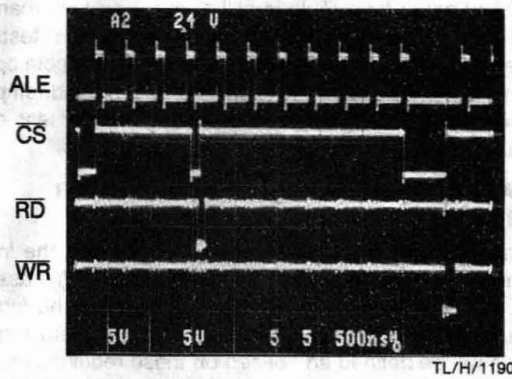
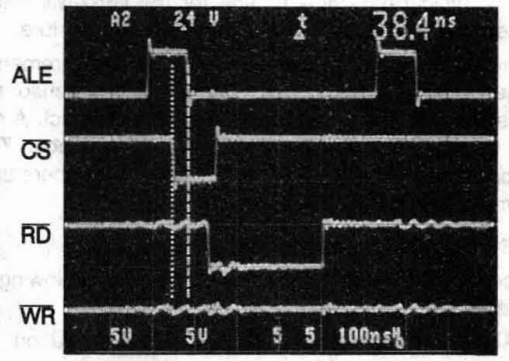
c) A Close Look at the $\overline{CS}$ to $\overline{RD}$ Setup Time, 2 Inverters in $\overline{RD}$ Line

FIGURE 10. Scope Photos of $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ Signals at the DAS, *Figure 7* Circuit



TL/H/11908–15

a) A Read and a Write Cycle with Zero Wait State



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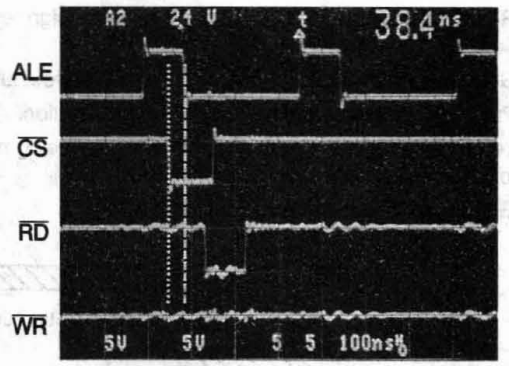
b) A Read Cycle with One Wait State



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c) A Read Cycle with Zero Wait State

FIGURE 11. Scope Photos of ALE, $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ Signals at the DAS, *Figure 8* Circuit

Practical measurements have shown reliable data transfer between the DAS and the HPC with the HPC running at 11.09 MHz clock at room temperature.

As a result of the HPC's lower clock frequency, the external data transfer can be performed with zero wait state, as opposed to the circuit of *Figure 7* where 1 wait state is essential. This speeds up the external read and write cycles and is especially useful when multiple successive reads are performed from the FIFO.

The circuit of *Figure 8* was also implemented and tested using the HPC development system. *Figure 11* shows scope photos of the ALE, $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ signals at the DAS inputs for the *Figure 8* circuit.*Figure 11a* shows a read and a write cycle with zero wait states. Notice that the read and write pulse rising edges occur after the $\overline{CS}$ signal. This does not matter since $\overline{CS}$ is internally latched. *Figures 11b* and *11c* give a more detailed view of the read cycles with 1 and 0 wait states, demonstrating about 180 ns shorter read cycle with no wait states. There is also about 38 ns of $\overline{CS}$ to

ALE low setup time. This is still about 2 ns less than the published DAS specifications. Although, practical tests resulted in reliable data transfer, to ensure dependable operation for the extremes of the circuit parameters and temperature variations, designers should use 10 MHz or less clock frequency for the HPC.

4.0 A SYSTEM EXAMPLE: A SEMICONDUCTOR FURNACE

In this application example the DAS measures the inputs from five sensors in a semiconductor furnace. We assume one of the circuits in *Figures 7* or *8* is used as the furnace data acquisition and control system. The system requirements will be defined and based on these requirements the DAS programming values for the DAS registers will be specified. A typical assembly routine for the HPC will also be presented for the DAS initialization and data capture.

Figure 12 shows a diagram of a typical measurement arrangement in a semiconductor furnace. A flow sensor measures the gas flow in the furnace chamber's duct. A pressure sensor measures the pressure in the chamber. Three temperature sensors measure the furnace temperature at the middle and each end of the furnace.

4.1 System Requirements and Assumptions

To control the operation of the furnace the following five measurements must be made:

— Absolute temperature at T1, with 12-bit resolution.
— Relative temperature, T1 to T2, with 12-bit + sign resolution.
— Relative temperature, TI to T3, with 12-bit + sign resolution.
— Gas flow, F, through the chamber, with 8-bit resolution.
— Pressure, P, in the chamber, with 8-bit resolution.

There are three alarm conditions that are also being monitored:

— Gas flow, F, exceeds a maximum limit.
— Gas flow, F, drops below a minimum limit.
— Pressure, P, exceeds a maximum limit.

The following assumptions are also made for the system:

— All the signals from the sensors are conditioned (gain and offset adjusted) to provide voltage levels within 0V–2.5V for the DAS inputs.
— The output of all signal conditioning circuits are single ended with respect to analog ground.
— The signal at the output of the flow sensor signal conditioner has 600Ω source impedance.
— The DAS reference voltage is 2.5V, i.e., V_{REF+} = 2.5V and V_{REF-} = AGND.
— The circuits in *Figure 7* or *8* (either one) is used for the furnace measurement and monitoring system. The following discussions and the program codes will be valid for both circuits.
— An approximate throughput rate of 50 Hz is desired for each set of measurement results (a set of results every 20 ms). However, due to the slow varying nature of the input signals, precisely controlled throughput rate is not essential for proper system performance.

4.2 DAS Setup and Register Programming

Based on the system requirements, we can proceed with the DAS setup and register settings.

The five sensor outputs are assigned to the first five DAS inputs:

— IN0: T1
— IN1: T2
— IN2: T3
— IN3: F
— IN4: P
— IN5: Not used - Tied to GND
— IN6: Not used - Tied to GND
— IN7: Not used - Tied to GND

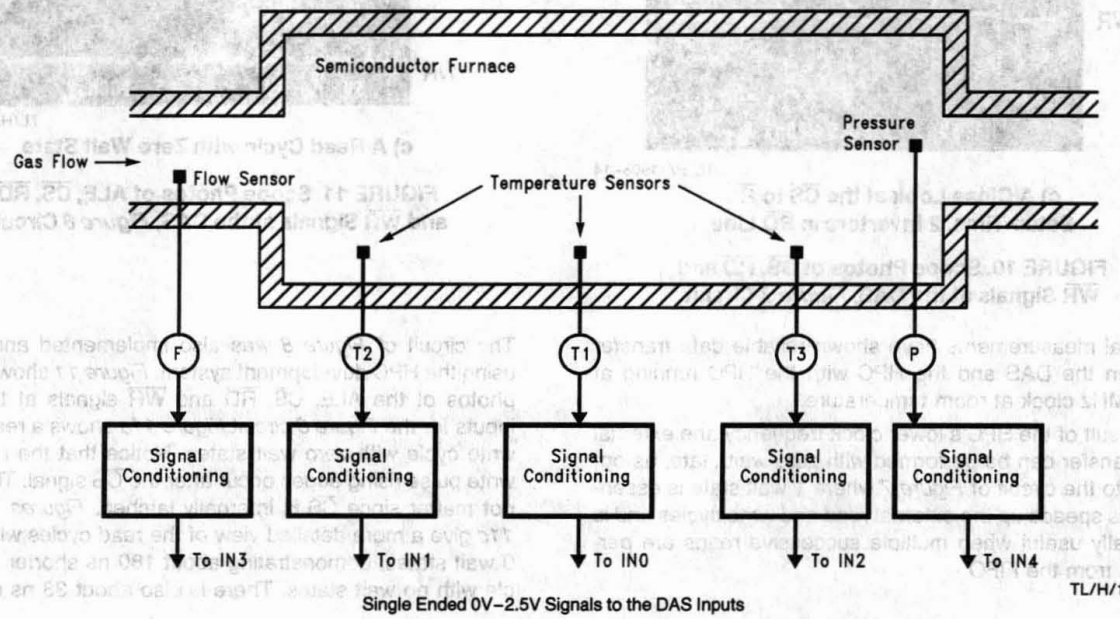


FIGURE 12. Diagram of a Typical Measurement Arrangement in a Semiconductor Furnace

Seven DAS instructions are needed for measurement and limit monitoring. Five perform the conversions and two perform the "watchdog" function for comparison of "F" and "P" against programmed limits. Note that the variable "F" needs only 1 instruction to monitor both high and low limits.

The following procedures are assumed for system operations:

— The seven instructions are executed in sequence from 0 to 6 with zero delay between them.

— After execution of instruction #6 the DAS loops back to instruction #0 and continues. Each loop is called an instruction loop.

— A delay is added, using the Timer register, before instruction #0 to provide 50 Hz throughput rate.

— Each instruction loop generates 5 conversion results. The FIFO is filled with 30 (6 sets of 5) results and is then read by the microcontroller. This is done by having an interrupt (from the DAS to the HPC) when a specified number of results are contained in the FIFO.

— Conversion will not be stopped during FIFO reads. Reads are performed during last comparison instruction (#6) and during the delay before instruction #0. The reads add extra delay after each six instruction loop, but the amount of the delay is negligible compared to the 20 ms loop duration. (See Section 2.3 for a discussion on reading during conversion and the interruption of the internal clock during reads and writes.)

The input from the flow sensor has a 600Ω source impedance, so it requires additional acquisition time. Referring to the equation in the DAS data sheet, for the 8-bit and "watchdog" mode, the acquisition time value (D) programmed in bits D12 through D15 of the Instruction register should be equal to 2 ($D = 0.36 \times Rs(k\Omega) \times f_{clk}(MHz) = 0.36 \times 0.6 \times 8 = 1.73$).

Now the contents of the DAS registers can be specified.

INSTRUCTION REGISTER:

— Sync and Pause bits are not used.

Instruction Register definition:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Acquisition Time				W-dog	8/12	Timer	Sync	V_{IN}^-			V_{IN}^+			Paus.	Loop

Instruction #0: Measuring T1, Single Ended, 12-Bit, Timer enabled

V_{IN}^+ = IN0 (T1), V_{IN}^- = AGND

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Instruction #1: Measuring T1–T2, Differential mode, 12-Bit + sign

V_{IN}^+ = IN0 (T1), V_{IN}^- = IN1 (T2)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Instruction #2: Measuring T1–T3, Differential mode, 12-Bit + sign

V_{IN}^+ = IN0 (T1), V_{IN}^- = IN2 (T3)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Instruction #3: Measuring F, Single Ended, 8-Bit, D = 2

V_{IN}^+ = IN3 (F), V_{IN}^- = AGND

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	0	0	0	0	0	1	1	0	0

Instruction #4: Watchdog mode, F, Single Ended, D = 2

V_{IN}^+ = IN3 (F), V_{IN}^- = AGND

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0

Instruction #5: Measuring P, Single Ended, 8-Bit

V_{IN}^+ = IN4 (P), V_{IN}^- = AGND

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0

Instruction #6: Watchdog mode, P, Single Ended, Loop bit enabled

V_{IN}^+ = IN4 (P), V_{IN}^- = AGND

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1

Instruction #7: Not Used

Instructions #4 and #6 also have limit values. Instruction #4 has two limit values and instruction #6 has only one limit value. These values are referred to as F_MIN, F_MAX, P_MAX.

Instruction RAM, Limits definition:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care						>/<	Sign	Limit							

Instruction #4, Limit #1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	F_MAX							

Instruction #4, Limit #2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	F_MIN							

Instruction #6, Limit #1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	P_MAX							

Instruction #6, Limit #2, Limit value equal negative full-scale to prevent false interrupts.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

INTERRUPT ENABLE REGISTER:

— INT0: Comparison Limit: Enable
— INT1: Instruction Number: Disable
— INT2: FIFO Full: Enable
— INT3: Auto Zero Complete: Disable
— INT4: Calibration Complete: Enable
— INT5: Pause: Disable
— INT6: Low Supply: Disable
— INT7: Standby Return: Disable
— Programmed instruction number: 0, Not used
— Programmed number of results in FIFO: 30 (11110 binary)

Interrupt Enable Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Number of results in FIFO				Instruction Number				INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
1	1	1	1	0	0	0	0	0	0	0	1	0	1	0	1

CONFIGURATION REGISTER:

— No auto zero or calibration before each conversion.

— Instruction number on bits D13 to D15 of the conversion results.

— Sync bit is not used and can be programmed as either input or output.

Configuration Register, Start Conversion Command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care				Diag.	Test	RAM Pointer		Sync I/O	A/Z Each	Chan Mask	Stand-by	Full Cal	Auto Zero	Reset	Start
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Configuration Register, Reset Command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Configuration Register, Full Calibration Command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Configuration Register, RAM bank 1 Selection Command (Conversion is stopped)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Configuration Register, stopping the Conversion Command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TIMER REGISTER:

To calculate the timer preset value, we must first calculate the total instruction execution time. The following table shows the number of clock cycles for each instruction. Please see datasheet, Section 4.0 (Sequencer), for the discussion of the states and their duration.

Instruction #	State 0	State 1	State 7	State 6	State 4	State 5	Number of Clock Cycles
0	1	1	9			44	55
1	1	1	9			44	55
2	1	1	9			44	55
3	1	1	2			21	25
4	1	1	2	5	1	5	15
5	1	1	6			21	29
6	1	1	6	5	1	5	19
						Total:	253

There is a total of 253 clock cycles required for instruction execution. The Timer delay includes a fixed 2 clock cycles that must be added to 253, resulting in

$$253 + 2 = 255 \text{ clock cycles.}$$

The total time for 255 clock cycles would be:

$$255 \times 1/8 \text{ MHz} = 31.875\ \mu\text{s.}$$

This time must be subtracted from 20 ms to get the Timer delay.

$$20 \text{ ms} - 31.875\ \mu\text{s} = 19.968 \text{ ms.}$$

A Timer count is 32 clock cycles, with an 8 MHz clock (125 ns period), each Timer count is

$$32 \times 125 \text{ ns} = 4\ \mu\text{s.}$$

The timer preset value is then

$$19.968 \text{ ms} \div 4\ \mu\text{s} = 4992,$$

with a hex value of 1380H.

Once the required contents of the DAS registers have been determined, the next step is to program the processor to interact with the DAS.

4.3 Microcontroller Programming

Interaction between a microcontroller and the DAS is basically accomplished by read and write operations, the microcontroller's external data transfer instructions are used for communications with the DAS.

A write operation to the DAS needs 2 variables: The DAS register address and the data to be written. A read operation from the DAS needs only the register address. The DAS register address and data will be referred to as DAS__REG__ADD and DAS__DATA in the following examples.

Examples of assembly mnemonics for the DAS read and write operations are presented below for the HPC, 8051, and 68HC11 microcontroller families:

The HPC family can directly write 16-bit data to a memory-mapped I/O. Its main data transfer instruction is "LD" (load). Each read or write is only one instruction.

Write:

```
LD    DAS_REG_ADD,#DAS_DATA
```

Read:

```
LD    [destination],DAS_REG_ADD
```

The 8051 family accesses an external memory-mapped I/O indirectly through the DPTR (data pointer) register. The data should be preloaded to the accumulator for writes and the accumulator is the destination for reads. The transfer is 8-bit and two cycles are needed for 16 bits of data. The basic instruction are "MOV" (move), "MOVX" (move external) and "INC" (increment).

Write:

```
MOV   DPTR,#DAS_REG_ADD
MOV   A,DAS_DATA(low byte)
MOVX  @DPTR,A
INC   DPTR
MOV   A,DAS_DATA(high byte)
MOVX  @DPTR,A
```

Read:

```
MOV DPTR,#DAS_REG_ADD
MOVXA,@DPTR
MOV [destination],A
INC DPTR
MOVXA,@DPTR
```

The above examples assume 16-bit addressing, however registers R0 or R1 of the 8051 can be used in place of DPTR for 8-bit addressing.

The 68HC11 family can access external memory mapped I/O directly. The data should be preloaded to the accumulator for writes and the accumulator is the destination for reads. Although, the 68HC11 is an 8-bit processor, it has 16-bit data transfer instructions that uses a double accumulator (A + B, called D) and performs 2 transfer cycles using a single instruction. The basic instructions are "LDD" (load double accumulator) and "STD" (store double accumulator).

Write:

```
LDD   #DAS_DATA
STD   DAS_REG_ADD
```

Read:

```
LDD   DAS_REG_ADD
```

4.3.1 HPC Assembly Routines for the Semiconductor Furnace Example

The program listing in *Figure 13* is the HPC assembly routine for the semiconductor furnace application example. The program contains only the DAS initialization and the DAS interrupt service routine. A complete program for the application will have all the data manipulation and control functions, which are not discussed here.

The routines closely follow the procedure in the flowcharts of *Figure 2* and are extensively commented to be self-explanatory. The routines also separated according to the flowchart sections. The main difference between the routines and the flowchart is that the DAS is not stopped at the start of the interrupt service routine.

The interrupt service routine uses the IFBIT (if bit is true) instruction to test for the state of the interrupt status bits. This is very handy for control applications.

The READ__FIFO routine reads the FIFO contents and stores them to a specified block of memory starting at the location called DAS__RESULT. The size of the block and, consequently, the number of FIFO locations being read is programmable (30 locations on the listing). The routine is only 5 lines of assembly. It uses the multi-function "XS" (exchange and skip) instruction to perform the data transfer, address increment or decrement, and a compare for decision making. The first LD instruction in the READ__FIFO routine loads the HPC's B and K registers with the starting address and the ending address of the memory block. The second instruction reads a word (16-bit) from the FIFO to "A" (accumulator). The XS instruction stores A in the memory location pointed to by B, increments B by 2 (for 2 bytes) and then compares B with K to test for the end of the memory block. If the end of the block has not been reached, the program jumps back to load the next word from the FIFO, otherwise the program skips the "JP" (jump) instruction and returns from the service routine.

```
1
2                       #NOHEADING
3                       #PWIDTH= 112
4
5                       ;*****************************************************************************
6                       ;*                                                                           *
7                       ;* AN HPC ASSEMBLY ROUTINE FOR THE SEMICODUCTOR APPLICATION EXAMPLE FOR THE *
8                       ;*   APPLICATION NOTE "INTERFACING THE LM12454/8 DATA ACQUISITION SYSTEM     *
9                       ;*             CHIPS TO MICROPROCESSORS AND MICROCONTROLLERS"                *
10                      ;*                                                                           *
11                      ;* BY: FARID SALEH                                                           *
12                      ;* DATE: 7/27/93                                                             *
13                      ;*****************************************************************************
14
15
16                      ;****** HPC REGISTERS SYMBOLIC DEFINITIONS ******
17
18 00C0                         PSW     = 0C0H          ;PROCESSOR STATUS REGISTER
19                      ;       SP      = 0C4H          ;STACK POINTER
20                      ;       PC      = 0C6H          ;PROGRAM COUNTER
21                      ;       A       = 0C8H          ;ACCUMULATOR
22                      ;       K       = 0CAH          ;K REGISTER
23                      ;       B       = 0CCH          ;B REGISTER
24                      ;       X       = 0CEH          ;X REGISTER
25 00E2                         PORTB   = 0E2H          ;PORT B DATA REGISTER
26 00F2                         DIRB    = 0F2H          ;PORT B DIREGTION REGISTER
27 00F4                         BFUN    = 0F4H          ;PORT B ALTERNATE FUNCTION REGISTER
28 00D0                         ENIR    = 0D0H          ;INTERRUPT ENABLE REGISTER
29 00D4                         IRCD    = 0D4H          ;INTERRUPT / INPUT CAPTURE CONDITION REGISTER
30 00D2                         IRPD    = 0D2H          ;INTRUPT PENDING REGISTER
31
32                      ;****** DAS REGISTERS / VARIABLES / CONSTANTS  SYMBOLIC DEFINITIONS ******
33
34 0200                         INSTR0  = 0200H         ;DAS INSTRUCTION REGISTER ADDRESSES
35 0202                         INSTR1  = 0202H         ;READ/WRITE REGISTERS
36 0204                         INSTR2  = 0204H         ; "
37 0206                         INSTR3  = 0206H         ; "
38 0208                         INSTR4  = 0208H         ; "
39 020A                         INSTR5  = 020AH         ; "
40 020C                         INSTR6  = 020CH         ; "
41 020E                         INSTR7  = 020EH         ; "
42
43 0210                         CONFIG  = 0210H         ;DAS CONFIGURATION REGISTER ADDRESS, R/W
44 0212                         INTEN   = 0212H         ;DAS INTERRUPT ENABLE REG. ADDRESS, R/W
45 0214                         INTSTAT = 0214H         ;DAS INTERRUPT STATUS REG. ADD. READ ONLY
46 0216                         TIMER   = 0216H         ;DAS TIMER REG. ADDRESS, R/W
47 0218                         FIFO    = 0218H         ;DAS FIFO ADDRESS, READ ONLY
48 021A                         LMTSTAT = 021AH         ;DAS LIMIT STATUS REG. ADD. READ ONLY
49
50 01C0                         DAS_RESULT = 01C0H      ;START ADDRESS OF TOP 64 LOCATION OF HPC
51                                                      ;ON-CHIP RAM TO STORE CONVERSION RESULTS
52 00BC                         DAS_INT_MEM = 00BCH     ;HPC MEMORY LOCATION TO STORE INTERRUPT
53                                                      ;STATUS REGISTER
54 00BE                         DAS_LIM_MEM = 00BEH     ;HPC MEMORY LOCATION TO STORE LIMIT STATUS
55                                                      ;REGISTER
56 001E                         FIFO_CNT = 30           ;NUNBER OF RESULTS IN FIFO, A DECIMAL VALUE
57 1380                         TIMER_SET = 01380H      ;TIMER PRESET VALUE
58
59 00FF                         F_MAX   = 0FFH          ;HIGH LIMIT FOR GAS FLOW
60 0000                         F_MIN   = 000H          ;LOW LIMIT FOR GAS FLOW
61 00FF                         P_MAX   = 0FFH          ;HIGH LIMIT FOR PRESSURE
62
63 00BA                         FLAGS   = 00BAH         ;GENERAL SOFTWARE FLAGS BYTE
64 0000                         CAL_FLG = 0             ;BIT 0 OF FLAGS BYTE FOR CALLIBRATION
65
66 0000                 .SECT PDASTST,ROM16
67
```

TL/H/11908–18

FIGURE 13. HPC Assembly Program Listing (Continued)

```
                        ;******  HPC INITIALIZATION ******
                        START:
0000 9718C0                     LD      PSW.B,#018H             ;PROCESSOR STATUS WORD,EXPANDED MODE
                                                                ;1 WAIT STATE, CAN BE ZERO WAIT STATE
                                                                ;FOR CIRCUIT IN FIGURE 8, #01CH
0003 9700D0                     LD      ENIR.B,#00H             ;DISABLE ALL INTERRUPTS
0006 9700D2                     LD      IRPD.B,#00H             ;CLEAR ANY INTERRUPT PENDING BIT
0009 9700D4                     LD      IRCD.B,#00H             ;SET I4 FOR HIGH TO LOW EDGE DETECT
000C B70000E2                   LD      PORTB.W,#00H            ;PORT B ALL ZERO
0010 B7FFFFF2                   LD      DIRB.W,#0FFFFH          ;PORT B ALL OUTPUTS, B10,11,12 AND 15
                                                                ;ARE PREDEFINED DUE TO EXPANDED MODE
                                                                ;NOTE: PORT A IS ALSO PREDEFINED
0014 B70000F4                   LD      BFUN.W,#00H             ;PORT B NO ALTERNATE FUNCTION

                        ;****** DAS REGISTERS INITIALIZATION ******
0018 83020210AB                 LD      CONFIG.W,#0002H         ;RESET, SELECT RAM SECTION 0, RP=00

001D 8702000200AB               LD      INSTR0.W,#0200H         ;INSTRUCTIONS INITIALIZATION, VALUES
0023 83200202AB                 LD      INSTR1.W,#0020H         ;ARE AS SPECIFIED ON THE SYSTEM
0028 83400204AB                 LD      INSTR2.W,#0040H         ;DESIGN
002D 87240C0206AB               LD      INSTR3.W,#0240CH        ; "
0033 87280C0208AB               LD      INSTR4.W,#0280CH        ; "
0039 870410020AAB               LD      INSTR5.W,#0410H         ; "
003F 870811020CAB               LD      INSTR6.W,#0811H         ; "

0045 8701000210AB               LD      CONFIG.W,#0100H         ;SELECT RAM SECTION 1, RP=01

004B 8702FF0208AB               LD      INSTR4.W,#(0200H+F_MAX) ;HIGH LIMIT FOR INSTRUCTION 4
0051 8702FF020CAB               LD      INSTR6.W,#(0200H+P_MAX) ;HIGH LIMIT FOR INSTRUCTION 6

0057 8702000210AB               LD      CONFIG.W,#0200H         ;SELECT RAM SECTION 2, RP=10

005D 83000208AB                 LD      INSTR4.W,#(0000H+F_MIN) ;LOW LIMIT FOR INSTRUCTION 4
0062 870100020CAB               LD      INSTR6.W,#0100H         ;LOW LIMIT FOR INSTRUCTION 6
                                                                ;NEGATIVE FULL-SCALE, NOT USED

0068 87F0150212AB               LD      INTEN.W,#((FIFO_CNT*2048)+015H)
                                                                ;SHIFT FIFO_CNT TO MSBs OF HIGH
                                                                ;BYTE, THEN ADD LOW BYTE (015H),
                                                                ;DAS INT # 0, 2 AND 4 ARE ENABLED
006E 8713800216AB               LD      TIMER.W,#TIMER_SET      ;TIMER INITIALIZED WITH PRESET VALUE

                        ;****** ENABLING HPC INTERRUPT #4 ******
0074 9711D0                     LD      ENIR.B,#011H            ;ENABLE HPC GLOBAL AND INTERRUPT #4

                        ;****** DAS FULL CALIBRATION ******
0077 96BA08                     SBIT    CAL_FLG,FLAGS.B         ;SET CALIBRATION FLAG FOR PROGRAM
                                                                ;CONTROL
007A 83080210AB                 LD      CONFIG.W,#0008H         ;DAS CALIBRATION IS STARTED

007F 96BA10             WAIT1:  IFBIT   CAL_FLG,FLAGS.B         ;CHECK FOR CAL_FLG, IF 1 WAIT,
                                                                ;IDEL LOOP UNTIL CALIBRATION IS DONE
0082 63                         JP      WAIT1                   ;AND INTRRUPT FROM DAS IS RECEIVED,
                                                                ;IN A COMPLETE PROGRAM, PROCESSOR
                                                                ;CAN DO OTHER TASKS

                        ;****** STARTING THE CONVERSIONS ******
0083 83010210AB                 LD      CONFIG.W,#0001H         ;START BIT = 1, DAS STARTS

0088 60                 WAIT2:  JP      WAIT2                   ;IDEL LOOP FOR HPC TO WAIT FOR DAS
                                                                ;INTERRUPT
                                                                ;THIS IS MAINLY A TEST STATEMENT HERE
                                                                ;AND IN A COMPLETE PROGRAM PROCESSOR
                                                                ;IS DOING OTHER TASKS
```

TL/H/11908–19

FIGURE 13. HPC Assembly Program Listing (Continued)

```
139                          ;****** THE DAS INTERRUPT SERVICE RUTINE ******
140
141 FFF6 8900            R   .IPT 4, DAS_INTSERV                  ;ASSEMBLER INTERRUPT ADDRESS DIRECTIVE
142
143 0089                     DAS_INTSERV:
144
145 0089 AFC8                        PUSH    A                    ;PUSH INSTRUCTIONS TO SAVE REGISTER
146 008B AFCC                        PUSH    B                    ;CONTENTS ON STACK, A, B, K, X AND
147 008D AFCA                        PUSH    K                    ;PSW ARE SHOWN AS GENERAL PURPOSE
148 008F AFCE                        PUSH    X                    ;REGISTERS, IF REGISTERS ARE NOT USED
149 0091 AFC0                        PUSH    PSW.W                ;IN INTERRUPT SERVICE ROUTINES, THEY
150                                                               ;CAN BE DELETED FROM THE LIST
151
152 0093 A40214BCAB                  LD      DAS_INT_MEM.W,INTSTAT.W ;STORE CONTENTS OF DAS INTERRUPT REG.
153                                                               ;IN HPC MEMORY FOR BIT TESTING
154
155                          ;****** INDIVIDUAL BITS IN THE DAS_INT_MEM ARE TESTED AND DIFFERENT ******
156                          ;****** ROUTINS WILL SERVE INDIVIDUAL CASES
157
158 0098 96BC12                      IFBIT   2,DAS_INT_MEM.B      ;IF INTERRUPT IS FROM FIFO FULL
159 009B 4E                          JP      READ_FIFO            ;JUMP TO ROUTINE READ_FIFO
160                                                               ;OTHERWISE TEST THE NEXT BIT
161 009C 96BC10                      IFBIT   0,DAS_INT_MEM.B      ;IF ANY LIMITS IS PASSED JUMP TO
162 009F 49                          JP      DAS_LIMIT            ;ROUTINE DAS_LIMIT FOR ACTION
163                                                               ;OTHERWISE MOVE ON
164 00A0 83020210AB                  LD      CONFIG.W,#0002H      ;IF NON OF THE ABOVE BITS MUST BE
165 00A5 96BA18                      RBIT    CAL_FLG,FLAGS.B      ;CALIBRATION COMPLETE, RESET THE DAS
166 00A8 4C                          JP      DONE                 ;AND CAL_FLG, THEN RETURN
167
168                          ;****** SERVICE ROUTINE DAS_LIMIT ******
169
170 00A9                     DAS_LIMIT:
171
172                                  ;BODY OF THE SERVICE ROUTINE
173                                  ;THIS ROUTINE SHOULD READ THE DAS LIMIT STATUS REGISTER AND TEST THE
174                                  ;NECESSARY BITS, BASED ON WHAT BIT IS SET THE PROPER ACTION IS TAKEN
175                                  ;
176 00A9 4B                          JP      DONE
177
178
179                          ;****** SERVICE ROUTINE READ_FIFO ******
180
181 00AA                     READ_FIFO:
182
183 00AA A701C001FA                  LD      BK.W,#DAS_RESULT,#(DAS_RESULT+2*FIFO_CNT-2)
184                                                               ;LOAD B FOR STARTING ADDRESS OF THE
185                                                               ;BLOCK TO BE FILLED WITH FIFO,
186                                                               ;SET K FOR UPPER LIMIT OF THE BLOCK
187
188 00AF B60218A8              LPFIFO: LD      A,FIFO.W             ;LOAD ACC WITH FIFO CONTENTS, FIFO
189                                                               ;POINTER IS INCREMENTED ON EACH READ
190 00B3 E1                          XS      A,[B+].W             ;STORE ACC TO THE HPC's RAM WITH B
191                                                               ;AUTO-INCREMENT AND SKIP IF GREATER
192                                                               ;THAN K
193 00B4 65                          JP      LPFIFO
194
195
196 00B5 3FC0                DONE:   POP     PSW.W                ;RELOAD THE SAVED REGISTERS BACK
197 00B7 3FCE                        POP     X                    ;FROM STACK
198 00B9 3FCA                        POP     K                    ;
199 00BB 3FCC                        POP     B                    ;
200 00BD 3FC8                        POP     A                    ;
201
202 00BF 3E                          RETI                         ;RETURN FROM INTRRUPT ROUTINE
203
204 00C0                     .END START

**** Errors:    0, Warnings:    0
```

TL/H/11908–20

FIGURE 13. HPC Assembly Program Listing

APPENDIX A: Registers Bit Assignments and Programmer's Notes

CONFIGURATION REGISTER (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care				Diag.	Test	RAM Pointer		Sync I/O	A/Z Each	Chan Mask	Stand-by	Full Cal	Auto Zero	Reset	Start

D0: - Start: 0 = Stops the instruction execution. 1 = Starts the instruction execution

D1: - Reset: When set to 1, resets the Start bit, also resets all the bits is status registers and resets the instruction pointer to zero, will automatically reset itself to zero after 2 clock pulses

D2: - Auto-Zero: When set to 1 a long auto-zero calibration cycle is performed

D3: - Full Calibration: When set to 1 a full calibration cycle is performed

D4: - Standby: When set to 1 the chip goes to low-power standby mode, resetting the bit will return the chip to active mode after a power-up delay

D5: - Channel Mask: 0 = Bits 13 to 15 of the conversion result hold the instruction number to which the result belongs, 1 = Bits 13 to 15 of the result hold the extended sign bit

D6: - A/Z Each: When set to 1 a short auto-zero cycle if performed before each conversion

D7: - Sync I/O: 0 = Sync pin is input, 1 = Sync pin is output

D9–D8: - RAM Pointer: Selects the sections of the instruction RAM, 00 = Instructions, 01 = Limits #1, 10 = Limits #2

D10: - This bit is used for production testing, must be kept zero for normal operation

D11: - Diagnostic: When set to 1 perform diagnostic conversion along with a properly selected instruction

D15–D12: - Don't care

PROGRAMMER'S NOTES:

Configuration Registers: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Configuration Register: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Configuration Register: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

APPENDIX A: Registers Bit Assignments and Programmer's Notes

INSTRUCTION RAM (Read/Write): (Continued)

Instruction:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Acquisition Time				W-dog	8/12	Timer	Sync	$V_{IN}-$			$V_{IN}+$			Paus.	Loop

D0: - Loop: 0 = Go to next instruction, 1 = Loop back to instruction #0

D1: - Pause: 0 = No pause, 1 = Pause, don't do the instruction, Start bit in configuration register resets to 0 when a pause encountered, a 1 written to Start bit restarts the instruction execution

D4–D2: - $V_{IN}+$: Selects which input channel is connected to A/D's non-inverting input

D7–D5: - $V_{IN}-$: Selects which input channel is connected to A/D's inverting input

D8: - Sync: 0 = Normal operation, internal timing, 1 = S/H and conversion (comparison) timing, is controlled by SYNC input pin

D9: - Timer: 0 = No timer operation, 1 = Instruction execution halts until timer counts down to zero

D10: - 8/12: 0 = 12-bit + sign resolution, 1 = 8-bit + sign resolution

D11: - Watchdog: 0 = No watchdog comparision, 1 = Instruction performs watchdog comparisons

D15–D12: - Acquisition Time: Determines S/H acquisition time
For 12-bit + sign: (9 + 2D) clock cycles, For 8-bit + sign: (2+2D) clock cycles
D = Content of D15–D12, R_S = Input source resistance
For 12-bit + sign: $D = 0.45 \times R_S[k\Omega] \times f_{CLK}[MHz]$
For 8-bit + sign: $D = 0.36 \times R_S[k\Omega] \times f_{CLK}[MHz]$

PROGRAMMER'S NOTES:

Instruction # 0: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction #3: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

APPENDIX A: Registers Bit Assignments and Programmer's Notes

INSTRUCTION RAM (Read/Write): (Continued)

PROGRAMMER'S NOTES:

Instruction # 4: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 5: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 6: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 7: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

APPENDIX A: Registers Bit Assignments and Programmer's Notes

INSTRUCTION RAM (Read/Write): (Continued)

Limits # 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care						>/<	Sign	Limit							

D7–D0: - Limit: 8-bit limit value

D8: - Sign: Sign bit for limit value, 0 = Positive, 1 = Negative

D9: - >/<: High or low limit determination, 0 = Inputs lower than limit generate interrupt, 1 = Inputs higher than limit generate interrupt

D15–D10 - Don't Care

PROGRAMMER'S NOTES:

Instruction # 0, Limit # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 1, Limit # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 2, Limit # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 3, Limit # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 4, Limit # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 5, Limit # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 6, Limit # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 7, Limit # 1: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

APPENDIX A

INSTRUCTION RAM (Read/Write): (Continued)

Limits #2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care						>/<	Sign	Limit							

D7–D0: - Limit: 8-bit limit value

D8: - Sign: Sign bit for limit value, 0 = Positive, 1 = Negative

D9: - >/<: High or low limit determination, 0 = Inputs lower than limit generate interrupt, 1 = Inputs higher than limit generate interrupt

D15–D10 - Don't Care

PROGRAMMER'S NOTES:

Instruction # 0, Limit # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 1, Limit # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 2, Limit # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 3, Limit # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 4, Limit # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 5, Limit # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 6, Limit # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Instruction # 7, Limit # 2: Address: Symbol:
Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

APPENDIX A: Registers Bit Assignments and Programmer's Notes

INTERRUPT ENABLE REGISTER (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Number of results in FIFO to Generate Interrupt (INT2)					Instruction Number to Generate Interrupt (INT1)			INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0

Bits # 0 to 7 enable interrupt generaton for the following conditions when the bit is set to 1.

D0: - INT0: Generates interrupt when a limit is passed in watchdog mode

D1: - INT1: Generates interrupt when the programmed instruction (D10–D8) is reached for execution

D2: - INT2: Generates interrupt when number of conversion results in FIFO is equal to the programmed value (D15–D11)

D3: - INT3: Generates interrupt when an auto-zero cycle is completed

D4: - INT4: Generates interrupt when a full calibration cycle is completed

D5: - INT5: Generates interrupt when a pause condition is encountered

D6: - INT6: Generates interrupt when low power supply is detected

D7: - INT7: Generates interrupt when the chip is returned from standby and is ready

D10–D8: - Programmable instruction number to generate an interrupt when that instruction is reached foR execution

D15–D11: - Programmable number of conversion results in the FIFO to generate an interrupt

PROGRAMMER's NOTES:

Interrupt Enable Register: Address: Symbol:

Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Interrupt Enable Register: Address: Symbol:

Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

TIMER REGISTER (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
N = Timer Preset Value															

Timer delays the execution of an instruction if Timer bit is set in the instruction.
The time delay in number of clock cycles is:

Delay = 32 x N + 2 [Clock Cycles]

PROGRAMMER's NOTES:

Timer Register: Address: Symbol

Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

Timer Register: Address: Symbol:

Note:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Hexadecimal value:

APPENDIX A: Registers Bit Assignments and Programmer's Notes

FIFO REGISTER (Read only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Instruction Number or Extended Sign			Sign	Conversion Result											

D11–D0: - Conversion Result:
For 12-bit + sign: 12-bit result value
For 8-bit + sign: D11–D4 = result value, D3–D0 = 1110

D12: - Sign: Conversion result sign bit, 0 = Positive, 1 = Negative

D15–D13: - Instruction number associated with the conversion result or the extended sign bit for 2's complement arithmetic, selected by bit D5 (Chan Mask) of Configuration Register

PROGRAMMER'S NOTES:

FIFO Register: Address: Symbol:
Note:

INTERRUPT STATUS REGISTER (Read only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Number of results in FIFO					Instruction Number Being executed			INST7	INST6	INST5	INST4	INST3	INST2	INST1	INST0

BITS # 0 to 7 are interrupt flags (vectors) that will be set to 1 when the following conditions occur. The bits set to 1 whether the interrupt is enabled or disabled in the Interrupt Enable register. The bits reset to 0 when the register is read, or by a device reset through Configuration register.

D0: - INST0: Is set to 1 when a limit is passed in watchdog mode

D1: - INST1: Is set to 1 when the programmed instruction (D10–D8) is reached for execution

D2: - INST2: Is set to 1 when number of conversion results in FIFO is equal to the programmed value (D15–D11)

D3: - INST3: Is set to 1 when an auto-zero cycle is completed

D4: - INST4: Is set to 1 when a full calibration cycle is completed

D5: - INST5: Is set to 1 when a pause condition is encountered

D6: - INST6: Is set to 1 when low power supply is detected

D7: - INST7: Is set to 1 when the chip is returned from standby and is ready

D10–D8: - Holds the instruction number being executed or will be executed during a Pause or Timer delay

D15–D11: - Holds the present number of conversion results in the FIFO while the device is running

PROGRAMMER'S NOTES:

Interrupt Status Register: Address: Symbol:
Note:

APPENDIX A: Registers Bit Assignments and Programmer's Notes

LIMIT STATUS REGISTER (Read only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Limits # 2: Status								Limits # 1: Status							

The bits in this register are limit flags (vectors) that will be set to 1 when a limit is passed. The bits are associated to individual instruction limits as indicated below.

D0: - Limit # 1 of Instruction # 0 is passed
D1: - Limit # 1 of Instruction # 1 is passed
D2: - Limit # 1 of Instruction # 2 is passed
D3: - Limit # 1 of Instruction # 3 is passed
D4: - Limit # 1 of Instruction # 4 is passed
D5: - Limit # 1 of Instruction # 5 is passed
D6: - Limit # 1 of Instruction # 6 is passed
D7: - Limit # 1 of Instruction # 7 is passed
D8: - Limit # 2 of Instruction # 0 is passed
D9: - Limit # 2 of Instruction # 1 is passed
D10: - Limit # 2 of Instruction # 2 is passed
D11: - Limit # 2 of Instruction # 3 is passed
D12: - Limit # 2 of Instruction # 4 is passed
D13: - Limit # 2 of Instruction # 5 is passed
D14: - Limit # 2 of Instruction # 6 is passed
D15: - Limit # 2 of Instruction # 7 is passed

PROGRAMMER'S NOTES:

Limit Status Register: Address Symbol:
Note:

Multivibrator/Timer CAD

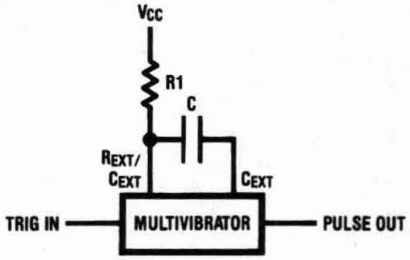
National Semiconductor
Application Brief 7

Circuit design making use of monolithic multivibrators and timers can be most easily and quickly done making use of a simple CAD (computer aided design) program. Fortunately, only 2 basic multivibrator types and 1 timer design type exist, reducing the program requirements to 3 sets of algorithms.

Figure 1 provides a view of the basic multivibrator and the t_{ON} (pulse width) determining resistor and capacitor (R1 and C). the Advanced Bipolar Logic Databook by National Semiconductor Corporation should be consulted for the specific device pinout and functions.

Figure 2 is a block diagram showing the basic timer and the t_{ON} (pulse width) determining resistor and capacitor (R1 and C) along with the t_{OFF} determining resistor R2 (required if astable operation is required). The Linear Databook by National Semiconductor should be consulted for the specific device pinout and additional device functions.

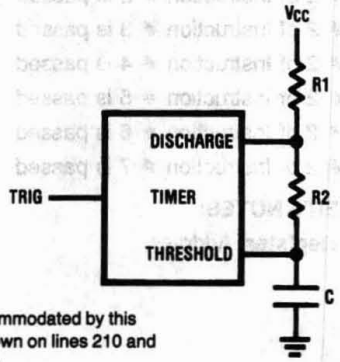
This program is in "transportable" BASIC. No INPUT prompts for strings or ELSE statements are used. All IF statements, if true, result in a GOTO. Variable and array names are unique and are limited to 2 characters in length. This program consists of multiple statement lines, which must be dissected for some unexpanded microcomputers. Some microcomputers may require that the DATA statements on lines 850 and 860 be implemented as strings, and the READ statement on line 250 be replaced with the string handling routine.



TL/H/5248–1

Multivibrators accommodated by this program are shown in lines 130 through 200 of the listing.

FIGURE 1



The timers accommodated by this program are shown on lines 210 and 220 of the listing.

FIGURE 2

TL/H/5248–2

```
100 For I=0 to 10:PRINT:NEXT
110 PRINT"MULTIV by Bob Nelson — 2/1/83":PRINT:PRINT
120 PRINT"The following multivibrators are available for design:":Print
130 PRINT"DM54/74121          One Shots                                  0"
140 PRINT"DM54/74LS122        Retriggerable One Shots with Clear         1"
150 PRINT"DM54/74123          Dual Retriggerable One Shots with Clear    2"
160 PRINT"DM54/74L123         Dual Retriggerable One Shots with Clear    3"
170 PRINT"DM54/74LS123        Dual Retriggerable One Shots with Clear    4"
180 PRINT"DM54/74LS221        Dual One Shots with Schmitt-Trigger Inputs 5"
190 PRINT"DM86/9601           Retriggerable One Shots                    6"
200 PRINT"DM86/9602           Dual Retriggerable, Resettable One Shots   7"
210 PRINT"LM555/555C          Timer                                      8"
220 PRINT"LM556/556C          Dual Timer                                 9"
230 PRINT:INPUT"Enter number representing choice . . . . . ",N:PRINT
240 IF N>9 THEN 100
250 FOR I=0 TO N:READ K:READ RN:READ RX:NEXT:IF K<>.693 THEN 270
260 PRINT"Astable or Monostable (A/M)";:INPUT M$
270 INPUT"Ton in nanoSeconds";T1:IF M$<>"A" THEN 300
280 INPUT"Toff in nanoSeconds";T2:IF 2*T2=<T1 THEN 300
290 PRINT"Toff cannot exceed 50% of Ton":PRINT:GOTO 270
300 INPUT"R1 in Kohms";R1:GOSUB 740:IF M$<>"A" THEN 320
310 INPUT"R2 in Kohms";R2
320 IF T1>0 AND R1>0 THEN 340
```

```
330 INPUT"C in picoFarads";C
340 IF K=.693 THEN 530
350 IF T1>0 AND R1>0 THEN 490
360 IF T1>0 AND C>0 THEN 450
370 IF R1>0 AND C>0 THEN 410
380 IF R1>0 THEN 400
390 R1=RN:GOSUB 730:GOTO 350
400 GOSUB 710:GOTO 690
410 IF K=0 THEN 430
420 T1=K*C*(R1+.7):GOTO 440
430 T1=.7*C*R1
440 GOSUB 720:GOTO 690
450 IF K=0 THEN 470
460 R1=T1/(K*C-.7):GOTO 480
470 R1=T1/(.7*C)
480 GOSUB 730:GOTO 690
490 IF K=0 THEN 510
500 C=T1/(K*(R1+.7)):GOTO 520
510 O=T1/(.7*R1)
520 GOSUB 790:GOTO 690
530 IF T1=0 THEN 570
540 IF T2>0 AND R1>0 AND R2>0 THEN 680
550 IF R1>0 AND T2=0 AND R2=0 THEN 680
560 IF C>0 THEN 650
570 IF R1=0 THEN 600
580 IF C>0 THEN 620
590 IF R1>0 THEN 610
600 R1=RN:GOSUB 730:GOTO 530
610 GOSUB 710
620 T1=K*(R1+2*R2)*C:T2=K*R2*C:GOSUB 720:IF M$<>"A" THEN 640
630 PRINT"Toff =";T2;"nS"
640 GOTO 690
650 R2=T2/(K*C):R1=(T1/(K*C))-2*R2:GOSUB 730:IF M$<>"A" THEN 670
660 PRINT"R2 =";R2;"Kohms"
670 GOTO 690
680 C=(T1+T2)/(K*(R1+2*R2)):GOSUB 790
690 PRINT:PRINT"Try same part again(Y/N)";:INPUT A$:IF A$<>"N" THEN 270
700 END
710 PRINT"****INSUFFICIENT DATA****": RETURN
720 PRINT"Ton =";T1;"nS":RETURN
730 PRINT"R1 =";R1;"Kohms"
740 IF R1>=RN THEN 760
750 PRINT"**** ??STABILITY - R1 <";RN;"Kohms ****"
760 IF R1=<RX THEN 780
770 PRINT"**** ??ACCURACY - R1 >";RX;"Kohms ****"
780 RETURN
790 PRINT"C =";C;"pF"
800 IF C>0 THEN GOTO 820
810 GOSUB 710:GOTO 840
820 IF C>1000 THEN 840
830 PRINT"**** ??ACCURACY - C < 1000 Pf ****"
840 RETURN
850 DATA 0, 1.4, 40, .45, 5, 260, .32, 5, 50, .33, 5, 400, .45, 5, 260
860 DATA .45, 1.4, 100, .31, 5, 50, .32, 5, 50, .693, .3, 10000, .693. .3, 10000
```

AB-10

Fluid Level Control Systems Utilizing the LM1830

National Semiconductor
Application Brief 10

Abstract. *The LM1830 fluid level detector is a device intended to signal the presence or absence of aqueous solutions. This application brief shows how to implement HIGH/LOW limit control applications utilizing this device.*

Many opportunities exist for a device that can reliably control the operation of pumps or solenoid actuated valves in fluid level control applications. Applications include sump pumps, bilge pumps, washing machines, humidifiers, plating baths, continuous replenishment photographic processors, coffee makers, municipal water and waste treatment plants, cooling towers, refrigeration equipment and others.

Classically, these needs have been met by various mechanical arrangements such as float valves or diaphragm actuated switches. These devices are bulky, inaccurate and, because they contain moving parts, unreliable—often with disastrous results when they fail. They are easily disabled by debris or environmental problems such as ice. They can be expensive when used to control the level of corrosive fluids such as plating baths or detergents, or when used to control large differences in depth such as in municipal water towers. Mechanical control devices are prone to false actuation in vehicular applications (such as bilge pump controls) due to their own inertia. In many applications such as coffee makers, they are too bulky to fit within the confines of the package. By utilizing electronic means based on the LM1830, problems inherent in mechanical solutions are overcome and a reliable, cost effective approach to fluid level control is made possible.

The LM1830 is a monolithic bipolar integrated circuit designed to detect the presence or absence of aqueous fluids. An AC signal generated on-chip is passed through two probes within the fluid. A detector determines the presence of the fluid by using the probes in a voltage divider circuit and measuring the signal level across the probes. An AC signal is used to prevent plating or dissolving of the probes as occurs when a DC signal is used. A pin is available for connecting an external resistance in cases where the fluid impedance is not compatible with the internal 13 kΩ divider resistance.

The addition of a CD4016 quad CMOS analog switch *(Figure 1)* allows the LM1830 to be used for HIGH/LOW limit control applications. The switch sections are opened and closed by a control signal, where a HIGH level turns the switch ON and a LOW level turns the switch OFF. Grounding the input of one switch section and pulling its output up with a resistor creates an inverter. Probes are connected to the inputs of two of the remaining analog switches. Their outputs are connected to pin 10 of the LM1830 which is the detector input. The remaining section of the CD4016 is used to buffer the open collector output of the LM1830. All of the control inputs of the quad analog switch are tied to this output. The last switch section controls the base of a transistor which in turn drives a relay or solenoid actuated valve.

The start and stop probes are set at their appropriate levels in the fluid container, and the ground return is connected to a third probe located at a depth greater than the start and stop probes. If the container is conductive, it may be used as the ground return. Let's assume we have a situation where we wish to empty the container when fluid reaches a predetermined level [sump or bilge pump, *Figure 1(a)*]. With no fluid covering either of the probes, pin 12 of the LM1830 switches LOW. This disables the relay and enables the analog switch connected to the start probe. Fluid eventually fills the container, covering the start probe. When this occurs, the output of the LM1830 switches HIGH and the pump relay is enabled, thereby draining the container. At the same time, the analog switch used as an inverter enables the analog switch connected to the stop probe and disables the start probe. Draining continues until the stop probe is above the level of fluid in the container. Then the output of the LM1830 switches LOW, disabling the relay (halting the drain operation) and switching the start probe back to its active state.

By reversing the labeling on the probes, as well as reversing the polarity of the relay drive, a container "fill" control is implemented such as would be used in a water tower. Necessary circuit changes are shown in *Figure 1(b)*.

A pump control for a waste water holding tank in a photographic darkroom has been implemented with this circuitry. This replaced a float actuated system which failed consistently due to the corrosive nature of the chemicals used in photographic processing. With one year of continuous service, no failures have occurred in this system. Furthermore, there is no evidence of plating on the sense electrodes, in spite of the fact that the waste water is loaded with silver ions. A plastic holding tank is used, with stainless steel bolts inserted through holes drilled in the tank as sense probes *(Figure 2)*. A solid-state relay controls a ¼ HP pump motor to empty the tank.

Obviously, careful selection of probe materials must be made to maximize reliability with this system. Excellent sources of information on materials in corrosive environments are available in publications such as Omega's *Temperature Measurement Handbook,* or Eastman Kodak's *Darkroom Design Manual.*

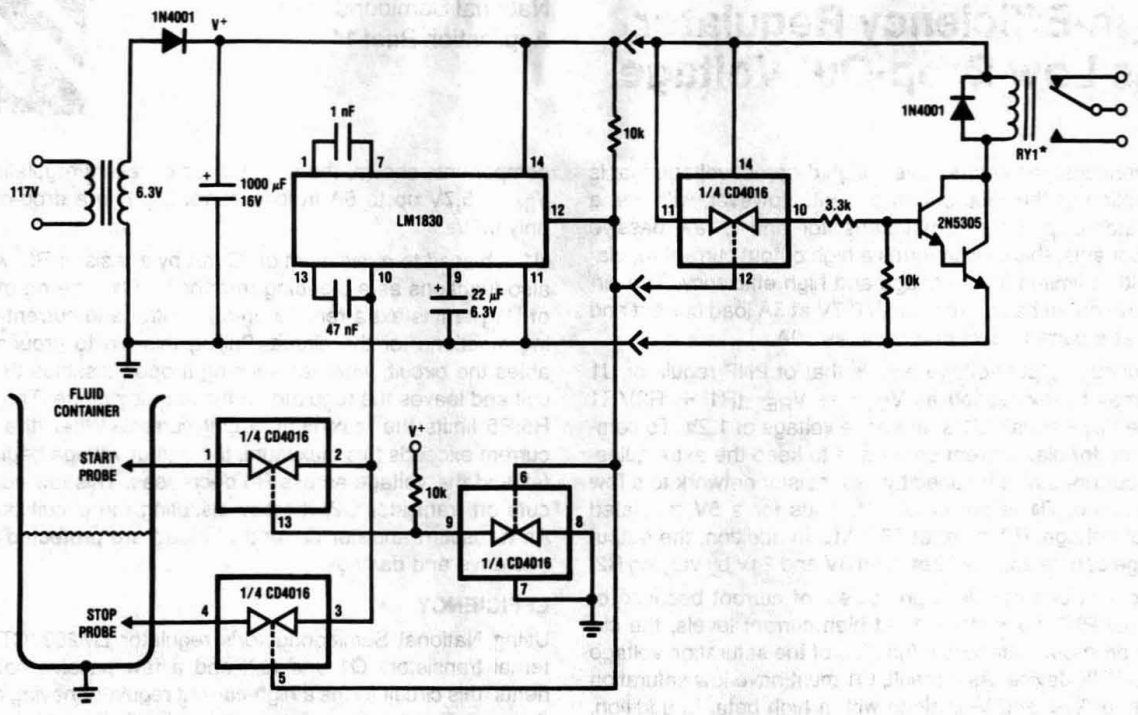


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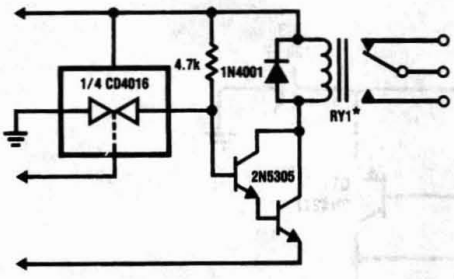
FIGURE 1(a). "Emptying" Processes are Controlled with this Circuit



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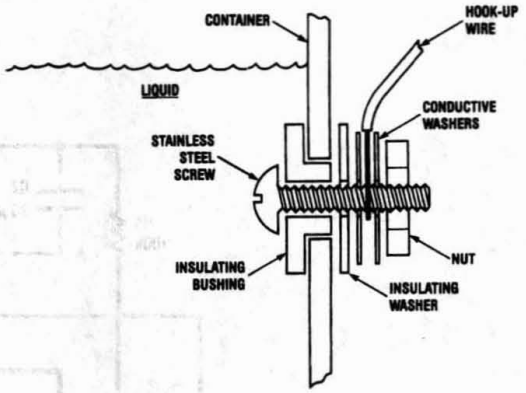
*RY1 = Magnecraft Part #W388CQX-5

FIGURE 1(b). Filling Processes are Implemented with this Output Circuit and Relabeled Probes



TL/H/5071–3

A sealing compound applied externally protects hook-up wire and prevents leaks.

FIGURE 2. Typical Probe Installation

AB-11

High-Efficiency Regulator has Low Drop-Out Voltage

National Semiconductor
Application Brief 11

Conventional regulators have a high drop-out voltage that is a function of the total output current. However, with just a regulator chip, an external transistor and a few passive components, this design forms a high output current regulator with a limited input voltage and high efficiency. The circuit presented has a drop-out of 0.7V at 5A load current and 1.3V at a current level of as high as 10A.

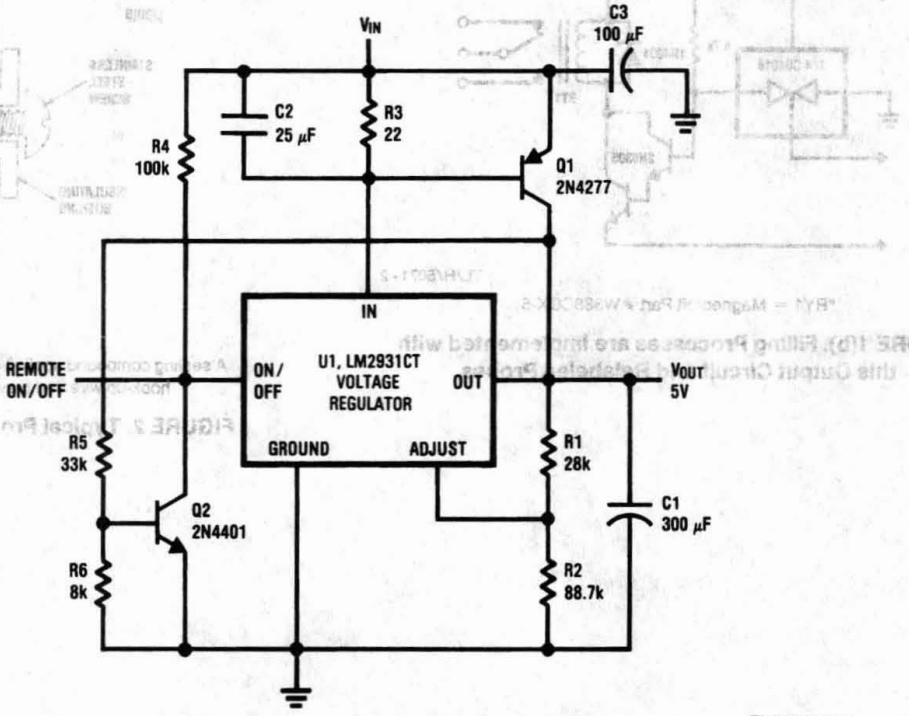
The circuit output voltage equals that of PNP regulator U1 and may be expressed as $V_{OUT} = V_{REF}$ (R1 + R2)/R1 where V_{REF} equals U1's reference voltage of 1.2V. To compensate for bias-current errors and to keep the extra quiescent current that is induced by this resistor network to a few μA, resistor R1 is set at 28 kΩ. Thus for a 5V regulated output voltage, R2 is set at 88.7 kΩ. In addition, the output voltage can be adjusted between 3V and 24V by varying R2.

The circuit can handle a great deal of current because of external PNP transistor Q1. At high current levels, the circuit's drop-out voltage is a function of the saturation voltage of the PNP device. As a result, Q1 must have low saturation levels for V_{CE} and V_{BE} along with a high beta. In addition, the maximum output current is equal to the maximum output sink of regulator U1 multiplied by the maximum beta of Q1. A germanium transistor, such as a 2N4277 for the external pass element, satisfies the above requirements. For the components shown, the circuit gives excellent regulation at V_{IN} = 5.7V up to 5A in load current, giving a drop-out of only 0.7V.

U1 is biased to a minimum of 30 mA by a resistor R3, which also functions as a bleeding resistor for Q1. The on-off pin of U1 permits extra remote on-off control and current-limiting functions for the circuit. Pulling this pin to ground enables the circuit, whereas keeping it open disables the circuit and leaves the regulator in the standby mode. The ratio R5:R6 limits the maximum output current. When the load current exceeds this maximum, the output voltage begins to fall and the voltage across R6 decreases. This low voltage cuts off transistor Q2, thereby disabling the circuit output. As a result, transistor Q1 and the load are protected from overdrive and damage.

EFFICIENCY

Using National Semiconductor's regulator LM2931CT, external transistors Q1 and Q2, and a few passive components, this circuit forms a high-current regulator having a low drop-out. For the components shown in the figure, the regulator has a drop-out of 0.7V at 5A load current and 1.3V at a level as high as 10A. The on-off pin of regulator U1 provides remote control, while transistor Q2 limits the maximum output current.



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Wide Adjustable Range PNP Voltage Regulator

National Semiconductor
Application Brief 12

What happens when the need arises for a regulator voltage that isn't matched by your stock of fixed voltage I/C regulators? For the standard NPN pass transistor regulators (LM340 for example) the answer may be as simple as adding a resistor (R1) in the ground pin *(Figure 1).* The new output voltage (V_O) will then be:

$$V_O = V_{REG} + I_Q \times R1 \quad (1)$$

where: V_{REG} is the original regulator output voltage,

I_Q is the regulator's quiescent current.

But if the need is also for a low drop across the regulator, then a PNP pass regulator is required. Simply adding a resistor in the ground pin doesn't work, since the regulator internal current varies too much because of increased base drive to compensate for lower PNP beta. However, if a zener is used instead of a resistor, the higher voltages can be accommodated *(Figure 2).* The new output voltage (V_O) is:

$$V_O = V_{REG} + V_Z \quad (2)$$

where V_Z is the zener voltage.

As V_{REG} is constant, the output voltage regulation will depend largely on the zener voltage (V_Z) and its dynamic impedance.

The zener voltage will vary slightly with the current flowing through. Let's take the popular LM2931Z PNP regulator from National Semiconductor as an example of variation of the quiescent current. When the regulator load changes from 50 mA to 150 mA, the zener current will increase by 12.5 mA. The zener voltage variation due to this current change will only be a few hundred mV. That is, the output voltage will vary slightly, but not as much (as high as a few volts) as with a resistor to ground. Thus, a much better regulated output voltage is maintained.

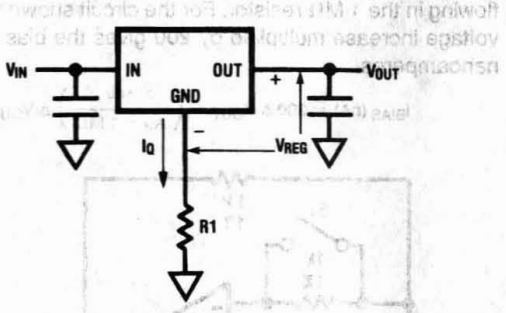

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FIGURE 1. NPN Regulator

One advantage inherent to this circuit is the ability to achieve higher output voltages than the normal regulator rating. The maximum regulator output is limited by the breakdown of its internal circuitry. However, carefully selecting the zener to keep the input and ground pin differential voltage well below the breakdown, the input is allowed to exceed its maximum rating. For example, a 5V 3-terminal LM2931Z PNP regulator (maximum operating input voltage = 26V) can become a 56V regulator with a 51V zener. And the input voltage can be as low as 56.6V with a load current of 150 mA or less. Most of the PNP regulator's features are still maintained. The short circuit protection may or may not be there, depending on the output voltage and the safe operating area of the output pass PNP transistor.

Capacitors C1 and C2 should have the same values as those specified for normal operation. However, their maximum operating voltage ratings should exceed the input voltage. Capacitor C3 should be located as close as possible to the ground pin to get good decoupling and ensure stable operation. The value of C3 will depend on zener impedance and noise characteristics. The capacitor types must also be rated over the desired operating temperature range.

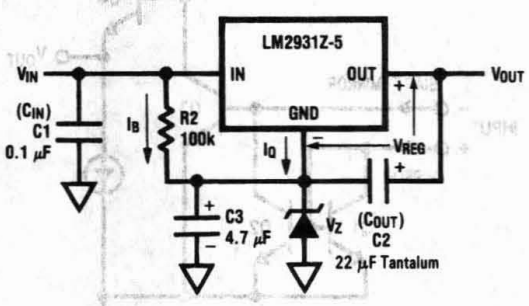

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FIGURE 2. PNP Regulator

Bench Testing LM3900 and LM359 Input Parameters

National Semiconductor
Application Brief 24

Two input parameters are extremely important in designing circuits with Norton op amps. These are the input bias current, I_{BIAS}, and the mirror gain constant, A_I. The mirror gain is especially important when a Norton amplifier is used as a voltage follower.

A simplified schematic of the LM3900 is shown in *Figure 1*. The op amp is basically a common emitter amplifier (Q3), with an emitter follower output stage. Added to the base of Q3 is a current mirror (Q1 and Q2). If a fixed current is injected into the non-inverting input and the output is fed back to the inverting input, the output will rise until the current in Q2 matches that flowing in Q1. The currents in the input terminals will not be equal since some current (I_{BIAS}) flows into the base of Q3. This is especially noticeable when the mirror current is very small—for instance in the 1 to 10 μA range. Input currents may also be unequal due to mismatch in the mirror transistors, Q1 and Q2. The degree of matching is called mirror gain, A_I, and is ideally equal to "1".

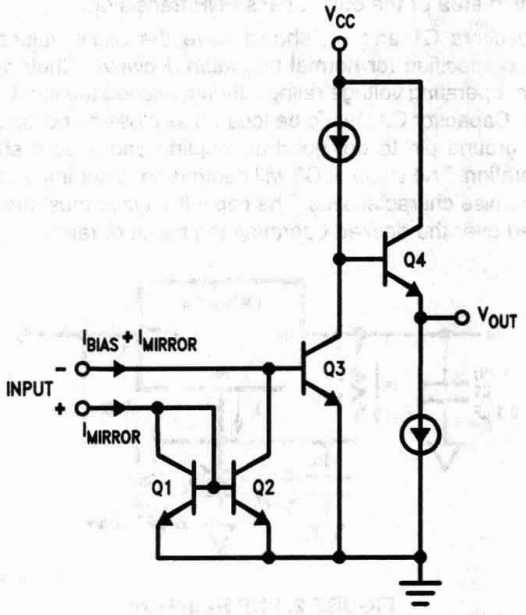

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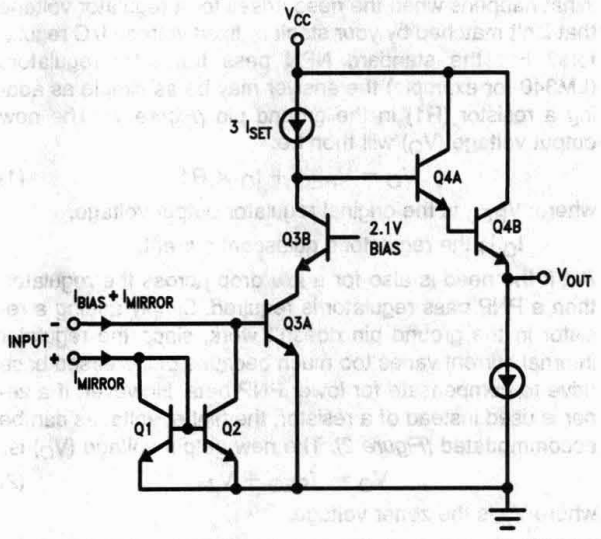
FIGURE 1. A simplified schematic of the LM3900

The LM359 (*Figure 2*) differs from the LM3900 in that "Q3" is a cascode stage, and "Q4" is a darlington follower. Also, the internal biasing is variable; set current (I_{SET}) is determined by an external resistor. Gain-bandwidth product, slew rate, input noise, output drive current, input bias current and, of course, supply current all vary with set current.

Any modern text detailing the operation of an op amp will tell you how to bench test its parameters. Norton amplifiers are, however, frequently overlooked and their important input parameters are difficult to test in the usual manner. Two measurements and a simple calculation can provide accurate characterization of I_{BIAS} and A_I.

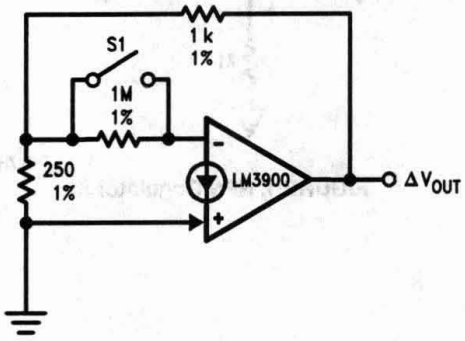


TL/H/5529–2

FIGURE 2. A simplified schematic of the LM359

The test circuit for measurement of I_{BIAS} in the LM3900 is shown in *Figure 3*. Two voltage measurements are made at the output of the LM3900, one with S1 closed and one with S1 opened. The output voltage increase is equal to the voltage appearing across the 1 MΩ resistor, multiplied by the closed loop gain (A_V) of 5. It is the result of Q3 bias current flowing in the 1 MΩ resistor. For the circuit shown the output voltage increase multiplied by 200 gives the bias current in nanoamperes.

$$I_{BIAS}\,(nA) = 200\,\Delta\,V_{OUT} = \left(\frac{10^9}{A_V \times 1\,M\Omega}\right)\Delta\,V_{OUT}$$



TL/H/5529–3

FIGURE 3. I_{BIAS} can be evaluated by measuring the change in output voltage when S1 is opened and closed.

LM3900 mirror gain is measured using the circuit of *Figure 4*. "R" is selected to provide the desired mirror current. The voltage across each "R" is measured, and their ratio is equal to the mirror gain, A_I. As previously mentioned, the

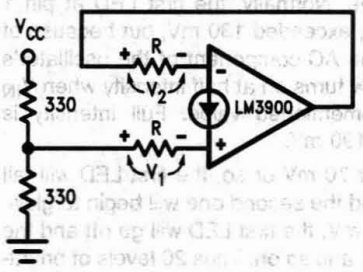
mirror gain is affected by the presence of I_{BIAS}. Where I_{BIAS} is a significant part of the mirror current, the formula (true for the LM3900 and the LM359) for A_I becomes

$$A_I = \frac{(V_2) - RI_{BIAS}}{V_1}$$

Many of the LM359's data sheet parameters, including I_{BIAS}, are measured with $I_{SET} = 0.5$ mA. Three times this current flows in the collector of Q3A, making its bias current about 15 μA. The LM3900 has a corresponding Q3 collector current of only 3 μA, and its $I_{BIAS} = 30$ nA. However, the current, adding an unpredictable error term to the DC biasing equations. This circumstance can be avoided by sizing the mirror current at least ⅓ I_{SET}.

Figures 5 and *6* show how to measure and calculate I_{BIAS} and A_I for the LM359. R_{SET} is selected to provide the appropriate set current and C_{COMP} is added for stability. I_{BIAS} and A_I are measured with the same set currents used in the data sheet.

All of the test circuits assume $V_{CC} = 12$V. Accuracy is as good as the resistors and meter used. Matching is important for the two "R's" used in *Figures 4* and *6*. 1% tolerance is recommended for each resistor (5% resistors can be sorted for accuracy) in *Figure 3*, and the 100 kΩ resistor in *Figure 5*. Most 3½ digit DVM's have sufficient accuracy for the voltage measurements; input impedance must be at least 10 MΩ to prevent circuit loading in the mirror gain tests. Detailed information concerning the use of the LM3900 and LM359 can be found in their data sheets and in AN-72.



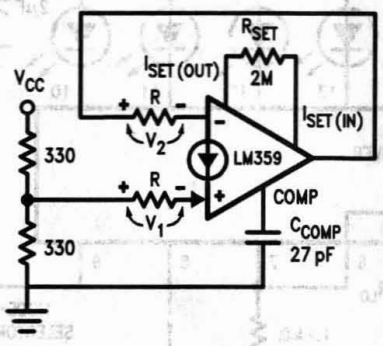
R (1%)	I_{MIRROR}
270 kΩ	20 μA
27 kΩ	200 μA

$$A_I = \frac{V_2}{V_1}$$

TL/H/5529–4

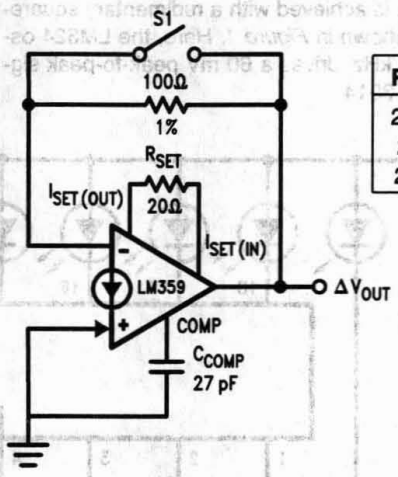
FIGURE 4. This circuit allows the measurement of the mirror gain, "A_I"

$10\,\Delta V_{OUT} = I_{BIAS}\,(\mu A)$



TL/H/5529–5

FIGURE 5. I_{BIAS} is measured with a set current of 500 μA



R (1%)	I_{MIRROR}
270 kΩ	20 μA
27 kΩ	200 μA
2.7 kΩ	2 mA

$$A_I = \frac{V^-}{V+}$$

TL/H/5529–6

FIGURE 6. Mirror gain, A_I, is measured with I_{SET} = 5 μA

LM3900 doesn't have a 400 MHz gain-bandwidth product. The mirror gain is measured with $I_{SET} = 5$ μA, making I_{BIAS} so small it has little affect on the measurement. In a practical application I_{BIAS} may be a significant part of the mirror

AB-25

'Dithering' Display Expands Bar Graph's Resolution

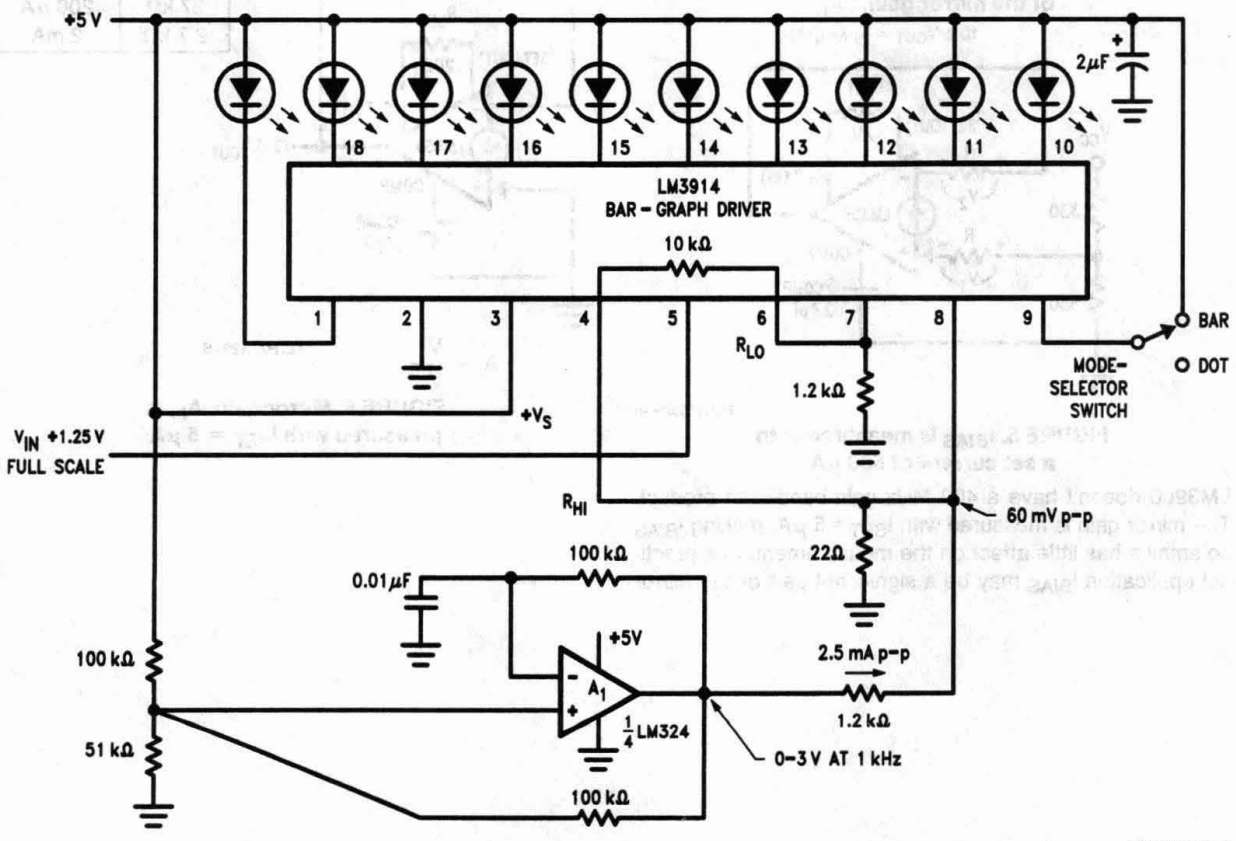
National Semiconductor
Application Brief 25
Robert A. Pease

Commercially available bar-graph chips such as National's LM3914 offer an inexpensive and generally attractive way of discerning 10 levels of signal. If 20, 30, or more steps of resolution are required, however, bar-graph displays must be stacked, and with that, the circuit's power drain, cost and complexity all rise. But the techniques used here for creating a scanning-type "dithering" or modulated display will expand the resolution to 20 levels with only one 3914 or, alternately, make it possible to implement fine-tuning control so that performance approaching infinite resolution can be achieved.

The light-emitting-diode display arrangement for simply distinguishing 20 levels is achieved with a rudimentary square-wave oscillator, as shown in *Figure 1.* Here, the LM324 oscillator, running at 1 kHz, drives a 60 mV peak-to-peak signal into pin 8 of the 3914.

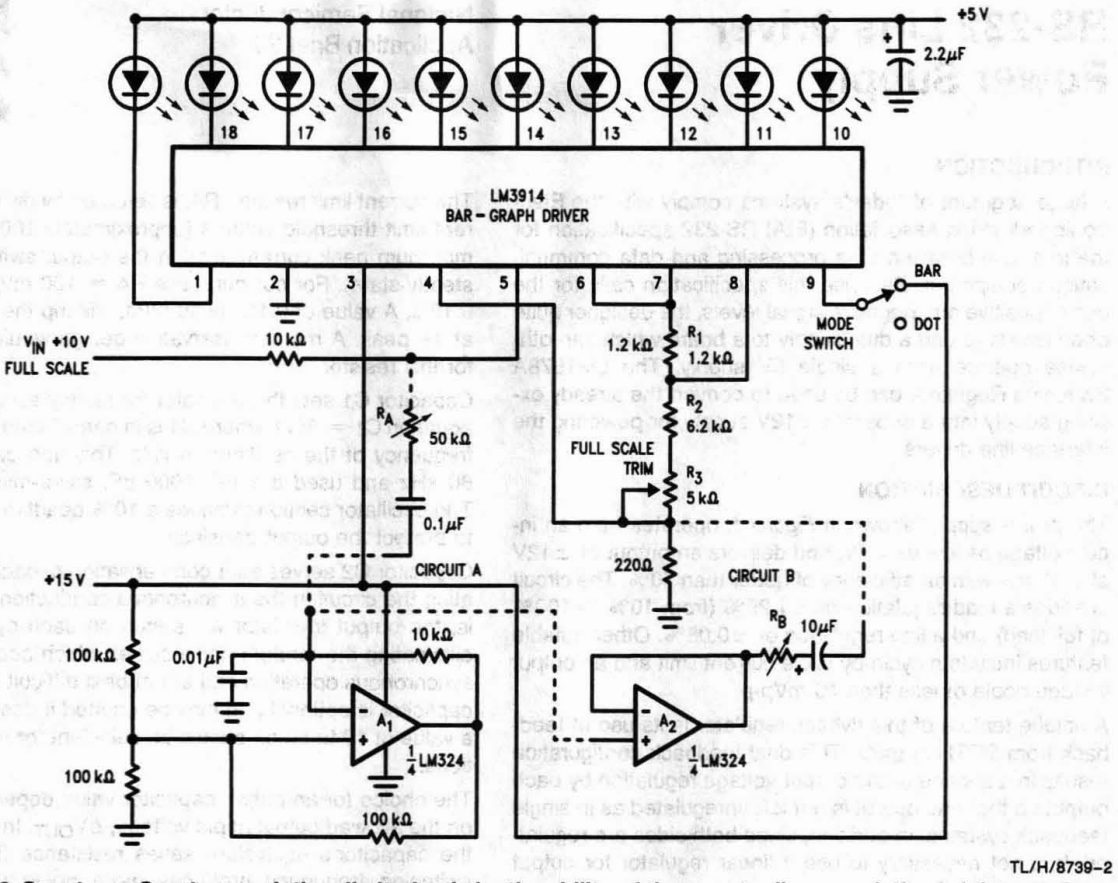
Now, the internal reference circuitry of the 3914 acts to force pin 7 to be 1.26V above pin 8, so that pins 4 and 8 are at an instantaneous potential of 4.0 mV plus a 60 mV p-p square wave, while pins 6 and 7 will be at 1.264V plus a 60 mV p-p square wave. Normally, the first LED at pin 1 would turn on when V_{IN} exceeded 130 mV, but because of the dither caused by the AC component of the oscillator's output, the first LED now turns on at half intensity when V_{IN} rises above the aforementioned value. Full intensity is achieved when V_{IN} = 190 mV.

When V_{IN} rises another 70 mV or so, the first LED will fall off to half brightness and the second one will begin to glow. When V_{IN} reaches 320 mV, the first LED will go off and the second will turn on fully, and so on. Thus 20 levels of brightness are easily obtained.



TL/H/8739-1

FIGURE 1. Half tones. Input-signal biasing on LM3914 bar-graph chip is set by the instantaneous output of a low-amplitude square-wave oscillator so that bar-graph resolution can be doubled. Each of 10 LEDs now has a fully-on and a partially-on mode, making 20 states discernible.



TL/H/8739–2

FIGURE 2. Spectrum. Greater resolution, limited only by the ability of the user to discern relative brightness, is achieved by employing a triangular-wave oscillator and more sensitive control circuitry to set the voltage levels and thus light levels of corresponding LEDs. Two RC networks, circuits A and B, provide required oscillator coupling and attenuation. B replaces A if oscillator cannot suffer heavy loading.

Similarly, greater resolution can be achieved by employing a triangular-wave oscillator and two simple RC networks as seen in *Figure 2.* Here, by means of circuit A, this voltage is capacitively coupled, attenuated, and superimposed on the input voltage at pin 5 of the LM3914. With appropriate setting of the 50 kΩ potentiometer, each incremental change in V_{IN} can be detected because the glow from each LED can be made to spread gradually from one device to the next.

Of course, if the signal-source impedance is not low or linear, the AC signals coupled into the input circuit can cause false readings at the output. In this case, the circuit in block B should be used to buffer the output of the triangular-wave oscillator.

The display is most effective in the dot mode, where supply voltages can be brought up to 15V. If the circuit's bar mode is used, the potentials applied to the LEDs should be made no greater than 5V to avoid overheating.

To trim the circuit, set the LM3914's output to full scale with R_3. R_A or R_B should then be trimmed so that when one LED is lit, any small measured change of V_{IN} will cause one of the adjacent LEDs in the chain to turn on.

AB-30

RS-232 Line Driver Power Supply

National Semiconductor
Application Brief 30

INTRODUCTION

A large segment of today's systems comply with the Electronic Industries Association (EIA) RS-232 specification for the interface between data processing and data communications equipment. Because this specification calls for the use of positive and negative signal levels, the designer quite often needs to add a dual supply to a board which can otherwise operate from a single 5V supply. The LM1578A Switching Regulator can be used to convert the already existing supply into a separate ±12V supply for powering the interface line drivers.

CIRCUIT DESCRIPTION

The power supply, shown in *Figure 1*, operates from an input voltage as low as 4.2V, and delivers an output of ±12V at ±40 mA with an efficiency of better than 70%. The circuit provides a load regulation of ±1.25% (from 10% to 100% of full load) and a line regulation of ±0.08%. Other notable features include a cycle-by-cycle current limit and an output voltage ripple of less than 40 mVp-p.

A unique feature of this flyback regulator is its use of feedback from BOTH outputs. This dual feedback configuration results in a sharing of the output voltage regulation by each output so that one output is not left unregulated as in single feedback systems. In addition, since both sides are regulated, it is not necessary to use a linear regulator for output regulation.

COMPONENT SELECTION

The following design procedure is provided for the user who wishes to tailor the power supply circuit to fit their own specific converter application.

The feedback resistors, R2 and R3, may be selected as follows by assuming a value of 10 kΩ for R1;

$R2 = (V_{OUT} - 1V)/45.8\ \mu A = 240\ k\Omega$

$R3 = (|V_{OUT}| + 1V)/54.2\ \mu A = 240\ k\Omega$

Actually, the currents used to program the values for the feedback resistors may vary from 40 μA to 60μA, as long as their sum is equal to the 100 μA necessary to establish the 1V threshold across R1 (10 kΩ). Ideally, these currents should be equal (50 μA each) for optimal control. However, as was done here, they may be mismatched in order to use standard resistor values. This results in a slight mismatch of regulation between the two outputs.

The current limit resistor, R4, is selected by dividing the current limit threshold voltage (approximately 100 mV) by the maximum peak current level in the output switch (750 mA steady-state). For our purposes R4 = 100 mV/750 mA = 0.13Ω. A value of 0.1Ω, used here, will trip the current limit at 1A peak. A more conservative design would use 0.15Ω for this resistor.

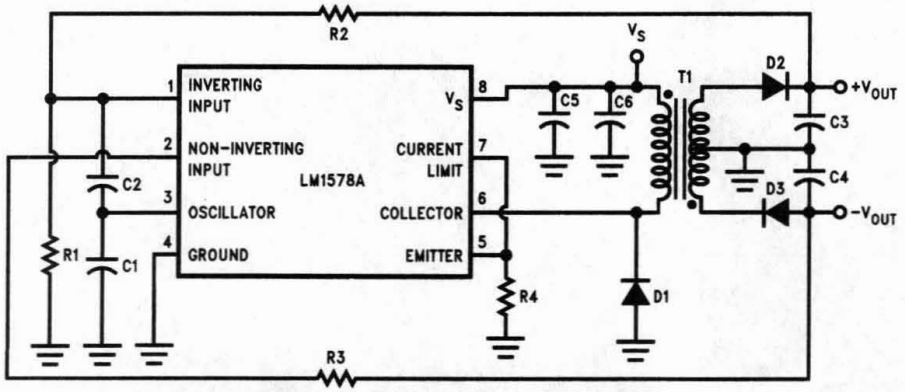
Capacitor C1 sets the oscillator frequency according to the equation C1 = 80/f, where C1 is in nano-Farads and f is the frequency of the oscillator in kHz. This application runs at 80 kHz and used a 1 nF (1000 pF) silver-mica capacitor. The oscillator section provides a 10% deadtime each cycle to protect the output transistor.

Capacitor C2 serves as a compensation capacitor for operating the circuit in the synchronous conduction mode. That is, the output transistor will switch on each cycle, thereby eliminating the random noise spikes which occur with non-synchronous operation and are at best difficult to filter. This capacitor is optional and may be omitted if desired. If used, a value of 10 to 50 pF should be sufficient for most applications.

The choice for an output capacitor value depends primarily on the allowed output ripple voltage, ΔV_{OUT}. In most cases, the capacitor's equivalent series resistance (ESR) at the switching frequency produces more ripple voltage than does the charging and discharging of the capacitor. The capacitor should be chosen to have an ESR ≤ ΔV_{OUT}/100 mA, where 100 mA is approximately the greatest ripple current produces by the transformer secondary. Higher-value capacitors tend to have lower ESR; 1000 μF aluminum electrolytic was used in this circuit to assure low ESR, under 0.4Ω.

The input capacitors, C5 and C6, are used to reduce the transients that may be fedback to the main supply. Capacitor C5 is a 100 μF electrolytic and is bypassed by C6, a 0.1 μF ceramic disc.

For good efficiency, the diodes must have a low forward voltage drop and be fast switching. 1N5819 Schottky diodes work well.



TL/H/8756–1

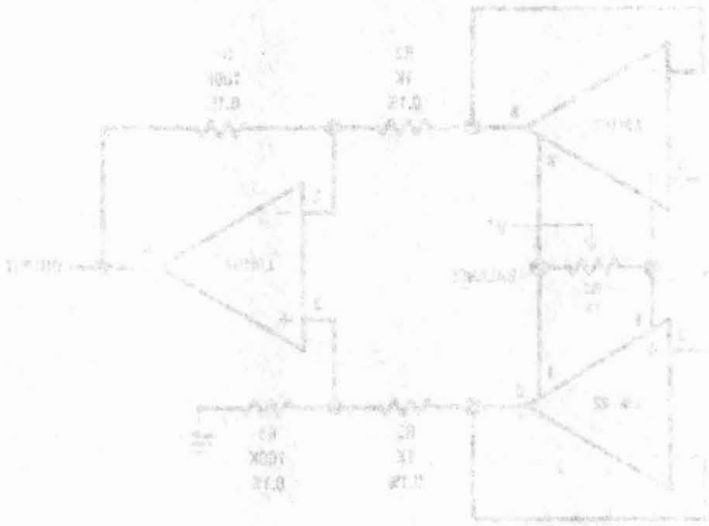
FIGURE 1. RS-232 Power Supply (See Table I, Parts List)

Transformer selection should be picked for an output transistor "on" time of 0.4/f, and a primary inductance high enough to prevent the output transistor switch from ramping higher than the transistor's rating of 750 mA. Pulse Engineering (San Diego, Calif.) and Renco Electronics, Inc. (Deer Park, N.Y.) can provide further assistance in selecting the proper transformer for a specific application need. The transformer used in the power supply was a Pulse Engineering PE-64287 with turns ratio of Np:Ns:Ns = 1:1.6:1.6 and primary inductance of 50 μH.

Table I is a parts listing for the components used in the building of the power supply circuit.

TABLE I
Parts List

R1 = 10 kΩ
R2 = 240 kΩ
R3 = 240 kΩ
R4 = 0.1Ω
C1 = 1000 pF
C2 = 18 pF
C3 = 220 μF
C4 = 220 μF
C5 = 100 μF
C6 = 0.1 μF
All diodes are 1N5819
T1 = Pulse Engineering PE-64287



Instrumentation Amplifier

National Semiconductor
Linear Brief 1

The differential input single-ended output instrumentation amplifier is one of the most versatile signal processing amplifiers available. It is used for precision amplification of differential dc or ac signals while rejecting large values of common mode noise. By using integrated circuits, a high level of performance is obtained at minimum cost.

Figure 1 shows a basic instrumentation amplifier which provides a 10 volt output for 100 mW input, while rejecting greater than ±11V of common mode noise. To obtain good input characteristics, two voltage followers buffer the input signal. The LM102 is specifically designed for voltage follower usage and has 10,000 MΩ input impedance with 3 nA input currents. This high of an input impedance provides two benefits: it allows the instrumentation amplifier to be used with high source resistances and still have low error; and it allows the source resistances to be unbalanced by over 10,000Ω with no degradation in common mode rejection. The followers drive a balanced differential amplifier, as shown in *Figure 1*, which provides gain and rejects the common mode voltage. The gain is set by the ratio of R_4 to R_2 and R_5 to R_3. With the values shown, the gain for differential signals is 100.

Figure 2 shows an instrumentation amplifier where the gain is linearly adjustable from 1 to 300 with a single resistor. An LM101A, connected as a fast inverter, is used as an attenuator in the feedback loop. By using an active attenuator, a very low impedance is always presented to the feedback resistors, and common mode rejection is unaffected by gain changes. The LM101A, used as shown, has a greater bandwidth than the LM107, and may be used in a feedback network without instability. The gain is linearly dependent on R_6 and is equal to 10^{-4} R_6.

To obtain good common mode rejection ratios, it is necessary that the ratio of R_4 to R_2 match the ratio of R_5 to R_3. For example, if the resistors in circuit shown in *Figure 1* had a total mismatch of 0.1%, the common mode rejection would be 60 dB times the closed loop gain, or 100 dB. The circuit shown in *Figure 2* would have constant common mode rejection of 60 dB, independent of gain. In either circuit, it is possible to trim any one of the resistors to obtain common mode rejection ratios in excess of 100 dB.

For optimum performance, several items should be considered during construction. R_1 is used for zeroing the output. It should be a high resolution, mechanically stable potentiometer to avoid a zero shift from occurring with mechanical disturbances. Since there are several ICs operating in close proximity, the power supplies should be bypassed with 0.01 μF disc capacitors to insure stability. The resistors should be of the same type to have the same temperature coefficient.

A few applications for a differential instrumentation amplifier are: differential voltage measurements, bridge outputs, strain gauge outputs, or low level voltage measurement.

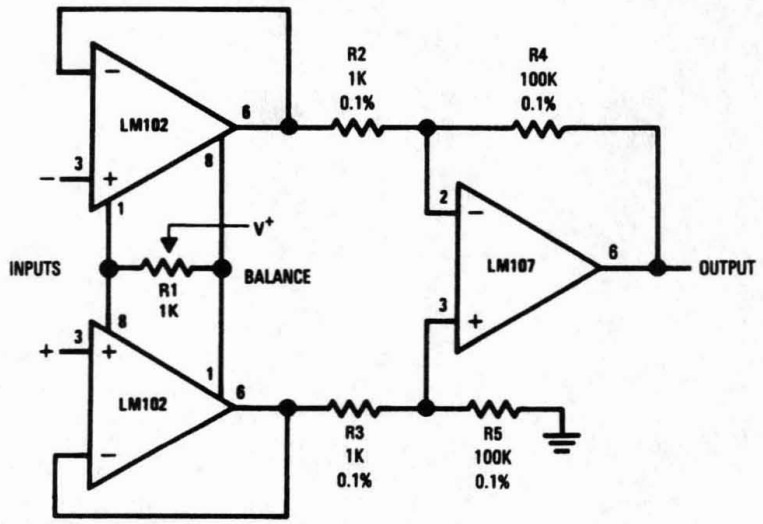
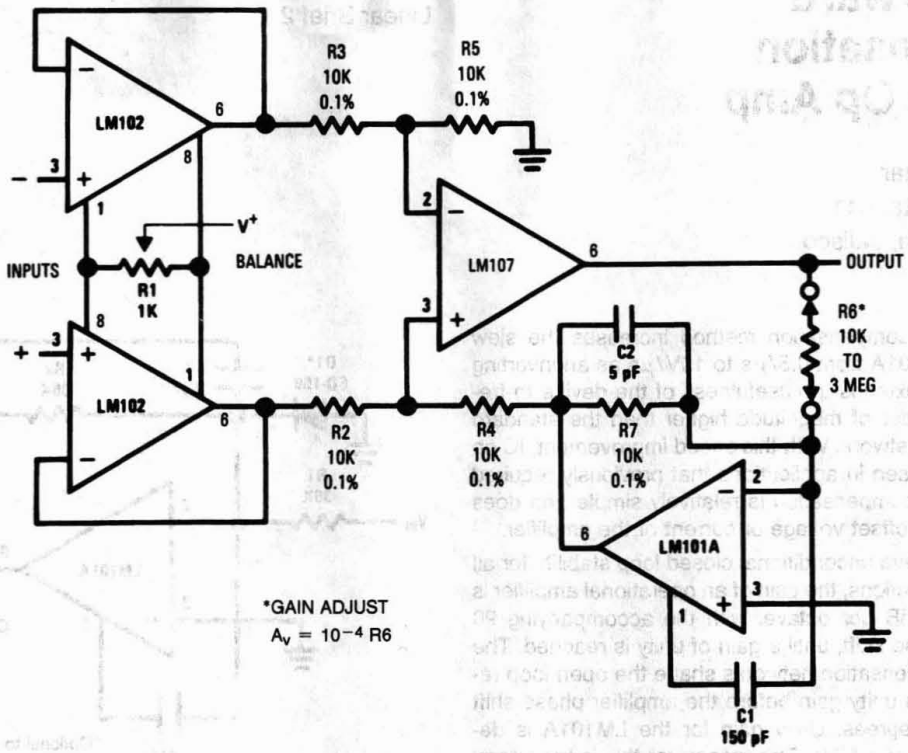


FIGURE 1. Differential-Input Instrumentation Amplifier



TL/H/8501–2

FIGURE 2. Variable Gain, Differential-Input Instrumentation Amplifier

Feedforward Compensation Speeds Op Amp

National Semiconductor
Linear Brief 2

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Apartado Postal 541
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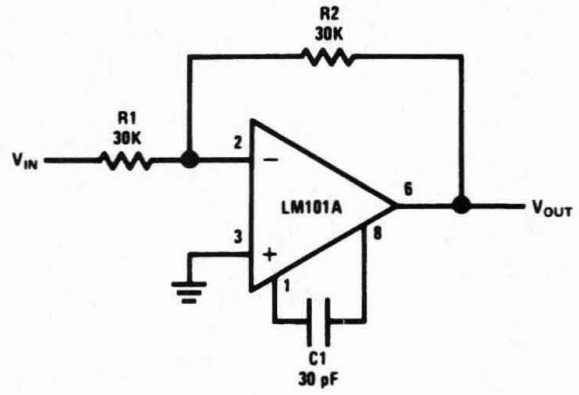
Mexico

A feedforward compensation method increases the slew rate of the LM101A from 0.5/μs to 10V/μs as an inverting amplifier. This extends the usefulness of the device to frequencies an order of magnitude higher than the standard compensation network. With this speed improvement, IC op amps may be used in applications that previously required discretes. The compensation is relatively simple and does not change the offset voltage or current of the amplifier.

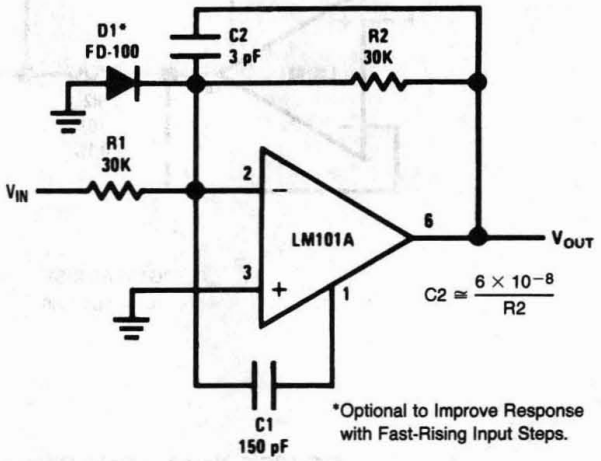
In order to achieve unconditional closed loop stability for all feedback connections, the gain of an operational amplifier is rolled off at 6 dB per octave, with the accompanying 90 degrees of phase shift, until a gain of unity is reached. The frequency compensation networks shape the open loop response to cross unity gain before the amplifier phase shift exceeds 180 degrees. Unity gain for the LM101A is designed to occur at 1 MHz. The reason for this is the lateral PNP transistors used for level shifting have poor high frequency response and exhibit excess phase shift about 1 MHz. Therefore, the stable closed loop bandwidth is limited to approximately 1 MHz.



TL/H/7327–1

Figure 1. Standard frequency compensation

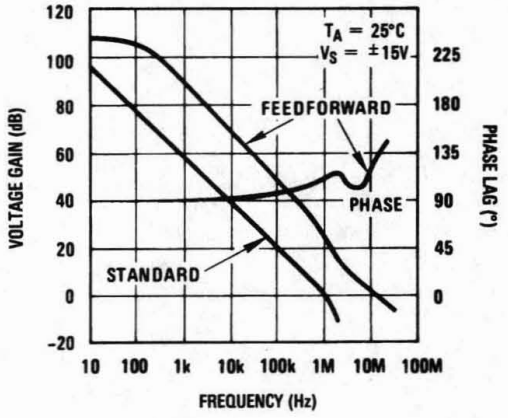
Usually, the LM101A is frequency compensated by a single 30 pF capacitor between Pins 1 and 8, as shown in *Figure 1*. This gives a slew rate of 0.5V/μs. The feedforward is achieved by connecting a 150 pF capacitor between the inverting input, Pin 2, and one of the compensation terminals, Pin 1, as shown in *Figure 2*. This eliminates the lateral PNP's from the signal path at high frequencies. Unity gain bandwidth is 10 MHz and the slew rate is 10V/μs. The diode can be added to improve slew with high speed input pulses.



TL/H/7327–2

Figure 2. Feedforward frequency compensation

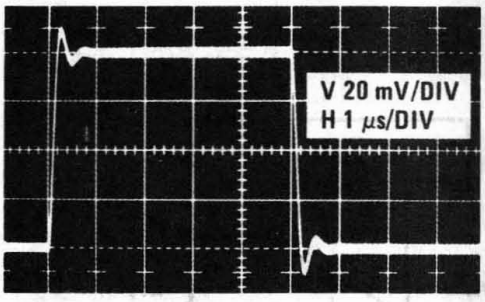
Figure 3 shows the open loop response in the high and low speed configuration. Higher open loop gain is realized with the fast compensation, as the gain rolls off at about 6 dB per octave until a gain of unity is reached at about 10 MHz.



TL/H/7327–3

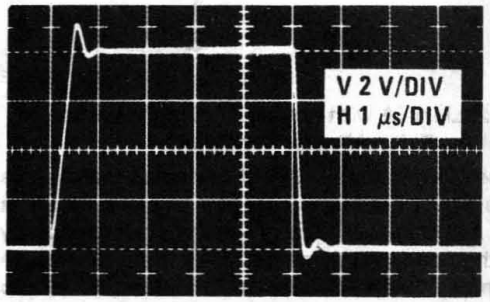
Figure 3. Open loop response for both frequency compensation networks

Figures 4 and *5* show the small signal and large signal transient response. There is a small amount of ringing; however, the amplifier is stable over a −55°C to +125°C temperature range. For comparison, large signal transient response with 30 pF frequency compensation is shown in *Figure 6*.



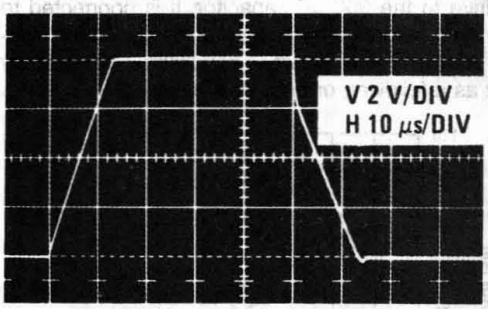
TL/H/7327–4

Figure 4. Small signal transient response with feedforward compensation



TL/H/7327–5

Figure 5. Large signal transient response with feedforward compensation

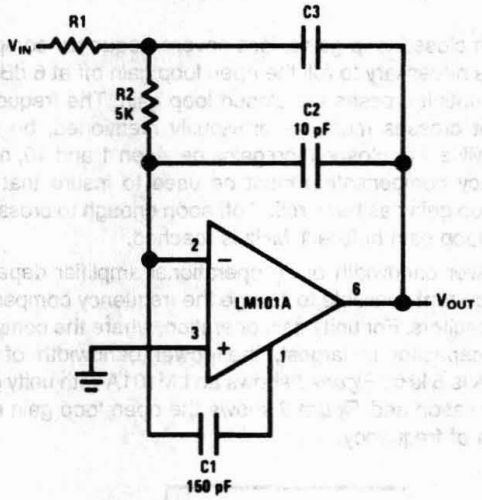


TL/H/7327–6

Figure 6. Large signal transient response with standard compensation

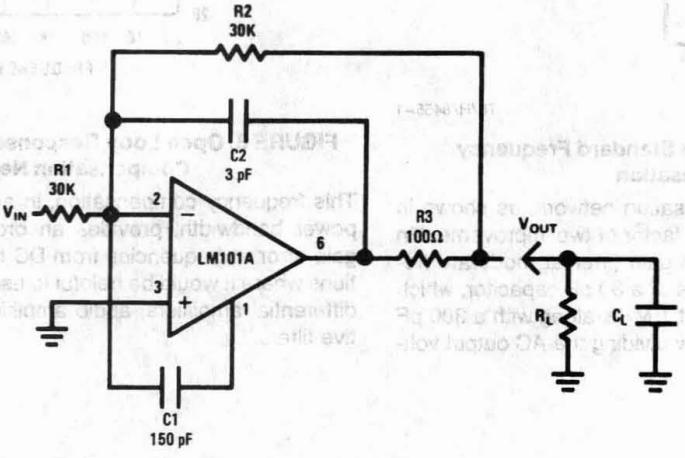
As with all high frequency, high-gain amplifiers, certain precautions should be taken to insure stable operation. The power supplies should be bypassd near the amplifier with .01 μF disc capacitors. Stray capacitance, such as large lands on printed circuit boards, should be avoided at Pins 1, 2, 5, and 8. Load capacitance in excess of 75 pF should be decoupled, as shown in *Figure 7*; however, 500 pF of load capacitance can be tolerated without decoupling at the expense of bandwidth by the addition of 3 pF between Pins 1 and 8. A small capacitor C_2 is needed as a lead across the feedback resistor to insure that the rolloff is less than 12 dB per octave at unity gain. The capacitive reactance of C_2 should equal the feedback resistance between 2 and 3 MHz. For integrator applications, the lead capacitor is isolated from the feedback capacitor by a resistor, as shown in *Figure 8*.

Feedforward compensation offers a marked improvement over standard compensation. In addition to having higher bandwidth and slew, there is vanishingly small gain error from DC to 3 kHz, and less than 1% gain error up to 100 kHz as a unity gain inverter. The power bandwidth is also extended from 6 kHz to 250 kHz. Some applications for this type of amplifier are: fast summing amplifier, pulse amplifier, D/A and A/D systems, and fast integrator.



TL/H/7327–8

Figure 8. Fast Integrator



TL/H/7327–7

Figure 7. Capacitive load isolation

Fast Compensation Extends Power Bandwidth

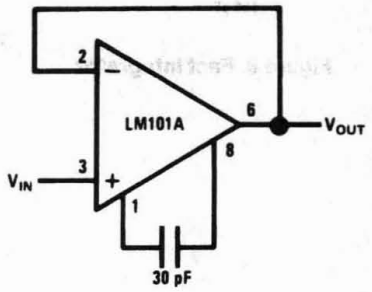
National Semiconductor
Linear Brief 4

In all IC operational amplifiers the power bandwidth depends on the frequency compensation. Normally, compensation for unity gain operation is accompanied by the lowest power bandwidth. A technique is presented which extends the power bandwidth of the LM101A for non-inverting gains of unity to ten, and also reduces the gain error at moderate frequencies.

In order to achieve unconditional stability, an operational amplifier is rolled off at 6 dB per octave, with an accompanying 90 degrees of phase shift, until a gain of unity is reached. Unity gain in most monolithic operational amplifiers is limited to 1 MHz, because the lateral PNP's used for level shifting have poor frequency response and exhibit excess phase shift at frequencies above 1 MHz. Hence, for stable operation, the closed loop bandwidth must be less than 1 MHz where the phase shift remains below 180 degrees.

For high closed loop gains, less severe frequency compensation is necessary to roll the open loop gain off at 6 dB per octave until it crosses the closed loop gain. The frequency where it crosses must, as previously mentioned, be less than 1 MHz. For closed loop gains between 1 and 10, more frequency compensation must be used to insure that the open loop gain has been rolled off soon enough to cross the closed loop gain before 1 MHz is reached.

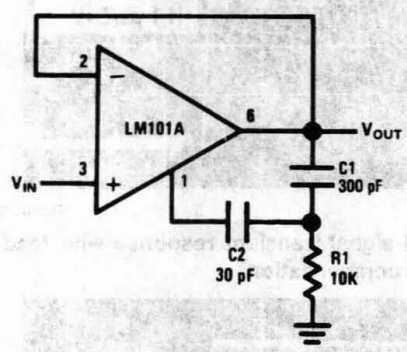
The power bandwidth of an operational amplifier depends on the current available to charge the frequency compensation capacitors. For unity gain operation, where the compensation capacitor is largest, the power bandwidth of the LM101A is 6 kHz. *Figure 1* shows an LM101A with unity gain compensation and *Figure 3* shows the open loop gain as a function of frequency.



TL/H/8455–1

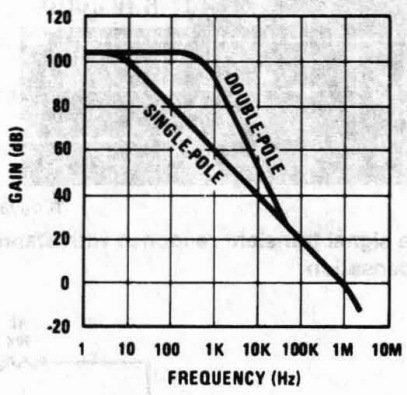
FIGURE 1. LM101A with Standard Frequency Compensation

A two-pole frequency compensation network, as shown in *Figure 2*, provides more than a factor of two improvement in power bandwidth and reduced gain error at moderate frequencies. The network consists of a 30 pF capacitor, which sets the unity gain frequency at 1 MHz, along with a 300 pF capacitor and a 10k resistor. By dividing the AC output voltage with the 10k resistor and 300 pF capacitor, there is less AC voltage across the 30 pF capacitor and less current is needed for charging. Since the voltage division is frequency sensitive, the open loop gain rolls off at 12 dB per octave until a gain of 20 is reached at 50 kHz. From 50 kHz to 1 MHz the 10k resistor is larger than the impedance of the 300 pF capacitor and the gain rolls off at 6 dB per octave. The open loop gain plot is shown in *Figure 3*. To insure sufficient drive to the 300 pF capacitor, it is connected to the output, Pin 6, rather than Pin 8. With this frequency compensation method, the power bandwidth is typically 15–20 kHz as a follower, or unity gain inverter.



TL/H/8455–2

FIGURE 2. LM101A with Frequency Compensation to Extend Power Bandwidth



TL/H/8455–3

FIGURE 3. Open Loop Response for Both Frequency Compensation Networks

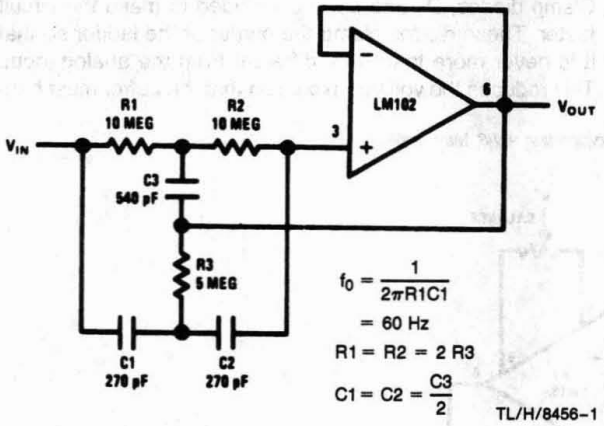
This frequency compensation, in addition to extending the power bandwidth, provides an order of magnitude lower gain error at frequencies from DC to 5 kHz. Some applications where it would be helpful to use the compensation are: differential amplifiers, audio amplifiers, oscillators, and active filters.

High Q Notch Filter

National Semiconductor
Linear Brief 5

The twin "T" network is one of the few RC filter networks capable of providing an infinitely deep notch. By combining the twin "T" with an LM102 voltage follower, the usual drawbacks of the network are overcome. The Q is raised from the usual 0.3 to something greater than 50. Further, the voltage follower acts as a buffer, providing a low output resistance; and the high input resistance of the LM102 makes it possible to use large resistance values in the "T" so that only small capacitors are required, even at low frequencies. The fast response of the follower allows the notch to be used at high frequencies. Neither the depth of the notch nor the frequency of the notch are changed when the follower is added.

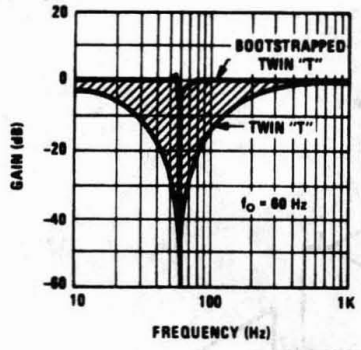
Figure 1 shows a twin "T" network connected to an LM102 to form a high Q, 60 Hz notch filter.



TL/H/8456–1

FIGURE 1. High Q Notch Filter

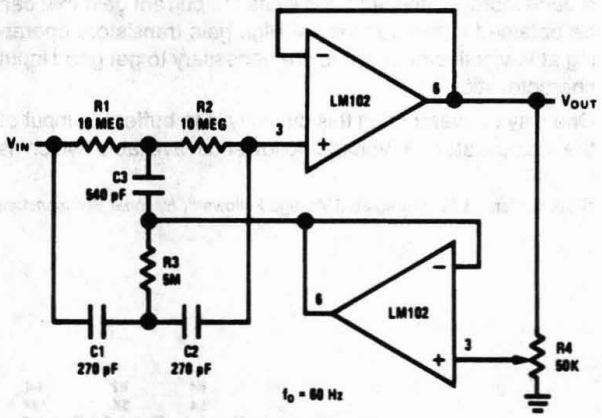
The junction of R_3 and C_3, which is normally connected to ground, is bootstrapped to the output of the follower. Because the output of the follower is a very low impedance, neither the depth nor the frequency of the notch change; however, the Q is raised in proportion to the amount of signal fed back to R_3 and C_3. *Figure 2* shows the response of a normal twin "T" and the response with the follower added.



TL/H/8456–2

FIGURE 2. Response of High and Low Q Notch Filter

In applications where the rejected signal might deviate slightly from the null of the notch network, it is advantageous to lower the Q of the network. This insures some rejection over a wider range of input frequencies. *Figure 3* shows a circuit where the Q may be varied from 0.3 to 50. A fraction of the output is fed back to R_3 and C_3 by a second voltage follower, and the notch Q is dependent on the amount of signal fed back. A second follower is necessary to drive the twin "T" from a low-resistance source so that the notch frequency and depth will not change with the potentiometer setting. Depending on the potentiometer setting, the circuit in *Figure 3* will have a response that falls in the shaded area of *Figure 2*.



TL/H/8456–3

FIGURE 3. Adjustable Q Notch Filter

An interesting change in the high Q twin "T" occurs when components are not exactly matched in ratio. For example, an increase of 1 to 10 percent in the value of C_3 will raise the Q, while degrading the depth of the notch. If the value of C_3 is raised by 10 to 20 percent, the network provides voltage gain and acts as a tuned amplifier. A voltage gain of 400 was obtained during testing. Further increases in C_3 cause the circuit to oscillate, giving a clipped sine wave output.

The circuit is easy to use and only a few items need be considered for proper operation. To minimize notch frequency shift with temperature, silver mica, or polycarbonate, capacitors should be used with precision resistors. Notch depth depends on component match, therefore, 0.1 percent resistors and 1 percent capacitors are suggested to minimize the trimming needed for a 60 dB notch. To insure stability of the LM102, the power supplies should be bypassed near the integrated circuit package with .01 μF disc capacitors.

Fast Voltage Comparators with Low Input Current

National Semiconductor
Linear Brief 6

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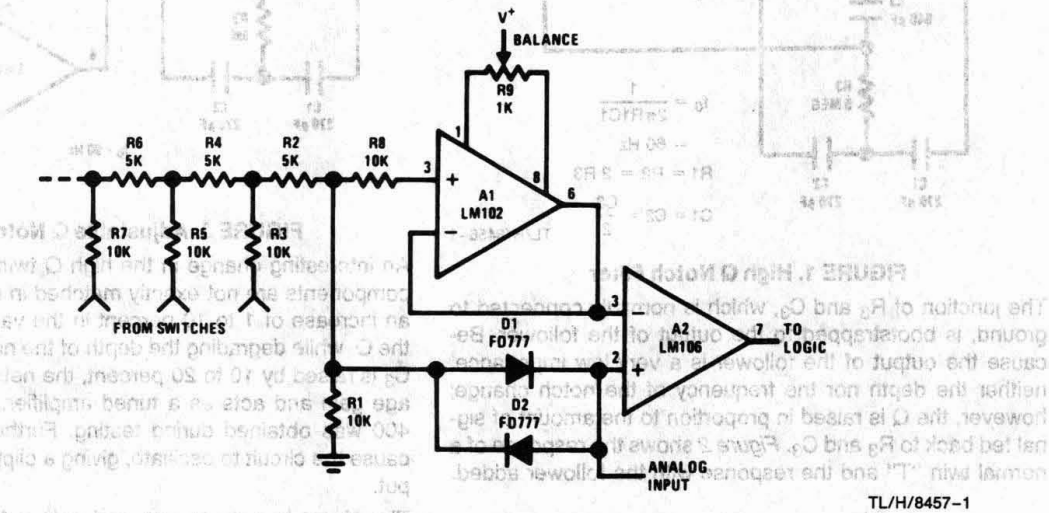
Monolithic voltage comparators are available today which are both fast and accurate. They can detect the height of a pulse with a 5 mV accuracy within 40 ns. However, these devices have relatively high input currents and low input impedances, which reduces their accuracy and speed when operating from high source resistances. This is probably a basic limitation since the input transistors of the integrated circuit must be operated at a relatively high current to get fast operation. Further, the circuit must be gold doped to reduce storage time, and this limits the current gain that can be obtained in the transistors. High gain transistors operating at low collector currents are necessary to get good input characteristics.

One way of overcoming this difficulty is to buffer the input of the comparator. A voltage follower is available which is ideally suited for this job. This device, the LM102*, is both fast and has a low input current. It can reduce the effective input current of the comparator by more than three orders of magnitude without greatly reducing speed.

A comparator circuit for an A/D converter which uses this technique is shown in *Figure 1a*. An LM102 voltage follower buffers the output of a ladder network and drives one input of the comparator. The analog signal is fed to the other input of the comparator. It should come from a low impedance source such as the output of a signal processing amplifier, or another LM102 buffer amplifier.

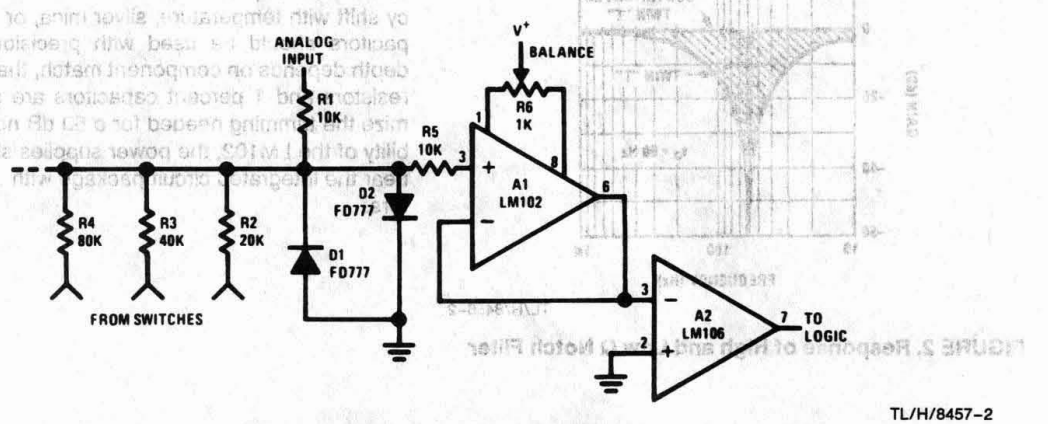
Clamp diodes, D_1 and D_2, are included to make the circuit faster. These diodes clamp the output of the ladder so that it is never more than 0.7V different from the analog input. This reduces the voltage excursion that the buffer must han-

*R. J. Widlar, "A Fast Integrated Voltage Follower", *National Semiconductor Corporation AN-8,* May, 1968.



TL/H/8457–1

a. using a ladder network



TL/H/8457–2

b. using a binary-weighted network

Figure 1. Comparator circuits for fast A/D converters

dle on the most significant bit and keeps it from slewing. If fast, low capacitance diodes are used, the signal to the comparator will stabilize approximately 200 ns after the most significant bit is switched in. This is about the same as the stabilization time of the ladder network alone, as its speed is limited by stray capacitances. The diodes also limit the voltage swing across the inputs of the comparator, increasing its operating speed and insuring that the device is not damaged by excessive differential input voltage.

The buffer reduces the loading on the ladder from 45 μA to 20 nA, maximum, over a $-55°C$ to $+125°C$ temperature range. Hence, in most applications the input current of the buffer is totally insignificant. This low current will often permit the use of larger resistances in the ladder which simplifies design of the switches driving it.

It is possible to balance out the offset of the LM102 with an external 1 kΩ potentiometer, R_9. The adjustment range of this balance control is large enough so that it can be used to null out the offset of both the buffer and the comparator. A 10 kΩ resistor should be installed in series with the input to the LM102, as shown. This is required to make the short circuit protection of the device effective and to insure that it will not oscillate. This resistor should be located close to the integrated circuit.

A similar technique can be used with A/D converters employing a binary-weighted resistor network. This is shown in *Figure 1b*. The analog input is fed into a scaling resistor, R_1. This resistor is selected so that the input voltage to the LM102 is zero when the output of the D/A network corresponds to the analog input voltage. Hence, if the D/A output is too low, the output of the LM106 will be a logical zero; and the output will change to a logical one as the D/A output exceeds the analog signal.

The analog signal must be obtained from a source impedance which is low by comparison to R_1. This can be either another LM102 buffer or the output of the signal-processing amplifier. Clamp diodes, D_1 and D_2, restrict the signal swing and speed up the circuit. They also limit the input signal seen by the LM106 to protect if from overloads. Operating speed can be increased even further by using silicon backward diodes (a degenerate tunnel diode) in place of the diodes shown, as they will clamp the signal swing to about 50 mV. The offset voltage of both the LM102 and the LM106 can be balanced out, if necessary, with R_6.

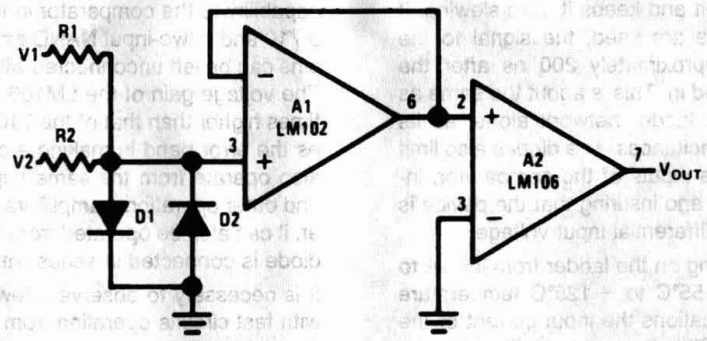
The binary weighted network can be driven with single pole, single-throw switches. This will result in a change in the output resistance of the network when it switches, but circuit performance will not be affected because the input current of the LM102 is negligible. Hence, using the LM102 greatly simplifies switch design.

Although it is possible to use a 710 as the voltage comparator in these circuits, the LM106 offers several advantages. First, it can drive a fan out of 10 with standard, integrated DTL or TTL. It also has two strobe terminals available which disable the comparator and give a high output when either of the terminals is held at a logical zero. This adds logic capability to the comparator in that it makes it equivalent to a 710 and a two-input NAND gate. If not needed, the strobe pins can be left unconnected without affecting performance. The voltage gain of the LM106 is about 45,000 which is 30 times higher than that of the 710. The increased gain reduces the error band in making a comparison. The LM106 will also operate from the same supply voltage as the LM102, and other operational amplifiers, for $\pm 12V$ supplies. However, it can also be operated from $\pm 15V$ supplies if a 3V zener diode is connected in series with the positive supply lead.

It is necessary to observe a few precautions when working with fast circuits operating from relatively high impedances. A good ground is necessary, and a ground plane is advisable. All the individual points in the circuit which are to be grounded, including bypass capacitors, should be returned separately to the same point on the ground so that voltages will not be developed across common lead inductance. The power supply leads of the integrated circuits should also be bypassed with low inductance 0.01 μF capacitors. These capacitors, preferably disc ceramic, should be installed with short leads and located close to the devices. Lastly, the output of the comparator should be shielded from the circuitry on the input of the buffer, as stray coupling can also cause oscillation.

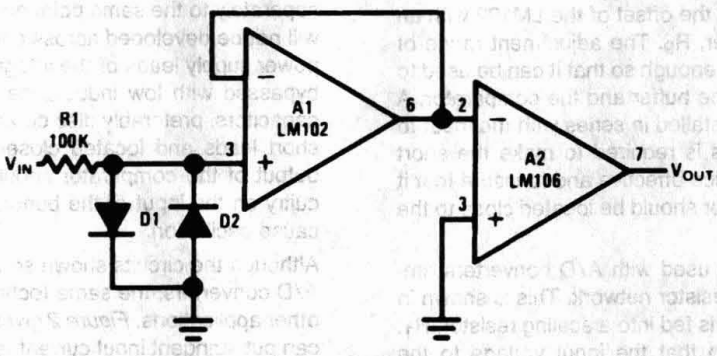
Although the circuits shown so far were designed for use in A/D converters, the same techniques apply to a number of other applications. *Figure 2* gives examples of circuits which can put stringent input current requirements on the comparator. The first is a comparator for signals of opposite polarity. Resistors (R_1 and R_2) are required to isolate the two signal sources. Frequently, these resistors must be relatively large so that the signal sources are not loaded. Hence, the input current of the comparator must be reduced to prevent inaccuracies. Another example is the zero-crossing detector in *Figure 2b*. When the input signal can exceed the common mode range of the comparator ($\pm 5V$ for the LM106), clamp diodes must be used. It is then necessary to isolate the comparator from the input with a relatively large resistance to prevent loading. Again, bias currents should be reduced. A third example, in *Figure 2c*, is a comparator with an ac coupled input. An LM106 will draw an input current which is twice the specified bias current when the signal is above the comparison threshold. Yet, it draws no current when the signal is below the threshold. This asymmetrical current drain will charge any coupling capacitor on the input and produce an error. This problem can be eliminated by using a buffer, as the input current will be both low and constant.

The foregoing has shown how two integrated circuits can be combined to provide state-of-the-art performance in both speed and input current. Equivalent results will probably not be achievable in a single circuit for some time, as the technologies required are not particularly compatible. Further, considering the low cost of monolithic circuits, approaches like this are certainly economical.



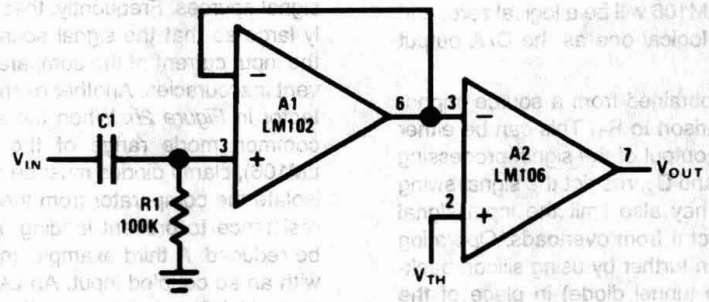
TL/H/8457–3

a. comparator for signals of opposite polarity



TL/H/8457–4

b. zero crossing detector



TL/H/8457–5

c. comparator for AC coupled signals

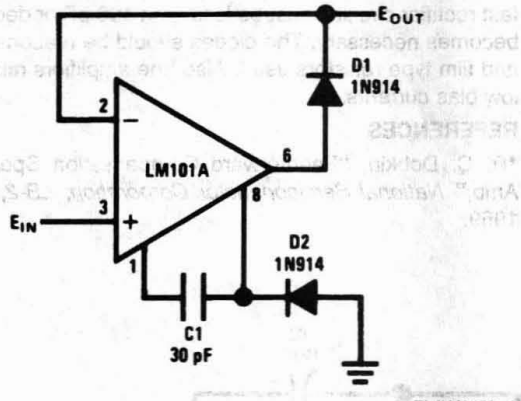
Figure 2. Applications requiring low input current comparators

Precision AC/DC Converters

National Semiconductor
Linear Brief 8

Although semiconductor diodes available today are close to "ideal" devices, they have severe limitations in low level applications. Silicon diodes have a 0.6V threshold which must be overcome before appreciable conduction occurs. By placing the diode in the feedback loop of an operational amplifier, the threshold voltage is divided by the open loop gain of the amplifier. With the threshold virtually eliminated, it is possible to rectify millivolt signals.

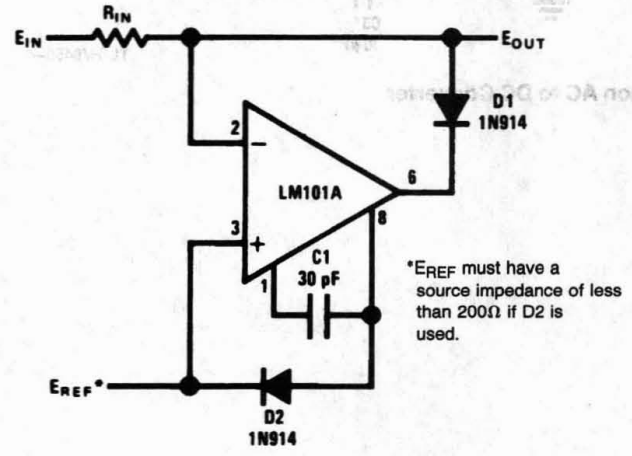
Figure 1 shows the simplest configuration for eliminating diode threshold potential. If the voltage at the non-inverting input of the amplifier is positive, the output of the LM101A



TL/H/8459–1

FIGURE 1. Precision Diode

swings positive. When the amplifier output swings 0.6V positive, D_1 becomes forward biased; and negative feedback through D_1 forces the inverting input to follow the non-inverting input. Therefore, the circuit acts as a voltage follower for positive signals. When the input swings negative, the output swings negative and D_1 is cut off. With D_1 cut off no current flows in the load except the 30 nA bias current of the LM101A. The conduction threshold is very small since less than 100 μV change at the input will cause the output of the LM101A to swing from negative to positive.



TL/H/8459–2

FIGURE 2. Precision Clamp

A useful variation of this circuit is a precision clamp, as is shown in *Figure 2*. In this circuit the output is precisely clamped from going more positive than the reference voltage. When E_{IN} is more positive than E_{REF}, the LM101A functions as a summing amplifier with the feedback loop closed through D_1. Neglecting offsets, negative feedback keeps the summing node, and therefore the output, within 100 μV of the voltage at the non-inverting input. When E_{IN} is about 100 μV more negative than E_{REF}, the output swings positive, reverse biasing D_1. Since D_1 now prevents negative feedback from controlling the voltage at the inverting input, no clamping action is obtained. On both of the circuits in *Figures 1* and *2* an output clamp diode is added at pin 8 to help speed response. The clamp prevents the operational amplifier from saturating when D_1 is reverse biased.

When D_1 is reverse biased in either circuit, a large differential voltage may appear between the inputs of the LM101A. This is necessary for proper operation and does no damage since the LM101A is designed to withstand large input voltages. These circuits will not work with amplifiers protected with back to back diodes across the inputs. Diode protection conducts when the differential input voltage exceeds 0.6V and would connect the input and output together. Also, unprotected devices such as the LM709, are damaged by large differential input signals.

The circuits in *Figures 1* and *2* are relatively slow. Since there is 100% feedback for positive input signals, it is necessary to use unity gain frequency compensation. Also, when D_1 is reverse biased, the feedback loop around the amplifier is opened and the input stage saturates. Both of these conditions cause errors to appear when the input frequency exceeds 1.5 kHz. A high performance precision half wave rectifier is shown in *Figure 3*. This circuit will provide rectification with 1% accuracy at frequencies from dc to 100 kHz. Further, it is easy to extend the operation to full wave rectification for precision AC/DC converters.

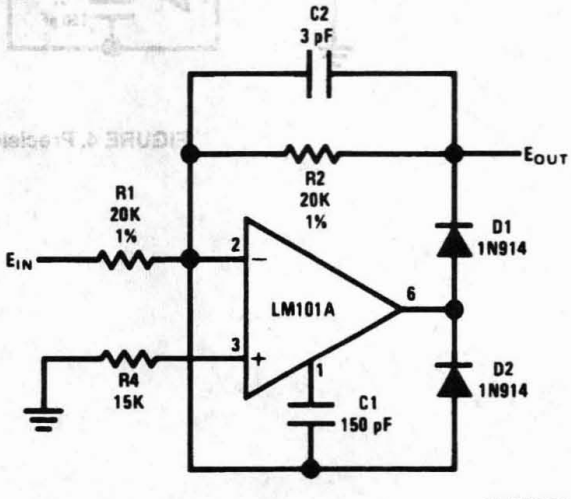


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FIGURE 3. Fast Half Wave Rectifier

This precision rectifier functions somewhat differently from the circuit in *Figure 1*. The input signal is applied through R_1 to the summing node of an inverting operational amplifier. When the signal is negative, D_1 is forward biased and develops an output signal across R_2. As with any inverting amplifier, the gain is R_2/R_1. When the signal goes positive, D_1 is non-conducting and there is no output. However, a negative feedback path is provided by D_2. The path through D_2 reduces the negative output swing to $-0.7V$, and prevents the amplifier from saturating.

Since* the LM101A is used as an inverting amplifier, feedforward compensation can be used. Feedforward compensation increases the slew rate to 10 V/μs and reduces the gain error at high frequencies. This compensation allows the half wave rectifier to operate at higher frequencies than the previous circuits with no loss in accuracy.

The addition of a second amplifier converts the half wave rectifier to a full wave rectifier. As is shown in *Figure 4*, the half wave rectifier is connected to inverting amplifier A_2. A_2 sums the half wave rectified signal and the input signal to provide a full wave output. For negative input signals the output of A_1 is zero and no current flows through R_3. Neglecting for the moment C_2, the output of A_2 is $-\frac{R_7}{R_6} E_{IN}$.

For positive input signals, A_2 sums the currents through R_3 and R_6; and

$$E_{OUT} = R_7\left[\frac{E_{IN}}{R_3} - \frac{E_{IN}}{R_6}\right].$$

If R_3 is ½ R_6, the output is $\frac{R_7}{R_6} E_{IN}$. Hence, the output is always the absolute value of the input.

Filtering, or averaging, to obtain a pure dc output is very easy to do. A capacitor, C_2, placed across R_7 rolls off the frequency response of A_2 to give an output equal to the average value of the input. The filter time constant is R_7C_2, and must be much greater than the maximum period of the input signal. For the values given in *Figure 4*, the time constant is about 2.0 seconds. This converter has better than 1% conversion accuracy to above 100 kHz and less than 1% ripple at 20 Hz. The output is calibrated to read the rms value of a sine wave input.

As with any high frequency circuit some care must be taken during construction. Leads should be kept short to avoid stray capacitance and power supplies bypassed with 0.01 μF disc ceramic capacitors. Capacitive loading of the fast rectifier circuits must be less than 100 pF or decoupling becomes necessary. The diodes should be reasonably fast and film type resistors used. Also, the amplifiers must have low bias currents.

REFERENCES

*R. C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor Corporation, LB-2*, March, 1969.

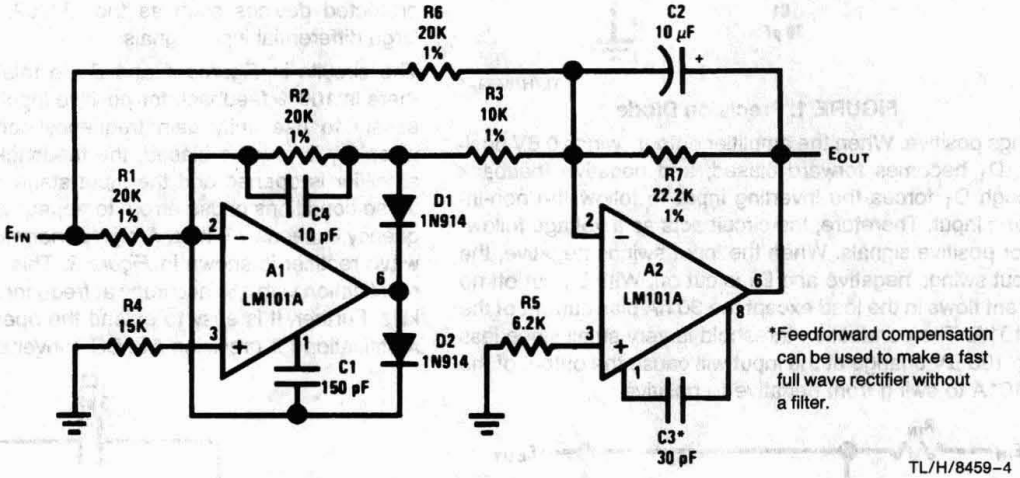
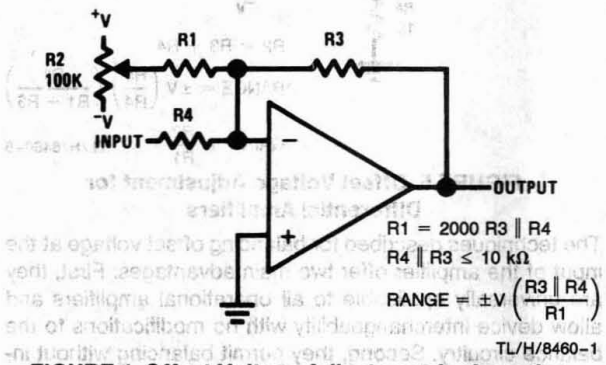


FIGURE 4. Precision AC to DC Converter

Universal Balancing Techniques

National Semiconductor
Linear Brief 9

IC op amps are widely accepted as a universal analog component. Although the circuit designs may vary, most devices are functionally interchangeable. However, offset voltage balancing remains a personality trait of the particular amplifier design. The techniques shown here allow offset voltage balancing without regard to the internal circuitry of the amplifier.



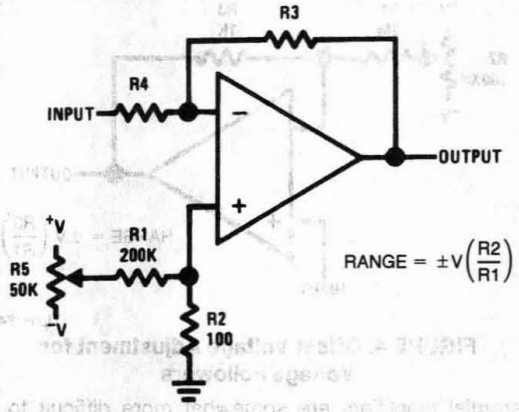
TL/H/8460–1

FIGURE 1. Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less

The circuit shown in *Figure 1* is used to balance out the offset voltage of inverting amplifiers having a source resistance of 10 kΩ or less. A small current is injected into the summing node of the amplifier through R_1. Since R_1 is 2000 times as large as the source resistance the voltage at the arm of the pot is attenuated by a factor of 2000 at the summing node. With the values given and ±15V supplies the output may be zeroed for offset voltages up to ±7.5 mW.

If the value of the source resistance is much larger than 10 kΩ, the resistance needed for R_1 becomes too large. In this case it is much easier to balance out the offset by supplying a small voltage at the non-inverting input of the amplifier. *Figure 2* shows such a scheme. Resistors R_1 and R_2 divide the voltage at the arm of the pot to supply a ±7.5 mW adjustment range with ±15V supplies.

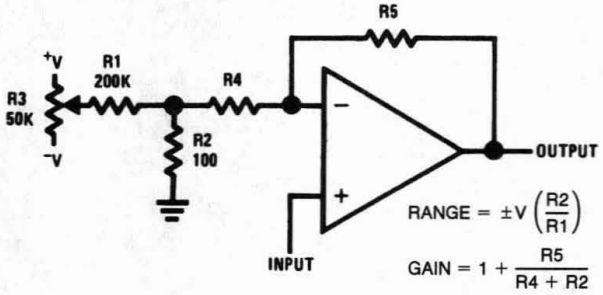
This adjustment method is also useful when the feedback element is a capacitor or non-linear device.



TL/H/8460–2

FIGURE 2. Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element

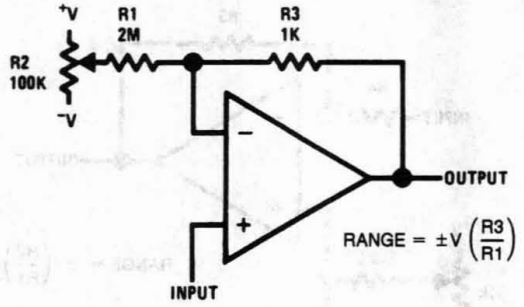
This technique of supplying a small voltage effectively in series with the input is also used for adjusting non-inverting amplifiers. As is shown in *Figure 3*, divider R_1, R_2 reduces the voltage at the arm of the pot to ±7.5 mW for offset adjustment. Since R_2 appears in series with R_4, R_2 should be considered when calculating the gain. If R_4 is greater than 10 kΩ the error due to R_2 is less than 1%.



TL/H/8460–3

FIGURE 3. Offset Voltage Adjustment for Non-Inverting Amplifiers

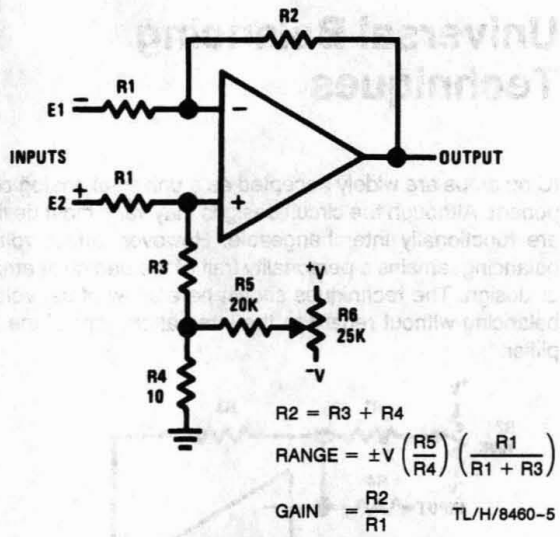
A voltage follower may be balanced by the technique shown in *Figure 4*. R_1 injects a current which produces a voltage drop across R_3 to cancel the offset voltage. The addition of the adjustment resistors causes a gain error, increasing the gain by 0.05%. This small error usually causes no problem. The adjustment circuit essentially causes the offset voltage to appear at full output, rather than at low output levels, where it is a large percentage error.



TL/H/8460–4

FIGURE 4. Offset Voltage Adjustment for Voltage Followers

Differential amplifiers are somewhat more difficult to balance. The offset adjustment used for a differential amplifier can degrade the common mode rejection ratio. *Figure 5* shows an adjustment circuit which has minimal effect on the common mode rejection. The voltage at the arm of the pot is divided by R_4 and R_5 to supply an offset correction of ±7.5 mV. R_4 and R_5 are chosen such that the common mode rejection ratio is limited by the amplifer for values of R_3 greater than 1 kΩ. If R_3 is less than 1k the shunting of R_4 by R_5 must be considered when choosing the value of R_3.



TL/H/8460–5

FIGURE 5. Offset Voltage Adjustment for Differential Amplifiers

The techniques described for balancing offset voltage at the input of the amplifier offer two main advantages: First, they are universally applicable to all operational amplifiers and allow device interchangeability with no modifications to the balance circuitry. Second, they permit balancing without interfering with the internal circuitry of the amplifier. The electrical parameters of the amplifiers are tested and guaranteed without balancing. Although it doesn't usually happen, balancing could degrade performance.

The LM110 An Improved IC Voltage Follower

National Semiconductor
Linear Brief 11

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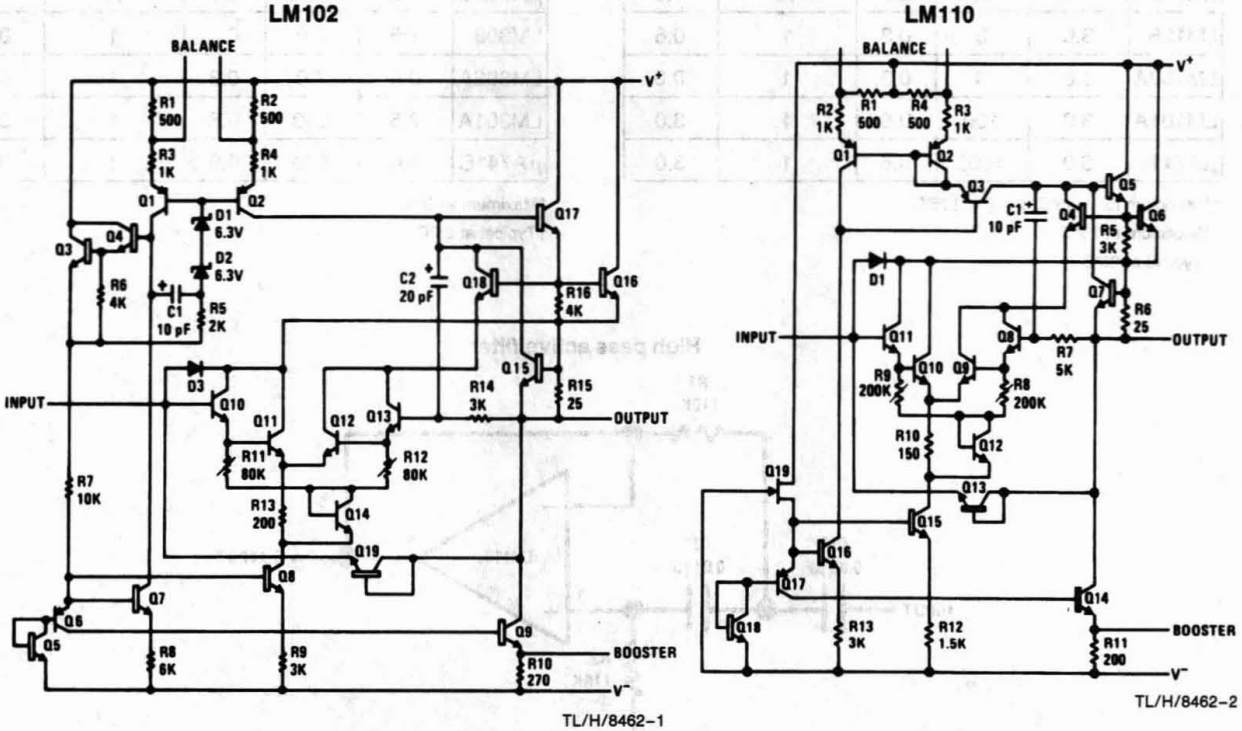
There are quite a few applications where op amps are used as voltage followers. These include sample and hold circuits and active filters as well as general purpose buffers for transducers or other high-impedance signal sources. The general usefullness of such an amplifier is particularly enhanced if it is both fast and has a low input bias current. High speed permits including the buffer in the signal path or within a feedback loop without significantly affecting response or stability. Low input current prevents loading of high impedance sources, which is the reason for using a buffer in the first place.

The LM102, introduced in 1967, was designed specifically as a voltage follower. Therefore, it was possible to optimize performance so that it worked better than general purpose IC amplifiers in this application. This was particularly true with respect to obtaining low input currents along with high-speed operation.

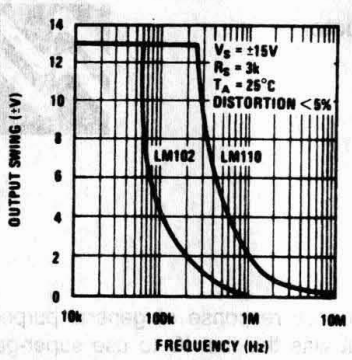
One secret of the LM102's performance is that followers do not require level shifting. Hence, lateral PNP's can be eliminated from the gain path. This has been the most significant limitation on the frequency response of general purpose amplifiers. Secondly, it was the first IC to use super-gain transistors. With these devices, high speed operation can be realized along with low input currents.

The LM110 is a voltage follower that has been designed to supersede the LM102. It is considerably more flexible in its application and offers substantially improved performance. In particular, the LM110 has lower offset-voltage drift, input current and noise. Further, it is faster, less prone to oscillations and operates over a wider range of supply voltages.

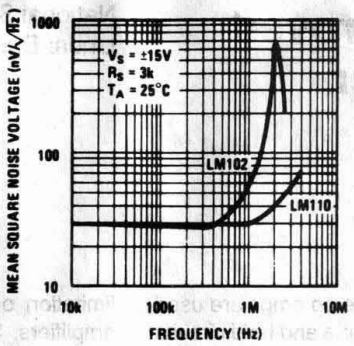
The advantages of the LM110 over the LM102 are described by the following curves. Improvements not included are increased output swing under load, larger small-signal bandwidth, and elimination of oscillations with low-impedance sources. The performance of these devices is also compared with general-purpose op amps in Tables I and II. The advantages of optimizing an IC for this particular slot are clearly demonstrated. Lastly, some typical applications for voltage followers with the performance capability of the LM110 are given.



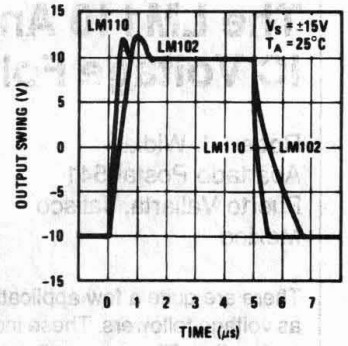
Biggest design difference between the LM102 and LM110 is the elimination of the zener diodes (D1 and D2) in the biasing circuit. This reduces noise and permits operation at low supply voltages.



Power bandwidth of the LM110 is five times larger than the LM102.



Eliminating zeners reduces typical high frequency noise by nearly a factor or 10. Worst case noise is reduced even more. High frequency noise of LM102 has caused problems when it was included inside feedback loop with other IC op amps.



TL/H/8462–3

Large signal pulse response shows 40V/μs slew for LM110 and 10V/μs for LM102. Leading edge overshoot on LM110 is virtually eliminated, so external clamp diode frequently required on the LM102 is not needed.

Table I. Comparing performance of military grade IC op amps in the voltage-follower connection

Device	Offset** Voltage (mV)	Bias** Current (nA)	Slew† Rate (V/μs)	Bandwidth† (MHz)	Supply* Current (mA)
LM110	6.0	10	40	20	5.5
LM102	7.5	100	10	10	5.5
MC1556	6.0	30	2.5	1	1.5
μA715	7.5	4000	20	10	7.0
LM108	3.0	3	0.3	1	0.6
LM108A	1.0	3	0.3	1	0.6
LM101A	3.0	100	0.6	1	3.0
μA741	6.0	1500	0.6	1	3.0

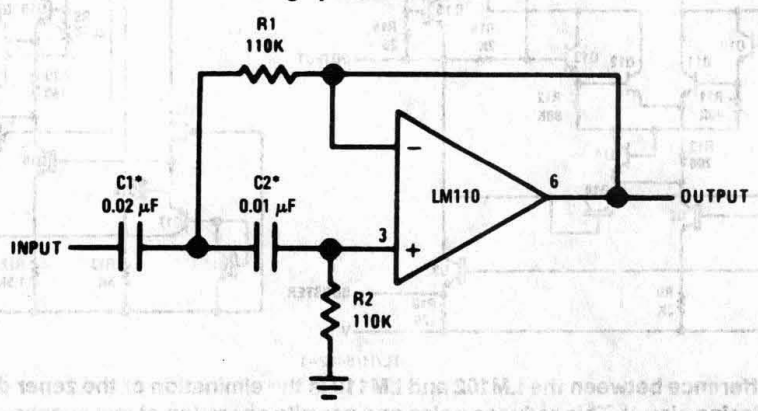
**Maximum for $-55°C \le T_A \le 125°C$
*Maximum at 25°C
†Typical at 25°C

Table II. Comparison of commercial grade devices

Device	Offset* Voltage (mV)	Bias* Current (nA)	Slew† Rate (V/μs)	Bandwidth† (MHz)	Supply* Current (mA)
LM310	7.5	7.0	40	20	5.5
LM302	15	30	20	10	5.5
MC1456	10	30	2.5	1	1.5
μA715C	7.5	1500	20	10	10
LM308	7.5	7.0	0.3	1	0.8
LM308A	0.5	7.0	0.3	1	0.8
LM301A	7.5	250	0.6	1	3.0
μA741C	6.0	500	0.6	1	3.0

*Maximum at 25°C
†Typical at 25°C

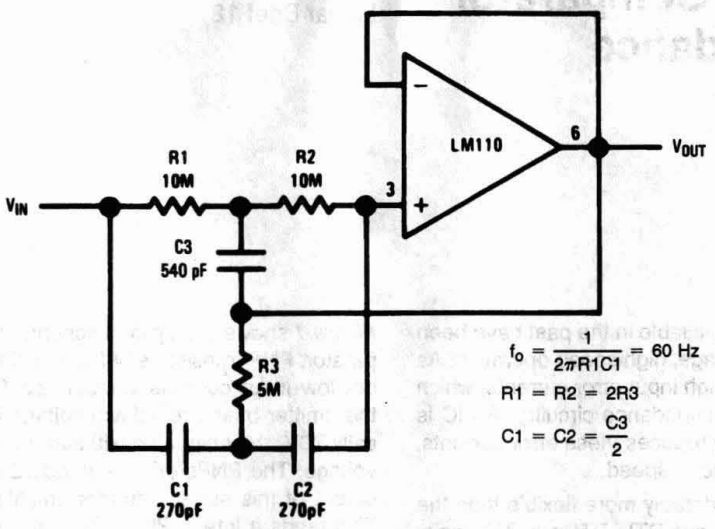
High pass active filter



TL/H/8462–4

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability

High Q Notch Filter



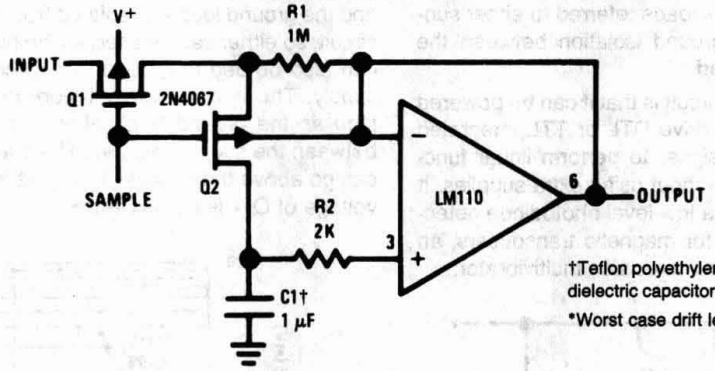
$$f_o = \frac{1}{2\pi R1C1} = 60\ \text{Hz}$$

$$R1 = R2 = 2R3$$

$$C1 = C2 = \frac{C3}{2}$$

TL/H/8462–5

Low Drift Sample and Hold*

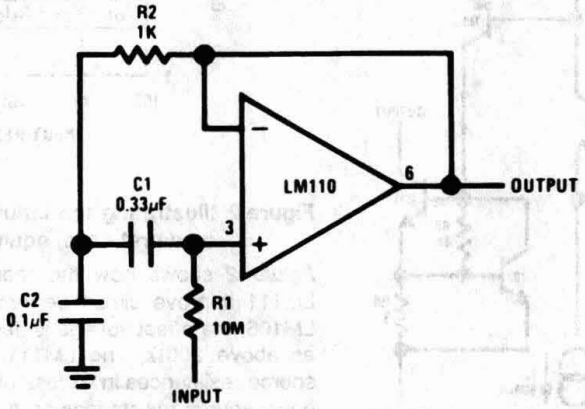


†Teflon polyethylene or polycarbonate dielectric capacitor

*Worst case drift less than 3 mV sec

TL/H/8462–6

Bandpass Filter



TL/H/8462–7

An IC Voltage Comparator for High Impedance Circuitry

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Linear Brief 12

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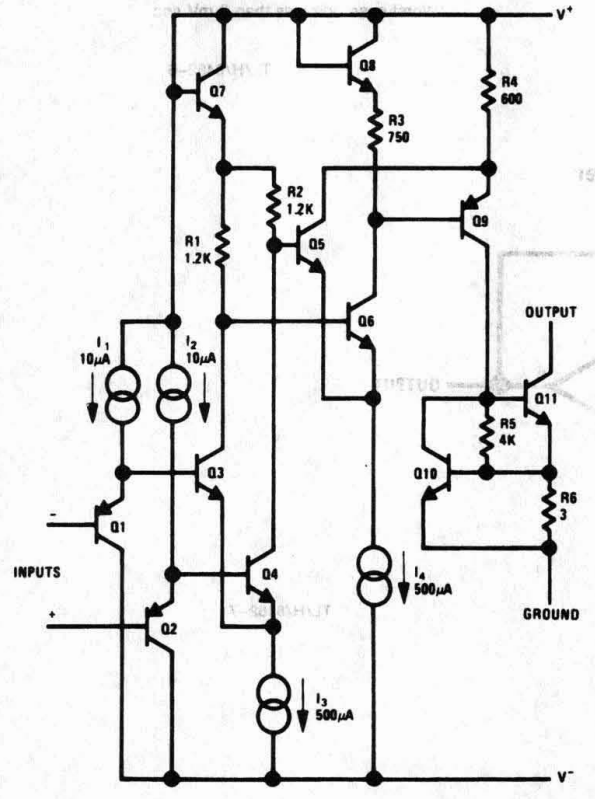
The IC voltage comparators available in the past have been designed primarily for low voltage, high speed operation. As a result, these devices have high input error currents, which limit their usefulness in high impedance circuitry. An IC is described here that drastically reduces these error currents, with only a moderate decrease in speed.

This new comparator is considerably more flexible than the older devices. Not only will it drive RTL, DTL and TTL logic; but also it can interface with MOS logic and FET analog switches. It operates from standard ±15V op amp supplies and can switch 50V, 50 mA loads, making it useful as a driver for relays, lamps or light-emitting diodes. A unique output stage enables it to drive loads referred to either supply or ground and provide ground isolation between the comparator inputs and the load.

Another useful feature of the circuit is that it can be powered from a single 5V supply and drive DTL or TTL integrated circuits. This enables the designer to perform linear functions on a digital-circuit card without using extra supplies. It can, for example, be used as a low-level photodiode detector, a zero crossing detector for magnetic transducers, an interface for high-level logic or a precision multivibrator.

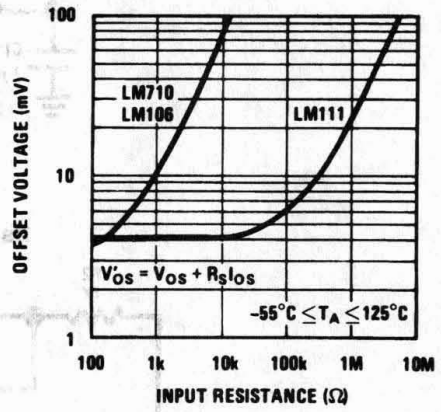


TL/H/8463-1

Figure 1. Simplified schematic of the LM111

Figure 1 shows a simplified schematic of this versatile comparator. PNP transistors buffer the differential input stage to get low input currents without sacrificing speed. Because the emitter base breakdown voltage of these PNPs is typically 70V, they can also withstand a large differential input voltage. The PNPs drive a standard differential stage. The output of this stage is further amplified by the Q_5-Q_6 pair. This feeds a lateral PNP, Q_9, that provides additional gain and drives the output stage.

The output transistor is Q_{11} which is driven by the level shifting PNP. Current limiting is provided by R_6 and Q_{10} to protect the circuit from intermittent shorts. Both the output and the ground lead are isolated from other points within the circuit, so either can be used as the output. The V^- terminal can also be tied to ground to run the circuit from a single supply. The comparator will work in any configuration as long as the ground terminal is at a potential somewhere between the supply voltages. The output terminal, however, can go above the positive supply as long as the breakdown voltage of Q_{11} is not exceeded.



TL/H/8463-2

Figure 2. Illustrating the influence of source resistance on worst case, equivalent input offset voltage

Figure 2 shows how the reduced error currents of the LM111 improve circuit performance. With the LM710 or LM106, the offset voltage is degraded for source resistances above 200Ω. The LM111, however, works well with source resistances in excess of 30 kΩ. *Figure 2* applies for equal source resistances on the two inputs. If they are unequal, the degradation will become pronounced at lower resistance levels.

Table I gives the important electrical characteristics of the LM111 and compares them with the specifications of older ICs.

A few, typical applications of the LM111 are illustrated in *Figure 3*. The first is a zero crossing detector driving a MOS

Table I. Comparing the LM111 with earlier IC comparators. Values given are worst case over a −55°C to +125°C temperature range, except as noted.

Parameter	LM111	LM106	LM710	Units
Input Offset Voltage	4	3	3	mV
Input Offset Current	0.02	7	7	μA
Input Bias Current	0.15	45	45	μA
Common Mode Range	±14	±5	±5	V
Differential Input Voltage Range	±30	±5	±5	V
Voltage Gain†	200	40	1.7	V/mV
Response Time†	200	40	40	ns
Output Drive Voltage Current	 50 50	 24 100	 2.5 1.6	 V mA
Fan Out (DTL/TTL)	8	16	1	
Power Consumption	80	145	160	mW

†Typical at 25°C.

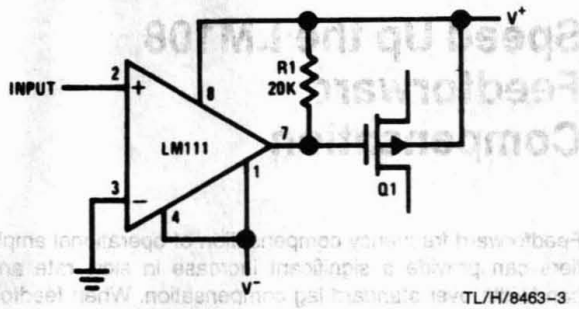
analog switch. The ground terminal of the IC is connected to V^-; hence, with ±15V supplies, the signal swing delivered to the gate of Q_1 is also ±15V. This type of circuit is useful where the gain or feedback configuration of an op amp circuit must be changed at some precisely-determined signal level. Incidentally, it is a simple matter to modify the circuit to work with junction FETs.

The second circuit is a zero crossing detector for a magnetic pickup such as a magnetometer or shaft-position pickoff. It delivers the output signal directly to DTL or TTL logic circuits and operates from the 5V logic supply. The resistive divider, R_1 and R_2, biases the inputs 0.5V above ground, within the common mode range of the device. An optional offset balancing circuit, R_3 and R_4, is included.

The next circuit shows a comparator for a low-level photodiode operating with MOS logic. The output changes state when the diode current reaches 1 μA. At the switching point, the voltage across the photodiode is nearly zero, so its leakage current does not cause an error. The output switches between ground and −10V, driving the data inputs of MOS logic directly.

The last circuit shows how a ground-referred load is driven from the ground terminal of the LM111. The input polarity is reversed because the ground terminal is used as the output. An incandescent lamp, which is the load here, has a cold resistance eight times lower than it is during normal operation. This produces a large inrush current, when it is switched on, that can damage the switch. However, the current limiting of the LM111 holds this current to a safe value.

The applications described above show that the output-circuit flexibility and wide supply-voltage range of the LM111 opens up new fields for IC comparators. Further, its low error currents permit its use in circuits with impedance levels above 1 kΩ. Although slower than older devices, it is more than an order of magnitude faster than op amps used as comparators.



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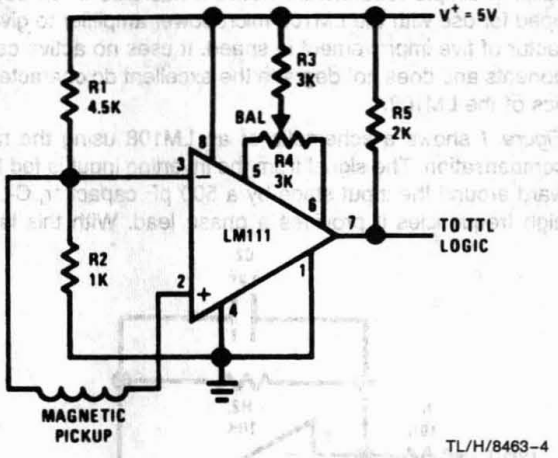
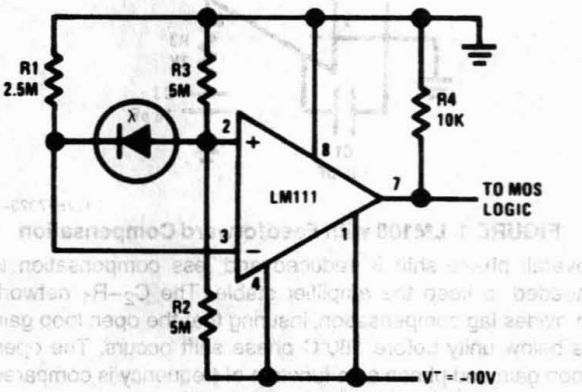
a. zero crossing detector driving analog switch



TL/H/8463–4

b. detector for magnetic transducer



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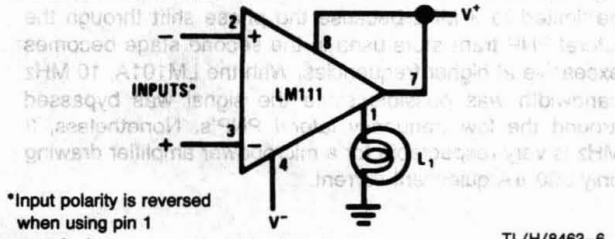
c. comparator for low level photodiode



*Input polarity is reversed when using pin 1 as output.

TL/H/8463–6

d. driving ground—referred load

Figure 3. Typical applications of the LM111

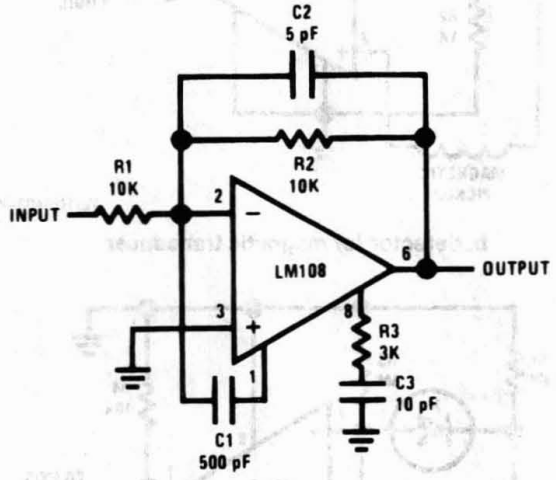
The LM111 has the same pin configuration as the LM710 and LM106. It is interchangeable with these devices in applications where speed is not of prime concern.

Speed Up the LM108 Feedforward Compensation

National Semiconductor
Linear Brief 14

Feedforward frequency compensation of operational amplifiers can provide a significant increase in slew rate and bandwidth over standard lag compensation. When feedforward compensation is applied to the LM101A operational amplifier,[1] an order of magnitude increase in bandwidth results. A simple feedforward network has also been developed for use with the LM108 micropower amplifier to give a factor of five improvement in speed. It uses no active components and does not degrade the excellent dc characteristics of the LM108.

Figure 1 shows a schematic of an LM108 using the new compensation. The signal from the inverting input is fed forward around the input stage by a 500 pF capacitor, C_1. At high frequencies it provides a phase lead. With this lead,



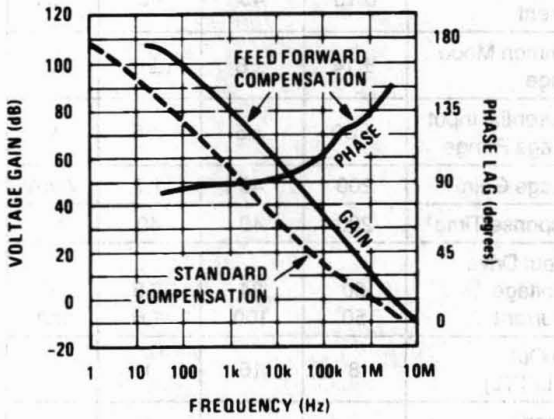
TL/H/7328–1

FIGURE 1. LM108 with Feedforward Compensation

overall phase shift is reduced and less compensation is needed to keep the amplifier stable. The C_2–R_1 network provides lag compensation, insuring that the open loop gain is below unity before 180°C phase shift occurs. The open loop gain and phase as a function of frequency is compared with standard compensation in *Figure 2*.

The slew rate is increased from 0.3V/μs to about 1.3V/μs and the 1 kHz gain is increased from 500 to 10,000. Small signal bandwidth is extended to 3 MHz. The bandwidth must be limited to 3 MHz because the phase shift through the lateral PNP transistors used in the second stage becomes excessive at higher frequencies. With the LM101A, 10 MHz bandwidth was possible since the signal was bypassed around the low frequency lateral PNP's. Nonetheless, 3 MHz is very respectable for a micropower amplifier drawing only 300 μA quiescent current.

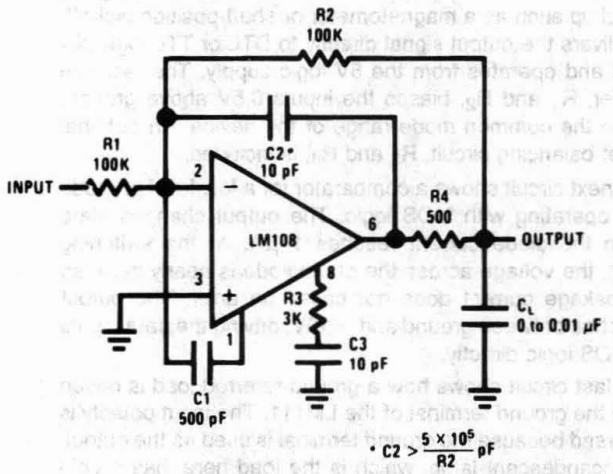
When the LM108 is used with feedforward compensation, it is less tolerant of capacitive loading and stray capacitance. Precautions must be taken to insure stability. If load capaci-



TL/H/7328–2

FIGURE 2. Open Loop Voltage Gain

tance is greater than about 75 to 100 pF, it must be isolated as shown in *Figure 3*. A small capacitor is always needed to provide a lead across the feedback resistor to compensate for strays at the input. About 3 to 5 pF is the minimum value capacitor. Care must be taken to minimize stray capacitance at Pins 1, 2 and 8 when feedforward compensation is used. Additionally, when the source resistance on the noninverting input is greater than 10k, it should be bypassed with a 0.1 μF capacitor.



TL/H/7328–3

FIGURE 3. Decoupling Load Capacitance

As with any externally compensated amplifier, increasing the compensation of the LM108 increases the stability at the expense of slew and bandwidth. The circuit shown is for the fastest response. Increasing the size of C_2 to 20 or 30 pF will provide 2 or 3 times greater stability and capacitive

load tolerance. Therefore, the size of the compensation capacitor should be optimized for the bandwidth of the particular application.

The stability of the LM108 with feedforward compensation is indicated by the small signal transient responses shown in *Figure 4*. It is quite stable since there is little overshoot and ringing even though the amplifier is loaded with a 50 pF capacitor. Large signal transient response for a 20V square wave is shown in *Figure 5*. The small positive overshoot is not severe and usually causes no problems.

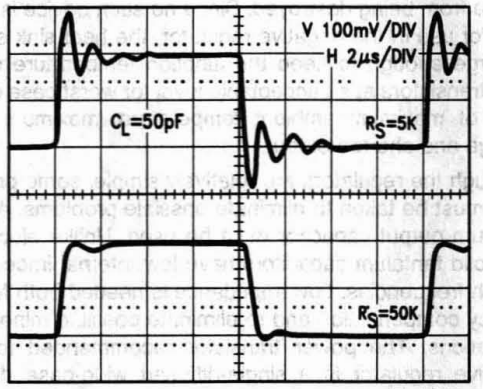


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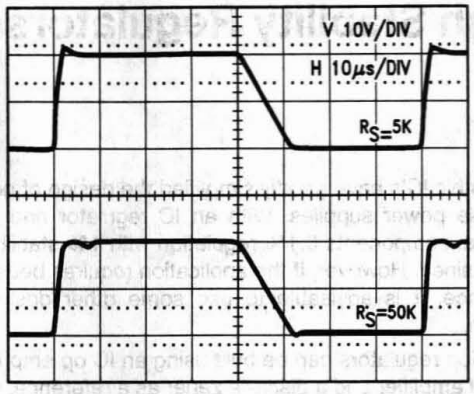
FIGURE 4. Small Signal Transient Response of LM108 with Feedforward Compensation

The LM108 is unusually insensitive to power supply bypassing with the new compensation. Even with several feet of wire between the device and power supply, it does not become unstable. However, it is still wise to bypass the supplies for drill since noise on the V^+ line can be injected to the summing junction by the 500 pF feedforward capacitor.



TL/H/7328–5

FIGURE 5. Large Signal Transient Response of LM108 with Feedforward Compensation

The new feedforward compensation is easy to use and offers a factor of five improvement over standard compensation. Slew rate is increased to 1.3V/μs and power bandwidth extended to 20 kHz. Also, gain error at high frequencies is reduced. This makes the LM108 more useful in precision applications where low dc error as well as low ac error is desired.

REFERENCE

1. Robert C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor LB-2*, March, 1969.

High Stability Regulators

National Semiconductor
Linear Brief 15

Monolithic IC's have greatly simplified the design of general purpose power supplies. With an IC regulator and a few external components 0.1% regulation with 1% stability can be obtained. However, if the application requires better performance, it is advisable to use some other design approach.

Precision regulators can be built using an IC op amp as the control amplifier and a discrete zener as a reference, where the performance is determined by the reference. *Figures 1* and *2* show schematics of simple positive and negative regulators. They are capable of providing better than 0.01% regulation for worst case changes of line, load and temperature. Typically, the line rejection is 120 dB to 1 kHz; and the load regulation is better than 10 μV for a 1A change. Temperature is the worst source of error; however, it is possible to achieve less than a 0.01% change in the output voltage over a $-55°C$ to $+125°C$ range.

The operation of both regulators is straightforward. An internal voltage reference is provided by a high-stability zener diode. The LM108A[1] operational amplifier compares a fraction of the output voltage with reference. In the positive regulator, the output of the op amp controls the ground terminal of an LM109[2] regulator through source follower, Q_1. Frequency compensation for the regulator is provided by both the R_1 C_2 combination and output capacitor, C_3.

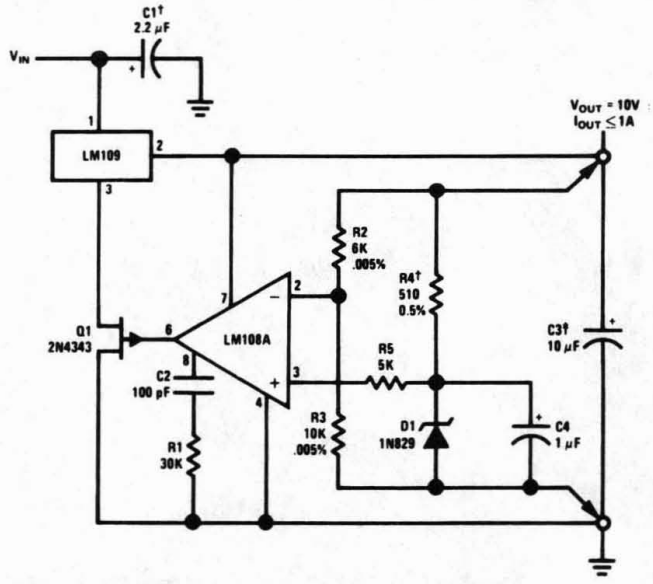
The negative regulator shown in *Figure 2* operates similarly, except that discrete transistors are used for the pass element. A transistor, Q_1, level shifts the output of the LM108 to drive output transistors, Q_3 and Q_4. Current limiting is provided by Q_2. Capacitors C_3 and C_4 frequency compensate the regulator.

In the positive regulator the use of an LM109 instead of discrete power transistors has several advantages. First, the LM109 contains all the biasing and current limit circuitry needed to supply a 1A load. This simplifies the regulator. Second, and probably most important, the LM109 has thermal overload protection, making the regulator virtually burnout proof. If the power dissipation becomes excessive or if there is inadequate heat sinking, the LM109 will turn off when the chip temperature reaches 175°C, preventing the device from being destroyed. Since no such device is available for use in the negative regulator, the heat sink should be large enough to keep the junction temperature of the pass transistors at an acceptable level for worst case conditions of maximum ambient temperature, maximum input voltage and shorted output.

Although the regulators are relatively simple, some precautions must be taken to eliminate possible problems. A solid tantalum output capacitor must be used. Unlike electrolytics, solid tantalum capacitors have low internal impedance at high frequencies. Low impedance is needed both for frequency compensation and to eliminate possible minor loop oscillations. The power transistor recommended for the negative regulator is a single-diffused wide-base device. This transistor type has fewer oscillation problems than double diffused transistors. Also, it seems less prone to failure under overload conditions.

Some unusual problems are encountered in the construction of a high stability regulator. Component choice is most important since the resistors, amplifier and zener can contribute to temperature drift. Also, good circuit layout is needed to eliminate the effect of lead drops, pickup, and thermal gradients.

The resistors must be low-temperature-coefficient wirewound or precision metal film. Ordinary 1% carbon film, tin oxide or metal film units are not suitable since they may drift as much as 0.5% over temperature. The resistor accuracy need not be 0.005% as shown in the schematic; however, they should track better than 1 ppm/°C. Additionally, wirewound resistors usually have lower thermoelectric effects than film types. The resistor driving the zener is not quite

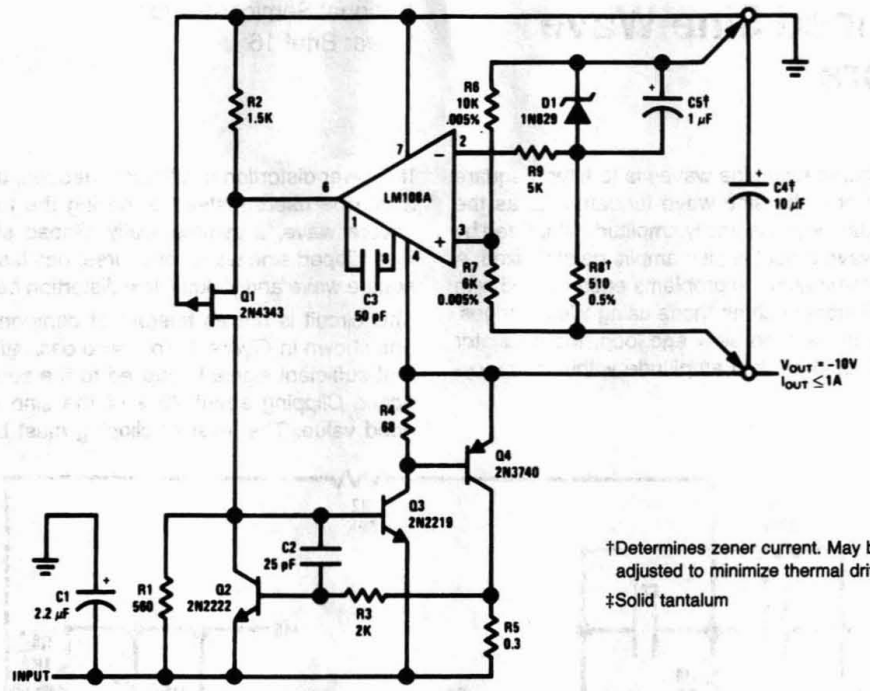


†Determines zener current. May be adjusted to minimize thermal drift.

‡Solid tantalum

TL/H/8465–1

FIGURE 1. High Stability Positive Regulator



TL/H/8465–2

FIGURE 2. High Stability Negative Regulator

as critical; but it should change less than 0.2% over temperature.

The excellent dc characteristics of the LM108A make it a good choice as the control amplifier. The offset voltage drift of less than 5 μV/°C contributes little error to the regulator output. Low input current allows standard cells to be used for the voltage reference instead of a reference diode. Also the LM108 is easily frequency compensated for regulator applications.

Of course, the most important item is the reference. The IN829 diode is representative of the better zeners available. However, it still has a temperature coefficient of 0.0005%/°C or a maximum drift of 0.05% over a −55°C to +125°C temperature range. The drift of the zener is usually linear with temperature and may be varied by changing the operating current from its nominal value of 7.5 mA. The temperature coefficient changes by about 50 μV/°C for a 15% change in operating current. Therefore, by adjusting the zener current, the temperature drift of the regulator may be minimized.

Good construction techniques are important. It is necessary to use remote sensing at the load, as is shown on the schematics. Even an inch of wire will degrade the load regulation. The voltage setting resistors, zener, and the amplifier should also be shielded. Board leakages or stray capacitance can easily introduce 100 μV of ripple or dc error into the regulator. Generally, short wire length and single-point grounding are helpful in obtaining proper operation.

REFERENCES

1. R.J. Widlar, "IC Op Amp Beats FETs on Input Current," *National Semiconductor AN-29*, December, 1969.
2. R.J. Widlar, "New Developments in IC Voltage Regulators," in *1970 International Solid-State Circuits Conference Digest of Technical Papers*, Vol. XIII, pp. 158–159.

Easily Tuned Sine Wave Oscillators

National Semiconductor
Linear Brief 16

One approach to generating sine waves is to filter a square wave. This leaves only the sine wave fundamental as the output. Since a square wave is easily amplitude stabilized by clipping, the sine wave output is also amplitude stabilized. A clipping oscillator eliminates the problems encountered with agc stabilized oscillators such as those using Wein bridges. Additionally, since there is no slow agc loop, the oscillator starts quickly and reaches final amplitude within a few cycles.

If a lower distortion oscillator is needed, the circuit in *Figure 2* can be used. Instead of driving the tuned circuit with a square wave, a symmetrically clipped sine wave is used. The clipped sine wave, of course, has less distortion than a square wave and yields a low distortion output when filtered.

This circuit is not as tolerant of component values as the one shown in *Figure 1*. To insure oscillation, it is necessary that sufficient signal is applied to the zeners for clipping to occur. Clipping about 20% of the sine wave is usually a good value. The level of clipping must be high enough to insure oscillation over the entire tuning range. If the clipping is too small, it is possible for the circuit to cease oscillation due to tuning, component aging, or temperature changes. Higher clipping levels increase distortion. As with the circuit in *Figure 1*, this circuit is self-starting.

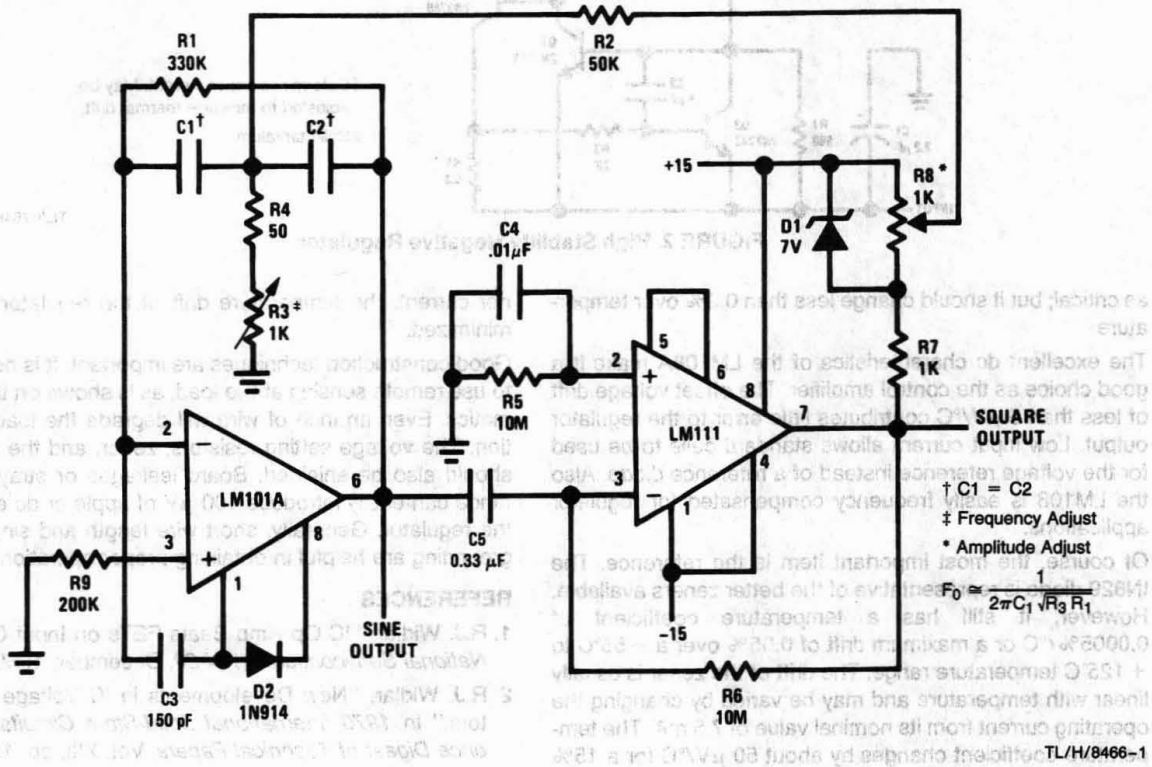


FIGURE 1. Easily Tuned Sine Wave Oscillator

The circuit in *Figure 1* will provide both a sine and square wave output for frequencies from below 20 Hz to above 20 kHz. The frequency of oscillation is easily tuned by varying a single resistor. This is a considerable advantage over Wein bridge circuits where two elements must be tuned simultaneously to change frequency. Also, the output amplitude is relatively stable when the frequency is changed.

An operational amplifier is used as a tuned circuit, driven by square wave from a voltage comparator. Frequency is controlled by R_1, R_2, C_1, C_2, and R_3, with R_3 used for tuning. Tuning the filter does not affect its gain or bandwidth so the output amplitude does not change with frequency. A comparator is fed with the sine wave output to obtain a square wave. The square wave is then fed back to the input of the tuned circuit to cause oscillation. Zener diode, D_1, stabilizes the amplitude of the square wave fed back to the filter input. Starting is insured by R_6 and C_5 which provide dc negative feedback around the comparator. This keeps the comparator in the active region.

Table I shows the component values for the various frequency ranges. Distortion from the circuit in *Figure 1* ranges between 0.75% and 2% depending on the setting of R_3. Although greater tuning range can be accomplished by increasing the size of R_3 beyond 1 kΩ, distortion becomes excessive. Decreasing R_3 lower than 50Ω can make the filter oscillate by itself. The circuit in *Figure 2* varies between 0.2% and 0.4% distortion for 20% clipping.

About 20 kHz is the highest usable frequency for these oscillators. At higher frequencies the tuned circuit is incapable of providing the high Q bandpass characteristic needed to filter the input into a clean sine wave. The low frequency end of oscillation is not limited except by capacitor size.

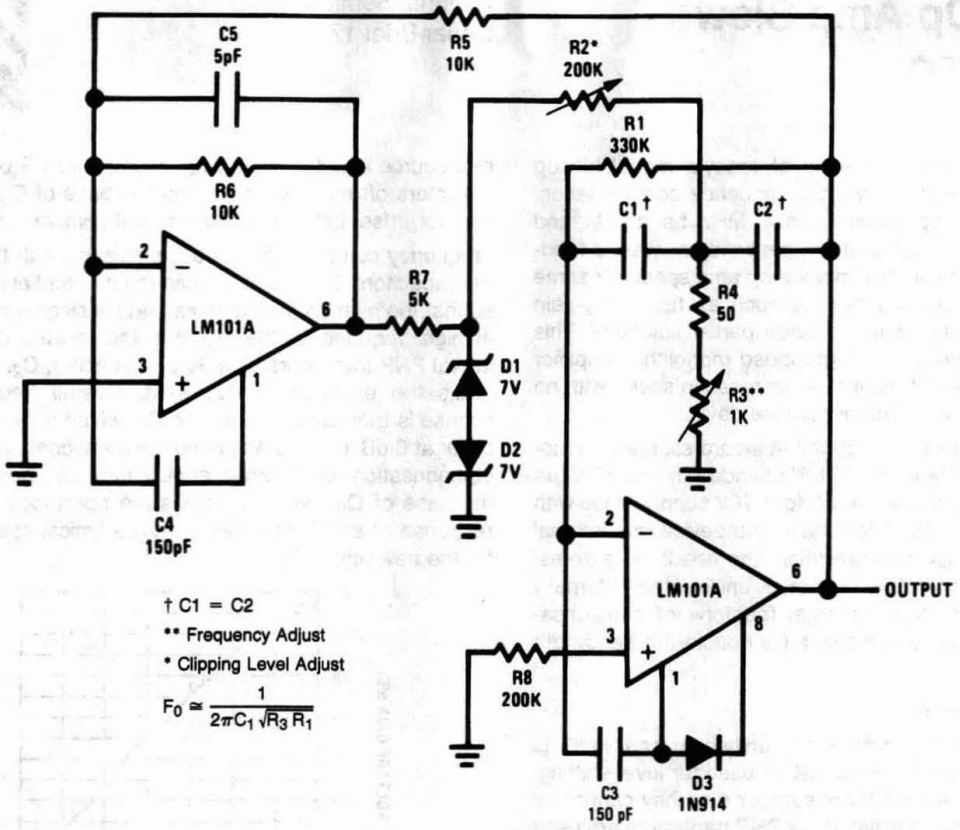


FIGURE 2. Low Distortion Sine Wave Oscillator

TABLE I

C_1, C_2	Min Frequency	Max Frequency
0.47 μF	18 Hz	80 Hz
0.1 μF	80 Hz	380 Hz
.022 μF	380 Hz	1.7 kHz
.0047 μF	1.7 kHz	8 kHz
.002 μF	4.4 kHz	20 kHz

In both oscillators, feedforward compensation[3] is used on the LM101A amplifiers to increase their bandwidth. Feedforward increases the bandwidth to over 10 MHz and the slew rate to better than 10 V/μs. With standard compensation the maximum output frequency would be limited to about 6 kHz.

Although these oscillators are not particularly tricky, good construction techniques are important. Since the amplifiers and the comparators are both wide band devices, proper power supply bypassing is in order. Both the positive and negative supplies should be bypassed with a 0.1 μF disc ceramic capacitor. The fast transition at the output of the comparator can be coupled to the sine wave output by stray capacitance, causing spikes on the output. Therefore the output of the comparator with the associated circuitry should be shielded from the inputs of the op amp.

Component choice is also important. Good quality resistors and capacitors must be used to insure temperature stability. Capacitor should be mylar, polycarbonate, or polystyrene — electrolytics will not work. One percent resistors are usually adequate.

The circuits shown provide an easy method of generating a sine wave. The frequency of oscillation can be varied over greater than a 4 to 1 range by changing a single resistor. The ease of tuning as well as the elimination of critical agc loops make these oscillators well suited for high volume production since no component selection is necessary.

REFERENCES

1. N.P. Doyle, "Swift, Sure Design of Active Bandpass Filters," *EDN*, Vol. 15, No. 2, January 15, 1970.
2. R.J. Widlar, "Precision IC Comparator Runs from 5V Logic Supply," *National Semiconductor AN-41*, October, 1970.
3. Robert C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor LB-2*, March, 1969.

LM118 Op Amp Slews 70 V/μsec

National Semiconductor
Linear Brief 17

One of the greatest limitations of today's monolithic op amps is speed. With unity gain frequency compensation, general purpose op amps have 1 MHz bandwidth and 0.3 V/μs slew rate. Optimized compensation as well as feedforward compensation can improve op amp speed for some applications. Specialized devices such as fast, unity-gain buffers are available which provide partial solutions. This paper will describe a new high speed monolithic amplifier that offers an order of magnitude increase in speed with no loss in flexibility over general purpose devices.

The LM118 is constructed by the standard six mask monolithic process and features 15 MHz bandwidth and 70 V/μs slew rate. It operates over a ±5 to ±18V supply range with little change in speed. Additionally, the device has internal unity-gain frequency compensation and needs no external components for operation. However, unlike other internally compensated amplifiers, external feedforward compensation may be added to approximately double the bandwidth and slew rate.

DESIGN CONCEPTS

In general purpose amplifiers the unity-gain bandwidth is limited by the lateral PNP transistors used for level shifting. The response above 2 MHz is so poor that they cannot be used in a feedback amplifier. If the PNP transistors are used for level shifting only at DC or low frequencies and the signal is fed forward around the PNP transistors at high frequencies, wide bandwidth can be obtained without the excessive phase shift of the PNP transistors.

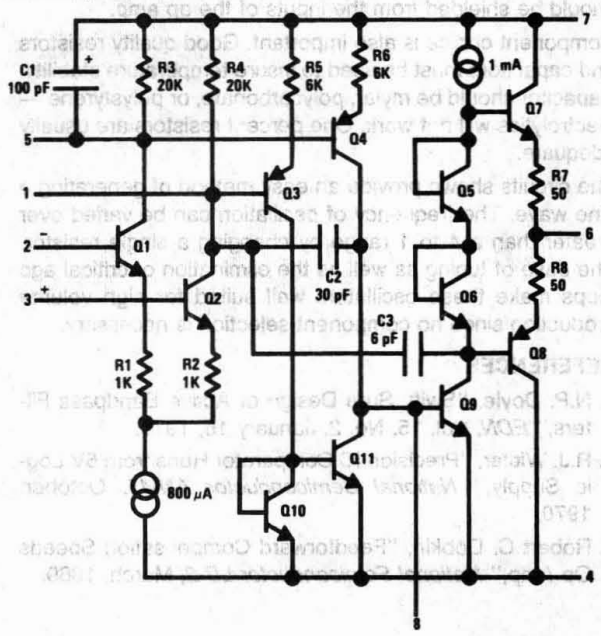


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FIGURE 1. Simplified Circuit of the LM118

Figure 1 shows a simplified schematic of the LM118. Transistors Q_1 and Q_2 are a conventional differential input stage with emitter degeneration and resistive collector loads. Q_3 and Q_4 form the second stage which further amplify the signal and level shift the signal towards V^-. The collectors of Q_3 and Q_4 drive a current inverter, Q_{10} and Q_{11} to convert from differential to single ended. Q_9, which has a current source load for high gain, drives a class B output. The collectors of the input stage and the base of Q_9 are available for offset balancing and external compensation.

Frequency compensation is accomplished with three internal capacitors. C_1 rolls off on half the differential input stage so that the high frequency signal path is single-ended. Also, at high frequencies, the signal is fed forward around the lateral PNP transistors by a 30 pF capacitor, C_2. This eliminates the excessive phase shift. Overall frequency response is then set by capacitor, C_3, which rolls off the amplifier at 6 dB/octave. As previously mentioned feedforward compensation for inverting applications can be applied to the base of Q_9. *Figure 2* shows the open loop frequency response of an LM118. Table I gives typical specifications for the new amplifier.

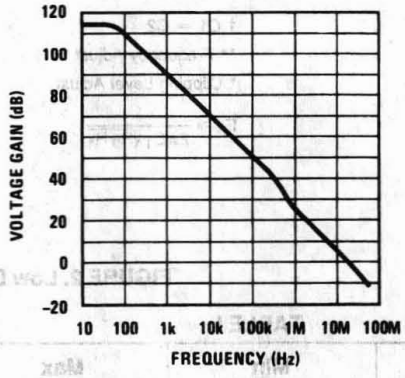

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FIGURE 2. Open Loop Voltage Gain as a Function of Frequency for LM118

TABLE I. Typical Specifications for the LM118

Input Offset Voltage	2 mV
Input Bias Current	200 nA
Offset Current	20 nA
Voltage Gain	200k
Common Mode Range	±11.5V
Output Voltage Swing	±13V
Small Signal Bandwidth	15 MHz
Slew Rate	70 V/μs

OPERATING CONFIGURATION

Although considerable effort was taken to make the LM118 trouble free, high frequency amplifiers are more prone to oscillations than low frequency devices such as the LM101A. Care must be taken to minimize the stray capacitance at the inverting input and at the output; however the LM118 will drive a 100 pF load. Good power supply bypassing is also in order—0.1 μF disc ceramic capacitors should be used within a few inches of the amplifier. Additionally, a small capacitor is usually necessary across the feedback resistor to compensate for unavoidable stray capacitance.

Figure 3 shows feedforward compensation of the LM118 for fast inverting applications. The signal is fed from the summing junction to the output stage driver by C_1 and R_4. Re-

sistors R_5, R_6 and R_7 have two purposes: they increase the internal operating current of the output stage to increase slew rate and they provide offset balancing. The current boost is necessary to drive internal stray capacitance at the higher slew rate. Mismatch of the external resistors can cause large voltage offsets so offset balancing is necessary. For supply voltages other than ±15V, R_5 and R_6 should be selected to draw about 500 μA from Pins 1 and 5.

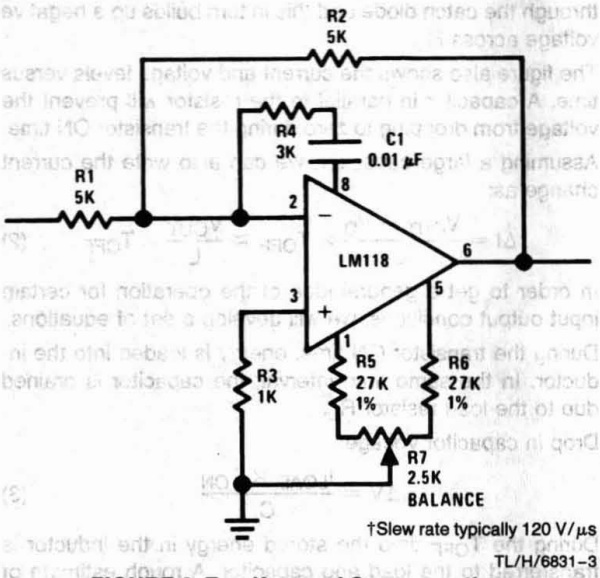


FIGURE 3. Feedforward Compensation for Greater Inverting Slew Rate†

When using feedforward resistor R_4 should be optimized for the application. It is necessary to have about 8 kΩ in the path from the output of the amplifier through the feedback resistor and through feedforward network to Pin 8 of the device. The series resistance is needed to limit the bandwidth and prevent minor loop oscillation.

At high gains, or with high value feedback resistors R_4 can be quite low—but not less than 100Ω. When the LM118 is used as a fast integrator, with a large feedback capacitor or with low values of feedback resistance, R_4 must be increased to 8 kΩ to insure stability over a full −55°C to +125°C temperature range.

One of the more important considerations for a high speed amplifier is settling time. Poor settling time can cancel the advantages of having high slew rate and bandwidth. For example—an amplifier can have severe ringing after a step input. A relatively long time is then needed before the output voltage can be read accurately. Settling time is the time necessary for the output to slew through a defined voltage change and settle to within a defined error of its final output voltage. *Figure 4* shows optimized compensation for settling

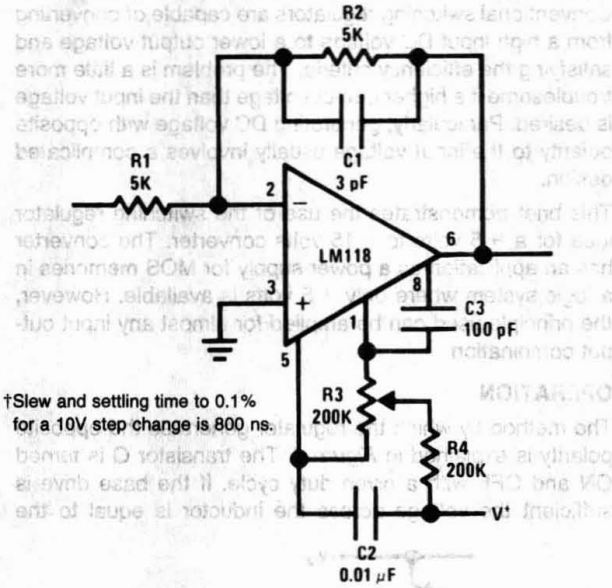


FIGURE 4. Compensation for Minimum Settling† Time

to within 0.1% error. Typically the settling time is 800 ns for a simple inverter circuit as shown. Settling time is, of course, subject to operating conditions external to the IC such as closed loop gain, circuit layout, stray capacitance and source resistance. An optional offset balancing circuit, R_3 and R_4 is included.

The LM118 opens up new fields for IC operational amplifiers. It is more than an order of magnitude faster than general purpose amplifiers while retaining the ease of use features. It is ideally suited for analog to digital converters, active filters, sample and hold circuits and wide band amplification. Further, the LM118 has the same pin configuration as the LM101A or LM741 and is interchangeable with these devices when speed is of prime concern.

+5 to −15 Volts DC Converter

National Semiconductor
Linear Brief 18

INTRODUCTION

It is frequently necessary to convert a DC voltage to another higher or lower DC-voltage while maximizing efficiency. Conventional switching regulators are capable of converting from a high input DC voltage to a lower output voltage and satisfying the efficiency criteria. The problem is a little more troublesome if a higher output voltage than the input voltage is desired. Particularly, generating DC voltage with opposite polarity to the input voltage usually involves a complicated design.

This brief demonstrates the use of the switching regulator idea for a +5 volts to −15 volts converter. The converter has an application as a power supply for MOS memories in a logic system where only +5 volts is available. However, the principle used can be amplied for almost any input output combination.

OPERATION

The method by which the regulator generates the opposite polarity is explained in *Figure 1*. The transistor Q is turned ON and OFF with a given duty cycle. If the base drive is sufficient the voltage across the inductor is equal to the supply voltage minus V_{SAT}. The current change in the inductor is given by:

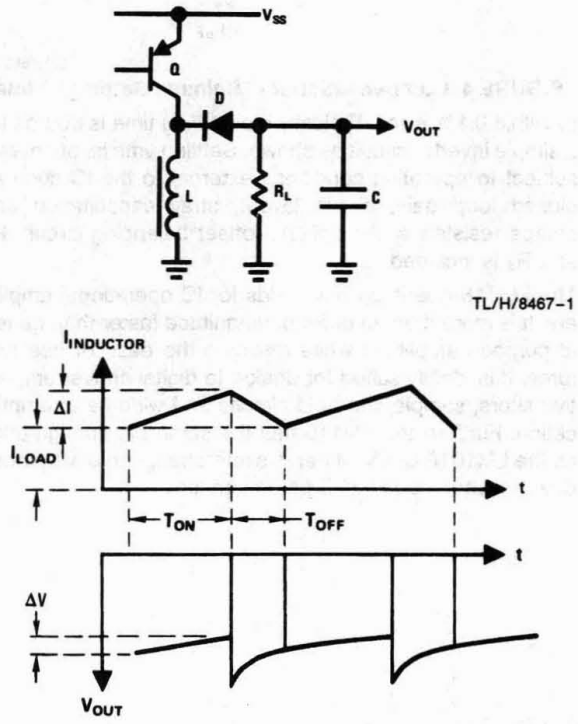


FIGURE 1. Switching Circuit for Voltage Conversion

$$\Delta I = \frac{V_{SS} - V_{SAT}}{L} \times T_{ON} \approx \frac{V_{SS}}{L} T_{ON} \qquad (1)$$

Turning OFF the transistor the inductor current has a path through the catch diode and this in turn builds up a negative voltage across R_L.

The figure also shows the current and voltage levels versus time. A capacitor in parallel to the resistor will prevent the voltage from dropping to zero during the transistor ON time.

Assuming a large capacitor, we can also write the current change as:

$$\Delta I = \frac{V_{OUT} - V_D}{L} \times T_{OFF} \approx \frac{V_{OUT}}{L} \times T_{OFF} \qquad (2)$$

In order to get a general idea of the operation for certain input output conditions, we will develop a set of equations.

During the transistor ON time, energy is loaded into the inductor. In the same time interval, the capacitor is drained due to the load resistor R_L.

Drop in capacitor voltage:

$$\Delta V = \frac{I_{LOAD} \times T_{ON}}{C} \qquad (3)$$

During the T_{OFF} time the stored energy in the inductor is transferred to the load and capacitor. A rough estimate of T_{OFF} can be expressed as:

$$T_{OFF} = \frac{V_{SS}}{V_{OUT}} \times T_{ON} \qquad (4)$$

The capacitor voltage will be restored with a average current given by:

$$I_C = \frac{\Delta V \times C}{T_{OFF}} = \frac{I_{LOAD} \times V_{OUT}}{V_{SS}} \qquad (5)$$

The total inductor current during the OFF time can be written as:

$$I_{INDUCTOR} = I_{LOAD} + I_C \qquad (6)$$

Inspecting *Figure 1*. We find:

$$I_C = \frac{\Delta I}{2} = \frac{V_{SS} \times T_{ON}}{2 \times L} \qquad (7)$$

which yields:

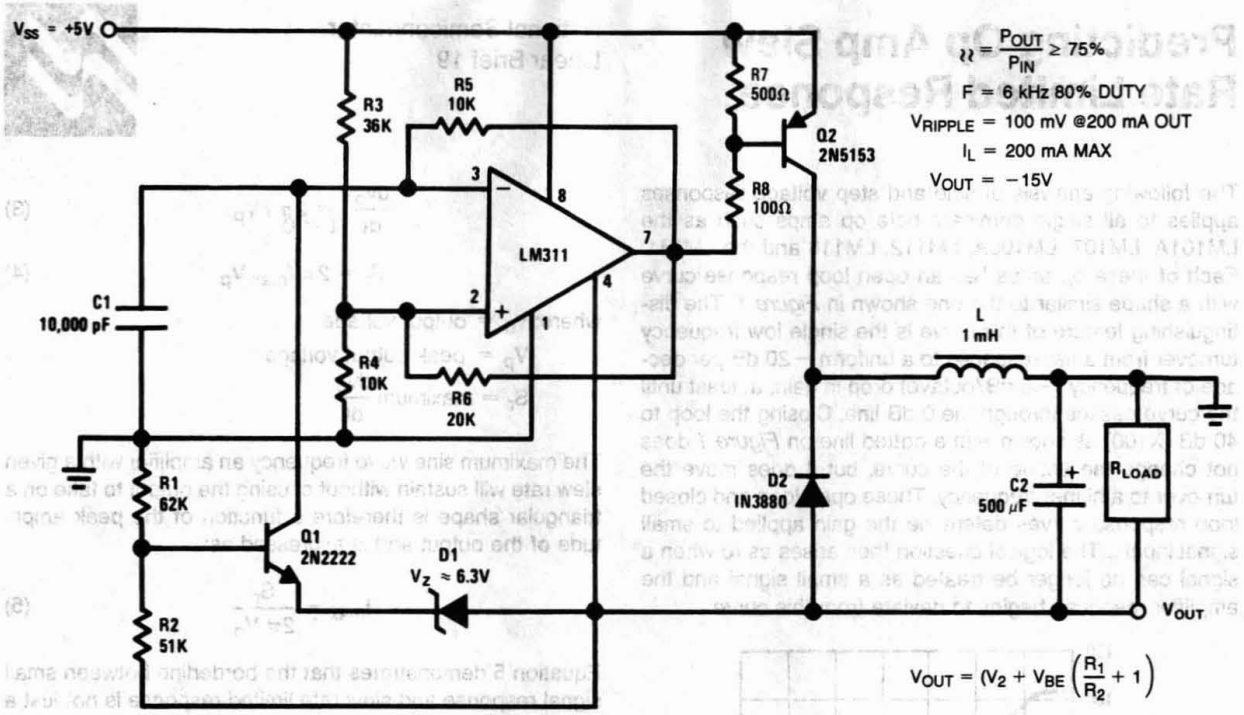
$$T_{ON} = \frac{2 \times L \times I_{LOAD} \times V_{OUT}}{V_{SS}^2} \qquad (8)$$

Taking into account that the efficiency is in the order of 75% the final expression is:

$$T_{ON} = \frac{1.5 \times L \times I_{LOAD} \times V_{OUT}}{V_{SS}^2} \qquad (9)$$

The above equations will be applied to the regulator shown at *Figure 2*. The regulator must deliver −15 volts at 200 mA from a +5 volt supply. Using a 1 mH inductor the T_{ON} time for Q_2 is 0.18 ms from equation 9. T_{OFF} is 60 μs from equation 4 and the oscillator frequency to:

$$F = \frac{1}{T_{ON} + T_{OFF}} \approx 4\ \text{kHz}$$



TL/H/8467–3

FIGURE 2. Switching Regulator for Voltage Conversion

The LM311 performs like a free running multivibrator with high duty cycle. The IC is designed to operate from a standard single 5 volt supply and has a high output current capability for driving the switching transistor Q_2. The duty cycle is given by the voltage divider R_3 and R_4 and the frequency of C_1 in conjunction with R_5.

By setting the duty cycle higher than first calculated, the output voltage will tend to increase above the desired output voltage of 15 volts. However, an extra loop performed by Q_1 and the zener diode in conjunction with the resistor network will modify the oscillator duty cycle until the desired output level is obtained.

The output voltage is given by:

$$V_{OUT} = \left(V_Z + V_{BE}\right)\left(\frac{R_1}{R_2} + 1\right)$$

Data and results obtained with the design:

V_{IN} = 5 volts
V_{OUT} = −15 volts
I_{OUT} = max 200 mA
Efficiency ≅ 75%
Frequency ≅ 6 kHz 80% duty cycle
V_{RIPPLE} ≅ 100 mV @ 200 mA load
Line regulation: V_{IN} = 5V to 10V < 3% V_{OUT}
I_{LOAD} = 200 mA
Load regulation: V_{IN} = 5V < 3% V_{OUT}
I_{LOAD} = 0 – 100 mA

Predicting Op Amp Slew Rate Limited Response

National Semiconductor
Linear Brief 19

The following analysis of sine and step voltage responses applies to all single dominant pole op amps such as the LM101A, LM107, LM108A, LM112, LM118 and the LM741. Each of these op amps has an open loop response curve with a shape similar to the one shown in *Figure 1*. The distinguishing feature of this curve is the single low frequency turnover from a flat response to a uniform −20 dB per decade of frequency (−6 dB/octave) drop in gain, at least until the curve passes through the 0 dB line. Closing the loop to 40 dB (X100) as shown with a dotted line on *Figure 1* does not change the shape of the curve, but it does move the turnover to a higher frequency. These open loop and closed loop response curves determine the gain applied to small signal inputs. The logical question then arises as to when a signal can no longer be treated as a small signal and the amplifier response begins to deviate from this curve.

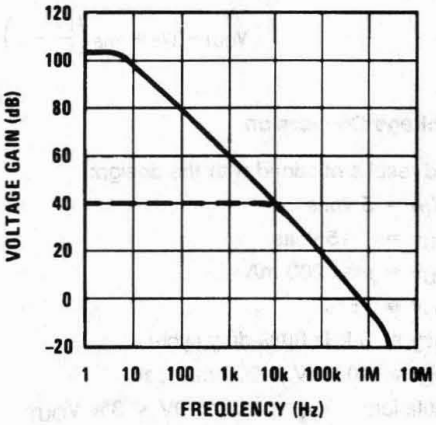


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FIGURE 1. Open and Closed Loop Frequency Response

The answer lies in the slew rate limit of the op amp. The slew rate limit is the maximum rate of change of the amplifier's output voltage and is due to the fact that the compensation capacitor inside the amplifier only has finite currents[1] available for charging and discharging. A sinusoidal output signal will cease being a small signal when its maximum rate of change equals the slew rate limit S_r of the amplifier. The maximum rate of change for a sine wave occurs at the zero crossing and may be derived as follows:

$$v_o = V_P \sin 2\pi ft \quad (1)$$

$$\frac{dv_o}{dt} = 2\pi f V_P \cos 2\pi ft \quad (2)$$

$$\left.\frac{dv_o}{dt}\right|_{t=0} = 2\pi f V_p \quad (3)$$

$$S_r = 2\pi f_{max} V_p \quad (4)$$

where: v_o = output voltage
V_p = peak output voltage
S_r = maximum $\frac{dv_o}{dt}$

The maximum sine wave frequency an amplifier with a given slew rate will sustain without causing the output to take on a triangular shape is therefore a function of the peak amplitude of the output and is expressed as:

$$f_{max} = \frac{S_r}{2\pi V_p} \quad (5)$$

Equation 5 demonstrates that the borderline between small signal response and slew rate limited response is not just a function of the peak output signal but that by trading off either frequency or peak amplitude one can continue to have a distortion free output. *Figure 2* shows a quick reference graphical presentation of equation 5 with the area above any V_{PEAK} line representing an undistorted small signal response and the area below a given V_{PEAK} line representing a distorted sine wave response due to slew rate limiting.

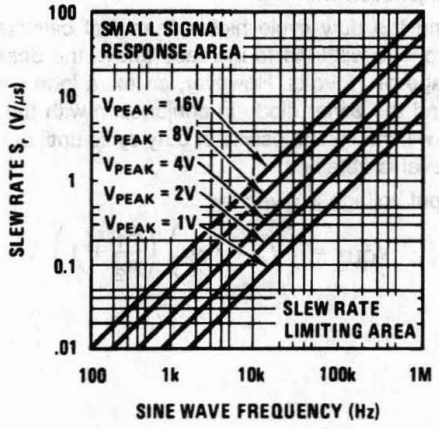

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FIGURE 2. Sine Wave Response

As a matter of convenience, amplifier manufacturers often give a "full-power bandwidth" or "large signal response" on their specification sheets.

This frequency can be derived by inserting the amplifier slew rate and peak rated output voltage into equation 5. The bandwidth from DC to the resulting f_{max} is the full-power bandwidth or "large signal response" of the amplifier. For example the full-power bandwidth of the LM741 with a 0.5V μs S_r is approximately 6 kHz while the full-power bandwidth of the LM118 with an S_r of 70 V/μs is approximately 900 kHz.

The step voltage response at the output of an op amp can also be divided into a small signal response and a slew rate limited response. The signal turnover and uniform −20 dB/decade slope shown in the small signal frequency response curve of *Figure 1* are also characteristic of a low pass filter and one can in fact model an op amp as a low pass RC filter followed by a very wideband amplifier. *Figure 3* shows a model of a X100 circuit with a 3 dB down rolloff frequency of

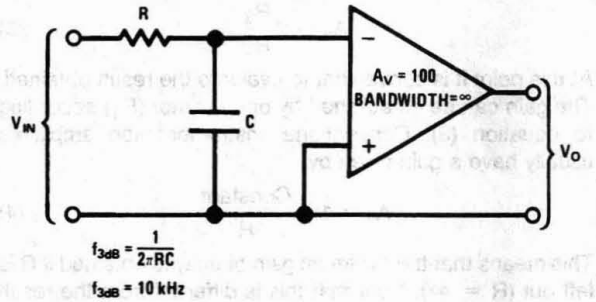

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FIGURE 3. Small Signal Op Amp Model

10 kHz. From basic filter theory[2] the 10% to 90% rise time of single pole low pass filter is:

$$t_r = \frac{0.35}{f_{3dB}} \quad (6)$$

which for this example would be 35 μs. Again this small signal or low pass filter response ceases when the required rate of change of the output voltage exceeds the slew rate limit S_r of the amplifier. Mathematically stated:

$$\frac{V_{STEP}}{t_r} \geq S_r \quad (7)$$

This means that as soon as the amplitude of the output step voltage divided by the rise time of the circuit exceeds the S_r of the amplifier, the amplifier will go into slew rate limiting. The output will then be a ramp function with a slope of S_r and a rise time equal to:

$$t'_r = \frac{V_{STEP}}{S_r} \quad (8)$$

Subsituting equation 6 into equation 7 gives the critical value of V_{STEP} directly in terms of f_{3dB}:

$$\frac{V_{STEP}\, f_{3db}}{0.35} \geq S_r \quad (9)$$

which can be graphed as shown in *Figure 4*. Any point in the area above a V_{STEP} line represents an undistorted low pass filter type response and any point in the area below a given V_{STEP} line represents a slew rate limited response.

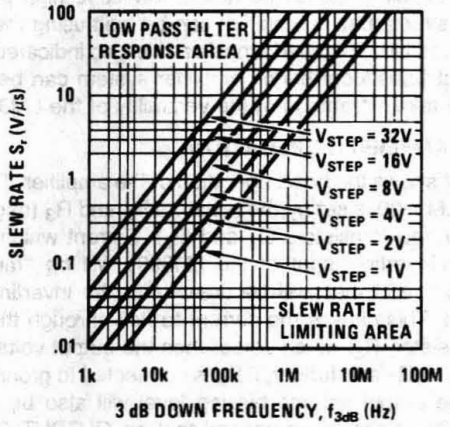

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FIGURE 4. Step Voltage Response

The above equations and graphs should allow one to avoid the pitfalls of slew rate limiting and also provide a means of using engineering tradeoffs to extend the response of the single dominant pole type of ampilfier.

REFERENCES

1. Solomon, J. E.; Davis, W. R.; and Lee, P. L.: *"A Self-Compensated Monolithic Operational Amplifier With Low Input Current and High Slew Rate"*, pp. 14–15, ISSCC Digest Tech. Papers, February 1969.
2. Millman, J. and Hawkias, C. C.: *"Electronic Devices and Circuits"*, pp. 465–466, McGraw-Hill Book Company, New York, 1967.

A Fully Differential Input Voltage Amplifier

National Semiconductor
Linear Brief 20

INTRODUCTION

The instrumentation amplifier is useful for amplifying small differential signals which may be riding on high common mode voltage levels. These amplifiers are particularly useful in amplifying signals in the milli-volt range which are supplied from a high impedance source (> 2 kΩ).

This brief will demonstrate how a low cost, high performance instrumentation amplifier can be built using the newly introduced LM3900 quad amplifier. It is also indicated how a compact transducer bridge amplifier system can be developed to take advantage of the versatility of the LM3900.

BASIC AMPLIFIER OPERATION

Figure 1 shows the basic operation of the amplifier. The bias of the LM3900 is set by the resistors R_2 and R_3 (neglecting for now, the transistors Q_1 and Q_2). Current which enters the non-inverting input of the LM3900 will be "mirrored" about V^- and then will be drawn into the inverting input terminal. This causes the current to flow through the feedback resistor, R_3, which establishes the output voltage level. If $R_2 = R_3$ and further, if R_2 is connected to ground (0V), then the output voltage biasing level will also be exactly zero volts. It should be noticed that an *OUTPUT OFFSET CONTROL* can be implemented by supplying a reference voltage, E_R, between R_2 and ground.

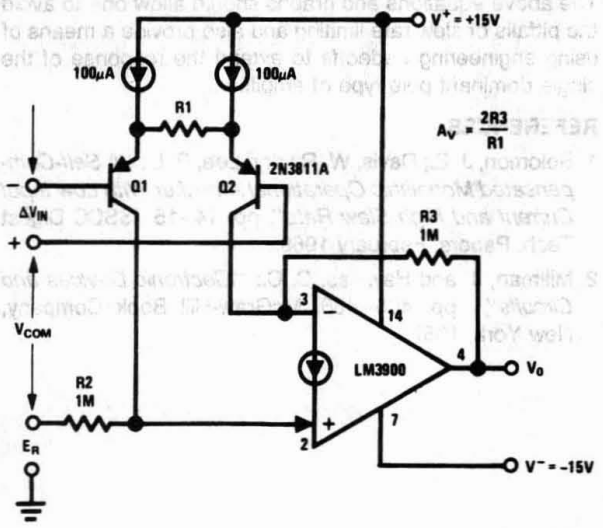

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FIGURE 1. Basic Instrumentation Amplifier

Adding transistors Q_1 and Q_2, as shown in *Figure 1* will not disturb this biasing if the two collector currents of the transistors are well matched for a 0V differential input signal. The current sources which bias Q_1 and Q_2, are chosen to be 100 μA each to guarantee high β and low offset voltage in Q_1 and Q_2.

The gain of the amplifier is calculated as follows:

Any differential input voltage, ΔV_{IN}, appears across R_1, and produces a current change ΔI, which is given by:

$$\Delta I = \frac{\Delta V_{IN}}{R_1} \quad (1)$$

This current change will show up in the collectors of Q_1 and Q_2 with opposite polarity. The input mirror of the LM3900 returns ΔI_{Q1} to the inverting input terminal where it is added (with sign) to ΔI_{Q2} yielding a total current change of 2ΔI. This current flows through the feedback resistor, R_3, which causes an output voltage change, ΔVo, which is given by:

$$\Delta Vo = 2\Delta I \times R_3 = 2 \times \frac{\Delta V_{IN}}{R_1} \times R_3 \quad (2)$$

to yield a gain,

$$A_v = 2\frac{R_3}{R_1} \quad (3)$$

At this point it is convenient to evaluate the result obtained. The gain can be established by one resistor (R_1) according to equation (3). Conventional instrumentation amplifiers usually have a gain given by:

$$A_v = 1 + \frac{\text{Constant}}{R} \quad (4)$$

This means that the minimum gain of unity is obtained if R is left out ($R = \infty$). Note that this is different from the result indicated in equation (3) where unity gain is obtained for

$$R_1 = 2R_3 \quad (5)$$

and minimum gain (or maximum attenuation) is obtained if R_1 is left out ($R_1 = \infty$). This suggests that the amplifier can be turned OFF without disturbing the output voltage dc bias.

The two current sources for Q_1 and Q_2 are implemented with a dual transistor (Q_3 and Q_4) in conjunction with an additional amplifier of the LM3900 as shown in *Figure 2*. The operation can be easily understood if R_4 and R_5 are incorporated within the amplifier, which then takes the form of a conventional opamp closed loop regulator which maintains a reference voltage (the drop across R_6) at the emitter of Q_4.

PERFORMANCE

The performance of the complete instrumentation amplifier of *Figure 2* is outlined below (Table I and *Figure 3*).

TABLE I. Typical Performance Characteristics

GAIN	
Range of gain	−34 dB ($R_1 = \infty$) to 72 dB ($R_1 = 0$)
Gain is set according to:	$A_v = \frac{2R_3}{R_1}$
INPUT	
Voltage offset referred to input is adjustable to zero.	Pos supply less 2.4V
Common-mode and differential input voltage	Neg supply less 300 mV
Common-mode rejection ratio at 10 Hz	115dB (gain of 1000)
Bias current (either input)	200 nA
OUTPUT	
Output offset is adjustable to zero.	12 mV_{rms} (open loop)
Output noise	3 mV_{rms} (A_{CL} = 66 dB)
FREQUENCY RESPONSE	
Small signal frequency response (−3 dB)	1 MHz (gain of 1000) 3 MHz (gain of 1)

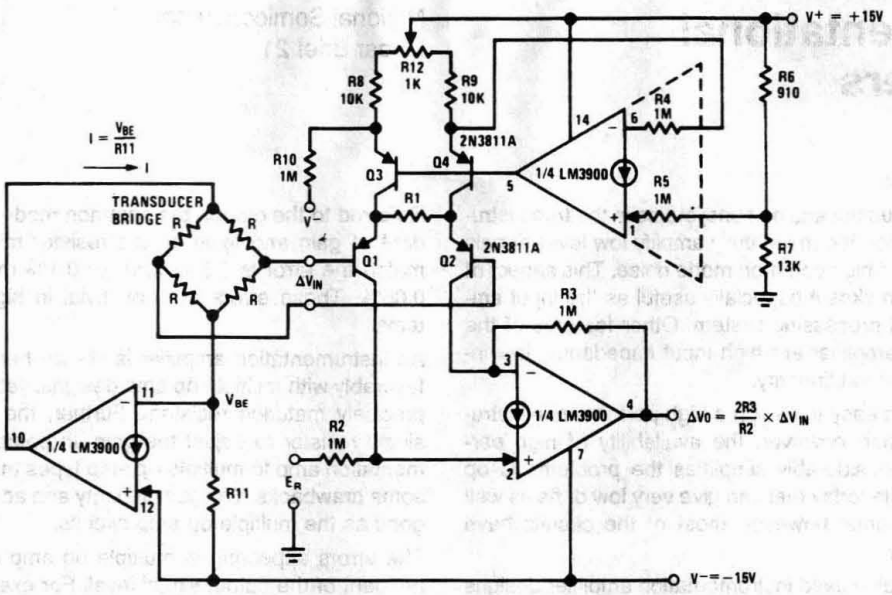

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FIGURE 2. Bridge Amplifier

Since quantitative discussion of the sources of offset voltage is beyond the scope of this brief, only the procedure for nulling the amplifier will be included.

Letting R_1 go to zero causes the amplifier to operate in the open-loop mode. The main offset voltage source is now the V_{BE} mismatch of Q_1 and Q_2. The output can be nulled by the *OUTPUT OFFSET CONTROL* (the reference voltage for R_2) or by adjusting the value of R_2. With $R_1 = \infty$, the main offset voltage source is the mismatch in the collector currents of Q_3 and Q_4. This is easily adjusted via R_{12}. These first and second adjustments interact, however, after repeating the procedure a couple of times a good result is obtained.

TRANSDUCER BIAS SOURCE

Having in mind that the LM3900 consists of four independent amplifiers makes it relatively easy to bias a transducer bridge with a constant current source using only one more of the amplifiers and one resistor. The technique is self-explanatory and is also shown in *Figure 2*.

CONCLUSION

A brief review of a new concept for an instrumentation amplifier has been presented. Many applications can be derived from this basic connection which require amplifying the low level differential signals which are obtained from sensors such as strain gages, pressure transducers, and thermocouples. The performance of this instrumentation amplifier is adequate for many system applications. (See National Semiconductor Application Note 72, "The LM3900 — A New Current-Differencing Quad of ± Input Amplifiers" for further information.)

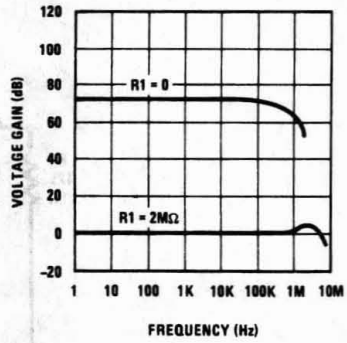

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FIGURE 3. Frequency Response

LB-21

Instrumentational Amplifiers

National Semiconductor
Linear Brief 21

INTRODUCTION

One of the most useful analog subsystems is the true instrumentation amplifier. It can faithfully amplify low level signals in the presence of high common mode noise. This aspect of its performance makes it especially useful as the input amplifier of a signal processing system. Other features of the instrumentation amplifier are high input impedance, low input current, and good linearity.

It has never been easy to design a high performance instrumentation amplifier; however, the availability of high performance IC's considerably simplifies the problem. IC op amps are available today that can give very low drifts as well as low bias currents; however, most of the circuits have some drawbacks.

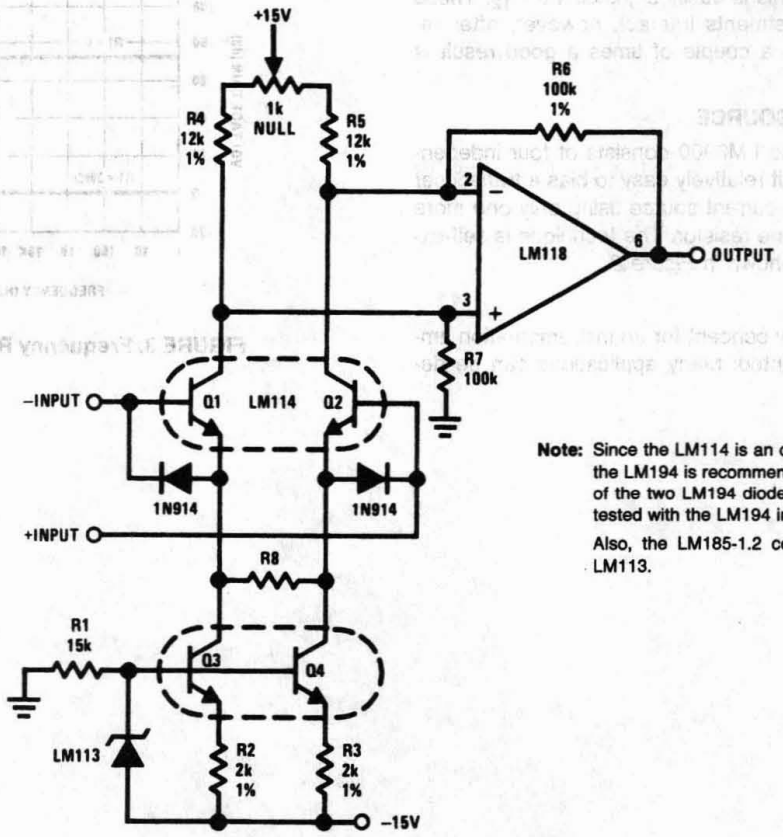
The most commonly used instrumentation amplifier designs utilize either 2 or 3 op amps and several precision resistors. These are capable of excellent performance; however, for high performance they require very precisely matched resistors. The common mode rejection of these designs depends on resistor matching and overall gain. Since op amps are now available with exceedingly high CMRR, this is no longer a problem. The CMRR of the instrumentation amplifier is approximately equal to half resistor mismatch plus the gain. For a 1% resistor mismatch the CMRR is limited to 46 dB plus the gain—referred to the input.

Referred to the output, the common mode error is independent of gain and fixed by the resistor mismatch. For 1% match the error is 0.5%, and for 0.1% match the error is 0.05%. These errors are not trivial in high precision systems.

An instrumentation amplifier is shown here that compares favorably with multiple op amp designs, yet does not require precisely matched resistors. Further, the design allows a single resistor to adjust the gain. In comparing this instrumentation amp to multiple op amp types there are of course some drawbacks. The gain linearity and accuracy are not as good as the multiple op amp circuits.

The errors appearing in multiple op amp circuits are independent of the output signal level. For example, a common mode error at the output of 0.5% of full scale is a 33% error if the desired output signal is only 1.5% of full scale. With the new circuit maximum errors at full scale output and the percentage of output error decreases at lower output levels.

Figure 1 shows a general purpose instrumentation amplifier optimized for wide bandwidth. It can provide gains from under 1 to over 1000 with a single resistor adjustment. Gain linearity is worst for unity-gain at 0.4%, and gain stability is better than 1.5% from −55°C to +125°C. Typically over a 0°C to +70°C range gain stability is 0.2%. Common mode rejection ratio is about 100 dB—independent of gain.



Note: Since the LM114 is an obsolete part, substitution of the LM194 is recommended, along with the removal of the two LM194 diodes. This circuit has not been tested with the LM194 included.

Also, the LM185-1.2 could be substituted for the LM113.

TL/H/8727–1

FIGURE 1. Instrumentation Amplifier

Transistor pair, Q1 and Q2, are operated open-loop as the input stage to give a floating, fully differential input. Current sources, Q3 and Q4, set the operating current of the input pair. To obtain good linearity the output current of Q3 and Q4 are set at about twice the current in R8 at full differential voltage. The temperature sensitivity of the transconductance of Q1 and Q2 is compensated by making their operating current directly proportional to absolute temperature. It has been shown that by biasing the base of transistor current sources at 1.22V, the output current varies as absolute temperature. The LM113 diode provides a constant 1.22V to the current sources. Both the compensated gm of Q1 and Q2 and the large degeneration from R8 give the amplifier stable gain over a wide temperature range.

In operation, transistors Q1 and Q2 convert a differential input voltage to a differential output current at their collectors. This is fed into a standard differential amplifier to obtain a single ended output voltage. Since the diff amp does not see the common mode input voltage, 1% resistors are adequate. Gain is set by the ratio of R8 (plus the r_e of Q1 and Q2) to the sum of R6 and R7.

As mentioned previously this circuit is optimized for wide bandwidth: however, it is easily modified for other applications. If low bias current is needed, all resistors can be increased by a factor of 100 and an LM108 substituted for the LM318. Other possible improvements are cascaded current sources and a modified Darlington input stage.

Low Drift Amplifiers

National Semiconductor
Linear Brief 22

INTRODUCTION

Since the introduction of the monolithic IC amplifier, there has been a continued improvement in DC accuracy. Bias currents have been decreased by five orders of magnitude over the past five years. Low offset voltage drift is also necessary in high-accuracy circuits. This is evidenced by the popularity of low-drift amplifier types as well as requests for selected low-drift op amps. However, little has been written about the problems associated with handling microvolt signals with a minimum of errors.

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted. In many cases, the low drift of the op amp is completely swamped by external effects while the amplifier is blamed for the high drift.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Whenever dissimilar metals are joined, a thermocouple results. The voltage generated by the thermocouple is proportional to the temperature difference between the junction and the measurement end of the metal. This voltage can range between essentially zero and hundreds of microvolts per degree, depending on the metals used. In any system using integrated circuits, a minimum of three metals are found: copper, solder, and kovar (lead material of the IC).

Nominally, most parts of the circuit are at the same temperature. However, a small temperature gradient can exist across even a few inches—and this is a big problem with the low level signals. Only a few degrees gradient can cause hundreds of microvolts of error. Two places where this shows up, generally, are the package-to-printed-circuit-board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

For example, a very low drift amplifier was constructed and the output monitored over a 1-minute period. During the one minute it appeared to have input referred offset variations of $\pm 5.0\ \mu V$. Shielding the circuit from air currents reduced this to $\pm 0.5\ \mu V$. The 10 μV error was due to thermal gradients across the circuit from air currents.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film, and some metal-film resistors can cause large thermocouple errors. Wirewound resistors of evenohm or managanin are best since they only generate about 2.0 $\mu V/°C$ referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low-drift stage electrically and thermally yields good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature, a gain error will result. For example, a gain-of-1000 amplifier with a constant 10 mV input will have 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50 μV error. Most precision resistors use different material for different ranges of resistor values. It is not unexpected that a resistor differing by a factor of 1000 does not track perfectly with temperature. For best results, ensure that the gain fixing resistors are of the same material or have tracking temperature coefficients.

It is appropriate to mention offset balancing as this can have a large effect on drift. Theoretically, the drift of a transistor differential amplifier depends on the offset voltage. For every millivolt of offset voltage the drift is 3.6 $\mu V/°C$. Therefore, if the offset is nulled, the drift should be zero. When working with IC op amps, this is not the case. Other effects, such as second stage drift and internal resistor TC, make the drift nontheoretical.

Certain types of amplifiers are optimized to have lower drift with offset balancing such as the LM121 and LM725. With this type of device offset, nulling improves the drift, and offset nulling should be used. Other types of devices, such as selected LM741's or LM308's, are selected for the drift without offset nulling connected to the device. The addition of a balancing network changes the internal currents and thus changes the drift—probably for the worse—so any offset balancing should be done at the input.

No matter which null network is applied, highly stable resistors must be used. They should have low TC and track. Wirewound pots are usually a good choice. Finally, when the null network reduces a drift, the balancing of the amplifier as close to zero offset as possible minimizes the drift.

Testing low-drift amplifiers is also difficult. Standard drift testing techniques such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method do not work. Thermal gradients can cause much greater errors than the amplifier drift. Coupling microvolt signal through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test, along with the gain setting resistor, should be isothermal. The circuit in *Figure 1* will yield good results if well constructed.

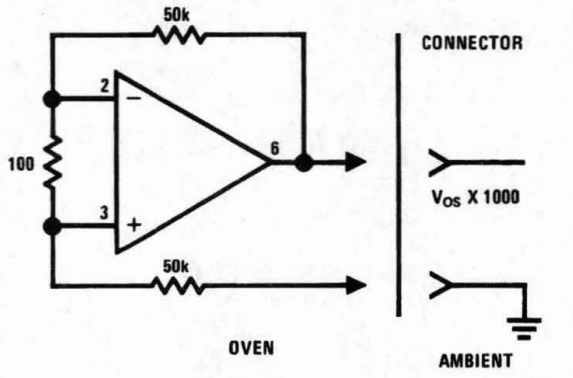


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FIGURE 1. Drift Measurement Circuit

CONCLUSION

Low-drift amplifiers need extreme care to achieve reproducable low drift. Thermal and electrical shielding minimize thermocouple effects. Resistor choice is also important as they can introduce large errors. Careful attention to circuit layout offset balancing circuitry is also necessary.

Precise Tri-Wave Generation

National Semiconductor
Linear Brief 23

INTRODUCTION

The simple Tri-wave generator has become an often used analog circuit. Tri-wave oscillators are more easily designed, require less circuitry, and are more easily stabilized than sine wave oscillators. Further, the highly linear output of todays Tri-wave generators make them useful in many "sweep" circuits and test equipment.

This article describes a triangle wave generator with an easily controlled peak-to-peak amplitude. The positive and negative peak amplitude is controllable to an accuracy of about ±0.01V by a DC input. Also, the output frequency and symmetry are easily adjustable.

CIRCUIT DESCRIPTION

The Tri-wave oscillator consists of an integrator and two comparators—one comparator sets the positive peak and the other the negative peak of the Tri-wave. To understand the operation, assume that the output of the comparator is low (−5V). Then −5.0V is applied through R1 to the input of the integrator. The LM118 will integrate positive until its output is equal to the positive reference on pin 9 of the LM119. Since the comparator outputs are low, D1 is reverse biased and the full output of the integrator is applied to the non-inverting input of comparator A. As the integrator output crosses the positive reference, comparator A switches "plus" and latches "plus" from positive feedback through D1 and R4. Now the polarity of the current to the integrator has changed and the integrator starts ramping negative. When the output reaches the negative reference voltage, comparator B swings negative. This forces the output of comparator A negative, also, and stops the positive feedback through D1 from holding the comparator's outputs positive. Once the positive feedback loop is broken, the outputs of the comparators stay low. With the comparator's outputs low, the integrator ramps positive again.

The frequency of operation is dependent upon R1, C1 and the reference voltages. Frequency is given by:

$$F = \frac{5.0V}{2R1\ C1\ (V_{REF}^{+} - V_{REF}^{-})}$$

The maximum frequency of operation is limited by the circuit delay to about 200 kHz. Also, the maximum difference in reference voltages is 5.0V.

APPLICATIONS

Regular or op amp testing is made easier with precise triangle waves. For example, IC voltage regulators are usually specified to operate over a certain input voltage range such as 7.0V to 25V. The Tri-wave generator can be set to deliver a 0.7V to 2.5V output. This output is then amplified by a factor of 10 by an op amp and used to sweep the regulator input over its operating range. With op amps, the generator can be used to sweep common mode voltages, power supply voltages, or even to test output swing. The output of the device can be displayed on an oscilloscope and performance monitored over the entire operating range.

Another application is a voltage controlled oscillator. Since the frequency depends on the input reference voltage, varying the reference varies the frequency. The useful VCO range is about 2 decades. The output is then taken from the comparators as the Tri-wave changes in amplitude.

Many sine wave oscillators use a non-linear network to convert triangle wave to sines. It is usually necessary to set triangle amplitude precisely for minimum distortion. If R1 is replaced by a pot, frequency can be varied over at least 10 to 1 range without affecting amplitude.

Symmetry is also easily adjustable. Current can be injected into the inverting input of the LM118 to change ramp time. The easiest way to achieve this is to connect a 50 kΩ resistor from the inverting input of the LM118 to the arm of a 1 kΩ pot. The ends of the pot are connected across the supplies. Current from the resistor either adds or subtracts from the current through R1, changing the ramp time.

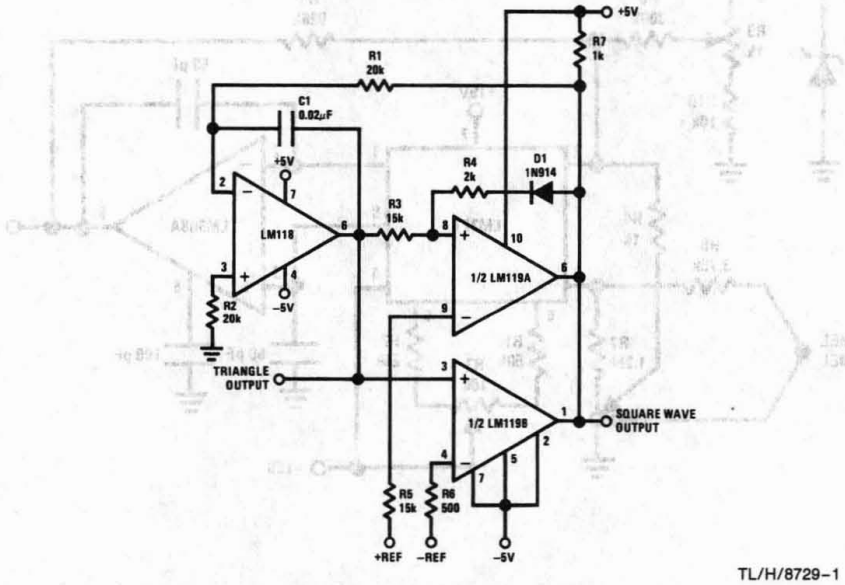

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FIGURE 1. Precision Tri-Wave Generator

Versatile IC Preamplifier Makes Thermocouple Amplifier with Cold Junction Compensation

National Semiconductor
Linear Brief 24

INTRODUCTION

Accurate electronic temperature measurements are not simple. There exists a large array of temperature sensors; each with its own peculiarities. The major sensors are thermistors, resistance sensors, and thermocouples. (Diodes and transistors have been used but they are not normally sold for this purpose.) Thermistors are highly non-linear, making wide range measurements difficult. Resistance sensors are large, require a bridge, and tend to be relatively costly. Thermocouples are small, relatively linear, inexpensive, but require reference junction temperature compensation.

Thermocouples are made when wires of different metals are joined. A voltage is produced proportional to the temperature *difference* between the junction and the output ends of the wire. This voltage is the Seebeck coefficient and is usually specified in volts (or microvolts) per degree. Depending on the material, it can range from nearly zero to volts—for some semiconductors. Commercially available thermocouples produce an output of between 10 μV/°C and 50 μV/°C.

Since the output voltage of thermocouples is proportional to temperature difference, the ambient temperature or measurement end of the thermocouple must be known. Alternatively, compensation can be applied for temperature changes. This is done either by terminating the thermocouple in a temperature controlled environment or with electrical compensation circuitry. The amplifier shown here provides a direct reading output of 10 mV/°C and automatically compensates for reference junction temperature changes. Further, calibration is relatively simple.

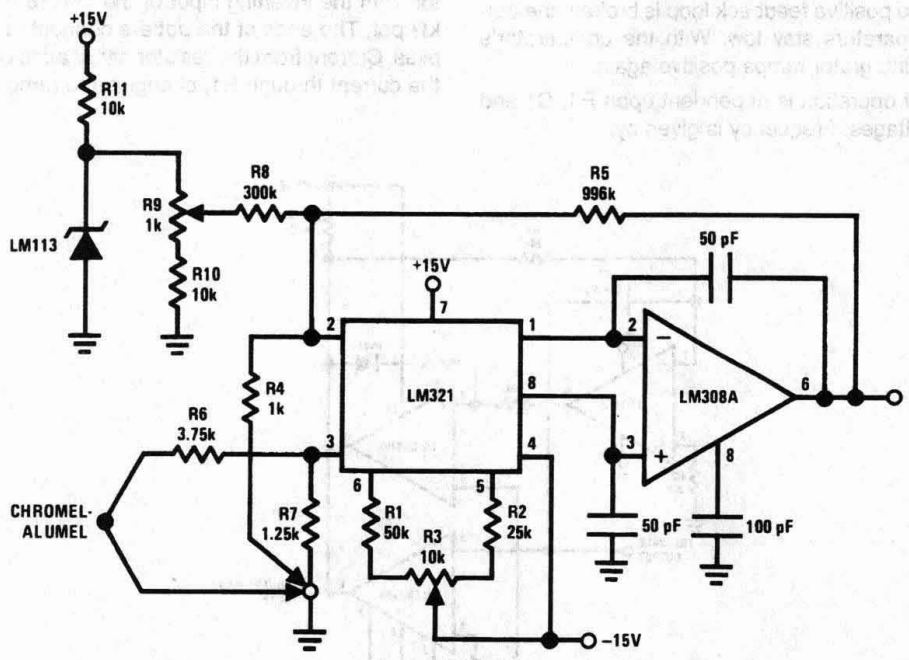
CIRCUIT DESCRIPTION

An LM321 preamp is used in conjunction with an LM308A op amp to form a precision, low-drift, operational amplifier. The LM321 is specifically designed for use with general purpose op amps to obtain drifts of 1 μV/°C. When the offset voltage is nulled, the drift is also nulled. There is a theoretical relationship between the offset voltage and drift when the offset is not nulled to zero. The drift of the amplifier is then used to compensate the thermocouple for ambient temperature variations. Drift given by:

$$\frac{d\,V_{OS}}{dT} = \frac{V_{OS}}{T}$$

where T is in degrees Kelvin.

Resistors R1, R2, and R3 set the operating current of the preamp, and R3 is used to adjust the offset. The offset and drift are amplified by the ratio of the feedback resistors R4 and R5 and appear at the output. R6 and R7 attenuate the thermocouple's output to 10 μV/°C to match the amplifier drift and set the scale factor at 10 mV/°C. The LM113 provides a temperature stable reference for offsetting the output to read directly in degrees centigrade.



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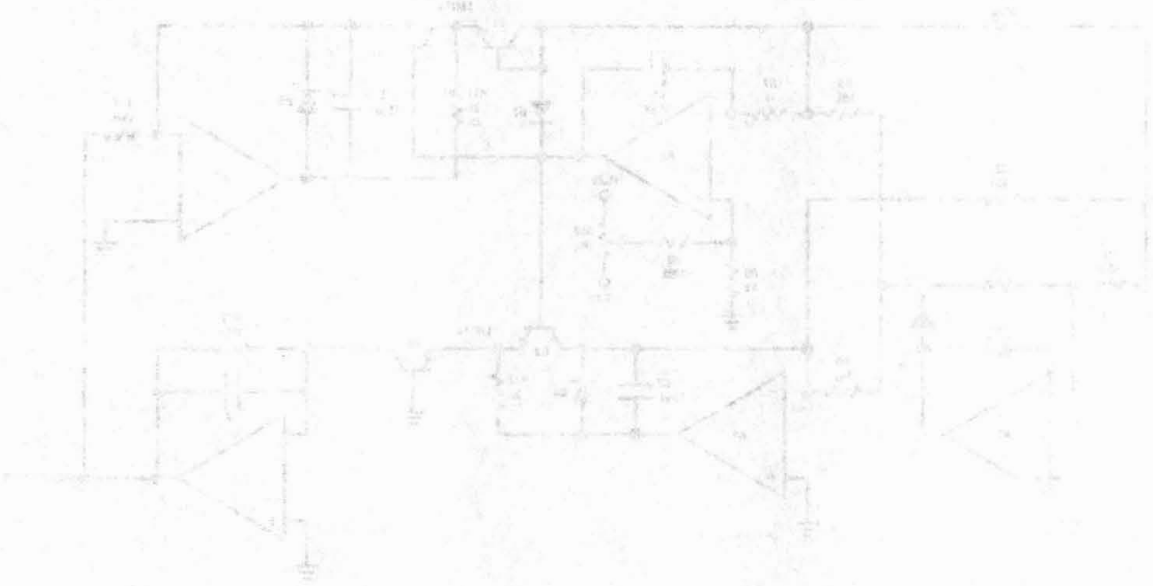
CALIBRATION

Calibration is independent of thermocouple type; however, circuit values are for chromel alumel. R6 and R7 must be changed for different thermocouples. First, the thermocouple is replaced by a short of copper wire and the LM113 is shorted to ground. Then the offset is adjusted so the output reads the ambient temperature at 10 mV/°k—for 25°C this is 2.98V. The short across the LM113 is removed and R9 is adjusted for the correct output in degrees centigrade. Connect the thermocouple, and it's ready to go.

PERFORMANCE

It should be mentioned that for stable performance, good construction techniques are necessary. Resistors R4, R6, and R7 should be wirewound so they contribute a minimum of error due to thermocouple effects from temperature gradients across the circuit. The entire circuit should be enclosed in a box with the end of the thermocouple terminated in the box near the LM321. This will minimize temperature gradients across the circuit and insure close thermal coupling between the LM321 and the reference end of the thermocouple.

Typically, the LM321 will track temperature changes with less then 0.03°C error per degree change. Self-heating of the LM321 will change its temperature by about 2°C; this is calibrated out initially. Reference and resistor drift can be expected to contribute about 0.02°C/°C. Of course, no compensation is made for nonlinearities of the thermocouple output voltage as a function of temperature. Over a wide measurement range with relatively stable ambient temperature, thermocouple error will be the major inaccuracy.



True rms Detector

National Semiconductor
Linear Brief 25

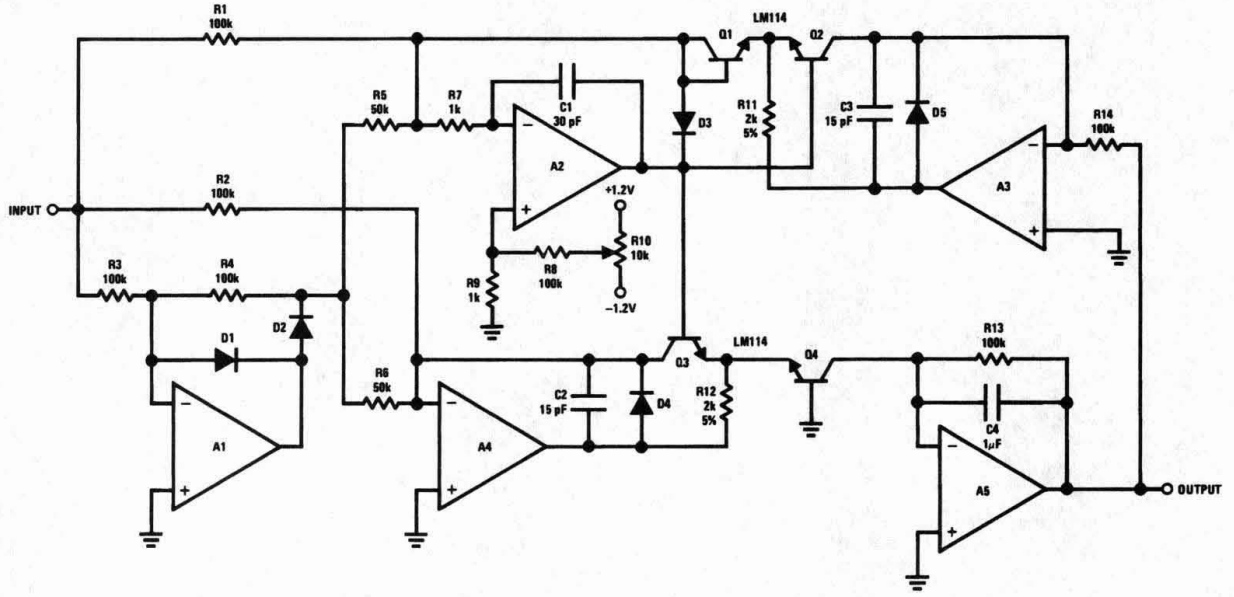
INTRODUCTION

The op amp precision rectifier circuits have greatly eased the problems of AC to DC conversion. It is possible to measure millivolt AC signal with a DC meter with better than 1% accuracy. Inaccuracy due to diode turn-on and nonlinearity is eliminated, and precise rectification of low level signals is obtained.

Once the signal is rectified, it is normally filtered to obtain a smooth DC output. The output is proportional to the average value of the AC input signal, rather than the root mean square. With known input waveforms such as a sine, triangle, or square; this is adequate since there is a known proportionality between rms and average values. However, when the waveform is complex or unknown, a direct readout of the rms value is desirable.

The circuit shown will provide a DC output equal to the rms value of the input. Accuracy is typically 2% for a 20 V_{p-p} input signal from 50 Hz to 100 kHz, although it's usable to about 500 kHz. The lower frequency is limited by the size of the filter capacitor. Further, since the input is DC coupled, it can provide the true rms equivalent of a DC and AC signal.

Basically, the circuit is a precision absolute value circuit connected to a one-quadrant multiplier/divider. Amplifier A1 is the absolute value amplifier and provides a positive input current to amplifiers A2 and A4 independent of signal polarity. If the input signal is positive, A1's output is clamped at −0.6V, D2 is reverse biased, and no signal flows through R5 and R6. Positive signal current flows through R1 and R2 into the summing junctions of A2 and A4. When the input is negative, an inverted signal appears at the output of A1 (output is taken from D2). This is summed through R5 and R6 with the input signal from R1 and R2. Twice the current flows through R5 and R6 and the net input to A2 and A4 is positive.



TL/H/8474–1

Note 1: All operational amplifiers are LM118.

Note 2: All resistors are 1% unless otherwise specified.

Note 3: All diodes are 1N914.

Note 4: Supply voltage ±15V.

Amplifiers A2 through A5 with transistors Q1 through Q4 form a log multiplier/divider. Since the currents into the op amps are negligible, all the input currents flow through the logging transistors. Assuming the transistors to be matched, the V_{be} of Q4 is:

$$V_{be}\,(Q4) = V_{be}\,(Q1) + V_{be}\,(Q3) - V_{be}\,(Q2)$$

The V_{be}'s of these transistors are logarithmically proportional to their collector currents so

$$\log\,(I_{C4}) = \log\,(I_{C1}) + \log\,(I_{C3}) - \log\,(I_{C2})$$

$$\text{or } I_{C4} = \frac{I_{C1}I_{C3}}{I_{C2}}$$

where I_{C1}, I_{C2}, I_{C3}, and I_{C4} are the collector currents of transistors Q1–Q4.

Since I_{C1} equal I_{C3} and is proportional to the input, the square of the input signal is generated. The square of the input appears as the collector current of Q4. Averaging is done by C4, giving a mean square output. The filtered output of Q4 is fed back to Q2 to perform continuous division where the divisor is proportional to the output signal for a true root mean square output.

Due to mismatches in transistors, it is necessary to calibrate the circuit. This is accomplished by feeding a small offset into amplifier A2. A 10V DC input signal is applied, and R10 is adjusted for a 10V DC output. The adjustment of R10 changes the gain of the multiplier by adding or subtracting voltage from the log voltages generated by the transistors. Therefore, both the resistor inaccuracies and V_{be} mismatches are corrected.

For best results, transistors Q1 through Q4 should be matched, have high beta, and be at the same temperature. Since dual transistors are common, good results can be obtained if Q1, Q2 and Q3, Q4 are paired. They should be mounted in close proximity or on a common heat sink, if possible. As a final note, it is necessary to bypass all op amps with 0.1 μF disc capacitors.

Specifying Selected Op Amps and Comparators

National Semiconductor
Linear Brief 26

It is not infrequent that commercially available standard IC components do not fit a particular application as they are specified. Often, however, a standard device selected to tighter limits will work. Thereupon, the IC manufacturer may be requested to supply a specially tested device.

The usual chain of events for a selected part is as follows: A specification is sent to the manufacturer with a request for quote. It is evaluated at the manufacturer for feasibility, yield, and testing requirements. Then price and delivery are quoted to the customer. (Sometimes this route is shortened by calling the manufacturer—but this does not always work.)

Some insight into the IC design and IC testing can help both the manufacturer and IC user with special selection. Proper specification helps the manufacturer test as well as reduce IC costs. Ambiguous or impossible specs will usually result in the return of the specification to the customer for clarification and delay the delivery of the required parts.

The manufacturer is usually familiar with the product and production spread of devices. Further, test equipment is available for measuring parameters specified by the data sheet. In general, tighting selected data sheet parameters causes no problems. Further, no additional test equipment is needed for these tests—only the limits need be changed.

Perhaps one of the largest problems is over-specification. Each tightened specification reduces the number of parts available to the specification. For example, tightening several specifications at once could result in a 1% or 0.1% yield; to supply 100 parts at this yield, between 10,000 and 100,000 parts might have to be tested, and that gets expensive.

Of course, spec limits cannot be tightened to any desired value. This is due to limitations on the IC design. For example, bias current, which depends on transistor H_{fe}; can not be tightened by a factor of 10. This would require beta's 10 times higher than normal. Also, some specifications are not independent, such as op amp bandwidth and slew-rate.

OP AMP AND COMPARATORS

These are the two most popular linear IC components requiring selection. Since many of the same specifications apply to both types of devices, they will be covered together. Table I shows the most common parameters tested on these devices and the relative difficulty of testing on high speed equipment.

Selected offset voltage and drift are very commonly specified parameters. Offset voltage and drift depends on component matching. In general, drift is not usually tested on general purpose devices; although, it may be guaranteed. Offset voltage can be correlated to drift, and the offset limits are set to guarantee the standard drift specification. Of course, very low drift devices must be 100% tested for drift, making them relatively expensive. Drift testing requires measuring the offset voltage at three or more temperatures; then subtracting and dividing by the temperature change to obtain the drift—a long and tedious measurement.

In some cases tightened offset voltage specifications over the operating temperature range offer the same performance as a drift tested device, but are less expensive. This is because offset voltage measurement can be a go/no-go measurement. For example, 15 μV/°C can be guaranteed over a 100°C range by limiting the maximum offset voltage to $\pm$0.75 mV or a 1.5 mV band. If the application has an error budget of $\pm$ "X" volts, it may be better to tighten the offset voltage rather than have the manufacturer to drift test. Drift testing a comparator is virtually impossible since they are not designed to operate closed loop.

Other parameters dependent upon matching are: offset current, common mode rejection, and supply rejections. These can be greatly tightened at the expense of yield.

Bias current, supply current, gain, slew rate, and response time are dependent upon both device design and processing. The limits for tighter parameters on these specifications are more restrictive. Table II gives reasonable special selection limits. This is only a guideline and, of course, depends on the device.

Noise testing is in a class by itself. Op amp noise will vary between manufacturers of the same device. Further, noise will vary between different types of devices from the same manufacturer. Since noise on a particular device is mostly process dependent, it will be relatively consistant from a single IC producer.

Noise can be broken into two categories: white noise, and popcorn noise. Both of these noise sources can be either voltage or current noise. It is possible with advanced processing to make IC transistors as good as the best discrete low noise transistors. With good processing only a very small percentage of op amps will have any popcorn noise.

Noise measurements are time consuming and costly. Popcorn noise testing may take as much as 30 seconds per unit which limits production to about 100 devices per hour. This low production rate will increase costs. If not absolutely necessary—do not specify noise.

As a final note, some mention should be made of other special testing. Anything reasonable can be done; however, it should be kept in mind that accurate specification in terms of the IC parameters is necessary. It is unlikely a positive result will come from a specification showing a system schematic, system output, and stating "select devices to produce desired outputs." Although this is an exaggeration, it points out the type of specification to be avoided. Performance specification should apply to the IC not to a circuit using the IC. Many manufacturers have circuits available showing the various electrical tests and the way they are done.

TABLE I. Relative Ease of Parameter Testing

Parameter	Op Amp	Comparator	Cost
Offset Voltage	Easy	Easy	Low
Offset Current	Easy	Easy	Low
Bias Current	Easy	Easy	Low
Supply Current	Easy	Easy	Low
Common Mode/Supply Rejection	Easy	Easy	Low
Gain	Moderate	Moderate	Low
Input Resistance	Guaranteed by Bias Current Measurement	Guaranteed by Bias Current Measurement	Not Tested
Slew Rate	Moderate	Moderate	Relatively Low
Bandwidth/Response Time	Difficult	Difficult	Moderate
Offset Voltage Drift	Very Difficult	Very Difficult	High
Offset Current Drift	Very Difficult	Very Difficult	High

TABLE II. Guideline to Tightened Specifications

Parameters	Limit	Comments
Offset Voltage	0.1 mV	Matching
Offset Current	−50% of Nominal	Matching
Bias Current	−50% of Nominal	Depends on H_{fe}
Supply Current	−25% of Nominal	Depends on Various Process Parameters
Gain	+100% of Nominal	Set by Design
Common Mode/Supply Rejection	+200% of Nominal	Matching
Slew Rate	+30% of Nominal	Set by Design
Bandwidth	+30% of Nominal	Set by Design
Response Time	−30% of Nominal	Set by Design and Processing
Offset Voltage Drift	0.2 μV/°C to 5 μV/°C	Lower Limit May Not Apply to Many Op Amps
Offset Current Drift	Guarantee by Offset Current Limit	

Micropower Thermometer

National Semiconductor
Linear Brief 27

The introduction of a monolithic temperature transducer for the −55°C to +125°C temperature range can considerably simplify the problems encountered in temperature measurement. The three most common sensors—thermistors, resistance sensors, and thermocouples—require a reasonable amount of circuitry for use. Thermistors are highly nonlinear, resistance sensors and thermistors require a stable excitation voltage, and thermocouples have low output. Further, none of these sensors provide an output directly calibrated in a known temperature scale.

The new monolithic temperature transducer provides an output directly proportional to absolute temperature at 10 mV/°K. The chip includes a temperature stable voltage reference and op amp. These allow the output to be offset and scaled to provide any desired temperature scale factor and zero output temperature.

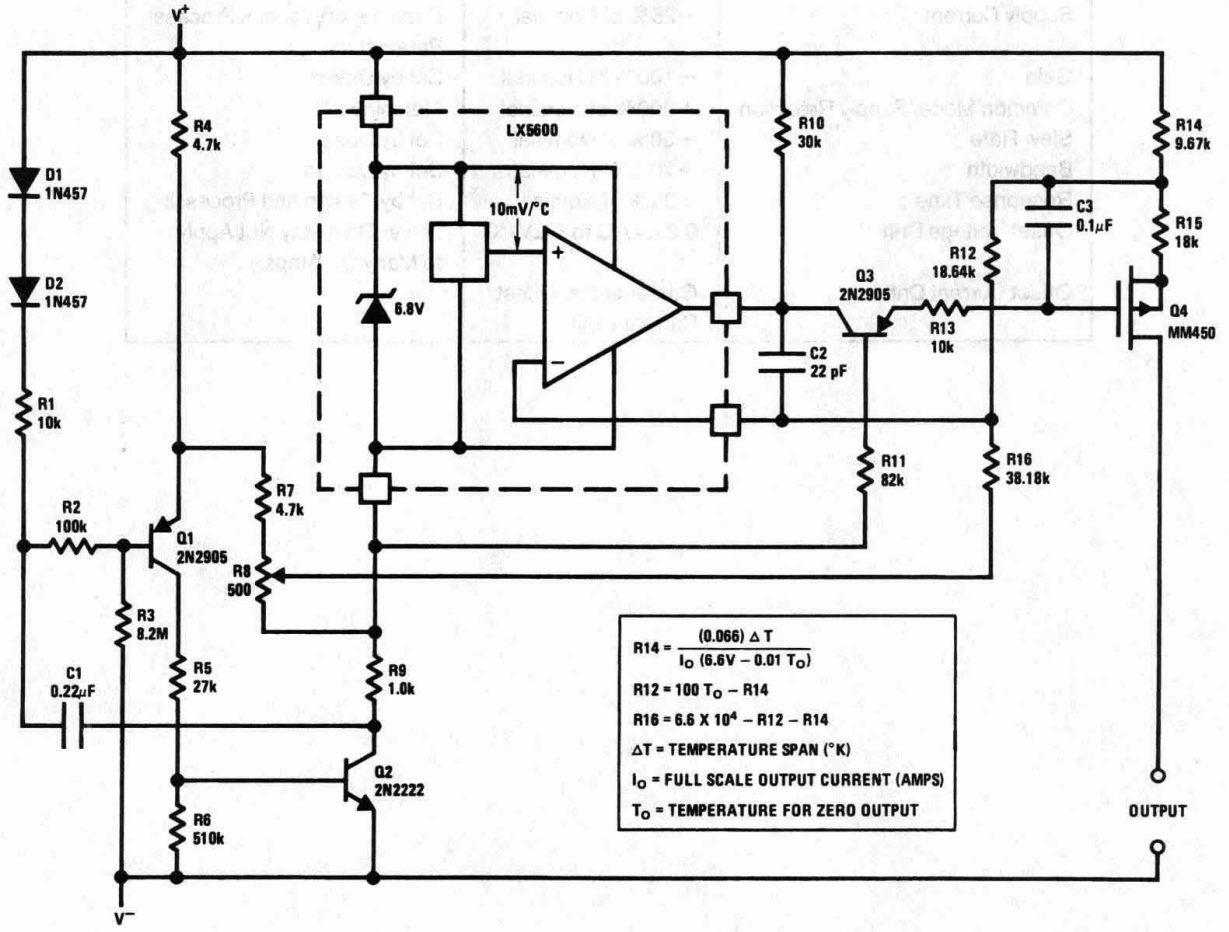
THERMOMETER DESIGN

The circuit shown will provide a temperature sensitive output with both zero and scale factor independently selectable. Since the temperature transducer requires about 1.0 mA for normal operation, the thermometer is pulsed at a low duty cycle to reduce power consumption. A continuous output is obtained between pulses by a sample and hold. Since temperature does not usually change rapidly, the pulsed operation of the thermometer does not detract from its usefulness.

With the components shown, duty cycle is about 0.2% with a one second sample rate. This gives an average current drain of about 25 μA plus the output current. It is designed to operate over a supply voltage of 8.0V to 12V with good results. A small 8.4V mercury battery can give an operational life in excess of one year.

The output of the thermometer is a current proportional to temperature which can be used to drive a meter for a direct readout. Alternatively, a resistor or op amp can be used to obtain a voltage output.

A complementary astable multivibrator, made of Q1 and Q2, drives the LX5600 through R9. The timing is set by several



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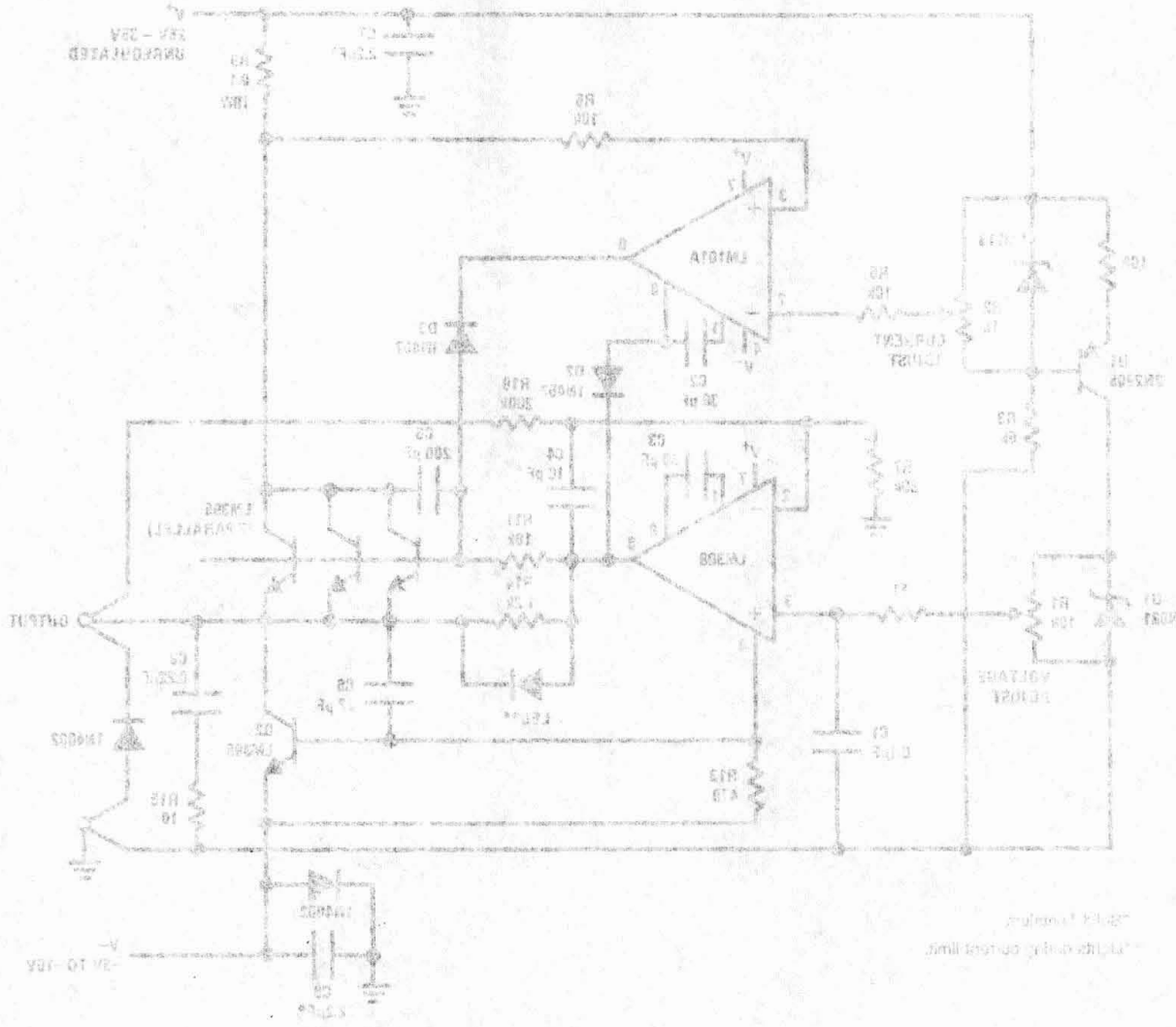
Micropower Thermometer Circuit Diagram

components. C1 and R3 control the off-time and C1, R1, R4 and R7 control the on-time. R9 sets the operating current of the transducer to 1.0 mA at the lowest supply voltage.

When the transducer is "on," sample transistor Q3 is also on. The output of the op amp drives the sample capacitor, C3, and MOSFET, Q4. Feedback is obtained from R12, R14 and R16 which set both the zero and scale factor of the thermometer. When the transducer is turned off, a continuous output is provided by C3 and Q4. Resistor R15 decreases the circuit's sensitivity to MOSFET gm, allowing almost any MOSFET to be used. About 2.0V should be dropped across R15 at full scale output. R8 is used to trim the thermometer, correcting for zener tolerance, temperature error in the sensor and resistor tolerance. With the values shown, a 0 to 50 μA output is obtained for a +50°F to +100°F temperature change. Other ranges can be selected by using the formulas shown in the box on the circuit diagram.

The low power consumption makes this thermometer especially attractive for battery operated equipment. Further, the current source output allows long lines to be driven with no loss of accuracy. Finally, the circuit is easy to set up for almost any desired temperature range.



General Purpose Power Supply

National Semiconductor
Linear Brief 28

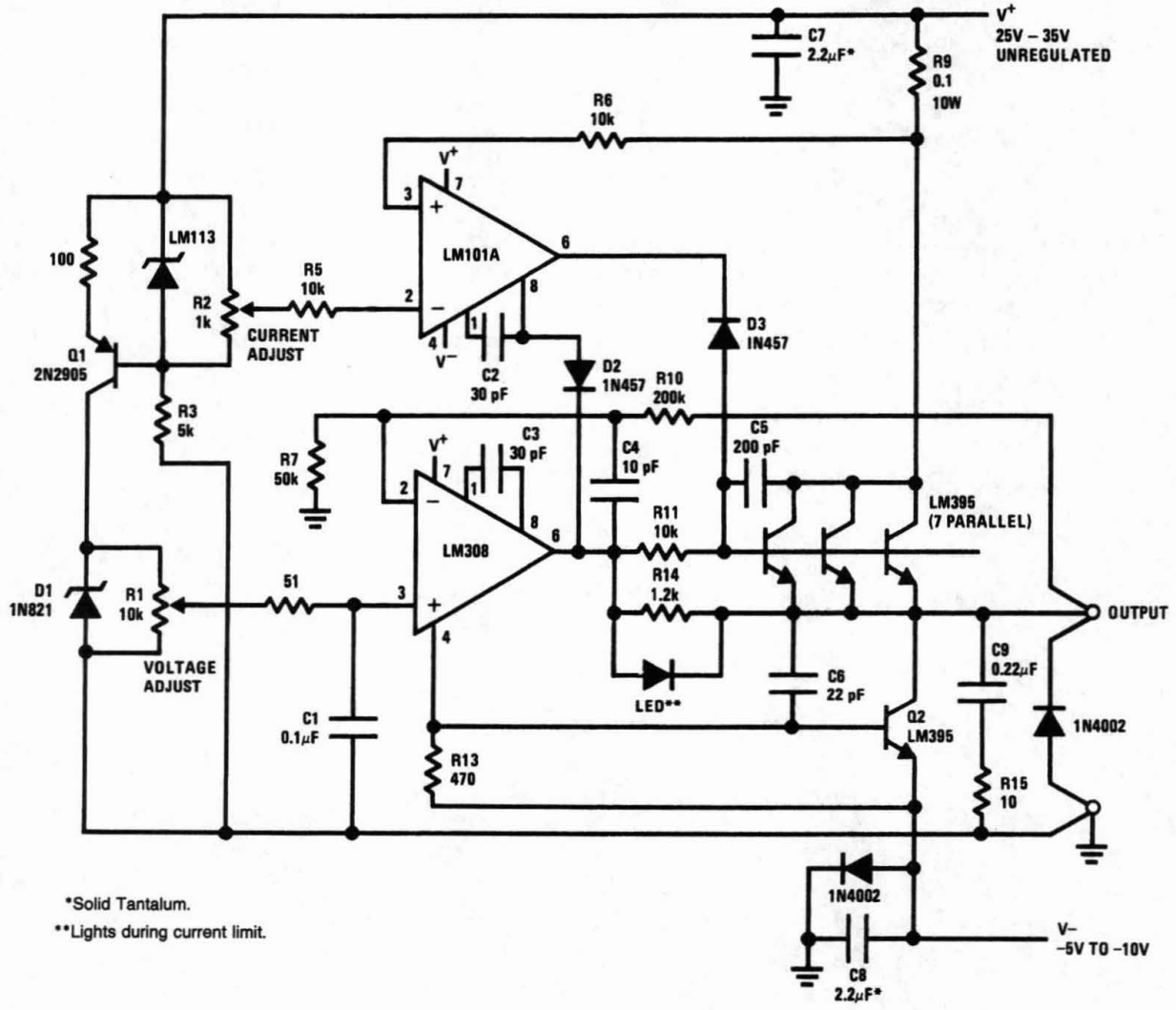
INTRODUCTION

A general purpose lab type constant voltage/constant current power supply is easily made using standard integrated circuits. The circuit shown will provide up to 25V at up to 10A output with both the output voltage and current adjustable down to zero. Although relatively simple, very high performance is obtained.

Lab supplies must withstand considerable abuse. Good control of maximum output current is mandatory both to protect the supply and the powered circuitry. One of the shortcomings of many commercial supplies is the use of a large output capacitor to help frequency compensate the regulator loop. This output capacitor can discharge many times the peak output current of the supply into the load as well as degrade the ac output impedance when the supply is used as a constant current source. (Of course, the output capacitor helps keep the ac output impedance low when the supply is used as a constant voltage source.) The circuit shown has good response both as a constant voltage or constant current source.

The use of the LM395 monolithic power transistor as the pass element considerably simplifies the design power. The LM395 acts as a 2A current limited, thermally limited, high gain power transistor. Since only a maximum of 10 μA is needed to drive the pass elements and complete overload protection is included on the chip, external biasing and protection circuitry is minimized. Only two control op amps are needed–one for voltage control and one for current control.

In constant voltage operation, a reference voltage is fed from voltage control pot, R1, through a high frequency filter into the non-inverting input of an LM308 op amp. The output of the LM308 drives seven paralleled LM395's as emitter followers to obtain a 10A capability.



*Solid Tantalum.

**Lights during current limit.

TL/H/8477–1

Feedback is taken through R10 directly from the output with the overall gain set at 5 by the ratio of R10 to R7. An additional LM395 is driven from the negative power supply lead of the LM308 to provide some output current sink capability (2A) so the supply can be quickly programmed even with large capacitive loads. Frequency compensation is achieved with C3 for the LM308 and C4 for the overall loop. Resistor R11, capacitors C5 and C6 and network R15–C9 suppress parasitic high frequency oscillations.

When the circuit is used in the constant current mode, the LM101A overcomes the constant voltage loop to control the output. Output current is sensed in R9 and compared with the voltage between V^+ and the arm of R2. R2 is connected across an LM113 low voltage reference diode to provide a 0V to 1.2V reference for 0A to 12A output. When the output current is below the set level, the LM101A output is positive, reverse biasing D3 and the LM308 control the outpput. When the current increases to the control point the output of the LM101A swings negative and decreases the drive to the output pass devices through D3, limiting the current. (Note that no separate positive supply is needed since the common mode operative range of the LM101A is equal to the positive supply.) Diode, D2, clamps the output of the LM101A when it is not regulating, decreasing the switchover time from voltage to current mode operation.

A few special precautions are needed in construction for proper operation. All LM395's should be mounted on the same heat sink to insure good current sharing. Also, a large heat sink is necessary since 300W will be dissipated under worst case conditions. Since the LM395's are high devices, the supply bypasses should be near the power transistors.

Microvolt Comparator

National Semiconductor
Linear Brief 32

INTRODUCTION

Comparison of dc signal levels within microvolts of each other can be made by using an LM121A pre-amp and an LM111 comparator IC. Implementing this with two separate IC's decreases noise, eliminates troublesome thermal effects, and achieves a maximum offset drift of 0.22 μV/°C *(Figure 1).*

Designing a practical comparator with a voltage gain of 10 million involves protecting the *input* stage from temperature changes or gradients, and avoiding problems of including the noise filter within the positive feedback loop. The circuit as shown has a 5 μV hysteresis which can be trimmed to 1 μV under certain conditions. Further, delays *decrease* with increasing overdrive (see chart) due to elimination of input stage thermal effects, saturating stages, and dielectric soak or polarization effects on signal filter capacitors (Table I).

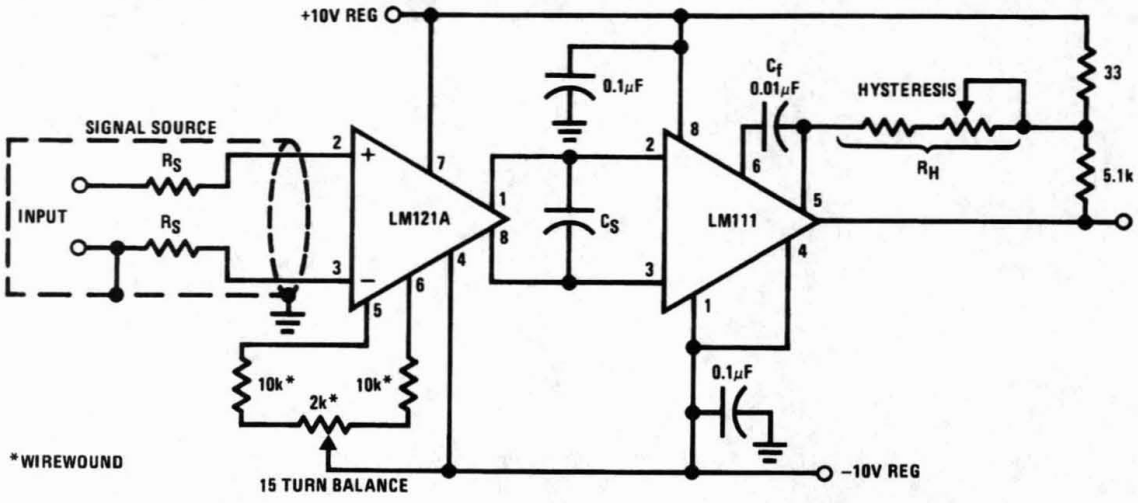
DESIGNING WITH A PRE-AMP

With the bias network shown, the LM121A input stage has an open-loop temperature stable voltage gain of close to 100. The 100k output impedance of the LM121A is shunted by C_S to filter out pickup and internally generated noise. No feedback to the inputs of the pre-amp is employed to avoid degrading common-mode rejection of the system.

The separate pre-amp with a gain of 100 provides two major advantages over single comparator designs. First, V_{OS} and other small errors attributed to the LM111 are reduced by the 100 gain factor. More important, temperature gradient changes which occur within the LM111 when switching any output load, are completely isolated by the separate packages and do not affect the pre-amp. If the entire microvolt comparator were on a single silicon chip, a temperature variation of as little as 1/1000°C across the input stage could have a significant effect.

TABLE 1. Typical Overdrive Delays

Hyst. Set	R_H	R_S	C_S	Delays with Various Overdrives			
				25%	100%	1000%	100 mV
5 μV	75 kΩ	10 kΩ Max.	6800 pF	2 ms	1.8 ms	600 μs	560 μs



TL/H/8733–1

FIGURE 1. Schematic Diagram

This effect is a major reason for designing circuits sensitive and stable to microvolt dc signals with a *separate* pre-amplifier. Further, the special 4-transistor input stage, when adjusted to zero offset with the "balance" control between pins 5 and 6, automatically reduces V_{OS} change with temperature to almost zero.

FILTERING

The pre-amp/comparator system generates a continuous stream of very fast pulses if assembled without a filter, even with positive feedback for hysteresis. This is caused by both stray output-input feedback, and noise. The noise is both thermal and pickup from the environment, including power switching transients and fluorescent light hash. To cure this, shunt filter capacitor C_S is used.

Placing this capacitor outside the positive feedback loop has two advantages. It eliminates a tendency for the comparator to oscillate during slow transitions. Also, response time to small signals is halved since the positive hysteresis feedback signal is not stored on the filter capacitor.

A higher frequency filter (C_f) is needed to provide a low impedance shunt to any high frequency noise and stray feedback that may be picked up between LM111 terminals 5 and 6. These two terminals have almost the same voltage sensitivity as the normal input terminals. The positive feedback to terminal 5, as described below, is only delayed slightly by this filter.

FEEDBACK

The positive feedback provided by the 5.1k/33Ω voltage divider with R_H is needed to insure clean, rapid changes of state. It is applied to one of the "balance" terminals (pin 5) of the LM111 to simplify the circuit over a balanced feedback network, and to minimize signal stored on C_S as previously described. The current fed back to terminal 5 is single ended with respect to the balance adjust network between these terminals, and hence injects a dc offset of the desired polarity and amplitude for a few microvolts of latching.

PERFORMANCE

A tabulation is shown for one of the many possible combinations of input circuits, filters, etc. For large amplitude signals, C_S can be decreased and hysteresis increased for greater speed. Conversely, to obtain hysteresis as low as 1 μV, trim R_H (to about 300k) use a C_S of 0.01 μF to 0.1 μF and have a low impedance source of signals.

For reduced ambient range and drift specifications, an LM321 can be paired with the LM311 for a cost saving while maintaining the same comparison sensitivity.

DESIGN TIPS FOR MICROVOLT SIGNALS

Even with high performance devices such as the LM121, microvolts of error can occur from thermocouple effects, common-mode signals, "microphonics," or unbalances in the input or nulling circuits. As pointed out in Application Note AN-79, Kovar lead to copper circuit board thermocouple effects can cause a 3.5 μV offset voltage for only 0.1°C difference across the input leads. A compact layout of input connections and shielding from air currents will minimize this problem.

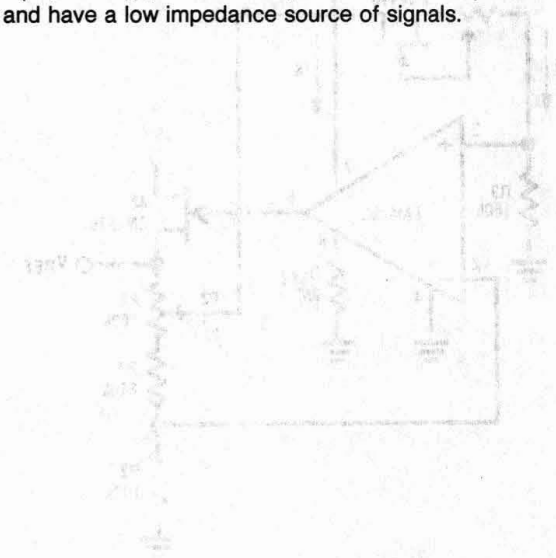
Although the LM121A has excellent common-mode rejection (> 120 dB), a 1V change in common-mode voltage can induce up to 1 μV of error voltage. For this reason common-mode voltage changes should be kept to a minimum. Also, common-mode voltages allow mechanical vibrations in the probe cable to induce "microphonic" noise signals. Short, stiff, low capacitance and symmetrical input shielded wires are recommended.

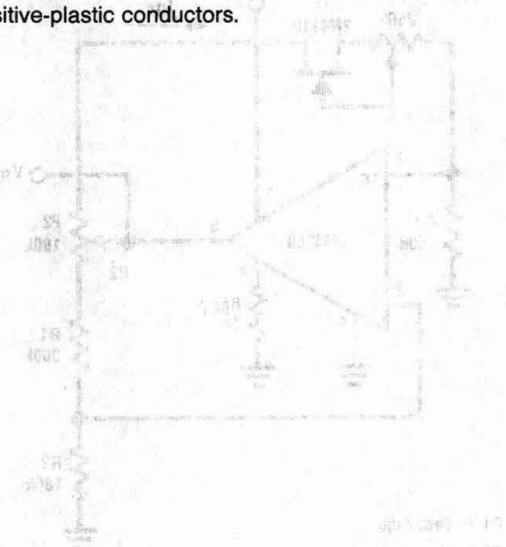
If it is possible to have a signal source balanced with regard to ground, it will help decrease errors due to bias currents, and noise due to common-mode and microphonic effects. Matched, low temperature coefficient parts should be used in the balance network, and care should be exercised in shielding input circuits and eliminating ground-loops.

APPLICATIONS

The microvolt comparator is particularly well suited to controllers or test equipment having thermocouples or strain gauges as inputs. This includes wind speed indicators, RMS to dc converters, vacuum gauges, gas analysis equipment, conductivity gauges, and hot wire controls. The strain gauges can be used in materials testing, electronic weighing, pressure transducers, and load limiting sensors for cranes, hoists, and rolling mills.

As a temperature controller, ⅛ degree or less on-off differential can be obtained using thermocouple types E, J, T or K. Other microvolt signals used for control may come from Hall effect sensors, Bolometers, slide-wires, and heat-flow thermopiles. A microvolt comparator will be useful in "Go/No-Go" testing of low resistances such as switch and relay contacts, RTDs, coil and fuse resistances, and pressure-sensitive-plastic conductors.





A Micropower Voltage Reference

National Semiconductor
Linear Brief 34

A low-drift voltage reference can be easily made by converting a zero temperature coefficient current to a voltage. JFETs biased slightly below pinch-off exhibit a zero temperature coefficient drain current (I_D) as shown in *Figure 1.* With the above property and a micropower operational amplifier, used to convert the drain current to a voltage, a low power consumption voltage reference can be built as shown in *Figure 2.* The consumption of LM4250 op amp is programmed through resistor R_{SET}. Potentiometer P1 should be adjusted for low output (V_{REF}) temperature coefficient. Actually, it can be trimmed for positive, negative or zero temperature coefficient. The output voltage is trimmed through P2 and it is expressed by:

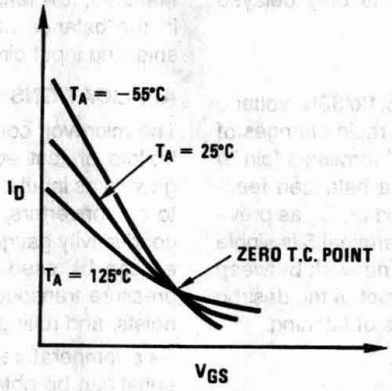
$$V_{REF} = I_{D1}(P2' + R1 + R2),$$

$$R2 = R3,\ I_{D1} \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

With the values shown in *Figure 2,* the temperature coefficient of the output is 0.002%/°C and the overall standby current less than 100 μA. The characteristics of the LM4250 are a function of its supply current, which depends on R_{SET}, and V^+. V^+ can be provided by V_{REF} through the addition of a second FET, J2, shown in *Figure 3.* This way the parameters of the op amp will be independent of the unregulated input. The reference voltage can be taken from the wiper of the potentiometer P2 ($V_{REF} = V^+$) or from the source of J2 ($V_{REF} > V^+$). In the first case, the output impedance of the circuit is quite high and buffering may be required according to the application. The output impedance in the second case is low, essentially the 1/gm of (J2) divided by the loop gain of the circuit. In this case, a small temperature coefficient due to the supply current of the LM4250 is going to be added and be compensated for by an additional trimming of P1. V_{REF} is computed by:

$$V_{REF} \cong I_{D1}[P2 + R1 + R2] + P2'[I_S + I_{D1}],$$

$$R2 = R3,\ I_S \cong \frac{6\,(V^+ - V_{BE})}{R_{SET}}$$



TL/H/8734–1

FIGURE 1. FET Transfer Characteristics

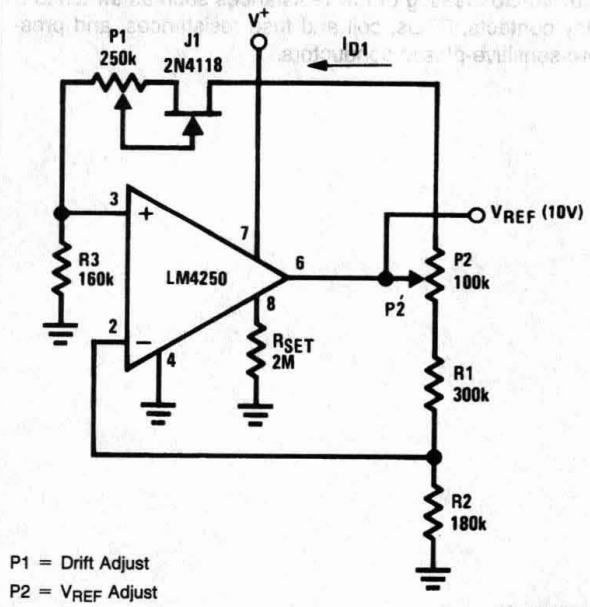


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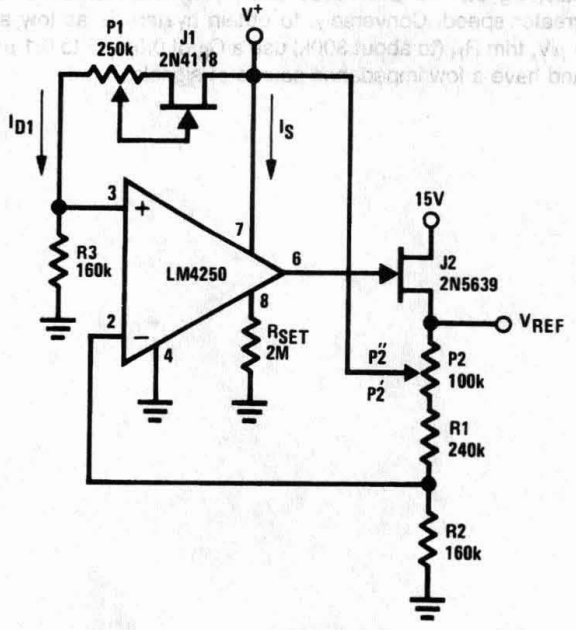
FIGURE 2. Basic Voltage Reference



TL/H/8734–3

FIGURE 3. Improved Voltage Reference

Adjustable 3-Terminal Regulator for Low-Cost Battery Charging Systems

National Semiconductor
Linear Brief 35

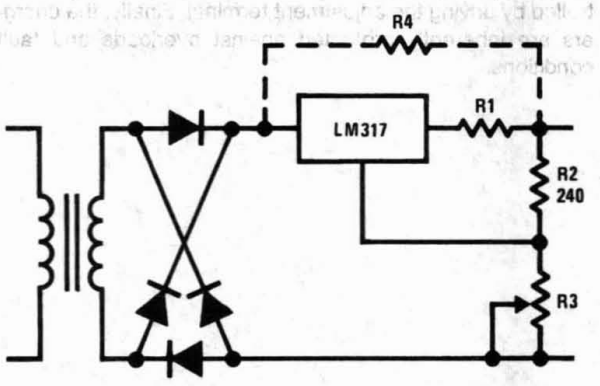
With the introduction of the LM317, a 3-terminal adjustable regulator, it becomes relatively easy to design high-performance, low-cost battery charging systems. Even single battery cells can be charged on this new regulator, which is adjustable down to 1.2V. The internal protection circuitry can be used to limit charging current as well as to protect against overloads. The output voltage is easily adjusted so multiple voltage chargers can be made.

The ability to accurately adjust the output voltage of the LM317 makes it especially attractive for constant voltage battery charging applications. Batteries are most quickly charged by "constant-voltage" charging circuits; however, close control of the charging voltage is necessary to prevent overcharging, especially with nickel cadmium cells. The internal protection circuitry of the LM317 is helpful in protecting against accidental overload conditions commonly occurring in charging systems.

INTERNAL CURRENT LIMIT

The peak charging current or output current is controlled by the internal current limit of the LM317. This current limit will work even if a battery is connected backwards to the output of the charger. Should a fault condition exist for an extended period of time, the thermal limiting circuitry will decrease the output current, protecting the regulator as well as the transformer. A constant voltage charger circuit is shown in *Figure 1*. The output voltage is set with resistors R2 and R3 and given by

$$V_{OUT} = 1.25\left(1 + \frac{R3}{R2}\right)$$



TL/H/8484–1

FIGURE 1. Constant Voltage Charging Circuit

Since, in low cost applications, no filter capacitors are used on the output of the rectifier, the battery is only charged on the peaks of the sine wave. This requires the peak output voltage from the transformer to be at least 50% greater than the battery voltage plus 3V. However, little cost premium should result since the average current from the transformer is lower than capacitive input filter circuits. Optional resistors R1 and R2 are used to further control the charging characteristics. Resistor R1 controls the output impedance of the charger allowing a "taper-charge" characteristic to be generated. The LM317 can also be used to limit the peak charging current to a partially charged battery at a value other than the regulator current limit. With R1 in the circuit, the output impedance is:

$$Z_{OUT} = R1\left(1 + \frac{R3}{R2}\right)$$

Including R1 in the feedback loop decreases the value of resistor needed for a particular output impedance reducing cost and power dissipation.

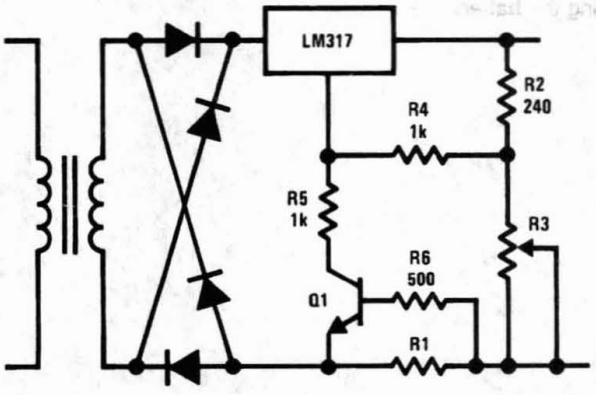
For example, with a 6V gelled electrolyte battery the regulator can be set to give a 6.9V output. Nominally, the battery is discharged to about 5V, making R1 0.4Ω output impedance and limiting the charging current to 0.5A at the start of charging rather than the internal current limit of the regulator. With a fully discharged battery or under short circuit conditions, the peak output current is still 2A for the LM317K with the resistor dissipating 1.6A as opposed to 8W if a 2Ω resistor were used directly in series with the battery.

Resistor R4 can be included to provide a low "topping-up" current for a charged battery.

This regulator configuration provides some other important features to the charger. If input power is removed and a fully charged battery is connected to the charger output, there is no damage. Under these conditions about 5 mA of current will be drawn by divider R2, R3. Since there is no ground connection to the LM317 regulator, very little current flows through the LM317. In this respect, the LM317 differs from other 3-terminal regulators, which can be damaged by applying power to the output terminal with the input open-circuited. If the battery is connected backwards, the LM317 will current limit and thermal limit normally, protecting the charger.

DECREASING CURRENT LIMIT

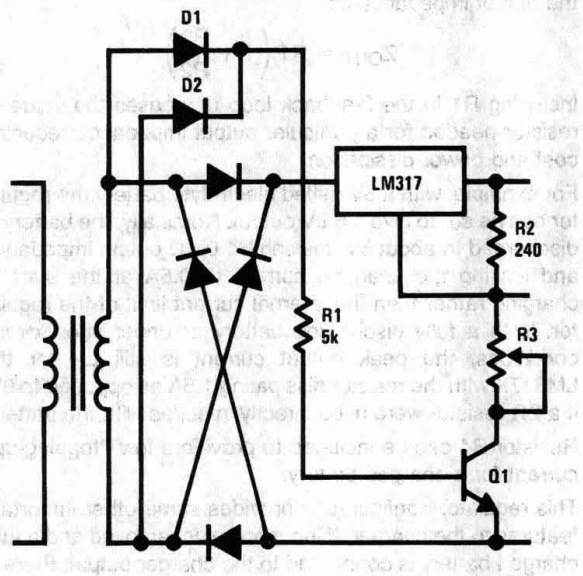
Adding a single NPN transistor can be used to decrease the current limit of the charge as shown in *Figure 2*.



TL/H/8484–2

FIGURE 2. Constant Voltage Charger with Peak Current Limiting

Resistor R1 senses the output current and turns on Q1 when I_{OUT} R1 equals about 0.6V. Transistor Q1 pulls the adjustment terminal negatively decreasing the output voltage and controlling the output current. A limitation of this circuit is that it does not work for direct short circuits. The output voltage must be above about 0.6V for the external current limiting to be active. The internal current limit of the LM317, of course, is still operative. This is not usually a problem since batteries charge to above 0.6V very quickly. Resistors R4, R5 and R6 protect the regulator and transistor for both direct short circuits or reverse battery connections.



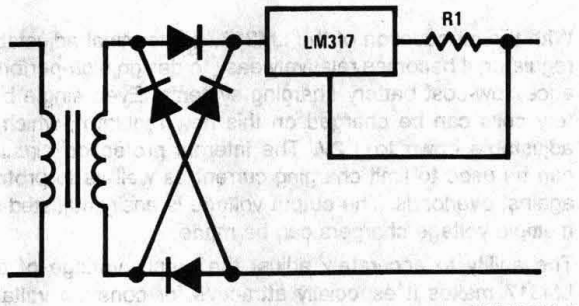
TL/H/8484–3

FIGURE 3. Charger with No Battery Loading when Power is "OFF"

As illustrated in *Figure 3*, in float or standby applications, it is desirable to remove all loading from the battery when input power is "OFF." When power is "ON," Q1 is saturated, grounding the voltage setting divider R2, R3 and the circuit works in a similar manner to the charger circuit in *Figure 1*. When power is "OFF," Q1 is open, eliminating any loading on the battery. A separate pair of low current diodes D1, D2 are necessary to bias Q1, rather than the power bridge rectifier. If R1 was tied to the output of the bridge, reverse current flow through the LM317 would keep Q1 "ON" and loading the battery.

A simple constant current charger for any type of battery is shown in *Figure 4*. A resistor R1 between the adjustment terminal and the output of the regulator sets the output current at:

$$I_{OUT} = \frac{1.25}{R1}$$



TL/H/8484–4

FIGURE 4. Constant Current Charger

Current can be set at anywhere between 10 mA and 1.5A by appropriate resistor choice. Current regulation is very tight at any current level since only 50 μA flows out of the adjustment terminal. This circuit is also immune to damage from shorts or reverse battery connections. The input voltage for regulation should also be about 1.5 times the battery voltage plus 3V.

UNIQUELY SUITED

The ability to adjust the output of the LM317 3-terminal regulator makes it uniquely suited for battery charging systems. Little has been included about charging specific types of batteries, since the characteristics of the charger should be matched to the battery. These charger circuits, although very simple, perform well. They are easily modified for voltage, current or even temperature coefficient by making the divider string temperature sensitive. More complex chargers can be made since the output of the LM317 is easily controlled by driving the adjustment terminal. Finally, the chargers are inherently protected against overloads and fault conditions.

Wide Range Timer

National Semiconductor
Linear Brief 38

One of the problems encountered in potentiometer controlled circuits is dynamic range. With a linear pot, about a 100:1 range is the limit. Although the pot resolution may be better than 1%, the angular displacement for good control becomes too small. Usually, range switching is then used.

A logarithmic control is a possible solution. With log controls, the resolution is the same anywhere within the operating range. For example, if 40° rotation is equal to a change from 10% to 100% of full scale, then 40° rotation is also equal to a change from 0.01% to 0.1% of full scale. It is easy to control a function over a 1,000,000:1 range with good control anywhere within the range.

The exponential relationship between the emitter-base voltage of a transistor and its collector current is well known. This relationship holds true within a few percent over extremely wide ranges. Using a transistor pair, and an op amp, it is easy to make a current source controllable over a 6 decade range.

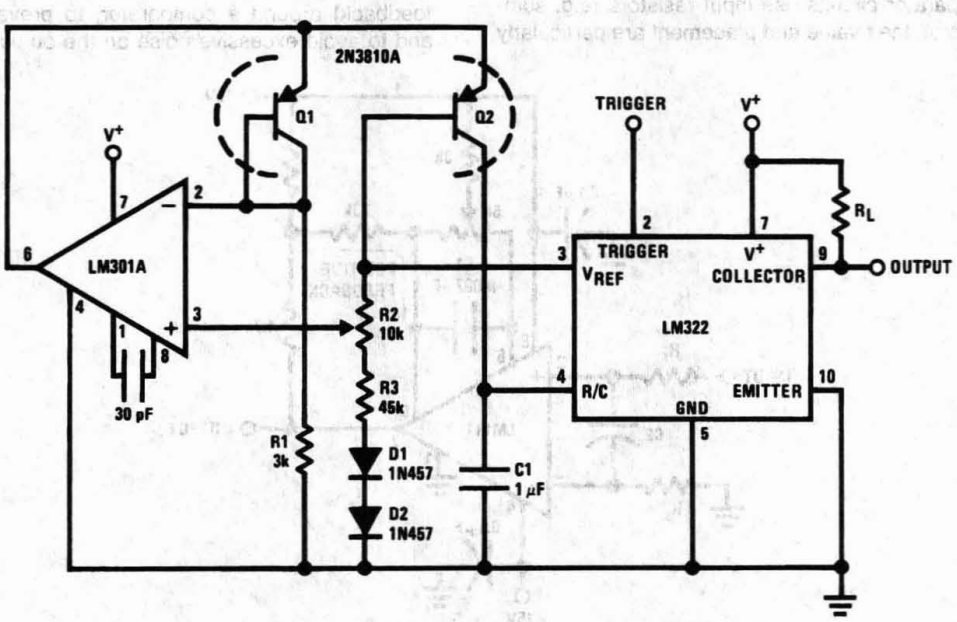
Figure 1 shows a timer which can be adjusted from 2 ms to 2000 seconds with a single control. An LM122 is used for the timing function in conjunction with a current source that is logarithmically controlled from a pot. The operation is as follows:

Transistors Q1 and Q2 are a matched PNP pair. Resistor R1 and the op amp set up a constant current of 1 mA through Q1 using the internal 3V reference from the timer. With R2 at the most positive end of its range, the non-inverting input of the op amp is a V_{REF}. This forces the emitter-base voltage of Q2 to equal Q1 and since the transistors are matched, the collector current of Q2 is also 1 mA. A time-out period of 2 ms results.

Rotating R2 subtracts the voltage between the arm of the pot and V_{REF} from the emitter-base voltage of Q2—lowering its collector current. The current is decreased by a factor of 10 for every 60 mV developed. A total of 360 mV is dropped across the pot, allowing a reduction in Q2 collector current by a factor of 1,000,000 or from 1 mA to 1 nA. A 1 nA charging current gives a 2000 second time out. (At maximum time, there is about a 30% error due to the 0.3 nA input current of the comparator). Finally, diodes D1 and D2 temperature compensate the voltage across the pot.

Calibrating the circuit is relatively easy (except for obtaining a log dial for the pot). Resistor R1 is adjusted for the minimum operating time removing for mismatch in the transistors, capacitor tolerance, and the offset of the op amp. R3 is used to calibrate the full scale time by adjusting the drop across R2 to 360 mV.

This type of log control is not limited to timers. If used in oscillator or function generator circuits, an ultra wide range VCO can be made. Also, in power supply circuitry, it is possible for a reguator to have as much resolution when adjusted for 0.001V output as when the output is 10V. Finally, a log current generator makes an easily adjusted low value current source without high value resistors.



TL/H/8487–1

FIGURE 1. 2 ms to 2000 Second Timer

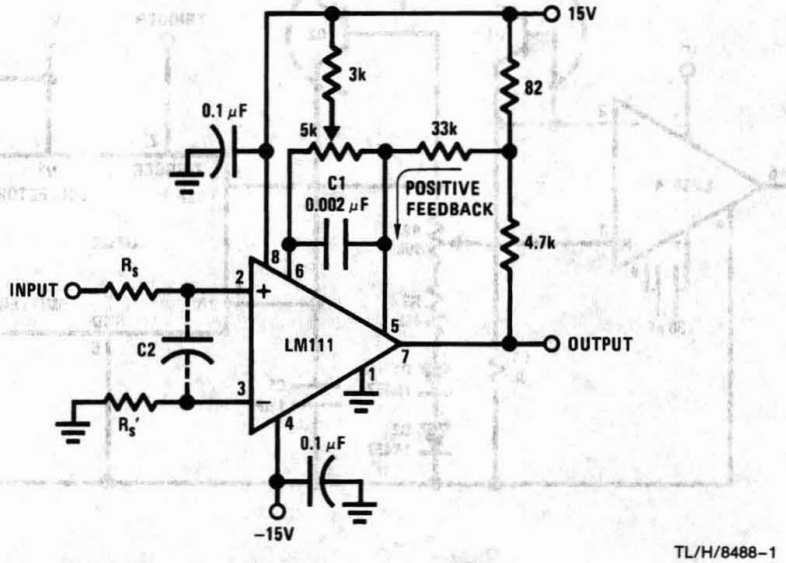
Circuit Techniques for Avoiding Oscillations in Comparator Applications

National Semiconductor
Linear Brief 39

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trimpot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.
4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the



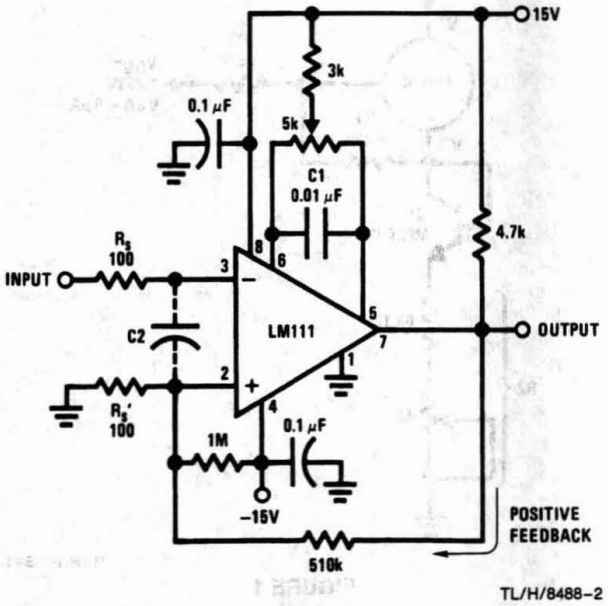
TL/H/8488–1

Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 1. Improved Positive Feedback

comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if the value of R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See paragraph 7, below, for the alternative.

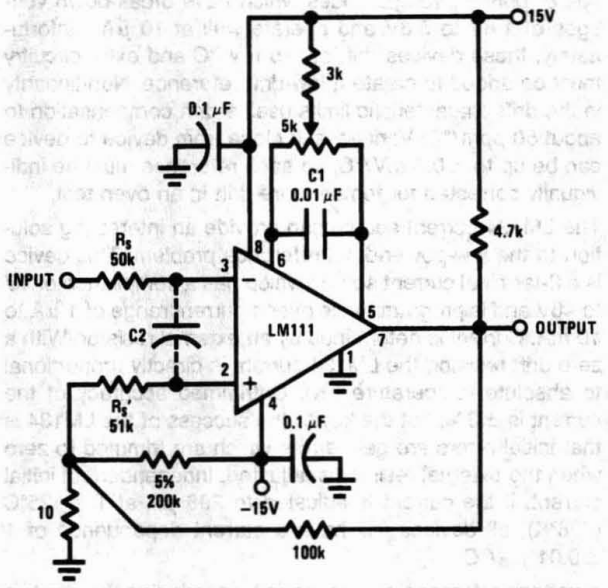
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and ensure sharp output transitions with input triangle waves from a few Hz to hundreds of kHz. The positive feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



TL/H/8488–2

Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 2. Conventional Positive Feedback



TL/H/8488–3

FIGURE 3. Positive Feedback with High Source Resistance

Precision Reference Uses Only Ten Microamperes

National Semiconductor
Linear Brief 41

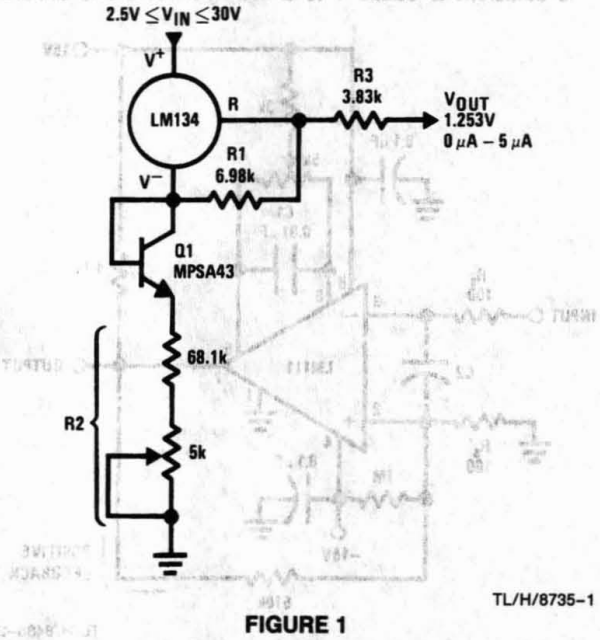
Increasing interest in battery-operated analog and digital circuitry in recent years has created the need for a micro-power voltage reference. In particular, the reference should draw 10 μA or less and operate from a single 5V supply. These requirements eliminate zener diodes which tend to have unpredictable temperature drift and are noisy at low currents and low voltages. One possibility is the LM103 series of punch-through diodes which have break-down voltages of 1.8V to 5.6V and operate well at 10 μA. Unfortunately, these devices drift at −5 mV/°C and extra circuitry must be added to create a low-drift reference. Non-linearity in the drift characteristic limits usable drift compensation to about 50 ppm/°C. Variations in slope from device to device can be up to ±0.5 mV/°C, so each reference must be individually corrected for temperature drift in an oven test.

The LM134 current source can provide an interesting solution to the low-power-drain reference problem. This device is a 3-terminal current source which has a compliance of 1V to 40V and is programmable over a current range of 1 μA to 10 mA. Current is determined by an external resistor. With a zero drift resistor, the LM134 current is directly proportional to absolute temperature (°K). Untrimmed accuracy of the current is ±3%, but the key to the success of the LM134 is that initial errors are gain errors which are trimmed to zero when the external resistor is adjusted. Independent of initial current, if the current is adjusted to 298 μA at T = 25°C (298°K), all devices will have a current dependence of 1 ±0.01 μA/°C.

A voltage reference can be made by combining the positive temperature coefficient of the LM134 with the negative TC of a forward-biased diode. The IC terminology for such a reference is "bandgap reference" because the total voltage of the reference is equal to the extrapolated (0°K) bandgap voltage of silicon. An important characteristic of bandgap references is that the zero TC voltage is independent of diode current even though the diode voltage and TC are not. This means that by adjusting the total voltage of the reference to a fixed value, T.C. will be adjusted to near zero at the same time. The zero TC voltage for most bandgap references falls between 1.20V and 1.28V.

The circuit in *Figure 1* is a micropower reference using the LM134 and an MPSA43 transistor connected as a diode with collector-base shorted. A transistor is used in place of a diode because the transistor characteristics as a double-diffused structure are more consistent than a diode. In particular, the emitter-biased voltage drift of wide-base high-voltage transistors connected as diodes is very linear with temperature.

In *Figure 1*, the LM134 controls the voltage between its R and V^- terminals to ≈ 64 mV. About 5.5% of the current out of the R terminal flows out of the V^- terminal. The total current flowing through R2 is then determined by 67.7 mV/R1. Output voltage is the sum of the diode voltage, plus the voltage across R2, plus 64 mV. The voltage TC across R2 and the 64 mV is positive and directly proportional to absolute temperature while the diode TC is negative. The overall TC of the output will be near zero (< 50 ppm/°C) when the output is adjusted to 1.253V by trimming R2. To obtain this level of performance, R1 and R2 must track well over temperature. 1% metal film resistors are suggested.



TL/H/8735–1

FIGURE 1

For optimum results with a single point adjustment of voltage and temperature coefficient, an additional error term must be accounted for. Internal to the LM134 are low I_{dss} FETs used for starting the control loop. This FET current adds directly to the V^- pin current and therefore creates an additional output voltage equal to $(I_{dss})(R2)$. Typical I_{dss} is 200 nA, causing V_{OUT} to be 14 mV high. Temperature coefficient of I_{dss} is low, typically 0.1%/°C. For best results in a single point adjustment, V_{OUT} should be adjusted to 1.253V + I_{dss} (R2). I_{dss} can be easily measured by open circuiting R1 and measuring the drop across R2. The resulting voltage must be divided by 2 due to an internal action which causes 2 I_{dss} to flow when no current flows from the R pin. Example: with R1 open, 32 mV is measured across R2. Set V_{OUT} equal to 1.253V + 32 mV/2 = 1.269V. Even lower TC can be obtained by measuring the output at 2 temperatures and using the following formula to calculate the exact zero TC output voltage for each reference.

$$V_{OUT}\,(0\ TC) = V1 - \frac{T1\,(V2 - V1)}{T2 - T1}$$

Where:

V1 = Output voltage at T1

V2 = Output voltage at T2

T = Absolute temperture (°K)

The limitation on temperature drift after a 2 point calibration is non-linearity. This reference circuit has a non-reducible bow error of ≈ 10 ppm/°C over a temperature range of −25°C to +100°C and ≈5 ppm/°C from 0°C to +70°C. At 125°C, leakage creates significant error, causing the output voltage to droop about 5 mV.

Noise of the reference consists primarily of theoretical shot noise current from the LM134. At the 10 μA level, this is about 6 pA/$\sqrt{\text{Hz}}$ rms from 10 Hz to 10 kHz. Total output noise would be 0.4 μV/$\sqrt{\text{Hz}}$ rms over this frequency range, except that C1 bypasses most of the noise above 2 kHz. Measured output noise was 25 μVrms over a 10 Hz to 10 kHz bandwidth with C1 = 1000 pF. Larger values of C1 may be used if lower broadband noise is needed. Low frequency noise is about 25 μV peak-to-peak from 0.1 Hz to 10 Hz.

The LM134 has a negative output resistance at the R pin when resistance is inserted in series with the V^- pin. The value of this negative resistance is approximately $-R_X/19$, where R_X is the equivalent resistance from V^- to ground. In this reference circuit R_X is 72 kΩ, yielding a negative output resistance of 3.8 kΩ. Resistor R2 sums with this resistance to give the reference a net zero output resistance (±400Ω). Loading should be limited to about 5 μA. Line regulation for the reference is typically less than 0.5 mV with an input voltage of 5V ±2V. Minimum input voltage for a 2 mV drop in output voltage is 2.5V at −55°C, 2.4V at 25°C and 2.3V at 125°C.

Although this reference was designed for ultra-low operating current, there is no reason that it cannot be used at higher current levels as well. All resistor values are simply scaled downward. Higher operating current will give lower output resistance, more drive capability, less sensitivity to FET I_{dss}, lower noise, and less droop at 125°C.

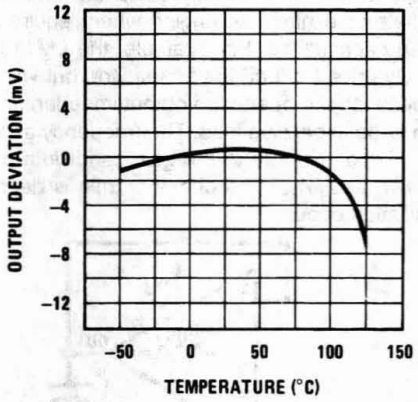


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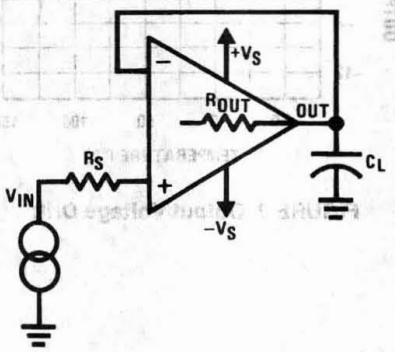
FIGURE 2. Output Voltage Drift

Get Fast Stable Response From Improved Unity-Gain Followers

National Semiconductor
Linear Brief 42
Robert A. Pease

In many applications, a unity-gain follower (e.g. any operational amplifier with tight feedback to the inverting input) may oscillate or exhibit bad ringing when required to drive heavy load capacitance. For example, the LM110 follower will normally drive a 50 pF load capacitor, but will not drive 500 pF, because the open-loop outout impedance is lagged by such a large capacitive load. The frequency at which this lag occurs is comparable to the gain-bandwidth product of the amplifier, and when the phase margin is decreased to zero, oscillation occurs.



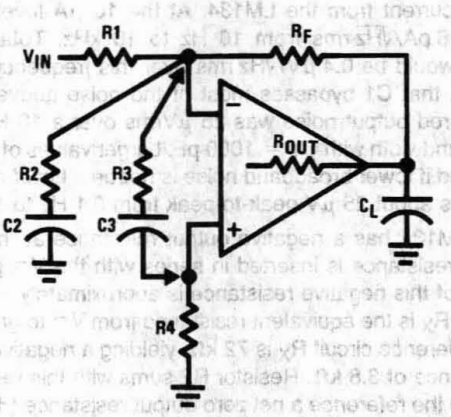
TL/H/8491–1

FIGURE 1. Unity-Gain Follower Attempting to Drive Capacitive Load

While the solution to this problem is not widely known, an analysis of the general problem shown in *Figure 2* can lead to a useful approach. It is generally known that increasing the noise gain of an op amp's feedback network will improve tolerance of capacitive load. In *Figure 2*, adding a resistor R2 ≅ $R_F/10$ will do this. (A moderate capacitor C2 is usually inserted in series with R2, to prevent the DC noise gain from increasing also—to avoid degrading DC offset, drift and inaccuracy.) If the op amp has a 1 MHz gain bandwidth product, and R1 = R_F, the closed-loop frequency response will be ½ MHz. Adding R2 = $R_F/10$ will drop the closed-loop frequency response to 90 kHz, where the amplifier can usually tolerate a much larger C_L;

$$\text{Noise Gain} = \frac{R_F}{R1} + \frac{R_F}{R2} + 1 \text{ (AC)}$$

$$\text{Noise Gain} = \frac{R_F}{R1} + 1 \text{ (DC)}$$



TL/H/8491–2

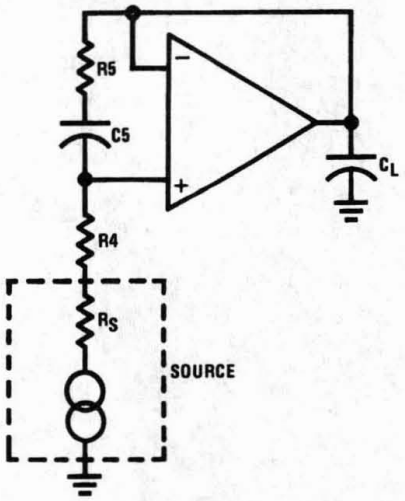
FIGURE 2. Stabilizing an Operational Amplifier for Capacitive Load

A similar result will occur if you install R3 and C3, instead of R2. Now the (AC) noise gain will be:

$$1 + \frac{R4}{R3} + \frac{R_F}{R3} + \left(\frac{R_F}{R1}\right)\left(\frac{R3 + R4}{R3}\right)$$

As a simplification, if R1 is an open circuit, the AC noise gain will be: ($R4/R3 + R_F/R3 + 1$). Now it can be seen that noise gain can be raised by having a low value of R3 and a high value of R4 or R_F (or both).

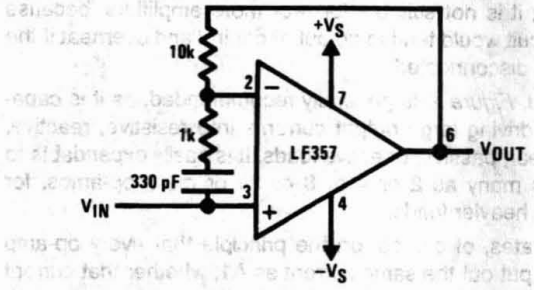
In particular, where R_F is required to be 0Ω, as in a follower, the noise gain can be raised by adding a large R4 and a small R5, as shown in *Figure 3*. If R_S is low, the AC noise gain will be R4/R5 + 1. (If R_S is large and constant, R4 may be unnecessary, and the noise gain would then be $R_S/R5 + 1$.) For LM110/LM310's R4 = 10 kΩ is recommended and when R5 = 3.3 kΩ, C5 = 200 pF, the LM110 will stably drive C_L up to 600 pF.



TL/H/8491–3

FIGURE 3. Stabilizing a Unity-Gain Follower for Capacitive Load

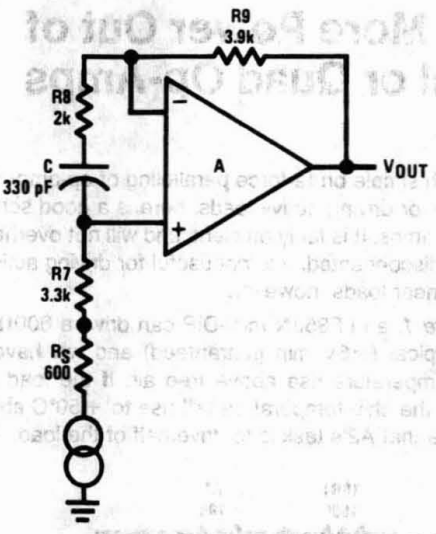
Another application of this technique is for making a fast follower with a high slew rate. An LF356 is specified as a follower, but an LF357 must be applied at an "$A_V = 5$" minimum, because it has been "decompensated" with a smaller internal capacitor. Most people do not realize how easy it is to apply an LF357 as a follower. In *Figure 4*, an LF357 will have fast, stable response just like an LF356 does, when R_S is $< 1\ k\Omega$, but it will have a $50V/\mu s$ slew rate (typical) vs. $12V/\mu s$ for an LF356.



TL/H/8491–4

FIGURE 4. Unity-Gain Follower With Fast Slew Rate

Similarly, an LM348 is a fast decompensated quad op amp. Its bipolar input stage has a finite bias current, 200 nA max. For best results, the resistance which makes up the noise gain should be put equally in the **plus** and **minus** input circuits, as shown in *Figure 5*. The LM349 can slew at $2V/\mu s$ typical, and is much faster for handling audio signals without distortion than the LM348 (which at $0.5V/\mu s$ is only as fast as an ordinary LM741). The same approach can be used for an LM101 with a 5 pF damping capacitor. While these circuits give faster slewing, the bandwidth may degrade if the source impedance R_S increases. Also, when the AC noise gain is raised, the AC noise will also be increased. While most modern op amps have low noise, a noise gain of 10 may make a significant increase in output noise, which the user should check to insure it is not objectionable.



TL/H/8491–5

FIGURE 5. Application of Fast Follower With Balanced Resistors, R9 = R7 + R_S, A = 1/4 LM349 (or LM101 with 5 pF Capacitor)

If the series capacitor is much larger than necessary, noise will be increased more than necessary. In general, choose the C5 for *Figure 3*, (e.g.) per these guidelines: (where f_V = unity-gain bandwidth of op amp)

$$\text{C5 Min} = \frac{4 \bullet \left(1 + \frac{R4}{R5}\right)}{2\pi R5 \bullet f_V} = \frac{R4 + R5}{\frac{\pi}{2} \bullet f_V \bullet (R5)^2}$$

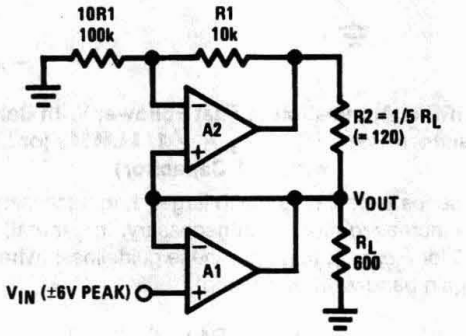
For best results, choose the design center value of C5 to be 2 or 3 times C5 min.

Get More Power Out of Dual or Quad Op-Amps

National Semiconductor
Linear Brief 44
Bob Pease

Although simple brute-force paralleling of op-amps is a bad scheme for driving heavy loads, here is a good scheme for dual op-amps. It is fairly efficient, and will not overheat if the load is disconnected. It is *not* useful for driving active loads or nonlinear loads, however.

In *Figure 1*, an LF353N mini-DIP can drive a 600Ω load to ±9V typical (±6V min guaranteed) and will have only a 47°C temperature rise above free air. If the load R is removed, the chip temperature will rise to +50°C above free air. Note that A2's task is to drive half of the load. A1 could be applied as a unity-gain follower *or* inverter, or as a high-gain or low-gain amplifier, integrator, etc.



TL/H/8493–1

A1, A2 = 1/2 LM747 or 1/2 LF353 or any op-amp.

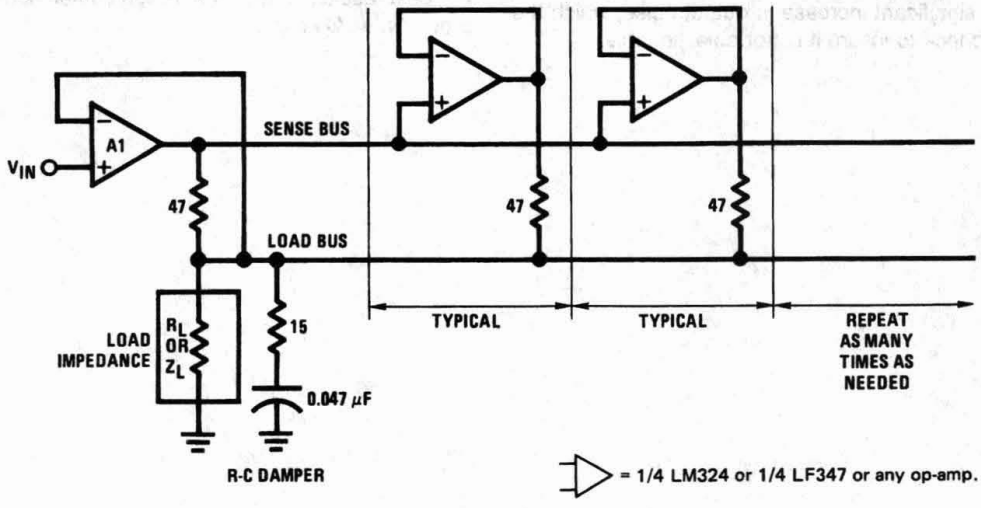
FIGURE 1. A1 and A2 Share the Load

While *Figure 1* is suitable for sharing a load between 2 amplifiers, it is not suitable for 4 or more amplifiers, because the circuit would tend to go out of control and overheat if the load is disconnected.

Instead, *Figure 2* is generally recommended, as it is capable of driving large output currents into resistive, reactive, nonlinear, passive, or active loads. It is easily expandable to use as many as 2 or 4 or 8 or 20 or more op-amps, for driving heavier loads.

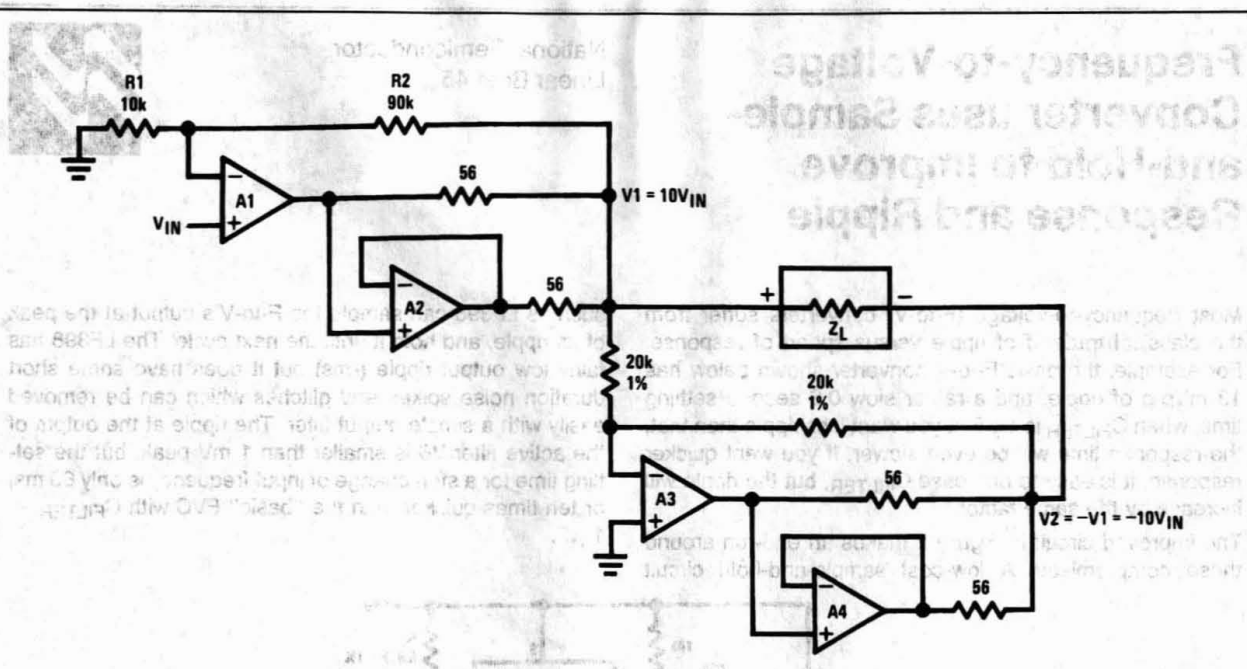
It operates, of course, on the principle that every op-amp has to put out the same current as A1, whether that current is plus, minus, or zero. Thus if the load is removed, all amplifiers will be unloaded together. A quad op-amp can drive 600Ω to ±11 or 12 volts. Two quads can put out ±40 mA, but they get only a little warm. A series R-C damper of 15Ω in series with 0.047 μF is useful to prevent oscillations (although LM324's do not seem to need any R-C damper).

Of course, there is no requirement for the main amplifier to run only as a unity-gain amplifier. In the example shown in *Figure 3*, A1 amplifies a signal with a gain of +10. A2 helps it drive the load. Then A3 operates as a unity-gain inverter to provide V2 = −V1, and A4 helps it drive the load. This circuit can drive a floating 2000Ω load to ±20V, accurately, using a slow LM324 or a quick LF347.



TL/H/8493–2

FIGURE 2. Improved Load-Sharing Circuit



TL/H/8493–3

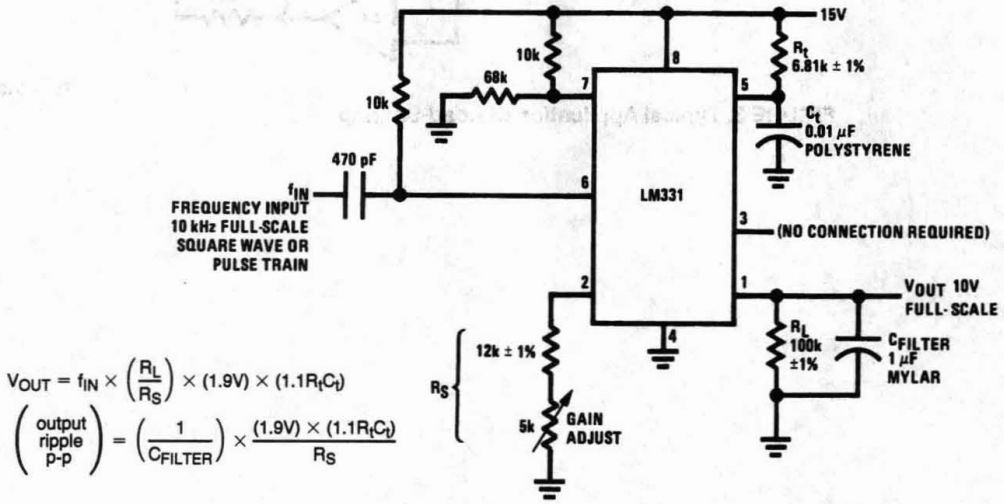
FIGURE 3. Typical Application of Load-Sharing

Frequency-to-Voltage Converter uses Sample-and-Hold to Improve Response and Ripple

National Semiconductor
Linear Brief 45

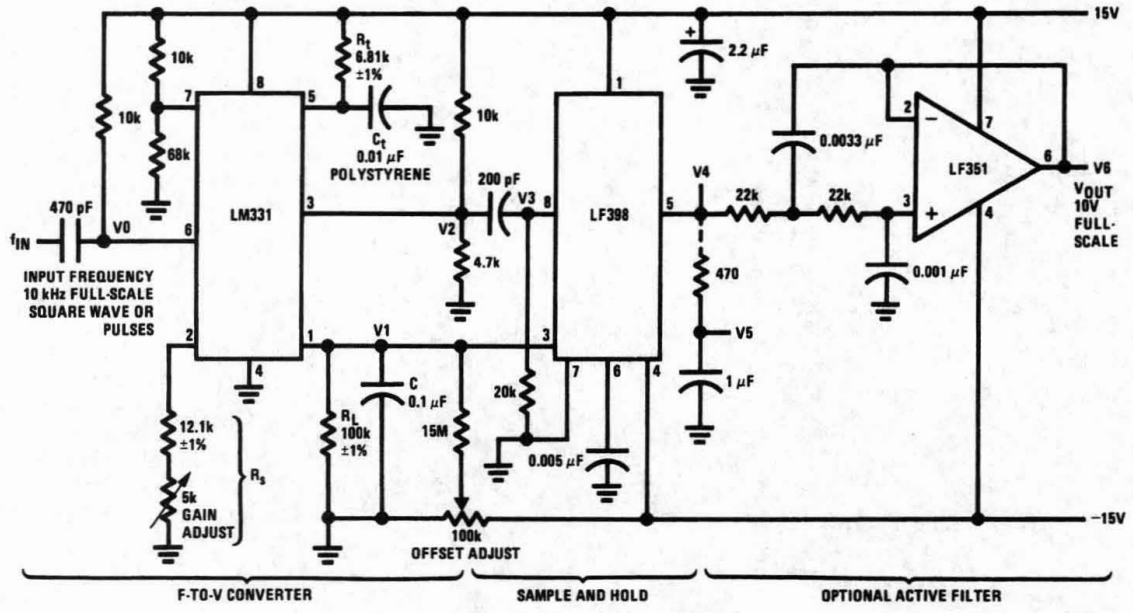
Most frequency-to-voltage (F-to-V) converters suffer from the classical tradeoff of ripple versus speed of response. For example, the basic F-to-V converter shown below has 13 mVp-p of ripple, and a rather slow 0.6 second settling time, when C_{FILTER} is 1 μF. If you want less ripple than that, the response time will be even slower. If you want quicker response, it is easy to decrease C_{FILTER}, but the ripple will increase by the same factor.

The improved circuit in *Figure 2* makes an end-run around these compromises. A low-cost sample-and-hold circuit such as LF398 can sample the F-to-V's output at the peak of its ripple, and hold it until the next cycle. The LF398 has fairly low output ripple (rms) but it does have some short duration noise spikes and glitches which can be removed easily with a simple output filter. The ripple at the output of the active filter V6 is smaller than 1 mV peak, but the settling time for a step change of input frequency is only 60 ms, or ten times quicker than the "basic" FVC with C_{FILTER} = 1 μF.



TL/H/8494–1

FIGURE 1. Basic Frequency-to-Voltage Converter



TL/H/8494–2

FIGURE 2. Improved F-to-V Converter Using Sample-and-Hold

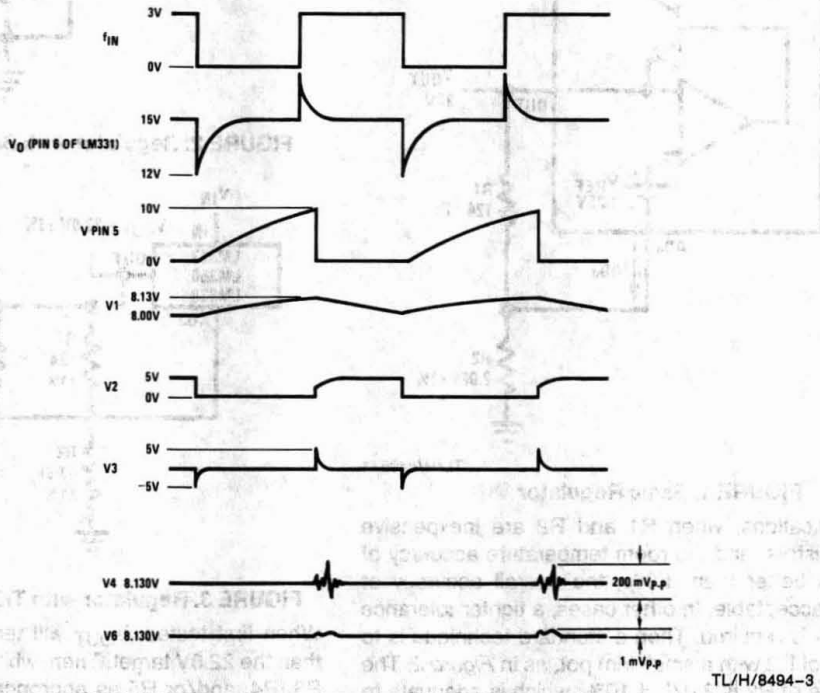
DETAILS OF OPERATION (Refer to *Figure 3*, Waveforms)

When the input frequency waveform has a negative-going transition, pin 6 of the LM331 is driven momentarily lower than the 13V threshold voltage at pin 7. This initiates a timing cycle controlled by the R_t and C_t at pin 5, and also causes a transition from +5V to 0V at pin 3, (the normal VFC logic output) which is usually left unused in F-to-V operation.

During the timing cycle ($t = 1.1 \times R_t \times C_t = 75\ \mu s$, for the example shown) a precision current source $i = 1.9\ V/R_S$ flows out of pin 1 of the LM331, and charges V1 up to a value slightly higher than the average DC value of V1. At the end of the timing cycle, V1 stops charging up, and also V2 rises. The 10 kΩ pull-up resistor is coupled (through the 200 pF capacitor) to V3, and causes the LF398 to *sample* for about 5 μs. Then the LF398 goes back into *hold*. This entire operation is repeated at the same frequency as f_{IN}. The average voltage at V1 will be the same 10V full scale, according to the same formula of *Figure 1*. And the peak-to-peak ripple can be computed as 65 mV peak, 130 mVp-p, using the appropriate formula.

Now, the input to the sample-and-hold at pin 3 may have a 10.000V average DC value, but the output will be at 10.065V, because the sample occurs at the peak value of V1. Thus, to get an output with low offset, a 15 MΩ resistor is used to offset the V1 signal to a lower level. Trim the offset adjust pot to get V_{OUT} = 1V at 1 kHz, and trim the gain adjust pot to get V_{OUT} = 10V at 10 kHz (the interaction is minor), as measured at V4, V5, or V6. The rms value of the ripple at V4 is rather small, but the peak-to-peak ripple (spikes and glitches) may be excessive. A simple R-C filter can provide a filtered output at V5; or a simple active filter using an inexpensive LF351, will give sub-millivolt (peak) ripple at V6, with improved settling time and low output impedance.

This F-to-V converter will have a good linearity, better than 0.1%, but only from 10 kHz down to 500 Hz. Between 200 Hz and 20 Hz, V_{OUT} is not very proportional to f_{IN}. And at 0 Hz, the output will be indeterminate, because the sample-and-hold will never sample! However, there are many F-to-V applications where a 20:1 frequency range is adequate.



TL/H/8494–3

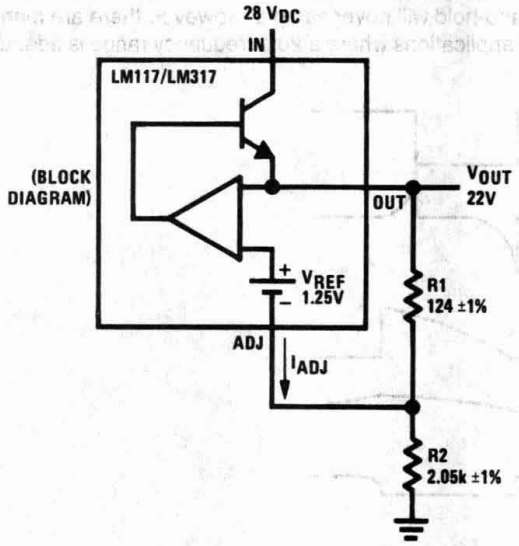
FIGURE 3. Waveforms, Improved F-to-V Converter

A New Production Technique for Trimming Voltage Regulators

National Semiconductor
Linear Brief 46
Robert A. Pease

Three-terminal adjustable voltage regulators such as the LM317 and LM337 are becoming popular for making regulated supplies in instruments and various other OEM applications. Because the regulated output voltage is easily programmed by two resistors, the designer can choose any voltage in a wide range such as 1.2V to 37V. In a typical example (*Figure 1*) the output voltage will be:

$$V_{OUT} = V_{REF}\left(\frac{R2}{R1} + 1\right) + R2 \bullet I_{ADJ}$$



TL/H/8495–1

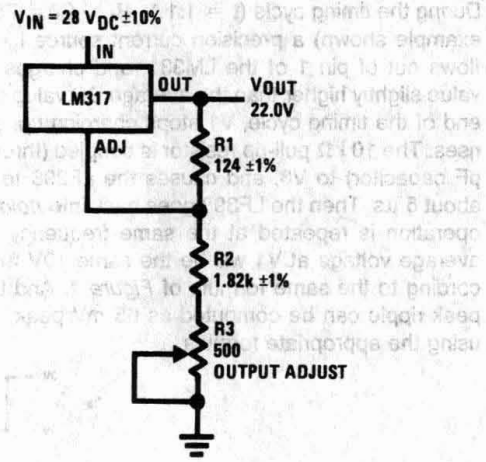
FIGURE 1. Basic Regulator

In many applications, when R1 and R2 are inexpensive ±1% film resistors, and the room temperature accuracy of the LM117 is better than ±3%, the overall accuracy of ±5% will be acceptable. In other cases, a tighter tolerance such as ±1% is required. Then a standard technique is to make up part of R2 with a small trim pot, as in *Figure 2*. The effective range of R2 is 2.07k ±10%, which is adequate to bring V_{OUT} to exactly 22.0V. (Note that a 200Ω rheostat in series with 1.96 kΩ ±1% would not necessarily give a ±5% trim range, because the end resistance and wiper resistance could be as high as 10Ω or 20Ω; and the maximum value of an inexpensive 10% or 20% tolerance trimmer might be as low as 180Ω or 160Ω.)

In some designs, the engineering policy may frown on the use of such trim pots, for one or more of the following reasons:

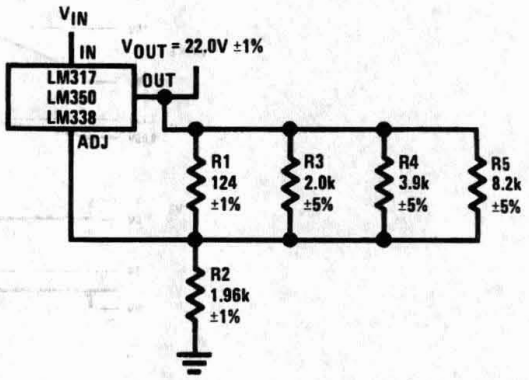
— Good trim pots are more expensive.
— Inexpensive trim pots may be drifty or unreliable.
— Any trim pot which can be adjusted can be *mis*adjusted, sooner or later.

To get a tighter accuracy on a regulated supply, while avoiding these disadvantages of trim pots, consider the scheme in *Figure 3*.



TL/H/8495–2

FIGURE 2. Regulator with Small Adjustment Range



TL/H/8495–3

FIGURE 3. Regulator with Trimmable Output Voltage

When first tested, V_{OUT} will tend to be 4% to 6% higher than the 22.0V target. Then, while monitoring V_{OUT}, snip out R3, R4, and/or R5 as appropriate to bring V_{OUT} closer to 22.0V. This procedure will bring the tolerance inside ±1%:

— If V_{OUT} is 23.08V or higher, cut out R3 (if lower, don't cut it out).
— Then if V_{OUT} is 22.47V or higher, cut out R4 (if lower, don't).
— Then if V_{OUT} is 22.16V or higher, cut out R5 (if lower, don't).

The entire production distribution will be brought inside 22.0V ±1%, with a cost of 3 inexpensive carbon resistors, much lower than the cost of any pot. After the circuit is properly trimmed, it is relatively immune to being misadjusted by a screwdriver. Of course, the resistors' carcasses must be properly removed and disposed of, for full reliability to be maintained.

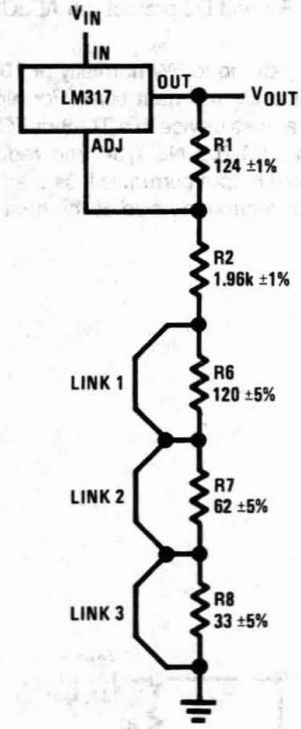
An alternate scheme shown in *Figure 4* has R6, R7, and R8 all shorted out initially with a stitch or jumper of wire. The

trim procedure is to open up a link to bring a resistor into effect. The advantage of this circuit is that V_{OUT} starts out *lower* than the target value, and never exceeds that voltage during trimming. In this scheme, note that a total "pot resistance" of 215Ω is plenty for a 10% trim span, because the *minimum* resistance is always below 1Ω, and the maximum resistance is always more than 200Ω—it can cover a much wider range than a 200Ω pot.

The circuit of *Figure 5* shows a combination of these trims which provides a new advantage, if a ±2% max tolerance is adequate. You may snip out R4, or link L1, or both, to accommodate the worst case tolerance, but in most cases, the output will be within spec without doing any trim work at all. This takes advantage of the fact that most ±1% resistors are well within ±⅓%, and most LM337's output voltage tolerances are between −½% and +1½%, to cut the average trim labor to a minimum. Note that L1 could be made up of a 2.7Ω ±10% resistor which may be easier to handle than a piece of wire.

In theory, a 10% total tolerance can be reduced by a factor of $(2^n - 1)$ when n binary-weighted trims are used. In practice, the factor would be $(1.8^n - 1)$ if ±10% trim resistors are used, or $(1.9^n - 1)$ if ±5% resistors are used. For n = 2, a 10% tolerance can be cut to 3.8% p-p or ±1.9%. For n = 3, the spread will be 1.7% p-p or ±0.85%, and most units will be inside ±0.5%, perfectly adequate for many regulator applications.

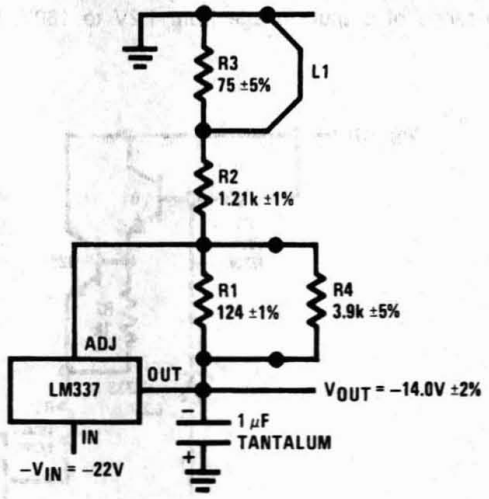
National Semiconductor manufactures several families of adjustable regulators including LM117, LM150, LM138, LM117HV, LM137, and LM137HV, with output capabilities from 0.5A to 5A and from 1.2V to 57V. For complete specifications and characteristics, refer to the appropriate data sheet or the 1982 Linear Databook.



TL/H/8495–4

If V_{OUT} is lower than 20.90V, snip link 1 (if not, don't).
Then if V_{OUT} is lower than 21.55V, snip link 2 (if not, don't).
Then if V_{OUT} is lower than 21.82V, snip link 3 (if not, don't).

FIGURE 4. Alternate Trim Scheme



TL/H/8495–5

If $|V_{OUT}|$ is smaller than 13.75V, snip L1 and it will get bigger by 6%.
Then if $|V_{OUT}|$ is bigger than 14.20V, snip R4 and it will get smaller by 3%.

FIGURE 5. Circuit Which Usually Needs No Trim to Get V_{OUT} Within ±2% Tolerance

High Voltage Adjustable Power Supplies

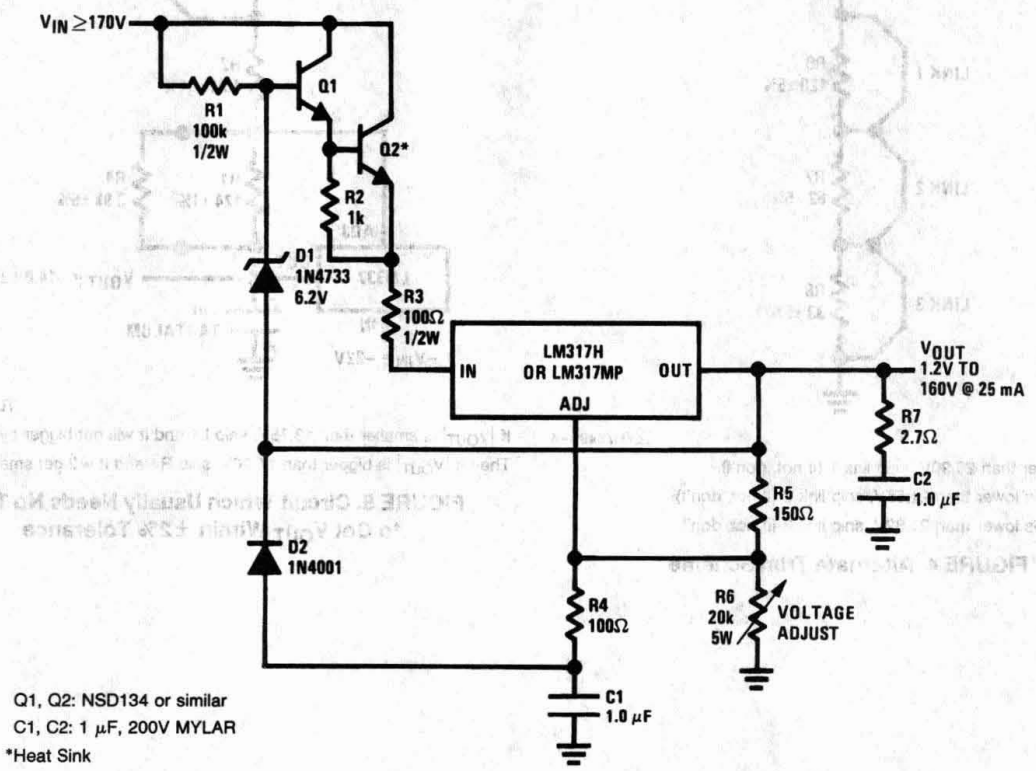
National Semiconductor
Linear Brief 47
Michael Maida

7.4.4 HIGH VOLTAGE ADJUSTABLE POWER SUPPLIES

The floating-mode operation of adjustable three-terminal regulators such as the LM117 family make them ideal for high voltage operation. The regulator has no ground pin; instead, all the quiescent current (about 5 mA) flows to the output terminal. Since the regulator sees only the input-output differential, its voltage rating — 40V for the standard LM117 series and 60V for the high voltage LM117HV series — will not be exceeded for outputs of hundreds of volts. However, the IC may break down when the output is shorted unless special design approaches are used to protect against it.

Figure 1 shows how it's done. Zener diode D1 ensures that the LM317H sees only a 5V input-output differential over the entire range of output voltage from 1.2V to 160V. Since high-voltage transistors by necessity have a low β, a Darlington is used to stand off the high voltage. The zener impedance is low enough that no bypass capacitor is required directly at the LM317 input. (In fact, *no* capacitor should be used here if the circuit is to survive an output short!) R3 limits short circuit current to 50 mA. The RC network on the output improves transient response as does bypassing the ADJUST pin, while R4 and D2 protect the ADJUST pin during shorts.

Since Q2 may dissipate up to 5W normally or 10W during a short circuit, it should be well heat sunk. For higher output currents substitute a pass device in a TO-3 or TO-220 package in place of the TO-202 NSD134 and reduce R3. Of course, if the required output current is less than 25 mA, R3 can be increased to reduce the size of the heat sink needed.

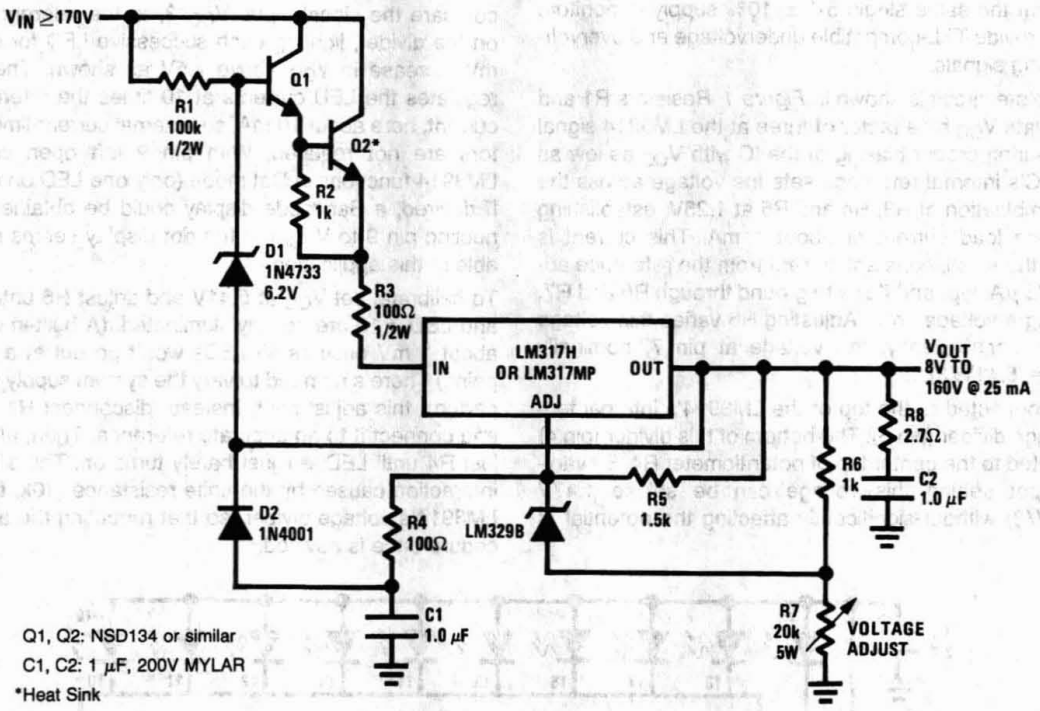


TL/H/7335–1

FIGURE 1. Basic High Voltage Regulator

An improved approach is shown in *Figure 2*. Here an LM329B 6.9V zener reference has been stacked in series with the LM317's internal reference. This both improves temperature stability, since the LM329B has a guaranteed TC of ±20 ppm/°C, and improves regulation, because more loop gain is available from the LM317.

These techniques can be extended for higher output voltages and/or currents by either using better high voltage transistors or cascoding or paralleling (with appropriate emitter ballasting resistors) several transistors. The output short circuit current, determined by R3, must be within Q2's safe area of operation so that secondary breakdown cannot occur.



TL/H/7335–2

FIGURE 2. Precision High Voltage Regulator

Simple Voltmeter Monitors TTL Supplies

National Semiconductor
Linear Brief 48
Michael Maida

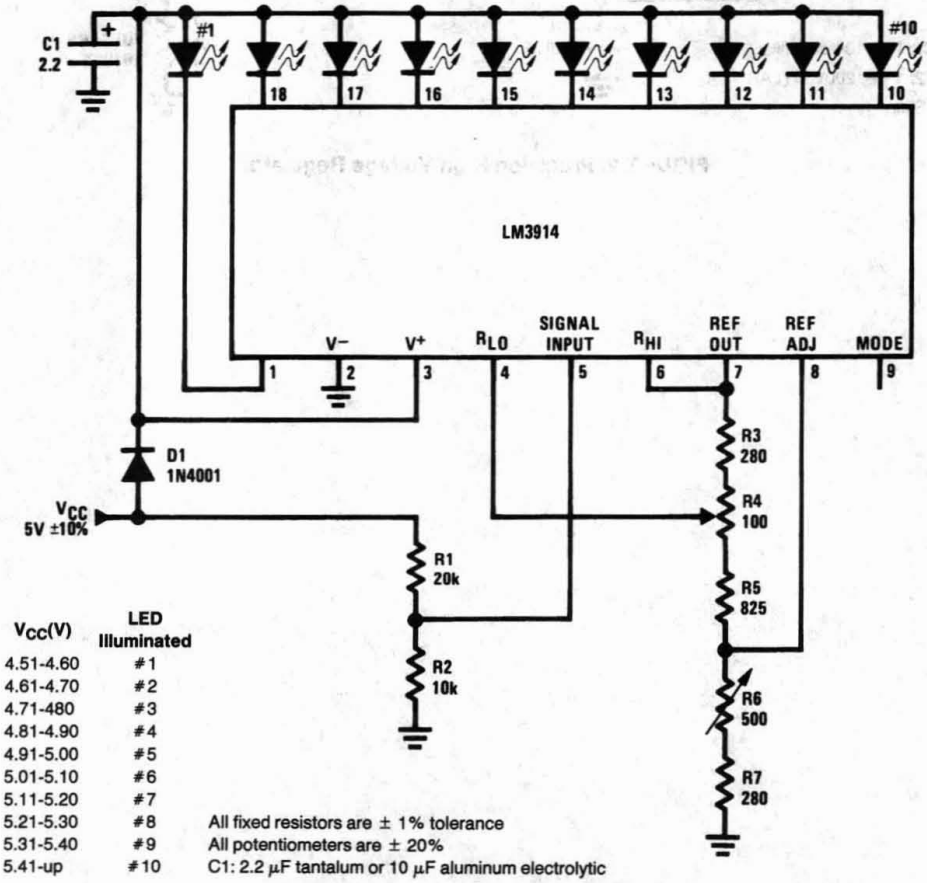
Using a National Semiconductor LM3914 bar/dot display driver chip, a few resistors and some LEDs, a simple expanded-scale voltmeter is easily constructed. Furthermore, it runs from the same single 5V ± 10% supply it monitors and can provide TTL-compatible undervoltage and overvoltage warning signals.

The complete circuit is shown in *Figure 1*. Resistors R1 and R2 attenuate V_{CC} by a factor of three at the LM3914 signal input, ensuring proper biasing of the IC with V_{CC} as low as 4V. The IC's internal reference sets the voltage across the series combination of R3, R4 and R5 at 1.25V, establishing a reference load current of about 1 mA. This current is joined by the small, constant current from the reference adjust pin (75 μA, typ) and flows to ground through R6 and R7, developing a voltage drop. Adjusting R6 varies this voltage drop and, consequently, the voltage at pin 7, nominally 1.803V (= 5.41V/3).

Pin 7 is connected to the top of the LM3914's internal ten-step voltage divider (pin 6). The bottom of this divider (pin 4) is connected to the center tap of potentiometer R4. By varying the pot setting this voltage can be set to 1.47V (= 4.41V/3) without significantly affecting the potential at pin 7. The optional diode D1 protects against damaging the IC by connecting the leads backwards.

In operation, the LM3914's ten internal voltage comparators compare the signal input, $V_{CC}/3$, to the reference voltage on the divider, lighting each successive LED for every 100 mV increase in V_{CC} above 4.5V as shown. The LM3914 regulates the LED currents at 10 times the reference load current, here about 10 mA, so external current-limiting resistors are not required. With pin 9 left open circuit, the LM3914 functions in Dot mode (only one LED on at a time). If desired, a Bar mode display could be obtained by connecting pin 9 to V_{CC}, but the dot display seems more suitable in this application.

To calibrate, set V_{CC} at 5.41V and adjust R6 until LED #9 and LED #10 are equally illuminated. (A built-in overlap of about 1 mV ensures all LEDs won't go out at a threshold point.) There's no need to vary the system supply voltage to perform this adjustment. Instead, disconnect R1 from V_{CC} and connect it to an accurate reference. Then, at 4.5V, adjust R4 until LED #1 just barely turns on. There is a slight interaction caused by the finite resistance (10k, typ) of the LM3914's voltage divider, so that repeating the above procedure once is advised.



V_{CC}(V)	LED Illuminated
4.51-4.60	#1
4.61-4.70	#2
4.71-480	#3
4.81-4.90	#4
4.91-5.00	#5
5.01-5.10	#6
5.11-5.20	#7
5.21-5.30	#8
5.31-5.40	#9
5.41-up	#10

All fixed resistors are ± 1% tolerance
All potentiometers are ± 20%
C1: 2.2 μF tantalum or 10 μF aluminum electrolytic

TL/H/8496–1

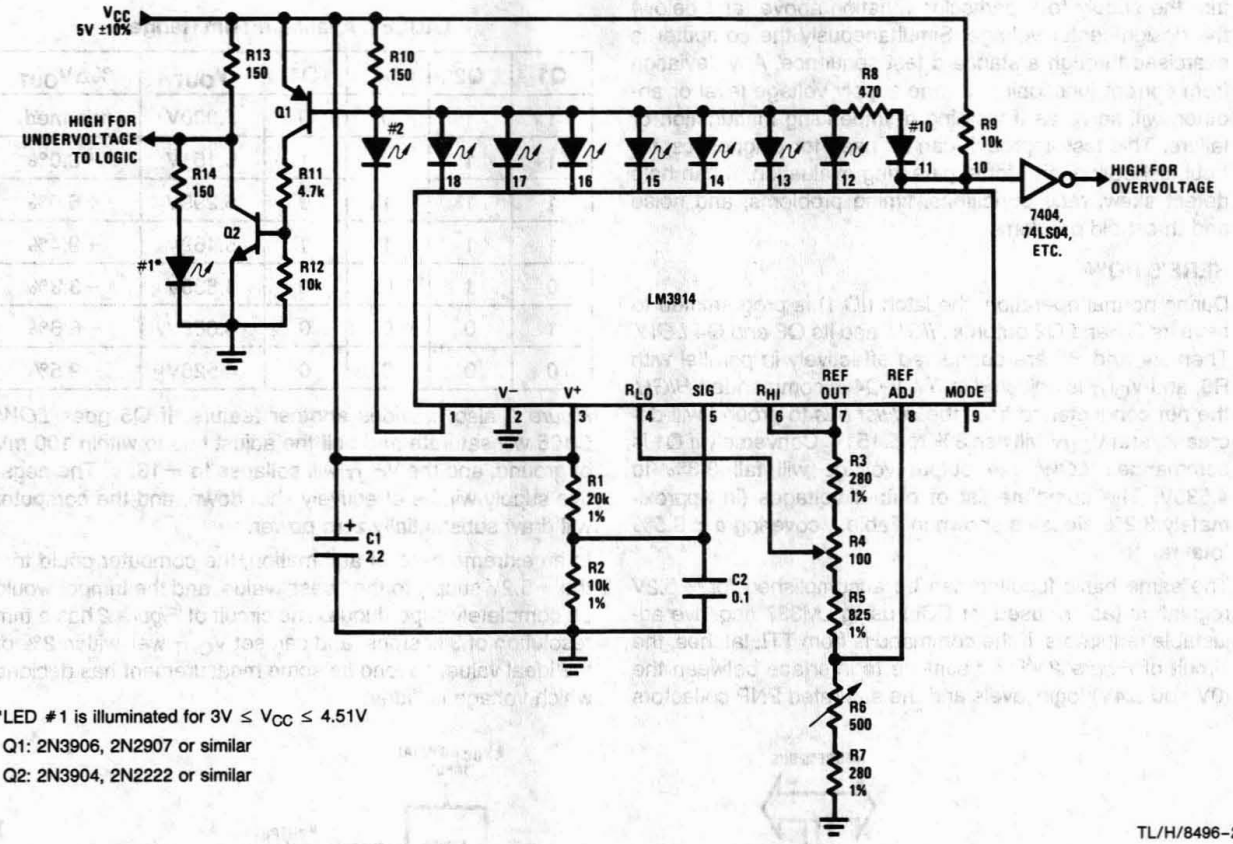
FIGURE 1. 5V Power Supply Monitor

The LED driver outputs can directly drive a TTL gate, so that the LED #1 and LED #10 outputs may be used for undervoltage and overvoltage warning signals. These may be used to initiate a soft shutdown or summon an operator, for example. The interfacing circuitry is shown in *Figure 2*. The 470Ω resistor R8 ensures that the LM3914 output will saturate to provide the proper TTL low level. Pull-up resistor R9 provides the logic high level.

In the previous circuit the undervoltage LED goes out when V_{CC} is less than 4.51V, a deficiency that is corrected here, Transistors Q1 and Q2 shut off LED #1 whenever any other LED is turned on by the LM3914. Q2's output will directly drive TTL.

Calibration procedure is the same as before. The LM3914 output thresholds have been shifted up by 100 mV and output #10 is or-tied with output #9. Other outputs may be wire-or'd together if 100 mV resolution is not necessary. If desired, the outputs can be color coded by making LED #1 and LED #10 red, LED #2 and LED #9 amber, and the rest of the LEDs green to ease interpretation.

This circuit is useful where quick and easy voltage adjustments must be made, such as in the field or on the production line. The circuit's low cost makes it feasible to incorporate it into the system, where the overvoltage and undervoltage warning signals provide an attractive extra. Of course, these techniques can be used to monitor any higher voltages, positive or negative.



*LED #1 is illuminated for 3V ≤ V_{CC} ≤ 4.51V

Q1: 2N3906, 2N2907 or similar

Q2: 2N3904, 2N2222 or similar

TL/H/8496–2

FIGURE 2. Power Supply Monitor with TTL Interface and Extended Undervoltage Range

Programmable Power Regulators Help Check Out Computer System Operating Margins

National Semiconductor
Linear Brief 49
Robert Pease

It is a familiar situation that some computer systems which are functional with a 5V supply may run marginally at 5.1V but can show a solid failure at 5.3V (or, vice versa) even though all these voltages are within the system's specifications. The LM338 is an example of a monolithic voltage regulator which can be placed under computer control, and can trim the supply to a particular variation above (and below) the design-center voltage. Simultaneously the computer is exercised through a standard test sequence. Any deviation from correct functioning, at one supply voltage level or another, will serve as a warning of impending malfunction or failure. This test approach can be used for diagnostics, for troubleshooting, and for engineering evaluation. It can help detect skew, race conditions, timing problems, and noise and threshold problems.

HERE'S HOW

During normal operation, the latch (IC 1) is programmed to have its Q1 and Q2 outputs *HIGH*, and its Q3 and Q4 *LOW*. Then R4 and R5 are connected effectively in parallel with R6, and V_{OUT} is adjusted to 5V. If Q4 is commanded *HIGH*, the net conductance from the *adjust bus* to ground will decrease, and V_{OUT} will rise 3% to 5.151V. Conversely if Q1 is commanded *LOW*, the output voltage will fall 3.3% to 4.835V. The complete list of output voltages (in approximately 3.2% steps) is shown in Table I, covering a ±9.5% total range.

The same basic function can be accomplished for −5.2V regulators (as are used for ECL) using LM337 negative adjustable regulators. If the command is from TTL latches, the circuit of *Figure 2* will be suitable to interface between the (0V and 2.4V) logic levels and the saturated PNP collectors as shown. The resistors R101–R104 are switched by transistors Q101–Q104 in a similar way to *Figure 1*. Note that the resistors in *Figure 2* are in a binary-weighted proportion. To decrease V_{OUT} by 2%, just change Q4 to *LOW*; but to *increase* V_{OUT} by 2%, set Q1 *HIGH* and Q2, Q3, Q4 all *LOW*, in a standard offset binary scheme.

TABLE I. Available Trim Range

Q1	Q2	Q3	Q4	V_{OUT}	$\%\Delta V_{OUT}$
1	1	0	0	5.000V	(trimmed)
1	1	0	1	5.151V	+3.0%
1	1	1	0	5.299V	+6.0%
1	1	1	1	5.469V	+9.4%
0	1	0	0	4.835V	−3.3%
1	0	0	0	4.669V	−6.6%
0	0	0	0	4.526V	−9.5%

Figure 2 also provides another feature. If Q5 goes *LOW*, Q105 will saturate and pull the adjust bus to within 100 mV of ground, and the V_{OUT} will collapse to −135V. The negative supply will be effectively shut down, and the computer will draw substantially zero power.

In an extreme case of automation, the computer could trim the −5.2V supply to the "best" value, and the trimpot would be completely superfluous. The circuit of *Figure 2* has a trim resolution of 3% steps, and can set V_{OUT} well within 2% of the ideal value, so long as some measurement has decided which voltage is "ideal".

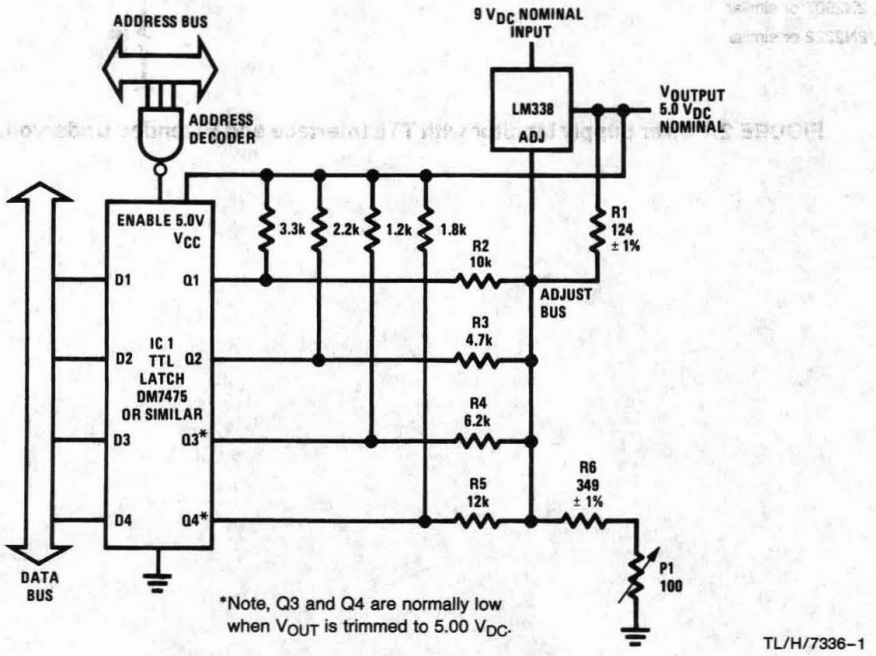
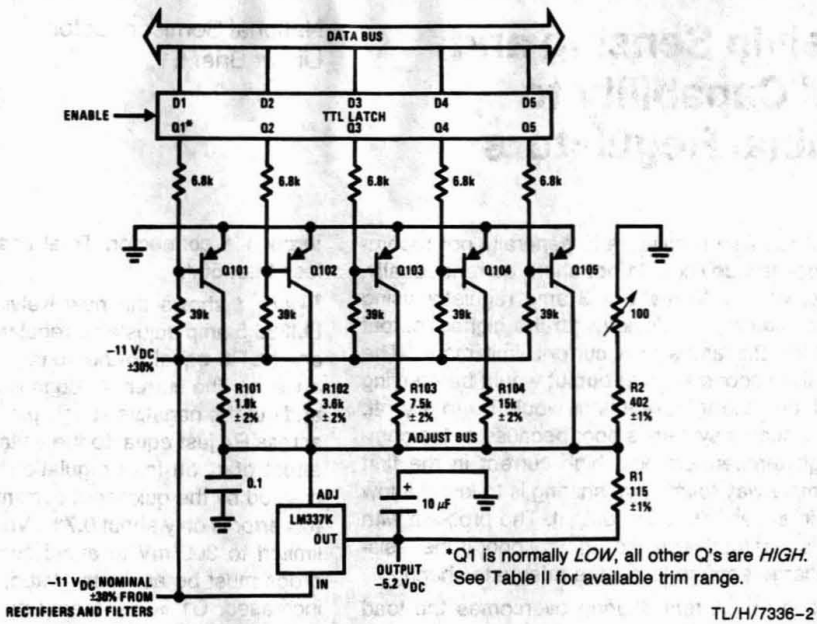


FIGURE 1. Programmable Power Supply



TL/H/7336–2

FIGURE 2. Programmable Negative Supply

TABLE II. Available Trim Range

Q1	Q2	Q3	Q4	V_{OUT}	$\%\Delta V_{OUT}$
0	1	1	1	5.200V	(trimmed)
0	1	1	0	5.110V	−1.7%
0	1	0	1	5.025V	−3.4%
0	1	0	0	4.944V	−4.9%
0	0	1	1	4.853V	−6.7%
0	0	1	0	4.779V	−8.1%
0	0	0	1	4.707V	−9.5%
0	0	0	0	4.638V	−10.8%
1	0	0	0	5.310V	+2.1%
1	0	0	1	5.409V	+4.0%
1	0	1	0	5.513V	+6.0%
1	0	1	1	5.622V	+8.1%
1	1	0	0	5.757V	+10.7%
1	1	0	1	5.880V	+13.1%
1	1	1	0	6.010V	+15.6%
1	1	1	1	6.147V	+18.2%

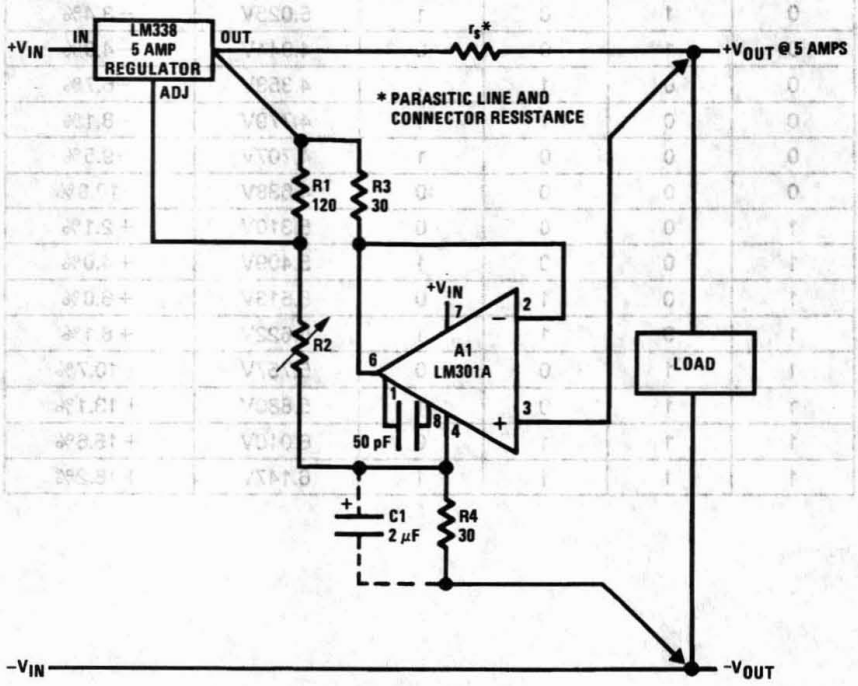
Add Kelvin Sensing and Parallel Capability to 3-Terminal Regulators

National Semiconductor
Linear Brief 51

Paralleling of 3-terminal regulators is generally not recommended because the devices do not share current equally. If, for instance, you try to make a 3 amp regulator using three 1 amp regulators, the device with the highest output could be carrying 2.5 amps in a current limit mode. The regulator with the second highest output would be carrying only 0.5 amps, and the third regulator would be totally off. The reliability of such a system is poor because of the combination of high temperature and high current in the first regulator. A simple way to improve sharing is to insert a low value resistor in series with each output. The problem with this approach is that load regulation is very poor if the resistors are made large enough to ensure adequate sharing.

A new technique for current sharing overcomes the load regulation problem and, as an added bonus, provides remote sensing capability not available in the standard 3-terminal regulators. This is a great advantage when the regulators must be mounted off-card with their outputs fed through a connector. Total cost of added components is less than 50¢.

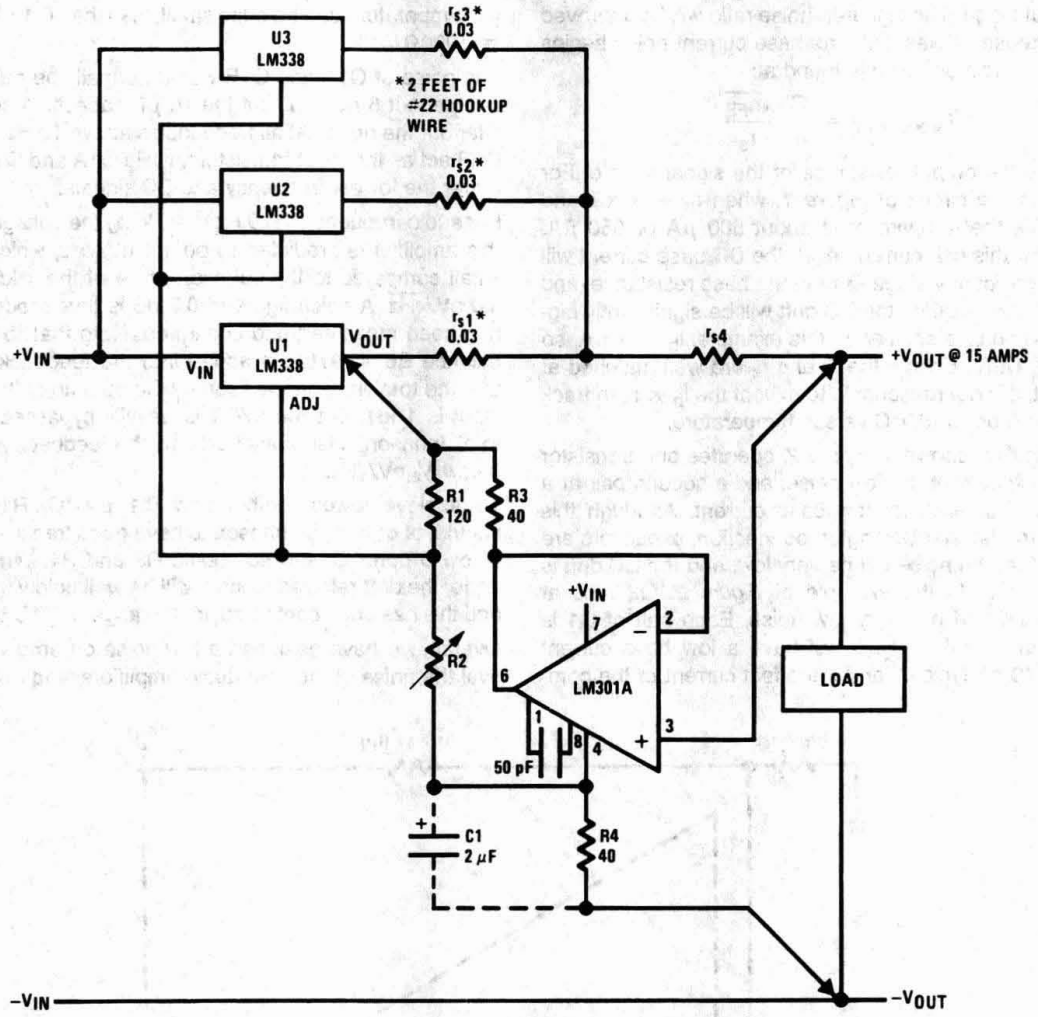
Figure 1 shows the new Kelvin sense scheme using the LM338 5 amp adjustable regulator. A1 forces a voltage drop across R3 equal to the voltage across the parasitic resistance, r_s. The current through R3 flows into the output of A1 and out the negative supply pin. This creates a voltage drop across R4 just equal to the voltage across r_s, cancelling the effect of r_s on load regulation. There is an error in V_{OUT} created by the quiescent current of A1, but for a 5V output, this error is only about 0.7%. Voltage loss across r_s must be limited to 300 mV to avoid current limiting in A1. If larger drops must be accommodated, R3 and R4 will have to be increased. C1 is necessary only if intermediate values of capacitance (2 μF–20 μF) are put directly across the load. Any of the positive adjustable regulators may be used in place of the LM338.



TL/H/8498–1

FIGURE 1

Figure 2 combines Kelvin sensing with paralleling, where the voltage loss across the current sharing resistors is corrected by the sensing connection. r_{S1} through r_{S3} are equal lengths of #22 gauge lead wire which act as ballasting resistors. These resistors can be kept small because LM338 adjustment pins are paralleled, forcing the outputs to track to within about 60 mV. r_{S4} consists of the parasitic resistance of any additional output lead plus connector loss. The total loss for r_{S4} may be up to 0.25V without loss of proper Kelvin sensing. Note that if U1 has the lowest reference voltage of the three regulators, full Kelvin sensing might not become effective until output current has increased above a threshold value of several amps. If this is undesirable, the adjustment pin of U1 may be connected to a 5Ω tap on R1, increasing its effective reference voltage by 50 mV. The current load for U1 would be 1.5 amps higher, however.



TL/H/8498–2

FIGURE 2

A Low-Noise Precision Op Amp

National Semiconductor
Linear Brief 52
Robert A. Pease

It is well known that the voltage noise of an operational amplifier can be decreased by increasing the emitter current of the input stage. The signal-to-noise ratio will be improved by the increase of bias, until the base current noise begins to dominate. The optimum is found at:

$$I_{e(optimum)} = \frac{KT}{q} \frac{\sqrt{h_{FE}}}{r_s}$$

where r_s is the output resistance of the signal source. For example, in the circuit of *Figure 1*, when r_s = 1 kΩ and h_{FE} = 500, the I_e optimum is about 500 μA or 560 μA. However, at this rich current level, the DC base current will cause a significant voltage error in the base resistance, and even after cancellation, the DC drift will be significantly bigger than when I_e is smaller. In this example, I_b = 1 μA, so $I_b \times r_s$ = 1 mV. Even if the I_b and r_s are well matched at each input, it is not reasonable to expect the $I_b \times r_s$ to track better than 5 or 10 μV/°C versus temperature.

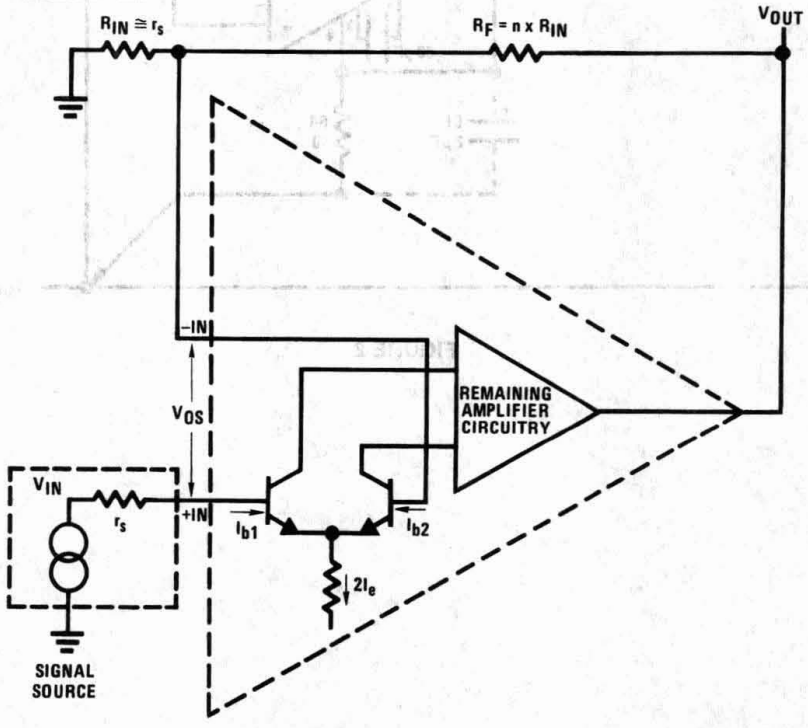
A new amplifier, shown in *Figure 2*, operates one transistor pair at a rich current, for low noise, and a second pair at a much leaner current, for low base current. Although this looks like the familiar Darlington connection, capacitors are added so that the noise will be very low, and the DC drift is very good, too. In the example of *Figure 2*, Q2 runs at I_e = 500 μA and has very low noise. Each half of Q1 is operated at 11 μA = I_e. It will have a low base current (20 nA to 40 nA typical), and the offset current of the composite op amp, $I_{b1} - I_{b2}$, will be very small, 1 nA or 2 nA. Thus, errors caused by bias current and offset current drift vs. temperature can be quite small, less than 0.1 μV/°C at r_s = 1000Ω.

The noise of Q1A and Q1B would normally be quite significant, about 6 nV/√Hz, but the 10 μF capacitors completely filter out the noise. At all frequencies above 10 Hz, Q2A and Q2B act as the input transistors, while Q1A and Q1B merely buffer the lowest frequency and DC signals.

For audio frequencies (20 Hz to 20 kHz) the voltage noise of this amplifier is predicted to be 1.4 nV/√Hz, which is quite small compared to the Johnson noise of the 1 kΩ source, 4.0 nV/√Hz. A noise figure of 0.7 dB is thus predicted, and has been measured and confirmed. Note that for best DC balance R6 = 976Ω is added into the feedback path, so that the total impedance seen by the op amp at its negative input is 1 kΩ. But the 976Ω is heavily bypassed, and the total Johnson noise contributed by the feedback network is below ½ nV/√Hz.

To achieve lowest drift, below 0.1 μV/°C, R1 and R2 should, of course, be chosen to have good tracking tempco, below 5 ppm/°C, and so should R3 and R4. When this is done, the drift referred to input will be well below 0.5 μV/°C, and this has been confirmed, in the range +10°C to +50°C.

Overall, we have designed a low-noise op amp which can rival the noise of the best audio amplifiers, and at the same



TL/H/8499–1

$$V_{OUT} \cong (n+1)V_{IN} + V_{OS} \times (n+1) + (I_{b2} - I_{b1}) \times r_s \times (n+1) + V_{noise} \times (n+1) + i_{noise} \times (r_s + R_{IN}) \times (n+1)$$

FIGURE 1. Conventional Low-Noise Operational Amplifier

time exhibits drift characteristics of the best low-drift amplifiers. The amplifier has been used as a precision pre-amp (gain = 1000), and also as the output amplifier for a 20-bit DAC, where low drift and low noise are both important.

To optimize the circuit for other r_s levels, the emitter current for Q2 should be proportional to $1/\sqrt{r_s}$. The emitter current of Q1A should be about ten times the base current of Q2A. The base current of the output op amp should be no more than 1/1000 of the emitter current of Q2. The values of R1 and R2 should be the same as R7.

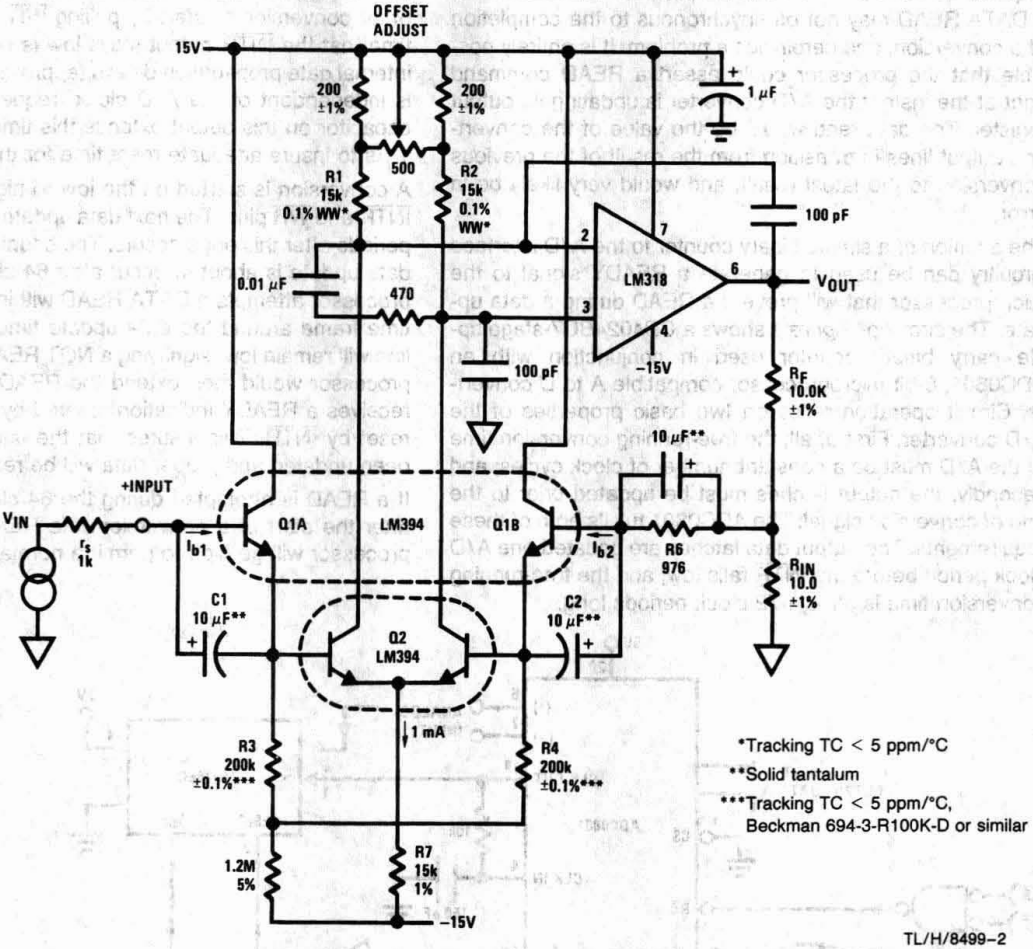
Various formulae for noise:

Voltage noise of a transistor, per $\sqrt{Hz}$, $e_n = KT\sqrt{\frac{2}{qI_C}}$

Current noise of a transistor, per $\sqrt{Hz}$, $i_n = \sqrt{\frac{2qI_C}{h_{FE}}}$

Voltage noise of a resistor, per $\sqrt{Hz}$, $e_n = \sqrt{4\,KTR_s}$

For a more complete analysis of low-noise amplifiers, see AN-222, "Super Matched Bipolar Transistor Pair Sets New Standards for Drift and Noise", Carl T. Nelson.



TL/H/8499–2

FIGURE 2. New Low-Noise Precision Operational Amplifier as Gain-of-1000 Pre-Amp

μP Interface for a Free-Running A/D Allows Asynchronous Reads

National Semiconductor
Linear Brief 53
Tim Regan

In many data acquisition applications it is necessary to have an A to D converter operate as its maximum conversion rate. The controlling microprocessor would then be able to read the most current input data at *any* point in time as required by software. To minimize program execution time, a DATA READ may not be snychronous to the completion of a conversion, and herein lies a problem. It is entirely possible that the processor could assert a READ command right at the instant the A/D converter is updating its output register. The data read would be the value of the converter's output lines in transition from the result of the previous conversion to the latest result, and would very likely be in error.

The addition of a simple binary counter to the A/D interface circuitry can be used to generate a READY signal to the microprocessor that will prevent a READ during a data update. The circuit of *Figure 1* shows a CD4024BC7-stage ripple carry binary counter used in conjunction with an ADC0801, 8-bit microprocessor compatible A to D converter. Circuit operation relies on two basic properties of the A/D converter. First of all, the free-running conversion time of the A/D must be a constant number of clock cycles; and secondly, the output latches must be updated prior to the end of conversion signal. The ADC0801 fulfills both of these requirements. The output data latches are updated one A/D clock period before the $\overline{INTR}$ falls low, and the free-running conversion time is always 72 clock periods long.

As part of the system power-up initializaton sequence, a logic low must be temporarily applied to the $\overline{SYSTEM\ RESET}$ input to the A/D to force the converter to start. At the end of a conversion, the $\overline{INTR}$ output goes low, and both resets the counter outputs to all zeros and signals another conversion to start by pulling $\overline{WR}$ low. The length of time that the $\overline{INTR}$ output stays low is normally only a few internal gate propagation delays (approximately 300 ns) and is independent of the A/D clock frequency. The 1000 pF capacitor on this output extends this time to approximately 1 μs to insure adequate reset time for the counter.

A conversion is started on the low to high transition of the $\overline{INTR}$ and $\overline{WR}$ pins. The next data update will occur 71 clock periods after this edge occurs. The counter will signal that a data update is about to occur after 64 clock periods. If the processor attempts a DATA READ within an 8 clock period time frame around the data update time, its READY input line will remain low, signifying a NOT READY condition. The processor would then extend the READ cycle time until it receives a READY indication created by the counter being reset by $\overline{INTR}$. This insures that the latches have already been updated and proper data will be read.

If a READ is attempted during the 64 clock period interval after the start of a conversion, the READY IN line to the processor will go high to permit a normal READ cycle, and

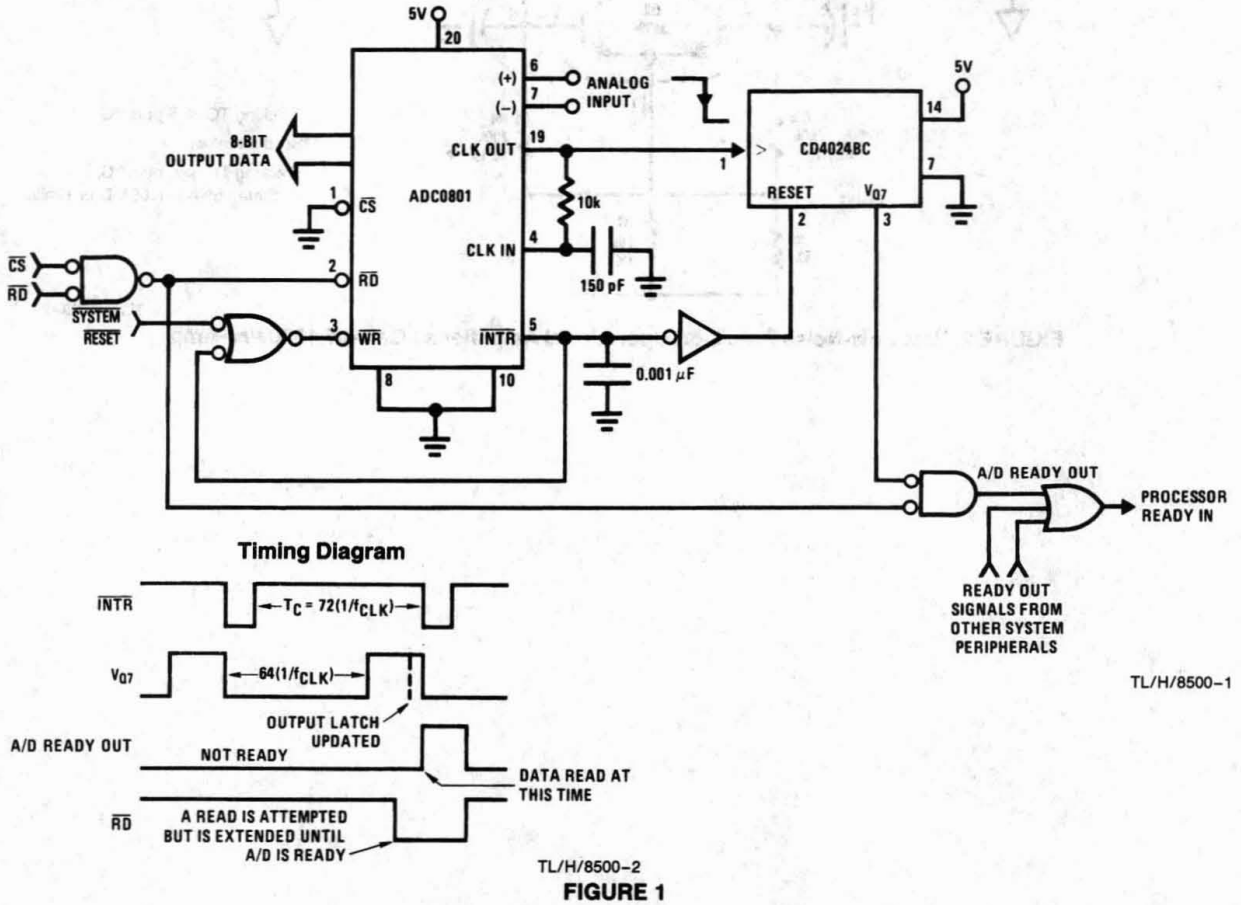
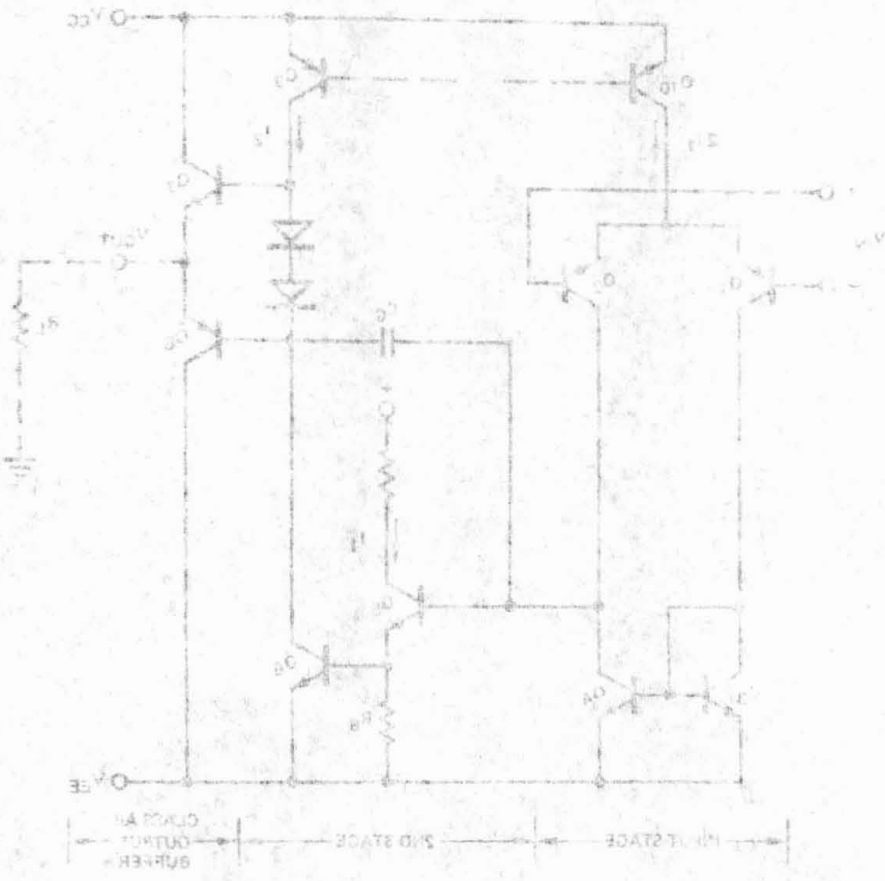


FIGURE 1

the data output by the A/D will be the result of the previous conversion. The processor READY IN logic, as shown, requires that all system devices that may need special READ or WRITE timing provide a NOT READY (a Logic 0 on their READY OUT lines) indication until selected to be read from or written to.

The chance of having the processor extend its READ cycle time is 1 in 9 (8 clock periods out of 72) and the maximum length of time a READ would be extended is 8 A/D clock periods. These two timing considerations are insignificant trade-offs to take to insure that proper A/D data is always read.



The Monolithic Operational Amplifier: A Tutorial Study

National Semiconductor
Appendix A

Invited Paper—
IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6

Abstract—A study is made of the integrated circuit operational amplifier (IC op amp) to explain details of its behavior in a simplified and understandable manner. Included are analyses of thermal feedback effects on gain, basic relationships for bandwidth and slew rate, and a discussion of pole-splitting frequency compensation. Sources of second-order bandlimiting in the amplifier are also identified and some approaches to speed and bandwidth improvement are developed. Brief sections are included on new JFET—bipolar circuitry and die area reduction techniques using transconductance reduction.

1.0 INTRODUCTION

The integrated circuit operational amplifier (IC op amp) is the most widely used of all linear circuits in production today. Over one hundred million of the devices will be sold in 1974 alone, and production costs are falling low enough so that op amps find applications in virtually every analog area. Despite this wide usage, however, many of the basic performance characteristics of the op amp are poorly understood.

It is the intent of this study to develop an understanding for op amp behavior in as direct and intuitive a manner as possible. This is done by using a variety of simplified circuit models which can be analyzed in some cases by inspection, or in others by writing just a few equations. These simplified models are generally developed from the single representative op amp configuration shown in *Figures 1* and *2*.

The rationale for starting with the particular circuit of *Figure 1* is based on the following: this circuit contains, in simplified form, all of the important elements of the most commonly used integrated op amps. It consists essentially of two voltage gain stages, an input differential amp and a common emitter second stage, followed by a class-AB output emitter follower which provides low impedance drive to the load. The two interstages are frequency compensated by a single small "pole-splitting" capacitor (see below) which is usually included on the op amp chip. In most respects this circuit is directly equivalent to the general purpose LM101 [1], μA 741 [2], and the newer dual and quad op amps [3], so the results of our study relate directly to these devices. Even for

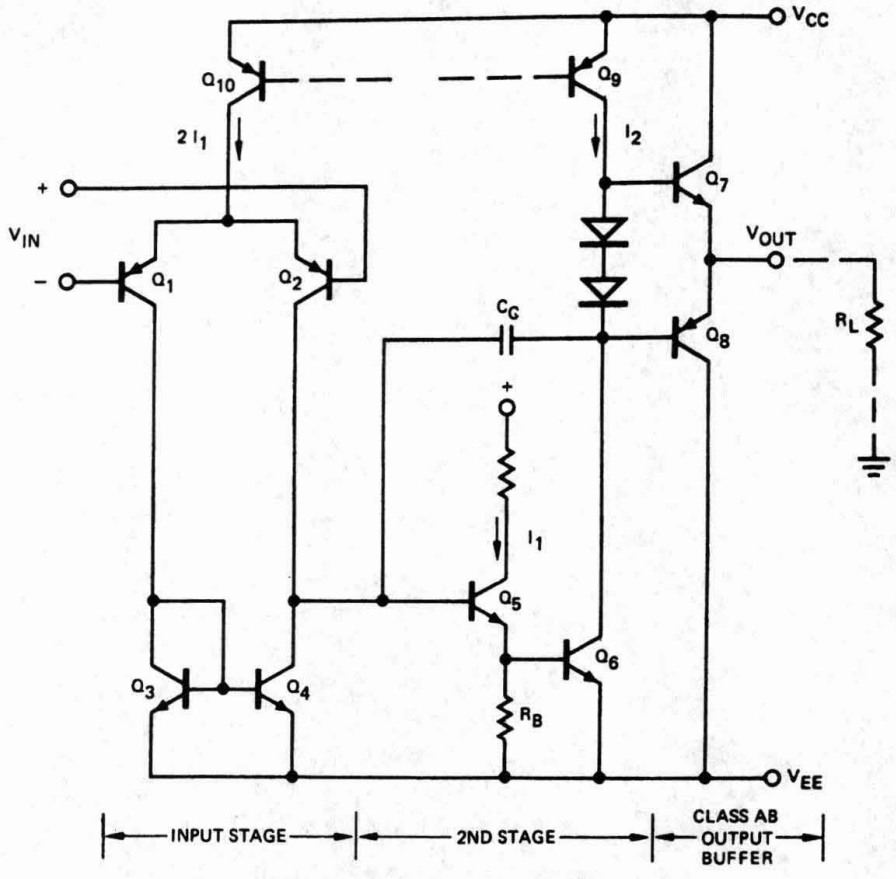


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FIGURE 1. Basic two-stage IC op amp used for study. Minimal modifications used in actual IC are shown in *Figure 2.*

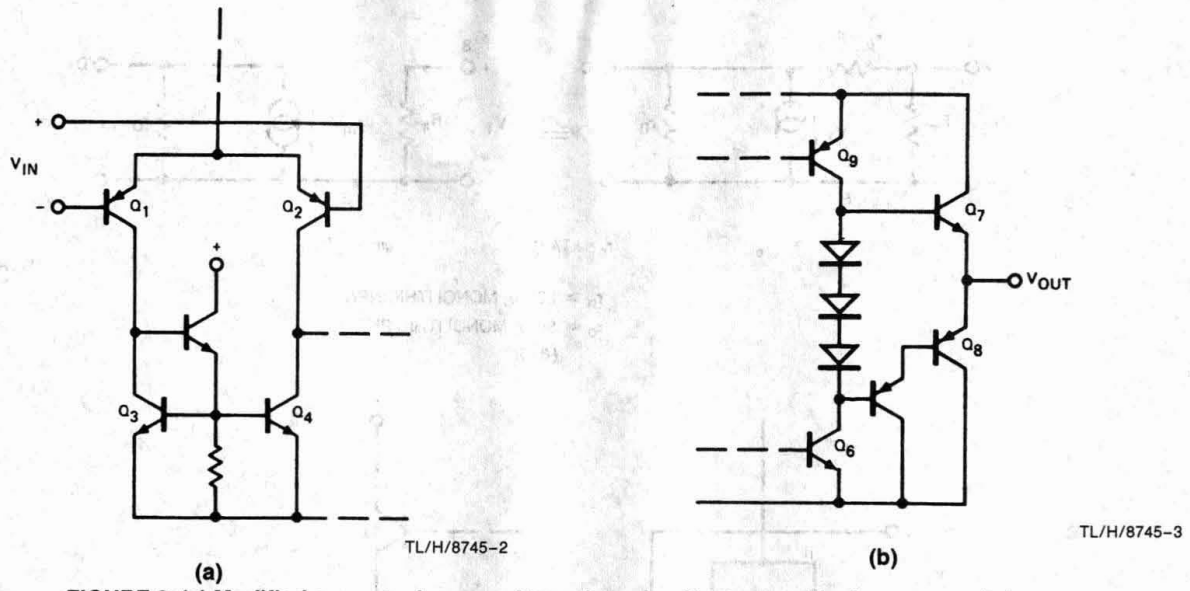

FIGURE 2. (a) Modified current mirror used to reduce dc offset caused by base currents in Q3 and Q4 in *Figure 1.* (b) Darlington p-n-p output stage needed to minimize gain fall-off when sinking large output currents. This is needed to offset the rapid β drop which occurs in IC p-n-p's.

more exotic designs, such as wide-band amps using feed-forward [4], [5], or the new FET input circuits [6], the basic analysis approaches still apply, and performance details can be accurately predicted. It has also been found that a good understanding of the limitations of the circuit in *Figure 1* provides a reasonable starting point from which higher performance amplifiers can be developed.

The study begins in Section 2, with an analysis of dc and low frequency gain. It is shown that the gain is typically limited by thermal feedback rather than electrical characteristics. A highly simplified thermal analysis is made, resulting in a gain equation containing only the maximum output current of the op amp and a thermal feedback constant.

The next three sections apply first-order models to the calculation of small-signal high frequency and large-signal slewing characteristics. Results obtained include an accurate equation for gain-bandwidth product, a general expression for slew rate, some important relationships between slew rate and bandwidth, and a solution for voltage follower behavior in a slewing mode. Due to the simplicity of the results in these sections, they are very useful to designers in the development of new amplifier circuits.

Section 6 applies more accurate models to the calculation of important second-order effects. An effort is made in this section to isolate all of the major contributors to bandlimiting in the modern amp.

In the final section, some techniques for reduction of op amp die size are considered. Transconductance reduction and layout techniques are discussed which lead to fabrication of an extremely compact op amp cell. An example yielding 8000 possible op amps per 3-in. wafer is given.

2.0 GAIN AT DC AND LOW FREQUENCIES

A. The Electronic Gain

The electronic voltage gain will first be calculated at dc using the circuit of *Figure 1.* This calculation becomes straightforward if we employ the simplified transistor model shown in *Figure 3(a).* The resulting gain from *Figure 3(b)* is

$$A_v(0) = \frac{v_{out}}{v_{in}} \cong \frac{g_{m1}\beta_5\beta_6\beta_7 R_L}{1 + r_{i2}/r_{01}'} \quad (1)$$

where

$$r_{i2} \cong \beta_5(r_{e5} + \beta_6 r_{e6})$$
$$r_{01}' \cong r_{04}//r_{02}.$$

It has been assumed that

$$\beta_7 R_L < r_{06}//r_{09},\ g_{m1} = g_{m2},\ \beta_7 = \beta_8.$$

The numerical subscripts relate parameters to transistor Q numbers (i.e., r_{e5} is r_e of Q_5, β_6 is β_0 pf Q_6, etc.). It has also been assumed that the current mirror transistors Q_3 and Q_4 have α's of unity, and the usually small loading of R_B has been ignored. Despite the several assumptions made in obtaining this simple form for (1), its accuracy is quite adequate for our needs.

An examination of (1) confirms the way in which the amplifier operates: the input pair and current mirror convert the input voltage to a current $g_{m1}V_{in}$ which drives the base of the second stage. Transistors Q_5, Q_6, and Q_7 simply multiply this current by β^3 and supply it to the load R_L. The finite output resistance of the first stage causes some loss when compared with second stage input resistance, as indicated by the term $1/(1 + r_{i2}/r_{01}')$. A numerical example will help our perspective: for the LM101A, $I_1 \cong 10\ \mu A$, $I_2 \cong 300\ \mu A$, $\beta_5 = \beta_6 \cong 150$, and $\beta_7 \cong 50$. From (1) and dc voltage gain with $R_L = 2\ k\Omega$ is

$$A_v(0) \cong 625{,}000 \quad (2)$$

The number predicted by (2) agrees well with that measured on a discrete breadboard of the LM101A, but is much higher than that observed on the integrated circuit. The reason for this is explained in the next section.

B. Thermal Feedback Effects on Gain

The typical IC op amp is capable of delivering powers of 50–100 mW to a load. In the process of delivering this power, the output stage of the amp internally dissipates similar power levels, which causes the temperature of the IC chip to rise in proportion to the output dissipated power. The silicon chip and the package to which it is bonded are good thermal conductors, so the whole chip tends to rise to the same temperature as the output stage. Despite this, small

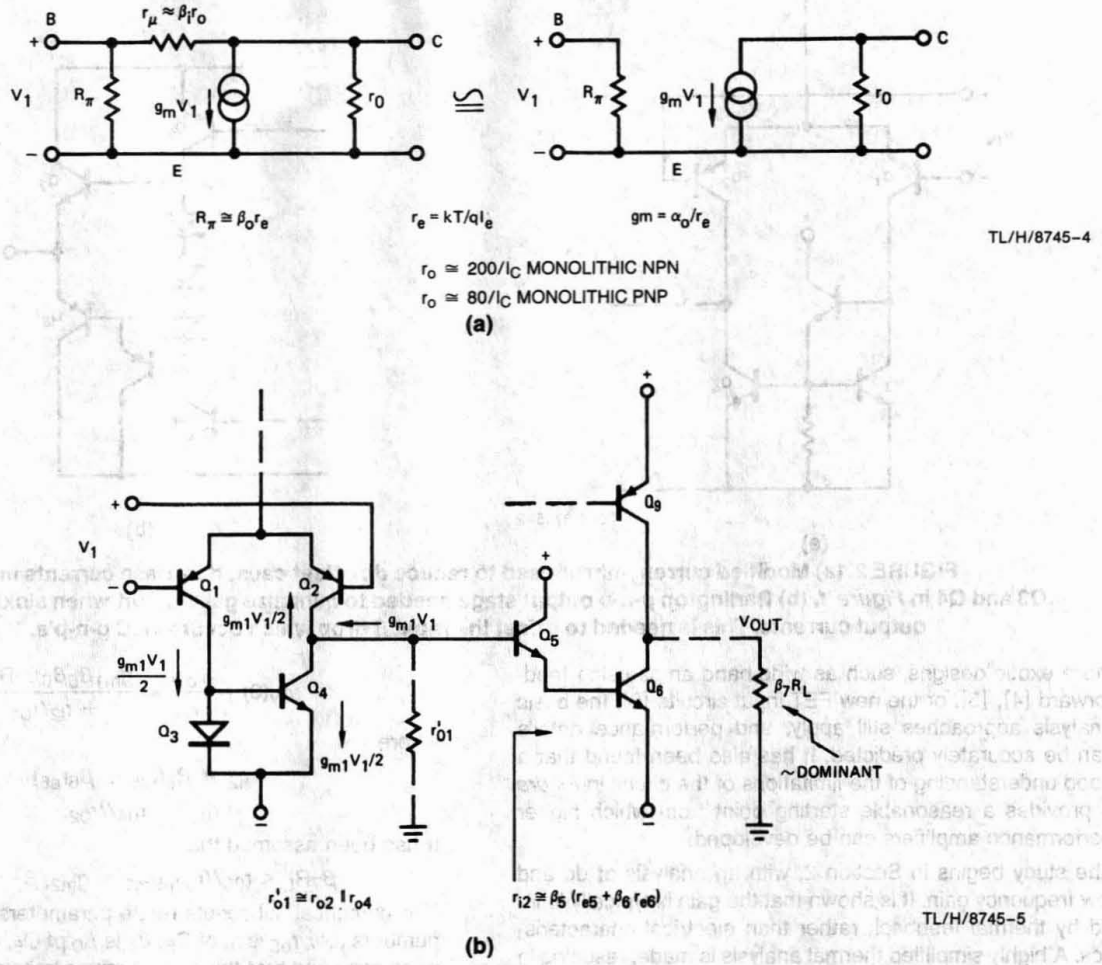

FIGURE 3. (a) Approximate π model for CE transistor at dc. Feedback element $r_\mu \cong \beta_4 r_o$ is ignored since this greatly simplifies hand calculations. The error caused is usually less than 10 percent because β_4, the intrinsic β under the emitter, is quite large. Base resistance r_x is also ignored for simplicity. (b) Circuit illustrating calculation of electronic gain for op amp of *Figure 1.* Consideration is given only to the fully loaded condition ($R_L \cong 2\ k\Omega$) where β_7 is falling (to about 50) due to high current density. Under this condition, the output resistance of Q6 and Q9 are nondominant.

temperature gradients from a few tenths to a few degrees centigrade develop across the chip with the output section being hotter than the rest. As illustrated in *Figure 4,* these temperature gradients appear across the input components of the op amp and induce an input voltage which is proportional to the output dissipated power.

To a first order, it can be assumed that the temperature difference $(T_2 - T_1)$ across a pair of matched and closely spaced components is given simply by

$$(T_2 - T_1) \cong \pm K_T P_d \quad °C \tag{3}$$

where

P_d power dissipated in the output circuit,

K_T a constant with dimensions of °C/W.

The plus/minus sign is needed because the direction of the thermal gradient is unknown. In fact, the sign may reverse polarity during the output swing as the dominant source of heat shifts from one transistor to another. If the dominant input components consist of the differential transistor pair of *Figure 4,* the thermally induced input voltage V_{int} can be calculated as

$$V_{int} \cong \pm K_T P_d (2 \times 10^{-3})$$
$$\cong \pm \gamma_T P_d \tag{4}$$

where $\gamma_T = K_T(2 \times 10^{-3})$ V/W, since the transistor emitter-base drops change about -2 mV/°C.

For a thermally well designed IC op amp, in which the power output devices are made to approximate either a point or a line source and the input components are placed on the resulting isothermal lines (see below and *Figure 8*), typical values measured for K_T are

$$K_T \approx 0.3°C/W \tag{5}$$

in a TO-5 package.

The dissipated power in the class-AB output stage P_d is written by inspection of *Figure 4*:

$$P_d = \frac{V_0 V_s - V_0^2}{R_L} \tag{6}$$

where

$V_s = +V_{cc}$ when $V_0 > 0$

$V_s = -V_{ee}$ when $V_0 < 0$.

A plot of (6) is *Figure 5* resembles the well-known class-AB dissipation characteristics, with zero dissipation occurring

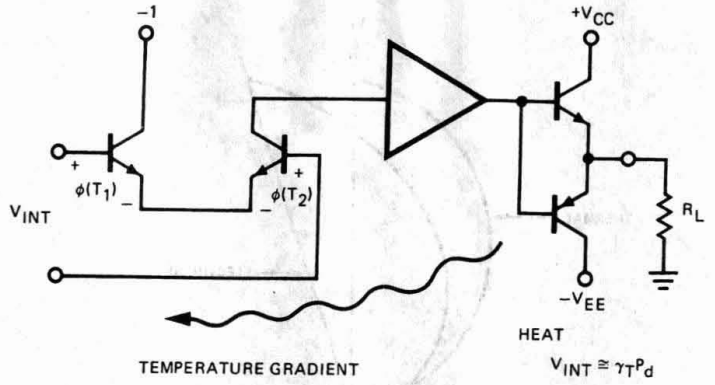

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FIGURE 4. Simple model illustrating thermal feedback in an IC op amp having a single dominant source of self-heat, the output stage. The constant $\gamma_T \cong 0.6$ mV/W and P_d is power dissipated in the output. For simplicity, we ignore input drift due to uniform heating of the package. This effect can be significant if the input stage drift is not low, see [7].

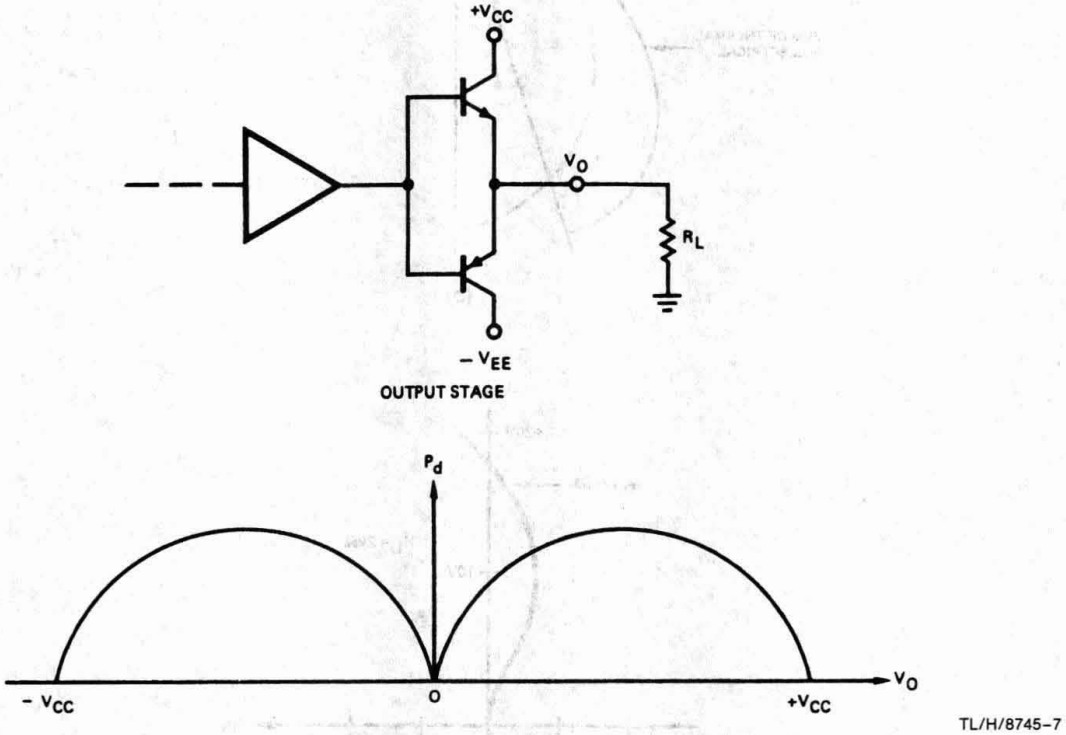

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FIGURE 5. Simple class-B output stage and plot of power dissipated in the stage, P_d, assuming device can swing to the power supplies. Equation (6) gives an expression for the plot.

for $V_0 = 0, +V_{cc}, -V_{ee}$. Dissipation peaks occur for $V_0 = +V_{cc}/2$ and $-V_{ee}/2$. Note also from (4) that the thermally induced input voltage V_{int} has this same double-humped shape since it is just equal to a constant times P_d at dc.

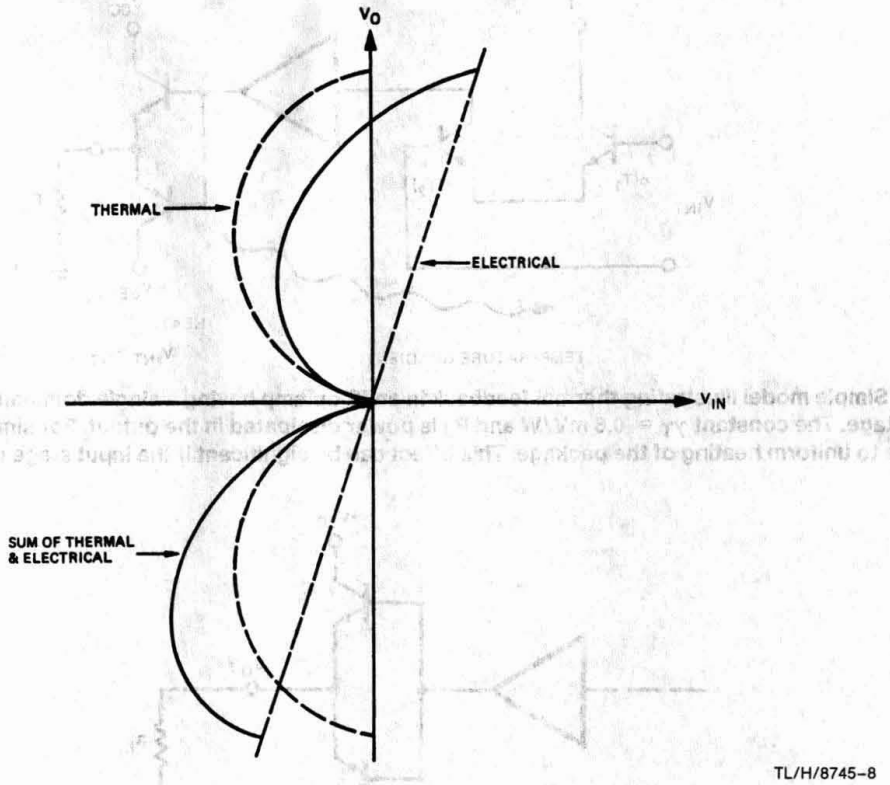
Now examine *Figures 6(a)* and *(b)* which are curves of open-loop V_0 versus V_{in} for the IC op amp. Note first that the overall curve can be visualized to be made up of two components: a) a normal straight line electrical gain curve of the sort expected from (1) and b) a double-humped curve similar to that of *Figure 5*. Further, note that the gain characteristic has either positive or negative slope depending on the value of output voltage. This means that the thermal feedback causes the open-loop gain of the feedback amplifier to change phase by 180°, apparently causing negative feedback to become positive feedback. If this is really true, the question arises: which input should be used as the inverting one for feedback? Further, is there any way to close the amplifier and be sure it will not find an unstable operating point and latch to one of the power supplies?

The answers to these questions can be found by studying a simple model of the op amp under closed-loop conditions, including the effects of thermal coupling. As shown in *Figure 7*, the thermal coupling can be visualized as just an additional feedback path which acts in parallel with the normal electrical feedback. Noting that the electrical form of the thermal feedback factor is [see (4) and (6)]

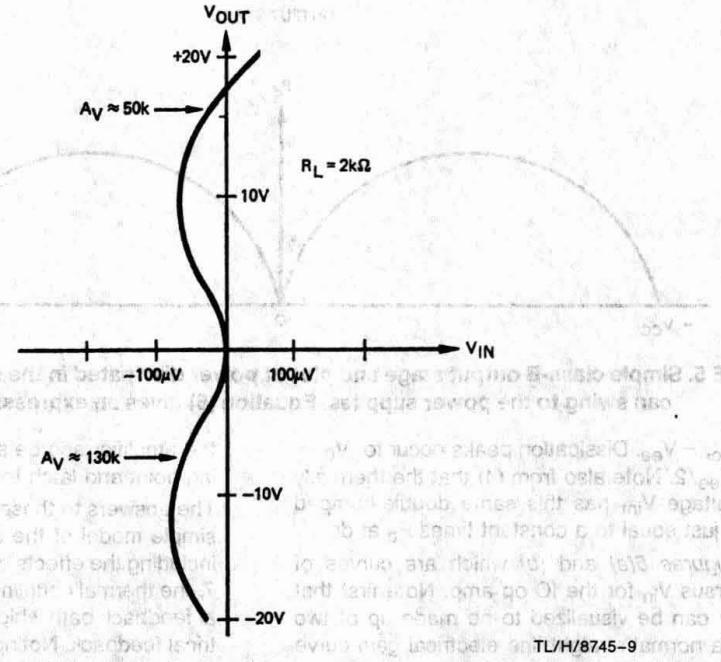
$$\beta_T = \frac{\partial V_{int}}{\partial V_0} = \pm \frac{\gamma_T}{R_L}(V_s - 2V_0). \qquad (7)$$

The closed-loop gain, including thermal feedback is

$$A_V(0) = \frac{\mu}{1 + \mu(\beta_e \pm \beta_T)} \qquad (8)$$



(a)



(b)

FIGURE 6. (a) Idealized dc transfer curve for an IC op amp showing its electrical and thermal components. (b) Experimental open-loop transfer curve for a representative op amp (LM101).

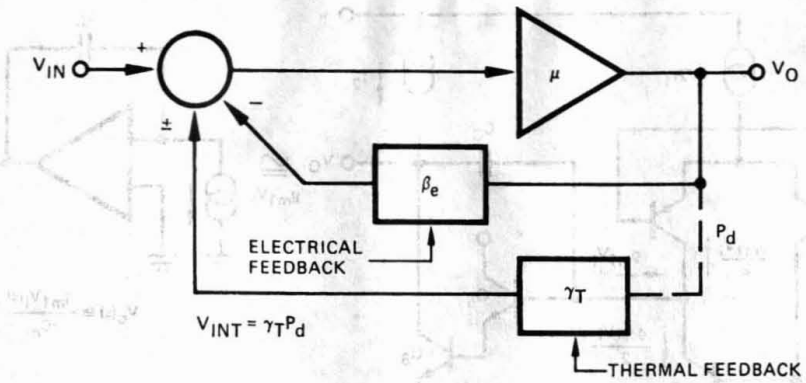


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FIGURE 7. Diagram used to calculate closed-loop gain with thermal feedback.

where μ is the open-loop gain in the absence of thermal feedback [(1)] and β_e is the applied electrical feedback as in *Figure 7.* Inspection of (8) confirms that as long as there is sufficient electrical feedback to swamp the thermal feedback (i.e., $\beta_e > \beta_T$), the amplifier will behave as a normal closed-loop device with characteristics determined principally by the electrical feedback (i.e., $A_V(0) \cong 1/\beta_e$). On the other hand, if β_e is small or nonexistant, the thermal term in (8) may dominate, giving an apparent open-loop gain characteristic determined by the thermal feedback factor β_T. Letting $\beta_e = 0$ and combining (7) and (8), $A_V(0)$ becomes

$$A_V(0) = \frac{\mu}{1 \pm \frac{\mu\gamma_T}{R_L}(V_s - 2V_0)}. \quad (9)$$

Recalling from (6) that V_0 ranges between 0 and V_S, we note that the incremental thermal feedback is greatest when $V_0 = 0$ or V_s, and it is at these points that the thermally limited gain is smallest. To use the amplifier in a predictable manner, one must always apply enough electrical feedback to reduce the gain below this minimum thermal gain. Thus, a *maximum usable gain* can be defined as that approximately equal to the value of (9) with $V_0 = 0$ or V_s which is

$$A_V(0)|_{max} \cong \frac{R_L}{\gamma_T V_S} \quad (10)$$

or

$$A_V(0)|_{max} \cong \frac{1}{\gamma_T I_{max}}. \quad (11)$$

It was assumed in (10) and (11) that thermal feedback dominates over the open-loop electrical gain, μ. Finally, in (11) a maximum current was defined $I_{max} = V_S/R_L$ as the maximum current which would flow if the amplifier output could swing all the way to the supplies.

Equation (11) is a strikingly simple and quite general result which can be used to predict the expected maximum usable gain for an amplifier if we know only the maximum output current and the thermal feedback constant γ_T.

Recall that typically $K_T \cong 0.3°C/W$ and $\gamma_T = (2 \times 10^{-3})$ $K_T \cong 0.6$ mV/W. Consider, as an example, the standard IC op amp operating with power supplies of $V_S = \pm 15V$ and a minimum load of 2 kΩ, which gives $I_{max} = 15V/2\,k\Omega = 7.5$ mA. Then, from (11), the maximum thermally limited gain is about:

$$A_V(0)|_{max} \cong 1/(0.6 \times 10^{-3})(7.5 \times 10^{-3}) \cong 220{,}000. \quad (12)$$

Comparing (2) and (12), it is apparent that the thermal characteristics dominate over the electrical ones if the minimum load resistor is used. For loads of 6 kΩ or more, the electrical characteristics should begin to dominate if thermal feedback from sources other than the output stage is negligible. It should be noted also that, in some high speed, high drain op amps, thermal feedback from the second stage dominates when there is no load.

As a second example, consider the so-called "power op amp" or high gain audio amp which suffers from the same thermal limitations just discussed. For a device which can deliver 1W into a 16Ω load, the peak output current and voltage are 350 mA and 5.7V. Typically, a supply voltage of about 16V is needed to allow for the swing loss in the IC output stage. I_{max} is then 8V/16Ω or 0.5A. If the device is in a TO-5 package γ_T is approximately 0.6 mV/W, so from (11) the maximum usable dc gain is

$$A_V(0)|_{max} \cong \frac{1}{(0.6 \times 10^{-3})(0.5)} \cong 3300. \quad (13)$$

This is quite low compared with electrical gains of, say, 100,000 which are easily obtainable. The situation can be improved considerably by using a large die to separate the power devices from the inputs and carefully placing the inputs on constant temperature (isothermal) lines as illustrated in *Figure 8.* If one also uses a power package with a heavy copper base, γ_T's as low as 50 μV/W have been observed. For example, a well-designed 5W amplifier driving an 8Ω load and using a 24V supply, would have a maximum gain of 13,000 in such a power package.

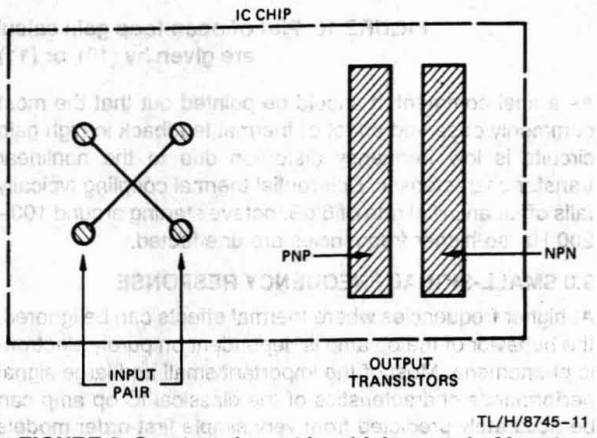

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FIGURE 8. One type layout in which a quad of input transistors is cross connected to reduce effect of nonuniform thermal gradients. The output transistors use distributed stripe geometrics to generate predictable isothermal lines.

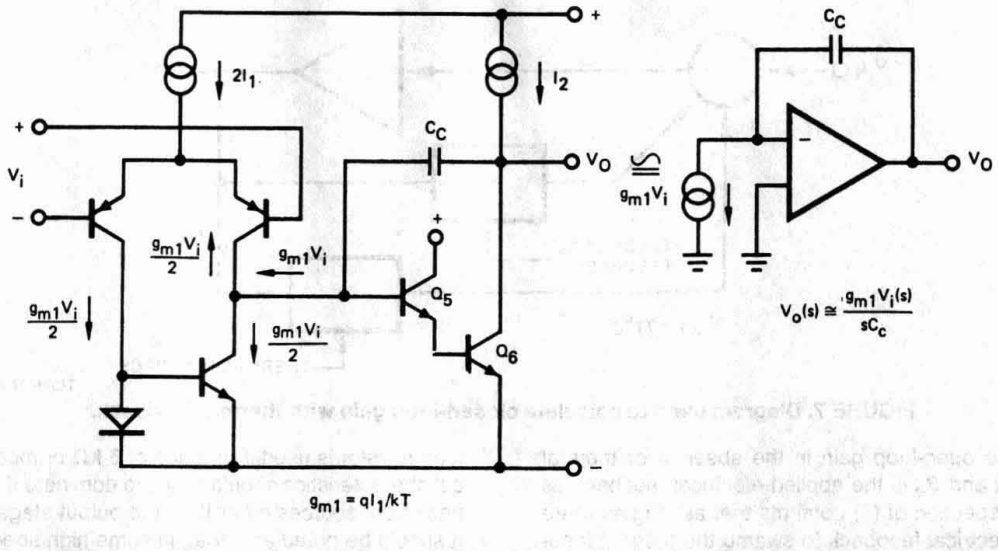

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FIGURE 9. First-order model of op amp used to calculate small signal high frequency gain. At frequencies of interest the input impedance of the second stage becomes low compared to first stage output impedance due to C_c feedback. Because of this, first stage output impedance can be assumed infinite, with no loss in accuracy.

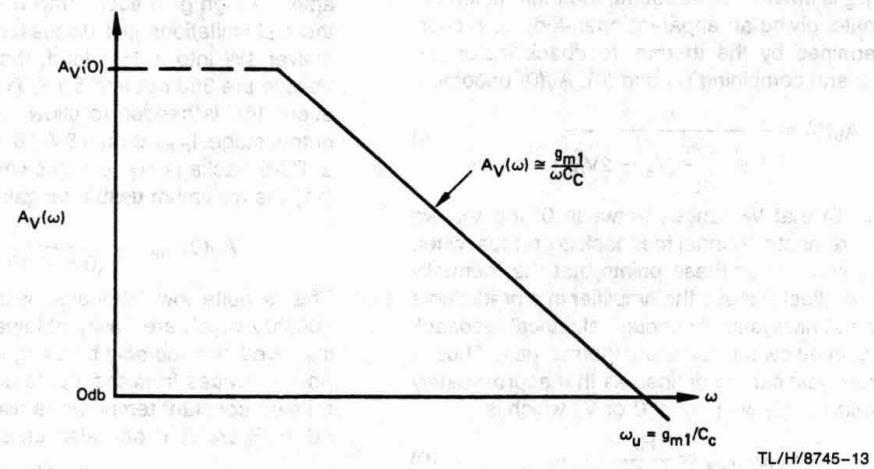

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FIGURE 10. Plot of open-loop gain calculated from model in *Figure 9*. The dc and LF gain are given by (10), or (11) if thermal feedback dominates.

As a final comment, it should be pointed out that the most commonly observed effect of thermal feedback in high gain circuits is low frequency distortion due to the nonlinear transfer characteristic. Differential thermal coupling typically falls off at an initial rate of 6 dB/octave starting around 100–200 Hz, so higher frequencies are uneffected.

3.0 SMALL-SIGNAL FREQUENCY RESPONSE

At higher frequencies where thermal effects can be ignored, the behavior of the op amp is dependent on purely electronic phenomena. Most of the important small and large signal performance characteristics of the classical IC op amp can be accurately predicted from very simple first-order models for the amplifier in *Figure 1* (8). The small-signal model that is used assumes that the input differential amplifier and current mirror can be replaced by a frequency independent voltage controlled current source, see *Figure 9*. The second stage consisting essentially of transistors Q_5 and Q_6, and the current source load, is modeled as an ideal frequency independent amplifier block with a feedback or "integrating capacitor" identical to the compensation capacitor, c_c. The output stage is assumed to have unity voltage gain and is ignored in our calculations. From *Figure 9*, the high frequency gain is calculated by inspection:

$$A_V(\omega) = \left|\frac{V_0}{V_i}(s)\right| = \left|\frac{g_{m1}}{sC_c}\right| = \frac{g_{m1}}{\omega C_c} \qquad (14)$$

where dc and low frequency behavior have not been included since this was evaluated in the last section. *Figure 10* is a plot of the gain magnitude as predicted by (14). From this figure it is a simple matter to calculate the open-loop unity gain frequency ω_u, which is also the gain-bandwidth product for the op amp under closed-loop conditions:

$$\omega_u = \frac{g_{m1}}{C_c}. \qquad (15)$$

In a practical amplifier, ω_u is set to a low enough frequency (by choosing a large C_c) so that negligible excess phase over the 90° due to C_c has built up. There are numerous contributors to excess phase including low f_t p-n-p's, stray capacitances, nondominant second stage poles, etc.

These are discussed in more detail in a later section, but for now suffice it to say that, in the simple IC op amp, $\omega_u/2\pi$ is limited to about 1 MHz. As a simple test of (15), the LM101 or the μA741 has a first stage bias current I_1 of 10 μA per side, and a compensation capacitor for unity gain operation, C_c, of 30 pF. These amplifiers each have a first stage g_m which is half that of the simple differential amplifer in *Figure 1* so $g_{m1} = qI_1/2kT$. Equation (15) then predicts a unity gain corner of

$$f_u = \frac{\omega_u}{2\pi} = \frac{g_{m1}}{2\pi C_c} = \frac{(0.192 \times 10^{-3})}{2\pi(30 \times 10^{-12})} = 1.02 \text{ MHz} \quad (16)$$

which agrees closely with the measured values.

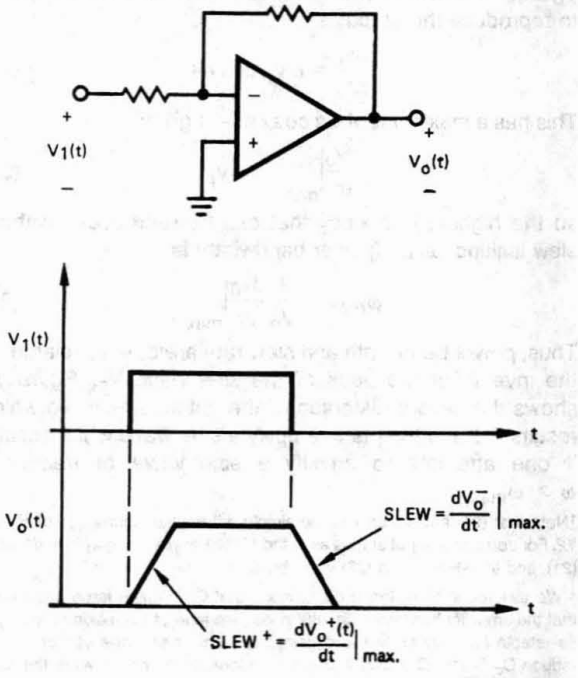

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FIGURE 11. Large signal "slewing" response observed if the input is overdriven.

4.0 SLEW RATE AND SOME SPECIAL LIMITS

A. A General Limit on Slew Rate

If an op amp is overdriven by a large-signal pulse or square wave having a fast enough rise time, the output does not follow the input immediately. Instead, it ramps or "slews" at some limiting rate determined by internal currents and capacitances, as illustrated in *Figure 11.* The magnitude of input voltage required to make the amplifier reach its maximum slew rate varies, depending on the type of input stage used. For an op amp with a simple input differential amp, an input of about 60 mV will cause the output to slew at 90 percent of its maximum rate, while a μA741, which has half the input g_m, requires 120 mV. High speed amplifiers such as the LM118 or a FET-input circuit require much greater overdrive, with 1–3V being common. The reasons for these overdrive requirements will become clear below.

An adequate model to calculate slew limits for the representative op amp in the inverting mode is shown in *Figure 12,* where the only important assumption made is that $I_2 \geq 2I_1$ in *Figure 1.* This condition always holds in a well-designed op amp. (If one lets I_2 be less than $2I_1$, the slew is limited by I_2 rather than I_1, which results in lower speed than is otherwise possible.) *Figure 12* requires some modification for noninverting operation, and we will study this later.

The limiting slew rate is now calculated from *Fig. 12.* Letting the input voltage be large enough to fully switch the input differential amp, we see that all of the first stage tail current $2I_1$ is simply diverted into the integrator consisting of A and C_c. The resulting slew rate is then:

$$\text{slew rate} = \left.\frac{dv_0}{dt}\right|_{max} = \frac{i_c(t)}{C_c}. \quad (17)$$

Noting that $i_c(t)$ is a constant $2I_1$, this becomes

$$\left.\frac{dv_0}{dt}\right|_{max} = \frac{2I_1}{C_c}. \quad (18)$$

As a check of this result, recall that the μA741 has $I_1 = 10$ μA and $C_1 = 30$ pF, so we calculate:

$$\left.\frac{dv_0}{dt}\right|_{max} = \frac{2 \times 10^{-5}}{30 \times 10^{-12}} = 0.67\frac{V}{\mu s} \quad (19)$$

which agrees with measured values.

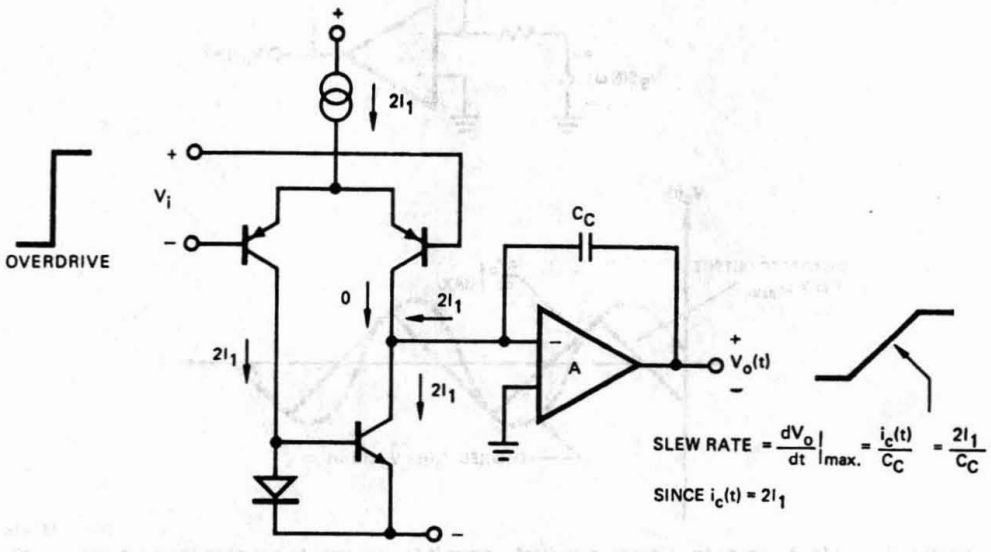

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FIGURE 12. Model used to calculate slew rate for the amp of *Figure 1* in the inverting mode. For simplicity, all transistor α's are assumed equal to unity, although results are essentially independent of α. An identical slew rate can be calculated for a negative-going output, obtained if the applied input polarity is reversed.

The large and small signal behavior of the op amp can be usefully related by combining (15) for ω_u with (18). The slew rate becomes

$$\left.\frac{dv_0}{dt}\right|_{max} = \frac{2\omega_u I_1}{g_{m1}}. \quad (20)$$

Equation (20) is a general and very useful relationship. It shows that, for a given unity-gain frequency, ω_u, the slew rate is determined entirely by just the ratio of first stage operating current to first stage transconductance, I_1/g_{m1}. Recall that ω_u is set at the point where excess phase begins to build up, and this point is determined largely by technology rather than circuit limitations. Thus, the only effective means available to the circuit designer for increasing op amp slew rate is to *decrease* the ratio of first stage transconductance to operating current, g_{m1}/I_1.

B. Slew Limiting for Simple Bipolar Input Stage

The significance of (20) is best seen by considering the specific case of a simple differential bipolar input as in *Figure 1*. For this circuit, the first stage transconductance (for $\alpha_1 = 1$) is[1]

$$g_{m1} = qI_1/kT \quad (21)$$

so that

$$\frac{g_{m1}}{I_1} = q/kT. \quad (22)$$

Using this in (20), the maximum bipolar slew rate is

$$\left.\frac{dv_0}{dt}\right|_{max} = 2\omega_u\frac{kT}{q}. \quad (23)$$

This provides us with the general (and somewhat dismal) conclusion that slew rate in an op amp with a simple bipolar input stage is dependent only upon the unity gain corner and fundamental constants. Slew rate can be increased only by incerasing the unity gain corner, which we have noted is generally difficult to do. As a demonstration of the severity of this limit, imagine an op amp using highly advanced technology and clever design, which might have a stable unity gain frequency of 100 MHz. Equation (23) predicts that the slew rate for this advanced device is only

$$\left.\frac{dv_0}{dt}\right|_{max} = 33\frac{V}{\mu s} \quad (24)$$

which is good, but hardly impressive when compared with the difficulty of building a 100 MHz op amp.[2] But, there are some ways to get around this limit as we shall see shortly.

C. Power Bandwidth

Our intuition regarding slew rate will be enhanced somewhat if we relate it to a term called "power bandwidth". Power bandwidth is defined as the maximum frequency at which full output swing (usually 10V peak) can be obtained without distortion. For a sinusoidal output voltage $v_0(t) = V_p \sin\omega t$, the rate of change of output, or slew rate, required to reproduce the output is

$$\frac{dv_0}{dt} = \omega V_p \cos\omega t. \quad (25)$$

This has a maximum when $\cos\omega t = 1$ giving

$$\left.\frac{dv_0}{dt}\right|_{max} = \omega V_p, \quad (26)$$

so the highest frequency that can be reproduced without slew limiting, ω_{max} (power bandwidth) is

$$\omega_{max} = \frac{1}{V_p}\left.\frac{dv_0}{dt}\right|_{max}. \quad (27)$$

Thus, power bandwidth and slew rate are directly related by the inverse of the peak of the sine wave V_p. *Figure 13* shows the severe distortion of the output sine wave which results if one attempts to amplify a sine wave which results if one attempts to amplify a sine wave of frequency $\omega > \omega_{max}$.

[1]Note that (21) applies only to the simple differential input stage of *Figure 12*. For compound input stages as in the LM101 or μA741, g_{m1} is half that in (21), and the slew rate in (23) is doubled.

[2] We assume in all of these calculations that C_c is made large enough so that the amplifier has less than 180° phase lag at ω_u, thus making the amplifier stable for unity closed-loop gain. For higher gains one can of course reduce C_c (if the IC allows external compensation) and increase the slew rate according to (18).

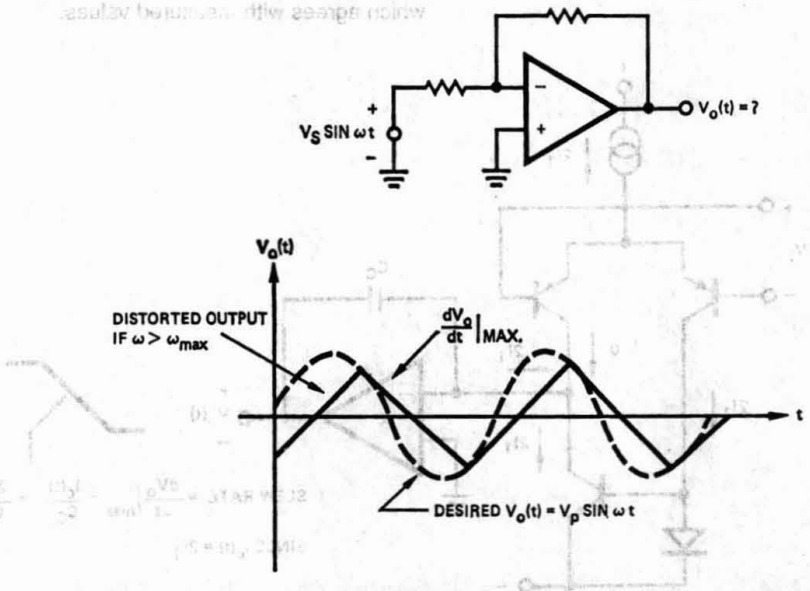

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FIGURE 13. Slew limiting effects on output sinewave that occur if frequency is greater than power bandwidth, ω_{max}. The onset of slew limiting occurs very suddenly as ω reaches ω_{max}. No distortion occurs below ω_{max}, while almost complete triangularization occurs at frequencies just slightly above ω_{max}.

Some numbers illustrate typical op amp limits. For a μA741 or LM101 having a maximum slew rate of 0.67V/μs, (27) gives a maximum frequency for an undistorted 10V peak output of

$$f_{max} = \frac{\omega_{max}}{2\pi} = 10.7 \text{ kHz}, \tag{28}$$

which is a quite modest frequency considering the much higher frequency small signal capabilities of these devices. Even the highly advanced 100 MHz amplifier considered above has a 10V power bandwidth of only 0.5 MHz, so it is apparent that a need exists for finding ways to improve slew rate.

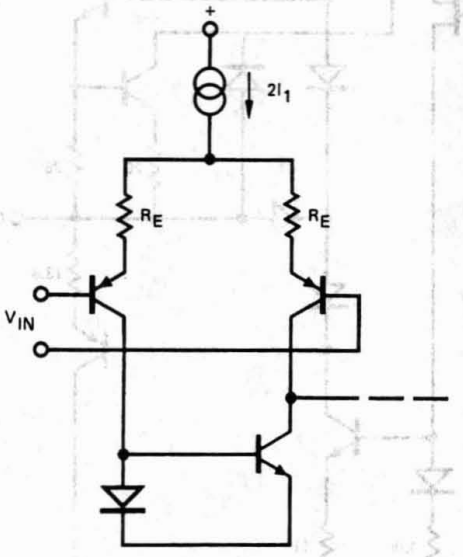

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FIGURE 14. Resistive degeneration used to provide slew rate enhancement according to (29).

D. Techniques for Increasing Slew Rate

1) Resistive Enhancement of the Bipolar Stage: Equation (20) indicates that slew rate can be improved if we reduce first stage g_{m1}/I_1. One of the most effective ways of doing this is shown in *Figure 14,* where simple resistive emitter degeneration has been added to the input differential amplifier (8). With this change, the g_{m1}/I_1 drops to

$$\frac{g_{m1}}{I_1} = \frac{38.5}{1 + T_E I_1/26 \text{ mV}} \tag{29}$$

at 25°C

The quantity g_{m1}/I_1 is seen to decrease rapidly with added R_E as soon as the voltage drop across R_E exceeds 26 mV. The LM118 is a good example of a bipolar amplifier which uses emitter degeneration to enhance slew rate [4]. This device uses emitter resistors to produce $R_E I_1$ = 500 mV, and has a unity gain corner of 16 MHz. Equations (20) and (29) then predict a maximum inverting slew rate of

$$\left.\frac{dv_0}{dt}\right|_{max} = 2\omega_u \frac{I_1}{g_{m1}} = \omega_u = 100\frac{V}{\mu s} \tag{30}$$

which is a twenty-fold improvement over a similar amplifier without emitter resistors.

A penalty is paid in using resistive slew enhancement, however. The two added emitter resistors must match extremely well or they add voltage offset and drift to the input. In the LM118, for example, the added emitter R's have values of 2.0 kΩ each and these contribute an input offset of 1 mV for each 4Ω (0.2 percent) of mismatch. The thermal noise of the resistors also unavoidably degrades noise performance.

2) Slew Rate in the FET Input Op Amp: The FET (JFET or MOSFET) has a considerably lower transconductance than a bipolar device operating at the same current. While this is normally considered a drawback of the FET, we note that this "poor" behavior is in fact highly desirable in applications to fast amplifiers. To illustrate, the drain current for a JFET in the "current saturation" region can be approximated by

$$I_D \cong I_{DSS}(V_{GS}/V_T - 1)^2 \tag{31}$$

where

I_{DSS} the drain current for $V_{GS} = 0$,

V_{GS} the gate source voltage having positive polarity for forward gate-diode bias,

V_T the threshold voltage having negative polarity for JFET's.

The small-signal transconductance is obtained from (31) as $g_m = \partial I_D/\partial V_G$. Dividing by I_D and simplifying, the ratio g_m/I_D for a JFET is

$$\frac{g_M}{I_D} \cong \frac{2}{(V_{GS} - V_T)} = \frac{2}{-V_T}\left[\frac{I_{DSS}}{I_D}\right]^{1/2}. \tag{32}$$

Maximum amplifier slew rate occurs for minimum g_m/I_D and, from (32), this occurs when I_D or V_{GS} is maximum. Normally it is impractical to forward bias the gate junction so a practical minimum occurs for (32) when $V_{GS} \cong 0V$ and $I_D \cong I_{DSS}$. Then

$$\left.\frac{g_m}{I_D}\right|_{min} \cong -2\frac{2}{V_T}. \tag{33}$$

Comparing (33) with the analogous bipolar expression, (22), we find from (20) that the JFET slew rate is greater than bipolar by the factor

$$\frac{\text{JFET slew}}{\text{bipolar slew}} \approx \frac{-V_T 2\omega_{uf}}{2kT/q\omega_{ub}} \tag{34}$$

where ω_{uf} and ω_{ub} are unity-gain bandwidths for JFET and bipolar amps, respectively. Typical JFET thresholds are around 2V ($V_T = -2V$), so for equal bandwidths (34) tells us that a JFET-input op amp is about forty times faster than a simple bipolar input. Further, if JFET's are properly substituted for the slow p-n-p's in a monolithic design, bandwidth improvements by at least a factor of ten are obtainable. JFET-input op amps, therefore, offer slew rate improvements by better than two orders of magnitude when compared with the conventional IC op amp. (Similar improvements are possible with MOSFET-input amplifiers.) This characteristic, coupled with picoamp input currents and reasonable offset and drift, make the JFET-input op amp a very desirable alternative to conventional bipolar designs.

As an example, *Figure 15,* illustrates one design for an op amp employing compatible p-channel JFET's on the same chip with the normal bipolar components. This circuit exhibits a unity gain corner of 10 MHz, a 33 V/μs slew rate, an input current of 10 pA and an offset voltage and drift of 3 mV amd 3 μV/°C [6]. Bandwidth and slew rate are thus improved over simple IC bipolar by factors of 10 and 100, respectively. At the same time input currents are smaller by about 10^3, and offset voltages and drifts are comparable to or better than slew enhanced bipolar circuits.

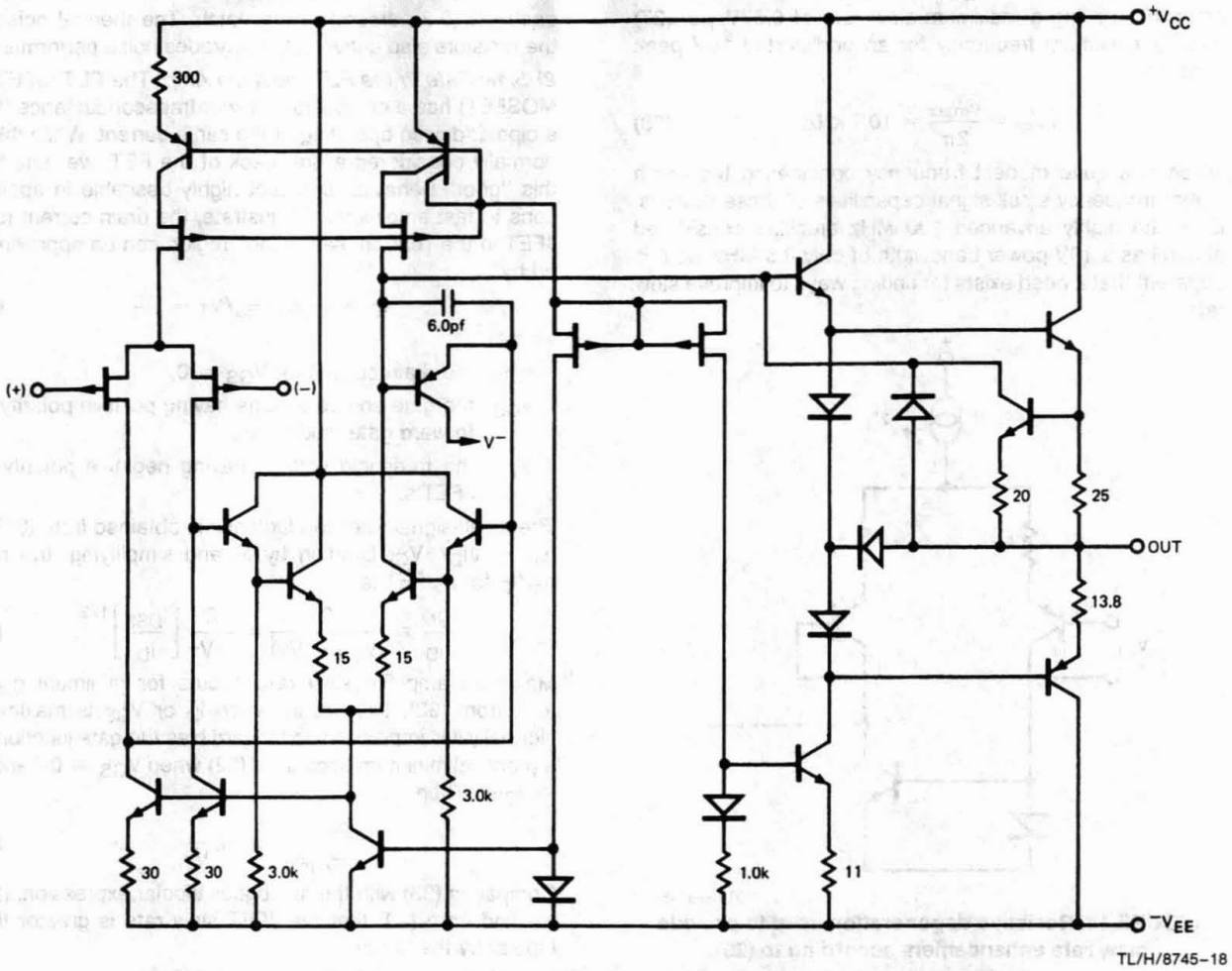

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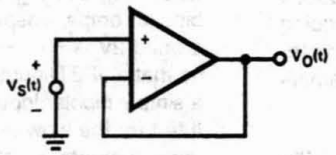
FIGURE 15. Monolithic operational amplifier employing compatible p-channel JFET's on the same chip with normal bipolar components.



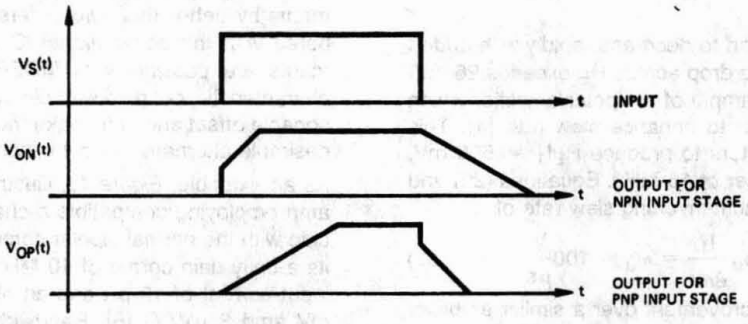


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FIGURE 16. Large signal response of the voltage follower. For an op amp with simple n-p-n input stage we get the waveform $v_{ON}(t)$, which exhibits a step slew "enhancement" on the positive going output, and a slew "degradation" on the negative going output. For a p-n-p input stage, these effects are reversed as shown by $v_{op}(t)$.

5.0 SECOND-ORDER EFFECTS: VOLTAGE FOLLOWER SLEW BEHAVIOR

If the op amp is operated in the noninverting mode and driven by a large fast rising input, the ouput exhibits the characteristic waveform in *Figure 16.* As shown, this waveform does not have the simple symmetrical slew characteristic of the inverter. In one direction, the output has a fast step (slew "enhancement") followed by a "normal" inverter slewing response. In the other direction, it suffers a slew "degradation" or reduced slope when compared with the inverter slewing response.

We will first study slew degradation in the voltage follower connection, since this represents a worst case slewing condition for the op amp. A model which adequately represents the follower under large-signal conditions can be obtained from that in *Figure 12* by simply tying the output to the inverting input, and including a capacitor C_s to account for the presence of any capacitance at the output of the first stage (tail) current source, see *Figure 17.* This "input tail" capacitance is important in the voltage follower because the input stage undergoes rapid large-signal excursions in this connection, and the charging currents in C_s can be quite large.

Circuit behavior can be understood by analyzing *Figure 17* as follows. The large-signal input step causes Q_1 to turn OFF, leaving Q_2 to operate as an emitter follower with its emitter tracking the variational output voltage, $v_0(t)$. It is seen that $v_0(t)$ is essentially the voltage appearing across both C_s and C_c so we can write

$$\frac{dv_0}{dt} \cong \frac{i_c}{C_c} \cong \frac{i_s}{C_s}. \tag{35}$$

Noting that $i_c \cong 2I_1 - i_s$ (unity α's assumed), (35) can be solved for i_s:

$$i_s \cong \frac{2I_1}{1 + C_c/C_s} \tag{36}$$

which is seen to be constant with time. The degraded voltage follower slew rate is then obtained by substituting (36) into (35):

$$\left.\frac{dv_0}{dt}\right|_{degr} \cong \frac{i_s}{C_s} \cong \frac{2I_1}{C_c + C_s}. \tag{37}$$

Comparing (37) with the slew rate for the inverter, (18), it is seen that the slew rate is reduced by the simple factor $1/(1 + C_s/C_c)$. As long as the input tail capacitance C_s is small compared with the compensation amplifiers where C_c is small, degradation become quite noticeable, and one is encouraged to develop circuits with small C_s.

As an example, consider the relatively fast LM118 which has $C_c \cong 5$ pF, $C_8 \cong 2$ pF, $2I_1 = 500$ μA. The calcualted inverter slew rate is $2I_1/C_c \cong 100V/\mu s$, and the degraded voltage follower slew rate is found to be $2I_1/(C_c + C_8) \cong 70V/\mu s$. The slew degradation is seen to be about 30 percent, which is very significant. By contrast a μA741 has $C_c \cong 30$ pF and $C_8 \cong 4$ pF which results in a degradation of less than 12 percent.

The slew "enhanced waveform can be similarly predicted from a simplified model. By reversing the polarity of the input and initally assuming a finite slope on the input step, the enhanced follower is analyzed, as shown in *Figure 18.* Noting that Q_1 is assumed to be turned ON by the step input and Q_2 is OFF, the output voltage becomes

$$v_0(t) \cong -\frac{1}{C_c}\int_0^t [2I_1 + i_s(t)]\, dt. \tag{38}$$

The voltage at the emitter of Q_1 is essentially the same as the input voltage, $v_i(t)$, so the current in the "tail" capacitance C_8 is

$$i_s(t) \cong C_8 \frac{dv_i}{dt} \cong \frac{C_8 V_{ip}}{t_1} \qquad 0 < t < t_1. \tag{39}$$

Combining (38) and (39), $v_0(t)$ is

$$-v_0(t) \cong \frac{1}{C_c}\int_0^t 2I_1\, dt + \frac{1}{C_c}\int_0^{t_1} \frac{C_8 V_{ip}}{t_1}\, dt \tag{40}$$

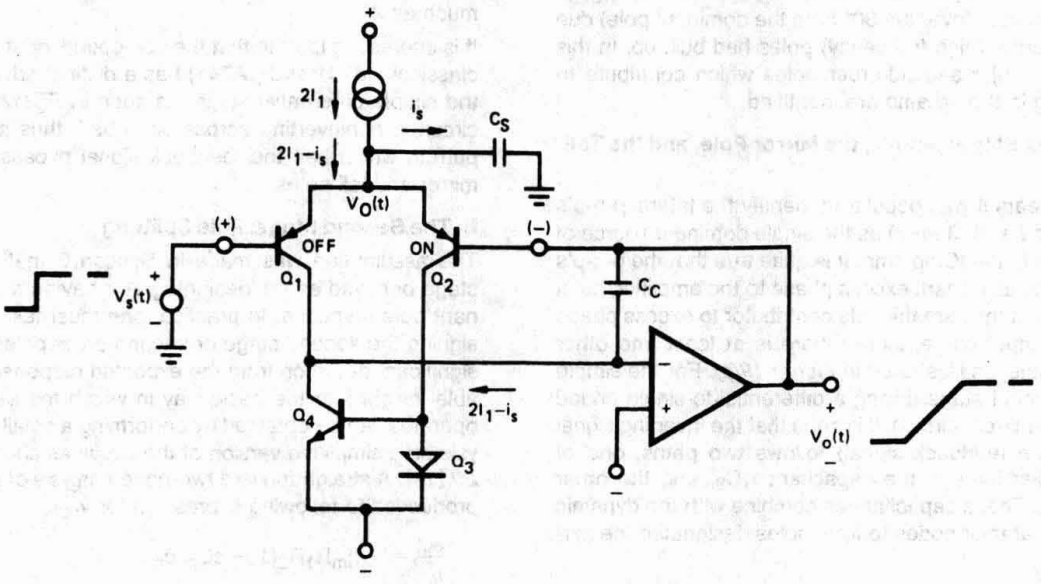

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FIGURE 17. Circuit used for calculation of slew "degradation" in the voltage follower. The degradation is caused by the capacitor C_8, which robs current from the tail, $2I_1$, thereby preventing the full $2I_1$ from slewing C_c.

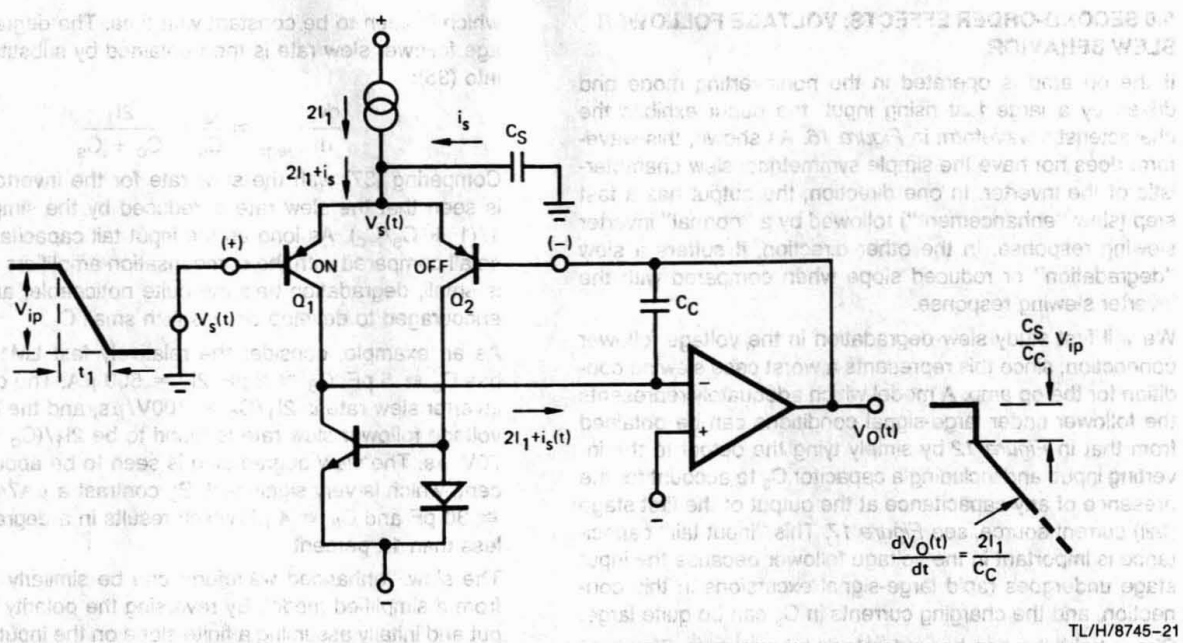

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FIGURE 18. Circuit used for calculation of slew "enhancement" in the voltage follower. The fast falling input casues a step output followed by a normal slew response as shown.

or

$$-v_0(t) \cong \frac{C_8}{C_c} V_{ip} + \frac{2I_1 t}{C_c}. \qquad (41)$$

Equation (41) tells us that the output has an initial negative step which is the fraction C_8/C_c of the input voltage. This is followed by a normal slewing response, in which the slew rate is identical to that of the inverter, see (18). This response is illustrated in *Figure 18.*

6. LIMITATIONS ON BANDWIDTH

In earilier sections, all bandlimiting effects were ignored except that of the compensation capacitor, C_c. The unity-gain frequency was set at a point sufficiently low so that negligible excess phase (over the 90° from the dominant pole) due to second-order (high frequency) poles had built up. In this section the major second-order poles which contribute to bandlimiting in the op amp are identified.

A. The Input Stage: p-n-p's, the Mirror Pole, and the Tail Pole

For many years it was popular to identify the lateral p-n-p's (which have f_t's $\cong$ 3 MHz) as the single dominant source of bandlimiting in the IC op amp. It is quite true that the p-n-p's do contribute significant excess phase to the amplifier, but it is not true that they are the sole contributor to excess phase [9]. In the input stage, alone, there is at least one other important pole, as illustrated in *Figure 19(a).* For the simple differential input stage driving a differential-to-single ended converter ("mirror" circuit), it is seen that the inverting signal (which is the feedback signal) follows two paths, one of which passes through the capacitance C_8, and the other through C_m. These capacitances combine with the dynamic resistances at their nodes to form poles designated the mirror pole at

$$p_m \cong \frac{I_1}{C_m kT/q}, \qquad (42)$$

and the tail pole at

$$p_t \cong \frac{2I_1}{C_8 kT/q}. \qquad (43)$$

It can be seen that if one attempts to operate the first stage at too low a current, these poles will bandlimit the amplifier. If, for example, we choose $I_1 = 1\ \mu A$, and assume $C_m \cong 7$ pF (consisting of 4 pF isolation capacitance and 3 pF emitter transition capacitance) and $C_8 \cong 4$ pF,[3] $p_m/2\pi \cong 0.9$ MHz and $p_t/2\pi \cong 3$ MHz either of which would seriously degrade the phase margin of a 1 MHz amplifier.

If a design is chosen in which either the tail pole or the mirror pole is absent (or unimportant), the remaining pole rolls off only half the signal, so the overall response contains a pole-zero pair separated by one octave. Such a pair generally has a small effect on amplifier response unless it occurs near ω_u, where it can degrade phase margin by as much as 20°.

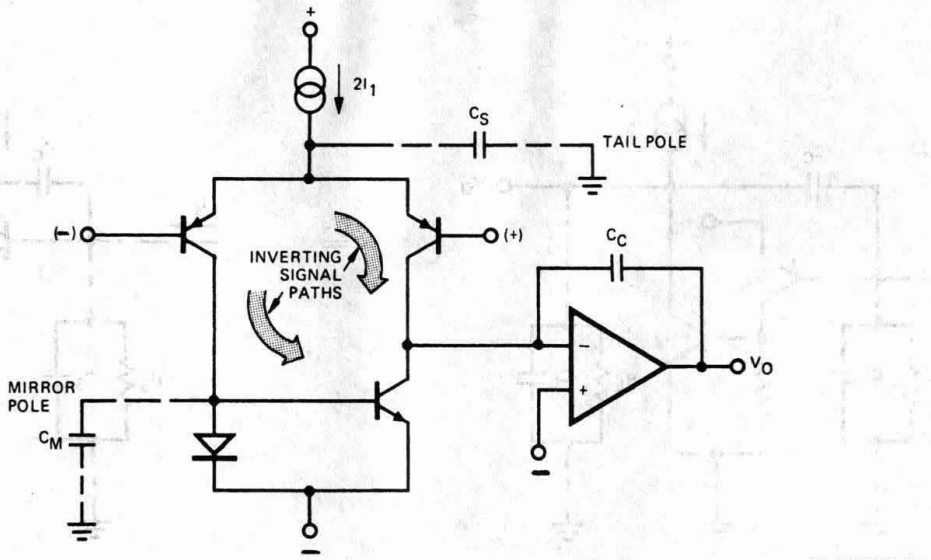
It is interesting to note that the compound input stage of the classical LM101 and μA741) has a distinct advantage over the simple differential stage, as seen in *Figure 19(b).* This circuit is noninverting across each half, thus it provides a path in which half the feedback signal bypasses both the mirror and tail poles.

B. The Second Stage: Pole Splitting

The assumption was made in Section 3 that the second stage behaved as an ideal integrator having a single dominant pole response. In practice, one must take care in designing the second stage or second-order poles can cause significant deviation from the expected response. Considerable insight into the basic way in which the second stage operates can be obtained by performing a small-signal analysis on a simplified version of the circuit as shown in *Figure 20* [10]. A straightforward two-node analysis of *Figure 20(c)* produces the following expression for v_{out}.

$$\frac{v_{out}}{i_s} = -g_m R_1 R_2 (1 - sC_p/g_m) \div$$
$$(1 + s[R_1 (C_1 + C_p) + R_2 (C_2 + C_p) + g_m R_1 R_2 C_p]$$
$$+ s^2 R_1 R_2 [C_1 C_2 + C_p (C_1 + C_2)]). \qquad (44)$$

[3] C_8 can have a wide range of values depending on circuit configuration. It is largest for n-p-n input differential amps since the current source has a collector-substrate capacitance ($C_8 \cong$ 3–4 pF at its output. For p-n-p input stages it can be as small as 1–2 pF.



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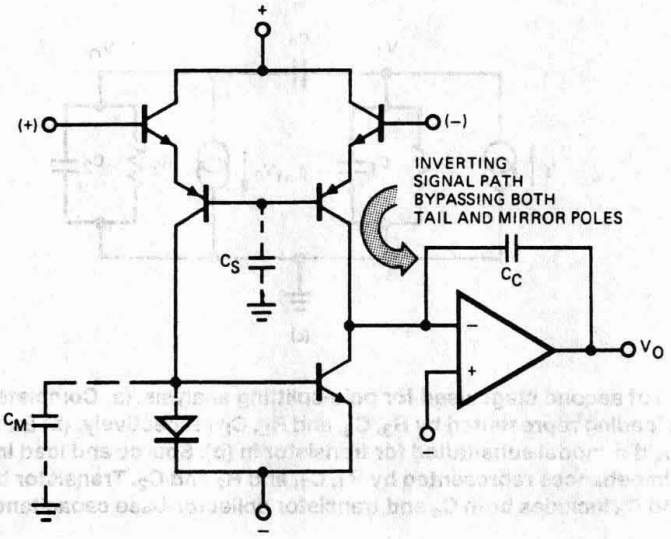
(a)



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(b)

FIGURE 19. (a) Circuit showing "mirror" pole due to C_m and "tail" pole due to C_8. One component of the signal due to an inverting input must pass through either the mirror or tail poles. (b) Alternate circuit to *Figure 19(a)* (LM101, μA741) which has less excess phase. Reason is that half the inverting signal path need not pass through the mirror pole or the tail pole.

The denominator of (44) can be approximately factored under conditions that its two poles are widely separated. Fortunately, the poles are, in fact, widely separated under most normal operating conditions. Therefore, one can assume that the denominator of (44) has the form

$$D(s) = (1 + s/p_1)(1 + s/p_2)$$
$$= 1 + s(1/p_1 + 1/p_2) + s^2/p_1p_2. \quad (45)$$

With the assumption that p_1 is the dominant pole and p_2 is nondominant, i.e., $p_1 \ll p_2$, (45) becomes

$$D(s) \cong 1 + s/p_1 + s^2/p_1p_2. \quad (46)$$

Equating coefficients of s in (44) and (46), the dominant pole p_1 is found directly:

$$p_1 \cong \frac{1}{R_1(C_1 + C_p) + R_2(C_2 + C_P) + g_mR_1R_2C_p} \quad (47)$$

$$\cong \frac{1}{g_mR_1R_2C_p}. \quad (48)$$

The latter approximation (48), normally introduces little error, because the g_m term is much larger than the other two. We note at this point that p_1, which represents the dominant pole of the amplifier, is due simply to the familiar Miller-multiplied feedback capacitance $g_mR_2C_p$ combined with input node resistance, R_1. The nondominant pole p_2 is found similarly by equating s^2 coefficients in (44) and (46) to get p_1p_2, and dividing by p_1 from (48). The result is

$$p_2 \cong \frac{g_mC_p}{C_1C_2 + C_p(C_1 + C_2)}. \quad (49)$$

Several interesting things can be seen in examining (48) and (49). First, we note that p_1 is inversely proportional to g_m (and C_p), while p_2 is directly dependent on g_m (and C_p).

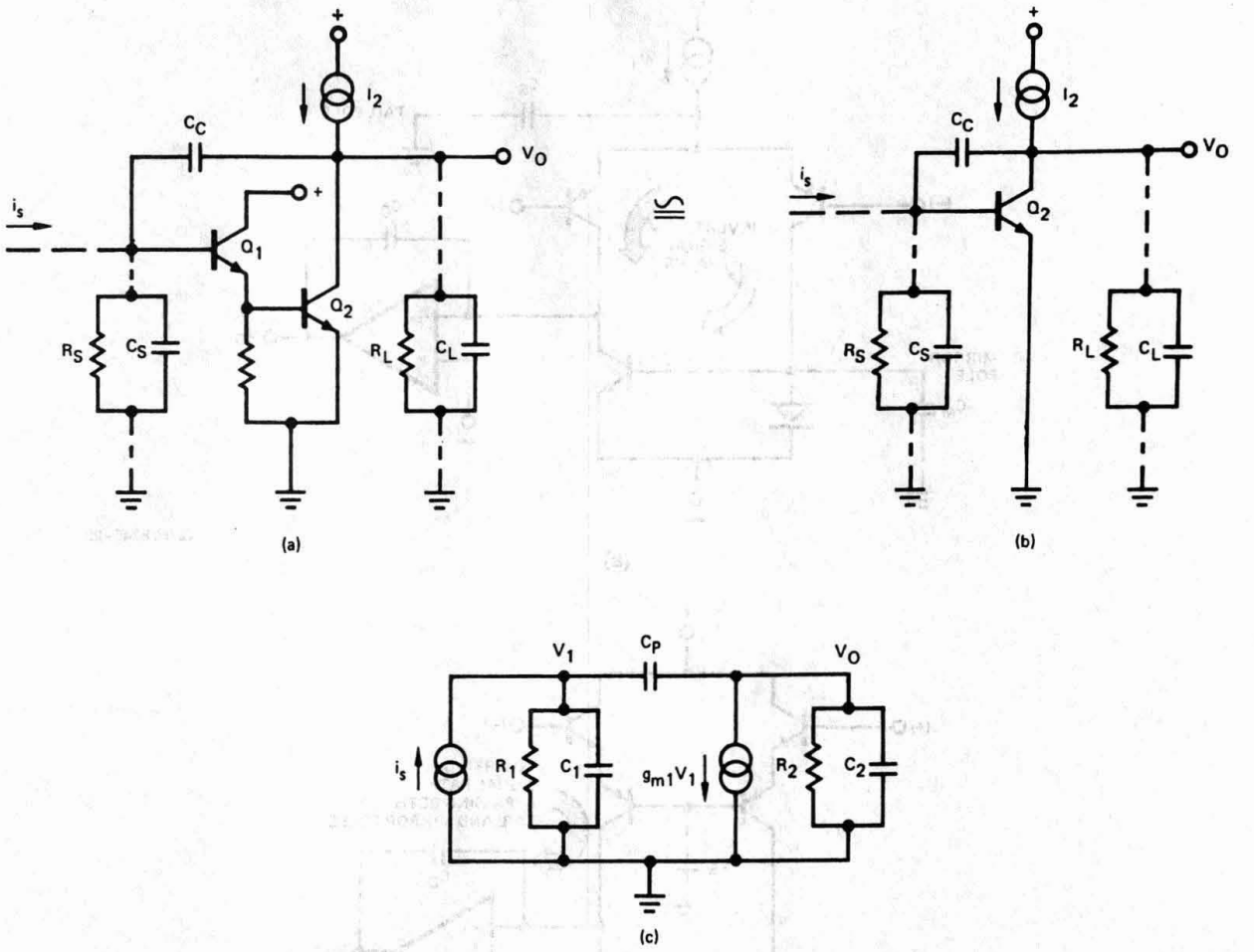

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FIGURE 20. Simplification of second stage used for pole-splitting analysis. (a) Complete second stage with input stage and output stage loading represented by R_8, C_8, and R_L, C_L respectively. (b) Emitter follower ignored to simplify analysis. (c) Hybrid π model substituted for transistor in (b). Source and load impedances are absorbed into model with the total impedances represented by R_1, C_1, and R_2 and C_2. Transistor base resistance is ignored and C_p includes both C_c and transistor collector-base capacitance.

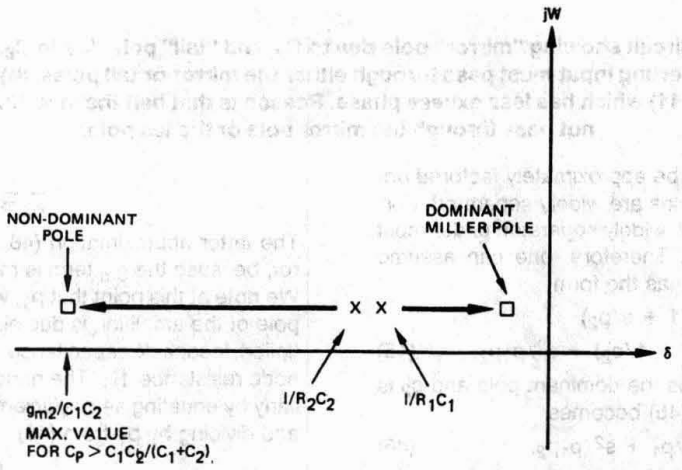

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FIGURE 21. Pole migration for second stage employing "pole-splitting" compensation. Plot is shown for increasing C_p and it is noted that the nondominant pole reaches a maximum value for large C_p.

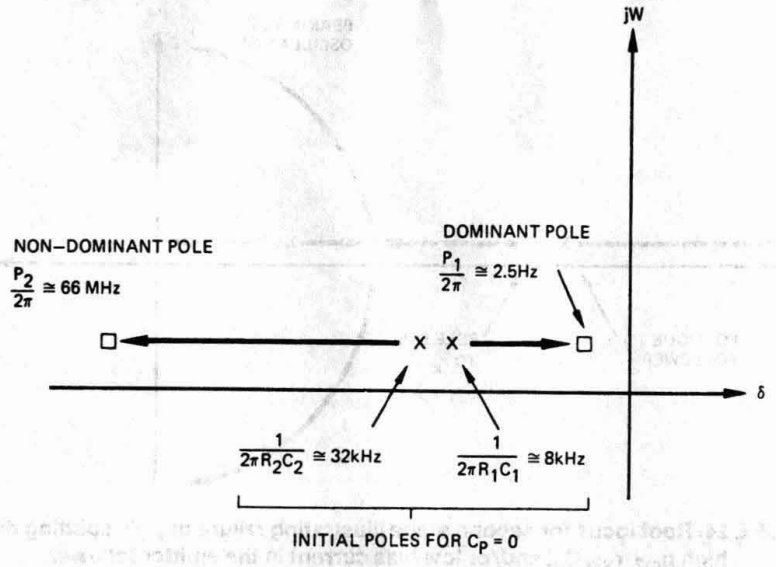

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FIGURE 22. Example of pole-splitting compensation in the μA741 op amp. Values used in (48) and (49) are: $g_{m2} = 1/87\Omega$, $C_p = 30$ pF, $C_1 \cong C_2 = 10$ pF, $R_1 = 1.7$ MΩ, $R_2 = 100$ kΩ.

Thus, as either C_p or transistor gain are increased, the dominant pole decreases and the nondominant pole increases. The poles p_1 and p_2 are being "split-apart" by the increased coupling action in a kind of inverse root locus plot.

This *pole-splitting* action is shown in *Figure 21,* where pole migration is plotted for C_p increasing from 0 to a large value. *Figure 22* further illustrates the action by giving specific pole positions for the μA741 op amp. It is seen that the initial poles (for $C_p = 0$) are both in the tens of kHz region and these are predicted to reach 2.5 Hz ($p_1/2\pi$) and 66 MHz ($p_2/2\pi$) after compensation is applied. This result is, of course, highly satisfactory since the second stage now has a single dominant pole effective over a wide frequency band.

C. Failure of Pole Splitting

There are several situations in which the application of pole-splitting compensation may not result in a single dominant pole response. One common case occurs in very wide-band op amps where the pole-splitting capacitor is small. In this situation the nondominant pole given by (49) may not become broadbanded sufficiently so that it can be ignored. To illustrate, suppose we attempt to minimize power dissipation by running the second stage of an LM118 (which has a small-signal bandwidth of 16 MHz) at 0.1 mA. For this op amp $C_p = 5$ pF, $C_1 \cong C_2 \cong 10$ pF. From (49), the nondominant pole is

$$\frac{p_2}{2\pi} \cong 16 \text{ MHz} \qquad (50)$$

which lies right at the unity-gain frequency. This pole alone would degrade phase margin by 45°, so it is clear that we need to bias the second stage with a collector current greater than 0.1 mA to obtain adequate g_m. Insufficient pole-splitting can therefore occur; but the cure is usually a simple increase in second stage g_m.

A second type of pole-splitting failure can occur, and it is ofen much more difficult to cope with. If, for example, one gets over-zealous in his attempt to broadband the nondominant pole, he soon discovers that other poles exist within the second stage which can cause difficulties. Consider a more exact equivalent circuit for the second stage of *Figure 20(a)* as shown in *Figure 23*. If the follower is biased at low currents or if c_p, Q_2 g_m, and/or r_x are high, the circuit can contain at least four important poles rather than the two

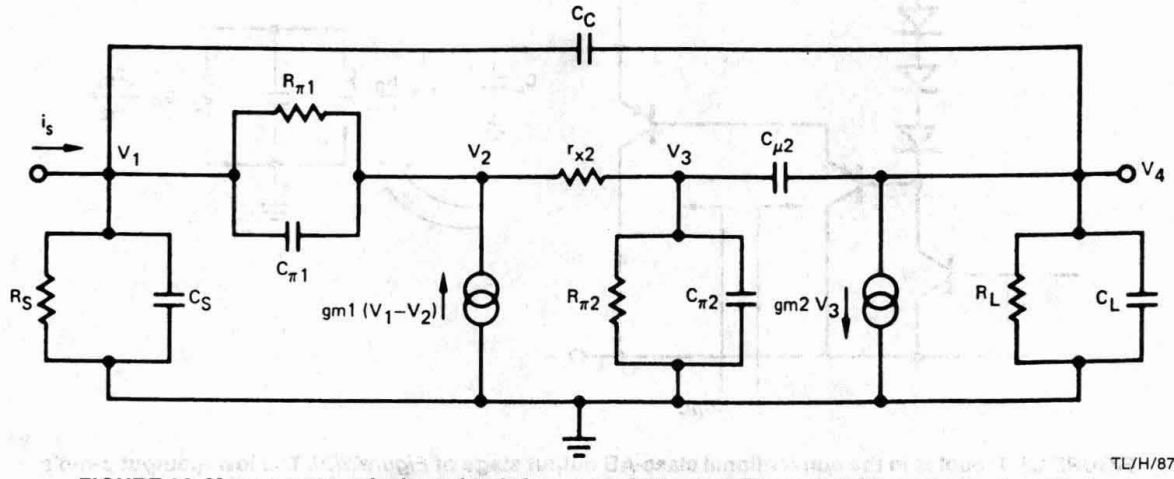

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FIGURE 23. More exact equivalent circuit for second stage of *Figure 20(a)* including a simplified π model for the emitter follower ($R\pi_1$, $C\pi_1$, g_{m1}) and a complete π for Q_2 (rx_2, $R\pi_2$, etc.).

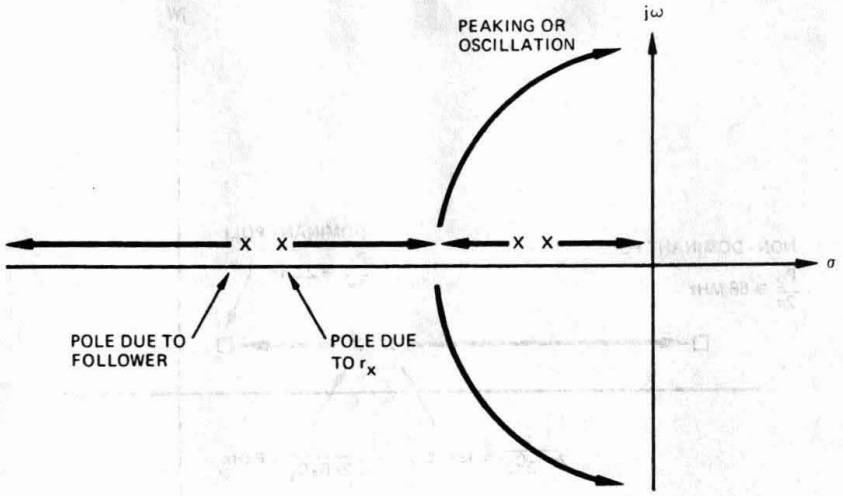

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FIGURE 24. Root locus for second stage illustrating failure of pole splitting due to high g_{m2}, r_{x2}, C_p, and/or low bias current in the emitter follower.

considered in simple pole splitting. Under these conditions, we no longer have a response with just negative real poles as in *Figure 21,* but observe a root locus of the sort shown in *Figure 24.* It is seen in this case that the circuit contains a pair of complex, possibly underdamped poles which, of course, can cause peaking or even oscillation. This effect occurs so commonly in the development of wide-band pole-split amplifiers that it has been (not fondly) dubbed "the second stage bump."

There are numerous ways to eliminate the "bump," but no single cure has been found which is effective in all situations. A direct hand analysis of *Figure 23* is possible, but the results are difficult to interpret. Computer analysis seems the best approach for this level of complexity, and numerous specific analyses have been made. The following is a list of circuit modifications that have been found effective in reducing the bump in various studies: 1) reduce g_{m2}, r_{x2}, $C_{\mu 2}$, 2) add capacitance or a series RC network from the stage input to ground—this reduces the high frequency local feedback due to C_p, 3) pad capacitance at the output for similar reasons, 4) increase operating current of the follower, 5) reduce C_p, 6) use a higher f_t process.

D. Troubles in the Output Stage

Of all the circuitry in the modern IC op amp, the class-AB output stage probably remains the most troublesome. None of the stages in use today behave as well as one might desire when stressed under worst case conditions. To illustrate, one of the most commonly used output stages is shown in *Figure 2(b).* The p-n-p's in this circuit are "substrate" p-n-p's having low current f_t's of around 20 MHz. Unfortunately, both β_0 and f_t begin to fall off rapidly at quite low current densities, so as one begins to sink just a few milliamps in the circuit, phase margin troubles can develop. The worst effect occurs when the amplifier is operated with a large capacitive load (>100 pF) while sinking high currents. As shown in *Figure 25,* the load capacitance on the

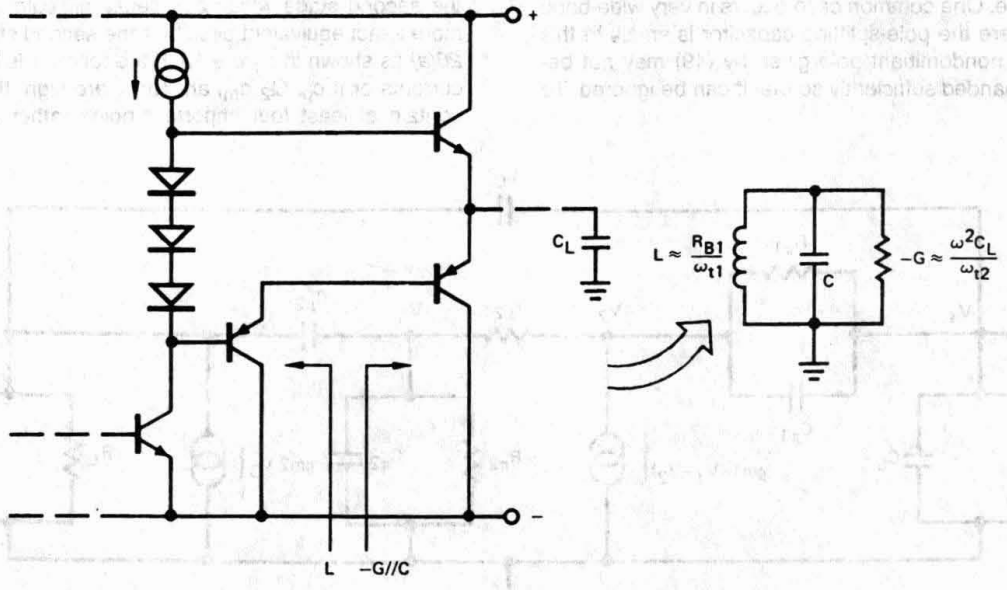

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FIGURE 25. Troubles in the conventional class-AB output stage of *Figure 2(b).* The low f_t output p-n-p's interact with load capacitance to form the equivalent of a one-port oscillator.

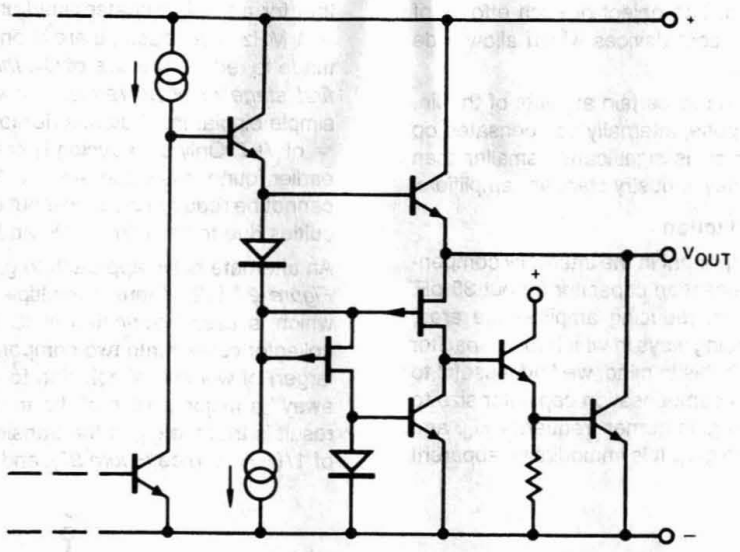


FIGURE 26. The "BI-FET™" output stage employing JFET's and bipolar n-p-n's to eliminate sensitivity to load capacitance.

output follower causes it to have negative input conductance, while the driver follower can have an inductive output impedance. These elements combine with the capacitance at the interstage to generate the equivalent of a one-port oscillator. In a carefully designed circuit, oscillation is suppressed, but peaking (the "output bump") can occur in most amplifiers under appropriate conditions.

One new type of output circuit which does not use p-n-p's is shown in *Figure 26* [6]. This circuit employs compatible JFET's (or MOSFET's, see similar circuit in [11]) in a FET/bipolar quasi-complementary output stage, which is insensitive to load capacitance. Unfortunately, this circuit is rather complex and employs extra process steps, so it does not appear to represent the cure for the very low cost op amps.

7. The Gain Cell: Linear Large-Scale Integration

As the true limitations of the basic op amp are more fully understood, this knowledge can be applied to the development of more "optimum" amplifiers. There are, of course, many ways in which one might choose to optimize the device. We might, for example, attempt to maximize speed (bandwidth, slew rate, settling time) without sacrificing dc characteristics. The compatible JFET/bipolar amp of *Figure 15* represents such an effort. An alternate choice might be to design an amplifier having all of the performance features of the most widely used general purpose op amps (i.e., μA741, LM107, etc.), but having minimum possible die area. Such a pursuit is parallel to the efforts of digital large-scale integration (LSI) designers in their devlelopment of minimum

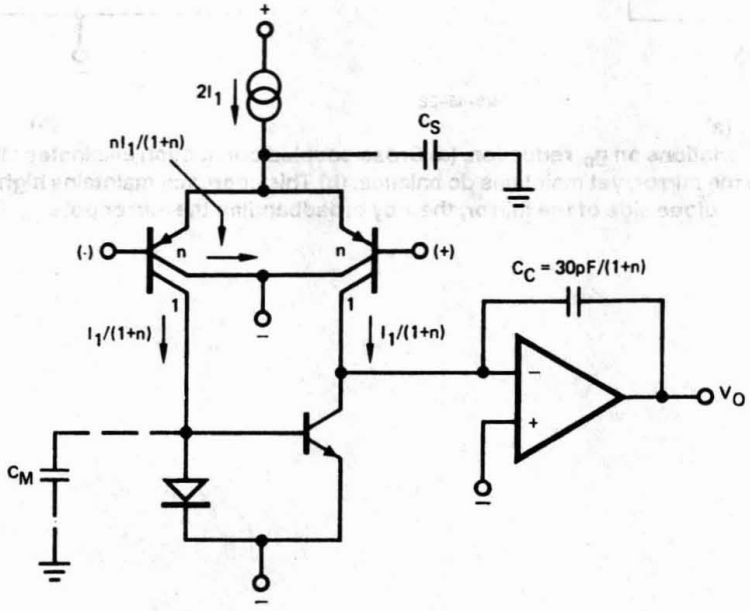


FIGURE 27. Basic g_m reduction obtained by using split collector p-n-p's. C_c and area are reduced since $C_c = g_{m1}/\omega_u$.

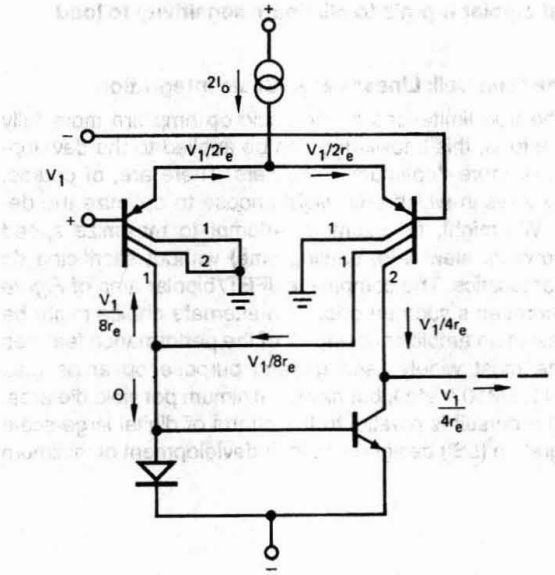
area memory cells or gates. The object of such efforts, of course, is to develop lower cost devices which allow wide and highly economic usage.

In this section we briefly discuss certain aspects of the linear *gain cell,* a general purpose, internally compensated op amp having a die area which is significantly smaller than that of equivalent, present day, industry standard amplifiers.

A. Transconductance Reduction

The single largest area component in the internally compensated op amp is the compensation capacitor (about 30 pF, typically). A major interest in reducing amplifier die area, therefore, centers about finding ways in which this capacitor can be reduced in size. With this in mind, we find it useful to examine (15), which relates compensation capacitor size to two other parameters, unity gain corner frequency ω_u, and first stage transconductance g_{m1}. It is immediately apparent that for a fixed, predetermined unity gain corner (about $2\pi \times 1$ MHz in our case), there is only one change that can be made to reduce the size of C_c: *the transconductance of the first stage must be reduced.* If we restrict our interest to simple bipolar input stages (for low cost), we recall the $g_{m1} = qI_1/kT$. Only by reducing I_1 can g_{m1} be reduced, and we earlier found in Section 6-A and *Figure 19(a)* and *(b)* that I_1 cannot be reduced much without causing phase margin difficulties due to the mirror pole and the tail pole.

An alternate basic approach to g_m reduction is illustrated in *Figure 27* [12]. there, a multiple collector p-n-p structure, which is easily fabricated in IC form, is used to split the collector current into two components, one component (the larger) of which is simply tied to ground, thereby "throwing away" a major portion of the transistor output current. The result is that the g_m of the transistor is reduced by the ratio of $1/(1 + n)$ (see *Figure 27*), and the compensation capaci-



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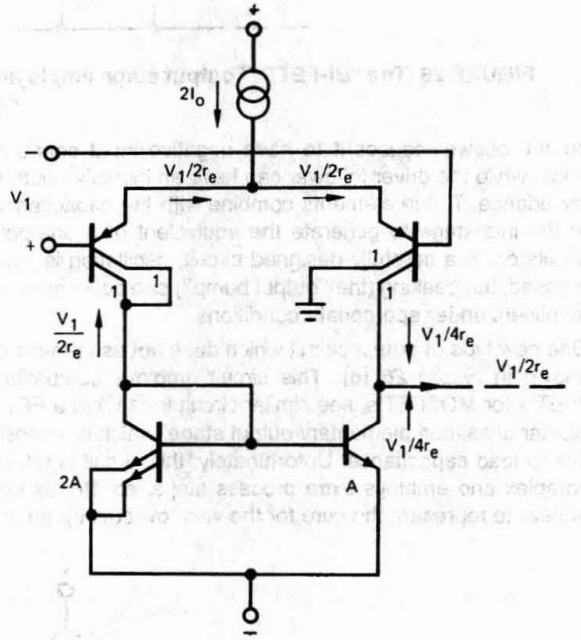
(a)



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(b)

FIGURE 28. Variations on g_m reduction. (a) Cross-coupled connection eliminates all ac current passing through the mirror, yet maintains dc balance. (b) This approach maintains high current on the diode side of the mirror, thereby broadbanding the mirror pole.

tance can be reduced directly by the same factor. It might appear that the mirror pole would still cause difficulties since the current mirror becomes current starved in *Figure 27,* but the effect is not as severe as might be expected. The reason is that the inverting signal can now pass through the high current wide-band path, across the differential amp emitters and into the second stage, so at least half the signal current does not become bandlimited. This partial bandlimiting can be further reduced by using one of the circuits in *Figure 28(a)* or *(b)*.[4] In (a), the p-n-p collectors are cross coupled in such a way that the ac signal is cancelled in the mirror circuit, while dc remains completely balanced. Thus the mirror pole is virtually eliminated. The circuit does have a drawback, however, in that the uncorrelated noise currents coming from the two p-n-p's add rather than subtract at the input to the mirror, thereby degrading noise performance. The circuit in *Figure 28(b)* does not have this defect, but requires care in matching p-n-p collector ratios to n-p-n emitter areas. Otherwise offset and drift will degrade as one attempts to reduce g_m by large factors.

B. A Gain Cell Example

As one tries to make large reductions in die area for the gain cell, many factors must be considered in addition to novel circuit approaches. Of great importance are special layout/circuit techniques which combine a maximum number of components into minimum area.

In a good layout, for example, all resistors are combined into islands with transistors. If this is not possible initially, circuit and device changes are made to allow it. The resulting device geometrics within the islands are further modified in shape to allow maximum "packing" of the islands. That is, when the layout is complete, the islands should have shapes which fit together as in a picture puzzle, with no waste of space. Further area reductions can be had by modifying the isolation process to one having minimum spacing between the isolation diffusion and adjacent p-regions.

As example of a gain cell which employs both circuit and layout optimization is shown in *Figure 29*: This circuit uses the g_m reduction technique of *Figure 28(a)* which results in a compensation capacitor size of only 5 pF rather than the normal 30 pF. The device achieves a full 1 MHz bandwidth, a 0.67V/μs slew rate, a gain greater than 100,000, typical offset voltages less than 1 mV, and other characteristics normally associated with an LM107 or μA741. In quad form each amplifier requires an area of only 23 x 35 mils which is one-fourth the size of today's industry standard μA741 (typically 56 x 56 mils). This allows over 8000 possible gain cells to be fabricated on a single 3-inch wafer. Further, it appears quite feasible to fabricate larger arrays of gain cells, with six or eight on a single chip. Only packaging and applications questions need be resolved before pursuing such a step.

[4]The circuit in *Figure 28(a)* is due to R. W. Russell and the variation in *Figure 28(b)* was developed by D. W. Zobel.

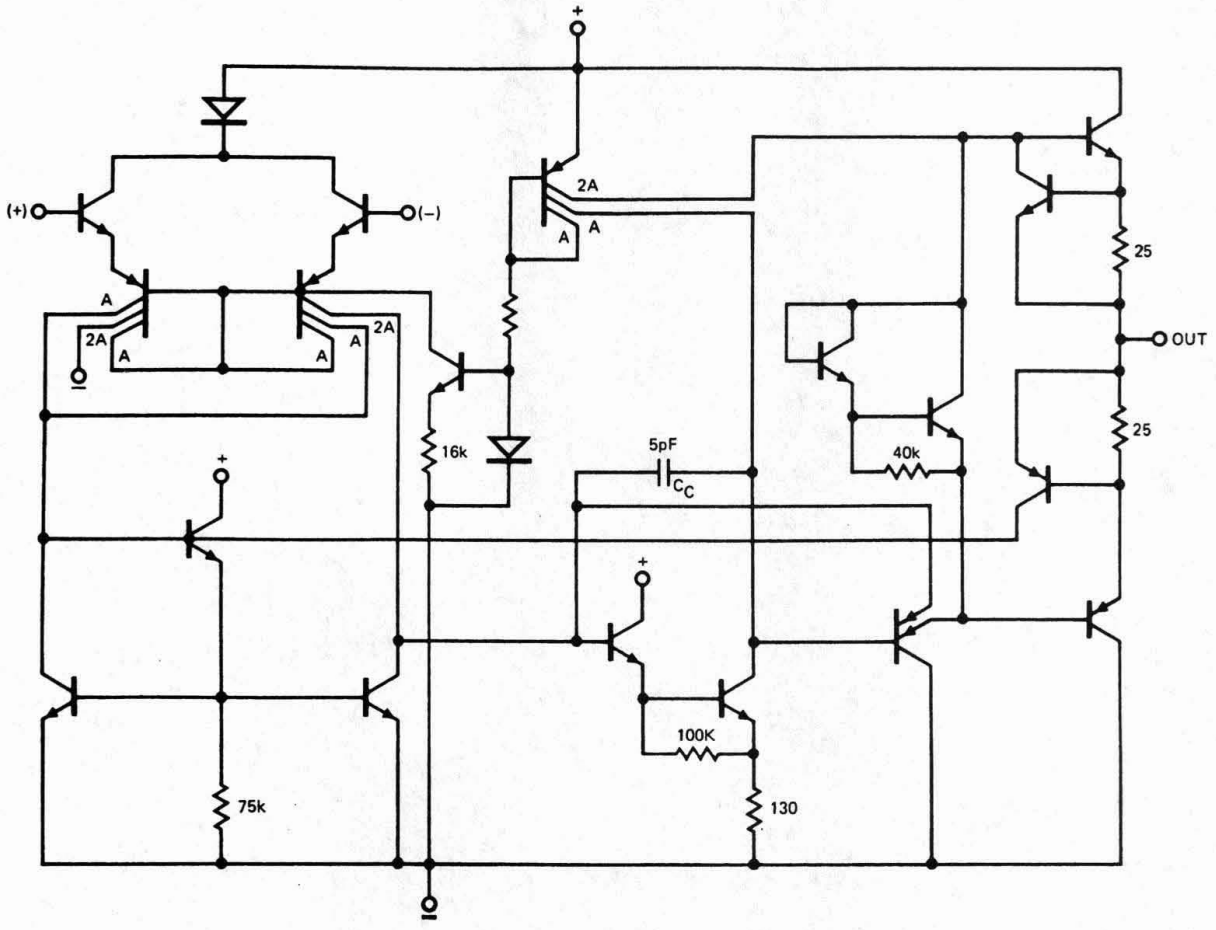

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FIGURE 29. Circuit for optimized gain cell which has been fabricated in one-fourth the die size of the equivalent μA741.

ACKNOWLEDGMENT

Many important contributions were made in the gain cell and FET/bipolar op amp areas by R. W. Russell. The author gratefully acknowledges his very competent efforts.

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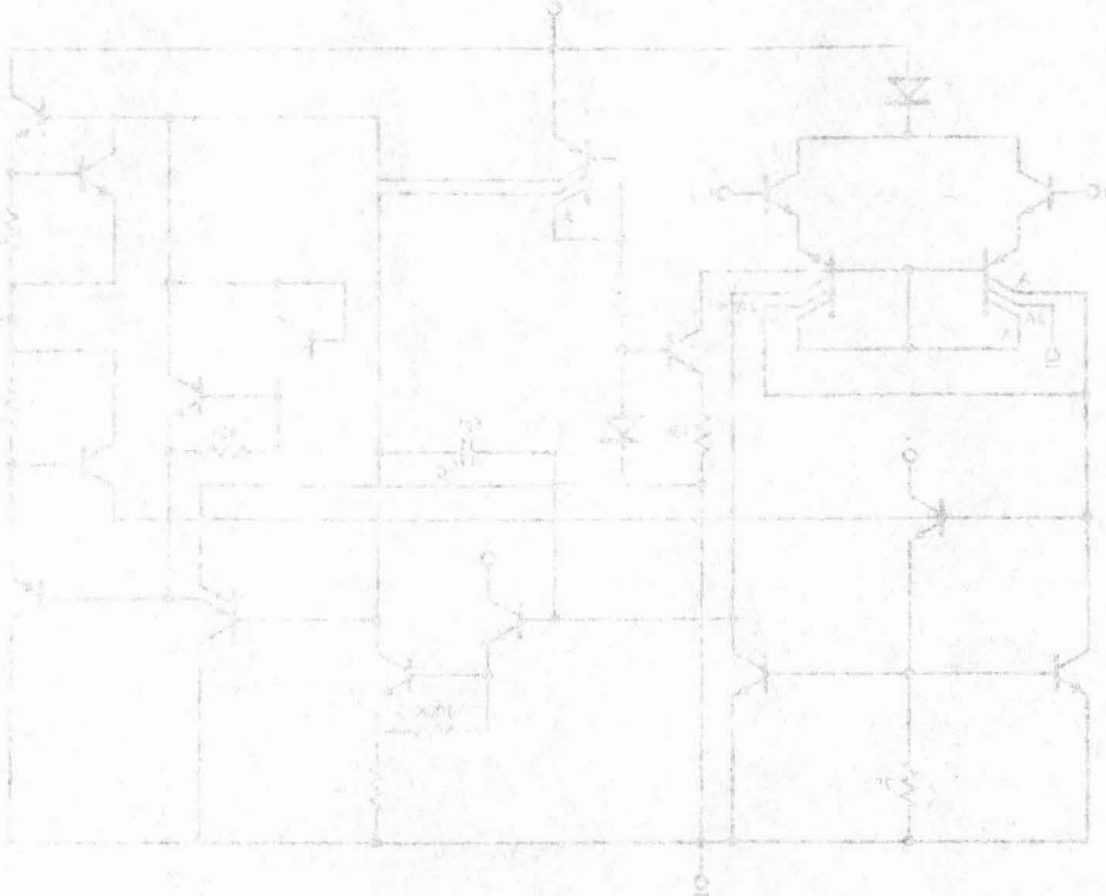

V/F Converter ICs Handle Frequency-to-Voltage Needs

National Semiconductor
Appendix C
Robert A. Pease

Simplify your F/V converter designs with versatile V/F ICs. Starting with a basic converter circuit, you can modify it to meet almost any application requirement. You can spare yourself some hard labor when designing frequency-to-voltage (F/V) converters by using a voltage-to-frequency IC in your designs. These ICs form the basis of a series of accurate, yet economical, F/V converters suiting a variety of applications.

Figure 1 shows an LM331 IC (or LM131 for the military temperature range) in a basic F/V converter configuration (sometimes termed a stand-alone converter because it requires no op amps or other active devices other than the IC). (Comparable V/F ICs, such as RM4151, can take advantage of this and other circuits described in this article, although they might not always be pin-for-pin compatible).

This circuit accepts a pulse-train or square wave input amplitude of 3V or greater. The 470 pF coupling capacitor suits negative-going input pulses between 80 μs and 1.5 μs, as well as accommodating square waves or positive-going pulses (so long as the interval between pulses is at least 10 μs).

IC Handles the Hard Part

The LM331 detects an input-signal change by sensing when pin 6 goes negative relative to the threshold voltage at pin 7, which is nominally biased 2V lower than the supply voltage. When a signal change occurs, the LM331's input comparator sets an internal latch and initiates a timing cycle. During this cycle, a current equal to V_{REF}/R_S flows out of pin 1 for a time $t = 1.1\ R_tC$. The 1 μF capacitor filters this pulsating current from pin 1, and the current's average value flows through load resistor R_L. As a result, for a 10 kHz input, the circuit outputs 10 V_{DC} across R_L with good (0.06% typical) nonlinearity.

Two problems remain, however: the output at V1 includes about 13 mVp-p ripple, and it also lags 0.1 second behind an input frequency step change, settling to 0.1% of full-scale in about 0.6 second. This ripple and slow response represent an inherent tradeoff that applies to almost every F/V converter.

The Art of Compromise

Increasing the filter capacitor's value reduces ripple but also increases response time. Conversely, lowering the filter capacitor's value improves response time at the expense of larger ripple. In some cases, adding an active filter results in faster response and less ripple for high input frequencies.

Although the circuit specifies a 15V power supply, you can use any regulated supply between 4 V_{DC} and 40 V_{DC}. The output voltage can extend to within 3 V_{DC} of the supply voltage, so choose R_L to maintain that output range.

Adding a 220 kΩ/0.1 μF postfilter to the circuit slows the response slightly, but it also reduces ripple to less than 1 mVp-p for frequencies from 200 Hz to 10 kHz. The reduction in ripple achieved by adding this passive filter, while not as good as that obtainable using an active filter, could suffice in some applications.

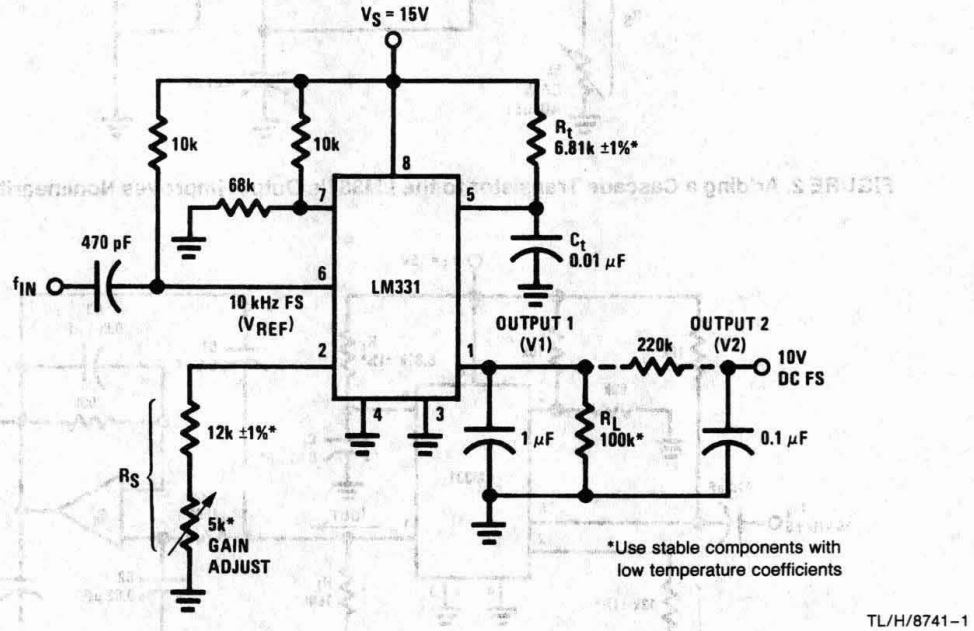

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FIGURE 1. A Simple Stand-Alone F/V Converter Forms the Basis for Many Other Converter-Circuit Configurations

Improving the Basic Circuit

Further modifications and additions to the basic F/V converter shown in *Figure 1* can adapt it to specific performance requirements. *Figure 2* shows one such modification, which improves the converter's nonlinearity to 0.006% typical.

Reconsideration of the basic stand-alone converter shows why its nonlinearity falls short of this improved version's. At low input frequencies, the current source feeding pin 1 in the LM331 is turned off most of the time. As the input frequency increases, however, the current source stays on more of the time, and its own impedance attenuates the output signal for an increasing fraction of each cycle time. This disproportionate attenuation at higher frequencies causes a parabolic change in full-scale gain rather than the desired linear one.

In the improved circuit, on the other hand, the PNP transistor acts as a cascade, so the output impedance at pin 1 sees a constant voltage that won't modulate the gain. Also, with an alpha ranging between 0.998 and 0.990, the transistor exhibits a temperature coefficient of between 10 ppm/°C and 40 ppm/°C—a fairly minor effect. Thus, this circuit's nonlinearity does not exceed 0.01% maximum for the 10V output range shown and is normally not worse than 0.01% for any supply voltage between 4V and 40V.

Add an Output Buffer

The circuit in *Figure 3* adds an output buffer (unity-gain follower) to the basic single-supply F/V converter. Either an LM324 or LM358 op amp functions well in a single-supply circuit because these devices' common-mode ranges extend down to ground. But if a negative supply is available, you can use any op amp; types such as the LF351B or LM308A, which have low input currents, provide the best accuracy.

The output buffer in *Figure 3* also acts as an active filter, furnishing a 2-pole response from a single op amp. This filter provides the general response

$$V_{OUT}/I_{OUT} = R_L/(1 + K1p + K2p^2).$$

(p is the differential operator d/dt.) As shown, R_L controls the filter's DC gain. The high frequency response rolls off at 12 dB/octave. Near the circuit's natural resonant frequency, you can choose the damping to give a little overshoot—or none, as desired.

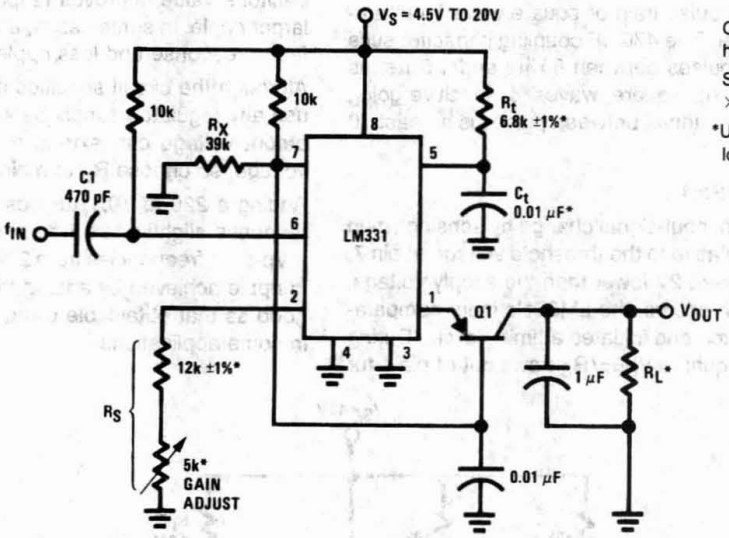

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FIGURE 2. Adding a Cascade Transistor to the LM331's Output Improves Nonlinearity to 0.006%

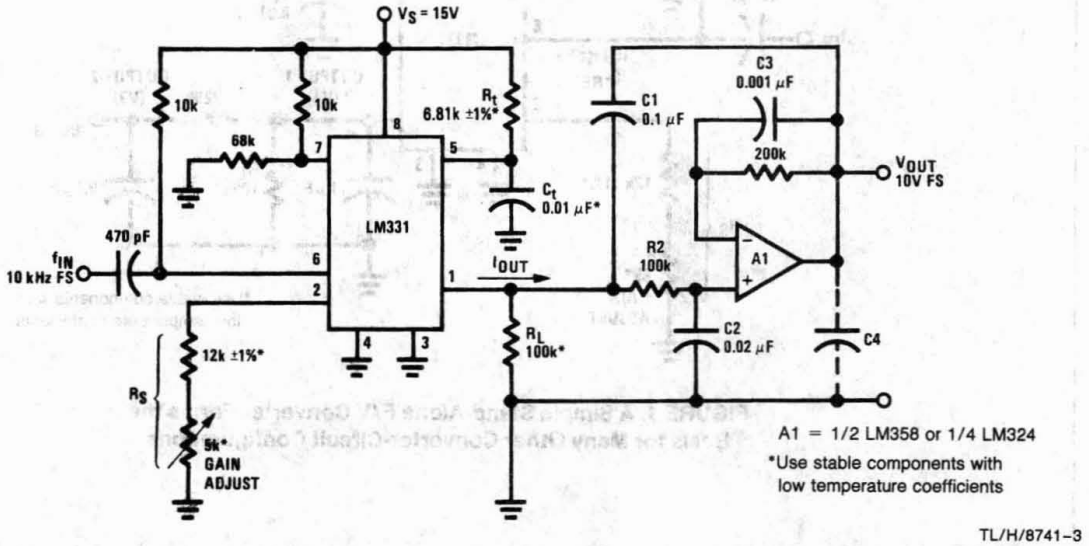

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FIGURE 3. The Op Amp on This F/V Converter's Output Acts as a Buffer as Well as a 2-Pole Filter

Dealing with F/V Converter Ripple

Voltage ripple on the output of F/V converters can present a problem, and the chart shown in *Figure A* indicates exactly how big a problem it is. A simple, slow, RC filter exhibits low ripple at all frequencies. Two-pole filters offer the lowest ripple at high frequencies and provide a 30-times-faster step response than RC devices.

To reduce a circuit's ripple at moderate frequencies, however, you can cascade a second active-filter stage on the F/V converter's output. That circuit's response also appears in *Figure A* and shows a significant improvement in low-ripple bandwidth over the single-active-filter configuration, with only a 30% degradation of step response.

Figures B and *C* show filter circuits suitable for cascading. The inverting filter in *Figure B* requires closely matched resistors with a low TC over their temperature range for best accuracy. For lowest DC error, choose R5 = R2 + ($R_{IN}|R_F$). This circuit's response is

$$-V_{OUT}/V_{IN} = n/(1+(R_F+R2+nR2)C4p+R_FR2C3C4p^2).$$

where n = DC gain. If $R_{IN} = R_F$ and n = 1,

$$-V_{OUT}/V_{IN} = 1/(1+(R_F+2R2)C4p+R_FR2C3C4p^2).$$

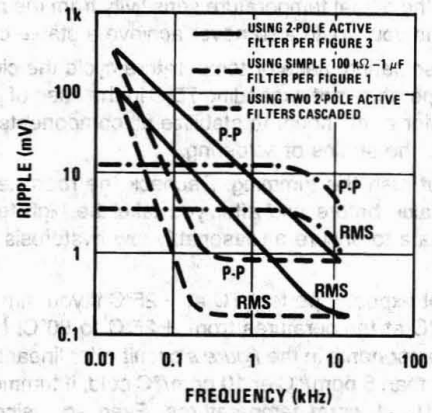

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FIGURE A. Output-Ripple Performance of Several Different F/V Converter Configurations Illustrates the Effect of Voltage Ripple

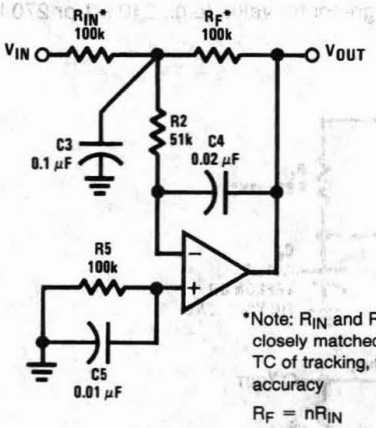

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FIGURE B. You Can Cascade This 2-Pole Inverting Filter onto an F/V Converter's Output

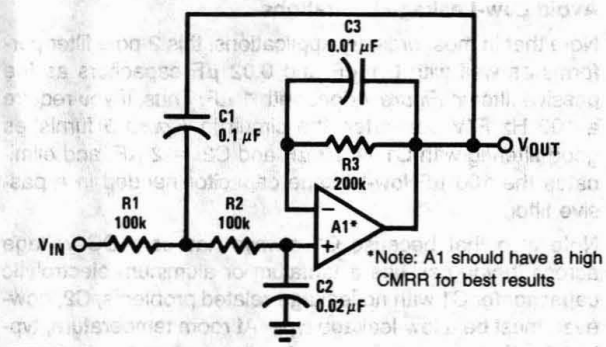

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FIGURE C. This 2-Pole Noninverting Filter Suits Cascade Requirements on F/V Converter Outputs

The circuit shown in *Figure C* does not require precision passive components, but for best accuracy, choosing an A1 with a high CMRR is critical. An LM308A op amp's 96 dB minimum CMRR suits this circuit well, but an LM358B's 85 dB typical figure also proves adequate for many applications. Circuit response is

$$V_{OUT}/V_{IN} = 1/(1 + (R1 + R2)\,C2p + R1R2C1C2p^2).$$

For best results, choose R3 = R1 + R2.

Components Determine Response

The specific response of the circuit in *Figure 3* is

$$V_{OUT}/I_{OUT} = R_L/(1 + (R_L + R2)C2p + R_LR2C1C2C2p^2).$$

Making C2 relatively large eliminates overshoot and sine peaking. Alternatively, making C2 a suitable fraction of C1 (as is done in *Figure 3*) produces both a sine response with 0 dB to 1 dB of peaking and a quick real-time response having only 10% to 30% overshoot for a step response. By maintaining *Figure 3's* ratio of C1:C2 and R2:R_L, you can adapt its 2-pole filter to a wide frequency range without tedious computations.

This filter settles to within 1% of a 5V step's final value in about 20 ms. By contrast, the circuit with the simple RC filter shown in *Figure 1* takes about 900 ms to achieve the same response, yet offers no less ripple than *Figure 3's* op amp approach.

As for the other component in the 2-pole filter, any capacitance between 100 pF and 0.05 μF suits C3 because it serves only as a bypass for the 200 kΩ resistor. C4 helps reduce output ripple in single positive power-supply systems when V_{OUT} approaches so close to ground that the op amp's output impedance suffers. In this circuit, using a tantalum capacitor of between 0.1 μF and 2.2 μF for C4 usually helps keep the filter's output much quieter without degrading the op amp's stability.

Avoid Low-Leakage Limitations

Note that in most ordinary applications, this 2-pole filter performs as well with 0.1 μF and 0.02 μF capacitors as the passive filter in *Figure 1* does with 1 μF. Thus, if you require a 100 Hz F/V converter, the circuit in *Figure 3* furnishes good filtering with C1 = 10 μF and C2 = 2 μF, and eliminates the 100 μF low-leakage capacitor needed in a passive filter.

Note also that because C1 always has zero DC voltage across it, you can use a tantalum or aluminum electrolytic capacitor for C1 with no leakage-related problems; C2, however, must be a low-leakage type. At room temperature, typical 1 μF tantalum components allow only a few nanoamperes of leakage, but leakage this low usually cannot be guaranteed.

Compensating for Temperature Coefficients

F/V converters often encounter temperature-related problems usually resulting from the temperature coefficients of passive components. Following some simple design and manufacturing guidelines can help immunize your circuits against loss of accuracy when the temperature changes.

Capacitors fabricated from Teflon or polystyrene usually exhibit a TC of −110 ±30 ppm/°C. When you use such a component for the timing capacitor in an F/V converter (such as C_t in the *figure*) the circuit's output voltage—or the gain in terms of volts per kilohertz—also exhibits a −110 ppm/°C TC.

But the resistor-diode network (R_X, D1, D2) connected from pin 2 to ground in the *figure* can cancel the effect of the timing capacitor's large TC. When R_X = 240 kΩ, the current flowing through pin 1 will then have an overall TC of 110 ppm/°C, effectively canceling a polystyrene timing capacitor's TC to a first approximation. Thus, you needn't find a zero-TC capacitor for C_t, so long as its temperature coefficient is stable and well established. As an additional advantage, the resistor-diode network nearly compensates to zero the TC of the rest of the circuit.

Bake it for a While

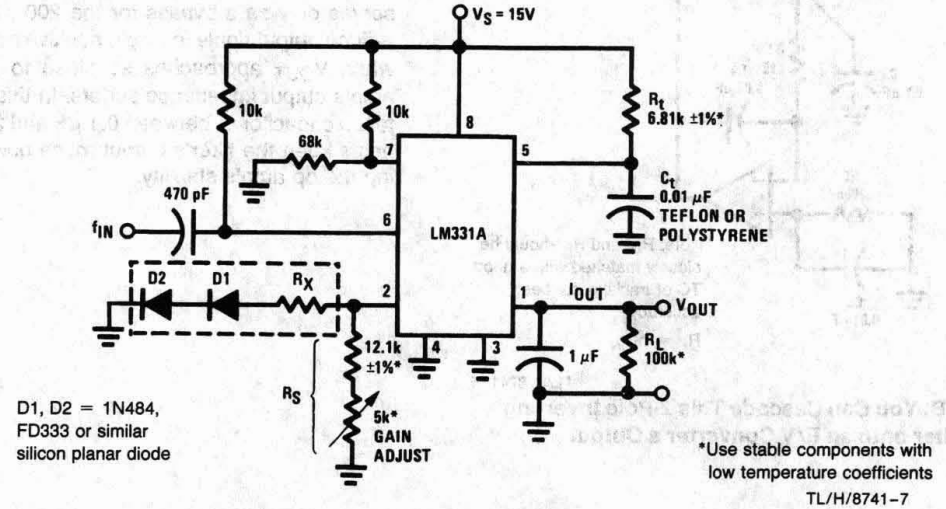
After the circuit has been built and checked out at room temperature, a brief oven test will indicate the sign and the size of the TC for the complete F/V converter. Then you can add resistance in series with R_X, or add conductance in parallel with it, to greatly diminish the TC previously observed and yield a complete circuit with a lower TC than you could obtain simply by buying low TC parts.

For example, if the circuit increases its full-scale output by 0.1% per 30°C (33 ppm/°C) during the oven test, adding 120 kΩ in series with R_X = 240 kΩ cancels the temperature-caused deviation. Or, if the full-scale output decreases by −0.04% per 20°C (−20 ppm/°C), just add 1.2 MΩ in parallel with R_X.

Note that to allow trimming in both directions, you must start with a finite *fixed* TC (such as the −110 ppm/°C of C_t), which then nominally cancels out by the addition of a finite *adjustable* TC. Only by using this procedure can you compensate for whatever polarity of TC is found by the oven test.

You can utilize this technique to obtain TCs as low as 20 ppm/°C, or perhaps even 10 ppm/°C, if you take a few passes to zero-in on the best value for R_X. For optimum results, consider the following guidelines:

- Use a good capacitor for C_t; the cheapest polystyrene capacitors can shift value by 0.05% or more per temperature cycle. In that case, you would not be able to distinguish the actual temperature sensitivity from the hysteresis, and you would also never achieve a stable circuit.
- After soldering, bake or temperature-cycle the circuit (at a temperature not exceeding 75°C in the case of polystyrene) for a few hours to stabilize all components and to relieve the strains of soldering.
- Do not rush the trimming. Recheck the room temperature value before *and* after you take the high temperature data to ensure a reasonably low hysteresis per cycle.
- Do not expect a perfect TC at −25°C if you trim for ±5 ppm/°C at temperatures from +25°C to 60°C. None of the components in the *figure's* circuit offer linearity much better than 5 ppm/°C or 10 ppm/°C cold, if trimmed for a zero TC at warm temperatures. Even so, using these techniques you can obtain a data converter with better than 0.02% accuracy and 0.003% linearity, for a ±20°C range around room temperature.
- Start out the trimming with R_X installed and its value near the design-center value (e.g., 240 kΩ or 270 kΩ), so you



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Two Diodes and a Resistor Help Decrease an F/V Converter's Temperature Coefficient

will be reasonably close to zero TC; you will usually find the process slower if you start without any resistor, because the trimming converges more slowly.

- If you change R_X from 240 kΩ to 220 kΩ, do not pull out the 240 kΩ part and put in a new 220 kΩ resistor—you will get much more consistent results by adding a 2.4 MΩ resistor in parallel. The same admonition holds true for adding resistance in series with R_X.
- Use reasonably stable components. If you use an LM331A (±50 ppm/°C maximum) and RN55D film resistors (each ±100 ppm/°C) for R_L, R_t and R_S, you probably won't be able to trim out the resulting ±350 ppm/°C worst-case TC. Resistors with a TC specification of 25 ppm/°C usually work well. Finally, use the same resistor value (e.g., 12.1 kΩ ±1%) for both R_S and R_t; when these resistors come from the same manufacturer's batch, their TC tracking will usually rate at better than 20 ppm/°C.

Whenever an op amp is used as a buffer (as in *Figure 3*), its offset voltage and current (±7.5 mV maximum and ±100 nA, respectively, for most inexpensive devices) can cause a ±17.5 mV worst-case output offset. If both plus and minus supplies are available, however, you can easily provide a symmetrical offset adjustment. With only one supply, you can add a small positive current to each op amp input and also trim one of the inputs.

Need a Negative Output?

If your F/V converter application requires a negative output voltage, the circuit shown in *Figure 4* provides a solution with excellent linearity (±0.003% typical, ±0.01% maximum). And because pin 1 of the LM331 always remains at 0 V_{DC}, this circuit needs no cascade transistor. (Note, however, that while the circuit's nonlinearity error is negligible, its ripple is not.)

The circuit in *Figure 4* offers a significant advantage over some other designs because the offset adjust voltage derives from the stable 1.9 V_{DC} reference voltage at pin 2 of the LM331; thus any supply voltage shifts cause no output shifts. The offset pot can have any value between 200 kΩ and 2 MΩ.

An optional bypass capacitor (C2) connected from the op amp's positive input to ground prevents output noise arising from stray noise pickup at that point; the capacitance value is not critical.

A Familiar Response

The circuit in *Figure 4* exhibits the same 2-pole response—with heavy output ripple attenuation—as the noninverting filter in *Figure 3*. Specifically,

$$V_{OUT}/I_{OUT} = R_F/(1 + (R4 + R_F)C4p + R4R_FC3C4p^2).$$

Here also, R5 = R4 + R_F = 200 kΩ provides the best bias current compensation.

The LM331 can handle frequencies up to 100 kHz by utilizing smaller-value capacitors as shown in *Figure 5*. This circuit increases the current at pin 2 to facilitate high-speed switching, but, despite these speed-ups, the LM331's 500 ppm/°C TC at 100 kHz causes problems because of switching speed shifts resulting from temperature changes.

To compensate for the device's positive TC, the LM334 temperature sensor feeds pin 2 a current that decreases linearly with temperature and provides a low overall temperature coefficient. An R_y value of 30 kΩ provides first-order compensation, but you can trim it higher or lower if you need more precise TC correction.

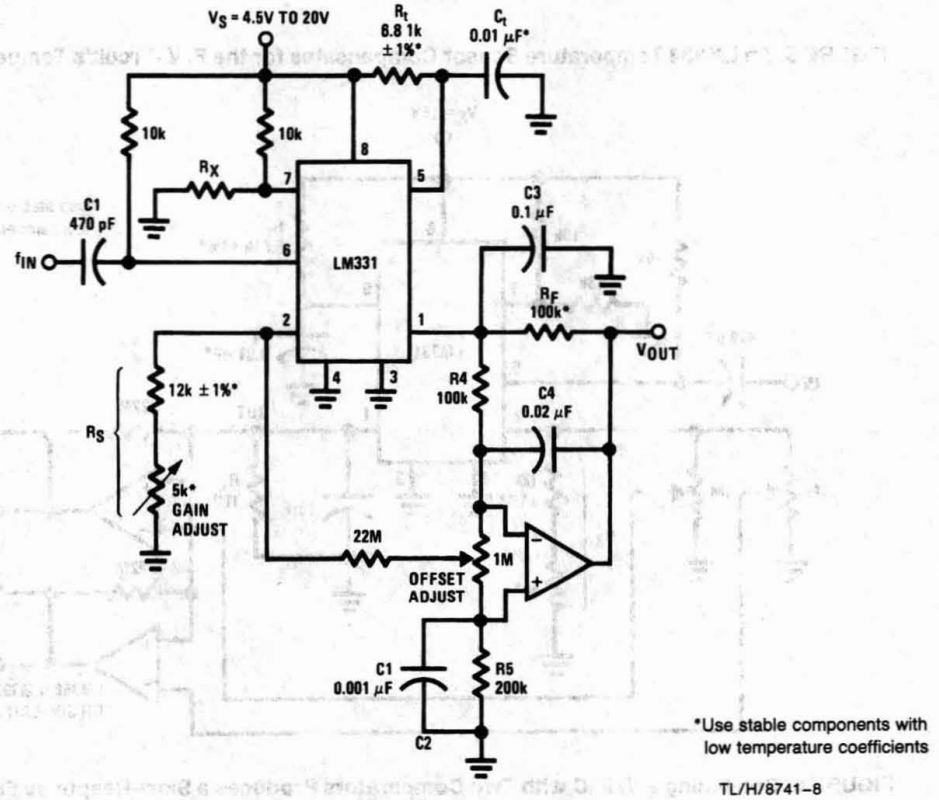

FIGURE 4. In This F/V Circuit, the Output-Buffer Op Amp Derives its Offset Voltage from the Precision Voltage Source at Pin 2 of the LM331

Detect Frequencies Accurately

Using an F/V converter combined with a comparator as a frequency detector is an obvious application for these devices. But when the F/V converter is utilized in this way, its output ripple hampers accurate frequency detection, and the slow filter frequency response causes delays.

If a quick response is not important, though, you can effectively utilize an LM331-based F/V converter to feed one or more comparators, as shown in *Figure 6*. For an input frequency drop from 1.1 kHz to 0.5 kHz, the converter's output responds within about 20 ms. When the input falls from 9 kHz to 0.9 kHz, however, the output responds only after a 600 ms lag, so utilize this circuit only in applications that can tolerate F/V circuits' inherent delays and ripples.

Author's Biography

Bob Pease is a staff scientist in the Advanced Linear Integrated Circuit Group at National Semiconductor Corp., Santa Clara, CA. Holder of four patents, he earned a BSEE from MIT. Bob lists tracking abandoned railroad roadbeds and designing V/F converters as hobbies.

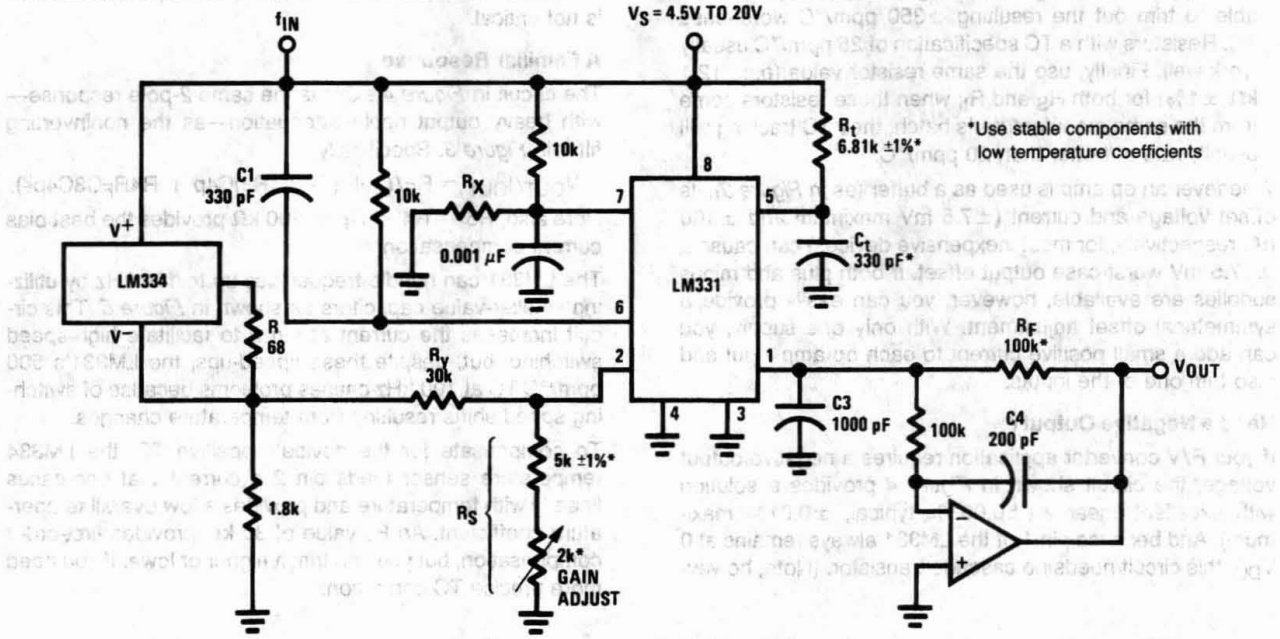

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FIGURE 5. An LM334 Temperature Sensor Compensates for the F/V Circuit's Temperature Coefficient

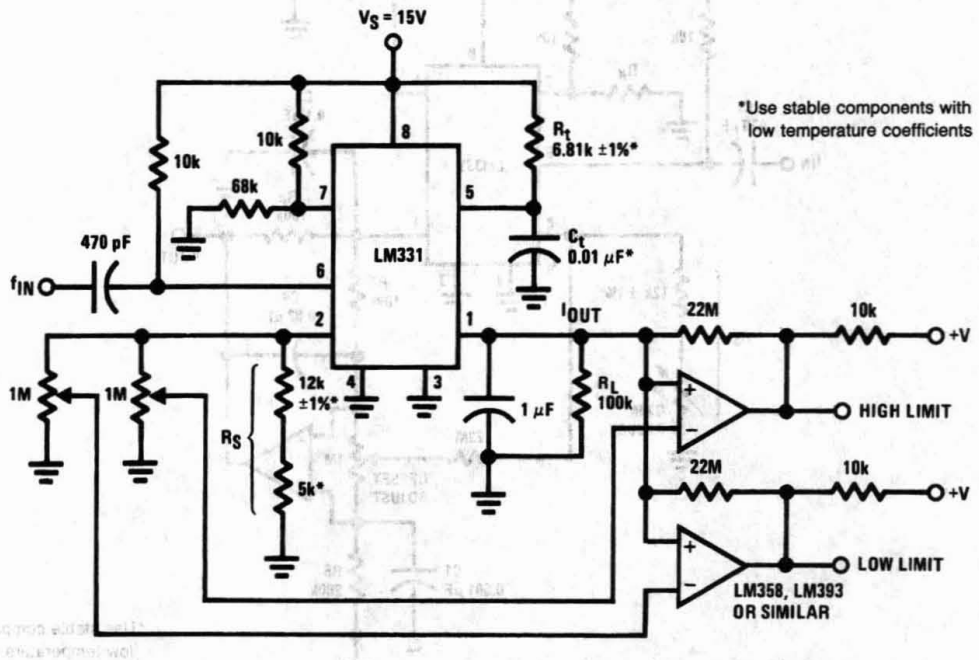

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FIGURE 6. Combining a V/F IC with Two Comparators Produces a Slow-Response Frequency Detector

Versatile Monolithic V/Fs Can Compute as Well as Convert with High Accuracy

National Semiconductor
Appendix D
Robert A. Pease

The best of the monolithic voltage-to-frequency (V/F) converters have performance that's so good it equals or exceeds that of modular types. Some of these ICs can be designed into quite a variety of circuits because they're notably versatile. Along with versatility and high performance come the advantages that are characteristic of all V/F converters, including good linearity, excellent resolution, wide dynamic range, and an output signal that's easy to transmit as well as couple through an isolator.

One of the recently introduced monolithic types, the LM131, has both high performance and a design that's rather flexible. For instance, it can compute and convert at the same time; the computation is a part of the conversion. Among other functions, it can provide the product, ratio and square root of analog inputs.

This IC has an internal reference for its conversion circuitry that's also brought out to a pin, so it's available to external circuits associated with the converter. Not surprisingly, it turns out that any deviations of the reference, due to process variations and temperature changes have equal and opposite effects on the scale factors of the converter and the external circuitry. (This presumes, of course, that the scale factor of the external circuitry is a linear function of voltage.)

PRECISION RELAXATION OSCILLATOR

Before looking at some applications, quickly take a look at the basic circuit of an LM131 V/F converter *(Figure 1).* Basically, this IC, like any V/F converter, is a precision relaxation oscillator that generates a frequency linearly proportional to the input voltage. As might be expected, the circuit has a capacitor, C_L, with a sawtooth voltage on it. Generally speaking, the circuit is a feedback loop that keeps this capacitor charged to a voltage very slightly higher than the input voltage, V_{IN}. If V_{IN} is high, C_L discharges relatively quickly through R_L, and the circuit generates a high frequency. If V_{IN} is low, C_L discharges slowly, and the converter puts out a low frequency.

When C_L discharges to a voltage equal to the input, the comparator triggers the one-shot. The one-shot closes the current switch and also turns on the output transistor. With the switch closed, current from the current source recharges C_L to a voltage somewhat higher than the input. Charging continues for a period determined by R_T and C_T. At the end of this period, the one-shot returns to its quiescent state and C_L resumes discharging.

Resistor R_S sets the amount of current put out by the current source. In fact, the current in pin 1, with the switch on, is identical to the current in pin 2. The latter pin is at a constant voltage (nominally 1.90V), so a given resistor value can set the operating currents. When connected to a high impedance buffer, this pin provides a stable reference for external circuits.

The open-collector output at pin 3 permits the output swing to be different from the converter's supply voltage, if the load circuit requires. The supplies don't have to be separate, however, and both the converter and its load can use the same voltage.

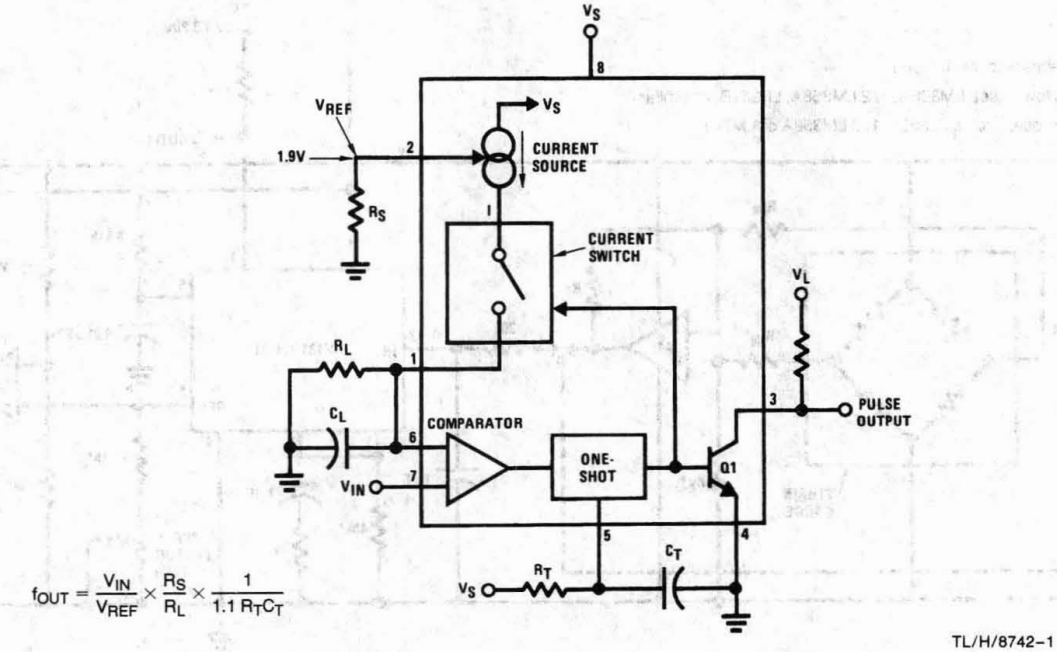

FIGURE 1. A voltage-to-frequency converter such as this is a relaxation oscillator with a frequency proportional to the input voltage. Current pulses keep C_L's average voltage slightly greater than the input voltage.

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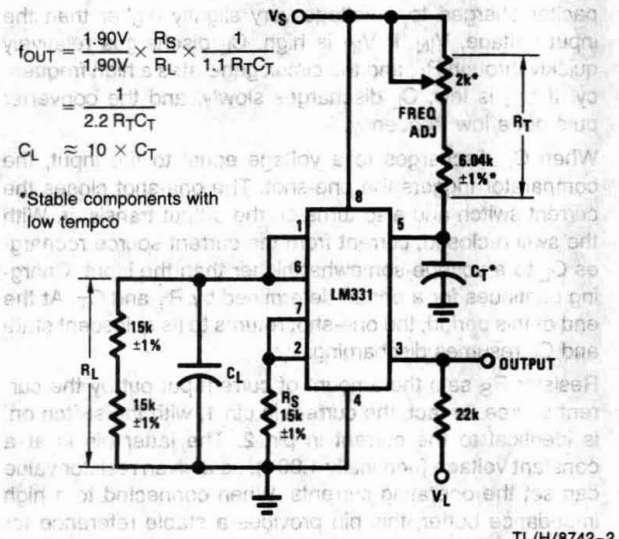
STEADY AS SHE GOES

By far the simplest of the circuits that make use of the reference output voltage from the LM131 is one that simply ties this output pin right back to the signal input. This connection is just a V/F converter with a constant input, which makes it a constant-frequency oscillator. Even with this simple circuit *(Figure 2),* variations in the reference voltage have two opposite effects that cancel each other out, so the circuit is particularly stable. In this type of circuit, the temperature-dependent internal delays tend to cancel as well, which isn't true of relaxation oscillators based on op amps or comparators.



TL/H/8742–2

FIGURE 2. A V/F converter is a stable-frequency oscillator if its input is connected to its reference output. If the reference voltage changes, the effects of the change cancel out, so the frequency doesn't change. With low tempco components for R_T and C_T, frequency stability vs temperature can be as good as ±25 ppm/°C.

Resistors R_L and R_S are best taken from the same batch. (R_L must be larger than R_S, so it's made up of two resistors.) By doing this, the tempco tracking, which is the critical parameter, is five to ten times better than it would be if R_L were a single 30.1 kΩ resistor.

Although the reference output, pin 2, can't be loaded without affecting the converter's sensitivity, the comparator input, pin 7, has a high impedance so this connection does no harm.

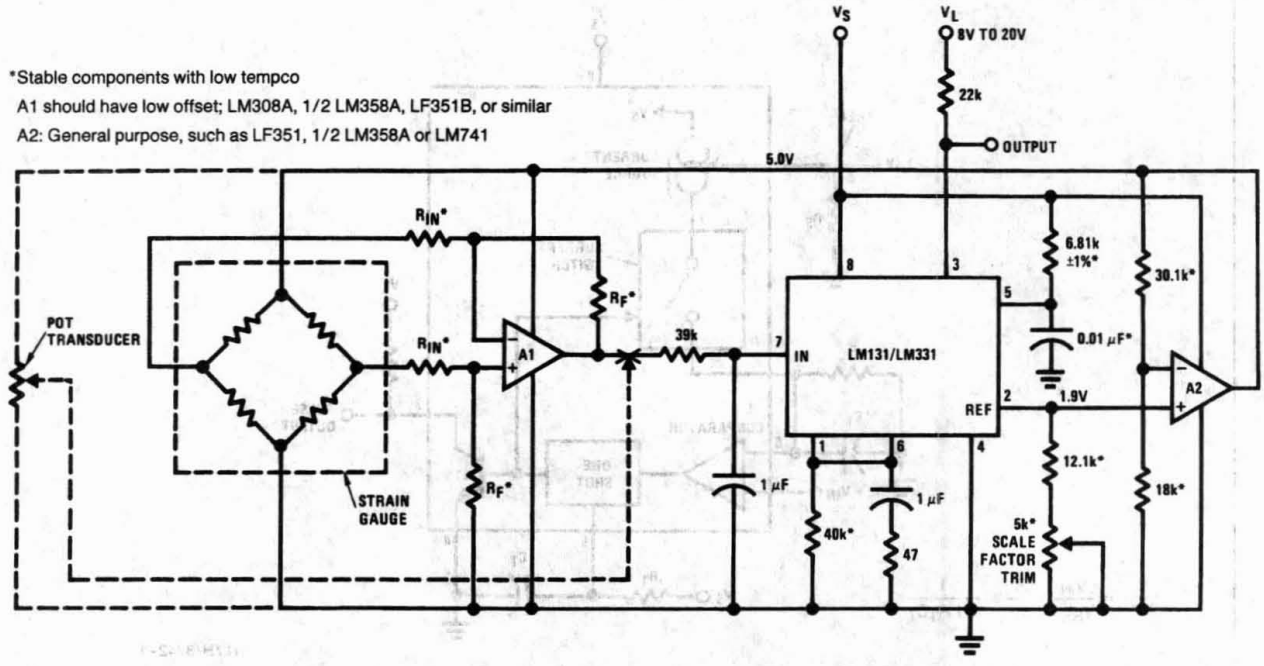
Frequency stability is typically ±25 ppm/°C, even with an LM331, which as a V/F converter is specified only to 150 ppm/°C maximum. From 20 Hz to 20 kHz, stability is excellent, and the circuit can generate frequencies up to 120 kHz.

Although the simplest way of using the reference output is to tie it back to the input, the reference can also be buffered and amplified to supply such external circuitry as a resistive transducer, which might be a strain gauge or a pot *(Figure 3).* As in the stable oscillator already described, deviations of the internal reference voltage from the ideal cause the transducer's and the converter's sensitivities to change equally in opposite directions, so the effects cancel.

In this circuit, op amp A2 buffers and amplifies the constant voltage at pin 2 of the converter to provide the 5V excitation for the strain gauge. Amplifier A1, connected as an instrumentation amplifier, raises the output of the strain gauge to a usable level while rejecting common-mode pickup.

A potentiometer-type transducer works just as well with this circuit. Its wiper output takes the place of A1's output as shown at the X.

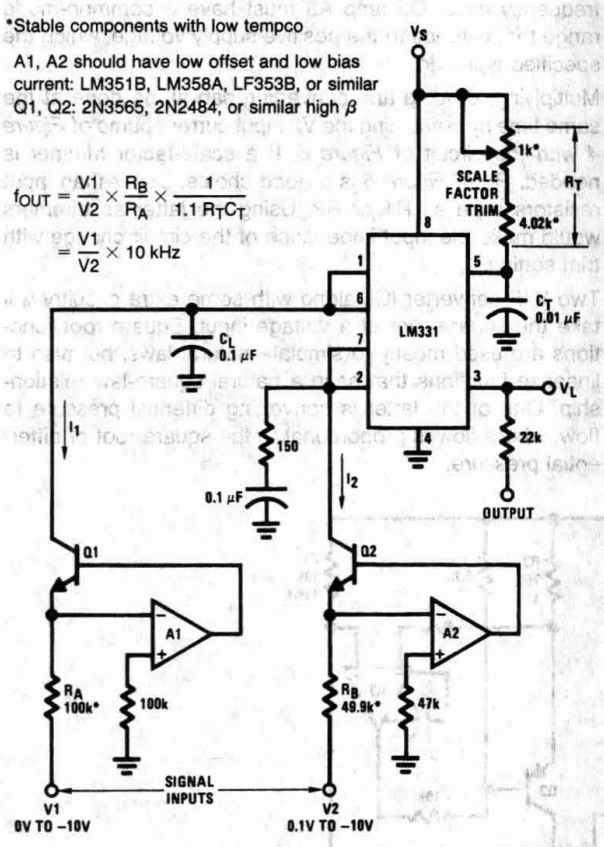
The reference terminal is both a constant voltage output and a current programming input. So far, it's been shown simply with one or two resistors going to ground. It is, however, a full-fledged signal input that accepts a signal from a current source quite well.



TL/H/8742–3

FIGURE 3. In this strain-to-frequency converter, the converter's reference excites the strain gauge (or the optional pot) through buffer amp A2. This makes the circuit insensitive to changes in the reference voltage.

This extra input is what enables the LM131 to compute while converting. For instance, it will convert the ratio of two voltages to a frequency proportional to the ratio *(Figure 4)*. The circuit is still a V/F converter, but has two signal inputs, both of them going to rather unorthodox places at that. The inputs, shown as voltages, are converted to currents by two current pumps (voltage-to-current converters). Of course, if currents of the proper ranges are available, the current pumps aren't needed. The left current pump, which includes Q1 and A1, determines how fast capacitor C_L discharges between output pulses. The other pump sets the current in the reference circuit to control the amount of recharge current when the one-shot fires. Tying the comparator input, pin 7, to the reference pin sets the comparator's trip point at a constant voltage.

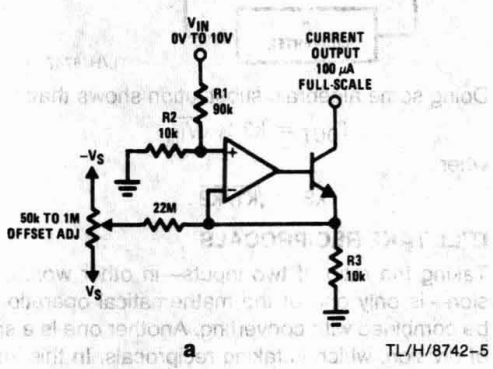


TL/H/8742–4

FIGURE 4. This circuit converts the ratio of two voltages to an equivalent frequency without a separate analog divider. Full-scale output is 15 kHz. The two op amp circuits convert the inputs to proportional currents.

To get an idea of how the circuit works, consider first the effect of, for instance, tripling the input voltage, V1. This make C_L discharge to the comparator trip point three times as fast, so the frequency triples. Next, consider a given change, such as doubling the voltage at the other input, V2. This doubles the recharge current to C_L during the fixed-width output pulse, which means C_L's voltage increases twice as much during recharging. Since the discharge into Q1 is linear (for V1 constant), it takes twice as long for C_L to discharge—the frequency becomes half of what it was before.

Although the current pumps in *Figure 4* must have negative inputs, rearranging the op amps according to *Figure 5* makes them accept positive inputs instead. Trimming out the offset in the op amp gives the ratio converter better linearity and accuracy. The trim circuit in *Figure 5a* needs stable positive and negative supplies for the offset trimmer, while the one in *Figure 5b* needs only a stable positive supply. Unmarked components in *Figure 5b* are the same as in *Figure 5a.*



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R1, R2, R3: Stable components with low tempco

Q1: $\beta \geq 330$

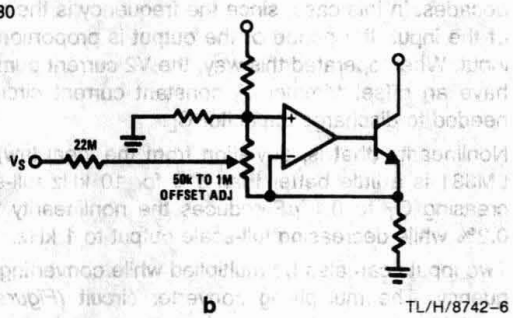

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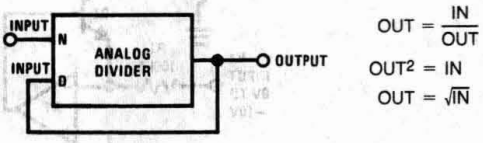
FIGURE 5. These current pumps adapt the converter circuits in *Figures 4* and *6* to positive input voltages. Optional offset trimming improves linearity and accuracy, especially with input signals that have a wide dynamic range.

Note that the full-scale range of the current pumps can be changed by varying the value of the input resistor(s). If either of these pump circuits is used with a single positive supply, the op amp should be a type such as 1/2 LM358 or 1/4 LM324, which has a common-mode range that includes the negative-supply bus.

COMPUTING SQUARE ROOTS IMPLICITLY

An analog divider computes the square root of a signal when the signal is fed to the divider's numerator input, and the output is fed back to the divider's denominator input.



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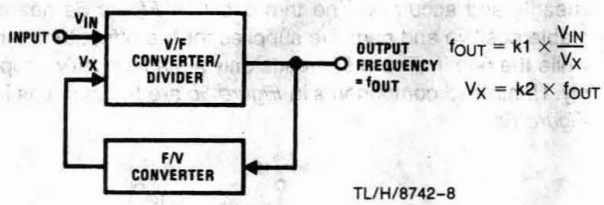
This type of computation is called implicit, because the end result of the computation is only implied, not explicitly stated by the equation that defines the computation.

In the implicit square root computing loop described in the text, a V/F converter serves as a divider. Since it's a converter, its inputs are voltages (or currents), but its output is a frequency. To connect its output back to one of its inputs so it will compute a square root means that its output frequency must be converted back to a voltage. This is taken care of by the frequency-to-voltage converter.



TL/H/8742–8

Doing some algebraic substitution shows that:

$$f_{OUT} = k3 \times \sqrt{V_{IN}}$$

where

$$k3 = \sqrt{k1/k2}\,.$$

IT'LL TAKE RECIPROCALS

Taking the ratio of two inputs—in other words, doing division—is only one of the mathematical operations that can be combined with converting. Another one is a special case of division, which is taking reciprocals. In this instance, the numerator (V1 in *Figure 4*) is held constant, and the denominator, V2, changes over a wide range such as one or two decades. In this case, since the frequency is the reciprocal of the input, the period of the output is proportional to the input. When operated this way, the V2 current pump should have an offset trimmer. A constant current circuit is still needed to discharge capacitor C_L.

Nonlinearity (that is, deviation from the ideal law) with an LM331 is a little better than 1% for 10 kHz full-scale. Increasing C_T to 0.1 μF reduces the nonlinearity to below 0.2% while decreasing full-scale output to 1 kHz.

Two inputs can also be multiplied while converting to a frequency. The multiplying converter circuit *(Figure 6)* that does this has a more elaborate current pump than the ratio circuit of *Figure 4*. This pump is really two cascaded circuits; it includes op amps A2 and A3 as well as transistors Q2 and Q3. Current from this pump goes to pin 5 to control the one-shot's pulse width. (This current ranges from 13.3 μA to 1.33 mA.)

As in the ratio circuit, the left current pump controls the discharge rate of C_L. The other pump, however, controls the one-shot's pulse width to vary the amount that C_L charges during the pulse. If the V2 input is close to zero, the current from the pump into pin 5 is small, and the one-shot develops a wide pulse. This allows C_L to charge quite a bit. It takes a relatively long time for C_L to discharge to the comparator threshold, so the resulting frequency is low. As V2 goes negative (a greater absolute magnitude), the output frequency rises. Op amp A3 must have a common-mode range that extends to the positive supply voltage, which the specified types do.

Multiplying, dividing and converting can all be done at the same time by combining the V2 input current pump of *Figure 4* with the circuit of *Figure 6*. If a scale-factor trimmer is needed, R4 in *Figure 6* is a good choice, better than input resistors such as R1 or R2. Using the latter as trimmers would make the input impedance of the circuit change with trim setting.

Two V/F converter ICs along with some extra circuitry will take the square root of a voltage input. Square root functions are used mostly to simulate natural laws, but also to linearize functions that have a natural square-law relationship. One of the latter is converting diffential pressure to flow, where flow is proportional to the square root of differential pressure.

*Stable components with low tempco

$$f_{OUT} = \frac{V1}{10V} \times \frac{V2}{10V} \times 10\ kHz$$

V_S = 15V, regulated and stable

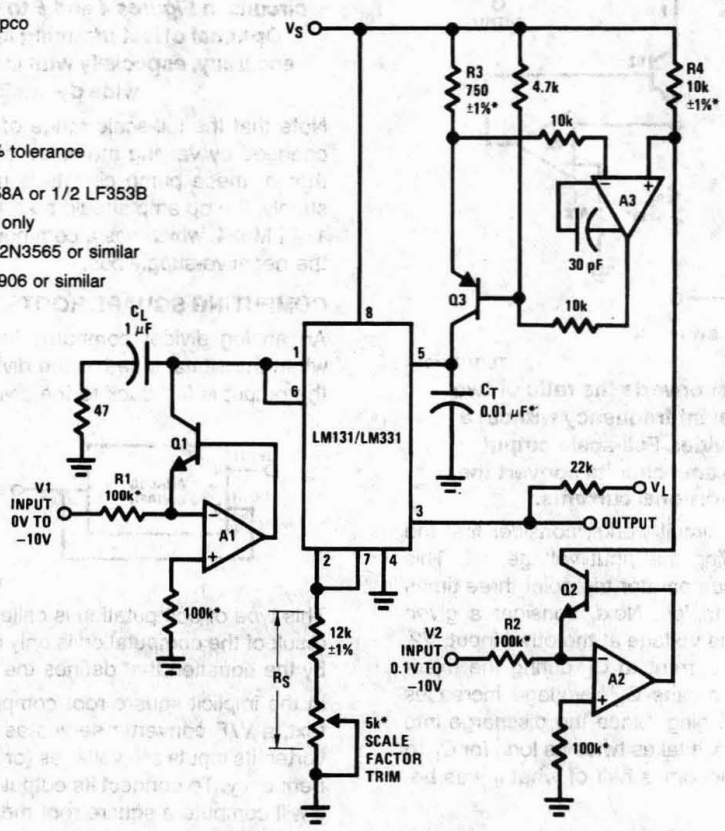
$$R3 = \left(\frac{15.00V}{+V_S} \times 750\Omega \text{ with } \pm 1\% \text{ tolerance}\right.$$

A1, A2: Each is 1/2 LM158/LM358A or 1/2 LF353B

A3: LM301A, LM307, or LF13741 only

Q1, Q2: High β such as 2N2484, 2N3565 or similar

Q3: High β such as 2N4250, 2N3906 or similar



TL/H/8742–9

FIGURE 6. The product of two input voltages becomes an equivalent frequency in this converter. A current pump that includes op amps A2 and A3 controls the pulse duration of the converter's internal one-shot.

VERSATILE PIN FUNCTIONS GIVE DESIGN FLEXIBILITY

Two features—the reference and the one-shot—of the LM131/LM331 V/F converter deserve a closer look because they are the key to its versatility. The simplified schematic of the chip, shown here along with a transducer and the components needed for a basic V/F converter, will help to illustrate how these features work.

The reference circuit, connected to pin 2, is both a constant voltage output and a current setting, scale-factor control input. The constant voltage can supply external circuitry, such as the transducer, that feeds the converter's input.

One great advantage of using the converter's internal reference to supply the external circuitry is that any variation in the reference voltage affects the sensitivities of the converter and the external circuitry by equal and opposite amounts, so the effects of the variation cancel.

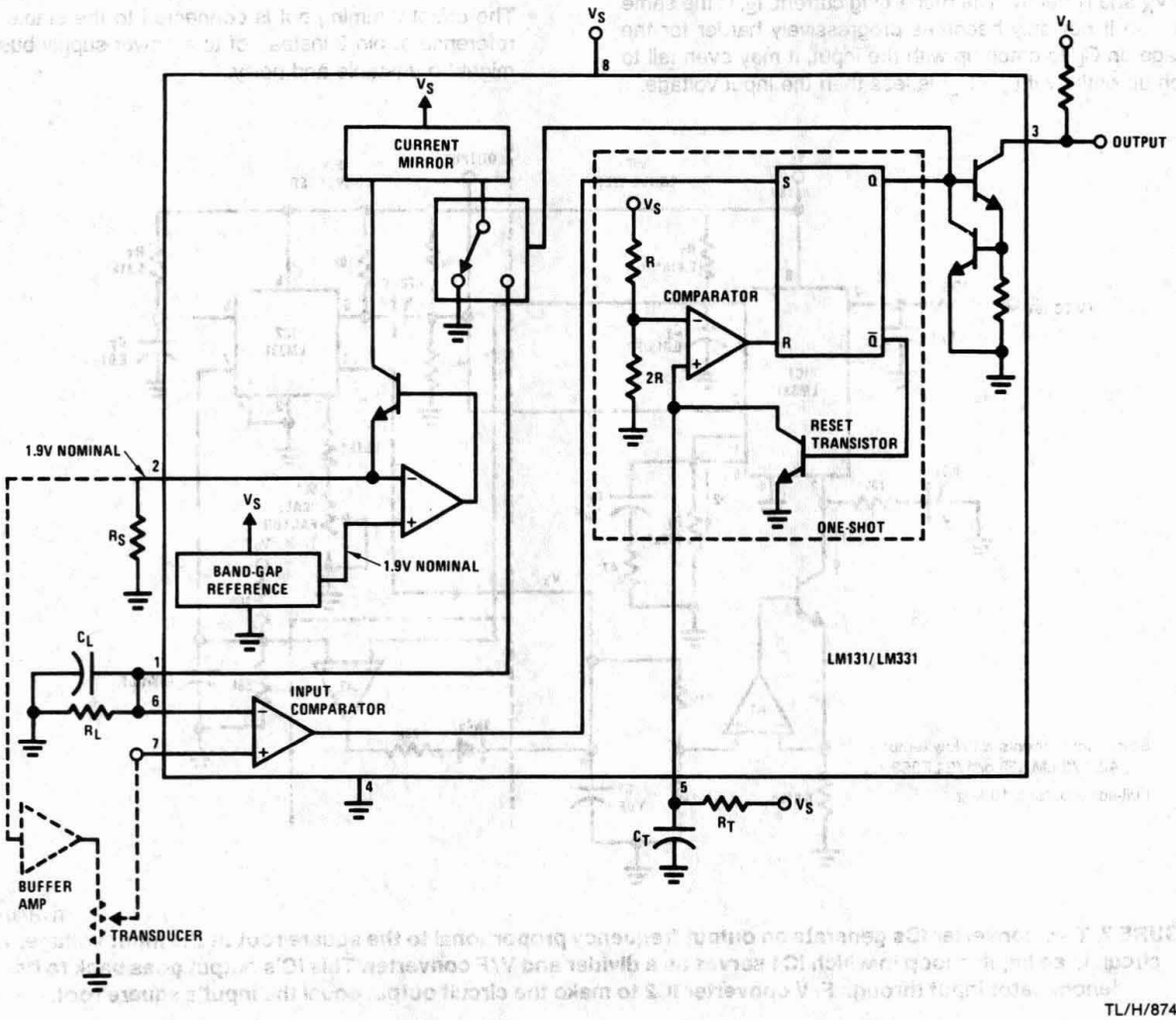
While providing a constant voltage output, pin 2 also provides scale-factor, or sensitivity control for the converter. Current supplied to an external circuit by this terminal comes from the supply (V_S) through the current mirror and the transistor. The op amp drives this transistor to hold pin 2 at a constant voltage equal to the internal reference, which is nominally 1.9V.

The current mirror provides a current to the switch that's essentially identical to that in pin 2. This means that a resistor to ground or a signal from a current source will set the current that is switched to pin 1. In most circuits, a capacitor goes from pin 1 to ground, and the switched current from this pin recharges the capacitor during the pulse from the one-shot.

The one-shot circuit is somewhat like the well known 555 timer's circuit. In the quiescent state, the reset transistor is on and holds pin 5 near ground. When pin 7 becomes more positive than pin 6 (or pin 6 falls below pin 7), the input comparator sets the flip-flop in the one-shot.

The flip-flop turns on the current limited output transistor (pin 3) and switches the current coming from the current mirror to pin 1. The flip-flop also turns off the reset transistor, and the timing capacitor C_T starts to charge toward V_S. This charge is exponential, and C_T's voltage reaches 2/3 of V_S in about 1.1 R_TC_T time constants. (The quantity 1.1 is $-\ln 0.333...$) When pin 5 reaches this voltage, the one-shot's comparator resets the flip-flop which turns off the current to pin 1, discharges C_T, and turns off the output transistor.

If the voltages at pins 6 and 7 still call for setting the flip-flop after pin 5 has reached 2/3 V_S, internal logic not shown in this simplified diagram overrides the reset signal from the one-shot's own comparator, and the flip-flop stays set. In this instance, C_T continues charging past 2/3 V_S.



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ROOT LOOP COMPUTES

The circuit in *Figure 7* is an implicit loop (see "Computing Square Roots Implicitly") that uses IC1 as a voltage-to-frequency converter and divider, and IC2 as a frequency-to-voltage converter. The F/V converter, IC2, and the current pump that includes A1 and the transistor return the output of IC1 to its denominator input. A relatively elaborate feedback circuit like this is needed to convert IC1's frequency output back to a current for its denominator input.

Looking at the circuit in more detail, IC1 puts out a frequency proportional to V_{IN} divided by the feedback voltage, V_X. The current I_1 is generated by a current pump that has V_X as its input *(Figure 5a)*. To develop the feedback IC2 converts the pulse output from IC1 into standard width precision current pulses that charge capacitor C1. This capacitor integrates them into the voltage V_X, thus closing the loop.

Op amp A2, serving as a comparator, ensures that the circuit will always start and continue running. If V_{IN} suddenly jumps to a higher voltage, one pulse from the one-shot in IC1 may not be enough to recharge C_L to a voltage higher than the input. In such a case, the IC's internal logic keeps its internal current switch turned on, and the voltage on C_L ramps up until it exceeds the input. During this time, however, IC1's output hasn't changed state. (Such a temporary hang-up isn't unique to this circuit, and equivalent things happen to other V/Fs besides the LM131/LM331.) What is worse here, though, is that the lack of pulses to IC2 means that V_X and I_1 decay. The recharging current, I_2, is the same as I_1, so it not only becomes progressively harder for the voltage on C_L to catch up with the input, it may even fail to catch up entirely if $(I_2 \times R_L)$ is less than the input voltage.

As a sign of this condition, when the converter hangs up, the one-shot's timing node, pin 5, continues to charge well beyond its normal peak of 2/3 V_S. As soon as the comparator A2 detects this rise, it pulls up voltage V_X, current I_1 increases, and the loop catches its breath again.

After all these nonlinear computations, this last circuit is about as linear as it can be. It's a precision, ultralinear V/F converter based on an LM331A *(Figure 8)* that has several detail refinements over previous V/F converter circuits. Choosing the proper components and trimming the tempco give less than 0.02% error and 0.003% nonlinearity for a ±20°C range around room temperature.

This circuit has an active integrator, which includes the op amp and the integrating feedback capacitor, C_F. The integrator converts the input voltage, which is negative, into a positive-going ramp. When the ramp reaches the converter IC's comparator threshold, the one-shot fires and switches a pulse of current to the integrator's summing junction. This current makes the integrator's output ramp down quickly. When the one-shot times out, the cycle repeats.

There are several reasons this converter circuit gives high performance:

- A feedback limiter prevents the op amp from driving pin 7 of the LM331A negative. The limiter circuit arrangement bypasses the leakage through CR5 to ground via R5, so it won't reach the summing junction. Bypassing leakage this way is especially important at high temperatures.
- The offset trimming pot is connected to the stable 1.9V reference at pin 2 instead of to a power supply bus that might be unstable and noisy.

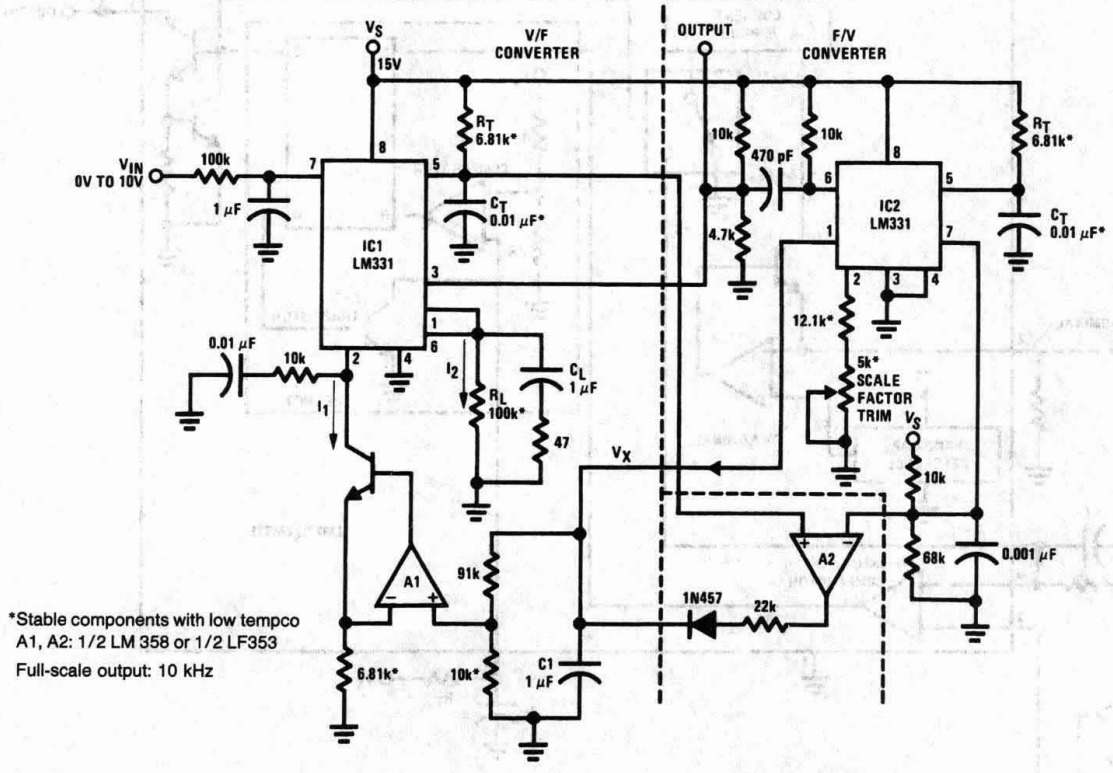

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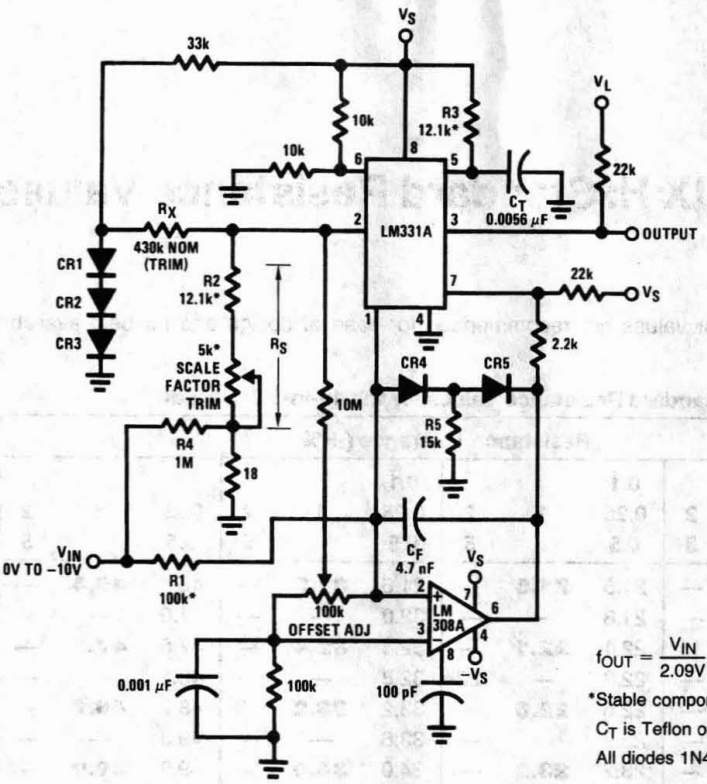
FIGURE 7. Two converter ICs generate an output frequency proportional to the square root of the input voltage. The circuit is an implicit loop in which IC1 serves as a divider and V/F converter. This IC's output goes back to its denominator input through F/V converter IC2 to make the circuit output equal the input's square root.



$$f_{OUT} = \frac{V_{IN}}{2.09V} \times \frac{R_S}{R1} \times \frac{1}{R_3 C_T}$$ Full-scale output 10 kHz

*Stable components with low tempco; see text

C_T is Teflon or Polystyrene

All diodes 1N457, 1N484, or FD333 (low-leakage silicon)

TL/H/8742–12

FIGURE 8. An ultraprecision V/F converter, capable of better than 0.02% error and 0.003% nonlinearity for a ±20°C range about room temperature, augments the basic converter with an external integrator.

- A small fraction (180 μV, full-scale) of the input voltage goes via R4 to the R_S network, which improves the nonlinearity from 0.004% to 0.002%.
- Resistors R2 and R3 are the same value, so that resistors such as Allen-Bradley type CC metal-film types can provide excellent tempco tracking at low cost. (This tracking is very good when equal values come from the same batch.) Resistor R1 should be a low tempco metal-film or wirewound type, with a maximum tempco of ±10 ppm/°C or ±25 ppm/°C.

In addition, C_T should be a polystyrene or Teflon type. Polystyrene is rated to 80°C, while Teflon goes to 150°C. Both types can be obtained with a tempco of −110 ±30 ppm/°C. Choosing this tempco for C_T makes the tempco, due to C_T, of the full-scale output frequency 110 ppm/°C.

Using tight tolerance components results in a total tempco between 0 ppm/°C and 220 ppm/°C, so the tempco will never be negative. The voltage at CR1 and R_X has a tempco of −6 mV/°C, which can be used to compensate the tempco of the rest of the circuit. Trimming R_X compensates for the tempco of the V/F IC, the capacitor, and all the resistors.

A good starting value for selecting R_X is 430 kΩ, which will give the 135 μA flowing out of pin 2 a slope of 110 ppm/°C. If the output frequency increases with temperature, a little more conductance should be added in parallel with R_X.

When doing a second round of trimming, though, note that a resistor of, say, 4.3 MΩ, has about the same effect on tempco when shunted across a 220 kΩ resistor that it does when shunted across one of 430 kΩ, namely, −11 ppm/°C. This technique can give tempcos below ±20 ppm/°C or even ±10 ppm/°C.

Some precautions help this procedure converge:

1. Use a good capacitor for C_T. The cheapest polystyrene capacitors will shift in value by 0.05% or more per temperature cycle. The actual temperature sensitivity would be indistinguishable from the hysteresis, and the circuit would never be stable.
2. After soldering, bake and/or temperature-cycle the circuit (at a temperature not exceeding 75°C if C_T is polystyrene) for a few hours, to stabilize all components and to relieve the strains from soldering.
3. Don't rush the trimming. Recheck the room temperature value, before and after the high temperature data are taken, to ensure that hysteresis per cycle is reasonably low.
4. Don't expect a perfect tempco at −25°C if the circuit is trimmed for ±5 ppm/°C between 25°C and 60°C. If it's been trimmed for zero tempco while warm, none of its components will be linear to much better than 5 ppm/°C or 10 ppm/°C when it's cold.

The values shown in this circuit are generally optimum for ±12V to ±16V regulated supplies but any stable supplies between ±4V and ±22V would be usable, after changing a few component values.

National Semiconductor

APPENDIX H: Standard Resistance Values

The standard 1% (and ½%) resistor values are recommended for ease of design and for best availability when designing precision analog circuits.

Standard Resistance Values for the 10-to-100 Decade

Resistance Tolerance (+%)																				
0.1			0.1			0.1			0.1			0.1			0.1					
0.25	1	2	0.25	1	2	0.25	1	2	0.25	1	2	0.25	1	2	0.25	1	2			
0.5		5	0.5		5	0.5		5	0.5		5	0.5		5	0.5		5			
10.0	**10.0**	10	14.7	**14.7**	—	21.5	**21.5**	—	31.6	**31.6**	—	46.4	**46.4**	—	68.1	**68.1**	68			
10.1	—	—	14.9	—	—	21.8	—	—	32.0	—	—	47.0	—	47	69.0	—	—			
10.2	**10.2**	—	15.0	**15.0**	15	22.1	**22.1**	—	32.4	**32.4**	—	47.5	**47.5**	—	69.8	**69.8**	—			
10.4	—	—	15.2	—	—	22.3	—	22	32.8	—	—	48.1	—	—	70.6	—	—			
10.5	**10.5**	—	15.4	**15.4**	—	22.6	**22.6**	—	33.2	**33.2**	33	48.7	**48.7**	—	71.5	**71.5**	—			
10.6	—	—	15.6	—	—	22.9	—	—	33.6	—	—	49.3	—	—	72.3	—	—			
10.7	**10.7**	—	15.8	**15.8**	—	23.2	**23.2**	—	34.0	**34.0**	—	49.9	**49.9**	—	73.2	**73.2**	—			
10.9	—	—	16.0	—	16	23.4	—	—	34.4	—	—	50.5	—	—	74.1	—	—			
11.0	**11.0**	11	16.2	**16.2**	—	23.7	**23.7**	—	34.8	**34.8**	—	51.1	**51.1**	51	75.0	**75.0**	75			
11.1	—	—	16.4	—	—	24.0	—	24	35.2	—	—	51.7	—	—	75.9	—	—			
11.3	**11.3**	—	16.5	**16.5**	—	24.3	**24.3**	—	35.7	**35.7**	—	52.3	**52.3**	—	76.8	**76.8**	—			
11.4	—	—	16.7	—	—	24.6	—	—	36.1	—	36	53.0	—	—	77.7	—	—			
11.5	**11.5**	—	16.9	**16.9**	—	24.9	**24.9**	—	36.5	**36.5**	—	53.6	**53.6**	—	78.7	**78.7**	—			
11.7	—	—	17.2	—	—	25.2	—	—	37.0	—	—	54.2	—	—	79.6	—	—			
11.8	**11.8**	—	17.4	**17.4**	—	25.5	**25.5**	—	37.4	**37.4**	—	54.9	**54.9**	—	80.6	**80.6**	—			
12.0	—	12	17.6	—	—	25.8	—	—	37.9	—	—	56.6	—	—	81.6	—	—			
12.1	**12.1**	—	17.8	**17.8**	—	26.1	**26.1**	—	38.3	**38.3**	—	56.2	**56.2**	56	82.5	**82.5**	82			
12.3	—	—	18.0	—	18	26.4	—	—	38.8	—	—	56.9	—	—	83.5	—	—			
12.4	**12.4**	—	18.2	**18.2**	—	26.7	**26.7**	—	39.2	**39.2**	39	57.6	**57.6**	—	84.5	**84.5**	—			
12.6	—	—	18.4	—	—	27.1	—	27	39.7	—	—	58.3	—	—	85.6	—	—			
12.7	**12.7**	—	18.7	**18.7**	—	27.4	**27.4**	—	40.2	**40.2**	—	59.0	**59.0**	—	86.6	**86.6**	—			
12.9	—	—	18.9	—	—	27.7	—	—	40.7	—	—	59.7	—	—	87.6	—	—			
13.0	**13.0**	13	19.2	**19.1**	—	28.0	**28.0**	—	41.2	**41.2**	—	60.4	**60.4**	—	88.7	**88.7**	—			
13.2	—	—	19.3	—	—	28.4	—	—	41.7	—	—	61.2	—	—	89.8	—	—			
13.3	**13.3**	—	19.6	**19.6**	—	28.7	**28.7**	—	42.2	**42.2**	—	61.9	**61.9**	62	90.9	**90.9**	91			
13.5	—	—	19.8	—	—	29.1	—	—	42.7	—	—	62.6	—	—	92.0	—	—			
13.7	**13.7**	—	20.0	**20.0**	20	29.4	**29.4**	—	43.2	**43.2**	43	63.4	**63.4**	—	93.1	**93.1**	—			
13.8	—	—	20.3	—	—	29.8	—	—	43.7	—	—	64.2	—	—	94.2	—	—			
14.0	**14.0**	—	20.5	**20.5**	—	30.1	**30.1**	30	44.2	**44.2**	—	64.9	**64.9**	—	95.3	**95.3**	—			
14.2	—	—	20.8	—	—	30.5	—	—	44.8	—	—	65.7	—	—	96.5	—	—			
14.3	**14.3**	—	21.0	**21.0**	—	30.9	**30.9**	—	45.3	**45.3**	—	66.5	**66.5**	—	97.6	**97.6**	—			
14.5	—	—	21.3	—	—	31.2	—	—	45.9	—	—	67.3	—	—	98.8	—	—			

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 12.1 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21 kΩ, etc.

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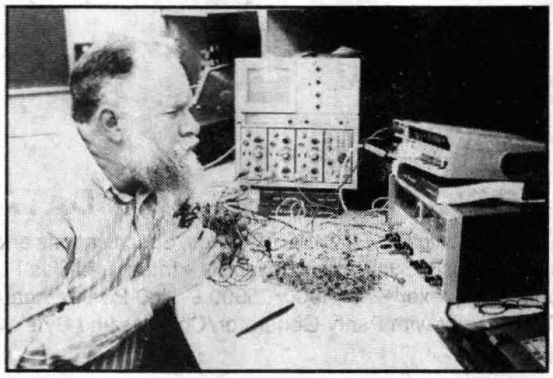

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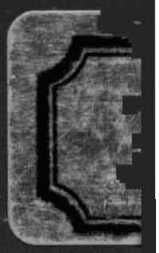

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